RZ/A1H Group, RZ/A1M Group

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Features

This LSI has following features.

■ CPU (Arm® Cortex®-A9)

- Operating frequency: 400 MHz
- Single-precision/double-precision FPU
- Arm® NEON™

■ On-chip memory

- 10 MB (RZ/A1H)
- 5 MB (RZ/A1M)

■ Main graphics and camera input functions

- Video display controller (VDC5): 2 channels
  - LCD output: Max. WXGA
  - Screen superimposition: 4 layers
  - Video input: Max. XGA (CVBS analog input supported)
- CMOS camera input (CEU): 1 channel
- PAL/NTSC decoder (DVDEC): 2 channels
- Distortion compensation unit (IMR): 1 channel
- Open VG accelerator: 1 channel
- JPEG coding engine: 1 channel

■ Main memory interface functions

- NOR flash, SDRAM, NAND flash
- QSPI serial flash: 2 channels (ability to run stored programs directly)
- SD host interface: 2 channels
- MMC host interface: 1 channel

■ Main communication functions

- USB 2.0 High Speed: 2 channels (Host/Function switchable)
- 10M/100M EtherMAC: 1channel
- SCIF: 8 channels
- I2C: 4 channels
- SSI: 6 channels
- RSPI: 5 channels
- Ethernet AVB: 1 channel
- CAN: 5 channels

1. Overview

1.1 Outline of Specification

Table 1.1 Features of RZ/A1H and RZ/A1M

Items	Specification
CPU	• Arm Cortex-A9 processor • Maximum operating frequency: 400 MHz • Instruction cache size: 32 Kbytes • Data cache size: 32 Kbytes (write-back algorithm) • TLB entries: 128 entries • Jazelle® architecture extension: Full implementation • Media processing engine with NEON™ technology
L2 cache memory	• Arm CoreLink™ Level 2 Cache Controller L2C-310 • Operating frequency: 133 MHz • Cache size: 128 Kbytes
Interrupt controller	• Arm PrimeCell® Generic Interrupt Controller (PL390) • External interrupt pins (NMI, IRQ7 to IRQ0, and TINT170 to TINT0) • On-chip peripheral interrupts: Priority level set for each module • 32 priority levels available
Bus state controller	• Address space divided into six areas (0 to 5), each a maximum of 64 Mbytes • The following features settable for each area independently —Bus size (8, 16, or 32 bits): Available sizes depend on the area. —Number of access wait cycles (different wait cycles can be specified for read and write access cycles in some areas) —Idle wait cycle insertion (between the same area access cycles or different area access cycles) —Specifying the memory to be connected to each area enables direct connection to SRAM, SRAM with byte selection, SDRAM, and burst ROM (clocked synchronous or asynchronous). The address/data multiplexed I/O (MPX) interface is also available. • Outputs a chip select signal ($\overline{CS0}$ to $\overline{CS5}$) according to the target area ($\overline{CS}$ assert or negate timing can be selected by software) • SDRAM refresh • Auto refresh or self refresh mode selectable • SDRAM burst access
Direct memory access controller	• Sixteen channels; external requests are available for one of them. • Can be activated by on-chip peripheral modules. • A specific DMA transfer interval can be specified to adjust the bus occupancy. • Link mode (DMA transfer under descriptor control) supported • Transfer information can be automatically reloaded.
Clock pulse generator	• Clock mode: Input clock can be selected from external input (EXTAL or USB_X1) or crystal resonator. • Input clock can be multiplied by 32 (max.) by the internal PLL circuit. • Peak values of EMI noise can be reduced by the on-chip SSCG circuit. • Five types of clocks generated: —CPU clock (Iφ): Maximum 400.00 MHz —Image processing clock (Gφ): Maximum 266.67 MHz —Internal bus clock (Bφ): Maximum 133.33 MHz —Peripheral clock 1 (P1φ): Maximum 66.67 MHz —Peripheral clock 0 (P0φ): Maximum 33.33 MHz
Watchdog timer	• On-chip one-channel watchdog timer • A counter overflow can reset the LSI.
Power-down modes	• Four power-down modes provided to reduce the power consumption in this LSI —Sleep mode —Software standby mode —Deep standby mode —Module standby mode

Items	Specification
Multi-function timer pulse unit 2	• Maximum 16 lines of pulse inputs/outputs based on five channels of 16-bit timers • 18 output compare and input capture registers • Input capture function • Pulse output modes • Toggle, PWM, complementary PWM, and reset-synchronized PWM modes • Synchronization of multiple counters • Complementary PWM output mode —Non-overlapping waveforms output for 3-phase inverter control —Automatic dead time setting —0% to 100% PWM duty value specifiable —A/D converter start request delaying function —Interrupt skipping at crest or trough • Reset-synchronized PWM mode Three-phase PWM waveforms in positive and negative phases can be output with a required duty value. • Phase counting mode Two-phase encoder pulse counting available
OS timer	• Two-channel 32-bit counters • Two operating modes: —Interval timer mode —Free-running comparison mode • DMA transfer request or interrupt request can be issued when a compare match occurs.
Realtime clock	• Internal clock, calendar function, alarm function • Interrupts can be generated at intervals of 1/64 s by the 32.768-kHz or 4-MHz on-chip crystal oscillator.
Serial communication interface with FIFO	• Eight channels • Clock synchronous mode or asynchronous mode selectable • Simultaneous transmission and reception (full-duplex communication) supported • Dedicated baud rate generator • Separate 16-byte FIFO registers for transmission and reception • Modem control function (channels 1, 5, and 7 in asynchronous mode)
Serial communication interface	• Two channels • Clock synchronous mode, asynchronous mode, or smart card interface mode is selectable. • Simultaneous transmission and reception (full-duplex communication) supported • Dedicated baud rate generator • LSB first/MSB first selectable • Modem control function • Encoding and decoding of IrDA communications waveforms in accord with version 1.0 of the IrDA standard (on channel 0)
Renesas serial peripheral interface	• Five channels • SPI operation • Master mode and slave mode selectable • Programmable bit length, clock polarity, and clock phase can be selected. • Consecutive transfers • MSB first/LSB first selectable • Maximum transfer rate: 33.33 Mbps
SPI multi I/O bus controller	• Two channels • Up to two serial flash memories with multiple I/O bus sizes (single/dual/quad) can be connected. • External address space read mode (built-in read cache) • SPI operating mode • Clock polarity and clock phase can be selected. • MSB first/LSB first selectable • Maximum transfer rate: 533.33 Mbps (SDR transfer, with two serial flash memories connected)
I^2C bus interface	• Four channels • Master mode and slave mode supported • Support for 7-bit and 10-bit slave address formats • Support for multi-master operation • Timeout detection

Items	Specification
Serial sound interface	• Six-channel bidirectional serial transfer • Duplex communication (channels 0, 1, 3, and 5) • Support of various serial audio formats • Support of master and slave functions • Generation of programmable word clock and bit clock • Multi-channel formats • Support of 8, 16, 18, 20, 22, 24, and 32-bit data formats • Support of eight-stage FIFO for transmission and reception • Support of TDM mode • Support of WS continue mode in which the SSIWS signal is not stopped. • Support of direct transfer to the SCUX module • A change of the sampling frequency can be detected.
Media local bus	• Conforms with version 2.0 of the MediaLB standard. Data transfer at up to 50 Mbps is possible.
SCUX	• Sampling rate conversion —Asynchronous or synchronous sampling rate conversion is possible. —Sampling rate (synchronous mode) Note: The selectable sampling rates depend on the number of used channels and rate ratio. Input [kHz]: 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, 48, 64, 88.2, or 96 is selectable. Output [kHz]: 8, 16, 24, 44.1, 48, or 96 is selectable. —Sampling rate (asynchronous mode) Note: The selectable sampling rates depend on the number of used channels and rate ratio. Input/output [kHz]: 1 to 96 —Data format: 16 or 24 bits • Digital volume and mute functions —The digital volume can be set within the range from a multiple of 0 to 8 (−120 to 18 dB) —Volume ramping supports soft mute, fade-in, and fade-out. —The zero crossing mute function can apply muting at zero-crossing points. • Mixer —Data of two to four source systems can be mixed (added together) into one system. —The ratio to add the sources can be set. —Direct transfer to the serial sound interface module is supported.
CAN interface	• Five channels • ISO11898-1 compliant • Message buffer: —Up to 64 5-channel receive message buffers: shared among all channels. —16 transmit message buffers per channel
IEBus™ controller	• Conforms with the IEBus protocol (communication modes 1 and 2). • Transfer rates: approximately 18 kbps (in communication mode 1), approximately 27 kbps (in communication mode 2) • Maximum numbers of bytes for transfer: 32 bytes/frame (in communication mode 1), 128 bytes/frame (in communication mode 2) • Operating clock: 8 MHz Note: Input of peripheral clock 0 (P0φ) running at 32 MHz is required.
Renesas SPDIF interface	• Support of IEC60958 standard (stereo and consumer use modes only) • Sampling frequencies of 32 kHz, 44.1 kHz, and 48 kHz • Audio word sizes of 16 to 24 bits per sample • Biphase mark encoding • Double buffered data • Parity encoded serial data • Simultaneous transmit and receive • Receiver autodetects IEC 61937 compressed mode data.
CD-ROM decoder	• Support of five formats: Mode 0, mode 1, mode 2, mode 2 form 1, and mode 2 form 2 • Sync codes detection and protection • (Protection: When a sync code is not detected, it is automatically inserted.) • Descrambling • ECC correction —P, Q, PQ, and QP correction —PQ or QP correction can be repeated up to three times. • EDC check Performed before and after ECC • Mode and form are automatically detected. • Link sectors are automatically detected. • Buffering data control Buffering CD-ROM data including Sync code is transferred in specified format, after the data is descrambled, corrected by ECC, and checked by EDC.

Items	Specification
LIN interface	• Two channels • Conforms with revisions 1.3, 2.0, 2.1, and 2.2 of the LIN protocol and SAEJ 2062. • Master mode supported
Ethernet controller	• Conforms with the Ethernet or the IEEE802.3 MAC (Media Access Control) layer standard • MAC function Constructs/deconstructs data frames (frame format conforming to IEEE802.3, 2000 Edition) Supports transfer at 10 and 100 Mbps Supports full-duplex mode Flow control conforming to IEEE802.3x Supports an MII (Media Independent Interface) for connection to a PHY interface in conformance with IEEE 802.3 Upward protocol support (checksum) function • E-DMAC (Direct Memory Access Controller for Ethernet controller) function
EthernetAVB	• Conforms with the Ethernet or the IEEE802.3 MAC (Media Access Control) layer standard • MAC function Constructs/deconstructs data frames (frame format conforming to IEEE802.3, 2000 Edition) Supports transfer at 100 Mbps Supports full-duplex mode Flow control conforming to IEEE802.3x Supports an MII (Media Independent Interface) for connection to a PHY interface in conformance with IEEE 802.3 Upward protocol support (checksum) function • AVB-DMAC (DMAC dedicated to EthernetAVB) function AVB-DMAC conforms with the following 3 standards; IEEE802.1AS (Clock Synchronization Protocol), IEEE802.1Qav (Realtime Transfer Protocol) and IEEE802.1Qat (Bandwidth Reservation Protocol)
NAND flash memory controller	• Direct-connected memory interface with NAND-type flash memory • Command access mode • Interrupt request and DMA transfer request • Supports flash memory requiring 5-byte addresses (2 Gbits and more)
USB 2.0 host/function module	• Two channels • Conforms to the Universal Serial Bus Specification Revision 2.0 • 480-Mbps, 12-Mbps, and 1.5-Mbps transfer rates provided (host mode) • 480-Mbps and 12-Mbps transfer rates provided (function mode) • On-chip 8-Kbyte RAM as communication buffers
Digital video decoder	• Two channels • Video input Composite video input (CVBS) • A/D converter for video signal input VIN1 and VIN2 pin input selection Low-pass filter (LPF) Sync tip clamp Programmable gain amplifier (PGA) (0 to 6.021 dB) 10-bit precision pipelined A/D converter • Sync separation Noise reduction LPF, auto level control sync slicer, horizontal auto frequency control (AFC), vertical count-down, interlace detection, auto gain control (AGC)/peak limiter control • Y/C separation NTSC 2D, PAL 2D, and SECAM 1D supported. • Chroma-key decoding NTSC, PAL, and SECAM supported. Color killer, auto color control (ACC), TINT correction, R-Y axis correction • Digital clamp Pedestal clamp (Y), center clamp (Cb/Cr), noise detection • Adjustment of output gain Contrast: 0 to approximately 2 times Color (Cb/Cr independently): 0 to approximately 2 times

Items	Specification
Video display controller 5	• Two channels • Video input interface: One channel can be selected from the followings. BT601, BT656 format (NTSC/PAL) input: Input clock: 27 MHz/54 MHz Digital pin input (channel 0): YCbCr422, YCbCr444, RGB888, RGB666, RGB565 Digital pin input size: Maximum input video image size to be set*: 1440 pixels × 1024 lines (horizontal × vertical) Note:*Depends on the AC characteristics of the connected device. Examples of input video image size : WXGA (1280 × 768) XGA (1024 × 768) SVGA (800 × 600), WVGA (800 × 480), VGA (640 × 480), WQVGA (480 × 240), QVGA (320 × 240, 240 × 320) Composite video (CVBS) signal input decoded by the digital video decoder • Input video control Horizontal noise reduction (NR), brightness adjustment and contrast adjustment using matrix operation • Scaling control Vertical and horizontal scaling up or down of input video possible at a desired ratio (scaling up of graphics also possible) Scaling up ratio: 1 to 8; scaling down ratio: 1/8 to 1 Interpolation: Hold or linear selectable 2D IP conversion: 2D IP conversion through separately setting the initial phases for the top and bottom fields • Video recording Output pixel format: YCbCr444, YCbCr422, RGB888, RGB565 Output field rate: 1/1, 1/2, 1/4, 1/8 Rotation: Horizontal mirroring and 90/180/270 degree rotation for YCbCr422 and RGB565 Maximum video image size to be stored: ×1 size of input video image • Output video control Black stretch: Black area stretched according to Y signal state Enhancer capability: LTI (transient improvement) and sharpness (contour emphasis) for Y signal

Items	Specification
Video display controller 5	• Four graphics layers (two of them also for input video) Available input pixel formats 1 bit/pixel: CLUT1 4 bits/pixel: CLUT4 8 bits/pixel: CLUT8 16 bits/pixel: YCbCr422 (graphics layers 0 and 1), RGB565, ARGB1555, RGBA5551, ARGB4444 32 bits/pixel: ARGB8888, RGBA8888, RGB888, YCbCr444 (graphics layers 0 and 1) • Blending of two input video images Two input video images superimposed by alpha blending over a rectangular area can be output. • Superimposition Alpha blending in a rectangular area: Input video, layer 1, and layer 2 blended according to the transparency percentage α (fade-in and fade-out function available) Chroma key function: Mixing based on transparency percentage α using the specified RGB and CLUT value Pixel-base alpha blending: Alpha blending for each pixel based on transparency percentage α Generation of output video images Video images superimposed on graphics layers can be output to memory. • Panel output control Panel output correction: Brightness adjustment and contrast adjustment, gamma correction, panel dithering TCON: Various timing output for LCD panel driving provided by a total of seven vertical and horizontal panel driver signals Panel output pixel format: RGB888, RGB666, RGB565, serial RGB Output video image size: Maximum output video image size to be set*: 1999 pixels × 2035 lines (horizontal × vertical) Note:*Depends on the AC characteristics of the display panel. Examples of output video image size: WXGA (1280 × 768) XGA (1024 × 768) SVGA (800 × 600), WVGA (800 × 480), VGA (640 × 480), WQVGA (480 × 240), QVGA (320 × 240, 240 × 320)
Dynamic range compression	• Two channels • Contrast adjustment of captured data Contrast expansion processing optimized per region of the image
Image renderer (IMR-LS2)	• Two channels • Refers to the video captured data as two-dimensional texture data and draws a shape by performing texture mapping for an arbitrary shape divided into triangular objects. • Display list system • Drawing functions Texture mapping, bilinear filtering, automatic coordinate generation (and relative coordinate input) • Instruction system Draw instruction: TRI for drawing a triangle Control instructions: TRAP, INT, NOP, SYNCM, SYNCW, WTL, and WTS • Drawing space Destination coordinates: 0 ≤ X ≤ 2,047, 0 ≤ Y ≤ 2,047 Source coordinates: 0 ≤ u ≤ 1,439, 0 ≤ v ≤ 1,023
Image renderer for display (IMR-LSD)	• Refers to the output video image data from the video display controller 5 (channel 0) as two-dimensional texture data and draws shapes by performing texture mapping for an arbitrary shape divided into triangular objects. • Display list system • Drawing functions Texture mapping, bilinear filtering, automatic coordinate generation (and relative coordinate input) • Instruction system Draw instruction: TRI for drawing a triangle Control instructions: TRAP, INT, NOP, SYNCM, SYNCW, WTL, and WTS • Drawing space Destination coordinates: 0 ≤ X ≤ 2,047, 0 ≤ Y ≤ 2,047 Source coordinates: 0 ≤ u ≤ 1,439, 0 ≤ v ≤ 1,023

Items	Specification
Display out comparison unit	• Two channels • Calculates the CRC code of an arbitrary graphics plane and compares it with the pre-calculated CRC code. • Specifies a rectangular area in an arbitrary graphics plane selected from among four graphics planes, one plane of the graphics data obtained after α blending, or one plane of the data read from the output video image generator of the video display controller 5. • Pixel format 32 bits/pixel: ARGB8888/RGB888/RGB666 16 bits/pixel: RGB565
Renesas graphics processor for OpenVG™	• OpenVG™, which is an open 2D vector graphics API, can be processed. • Processes can be accelerated in OpenVG™ stage 2 to stage 8 using the dedicated hardware and programmable shader.
JPEG codec unit	• Compression and decompression method conforming to the JPEG baseline standard within the range described in this document. • Operational precision: Conforming to JPEG Part 2, ISO-IEC10918-2 • Pixel format: Compression: YCbCr422 Decompression: YCbCr444, YCbCr422, YCbCr411, YCbCr420 Output pixel format to the buffer: YCbCr422, ARGB8888, RGB565 • Four quantization tables provided • Four Huffman tables provided (two tables for AC coefficients and two tables for DC coefficients) • Markers supported: SOI, SOF0, SOS, DQT, DHT, DRI, RSTm, and EOI • Image data rate: Max. 133.33 Mbytes/s (at 66.67-MHz operation)
Capture engine unit	• Examples of input video image size : 5 megapixels (2,560 × 1,920) 3 megapixels (2,048 × 1,536) 2 megapixels (1,632 × 1,224) UXGA (1,600 × 1,200) SXGA (1) (1,280 × 1,024) SXGA (2) (1,280 × 960) WXGA (1,280 × 768) XGA (1,024 × 768) SVGA (800 × 600) WVGA (800 × 480) VGA (640 × 480) WQVGA (480 × 240) QVGA (320 × 240, 240 × 320) Note: Depends on the AC characteristics of the connected device, frame rate of the connected device, and transfer speed to the destination RAM. • Input format: 8- or 16-bit YCbCr422 binary data • Memory output format: YCbCr422, YCbCr420 Note: The captured data cannot be displayed via the video display controller 5 because the Y data and CbCr data are split when written to memory.
Pixel format converter	• Two channels • Brightness adjustment, gain adjustment, and YCbCr and RGB mutual conversion. • Input pixel data: RGB888, RGB565, YCbCr422 • Output pixel data: ARGB8888, RGB565, YCbCr422
Sound generator	• Four channels • Capable of adjusting sound volume using 8-bit PWM output • Four types of operating clocks (P0φ/2, P0φ/4, P0φ/8, and P0φ/16) can be selected. • Frequency settings in the 25-Hz to 20-kHz range with precision of 1% or less • Automatic attenuator function can be selected.
SD host interface	• Two channels • SD memory I/O card interface (1-/4-bit SD bus) • Error check function: CRC7 (command), CRC16 (data) • Interrupt requests —Card access interrupt —SDIO access interrupt —Card detect interrupt • DMA transfer requests —SD_BUF write —SD_BUF read • Card detection function, write protect supported

Items	Specification
MMC host interface	• Interface to multi-media card (MMC) • Data bus: 1-/4-/8-bit MMC mode • Interrupt requests: card detection, error/time-out, and normal operation • DMA transfer requests: CE_DATA write and CE_DATA read • Card detection function
General I/O ports	• 256-pin: 115 I/Os, 8 inputs with open-drain outputs, and 16 inputs (input only) • 324-pin: 147 I/Os, 8 inputs with open-drain outputs, and 16 inputs (input only) • Input or output can be selected for each bit.
A/D converter	• 12-bit resolution • Eight input channels • Minimum conversion time: 5.0 µs • A/D conversion request by the external trigger or timer trigger
Motor control PWM timer	• Two 10-bit PWM channels, each with eight outputs
Debugging interface	• Arm CoreSight™ architecture • JTAG-standard pin assignment
On-chip RAM	• 10-Mbyte (RZ/A1H) or 5-Mbyte (RZ/A1M) large capacity memory for video display/recording and work (128 Kbytes are used for data retention) • 128-Kbyte memory for data retention (16 Kbytes × 2, 32 Kbytes × 1, 64 Kbytes × 1)
Boot modes	• Five boot modes Boot mode 0: Booting from memory (bus width: 16 bits) connected to the CS0 space Boot mode 1: Booting from memory (bus width: 32 bits) connected to the CS0 space Boot mode 2: — Boot mode 3: Booting from a serial flash memory Boot mode 4: Booting from a NAND flash memory with SD controller Boot mode 5: Booting from a NAND flash memory with MMC controller
Power supply voltage	• Vcc: 1.10 to 1.26 V • PVcc: 3.0 to 3.6 V
Package	• PLBG0256KA-B 256-pin BGA, 11-mm square, 0.5-mm pitch JEITA package code: P-LFBGA256-11×11-0.50 RENESAS code: PLBG0256KA-B • PLQP0256LB-A 256-pin QFP, 28-mm square, 0.4-mm pitch JEITA package code: P-LFQFP256-28×28-0.40 RENESAS code: PLQP0256LB-A • PRBG0324GA-A 324-pin BGA, 19-mm square, 0.8-mm pitch JEITA package code: P-FBGA324-19×19-0.80 RENESAS code: PRBG0324GA-A

1.2 Block Diagram

This LSI has two main buses: the north main bus where peripheral modules are connected and the south main bus where on-chip RAM and external ROM and RAM are connected. Figure 1.1 is a schematic diagram of the internal buses.

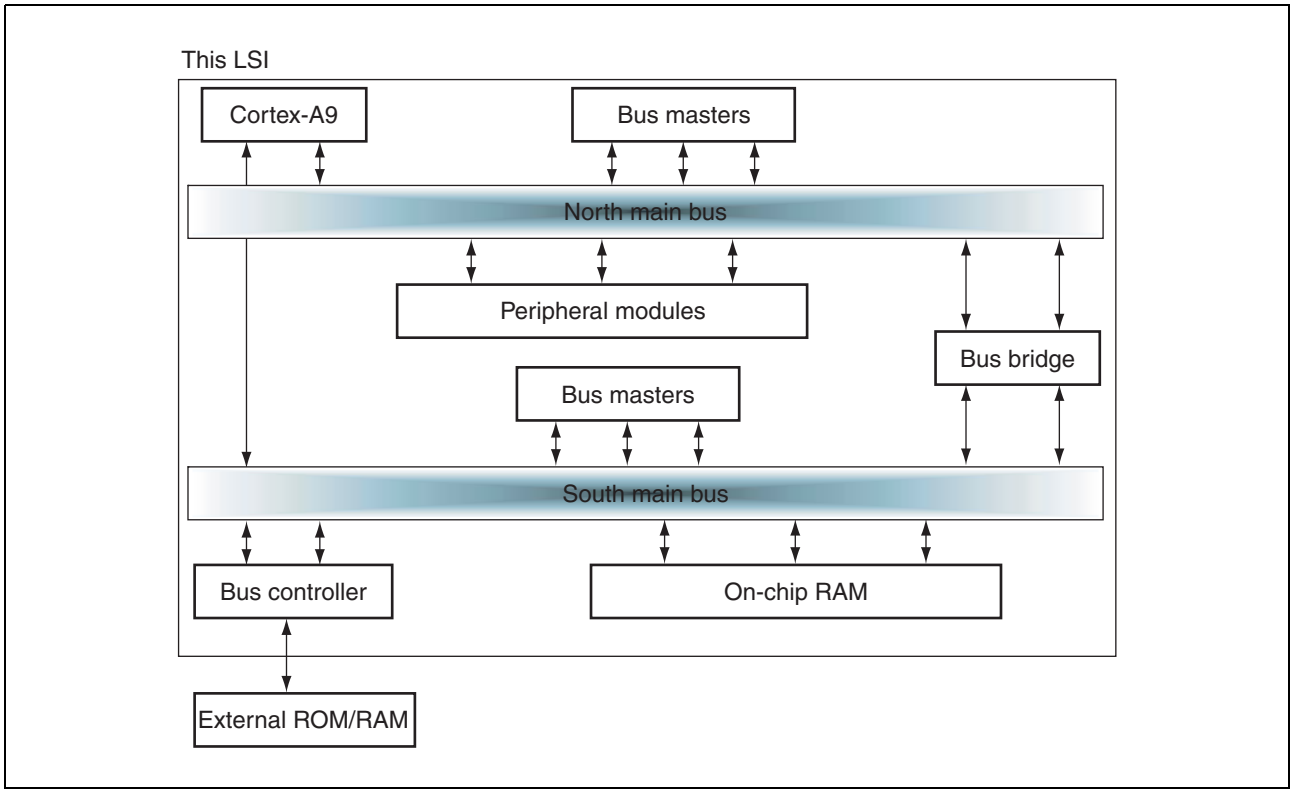


Figure 1.1 Schematic Diagram of LSI Internal Bus

Figure 1.2 shows the schematic diagram of North Main Bus, Figure 1.3 shows the schematic diagram of South Main Bus.

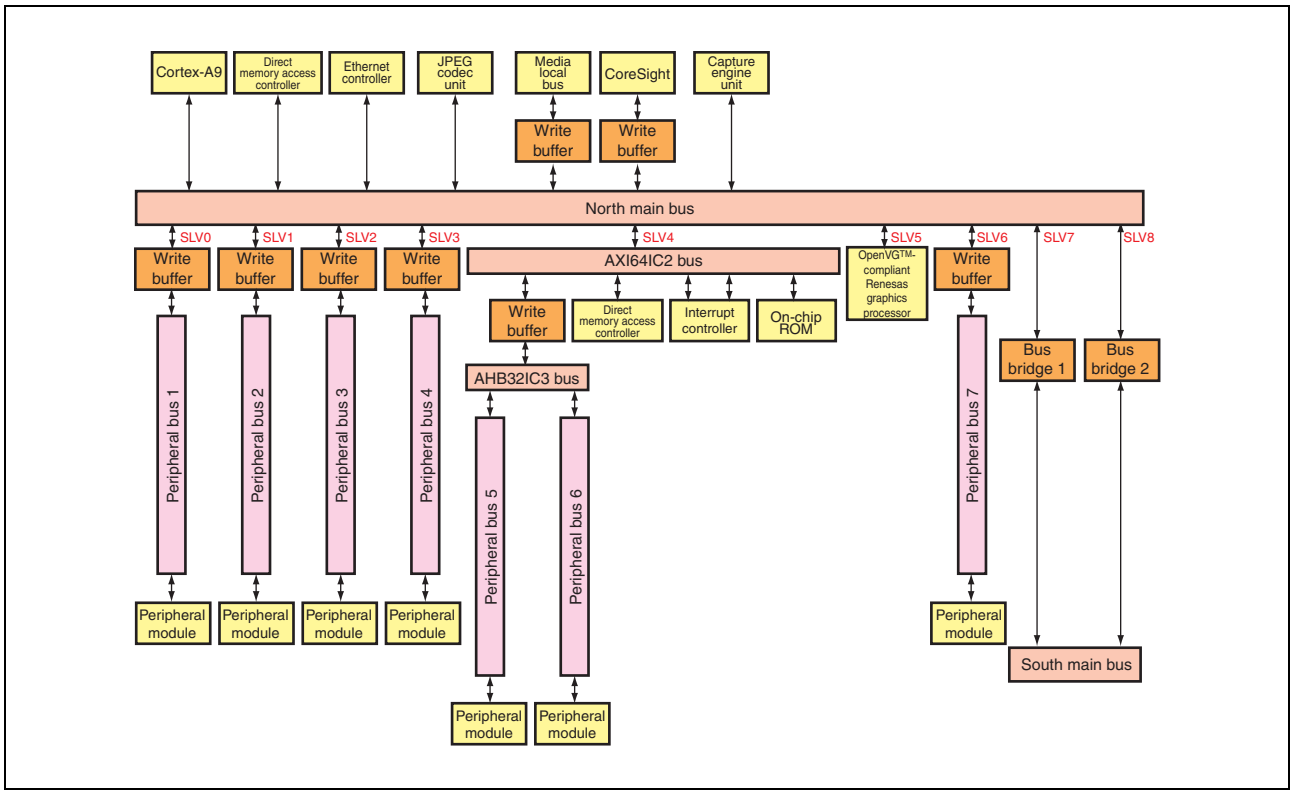


Figure 1.2 North Main Bus Configuration

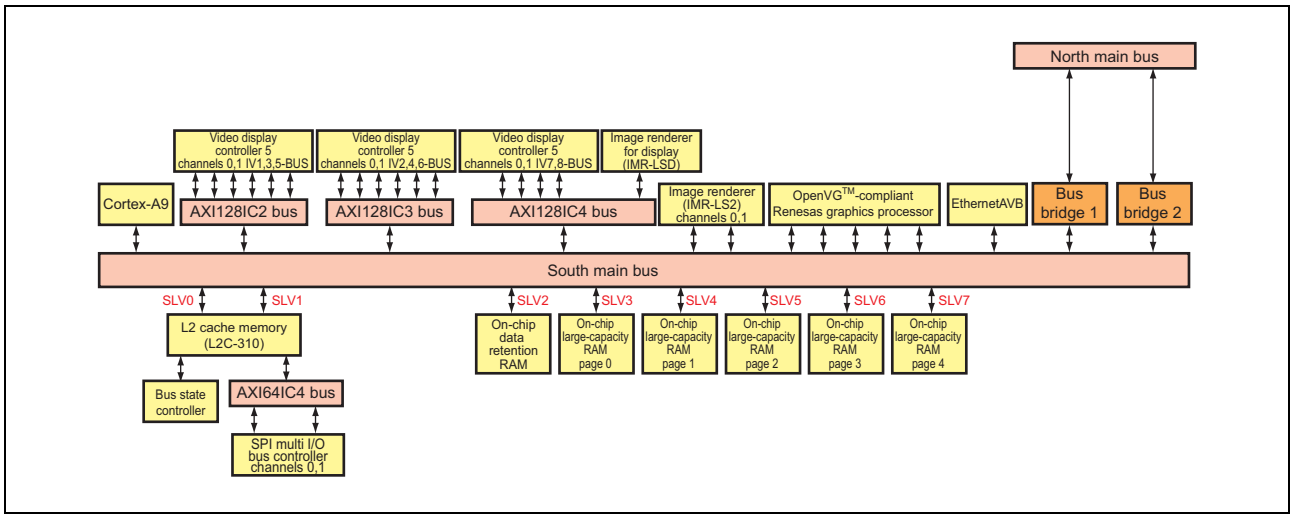


Figure 1.3 South Main Bus Configuration

1.3 Product Lineup

Table 1.2 Product Lineup

Group	Part Number	Temperature Range	Quality Level	Package
RZ/A1H	R7S721000VCBG	-40 to +85°C	Industry usage etc.	PLBG0256KA-B
	R7S721000VCFP		Industry usage etc.	PLQP0256LB-A
	R7S721000VLFP		Car Accessories	
	R7S721001VCBG		Industry usage etc.	PRBG0324GA-A
	R7S721001VLBG		Car Accessories	
RZ/A1M	R7S721010VCBG	-40 to +85°C	Industry usage etc.	PLBG0256KA-B
	R7S721010VCFP		Industry usage etc.	PLQP0256LB-A
	R7S721010VLFP		Car Accessories	
	R7S721011VCBG		Industry usage etc.	PRBG0324GA-A
	R7S721011VLBG		Car Accessories	

2. Pin

2.1 Pin Functions

2.1.1 Pin Function of Functional Blocks

Table 2.1 List of Pin Functions

Classification	Symbol	I/O	Name	Function
Power supply	Vcc	I	Power supply	Power supply pins. All the Vcc pins must be connected to the system power supply. This LSI does not operate correctly if there is a pin left open.
	Vss	I	Ground	Ground pins. All the Vss pins must be connected to the system power supply (0 V). This LSI does not operate correctly if there is a pin left open.
	PVcc	I	Power supply for I/O circuits	Power supply for I/O pins. All the PVcc pins must be connected to the system power supply. This LSI does not operate correctly if there is a pin left open.
	PLLVcc	I	Power supply for PLL	Power supply for the on-chip PLL oscillator.
Clock	EXTAL	I	External clock	Connected to a crystal resonator. An external clock signal may also be input to the EXTAL pin.
	XTAL	O	Crystal	Connected to a crystal resonator.
	CKIO	O	System clock output	Supplies the system clock to external devices.
	AUDIO_CLK	I	External clock for audio	Input pin of external clock for audio. A clock input to the divider is selected from an oscillation clock input on this pin or pins AUDIO_X1 and AUDIO_X2.
	AUDIO_X1	I	Crystal resonator/ external clock for audio	Pins connected to a crystal resonator for audio. An external clock can be input on pin AUDIO_X1. A clock input to the divider is selected from an oscillation clock input on these pins or the AUDIO_CLK pin.
	AUDIO_X2	O		
	AUDIO_XOUT	O	AUDIO_X1 clock output	Output for the on-chip crystal oscillator on AUDIO_X1 or the external clock signal.
	AUDIO_XOUT2	O	AUDIO_X1 divided-by-two clock output	Output for the on-chip crystal oscillator on AUDIO_X1 or the external clock signal after frequency division of the selected signal by two.
	AUDIO_XOUT3	O	AUDIO_X1 divided-by-three clock output	Output for the on-chip crystal oscillator on AUDIO_X1 or the external clock signal after frequency division of the selected signal by three.

Classification	Symbol	I/O	Name	Function
Operating mode control	MD_BOOT2, MD_BOOT1, MD_BOOT0	I	Mode set	Sets the operating mode. Do not change the signal levels on these pins while the $\overline{\text{RES}}$ pin is asserted or until the mode is fixed, after the negation.
	MD_CLK	I	Clock mode set	Sets the clock operating mode. Do not change the signal levels on this pin while the $\overline{\text{RES}}$ pin is asserted or until the mode is fixed, after the negation.
	MD_CLKS	I	SSCG clock mode set	Switches the SSCG circuit on or off. Do not change the signal levels on this pin while the $\overline{\text{RES}}$ pin is asserted or until the mode is fixed, after the negation.
	BSCANP	I	Boundary scan set	Boundary scan setting pin. This pin is set to the high level for a boundary scan and to the low level for normal operation.
System control	$\overline{\text{RES}}$	I	Power-on reset	This LSI enters the power-on reset state when this signal goes low.
	$\overline{\text{WDTOVF}}$	O	Watchdog timer overflow	Outputs an overflow signal from the watchdog timer.
Interrupts	NMI	I	Non-maskable interrupt	Non-maskable interrupt request pin. It is handled as an FIQ exception. Fix it high when not in use.
	IRQ7 to IRQ0	I	Interrupt requests 7 to 0	Maskable interrupt request pins. Level-input or edge-input detection can be selected. When the edge-input detection is selected, the rising edge, falling edge, or both edges can also be selected.
	TINT170 to TINT0	I	Interrupt requests 170 to 0	Maskable interrupt request pins. Detection through input of the high level or a rising edge can be selected.
Address bus	A25 to A0	O	Address bus	Outputs addresses.
Data bus	D31 to D0	I/O	Data bus	Bidirectional data bus.

Classification	Symbol	I/O	Name	Function
Bus control	$\overline{CS5}$ to $\overline{CS0}$	O	Chip select 5 to 0	Chip-select signals for external memory or devices.
	$\overline{RD}$	O	Read	Indicates that data is read from an external device.
	RD/$\overline{WR}$	O	Read/write	Read/write signal.
	$\overline{BS}$	O	Bus start	Bus-cycle start signal.
	$\overline{AH}$	O	Address hold	Address hold timing signal for the device that uses the address/data-multiplexed bus.
	$\overline{WAIT}$	I	Wait	Inserts a wait cycle into the bus cycles during access to the external space.
	$\overline{WE0}$	O	Byte select	Indicates a write access to bits 7 to 0 of data of external memory or device.
	$\overline{WE1}$	O	Byte select	Indicates a write access to bits 15 to 8 of data of external memory or device.
	$\overline{WE2}$	O	Byte select	Indicates a write access to bits 23 to 16 of data of external memory or device.
	$\overline{WE3}$	O	Byte select	Indicates a write access to bits 31 to 24 of data of external memory or device.
	DQMLL	O	Byte select	Selects bits D7 to D0 when SDRAM is connected.
	DQMLU	O	Byte select	Selects bits D15 to D8 when SDRAM is connected.
	DQMUL	O	Byte select	Selects bits D23 to D16 when SDRAM is connected.
	DQMUU	O	Byte select	Selects bits D31 to D24 when SDRAM is connected.
	$\overline{RAS}$	O	RAS	Connected to the $\overline{RAS}$ pin when SDRAM is connected.
	$\overline{CAS}$	O	CAS	Connected to the $\overline{CAS}$ pin when SDRAM is connected.
	CKE	O	CK enable	Connected to the CKE pin when SDRAM is connected.
Direct memory access controller	DREQ0	I	DMA-transfer request	Input pin to receive external requests for DMA transfer.
	DACK0	O	DMA-transfer request accept	Output pin for signals indicating acceptance of external requests from external devices.
	TEND0	O	DMA-transfer end output	Output pin for DMA transfer end.

Classification	Symbol	I/O	Name	Function
Multi-function timer pulse unit 2	TCLKA, TCLKB, TCLKC, TCLKD	I	Timer clock input	External clock input pins for the timer.
	TIOC0A, TIOC0B, TIOC0C, TIOC0D	I/O	Input capture/ output compare (channel 0)	The TGRA_0 to TGRD_0 input capture input/output compare output/PWM output pins.
	TIOC1A, TIOC1B	I/O	Input capture/ output compare (channel 1)	The TGRA_1 and TGRB_1 input capture input/output compare output/PWM output pins.
	TIOC2A, TIOC2B	I/O	Input capture/ output compare (channel 2)	The TGRA_2 and TGRB_2 input capture input/output compare output/PWM output pins.
	TIOC3A, TIOC3B, TIOC3C, TIOC3D	I/O	Input capture/ output compare (channel 3)	The TGRA_3 to TGRD_3 input capture input/output compare output/PWM output pins.
	TIOC4A, TIOC4B, TIOC4C, TIOC4D	I/O	Input capture/ output compare (channel 4)	The TGRA_4 to TGRD_4 input capture input/output compare output/PWM output pins.
Realtime clock	RTC_X1	I	Crystal resonator for realtime clock/ external clock	Connected to 32.768-kHz crystal resonator. The RTC_X1 pin can also be used to input an external clock.
	RTC_X2	O		
	RTC_X3	I	Crystal resonator for realtime clock/ external clock	Connected to 4-MHz crystal resonator. The RTC_X3 pin can also be used to input an external clock.
	RTC_X4	O		
Serial communication interface with FIFO	TxD7 to TxD0	O	Transmit data	Data output pins.
	RxD7 to RxD0	I	Receive data	Data input pins.
	SCK7 to SCK0	I/O	Serial clock	Clock input/output pins.
	$\overline{\text{RTS7}}$, $\overline{\text{RTS5}}$, $\overline{\text{RTS1}}$	I/O	Transmit request	Modem control pins.
	$\overline{\text{CTS7}}$, $\overline{\text{CTS5}}$, $\overline{\text{CTS1}}$	I/O	Transmit enable	Modem control pins.
Serial communication interface	SCI_SCK1, SCI_SCK0	I/O	Serial clock	Clock input/output pins.
	SCI_TXD1, SCI_TXD0	O	Transmit data	Data output pins.
	SCI_RXD1, SCI_RXD0	I	Receive data	Data input pins.
	$\overline{\text{SCI\_CTS1}}$/$\overline{\text{RTS1}}$, $\overline{\text{SCI\_CTS0}}$/$\overline{\text{RTS0}}$	I/O	Transmit and receive start control	I/O pins for controlling the start of transmission and reception.
Renesas serial peripheral interface	MOSI4 to MOSI0	I/O	Data	Data I/O pins.
	MISO4 to MISO0	I/O	Data	Data I/O pins.
	RSPCK4 to RSPCK0	I/O	Clock	Clock I/O pins.
	SSL40, SSL30, SSL20, SSL10, SSL00	I/O	Slave select	Slave select I/O pins.

Classification	Symbol	I/O	Name	Function
SPI multi I/O bus controller	SPBCLK_1, SPBCLK_0	O	Clock	Clock output pins.
	SPBSSL_1, SPBSSL_0	O	Slave select	Slave select output pins.
	SPBMO0_0/SPBIO00_0, SPBMI0_0/SPBIO10_0, SPBIO20_0, SPBIO30_0, SPBMO1_0/SPBIO01_0, SPBMI1_0/SPBIO11_0, SPBIO21_0, SPBIO31_0	I/O	Data	Data I/O pins for channel 0.
	SPBMO0_1/SPBIO00_1, SPBMI0_1/SPBIO10_1, SPBIO20_1, SPBIO30_1, SPBMO1_1/SPBIO01_1, SPBMI1_1/SPBIO11_1, SPBIO21_1, SPBIO31_1	I/O	Data	Data I/O pins for channel 1.
I^2C bus interface	RIIC3SCL to RIIC0SCL	I/O	Serial clock pin	Serial clock I/O pins.
	RIIC3SDA to RIIC0SDA	I/O	Serial data pin	Serial data I/O pins.
Serial sound interface	SSITxD5, SSITxD3, SSITxD1, SSITxD0	O	Data output	Serial data output pin.
	SSIRxD5, SSIRxD3, SSIRxD1, SSIRxD0	I	Data input	Serial data input pin.
	SSIDATA4, SSIDATA2	I/O	Data I/O	Serial data I/O pins.
	SSISCK5 to SSISCK0	I/O	SSI clock I/O	I/O pins for serial clocks.
	SSIWS5 to SSIWS0	I/O	SSI clock LR I/O	I/O pins for word selection.
Media local bus	MLB_CLK	I	Clock input	MediaLB clock input pin.
	MLB_SIG	I/O	Signal information I/O	MediaLB signal information I/O pin.
	MLB_DAT	I/O	Data I/O	MediaLB data I/O pin.
CAN interface	CAN_CLK	I	Clock source for CAN communication	Clock source for CAN communication.
	CAN4TX to CAN0TX	O	CAN bus transmit data	Output pins for transmit data on the CAN bus.
	CAN4RX to CAN0RX	I	CAN bus receive data	Input pins for receive data on the CAN bus.
IEBus™ controller	IETxD	O	IEBus™ controller transmit data	Output pin for transmit data on IEBus™ controller.
	IERxD	I	IEBus™ controller receive data	Input pin for receive data on IEBus™ controller.
Renesas SPDIF interface	SPDIF_OUT	O	Output data	Transmit data output pin.
	SPDIF_IN	I	Input data	Receive data input pin.
LIN interface	RLIN31TX, RLIN30TX	O	Output data	Transmit data output pins.
	RLIN31RX, RLIN30RX	I	Input data	Receive data input pins.

Classification	Symbol	I/O	Name	Function
Ethernet controller, EthernetAVB Note: Regarding the switching of pin functions between Ethernet controller and EthernetAVB, refer to section 54, Ports, in the RZ/A1H Group, RZ/A1M Group User's Manual.	ET_TXCLK	I	Transmit clock	Clock pin for transmission.
	ET_TXEN	O	Transmit enable	Transmit data enable pin
	ET_TXD3 to ET_TXD0	O	Transmit data	MII transmit data pins.
	ET_COL	I	Collision detection	Collision detection pin.
	ET_TXER	O	Transmit error	Transmit error output pin.
	ET_RXCLK	I	Receive clock	Receive clock pin
	ET_RXDV	I	Receive enable	Receive data enable pin
	ET_RXD3 to ET_RXD0	I	Receive data	MII receive data pins.
	ET_RXER	I	Receive error	Receive error input pin.
	ET_CRS	I	Carrier detection	Carrier detection pin.
	ET_MDC	O	Management data clock	Clock pin for information transfer via MDIO.
	ET_MDIO	I/O	Management data I/O	Bidirectional pin for exchange of management data
EthernetAVB	AVB_CAPTURE	I	Timer capture	Capturing input pin for AVTP presentation timer
	AVB_GPTP_EXTERN	I	gPTP timer external clock	External clock pin for gPTP timer
NAND flash memory controller	FALE	O	Flash memory address latch enable	Asserted for address output and negated for data I/O.
	$\overline{\text{FRE}}$	O	Flash memory read enable	Reads data at falling edge.
	$\overline{\text{FCE}}$	O	Flash memory chip enable	Enables the flash memory connected to this LSI.
	FCLE	O	Flash memory command latch enable	Asserted at command output.
	FRB	I	Flash memory ready/ busy	High level indicates ready state and low level indicates busy state.
	$\overline{\text{FWE}}$	O	Flash memory write enable	Flash memory latches commands, addresses, and data at falling edge.
	NAF7 to NAF0	I/O	Flash memory data	Data I/O pins.
USB 2.0 host/ function module	DP1, DP0	I/O	USB 2.0 host/function module D+ data	D+ data pins for USB 2.0 host/function module bus.
	DM1, DM0	I/O	USB 2.0 host/function module D– data	D– data pins for USB 2.0 host/function module bus.
	VBUS1, VBUS0	I	VBUS input	Connected to Vbus on USB 2.0 host/ function module bus.
	REFRIN	I	Reference input	Connected to USBAPVss via 5.6-kΩ ± 1% resistance. (QFP package) Connected to Vss via 5.6-kΩ ± 1% resistance. (BGA package)

Classification	Symbol	I/O	Name	Function
USB 2.0 host/ function module	USB_X1	I	Crystal resonator/ external clock for USB 2.0 host/function module	Connected to a crystal resonator for USB 2.0 host/function module. An external clock signal may also be input to the USB_X1 pin.
	USB_X2	O		
	USBAPVcc	I	Power supply for transceiver analog pins	Power supply for pins.
	USBAPVss Note: This pin is not present on products in the BGA package.	I	Ground for transceiver analog pins	Ground for pins.
	USBDPVcc Note: This pin is not present on products in the BGA package.	I	Power supply for transceiver digital pins	Power supply for pins.
	USBDPVss Note: This pin is not present on products in the BGA package.	I	Ground for transceiver digital pins	Ground for pins.
	USBAVcc	I	Power supply for transceiver analog core	Power supply for core.
	USBAVss Note: This pin is not present on products in the BGA package.	I	Ground for transceiver analog core	Ground for core.
	USBDVcc Note: This pin is not present on products in the BGA package.	I	Power supply for transceiver digital core	Power supply for core.
	USBDVss Note: This pin is not present on products in the BGA package.	I	Ground for transceiver digital core	Ground for core.
	USBUVcc Note: This pin is not present on products in the BGA package.	I	480-MHz power supply for USB 2.0 host/function module	Power supply for 480-MHz sections
	USBUVss Note: This pin is not present on products in the BGA package.	I	480-MHz ground for USB 2.0 host/function module	Ground for 480-MHz sections

Classification	Symbol	I/O	Name	Function
Digital video decoder	VIN1A, VIN2A	I	Composite video signal (CVBS) input	Composite video signal (CVBS) channel 0 input pins.
	VIN1B, VIN2B	I	Composite video signal (CVBS) input	Composite video signal (CVBS) channel 1 input pins.
	VIDEO_X1	I	Crystal resonator/ external clock for digital video decoder	Connected to a crystal resonator for digital video decoder. An external clock signal may also be input to the VIDEO_X1 pin.
	VIDEO_X2	O		
	VRP	O	TOP reference voltage	TOP reference voltage pin for the A/D converter to input video signals. Connected to VDAVss via 0.1-μF capacitor.
	VRM	O	BOTTOM reference voltage	BOTTOM reference voltage pin for the A/D converter to input video signals. Connected to VDAVss via 0.1-μF capacitor.
	REXT	I	Reference voltage	Reference voltage pin for the A/D converter to input video signals. Connected to VDAVss via 22-kΩ ± 1% resistance.
	VDAVcc	I	Analog power supply	Power supply pin for the A/D converter to input video signals.
	VDAVss	I	Analog ground	Ground pin for the A/D converter to input video signals.
Video display controller 5	LCD1_DATA23 to LCD1_DATA0, LCD0_DATA23 to LCD0_DATA0	O	Output data	Data output pins for panel.
	LCD1_TCON6 to LCD1_TCON0, LCD0_TCON6 to LCD0_TCON0	O	Panel timing adjustment output	Output pins for panel timing adjustment
	LCD1_CLK, LCD0_CLK	O	Panel clock	Panel clock output pins.
	LCD1_EXTCLK, LCD0_EXTCLK	I	Panel clock source	Panel clock source input pins.
	DV0_DATA23 to DV0_DATA0, DV1_DATA7 to DV1_DATA0	I	Input data	Data input pins for graphics data.
	DV1_VSYNC, DV0_VSYNC	I	VSYNC input	VSYNC input pins.
	DV1_HSYNC, DV0_HSYNC	I	HSYNC input	HSYNC input pins.
	DV1_CLK, DV0_CLK	I	Input clock	Clock input signal pins for graphics data.
LVDS output interface	TXCLKOUTP, TXCLKOUTM	O	Output clock	LVDS differential clock output pins.
	TXOUT2P to TXOUT0P, TXOUT2M to TXOUT0M	O	Output data	LVDS differential data output pins.
	LVDSREFRIN	I	Reference input	Connected to LVDSAPVss via 5.6-kΩ ± 1% resistance.(QFP package) Connected to Vss via 5.6-kΩ ± 1% resistance. (BGA package)
	LVDSAPVcc	I	LVDS analog power supply	Power supply for LVDS output.
	LVDSAPVss Note: This pin is not present on products in the BGA package.	I	LVDS analog ground	Ground for LVDS output.
	LVDSPLLVcc	I	LVDS PLL power supply	Power supply for LVDS PLL.
Capture engine unit	VIO_D15 to VIO_D0	I	Input data	Graphics data input pins.
	VIO_CLK	I	Input clock	Graphics data clock input pin.
	VIO_VD	I	VSYNC input	VSYNC input pin.
	VIO_HD	I	HSYNC input	HSYNC input pin.
	VIO_FLD	I	FIELD input	Input pin for field information

Classification	Symbol	I/O	Name	Function
Sound generator	SGOUT3 to SGOUT0	O	Sound generator output	Sound generator output pins.
SD host interface	SD_CLK_0, SD_CLK_1	O	SD clock	Output pins for SD clock.
	SD_CMD_0, SD_CMD_1	I/O	SD command	SD command output and response input signals.
	SD_D3_0 to SD_D0_0, SD_D3_1 to SD_D0_1	I/O	SD data	SD data bus signals.
	SD_CD_0, SD_CD_1	I	SD card detection	SD card detection.
	SD_WP_0, SD_WP_1	I	SD write protection	SD write protection signals.
MMC host interface	MMC_CLK	O	MMC clock	Output pin for MMC clock.
	MMC_CMD	I/O	MMC command	MMC command output and response input signal.
	MMC_D7 to MMC_D0	I/O	MMC data	MMC data bus signals.
	MMC_CD	I	MMC card detection	MMC card detection.
Motor control PWM timer	PWM1H to PWM1A PWM2H to PWM2A	O	Timer output	PWM output pins.
A/D converter	AN7 to AN0	I	Analog input pins	Analog input pins.
	$\overline{\text{ADTRG}}$	I	A/D conversion trigger input	External trigger input pin for starting A/D conversion.
	AVcc	I	Analog power supply	Power supply pin for A/D converter.
	AVss	I	Analog ground	Ground pin for A/D converter.
	AVref	I	Analog reference voltage	Reference voltage pin for A/D converter.
General I/O ports	P2_0 to P2_15, P3_0 to P3_15, P4_0 to P4_15, P5_0 to P5_10, P6_0 to P6_15, P7_0 to P7_15, P8_0 to P8_15, P9_0 to P9_7, P10_0 to P10_15 P11_0 to P11_15	I/O	General port	General I/O port pins.
	P1_0 to P1_7	I/O	General port	8 input port pins with open-drain output.
	JP0_0, JP0_1, P0_0 to P0_5, P1_8 to P1_15	I	General port	16 general input port pins.
Debugging interface	TCK/SWDCLK	I	Test clock	Test-clock input pin. Also used as the input clock pin for serial wire debugging
	TMS/SWDIO	I, I/O	Test mode select	Test-mode select signal input pin. Also used as the I/O data pin for serial wire debugging
	TDI	I	Test data input	Serial input pin for instructions and data.
	TDO	O	Test data output	Serial output pin for instructions and data.
	$\overline{\text{TRST}}$	I	Test reset	Initialization-signal input pin.
	TRACEDATA3 to TRACEDATA0	O	Data output	Trace data output pins.
	TRACECLK	O	Clock output	Trace clock output pin.
	TRACECTL	O	Enable output	Trace enable output pin.

2.1.2 List of Pins

Table 2.2 List of Pins (256-Pin, BGA)

Ball Number	Port Function/ Dedicated Function		Mode Function		Function 1		Function 2		Function 3		Function 4		Function 5		Function 6		Function 7		Function 8		Simplified Circuit Diagram Figure 2.1
	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	
A1	PVcc																				
A2	P6_4	I(s)/O	—	—	D4	I(s)/O	LCD1_DATA12	O	CAN2RX	I(s)	IRQ3	I(s)	$\overline{RTS5}$	I(s)/O	—	—	RSPCK1	I(s)/O	DV0_DATA20	I(s)	(8)
A3	P6_2	I(s)/O	—	—	D2	I(s)/O	LCD1_DATA10	O	RLIN31RX	I(s)	IRQ7	I(s)	TCLKA	I(s)	TIOC2A	I(s)/O	RxD2	I(s)	DV0_DATA18	I(s)	(8)
A4	P6_0	I(s)/O	—	—	D0	I(s)/O	LCD1_DATA8	O	RLIN30RX	I(s)	DV0_CLK	I(s)	TIOC1A	I(s)/O	IRQ5	I(s)	RxD3	I(s)	DV0_DATA16	I(s)	(8)
A5	P9_7	I(s)/O	—	—	LCD1_DATA23	O	SPBIO30_0	I(s)/O	SSIDATA2	I(s)/O	TIOC1A	I(s)/O	—	—	—	—	—	—	—	—	(7)
A6	P9_4	I(s)/O	—	—	LCD1_DATA20	O	SPBIO00_0	I(s)/O	—	—	RxD1	I(s)	—	—	—	—	—	—	—	—	(7)
A7	P5_10	I(s)/O	—	—	$\overline{WE3}$/DQMUU/AH	O	—	—	DV0_HSYNC	I(s)	—	—	CAN1TX	O	IETxD	O	LCD1_DATA17	O	—	—	(7)
A8	P5_8	I(s)/O	—	—	LCD0_EXTCLK	I(s)	IRQ0	I(s)	DV1_CLK	I(s)	—	—	DV0_CLK	I(s)	$\overline{CS2}$	O	—	—	—	—	(7)
A9	P5_7	I(s)/O	—	—	TXOUT0M	O	LCD1_DATA7	O	LCD0_DATA23	O	DV1_DATA7	I(s)	RxD6	I(s)	TIOC0D	I(s)/O	SPDIF_OUT	O	DV0_DATA15	I(s)	(12), (13)
A10	P5_3	I(s)/O	—	—	TXOUT2M	O	LCD1_DATA3	O	LCD0_DATA19	O	DV1_DATA3	I(s)	TxD3	O	TIOC3C	I(s)/O	—	—	MISO3	I(s)/O	(12), (13)
A11	P5_1	I(s)/O	—	—	TXCLKOUTM	O	LCD1_DATA1	O	LCD0_DATA17	O	DV1_DATA1	I(s)	RxD4	I(s)	TIOC0B	I(s)/O	—	—	SSL30	I(s)/O	(12), (13)
A12	LVDSRE-FRIN	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(12), (13)
A13	VIN2B	I(a)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
A14	VDAVss																				
A15	VIN1A	I(a)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
A16	P0_2	I(s)	MD_CLK	I(s)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(3)
A17	P1_4	I(s)/O(o)	—	—	RIIC2SCL	I(s)/O(o)	DV0_CLK	I(s)	CAN1RX	I(s)	IRQ4	I(s)	—	—	—	—	CAN_CLK	I(s)	—	—	(9)
A18	P2_15	I(s)/O	—	—	D31	I(s)/O	MISO0	I(s)/O	DV0_DATA15	I(s)	SPBIO31_0	I(s)/O	CAN_CLK	I(s)	RxD0	I(s)	LCD1_DATA15	O	IRQ1	I(s)	(8)
A19	P2_12	I(s)/O	—	—	D28	I(s)/O	RSPCK0	I(s)/O	DV0_DATA12	I(s)	SPBIO01_0	I(s)/O	CAN3RX	I(s)	IRQ6	I(s)	LCD1_DATA12	O	TIOC1B	I(s)/O	(8)
A20	PVcc																				
A21	Vss																				
B1	Vss																				
B2	PVcc																				
B3	P6_3	I(s)/O	—	—	D3	I(s)/O	LCD1_DATA11	O	RLIN31TX	O	IRQ2	I(s)	$\overline{CTS5}$	I(s)/O	TIOC2B	I(s)/O	TxD2	O	DV0_DATA19	I(s)	(8)
B4	P6_1	I(s)/O	—	—	D1	I(s)/O	LCD1_DATA9	O	RLIN30TX	O	IRQ4	I(s)	TIOC1B	I(s)/O	SSIDATA4	I(s)/O	TxD3	O	DV0_DATA17	I(s)	(8)
B5	P0_3	I(s)	MD_CLKS	I(s)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(3)
B6	P9_5	I(s)/O	—	—	LCD1_DATA21	O	SPBIO10_0	I(s)/O	SSISCK2	I(s)/O	$\overline{CTS1}$	I(s)/O	$\overline{CS4}$	O	—	—	—	—	—	—	(7)
B7	P5_9	I(s)/O	—	—	$\overline{WE2}$/DQMUL	O	ET_MDC	O	DV0_VSYNC	I(s)	IRQ2	I(s)	CAN1RX	I(s)	IERxD	I(s)	LCD1_DATA16	O	—	—	(7)
B8	Vss																				(1)
B9	P5_6	I(s)/O	—	—	TXOUT0P	O	LCD1_DATA6	O	LCD0_DATA22	O	DV1_DATA6	I(s)	TxD6	O	IRQ6	I(s)	SPDIF_IN	I(s)	DV0_DATA14	I(s)	(12), (13)
B10	P5_2	I(s)/O	—	—	TXOUT2P	O	LCD1_DATA2	O	LCD0_DATA18	O	DV1_DATA2	I(s)	SCK3	I(s)/O	TIOC1B	I(s)/O	—	—	MOSI3	I(s)/O	(12), (13)
B11	P5_0	I(s)/O	—	—	TXCLKOUTP	O	LCD1_DATA0	O	LCD0_DATA16	O	DV1_DATA0	I(s)	TxD4	O	TIOC0A	I(s)/O	—	—	RSPCK3	I(s)/O	(12), (13)
B12	Vss																				
B13	VIN1B	I(a)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
B14	VDAVcc																				
B15	VIN2A	I(a)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
B16	P1_5	I(s)/O(o)	—	—	RIIC2SDA	I(s)/O(o)	DV1_CLK	I(s)	CAN4RX	I(s)	IRQ5	I(s)	VIO_CLK	I(s)	—	—	LCD1_EXTCLK	I(s)	—	—	(9)
B17	P1_0	I(s)/O(o)	—	—	RIIC0SCL	I(s)/O(o)	DV0_DATA16	I(s)	TCLKA	I(s)	IRQ0	I(s)	VIO_VD	I(s)	DV0_VSYNC	I(s)	—	—	—	—	(9)
B18	P2_14	I(s)/O	—	—	D30	I(s)/O	MOSI0	I(s)/O	DV0_DATA14	I(s)	SPBIO21_0	I(s)/O	CAN4RX	I(s)	TxD0	O	LCD1_DATA14	O	IRQ0	I(s)	(8)
B19	PVcc																				
B20	Vss																				
B21	P2_10	I(s)/O	—	—	D26	I(s)/O	ET_RXD2	I(s)	DV0_DATA10	I(s)	SSIRxD0	I(s)	RLIN30TX	O	LCD1_DATA10	O	VIO_D10	I(s)	MOSI4	I(s)/O	(8)
C1	Vcc																				
C2	Vss																				
C20	P2_11	I(s)/O	—	—	D27	I(s)/O	ET_RXD3	I(s)	DV0_DATA11	I(s)	SSITxD0	O	TIOC1A	I(s)/O	LCD1_DATA11	O	VIO_D11	I(s)	MISO4	I(s)/O	(8)
C21	P2_9	I(s)/O	—	—	D25	I(s)/O	ET_RXD1	I(s)	DV0_DATA9	I(s)	SSIWS0	I(s)/O	RLIN30RX	I(s)	LCD1_DATA9	O	VIO_D9	I(s)	SSL40	I(s)/O	(8)

Ball Number	Port Function/ Dedicated Function		Mode Function		Function 1		Function 2		Function 3		Function 4		Function 5		Function 6		Function 7		Function 8		Simplified Circuit Diagram Figure 2.1
	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	
D1	P6_8	I(s)/O	—	—	D8	I(s)/O	DV0_DATA12	I(s)	—	—	CAN_CLK	I(s)	SCK0	I(s)/O	LCD0_DATA0	O	—	—	IRQ0	I(s)	(8)
D2	Vcc																				
D4	PVcc																				
D5	P9_6	I(s)/O	—	—	LCD1_DATA22	O	SPBIO20_0	I(s)/O	SSIWS2	I(s)/O	$\overline{RTS1}$	I(s)/O	$\overline{CS5}$	O	—	—	—	—	—	—	(7)
D6	P9_3	I(s)/O	—	—	LCD1_DATA19	O	SPBSSL_0	O	—	—	TxD1	O	—	—	—	—	—	—	—	—	(7)
D7	LVD SAPVcc																				
D8	LVD SPLLVcc																				
D9	P5_5	I(s)/O	—	—	TXOUT1M	O	LCD1_DATA5	O	LCD0_DATA21	O	DV1_DATA5	I(s)	AUDIO_XOUT	O	TIOC0C	I(s)/O	$\overline{FCE}$	O	DV0_DATA13	I(s)	(12), (13)
D10	P5_4	I(s)/O	—	—	TXOUT1P	O	LCD1_DATA4	O	LCD0_DATA20	O	DV1_DATA4	I(s)	RxD3	I(s)	TIOC3D	I(s)/O	—	—	DV0_DATA12	I(s)	(12), (13)
D11	VRP	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
D12	REXT	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
D13	P1_7	I(s)/O(o)	—	—	RIIC3SDA	I(s)/O(o)	DV1_HSYNC	I(s)	RLIN30RX	I(s)	IRQ7	I(s)	VIO_D13	I(s)	DV0_DATA13	I(s)	—	—	—	—	(9)
D14	P1_3	I(s)/O(o)	—	—	RIIC1SDA	I(s)/O(o)	DV0_DATA19	I(s)	ET_COL	I(s)	IRQ3	I(s)	$\overline{ADTRG}$	I(s)	—	—	—	—	—	—	(9)
D15	P1_1	I(s)/O(o)	—	—	RIIC0SDA	I(s)/O(o)	DV0_DATA17	I(s)	TCLKC	I(s)	IRQ1	I(s)	VIO_HD	I(s)	DV0_HSYNC	I(s)	—	—	—	—	(9)
D16	P2_13	I(s)/O	—	—	D29	I(s)/O	SSL00	I(s)/O	DV0_DATA13	I(s)	SPBIO11_0	I(s)/O	CAN3TX	O	SCK0	I(s)/O	LCD1_DATA13	O	IRQ7	I(s)	(8)
D17	PVcc																				
D18	Vss																				
D20	P2_7	I(s)/O	—	—	D23	I(s)/O	ET_TXD3	O	DV0_DATA7	I(s)	SSITxD5	O	IETxD	O	$\overline{RTS1}$	I(s)/O	VIO_D7	I(s)	LCD0_DATA23	O	(8)
D21	P2_8	I(s)/O	—	—	D24	I(s)/O	ET_RXD0	I(s)	DV0_DATA8	I(s)	SSISCK0	I(s)/O	LCD0_TCON6	O	LCD1_DATA8	O	VIO_D8	I(s)	RSPCK4	I(s)/O	(8)
E1	P6_9	I(s)/O	—	—	D9	I(s)/O	DV0_DATA13	I(s)	—	—	—	—	TxD0	O	LCD0_DATA1	O	—	—	IRQ1	I(s)	(8)
E2	P6_7	I(s)/O	—	—	D7	I(s)/O	LCD1_DATA15	O	—	—	LCD0_TCON6	O	RxD5	I(s)	—	—	MISO1	I(s)/O	DV0_DATA23	I(s)	(8)
E4	Vss																				
E5	PVcc																				
E6	P9_2	I(s)/O	—	—	LCD1_DATA18	O	SPBCLK_0	O	RLIN30TX	O	SCK1	I(s)/O	A0	O	—	—	—	—	—	—	(7)
E7	LVD SAPVcc																				
E8	LVD SAPVcc																				
E9	Vss																				
E10	Vss																				
E11	Vcc																				
E12	VRM	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
E13	P1_6	I(s)/O(o)	—	—	RIIC3SCL	I(s)/O(o)	DV1_VSYNC	I(s)	IERxD	I(s)	IRQ6	I(s)	VIO_D12	I(s)	DV0_DATA12	I(s)	—	—	—	—	(9)
E14	P1_2	I(s)/O(o)	—	—	RIIC1SCL	I(s)/O(o)	DV0_DATA18	I(s)	$\overline{RFB}$	I(s)	IRQ2	I(s)	—	—	—	—	LCD1_EXTCLK	I(s)	—	—	(9)
E15	Vss																				
E16	PVcc																				
E17	Vss																				
E18	P2_4	I(s)/O	—	—	D20	I(s)/O	ET_TXD0	O	DV0_DATA4	I(s)	SSISCK5	I(s)/O	SPBCLK_1	O	SCK1	I(s)/O	VIO_D4	I(s)	LCD0_DATA20	O	(8)
E20	P2_5	I(s)/O	—	—	D21	I(s)/O	ET_TXD1	O	DV0_DATA5	I(s)	SSIWS5	I(s)/O	SPBSSL_1	O	TxD1	O	VIO_D5	I(s)	LCD0_DATA21	O	(8)
E21	P2_6	I(s)/O	—	—	D22	I(s)/O	ET_TXD2	O	DV0_DATA6	I(s)	SSIRxD5	I(s)	—	—	RxD1	I(s)	VIO_D6	I(s)	LCD0_DATA22	O	(8)
F1	P6_12	I(s)/O	—	—	D12	I(s)/O	DV0_DATA20	I(s)	—	—	—	—	TxD1	O	LCD0_DATA4	O	—	—	IRQ4	I(s)	(8)
F2	P6_10	I(s)/O	—	—	D10	I(s)/O	DV0_DATA14	I(s)	—	—	LCD0_TCON5	O	RxD0	I(s)	LCD0_DATA2	O	—	—	IRQ2	I(s)	(8)
F4	Vcc																				
F5	Vss																				
F17	P4_14	I(s)/O	—	—	LCD0_DATA22	O	LCD1_TCON1	O	SD_D3_0	I(s)/O	MMC_D3	I(s)/O	SPBIO21_1	I(s)/O	SSIRxD3	I(s)	TxD2	O	IRQ6	I(s)	(7)
F18	P4_15	I(s)/O	—	—	LCD0_DATA23	O	LCD1_TCON2	O	SD_D2_0	I(s)/O	MMC_D2	I(s)/O	SPBIO31_1	I(s)/O	SSITxD3	O	RxD2	I(s)	IRQ7	I(s)	(7)
F20	P2_2	I(s)/O	—	—	D18	I(s)/O	ET_TXEN	O	DV0_DATA2	I(s)	SPBIO20_1	I(s)/O	MLB_SIG	I(s)/O	TIOC2B	I(s)/O	VIO_D2	I(s)	LCD0_DATA18	O	(8)
F21	P2_3	I(s)/O	—	—	D19	I(s)/O	ET_CRS	I(s)	DV0_DATA3	I(s)	SPBIO30_1	I(s)/O	IERxD	I(s)	$\overline{CTS1}$	I(s)/O	VIO_D3	I(s)	LCD0_DATA19	O	(8)
G1	P7_0	I(s)/O	MD_BOOT2	I(s)	$\overline{CS0}$	O	DV0_DATA16	I(s)	ET_MDC	O	SCK4	I(s)/O	RLIN30TX	O	—	—	TIOC0A	I(s)/O	—	—	(7)
G2	P6_11	I(s)/O	—	—	D11	I(s)/O	DV0_DATA15	I(s)	—	—	LCD0_TCON6	O	SCK1	I(s)/O	LCD0_DATA3	O	—	—	IRQ3	I(s)	(8)

Ball Number	Port Function/ Dedicated Function		Mode Function		Function 1		Function 2		Function 3		Function 4		Function 5		Function 6		Function 7		Function 8		Simplified Circuit Diagram Figure 2.1
	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	
G4	P6_5	I(s)/O	—	—	D5	I(s)/O	LCD1_DATA13	O	CAN2TX	O	—	—	SCK5	I(s)/O	—	—	SSL10	I(s)/O	DV0_DATA21	I(s)	(8)
G5	Vcc																				
G17	Vcc																				
G18	P4_11	I(s)/O	—	—	LCD0_DATA19	O	LCD1_TCON6	O	SD_D0_0	I(s)/O	MMC_D0	I(s)/O	SSITxD5	O	CAN4TX	O	SCK1	I(s)/O	IRQ3	I(s)	(8)
G20	P4_13	I(s)/O	—	—	LCD0_DATA21	O	LCD1_TCON0	O	SD_CMD_0	I(s)/O	MMC_CMD	I(s)/O	SPBIO11_1	I(s)/O	SSIWS3	I(s)/O	RxD1	I(s)	IRQ5	I(s)	(7)
G21	Vss																				
H1	P7_2	I(s)/O	—	—	$\overline{RAS}$	O	DV0_DATA18	I(s)	ET_TXER	O	RxD4	I(s)	CAN2RX	I(s)	SSIWS1	I(s)/O	TIOC0C	I(s)/O	—	—	(7)
H2	P6_13	I(s)/O	—	—	D13	I(s)/O	DV0_DATA21	I(s)	—	—	SCK6	I(s)/O	RxD1	I(s)	LCD0_DATA5	O	—	—	IRQ5	I(s)	(8)
H4	P6_6	I(s)/O	—	—	D6	I(s)/O	LCD1_DATA14	O	—	—	LCD0_TCON5	O	TxD5	O	—	—	MOSI1	I(s)/O	DV0_DATA22	I(s)	(8)
H5	Vss																				
H17	Vcc																				
H18	P2_1	I(s)/O	—	—	D17	I(s)/O	ET_TXER	O	DV0_DATA1	I(s)	SPBIO10_1	I(s)/O	MLB_DAT	I(s)/O	TIOC2A	I(s)/O	VIO_D1	I(s)	LCD0_DATA17	O	(8)
H20	P4_10	I(s)/O	—	—	LCD0_DATA18	O	LCD1_TCON5	O	SD_D1_0	I(s)/O	MMC_D1	I(s)/O	SSIRxD5	I(s)	—	—	RxD0	I(s)	IRQ2	I(s)	(7)
H21	P4_12	I(s)/O	—	—	LCD0_DATA20	O	LCD1_CLK	O	SD_CLK_0	O	MMC_CLK	O	SPBIO01_1	I(s)/O	SSISCK3	I(s)/O	TxD1	O	IRQ4	I(s)	(7)
J1	P7_4	I(s)/O	—	—	CKE	O	DV0_DATA20	I(s)	ET_TXD0	O	TxD7	O	—	—	SSITxD1	O	TIOC1A	I(s)/O	—	—	(7)
J2	P7_3	I(s)/O	—	—	$\overline{CAS}$	O	DV0_DATA19	I(s)	ET_TXEN	O	SCK7	I(s)/O	CAN2TX	O	SSIRxD1	I(s)	TIOC0D	I(s)/O	—	—	(7)
J4	P6_14	I(s)/O	—	—	D14	I(s)/O	DV0_DATA22	I(s)	—	—	TxD6	O	—	—	LCD0_DATA6	O	—	—	IRQ6	I(s)	(8)
J5	Vss																				
J17	Vss																				
J18	P2_0	I(s)/O	—	—	D16	I(s)/O	ET_TXCLK	I(s)	DV0_DATA0	I(s)	SPBIO00_1	I(s)/O	MLB_CLK	I(s)	IRQ5	I(s)	VIO_D0	I(s)	LCD0_DATA16	O	(8)
J20	P4_9	I(s)/O	—	—	LCD0_DATA17	O	LCD1_TCON4	O	SD_WP_0	I(s)	—	—	SSIWS5	I(s)/O	CAN2RX	I(s)	TxD0	O	IRQ1	I(s)	(7)
J21	P4_8	I(s)/O	—	—	LCD0_DATA16	O	LCD1_TCON3	O	SD_CD_0	I(s)	MMC_CD	I(s)	SSISCK5	I(s)/O	CAN2TX	O	SCK0	I(s)/O	IRQ0	I(s)	(7)
K1	P7_8	I(s)/O	—	—	$\overline{RD}$	O	SSISCK3	I(s)/O	—	—	CAN0RX	I(s)	—	—	—	—	TIOC3A	I(s)/O	IRQ1	I(s)	(7)
K2	P7_6	I(s)/O	—	—	$\overline{WE0}$/DQMLL	O	DV0_DATA22	I(s)	ET_TXD2	O	$\overline{CTS7}$	I(s)/O	—	—	SSIWS2	I(s)/O	TIOC2A	I(s)/O	—	—	(7)
K4	P7_1	I(s)/O	—	—	$\overline{CS3}$	O	DV0_DATA17	I(s)	ET_TXCLK	I(s)	TxD4	O	DV0_CLK	I(s)	SSISCK1	I(s)/O	TIOC0B	I(s)/O	—	—	(7)
K5	P6_15	I(s)/O	—	—	D15	I(s)/O	DV0_DATA23	I(s)	—	—	RxD6	I(s)	—	—	LCD0_DATA7	O	—	—	IRQ7	I(s)	(8)
K17	Vss																				
K18	P4_3	I(s)/O	—	—	LCD0_DATA11	O	TIOC0D	I(s)/O	$\overline{FWE}$	O	CAN3TX	O	RxD2	I(s)	—	—	MISO4	I(s)/O	MMC_D7	I(s)/O	(7)
K20	P4_7	I(s)/O	—	—	LCD0_DATA15	O	MISO1	I(s)/O	TIOC4D	I(s)/O	PWM2H	O	SSITxD0	O	—	—	DV0_DATA15	I(s)	—	—	(7)
K21	P4_6	I(s)/O	—	—	LCD0_DATA14	O	MOSI1	I(s)/O	TIOC4C	I(s)/O	PWM2G	O	SSIRxD0	I(s)	—	—	DV0_DATA14	I(s)	—	—	(7)
L1	P7_10	I(s)/O	—	—	A2	O	SSIRxD3	I(s)	ET_RXD1	I(s)	CAN1TX	O	—	—	—	—	TIOC3C	I(s)/O	IRQ2	I(s)	(7)
L2	P7_9	I(s)/O	—	—	A1	O	SSIWS3	I(s)/O	ET_RXD0	I(s)	CAN0TX	O	—	—	—	—	TIOC3B	I(s)/O	IRQ0	I(s)	(7)
L4	P7_7	I(s)/O	—	—	$\overline{WE1}$/DQMLU	O	DV0_DATA23	I(s)	ET_TXD3	O	$\overline{RTS7}$	I(s)/O	—	—	SSIDATA2	I(s)/O	TIOC2B	I(s)/O	—	—	(7)
L5	P7_5	I(s)/O	—	—	RD/$\overline{WR}$	O	DV0_DATA21	I(s)	ET_TXD1	O	RxD7	I(s)	—	—	SSISCK2	I(s)/O	TIOC1B	I(s)/O	—	—	(7)
L17	P3_15	I(s)/O	—	—	LCD0_DATA7	O	—	—	NAF7	I(s)/O	—	—	TRACECTL	O	—	—	SD_D2_1	I(s)/O	MMC_D2	I(s)/O	(7)
L18	P4_0	I(s)/O	—	—	LCD0_DATA8	O	TIOC0A	I(s)/O	$\overline{FRE}$	O	—	—	—	—	—	—	RSPCK4	I(s)/O	MMC_D4	I(s)/O	(7)
L20	P4_5	I(s)/O	—	—	LCD0_DATA13	O	SSL10	I(s)/O	TIOC4B	I(s)/O	PWM2F	O	SSIWS0	I(s)/O	—	—	DV0_DATA13	I(s)	—	—	(7)
L21	P4_4	I(s)/O	—	—	LCD0_DATA12	O	RSPCK1	I(s)/O	TIOC4A	I(s)/O	PWM2E	O	SSISCK0	I(s)/O	—	—	DV0_DATA12	I(s)	—	—	(7)
M1	P7_14	I(s)/O	—	—	A6	O	SSIDATA4	I(s)/O	ET_CRS	I(s)	—	—	—	—	—	—	TIOC4C	I(s)/O	IRQ6	I(s)	(7)
M2	P7_13	I(s)/O	—	—	A5	O	SSIWS4	I(s)/O	ET_MDIO	I(s)/O	—	—	—	—	—	—	TIOC4B	I(s)/O	IRQ5	I(s)	(7)
M4	P7_12	I(s)/O	—	—	A4	O	SSISCK4	I(s)/O	ET_RXD3	I(s)	—	—	—	—	—	—	TIOC4A	I(s)/O	IRQ4	I(s)	(7)
M5	P7_11	I(s)/O	—	—	A3	O	SSITxD3	O	ET_RXD2	I(s)	CAN1RX	I(s)	—	—	—	—	TIOC3D	I(s)/O	IRQ3	I(s)	(7)
M17	P3_10	I(s)/O	—	—	LCD0_DATA2	O	—	—	NAF2	I(s)/O	—	—	TRACEDATA2	O	TIOC4C	I(s)/O	SD_D1_1	I(s)/O	MMC_D1	I(s)/O	(7)
M18	P3_11	I(s)/O	—	—	LCD0_DATA3	O	—	—	NAF3	I(s)/O	—	—	TRACEDATA3	O	TIOC4D	I(s)/O	SD_D0_1	I(s)/O	MMC_D0	I(s)/O	(7)
M20	P4_2	I(s)/O	—	—	LCD0_DATA10	O	TIOC0C	I(s)/O	FALE	O	CAN3RX	I(s)	TxD2	O	—	—	MOSI4	I(s)/O	MMC_D6	I(s)/O	(7)
M21	P4_1	I(s)/O	—	—	LCD0_DATA9	O	TIOC0B	I(s)/O	FCLE	O	—	—	SCK2	I(s)/O	—	—	SSL40	I(s)/O	MMC_D5	I(s)/O	(7)
N1	P8_1	I(s)/O	—	—	A9	O	MOSI0	I(s)/O	ET_RXDV	I(s)	TxD5	O	SCI_RXD0	I(s)	—	—	—	—	—	—	(7)

Ball Number	Port Function/ Dedicated Function		Mode Function		Function 1		Function 2		Function 3		Function 4		Function 5		Function 6		Function 7		Function 8		Simplified Circuit Diagram Figure 2.1
	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	
N2	P8_2	I(s)/O	—	—	A10	O	MISO0	I(s)/O	AVB_GPTP_EXTERN	I(s)	RxD5	I(s)	IRQ0	I(s)	—	—	—	—	—	—	(7)
N4	P8_0	I(s)/O	—	—	A8	O	SSL00	I(s)/O	ET_RXER	I(s)	SCK5	I(s)/O	SCI_SCK0	I(s)/O	—	—	—	—	—	—	(7)
N5	P7_15	I(s)/O	—	—	A7	O	RSPCK0	I(s)/O	ET_RXCLK	I(s)	$\overline{CTS5}$	I(s)/O	SCI_TXD0	O	—	—	TIOC4D	I(s)/O	—	—	(7)
N17	JP0_1	I	—	—	TDO	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(6)
N18	JP0_0	I	—	—	TDI	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(2)
N20	P3_13	I(s)/O	—	—	LCD0_DATA5	O	—	—	NAF5	I(s)/O	AUDIO_XOUT	O	—	—	—	—	SD_CMD_1	I(s)/O	MMC_CMD	I(s)/O	(7)
N21	P3_14	I(s)/O	—	—	LCD0_DATA6	O	—	—	NAF6	I(s)/O	—	—	TRACECLK	O	—	—	SD_D3_1	I(s)/O	MMC_D3	I(s)/O	(7)
P1	P8_4	I(s)/O	—	—	A12	O	DV1_DATA1	I(s)	SSL20	I(s)/O	—	—	—	—	IERxD	I(s)	RxD2	I(s)	—	—	(7)
P2	P8_5	I(s)/O	—	—	A13	O	DV1_DATA2	I(s)	MOSI2	I(s)/O	—	—	—	—	—	—	—	—	—	—	(7)
P4	P8_3	I(s)/O	—	—	A11	O	DV1_DATA0	I(s)	RSPCK2	I(s)/O	$\overline{RTS5}$	I(s)/O	—	—	IRQ1	I(s)	SCK2	I(s)/O	—	—	(7)
P5	P8_6	I(s)/O	—	—	A14	O	DV1_DATA3	I(s)	MISO2	I(s)/O	—	—	—	—	IETxD	O	TxD2	O	—	—	(7)
P17	PVcc																				
P18	PVcc																				
P20	Vss																				
P21	P3_12	I(s)/O	—	—	LCD0_DATA4	O	—	—	NAF4	I(s)/O	—	—	—	—	—	—	SD_CLK_1	O	MMC_CLK	O	(7)
R1	CKIO	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(5)
R2	P8_7	I(s)/O	—	—	A15	O	DV1_DATA4	I(s)	AUDIO_XOUT	O	IRQ5	I(s)	ET_COL	I(s)	—	—	—	—	—	—	(7)
R4	P8_10	I(s)/O	—	—	A18	O	DV1_DATA7	I(s)	SPBIO20_1	I(s)/O	TIOC3A	I(s)/O	CAN4TX	O	PWM1C	O	SGOUT_0	O	SSITxD5	O	(7)
R5	PVcc																				
R17	PVcc																				
R18	PVcc																				
R20	TMS	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(6)
R21	TCK	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(2)
T1	P8_8	I(s)/O	—	—	A16	O	DV1_DATA5	I(s)	SPBIO00_1	I(s)/O	SPDIF_IN	I(s)	TIOC1A	I(s)/O	PWM1A	O	TxD3	O	SSISCK5	I(s)/O	(7)
T2	P8_9	I(s)/O	—	—	A17	O	DV1_DATA6	I(s)	SPBIO10_1	I(s)/O	SPDIF_OUT	O	TIOC1B	I(s)/O	PWM1B	O	RxD3	I(s)	SSIWS5	I(s)/O	(7)
T4	PVcc																				
T5	Vss																				
T17	Vss																				
T18	BSCANP	I(s)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(1)
T20	P3_9	I(s)/O	—	—	LCD0_DATA1	O	—	—	NAF1	I(s)/O	—	—	TRACEDATA1	O	TIOC4B	I(s)/O	SD_WP_1	I(s)	IRQ6	I(s)	(7)
T21	$\overline{TRST}$	I(s)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(3)
U1	P8_11	I(s)/O	—	—	A19	O	—	—	SPBIO30_1	I(s)/O	TIOC3B	I(s)/O	RxD5	I(s)	PWM1D	O	SGOUT_1	O	DV0_CLK	I(s)	(7)
U2	P8_12	I(s)/O	—	—	A20	O	—	—	SPBCLK_1	O	TIOC3C	I(s)/O	SCK5	I(s)/O	PWM1E	O	SGOUT_2	O	SSISCK4	I(s)/O	(7)
U4	PVcc																				
U5	Vss																				
U6	Vcc																				
U7	Vss																				
U8	P3_3	I(s)/O	—	—	LCD0_TCON2	O	ET_MDIO	I(s)/O	IRQ4	I(s)	$\overline{BS}$	O	$\overline{SCI\_CTS1}$/RTS1	I(s)/O	DACK0	O	PWM2D	O	MISO3	I(s)/O	(7)
U9	$\overline{RES}$	I(s)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(1)
U10	Vss																				
U11	PVcc																				
U12	PVcc																				
U13	USBAPVcc																				
U14	PLLVcc																				
U15	Vss																				
U16	Vcc																				
U17	Vcc																				
U18	Vss																				
U20	AUDIO_X2	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(10)
U21	P3_8	I(s)/O	—	—	LCD0_DATA0	O	—	—	NAF0	I(s)/O	—	—	TRACEDATA0	O	TIOC4A	I(s)/O	SD_CD_1	I(s)	MMC_CD	I(s)	(7)
V1	P8_13	I(s)/O	—	—	A21	O	—	—	SPBSSL_1	O	TIOC3D	I(s)/O	TxD5	O	PWM1F	O	SGOUT_3	O	SSIWS4	I(s)/O	(7)
V2	P8_14	I(s)/O	—	—	A22	O	SPBIO01_0	I(s)/O	SPBIO00_1	I(s)/O	TIOC2A	I(s)/O	RSPCK2	I(s)/O	PWM1G	O	TxD4	O	SSIDATA4	I(s)/O	(7)
V4	Vss																				

Ball Number	Port Function/ Dedicated Function		Mode Function		Function 1		Function 2		Function 3		Function 4		Function 5		Function 6		Function 7		Function 8		Simplified Circuit Diagram Figure 2.1
	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	
V5	Vcc																				
V6	P3_6	I(s)/O	—	—	LCD0_TCON5	O	ET_RXDV	I(s)	SSIRxD1	I(s)	—	—	SCI_RXD0	I(s)	TIOC3C	I(s)/O	RxD3	I(s)	—	—	(7)
V7	P3_5	I(s)/O	—	—	LCD0_TCON4	O	ET_RXER	I(s)	SSIWS1	I(s)/O	AUDIO_XOUT3	O	SCI_TXD0	O	TIOC3B	I(s)/O	TxD3	O	—	—	(7)
V8	P3_1	I(s)/O	—	—	LCD0_TCON0	O	ET_TXER	O	IRQ6	I(s)	TxD2	O	SCI_TXD1	O	AUDIO_CLK	I(s)	PWM2B	O	SSL30	I(s)/O	(7)
V9	NMI	I(s)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(3)
V10	P0_4	I(s)	—	—	RTC_X3	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(3), (10)
V11	P0_5	I(s)	—	—	RTC_X4	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(3), (10)
V12	REFRIN	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
V13	USBAVcc																				
V14	P0_0	I(s)	MD_BOOT0	I(s)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(3)
V15	P1_9	I(s)	—	—	AN1	I(a)	—	—	IRQ3	I(s)	—	—	VIO_D15	I(s)	DV0_DATA15	I(s)	—	—	—	—	(4)
V16	P1_10	I(s)	—	—	AN2	I(a)	—	—	IRQ4	I(s)	TCLKB	I(s)	—	—	—	—	—	—	—	—	(4)
V17	P1_11	I(s)	—	—	AN3	I(a)	—	—	IRQ5	I(s)	TCLKD	I(s)	—	—	—	—	—	—	—	—	(4)
V18	Vcc																				
V20	VIDEO_X2	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(10)
V21	AUDIO_X1	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(10)
W1	P8_15	I(s)/O	—	—	A23	O	SPBIO11_0	I(s)/O	SPBIO10_1	I(s)/O	TIOC2B	I(s)/O	SSL20	I(s)/O	PWM1H	O	RxD4	I(s)	—	—	(7)
W2	PVcc																				
W20	Vss																				
W21	VIDEO_X1	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(10)
Y1	PVcc																				
Y2	Vss																				
Y3	Vcc																				
Y4	P9_0	I(s)/O	—	—	A24	O	SPBIO21_0	I(s)/O	CAN0TX	O	TCLKC	I(s)	MOSI2	I(s)/O	—	—	—	—	—	—	(7)
Y5	P3_4	I(s)/O	—	—	LCD0_TCON3	O	ET_RXCLK	I(s)	SSISCK1	I(s)/O	AUDIO_XOUT2	O	SCI_SCK0	I(s)/O	TIOC3A	I(s)/O	SCK3	I(s)/O	—	—	(7)
Y6	Vss																				
Y7	RTC_X2	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(11)
Y8	Vss																				
Y9	DP1	I/O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
Y10	VBUS1	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
Y11	DP0	I/O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
Y12	VBUS0	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
Y13	USB_X2	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(10)
Y14	Vss																				
Y15	P0_1	I(s)	MD_BOOT1	I(s)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(3)
Y16	P1_8	I(s)	—	—	AN0	I(a)	—	—	IRQ2	I(s)	DREQ0	I(s)	VIO_D14	I(s)	DV0_DATA14	I(s)	—	—	—	—	(4)
Y17	AVcc																				
Y18	P1_12	I(s)	—	—	AN4	I(a)	DV0_VSYNC	I(s)	—	—	VIO_FLD	I(s)	—	—	—	—	—	—	—	—	(4)
Y19	P1_14	I(s)	—	—	AN6	I(a)	—	—	—	—	ET_COL	I(s)	—	—	—	—	—	—	—	—	(4)
Y20	Vcc																				
Y21	Vss																				
AA1	Vss																				
AA2	Vcc																				
AA3	P9_1	I(s)/O	—	—	A25	O	SPBIO31_0	I(s)/O	CAN0RX	I(s)	IRQ0	I(s)	MISO2	I(s)/O	—	—	—	—	—	—	(7)
AA4	P3_7	I(s)/O	—	—	LCD0_TCON6	O	—	—	SSITxD1	O	LCD1_EXTCLK	I(s)	$\overline{\text{SCI\_CTS0}}$/RTS0	I(s)/O	TIOC3D	I(s)/O	$\overline{\text{CS1}}$	O	$\overline{\text{WDTOVF}}$	O	(7)
AA5	P3_2	I(s)/O	—	—	LCD0_TCON1	O	ET_TXEN	O	—	—	RxD2	I(s)	SCI_RXD1	I(s)	TEND0	O	PWM2C	O	MOSI3	I(s)/O	(7)
AA6	P3_0	I(s)/O	—	—	LCD0_CLK	O	ET_TXCLK	I(s)	IRQ2	I(s)	SCK2	I(s)/O	SCI_SCK1	I(s)/O	TxD2	O	PWM2A	O	RSPCK3	I(s)/O	(7)
AA7	RTC_X1	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(11)
AA8	Vss																				
AA9	DM1	I/O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
AA10	Vss																				
AA11	DM0	I/O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
AA12	Vss																				
AA13	USB_X1	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(10)
AA14	EXTAL	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(10)
AA15	XTAL	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(10)

Ball Number	Port Function/ Dedicated Function		Mode Function		Function 1		Function 2		Function 3		Function 4		Function 5		Function 6		Function 7		Function 8		Simplified Circuit Diagram Figure 2.1
	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	
AA16	Vss																				
AA17	AVss																				
AA18	AVref																				
AA19	P1_13	I(s)	—	—	AN5	I(a)	DV0_HSYNC	I(s)	—	—	$\overline{\text{WAIT}}$	I(s)	—	—	—	—	—	—	—	—	(4)
AA20	P1_15	I(s)	—	—	AN7	I(a)	—	—	—	—	AVB_CAPTURE	I(s)	—	—	—	—	—	—	—	—	(4)
AA21	Vcc																				

[Legend]
(s): Schmitt
(a): Analog
(o): Open drain

Table 2.3 List of Pins (256-Pin, QFP)

No.	Port Function/ Dedicated Function		Mode Function		Function 1		Function 2		Function 3		Function 4		Function 5		Function 6		Function 7		Function 8		Simplified Circuit Diagram Figure 2.1
	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	
1	P6_5	I(s)/O	—	—	D5	I(s)/O	LCD1_ DATA13	O	CAN2TX	O	—	—	SCK5	I(s)/O	—	—	SSL10	I(s)/O	DV0_ DATA21	I(s)	(8)
2	P6_6	I(s)/O	—	—	D6	I(s)/O	LCD1_ DATA14	O	—	—	LCD0_ TCON5	O	TxD5	O	—	—	MOSI1	I(s)/O	DV0_ DATA22	I(s)	(8)
3	P6_7	I(s)/O	—	—	D7	I(s)/O	LCD1_ DATA15	O	—	—	LCD0_ TCON6	O	RxD5	I(s)	—	—	MISO1	I(s)/O	DV0_ DATA23	I(s)	(8)
4	Vcc																				
5	P6_8	I(s)/O	—	—	D8	I(s)/O	DV0_ DATA12	I(s)	—	—	CAN_CLK	I(s)	SCK0	I(s)/O	LCD0_ DATA0	O	—	—	IRQ0	I(s)	(8)
6	Vss																				
7	P6_9	I(s)/O	—	—	D9	I(s)/O	DV0_ DATA13	I(s)	—	—	—	—	TxD0	O	LCD0_ DATA1	O	—	—	IRQ1	I(s)	(8)
8	PVcc																				
9	P6_10	I(s)/O	—	—	D10	I(s)/O	DV0_ DATA14	I(s)	—	—	LCD0_ TCON5	O	RxD0	I(s)	LCD0_ DATA2	O	—	—	IRQ2	I(s)	(8)
10	P6_11	I(s)/O	—	—	D11	I(s)/O	DV0_ DATA15	I(s)	—	—	LCD0_ TCON6	O	SCK1	I(s)/O	LCD0_ DATA3	O	—	—	IRQ3	I(s)	(8)
11	P6_12	I(s)/O	—	—	D12	I(s)/O	DV0_ DATA20	I(s)	—	—	—	—	TxD1	O	LCD0_ DATA4	O	—	—	IRQ4	I(s)	(8)
12	P6_13	I(s)/O	—	—	D13	I(s)/O	DV0_ DATA21	I(s)	—	—	SCK6	I(s)/O	RxD1	I(s)	LCD0_ DATA5	O	—	—	IRQ5	I(s)	(8)
13	P6_14	I(s)/O	—	—	D14	I(s)/O	DV0_ DATA22	I(s)	—	—	TxD6	O	—	—	LCD0_ DATA6	O	—	—	IRQ6	I(s)	(8)
14	P6_15	I(s)/O	—	—	D15	I(s)/O	DV0_ DATA23	I(s)	—	—	RxD6	I(s)	—	—	LCD0_ DATA7	O	—	—	IRQ7	I(s)	(8)
15	P7_0	I(s)/O	MD_BOOT2	I(s)	$\overline{CS0}$	O	DV0_ DATA16	I(s)	ET_MDC	O	SCK4	I(s)/O	RLIN30TX	O	—	—	TIOC0A	I(s)/O	—	—	(7)
16	Vss																				
17	P7_1	I(s)/O	—	—	$\overline{CS3}$	O	DV0_ DATA17	I(s)	ET_TXCLK	I(s)	TxD4	O	DV0_CLK	I(s)	SSISCK1	I(s)/O	TIOC0B	I(s)/O	—	—	(7)
18	Vcc																				
19	P7_2	I(s)/O	—	—	$\overline{RAS}$	O	DV0_ DATA18	I(s)	ET_TXER	O	RxD4	I(s)	CAN2RX	I(s)	SSIWS1	I(s)/O	TIOC0C	I(s)/O	—	—	(7)
20	Vss																				
21	P7_3	I(s)/O	—	—	$\overline{CAS}$	O	DV0_ DATA19	I(s)	ET_TXEN	O	SCK7	I(s)/O	CAN2TX	O	SSIRxD1	I(s)	TIOC0D	I(s)/O	—	—	(7)
22	PVcc																				
23	P7_4	I(s)/O	—	—	CKE	O	DV0_ DATA20	I(s)	ET_TXD0	O	TxD7	O	—	—	SSITxD1	O	TIOC1A	I(s)/O	—	—	(7)
24	P7_5	I(s)/O	—	—	RD/$\overline{WR}$	O	DV0_ DATA21	I(s)	ET_TXD1	O	RxD7	I(s)	—	—	SSISCK2	I(s)/O	TIOC1B	I(s)/O	—	—	(7)
25	P7_6	I(s)/O	—	—	$\overline{WE0}$/ DQMLL	O	DV0_ DATA22	I(s)	ET_TXD2	O	$\overline{CTS7}$	I(s)/O	—	—	SSIWS2	I(s)/O	TIOC2A	I(s)/O	—	—	(7)
26	P7_7	I(s)/O	—	—	$\overline{WE1}$/ DQMLU	O	DV0_ DATA23	I(s)	ET_TXD3	O	$\overline{RTS7}$	I(s)/O	—	—	SSIDATA2	I(s)/O	TIOC2B	I(s)/O	—	—	(7)
27	P7_8	I(s)/O	—	—	$\overline{RD}$	O	SSISCK3	I(s)/O	—	—	CAN0RX	I(s)	—	—	—	—	TIOC3A	I(s)/O	IRQ1	I(s)	(7)
28	P7_9	I(s)/O	—	—	A1	O	SSIWS3	I(s)/O	ET_RXD0	I(s)	CAN0TX	O	—	—	—	—	TIOC3B	I(s)/O	IRQ0	I(s)	(7)
29	Vcc																				
30	P7_10	I(s)/O	—	—	A2	O	SSIRxD3	I(s)	ET_RXD1	I(s)	CAN1TX	O	—	—	—	—	TIOC3C	I(s)/O	IRQ2	I(s)	(7)
31	Vss																				
32	P7_11	I(s)/O	—	—	A3	O	SSITxD3	O	ET_RXD2	I(s)	CAN1RX	I(s)	—	—	—	—	TIOC3D	I(s)/O	IRQ3	I(s)	(7)
33	Vcc																				
34	P7_12	I(s)/O	—	—	A4	O	SSISCK4	I(s)/O	ET_RXD3	I(s)	—	—	—	—	—	—	TIOC4A	I(s)/O	IRQ4	I(s)	(7)
35	Vss																				
36	P7_13	I(s)/O	—	—	A5	O	SSIWS4	I(s)/O	ET_MDIO	I(s)/O	—	—	—	—	—	—	TIOC4B	I(s)/O	IRQ5	I(s)	(7)
37	PVcc																				
38	P7_14	I(s)/O	—	—	A6	O	SSIDATA4	I(s)/O	ET_CRS	I(s)	—	—	—	—	—	—	TIOC4C	I(s)/O	IRQ6	I(s)	(7)
39	P7_15	I(s)/O	—	—	A7	O	RSPCK0	I(s)/O	ET_RXCLK	I(s)	$\overline{CTS5}$	I(s)/O	SCI_TXD0	O	—	—	TIOC4D	I(s)/O	—	—	(7)
40	P8_0	I(s)/O	—	—	A8	O	SSL00	I(s)/O	ET_RXER	I(s)	SCK5	I(s)/O	SCI_SCK0	I(s)/O	—	—	—	—	—	—	(7)

No.	Port Function/ Dedicated Function		Mode Function		Function 1		Function 2		Function 3		Function 4		Function 5		Function 6		Function 7		Function 8		Simplified Circuit Diagram Figure 2.1
	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	
41	P8_1	I(s)/O	—	—	A9	O	MOSI0	I(s)/O	ET_RXDV	I(s)	TxD5	O	SCI_RXD0	I(s)	—	—	—	—	—	—	(7)
42	P8_2	I(s)/O	—	—	A10	O	MISO0	I(s)/O	AVB_GPTP_EXTERN	I(s)	RxD5	I(s)	IRQ0	I(s)	—	—	—	—	—	—	(7)
43	P8_3	I(s)/O	—	—	A11	O	DV1_DATA0	I(s)	RSPCK2	I(s)/O	$\overline{\text{RTS5}}$	I(s)/O	—	—	IRQ1	I(s)	SCK2	I(s)/O	—	—	(7)
44	P8_4	I(s)/O	—	—	A12	O	DV1_DATA1	I(s)	SSL20	I(s)/O	—	—			IERxD	I(s)	RxD2	I(s)	—	—	(7)
45	P8_5	I(s)/O	—	—	A13	O	DV1_DATA2	I(s)	MOSI2	I(s)/O	—	—	—	—	—	—	—	—	—	—	(7)
46	PVcc																				
47	P8_6	I(s)/O	—	—	A14	O	DV1_DATA3	I(s)	MISO2	I(s)/O	—	—	—	—	IETxD	O	TxD2	O	—	—	(7)
48	Vss																				
49	CKIO	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(5)
50	Vcc																				
51	P8_7	I(s)/O	—	—	A15	O	DV1_DATA4	I(s)	AUDIO_XOUT	O	IRQ5	I(s)	ET_COL	I(s)	—	—	—	—	—	—	(7)
52	Vss																				
53	Vss																				
54	P8_8	I(s)/O	—	—	A16	O	DV1_DATA5	I(s)	SPBIO00_1	I(s)/O	SPDIF_IN	I(s)	TIOC1A	I(s)/O	PWM1A	O	TxD3	O	SSISCK5	I(s)/O	(7)
55	P8_9	I(s)/O	—	—	A17	O	DV1_DATA6	I(s)	SPBIO10_1	I(s)/O	SPDIF_OUT	O	TIOC1B	I(s)/O	PWM1B	O	RxD3	I(s)	SSIWS5	I(s)/O	(7)
56	P8_10	I(s)/O	—	—	A18	O	DV1_DATA7	I(s)	SPBIO20_1	I(s)/O	TIOC3A	I(s)/O	CAN4TX	O	PWM1C	O	SGOUT_0	O	SSITxD5	O	(7)
57	P8_11	I(s)/O	—	—	A19	O	—	—	SPBIO30_1	I(s)/O	TIOC3B	I(s)/O	RxD5	I(s)	PWM1D	O	SGOUT_1	O	DV0_CLK	I(s)	(7)
58	P8_12	I(s)/O	—	—	A20	O	—	—	SPBCLK_1	O	TIOC3C	I(s)/O	SCK5	I(s)/O	PWM1E	O	SGOUT_2	O	SSISCK4	I(s)/O	(7)
59	P8_13	I(s)/O	—	—	A21	O	—	—	SPBSSL_1	O	TIOC3D	I(s)/O	TxD5	O	PWM1F	O	SGOUT_3	O	SSIWS4	I(s)/O	(7)
60	PVcc																				
61	P8_14	I(s)/O	—	—	A22	O	SPBIO01_0	I(s)/O	SPBIO00_1	I(s)/O	TIOC2A	I(s)/O	RSPCK2	I(s)/O	PWM1G	O	TxD4	O	SSIDATA4	I(s)/O	(7)
62	Vss																				
63	P8_15	I(s)/O	—	—	A23	O	SPBIO11_0	I(s)/O	SPBIO10_1	I(s)/O	TIOC2B	I(s)/O	SSL20	I(s)/O	PWM1H	O	RxD4	I(s)	—	—	(7)
64	Vcc																				
65	P9_0	I(s)/O	—	—	A24	O	SPBIO21_0	I(s)/O	CAN0TX	O	TCLKC	I(s)	MOSI2	I(s)/O	—	—	—	—	—	—	(7)
66	P9_1	I(s)/O	—	—	A25	O	SPBIO31_0	I(s)/O	CAN0RX	I(s)	IRQ0	I(s)	MISO2	I(s)/O	—	—	—	—	—	—	(7)
67	P3_7	I(s)/O	—	—	LCD0_TCON6	O	—	—	SSITxD1	O	LCD1_EXTCLK	I(s)	$\overline{\text{SCI\_CTS0}}$/ $\overline{\text{RTS0}}$	I(s)/O	TIOC3D	I(s)/O	$\overline{\text{CS1}}$	O	$\overline{\text{WDTOVF}}$	O	(7)
68	P3_6	I(s)/O	—	—	LCD0_TCON5	O	ET_RXDV	I(s)	SSIRxD1	I(s)	—	—	SCI_RXD0	I(s)	TIOC3C	I(s)/O	RxD3	I(s)	—	—	(7)
69	P3_5	I(s)/O	—	—	LCD0_TCON4	O	ET_RXER	I(s)	SSIWS1	I(s)/O	AUDIO_XOUT3	O	SCI_TXD0	O	TIOC3B	I(s)/O	TxD3	O	—	—	(7)
70	P3_4	I(s)/O	—	—	LCD0_TCON3	O	ET_RXCLK	I(s)	SSISCK1	I(s)/O	AUDIO_XOUT2	O	SCI_SCK0	I(s)/O	TIOC3A	I(s)/O	SCK3	I(s)/O	—	—	(7)
71	P3_3	I(s)/O	—	—	LCD0_TCON2	O	ET_MDIO	I(s)/O	IRQ4	I(s)	$\overline{\text{BS}}$	O	$\overline{\text{SCI\_CTS1}}$/ $\overline{\text{RTS1}}$	I(s)/O	DACK0	O	PWM2D	O	MISO3	I(s)/O	(7)
72	P3_2	I(s)/O	—	—	LCD0_TCON1	O	ET_TXEN	O	—	—	RxD2	I(s)	SCI_RXD1	I(s)	TEND0	O	PWM2C	O	MOSI3	I(s)/O	(7)
73	PVcc																				
74	P3_1	I(s)/O	—	—	LCD0_TCON0	O	ET_TXER	O	IRQ6	I(s)	TxD2	O	SCI_TXD1	O	AUDIO_CLK	I(s)	PWM2B	O	SSL30	I(s)/O	(7)
75	Vss																				
76	P3_0	I(s)/O	—	—	LCD0_CLK	O	ET_TXCLK	I(s)	IRQ2	I(s)	SCK2	I(s)/O	SCI_SCK1	I(s)/O	TxD2	O	PWM2A	O	RSPCK3	I(s)/O	(7)
77	$\overline{\text{RES}}$	I(s)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(1)
78	NMI	I(s)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(3)
79	PVcc																				
80	RTC_X1	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(11)
81	RTC_X2	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(11)
82	Vss																				

No.	Port Function/ Dedicated Function		Mode Function		Function 1		Function 2		Function 3		Function 4		Function 5		Function 6		Function 7		Function 8		Simplified Circuit Diagram Figure 2.1
	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	
83	Vss																				
84	P0_4	I(s)	—	—	RTC_X3	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(3), (10)
85	P0_5	I(s)	—	—	RTC_X4	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(3), (10)
86	Vcc																				
87	USBDPVcc																				
88	USBDPVss																				
89	DM1	I/O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
90	DP1	I/O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
91	VBUS1	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
92	USBDVcc																				
93	USBDVss																				
94	USBDPVcc																				
95	USBDPVss																				
96	DM0	I/O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
97	DP0	I/O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
98	VBUS0	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
99	USBDVcc																				
100	USBDVss																				
101	REFRIN	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
102	USBAPVss																				
103	USBAPVcc																				
104	USBAVcc																				
105	USBAVss																				
106	USBUVcc																				
107	USBUVss																				
108	USB_X1	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(10)
109	USB_X2	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(10)
110	P0_0	I(s)	MD_BOOT0	I(s)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(3)
111	Vss																				
112	EXTAL	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(10)
113	XTAL	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(10)
114	PLLVcc																				
115	PVcc																				
116	P0_1	I(s)	MD_BOOT1	I(s)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(3)
117	Vss																				
118	P1_8	I(s)	—	—	AN0	I(a)	—	—	IRQ2	I(s)	DREQ0	I(s)	VIO_D14	I(s)	DV0_ DATA14	I(s)	—	—	—	—	(4)
119	AVcc																				
120	AVss																				
121	AVref																				
122	P1_9	I(s)	—	—	AN1	I(a)	—	—	IRQ3	I(s)	—	—	VIO_D15	I(s)	DV0_ DATA15	I(s)	—	—	—	—	(4)
123	P1_10	I(s)	—	—	AN2	I(a)	—	—	IRQ4	I(s)	TCLKB	I(s)	—	—	—	—	—	—	—	—	(4)
124	P1_11	I(s)	—	—	AN3	I(a)	—	—	IRQ5	I(s)	TCLKD	I(s)	—	—	—	—	—	—	—	—	(4)
125	P1_12	I(s)	—	—	AN4	I(a)	DV0_ VSYNC	I(s)	—	—	VIO_FLD	I(s)	—	—	—	—	—	—	—	—	(4)
126	P1_13	I(s)	—	—	AN5	I(a)	DV0_ HSYNC	I(s)	—	—	$\overline{\text{WAIT}}$	I(s)	—	—	—	—	—	—	—	—	(4)
127	P1_14	I(s)	—	—	AN6	I(a)	—	—	—	—	ET_COL	I(s)	—	—	—	—	—	—	—	—	(4)
128	P1_15	I(s)	—	—	AN7	I(a)	—	—	—	—	AVB_ CAPTURE	I(s)	—	—	—	—	—	—	—	—	(4)
129	BSCANP	I(s)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(1)
130	VIDEO_X1	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(10)
131	VIDEO_X2	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(10)

No.	Port Function/ Dedicated Function		Mode Function		Function 1		Function 2		Function 3		Function 4		Function 5		Function 6		Function 7		Function 8		Simplified Circuit Diagram Figure 2.1
	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	
132	Vss																				
133	AUDIO_X1	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(10)
134	AUDIO_X2	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(10)
135	PVcc																				
136	P3_8	I(s)/O	—	—	LCD0_DATA0	O	—	—	NAF0	I(s)/O	—	—	TRACEDATA0	O	TIOC4A	I(s)/O	SD_CD_1	I(s)	MMC_CD	I(s)	(7)
137	Vss																				
138	P3_9	I(s)/O	—	—	LCD0_DATA1	O	—	—	NAF1	I(s)/O	—	—	TRACEDATA1	O	TIOC4B	I(s)/O	SD_WP_1	I(s)	IRQ6	I(s)	(7)
139	Vcc																				
140	$\overline{\text{TRST}}$	I(s)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(3)
141	JP0_1	I	—	—	TDO	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(6)
142	JP0_0	I	—	—	TDI	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(2)
143	TMS	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(6)
144	TCK	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(2)
145	P3_10	I(s)/O	—	—	LCD0_DATA2	O	—	—	NAF2	I(s)/O	—	—	TRACEDATA2	O	TIOC4C	I(s)/O	SD_D1_1	I(s)/O	MMC_D1	I(s)/O	(7)
146	P3_11	I(s)/O	—	—	LCD0_DATA3	O	—	—	NAF3	I(s)/O	—	—	TRACEDATA3	O	TIOC4D	I(s)/O	SD_D0_1	I(s)/O	MMC_D0	I(s)/O	(7)
147	PVcc																				
148	P3_12	I(s)/O	—	—	LCD0_DATA4	O	—	—	NAF4	I(s)/O	—	—	—	—	—	—	SD_CLK_1	O	MMC_CLK	O	(7)
149	Vss																				
150	P3_13	I(s)/O	—	—	LCD0_DATA5	O	—	—	NAF5	I(s)/O	AUDIO_XOUT	O	—	—	—	—	SD_CMD_1	I(s)/O	MMC_CMD	I(s)/O	(7)
151	Vcc																				
152	P3_14	I(s)/O	—	—	LCD0_DATA6	O	—	—	NAF6	I(s)/O	—	—	TRACECLK	O	—	—	SD_D3_1	I(s)/O	MMC_D3	I(s)/O	(7)
153	P3_15	I(s)/O	—	—	LCD0_DATA7	O	—	—	NAF7	I(s)/O	—	—	TRACECTL	O	—	—	SD_D2_1	I(s)/O	MMC_D2	I(s)/O	(7)
154	Vss																				
155	P4_0	I(s)/O	—	—	LCD0_DATA8	O	TIOC0A	I(s)/O	$\overline{\text{FRE}}$	O	—	—	—	—	—	—	RSPCK4	I(s)/O	MMC_D4	I(s)/O	(7)
156	P4_1	I(s)/O	—	—	LCD0_DATA9	O	TIOC0B	I(s)/O	FCLE	O	—	—	SCK2	I(s)/O	—	—	SSL40	I(s)/O	MMC_D5	I(s)/O	(7)
157	P4_2	I(s)/O	—	—	LCD0_DATA10	O	TIOC0C	I(s)/O	FALE	O	CAN3RX	I(s)	TxD2	O	—	—	MOSI4	I(s)/O	MMC_D6	I(s)/O	(7)
158	P4_3	I(s)/O	—	—	LCD0_DATA11	O	TIOC0D	I(s)/O	$\overline{\text{FWE}}$	O	CAN3TX	O	RxD2	I(s)	—	—	MISO4	I(s)/O	MMC_D7	I(s)/O	(7)
159	PVcc																				
160	P4_4	I(s)/O	—	—	LCD0_DATA12	O	RSPCK1	I(s)/O	TIOC4A	I(s)/O	PWM2E	O	SSISCK0	I(s)/O	—	—	DV0_DATA12	I(s)	—	—	(7)
161	Vss																				
162	P4_5	I(s)/O	—	—	LCD0_DATA13	O	SSL10	I(s)/O	TIOC4B	I(s)/O	PWM2F	O	SSIWS0	I(s)/O	—	—	DV0_DATA13	I(s)	—	—	(7)
163	Vcc																				
164	P4_6	I(s)/O	—	—	LCD0_DATA14	O	MOSI1	I(s)/O	TIOC4C	I(s)/O	PWM2G	O	SSIRxD0	I(s)	—	—	DV0_DATA14	I(s)	—	—	(7)
165	P4_7	I(s)/O	—	—	LCD0_DATA15	O	MISO1	I(s)/O	TIOC4D	I(s)/O	PWM2H	O	SSITxD0	O	—	—	DV0_DATA15	I(s)	—	—	(7)
166	P2_0	I(s)/O	—	—	D16	I(s)/O	ET_TXCLK	I(s)	DV0_DATA0	I(s)	SPBIO00_1	I(s)/O	MLB_CLK	I(s)	IRQ5	I(s)	VIO_D0	I(s)	LCD0_DATA16	O	(8)
167	P2_1	I(s)/O	—	—	D17	I(s)/O	ET_TXER	O	DV0_DATA1	I(s)	SPBIO10_1	I(s)/O	MLB_DAT	I(s)/O	TIOC2A	I(s)/O	VIO_D1	I(s)	LCD0_DATA17	O	(8)
168	P4_8	I(s)/O	—	—	LCD0_DATA16	O	LCD1_TCON3	O	SD_CD_0	I(s)	MMC_CD	I(s)	SSISCK5	I(s)/O	CAN2TX	O	SCK0	I(s)/O	IRQ0	I(s)	(7)
169	P4_9	I(s)/O	—	—	LCD0_DATA17	O	LCD1_TCON4	O	SD_WP_0	I(s)	—	—	SSIWS5	I(s)/O	CAN2RX	I(s)	TxD0	O	IRQ1	I(s)	(7)
170	P4_10	I(s)/O	—	—	LCD0_DATA18	O	LCD1_TCON5	O	SD_D1_0	I(s)/O	MMC_D1	I(s)/O	SSIRxD5	I(s)	—	—	RxD0	I(s)	IRQ2	I(s)	(7)

No.	Port Function/ Dedicated Function		Mode Function		Function 1		Function 2		Function 3		Function 4		Function 5		Function 6		Function 7		Function 8		Simplified Circuit Diagram Figure 2.1
	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	
171	P4_11	I(s)/O	—	—	LCD0_ DATA19	O	LCD1_ TCON6	O	SD_D0_0	I(s)/O	MMC_D0	I(s)/O	SSITxD5	O	CAN4TX	O	SCK1	I(s)/O	IRQ3	I(s)	(7)
172	PVcc																				
173	P4_12	I(s)/O	—	—	LCD0_ DATA20	O	LCD1_CLK	O	SD_CLK_0	O	MMC_CLK	O	SPBIO01_1	I(s)/O	SSISCK3	I(s)/O	TxD1	O	IRQ4	I(s)	(7)
174	Vss																				
175	P4_13	I(s)/O	—	—	LCD0_ DATA21	O	LCD1_ TCON0	O	SD_CMD_0	I(s)/O	MMC_CMD	I(s)/O	SPBIO11_1	I(s)/O	SSIWS3	I(s)/O	RxD1	I(s)	IRQ5	I(s)	(7)
176	Vcc																				
177	P4_14	I(s)/O	—	—	LCD0_ DATA22	O	LCD1_ TCON1	O	SD_D3_0	I(s)/O	MMC_D3	I(s)/O	SPBIO21_1	I(s)/O	SSIRxD3	I(s)	TxD2	O	IRQ6	I(s)	(7)
178	P4_15	I(s)/O	—	—	LCD0_ DATA23	O	LCD1_ TCON2	O	SD_D2_0	I(s)/O	MMC_D2	I(s)/O	SPBIO31_1	I(s)/O	SSITxD3	O	RxD2	I(s)	IRQ7	I(s)	(7)
179	P2_2	I(s)/O	—	—	D18	I(s)/O	ET_TXEN	O	DV0_DATA2	I(s)	SPBIO20_1	I(s)/O	MLB_SIG	I(s)/O	TIOC2B	I(s)/O	VIO_D2	I(s)	LCD0_ DATA18	O	(8)
180	P2_3	I(s)/O	—	—	D19	I(s)/O	ET_CRS	I(s)	DV0_DATA3	I(s)	SPBIO30_1	I(s)/O	IERxD	I(s)	$\overline{\text{CTS1}}$	I(s)/O	VIO_D3	I(s)	LCD0_ DATA19	O	(8)
181	P2_4	I(s)/O	—	—	D20	I(s)/O	ET_TXD0	O	DV0_DATA4	I(s)	SSISCK5	I(s)/O	SPBCLK_1	O	SCK1	I(s)/O	VIO_D4	I(s)	LCD0_ DATA20	O	(8)
182	P2_5	I(s)/O	—	—	D21	I(s)/O	ET_TXD1	O	DV0_DATA5	I(s)	SSIWS5	I(s)/O	SPBSSL_1	O	TxD1	O	VIO_D5	I(s)	LCD0_ DATA21	O	(8)
183	P2_6	I(s)/O	—	—	D22	I(s)/O	ET_TXD2	O	DV0_DATA6	I(s)	SSIRxD5	I(s)	—	—	RxD1	I(s)	VIO_D6	I(s)	LCD0_ DATA22	O	(8)
184	PVcc																				
185	P2_7	I(s)/O	—	—	D23	I(s)/O	ET_TXD3	O	DV0_DATA7	I(s)	SSITxD5	O	IETxD	O	$\overline{\text{RTS1}}$	I(s)/O	VIO_D7	I(s)	LCD0_ DATA23	O	(8)
186	P2_8	I(s)/O	—	—	D24	I(s)/O	ET_RXD0	I(s)	DV0_DATA8	I(s)	SSISCK0	I(s)/O	LCD0_ TCON6	O	LCD1_ DATA8	O	VIO_D8	I(s)	RSPCK4	I(s)/O	(8)
187	Vss																				
188	P2_9	I(s)/O	—	—	D25	I(s)/O	ET_RXD1	I(s)	DV0_DATA9	I(s)	SSIWS0	I(s)/O	RLIN30RX	I(s)	LCD1_ DATA9	O	VIO_D9	I(s)	SSL40	I(s)/O	(8)
189	Vcc																				
190	P2_10	I(s)/O	—	—	D26	I(s)/O	ET_RXD2	I(s)	DV0_ DATA10	I(s)	SSIRxD0	I(s)	RLIN30TX	O	LCD1_ DATA10	O	VIO_D10	I(s)	MOSI4	I(s)/O	(8)
191	P2_11	I(s)/O	—	—	D27	I(s)/O	ET_RXD3	I(s)	DV0_ DATA11	I(s)	SSITxD0	O	TIOC1A	I(s)/O	LCD1_ DATA11	O	VIO_D11	I(s)	MISO4	I(s)/O	(8)
192	Vss																				
193	P2_12	I(s)/O	—	—	D28	I(s)/O	RSPCK0	I(s)/O	DV0_ DATA12	I(s)	SPBIO01_0	I(s)/O	CAN3RX	I(s)	IRQ6	I(s)	LCD1_ DATA12	O	TIOC1B	I(s)/O	(8)
194	P2_13	I(s)/O	—	—	D29	I(s)/O	SSL00	I(s)/O	DV0_ DATA13	I(s)	SPBIO11_0	I(s)/O	CAN3TX	O	SCK0	I(s)/O	LCD1_ DATA13	O	IRQ7	I(s)	(8)
195	P2_14	I(s)/O	—	—	D30	I(s)/O	MOSI0	I(s)/O	DV0_ DATA14	I(s)	SPBIO21_0	I(s)/O	CAN4RX	I(s)	TxD0	O	LCD1_ DATA14	O	IRQ0	I(s)	(8)
196	P2_15	I(s)/O	—	—	D31	I(s)/O	MISO0	I(s)/O	DV0_ DATA15	I(s)	SPBIO31_0	I(s)/O	CAN_CLK	I(s)	RxD0	I(s)	LCD1_ DATA15	O	IRQ1	I(s)	(8)
197	P1_0	I(s)/ O(o)	—	—	RIIC0SCL	I(s)/ O(o)	DV0_ DATA16	I(s)	TCLKA	I(s)	IRQ0	I(s)	VIO_VD	I(s)	DV0_ VSYNC	I(s)	—	—	—	—	(9)
198	P1_1	I(s)/ O(o)	—	—	RIIC0SDA	I(s)/ O(o)	DV0_ DATA17	I(s)	TCLKC	I(s)	IRQ1	I(s)	VIO_HD	I(s)	DV0_ HSYNC	I(s)	—	—	—	—	(9)
199	P1_2	I(s)/ O(o)	—	—	RIIC1SCL	I(s)/ O(o)	DV0_ DATA18	I(s)	FRB	I(s)	IRQ2	I(s)	—	—	—	—	LCD1_ EXTCLK	I(s)	—	—	(9)
200	P1_3	I(s)/ O(o)	—	—	RIIC1SDA	I(s)/ O(o)	DV0_ DATA19	I(s)	ET_COL	I(s)	IRQ3	I(s)	$\overline{\text{ADTRG}}$	I(s)	—	—	—	—	—	—	(9)
201	P1_4	I(s)/ O(o)	—	—	RIIC2SCL	I(s)/ O(o)	DV0_CLK	I(s)	CAN1RX	I(s)	IRQ4	I(s)	—	—	—	—	CAN_CLK	I(s)	—	—	(9)
202	P1_5	I(s)/ O(o)	—	—	RIIC2SDA	I(s)/ O(o)	DV1_CLK	I(s)	CAN4RX	I(s)	IRQ5	I(s)	VIO_CLK	I(s)	—	—	LCD1_ EXTCLK	I(s)	—	—	(9)
203	P1_6	I(s)/ O(o)	—	—	RIIC3SCL	I(s)/ O(o)	DV1_ VSYNC	I(s)	IERxD	I(s)	IRQ6	I(s)	VIO_D12	I(s)	DV0_ DATA12	I(s)	—	—	—	—	(9)
204	P1_7	I(s)/ O(o)	—	—	RIIC3SDA	I(s)/ O(o)	DV1_ HSYNC	I(s)	RLIN30RX	I(s)	IRQ7	I(s)	VIO_D13	I(s)	DV0_ DATA13	I(s)	—	—	—	—	(9)
205	P0_2	I(s)	MD_CLK	I(s)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(3)
206	PVcc																				
207	Vss																				

No.	Port Function/ Dedicated Function		Mode Function		Function 1		Function 2		Function 3		Function 4		Function 5		Function 6		Function 7		Function 8		Simplified Circuit Diagram Figure 2.1
	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	
208	VIN1A	I(a)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
209	VIN2A	I(a)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
210	VDAVcc																				
211	VDAVss																				
212	REXT	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
213	VRP	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
214	VRM	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
215	VIN1B	I(a)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
216	VIN2B	I(a)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
217	PVcc																				
218	Vss																				
219	Vcc																				
220	Vss																				
221	LVDSAPVss																				
222	LVDSREFRIN	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
223	LVDSAPVcc																				
224	P5_0	I(s)/O	—	—	TXCLKOUTP	O	LCD1_DATA0	O	LCD0_DATA16	O	DV1_DATA0	I(s)	TxD4	O	TIOC0A	I(s)/O	—	—	RSPCK3	I(s)/O	(12), (13)
225	LVDSAPVss																				
226	P5_1	I(s)/O	—	—	TXCLKOUTM	O	LCD1_DATA1	O	LCD0_DATA17	O	DV1_DATA1	I(s)	RxD4	I(s)	TIOC0B	I(s)/O	—	—	SSL30	I(s)/O	(12), (13)
227	P5_2	I(s)/O	—	—	TXOUT2P	O	LCD1_DATA2	O	LCD0_DATA18	O	DV1_DATA2	I(s)	SCK3	I(s)/O	TIOC1B	I(s)/O	—	—	MOSI3	I(s)/O	(12), (13)
228	LVDSAPVcc																				
229	P5_3	I(s)/O	—	—	TXOUT2M	O	LCD1_DATA3	O	LCD0_DATA19	O	DV1_DATA3	I(s)	TxD3	O	TIOC3C	I(s)/O	—	—	MISO3	I(s)/O	(12), (13)
230	P5_4	I(s)/O	—	—	TXOUT1P	O	LCD1_DATA4	O	LCD0_DATA20	O	DV1_DATA4	I(s)	RxD3	I(s)	TIOC3D	I(s)/O	—	—	DV0_DATA12	I(s)	(12), (13)
231	LVDSAPVss																				
232	P5_5	I(s)/O	—	—	TXOUT1M	O	LCD1_DATA5	O	LCD0_DATA21	O	DV1_DATA5	I(s)	AUDIO_XOUT	O	TIOC0C	I(s)/O	$\overline{FCE}$	O	DV0_DATA13	I(s)	(12), (13)
233	P5_6	I(s)/O	—	—	TXOUT0P	O	LCD1_DATA6	O	LCD0_DATA22	O	DV1_DATA6	I(s)	TxD6	O	IRQ6	I(s)	SPDIF_IN	I(s)	DV0_DATA14	I(s)	(12), (13)
234	LVDSAPVcc																				
235	P5_7	I(s)/O	—	—	TXOUT0M	O	LCD1_DATA7	O	LCD0_DATA23	O	DV1_DATA7	I(s)	RxD6	I(s)	TIOC0D	I(s)/O	SPDIF_OUT	O	DV0_DATA15	I(s)	(12), (13)
236	LVDSPLLVcc																				
237	Vss																				
238	Vss																				
239	PVcc																				
240	P5_8	I(s)/O	—	—	LCD0_EXTCLK	I(s)	IRQ0	I(s)	DV1_CLK	I(s)	—	—	DV0_CLK	I(s)	$\overline{CS2}$	O	—	—	—	—	(7)
241	P5_9	I(s)/O	—	—	$\overline{WE2}$/DQMUL	O	ET_MDC	O	DV0_VSYNC	I(s)	IRQ2	I(s)	CAN1RX	I(s)	IERxD	I(s)	LCD1_DATA16	O	—	—	(7)
242	P5_10	I(s)/O	—	—	$\overline{WE3}$/DQMUU/$\overline{AH}$	O	—	—	DV0_HSYNC	I(s)	—	—	CAN1TX	O	IETxD	O	LCD1_DATA17	O	—	—	(7)
243	P9_2	I(s)/O	—	—	LCD1_DATA18	O	SPBCLK_0	O	RLIN30TX	O	SCK1	I(s)/O	A0	O	—	—	—	—	—	—	(7)
244	P9_3	I(s)/O	—	—	LCD1_DATA19	O	SPBSSL_0	O	—	—	TxD1	O	—	—	—	—	—	—	—	—	(7)
245	P9_4	I(s)/O	—	—	LCD1_DATA20	O	SPBIO00_0	I(s)/O	—	—	RxD1	I(s)	—	—	—	—	—	—	—	—	(7)
246	P9_5	I(s)/O	—	—	LCD1_DATA21	O	SPBIO10_0	I(s)/O	SSISCK2	I(s)/O	$\overline{CTS1}$	I(s)/O	$\overline{CS4}$	O	—	—	—	—	—	—	(7)
247	P9_6	I(s)/O	—	—	LCD1_DATA22	O	SPBIO20_0	I(s)/O	SSIWS2	I(s)/O	$\overline{RTS1}$	I(s)/O	$\overline{CS5}$	O	—	—	—	—	—	—	(7)
248	P9_7	I(s)/O	—	—	LCD1_DATA23	O	SPBIO30_0	I(s)/O	SSIDATA2	I(s)/O	TIOC1A	I(s)/O	—	—	—	—	—	—	—	—	(7)

No.	Port Function/ Dedicated Function		Mode Function		Function 1		Function 2		Function 3		Function 4		Function 5		Function 6		Function 7		Function 8		Simplified Circuit Diagram Figure 2.1
	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	
249	P0_3	I(s)	MD_CLKS	I(s)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(3)
250	Vss																				
251	PVcc																				
252	P6_0	I(s)/O	—	—	D0	I(s)/O	LCD1_ DATA8	O	RLIN30RX	I(s)	DV0_CLK	I(s)	TIOC1A	I(s)/O	IRQ5	I(s)	RxD3	I(s)	DV0_ DATA16	I(s)	(8)
253	P6_1	I(s)/O	—	—	D1	I(s)/O	LCD1_ DATA9	O	RLIN30TX	O	IRQ4	I(s)	TIOC1B	I(s)/O	SSIDATA4	I(s)/O	TxD3	O	DV0_ DATA17	I(s)	(8)
254	P6_2	I(s)/O	—	—	D2	I(s)/O	LCD1_ DATA10	O	RLIN31RX	I(s)	IRQ7	I(s)	TCLKA	I(s)	TIOC2A	I(s)/O	RxD2	I(s)	DV0_ DATA18	I(s)	(8)
255	P6_3	I(s)/O	—	—	D3	I(s)/O	LCD1_ DATA11	O	RLIN31TX	O	IRQ2	I(s)	$\overline{\text{CTS5}}$	I(s)/O	TIOC2B	I(s)/O	TxD2	O	DV0_ DATA19	I(s)	(8)
256	P6_4	I(s)/O	—	—	D4	I(s)/O	LCD1_ DATA12	O	CAN2RX	I(s)	IRQ3	I(s)	$\overline{\text{RTS5}}$	I(s)/O	—	—	RSPCK1	I(s)/O	DV0_ DATA20	I(s)	(8)

[Legend]
(s): Schmitt
(a): Analog
(o): Open drain

Table 2.4 List of Pins (324-Pin, BGA)

Ball Number	Port Function/ Dedicated Function		Mode Function		Function 1		Function 2		Function 3		Function 4		Function 5		Function 6		Function 7		Function 8		Simplified Circuit Diagram Figure 2.1
	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	
A1	Vss																				
A2	P6_4	I(s)/O	—	—	D4	I(s)/O	LCD1_ DATA12	O	CAN2RX	I(s)	IRQ3	I(s)	$\overline{\text{RTS5}}$	I(s)/O	—	—	RSPCK1	I(s)/O	DV0_ DATA20	I(s)	(8)
A3	P0_3	I(s)	MD_ CLKS	I(s)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(3)
A4	P11_0	I(s)/O	—	—	DV0_ DATA12	I(s)	TIOC4A	I(s)/O	—	—	SCK6	I(s)/O	LCD0_ DATA7	O	VIO_D12	I(s)	—	—	—	—	(7)
A5	P9_6	I(s)/O	—	—	LCD1_ DATA22	O	SPBIO 20_0	I(s)/O	SSIWS2	I(s)/O	$\overline{\text{RTS1}}$	I(s)/O	$\overline{\text{CS5}}$	O	—	—	—	—	—	—	(7)
A6	P9_3	I(s)/O	—	—	LCD1_ DATA19	O	SPBSSL_ 0	O	—	—	TxD1	O	—	—	—	—	—	—	—	—	(7)
A7	P5_9	I(s)/O	—	—	$\overline{\text{WE2}}$/ DQMUL	O	ET_ MDC	O	DV0_ VSYNC	I(s)	IRQ2	I(s)	CAN1RX	I(s)	IERxD	I(s)	LCD1_ DATA16	O	—	—	(7)
A8	Vss																				
A9	P5_6	I(s)/O	—	—	TXOUT 0P	O	LCD1_ DATA6	O	LCD0_ DATA22	O	DV1_ DATA6	I(s)	TxD6	O	IRQ6	I(s)	SPDIF_ IN	I(s)	DV0_ DATA14	I(s)	(12), (13)
A10	P5_2	I(s)/O	—	—	TXOUT 2P	O	LCD1_ DATA2	O	LCD0_ DATA18	O	DV1_ DATA2	I(s)	SCK3	I(s)/O	TIOC1B	I(s)/O	—	—	MOSI3	I(s)/O	(12), (13)
A11	P5_0	I(s)/O	—	—	TXCLK OUTP	O	LCD1_ DATA0	O	LCD0_ DATA16	O	DV1_ DATA0	I(s)	TxD4	O	TIOC0A	I(s)/O	—	—	RSPCK3	I(s)/O	(12), (13)
A12	Vss																				
A13	VIN2B	I(a)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
A14	VDAVss																				
A15	VIN2A	I(a)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
A16	P0_2	I(s)	MD_CLK	I(s)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(3)
A17	P1_6	I(s)/O(o)	—	—	RIIC3 SCL	I(s)/O(o)	DV1_ VSYNC	I(s)	IERxD	I(s)	IRQ6	I(s)	VIO_D12	I(s)	DV0_ DATA12	I(s)	—	—	—	—	(9)
A18	P1_3	I(s)/O(o)	—	—	RIIC1 SDA	I(s)/O(o)	DV0_ DATA19	I(s)	ET_ COL	I(s)	IRQ3	I(s)	$\overline{\text{ADTRG}}$	I(s)	—	—	—	—	—	—	(9)
A19	P1_0	I(s)/O(o)	—	—	RIIC0 SCL	I(s)/O(o)	DV0_ DATA16	I(s)	TCLKA	I(s)	IRQ0	I(s)	VIO_VD	I(s)	DV0_ VSYNC	I(s)	—	—	—	—	(9)
A20	P2_13	I(s)/O	—	—	D29	I(s)/O	SSL00	I(s)/O	DV0_ DATA13	I(s)	SPBIO 11_0	I(s)/O	CAN3TX	O	SCK0	I(s)/O	LCD1_ DATA13	O	IRQ7	I(s)	(8)
A21	P2_12	I(s)/O	—	—	D28	I(s)/O	RSPCK0	I(s)/O	DV0_ DATA12	I(s)	SPBIO 01_0	I(s)/O	CAN3RX	I(s)	IRQ6	I(s)	LCD1_ DATA12	O	TIOC1B	I(s)/O	(8)
A22	Vss																				
B1	Vcc																				
B2	Vss																				
B3	P6_0	I(s)/O	—	—	D0	I(s)/O	LCD1_ DATA8	O	RLIN30 RX	I(s)	DV0_ CLK	I(s)	TIOC1A	I(s)/O	IRQ5	I(s)	RxD3	I(s)	DV0_ DATA16	I(s)	(8)
B4	P11_2	I(s)/O	—	—	DV0_ DATA14	I(s)	TIOC4C	I(s)/O	—	—	RxD6	I(s)	LCD0_ DATA5	O	VIO_D14	I(s)	—	—	—	—	(7)
B5	P9_7	I(s)/O	—	—	LCD1_ DATA23	O	SPBIO 30_0	I(s)/O	SSI DATA2	I(s)/O	TIOC1A	I(s)/O	—	—	—	—	—	—	—	—	(7)
B6	P9_4	I(s)/O	—	—	LCD1_ DATA20	O	SPBIO 00_0	I(s)/O	—	—	RxD1	I(s)	—	—	—	—	—	—	—	—	(7)
B7	P5_10	I(s)/O	—	—	$\overline{\text{WE3}}$/ DQMUU/ AH	O	—	—	DV0_ HSYNC	I(s)	—	—	CAN1TX	O	IETxD	O	LCD1_ DATA17	O	—	—	(7)
B8	P5_8	I(s)/O	—	—	LCD0_ EXTCLK	I(s)	IRQ0	I(s)	DV1_ CLK	I(s)	—	—	DV0_ CLK	I(s)	$\overline{\text{CS2}}$	O	—	—	—	—	(7)
B9	P5_7	I(s)/O	—	—	TXOUT 0M	O	LCD1_ DATA7	O	LCD0_ DATA23	O	DV1_ DATA7	I(s)	RxD6	I(s)	TIOC0D	I(s)/O	SPDIF_ OUT	O	DV0_ DATA15	I(s)	(12), (13)
B10	P5_3	I(s)/O	—	—	TXOUT 2M	O	LCD1_ DATA3	O	LCD0_ DATA19	O	DV1_ DATA3	I(s)	TxD3	O	TIOC3C	I(s)/O	—	—	MISO3	I(s)/O	(12), (13)
B11	P5_1	I(s)/O	—	—	TXCLK OUTM	O	LCD1_ DATA1	O	LCD0_ DATA17	O	DV1_ DATA1	I(s)	RxD4	I(s)	TIOC0B	I(s)/O	—	—	SSL30	I(s)/O	(12), (13)
B12	Vss																				
B13	VIN1B	I(a)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
B14	VDAVcc																				
B15	VIN1A	I(a)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
B16	P1_7	I(s)/O(o)	—	—	RIIC3 SDA	I(s)/O(o)	DV1_ HSYNC	I(s)	RLIN30 RX	I(s)	IRQ7	I(s)	VIO_D13	I(s)	DV0_ DATA13	I(s)	—	—	—	—	(9)

Ball Number	Port Function/ Dedicated Function		Mode Function		Function 1		Function 2		Function 3		Function 4		Function 5		Function 6		Function 7		Function 8		Simplified Circuit Diagram Figure 2.1
	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	
B17	P1_4	I(s)/O(o)	—	—	RIIC2 SCL	I(s)/O(o)	DV0_ CLK	I(s)	CAN1RX	I(s)	IRQ4	I(s)	—	—	—	—	CAN_ CLK	I(s)	—	—	(9)
B18	P1_2	I(s)/O(o)	—	—	RIIC1 SCL	I(s)/O(o)	DV0_ DATA18	I(s)	FRB	I(s)	IRQ2	I(s)	—	—	—	—	LCD1_ EXTCLK	I(s)	—	—	(9)
B19	P2_15	I(s)/O	—	—	D31	I(s)/O	MISO0	I(s)/O	DV0_ DATA15	I(s)	SPBIO 31_0	I(s)/O	CAN_ CLK	I(s)	RxD0	I(s)	LCD1_ DATA15	O	IRQ1	I(s)	(8)
B20	PVcc																				
B21	Vss																				
B22	P2_10	I(s)/O	—	—	D26	I(s)/O	ET_ RXD2	I(s)	DV0_ DATA10	I(s)	SSIRxD0	I(s)	RLIN30 TX	O	LCD1_ DATA10	O	VIO_D10	I(s)	MOSI4	I(s)/O	(8)
C1	P6_5	I(s)/O	—	—	D5	I(s)/O	LCD1_ DATA13	O	CAN2TX	O	—	—	SCK5	I(s)/O	—	—	SSL10	I(s)/O	DV0_ DATA21	O	(8)
C2	Vcc																				
C3	Vss																				
C4	P6_2	I(s)/O	—	—	D2	I(s)/O	LCD1_ DATA10	O	RLIN31 RX	I(s)	IRQ7	I(s)	TCLKA	I(s)	TIOC2A	I(s)/O	RxD2	I(s)	DV0_ DATA18	I(s)	(8)
C5	P11_3	I(s)/O	—	—	DV0_ DATA15	I(s)	TIOC4D	I(s)/O	—	—	—	—	LCD0_ DATA4	O	VIO_D15	I(s)	—	—	—	—	(7)
C6	P11_1	I(s)/O	—	—	DV0_ DATA13	I(s)	TIOC4B	I(s)/O	—	—	TxD6	O	LCD0_ DATA6	O	VIO_D13	I(s)	—	—	—	—	(7)
C7	P9_5	I(s)/O	—	—	LCD1_ DATA21	O	SPBIO 10_0	I(s)/O	SSISCK2	I(s)/O	$\overline{\text{CTS1}}$	I(s)/O	$\overline{\text{CS4}}$	O	—	—	—	—	—	—	(7)
C8	P9_2	I(s)/O	—	—	LCD1_ DATA18	O	SPBCLK_ 0	O	RLIN30 TX	O	SCK1	I(s)/O	A0	O	—	—	—	—	—	—	(7)
C9	Vss																				
C10	P5_5	I(s)/O	—	—	TXOUT 1M	O	LCD1_ DATA5	O	LCD0_ DATA21	O	DV1_ DATA5	I(s)	AUDIO_ XOUT	O	TIOC0C	I(s)/O	$\overline{\text{FCE}}$	O	DV0_ DATA13	I(s)	(12), (13)
C11	P5_4	I(s)/O	—	—	TXOUT 1P	O	LCD1_ DATA4	O	LCD0_ DATA20	O	DV1_ DATA4	I(s)	RxD3	I(s)	TIOC3D	I(s)/O	—	—	DV0_ DATA12	I(s)	(12), (13)
C12	LVDS APVcc																				
C13	VRM	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
C14	REXT	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
C15	Vss																				
C16	P1_5	I(s)/O(o)	—	—	RIIC2 SDA	I(s)/O(o)	DV1_ CLK	I(s)	CAN4RX	I(s)	IRQ5	I(s)	VIO_ CLK	I(s)	—	—	LCD1_ EXTCLK	I(s)	—	—	(9)
C17	P1_1	I(s)/O(o)	—	—	RIIC0 SDA	I(s)/O(o)	DV0_ DATA17	I(s)	TCLKC	I(s)	IRQ1	I(s)	VIO_HD	I(s)	DV0_ HSYNC	I(s)	—	—	—	—	(9)
C18	P2_14	I(s)/O	—	—	D30	I(s)/O	MOSI0	I(s)/O	DV0_ DATA14	I(s)	SPBIO 21_0	I(s)/O	CAN4RX	I(s)	TxD0	O	LCD1_ DATA14	O	IRQ0	I(s)	(8)
C19	PVcc																				
C20	Vss																				
C21	P2_9	I(s)/O	—	—	D25	I(s)/O	ET_ RXD1	I(s)	DV0_ DATA9	I(s)	SSIWS0	I(s)/O	RLIN30 RX	I(s)	LCD1_ DATA9	O	VIO_D9	I(s)	SSL40	I(s)/O	(8)
C22	P2_7	I(s)/O	—	—	D23	I(s)/O	ET_ TXD3	O	DV0_ DATA7	I(s)	SSITxD5	O	IETxD	O	$\overline{\text{RTS1}}$	I(s)/O	VIO_D7	I(s)	LCD0_ DATA23	O	(8)
D1	P6_7	I(s)/O	—	—	D7	I(s)/O	LCD1_ DATA15	O	—	—	LCD0_ TCON6	O	RxD5	I(s)	—	—	MISO1	I(s)/O	DV0_ DATA23	O	(8)
D2	P6_6	I(s)/O	—	—	D6	I(s)/O	LCD1_ DATA14	O	—	—	LCD0_ TCON5	O	TxD5	O	—	—	MOSI1	I(s)/O	DV0_ DATA22	O	(8)
D3	Vcc																				
D4	Vss																				
D5	P6_3	I(s)/O	—	—	D3	I(s)/O	LCD1_ DATA11	O	RLIN31 TX	O	IRQ2	I(s)	$\overline{\text{CTS5}}$	I(s)/O	TIOC2B	I(s)/O	TxD2	O	DV0_ DATA19	I(s)	(8)
D6	P6_1	I(s)/O	—	—	D1	I(s)/O	LCD1_ DATA9	O	RLIN30 TX	O	IRQ4	I(s)	TIOC1B	I(s)/O	SSI DATA4	I(s)/O	TxD3	O	DV0_ DATA17	I(s)	(8)
D7	PVcc																				
D8	PVcc																				
D9	LVDS PLLVcc																				
D10	Vss																				
D11	LVDS REFRIN	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	

Ball Number	Port Function/ Dedicated Function		Mode Function		Function 1		Function 2		Function 3		Function 4		Function 5		Function 6		Function 7		Function 8		Simplified Circuit Diagram Figure 2.1
	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	
D12	LVDS APVcc																				
D13	Vcc																				
D14	VRP	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
D15	Vss																				
D16	PVcc																				
D17	PVcc																				
D18	PVcc																				
D19	Vss																				
D20	P2_8	I(s)/O	—	—	D24	I(s)/O	ET_ RXD0	I(s)	DV0_ DATA8	I(s)	SSISCK0	I(s)/O	LCD0_ TCON6	O	LCD1_ DATA8	O	VIO_D8	I(s)	RSPCK4	I(s)/O	(8)
D21	P10_15	I(s)/O	—	—	DV0_ DATA11	I(s)	SSITxD1	O	—	—	MISO0	I(s)/O	LCD0_ DATA8	O	VIO_D11	I(s)	—	—	—	—	(7)
D22	P10_14	I(s)/O	—	—	DV0_ DATA10	I(s)	SSIRxD1	I(s)	—	—	MOSI0	I(s)/O	LCD0_ DATA9	O	VIO_D10	I(s)	—	—	—	—	(7)
E1	P6_10	I(s)/O	—	—	D10	I(s)/O	DV0_ DATA14	I(s)	—	—	LCD0_ TCON5	O	RxD0	I(s)	LCD0_ DATA2	O	—	—	IRQ2	I(s)	(8)
E2	P6_9	I(s)/O	—	—	D9	I(s)/O	DV0_ DATA13	I(s)	—	—	—	—	TxD0	O	LCD0_ DATA1	O	—	—	IRQ1	I(s)	(8)
E3	P6_8	I(s)/O	—	—	D8	I(s)/O	DV0_ DATA12	I(s)	—	—	CAN_ CLK	I(s)	SCK0	I(s)/O	LCD0_ DATA0	O	—	—	IRQ0	I(s)	(8)
E4	Vcc																				
E19	P2_11	I(s)/O	—	—	D27	I(s)/O	ET_ RXD3	I(s)	DV0_ DATA11	I(s)	SSITxD0	O	TIOC1A	I(s)/O	LCD1_ DATA11	O	VIO_D11	I(s)	MISO4	I(s)/O	(8)
E20	P2_6	I(s)/O	—	—	D22	I(s)/O	ET_ TXD2	O	DV0_ DATA6	I(s)	SSIRxD5	I(s)	—	—	RxD1	I(s)	VIO_D6	I(s)	LCD0_ DATA22	O	(8)
E21	P10_12	I(s)/O	—	—	DV0_ DATA8	I(s)	SSISCK1	I(s)/O	—	—	RSPCK0	I(s)/O	LCD0_ DATA11	O	VIO_D8	I(s)	—	—	—	—	(7)
E22	P2_5	I(s)/O	—	—	D21	I(s)/O	ET_ TXD1	O	DV0_ DATA5	I(s)	SSIWS5	I(s)/O	SPBSSL_ 1	O	TxD1	O	VIO_D5	I(s)	LCD0_ DATA21	O	(8)
F1	P6_14	I(s)/O	—	—	D14	I(s)/O	DV0_ DATA22	I(s)	—	—	TxD6	O	—	—	LCD0_ DATA6	O	—	—	IRQ6	I(s)	(8)
F2	P6_13	I(s)/O	—	—	D13	I(s)/O	DV0_ DATA21	I(s)	—	—	SCK6	I(s)/O	RxD1	I(s)	LCD0_ DATA5	O	—	—	IRQ5	I(s)	(8)
F3	P6_11	I(s)/O	—	—	D11	I(s)/O	DV0_ DATA15	I(s)	—	—	LCD0_ TCON6	O	SCK1	I(s)/O	LCD0_ DATA3	O	—	—	IRQ3	I(s)	(8)
F4	Vcc																				
F19	P2_4	I(s)/O	—	—	D20	I(s)/O	ET_ TXD0	O	DV0_ DATA4	I(s)	SSISCK5	I(s)/O	SPBCLK_ 1	O	SCK1	I(s)/O	VIO_D4	I(s)	LCD0_ DATA20	O	(8)
F20	P10_13	I(s)/O	—	—	DV0_ DATA9	I(s)	SSIWS1	I(s)/O	—	—	SSL00	I(s)/O	LCD0_ DATA10	O	VIO_D9	I(s)	—	—	—	—	(7)
F21	P2_2	I(s)/O	—	—	D18	I(s)/O	ET_ TXEN	O	DV0_ DATA2	I(s)	SPBIO 20_1	I(s)/O	MLB_ SIG	I(s)/O	TIOC2B	I(s)/O	VIO_D2	I(s)	LCD0_ DATA18	O	(8)
F22	P4_15	I(s)/O	—	—	LCD0_ DATA23	O	LCD1_ TCON2	O	SD_ D2_0	I(s)/O	MMC_ D2	I(s)/O	SPBIO 31_1	I(s)/O	SSITxD3	O	RxD2	I(s)	IRQ7	I(s)	(7)
G1	P11_13	I(s)/O	—	—	CAN1TX	O	SSL10	I(s)/O	LCD0_ TCON4	O	MMC_ D5	I(s)/O	LCD0_ TCON1	O	—	—	—	—	—	—	(7)
G2	P11_12	I(s)/O	—	—	CAN1RX	I(s)	RSPCK1	I(s)/O	IRQ3	I(s)	MMC_ D4	I(s)/O	LCD0_ TCON2	O	—	—	—	—	—	—	(7)
G3	P6_15	I(s)/O	—	—	D15	I(s)/O	DV0_ DATA23	I(s)	—	—	RxD6	I(s)	—	—	LCD0_ DATA7	O	—	—	IRQ7	I(s)	(8)
G4	P6_12	I(s)/O	—	—	D12	I(s)/O	DV0_ DATA20	I(s)	—	—	—	—	TxD1	O	LCD0_ DATA4	O	—	—	IRQ4	I(s)	(8)
G19	P4_14	I(s)/O	—	—	LCD0_ DATA22	O	LCD1_ TCON1	O	SD_ D3_0	I(s)/O	MMC_ D3	I(s)/O	SPBIO 21_1	I(s)/O	SSIRxD3	I(s)	TxD2	O	IRQ6	I(s)	(7)
G20	P2_3	I(s)/O	—	—	D19	I(s)/O	ET_ CRS	I(s)	DV0_ DATA3	I(s)	SPBIO 30_1	I(s)/O	IERxD	I(s)	$\overline{\text{CTS1}}$	I(s)/O	VIO_D3	I(s)	LCD0_ DATA19	O	(8)
G21	P4_13	I(s)/O	—	—	LCD0_ DATA21	O	LCD1_ TCON0	O	SD_ CMD_0	I(s)/O	MMC_ CMD	I(s)/O	SPBIO 11_1	I(s)/O	SSIWS3	I(s)/O	RxD1	I(s)	IRQ5	I(s)	(7)
G22	Vss																				
H1	P7_2	I(s)/O	—	—	$\overline{\text{RAS}}$	O	DV0_ DATA18	I(s)	ET_ TXER	O	RxD4	I(s)	CAN2RX	I(s)	SSIWS1	I(s)/O	TIOC0C	I(s)/O	—	—	(7)
H2	P7_1	I(s)/O	—	—	$\overline{\text{CS3}}$	O	DV0_ DATA17	I(s)	ET_ TXCLK	I(s)	TxD4	O	DV0_ CLK	I(s)	SSISCK1	I(s)/O	TIOC0B	I(s)/O	—	—	(7)
H3	P11_14	I(s)/O	—	—	SPDIF_ IN	I(s)	MOSI1	I(s)/O	LCD0_ TCON5	O	MMC_ D6	I(s)/O	LCD0_ TCON0	O	—	—	—	—	—	—	(7)

Ball Number	Port Function/ Dedicated Function		Mode Function		Function 1		Function 2		Function 3		Function 4		Function 5		Function 6		Function 7		Function 8		Simplified Circuit Diagram Figure 2.1
	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	
H4	P7_0	I(s)/O	MD_ BOOT2	I(s)	$\overline{CS0}$	O	DV0_ DATA16	I(s)	ET_ MDC	O	SCK4	I(s)/O	RLIN30 TX	O	—	—	TIOC0A	I(s)/O	—	—	(7)
H19	P4_11	I(s)/O	—	—	LCD0_ DATA19	O	LCD1_ TCON6	O	SD_ D0_0	I(s)/O	MMC_ D0	I(s)/O	SSITxD5	O	CAN4TX	O	SCK1	I(s)/O	IRQ3	I(s)	(7)
H20	P10_11	I(s)/O	—	—	DV0_ DATA7	I(s)	TIOC2B	I(s)/O	—	—	ET_ RXD3	I(s)	LCD0_ DATA12	O	VIO_D7	I(s)	—	—	—	—	(7)
H21	P10_10	I(s)/O	—	—	DV0_ DATA6	I(s)	TIOC2A	I(s)/O	—	—	ET_ RXD2	I(s)	LCD0_ DATA13	O	VIO_D6	I(s)	—	—	—	—	(7)
H22	P4_12	I(s)/O	—	—	LCD0_ DATA20	O	LCD1_ CLK	O	SD_ CLK_0	O	MMC_ CLK	O	SPBIO 01_1	I(s)/O	SSISCK3	I(s)/O	TxD1	O	IRQ4	I(s)	(7)
J1	P7_5	I(s)/O	—	—	$\overline{RD}$/$\overline{WR}$	O	DV0_ DATA21	I(s)	ET_ TXD1	O	RxD7	I(s)	—	—	SSISCK2	I(s)/O	TIOC1B	I(s)/O	—	—	(7)
J2	P7_4	I(s)/O	—	—	CKE	O	DV0_ DATA20	I(s)	ET_ TXD0	O	TxD7	O	—	—	SSITxD1	O	TIOC1A	I(s)/O	—	—	(7)
J3	P7_3	I(s)/O	—	—	$\overline{CAS}$	O	DV0_ DATA19	I(s)	ET_ TXEN	O	SCK7	I(s)/O	CAN2TX	O	SSIRxD1	I(s)	TIOC0D	I(s)/O	—	—	(7)
J4	P11_15	I(s)/O	—	—	SPDIF_ OUT	O	MISO1	I(s)/O	IRQ1	I(s)	MMC_ D7	I(s)/O	LCD0_ CLK	O	—	—	—	—	—	—	(7)
J9	Vss																				
J10	Vss																				
J11	Vss																				
J12	Vss																				
J13	Vss																				
J14	Vss																				
J19	Vcc																				
J20	P10_9	I(s)/O	—	—	DV0_ DATA5	I(s)	TIOC1B	I(s)/O	—	—	ET_ RXD1	I(s)	LCD0_ DATA14	O	VIO_D5	I(s)	—	—	—	—	(7)
J21	P10_8	I(s)/O	—	—	DV0_ DATA4	I(s)	TIOC1A	I(s)/O	—	—	ET_ RXD0	I(s)	LCD0_ DATA15	O	VIO_D4	I(s)	—	—	—	—	(7)
J22	P4_10	I(s)/O	—	—	LCD0_ DATA18	O	LCD1_ TCON5	O	SD_ D1_0	I(s)/O	MMC_ D1	I(s)/O	SSIRxD5	I(s)	—	—	RxD0	I(s)	IRQ2	I(s)	(7)
K1	P7_9	I(s)/O	—	—	A1	O	SSIWS3	I(s)/O	ET_ RXD0	I(s)	CAN0TX	O	—	—	—	—	TIOC3B	I(s)/O	IRQ0	I(s)	(7)
K2	P7_7	I(s)/O	—	—	$\overline{WE1}$/ DQMLU	O	DV0_ DATA23	I(s)	ET_ TXD3	O	$\overline{RTS7}$	I(s)/O	—	—	SSI DATA2	I(s)/O	TIOC2B	I(s)/O	—	—	(7)
K3	P7_6	I(s)/O	—	—	$\overline{WE0}$/ DQMLL	O	DV0_ DATA22	I(s)	ET_ TXD2	O	$\overline{CTS7}$	I(s)/O	—	—	SSIWS2	I(s)/O	TIOC2A	I(s)/O	—	—	(7)
K4	P7_8	I(s)/O	—	—	$\overline{RD}$	O	SSISCK3	I(s)/O	—	—	CAN0RX	I(s)	—	—	—	—	TIOC3A	I(s)/O	IRQ1	I(s)	(7)
K9	Vss																				
K10	Vss																				
K11	Vss																				
K12	Vss																				
K13	Vss																				
K14	Vss																				
K19	Vcc																				
K20	P4_8	I(s)/O	—	—	LCD0_ DATA16	O	LCD1_ TCON3	O	SD_ CD_0	I(s)	MMC_ CD	I(s)	SSISCK5	I(s)/O	CAN2TX	O	SCK0	I(s)/O	IRQ0	I(s)	(7)
K21	P4_9	I(s)/O	—	—	LCD0_ DATA17	O	LCD1_ TCON4	O	SD_ WP_0	I(s)	—	—	SSIWS5	I(s)/O	CAN2RX	I(s)	TxD0	O	IRQ1	I(s)	(7)
K22	P2_1	I(s)/O	—	—	D17	I(s)/O	ET_ TXER	O	DV0_ DATA1	I(s)	SPBIO 10_1	I(s)/O	MLB_ DAT	I(s)/O	TIOC2A	I(s)/O	VIO_D1	I(s)	LCD0_ DATA17	O	(8)
L1	P11_5	I(s)/O	—	—	DV0_ DATA17	I(s)	SD_ WP_0	I(s)	SSIWS4	I(s)/O	—	—	LCD0_ DATA2	O	—	—	—	—	—	—	(7)
L2	P7_11	I(s)/O	—	—	A3	O	SSITxD3	O	ET_ RXD2	I(s)	CAN1RX	I(s)	—	—	—	—	TIOC3D	I(s)/O	IRQ3	I(s)	(7)
L3	P7_10	I(s)/O	—	—	A2	O	SSIRxD3	I(s)	ET_ RXD1	I(s)	CAN1TX	O	—	—	—	—	TIOC3C	I(s)/O	IRQ2	I(s)	(7)
L4	P11_4	I(s)/O	—	—	DV0_ DATA16	I(s)	SD_ CD_0	I(s)	SSISCK4	I(s)/O	MMC_ CD	I(s)	LCD0_ DATA3	O	—	—	—	—	—	—	(7)
L9	Vss																				
L10	Vss																				
L11	Vss																				

Ball Number	Port Function/ Dedicated Function		Mode Function		Function 1		Function 2		Function 3		Function 4		Function 5		Function 6		Function 7		Function 8		Simplified Circuit Diagram Figure 2.1
	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	
L12	Vss																				
L13	Vss																				
L14	Vss																				
L19	PVcc																				
L20	P4_7	I(s)/O	—	—	LCD0_ DATA15	O	MISO1	I(s)/O	TIOC4D	I(s)/O	PWM2H	O	SSITxD0	O	—	—	DV0_ DATA15	I(s)	—	—	(7)
L21	P2_0	I(s)/O	—	—	D16	I(s)/O	ET_ TXCLK	I(s)	DV0_ DATA0	I(s)	SPBIO 00_1	I(s)/O	MLB_ CLK	I(s)	IRQ5	I(s)	VIO_D0	I(s)	LCD0_ DATA16	O	(8)
L22	P4_6	I(s)/O	—	—	LCD0_ DATA14	O	MOSI1	I(s)/O	TIOC4C	I(s)/O	PWM2G	O	SSIRxD0	I(s)	—	—	DV0_ DATA14	I(s)	—	—	(7)
M1	P7_12	I(s)/O	—	—	A4	O	SSISCK4	I(s)/O	ET_ RXD3	I(s)	—	—	—	—	—	—	TIOC4A	I(s)/O	IRQ4	I(s)	(7)
M2	P11_6	I(s)/O	—	—	DV0_ DATA18	I(s)	SD_ D1_0	I(s)/O	SSI DATA4	I(s)/O	MMC_ D1	I(s)/O	LCD0_ DATA1	O	—	—	—	—	—	—	(7)
M3	P11_7	I(s)/O	—	—	DV0_ DATA19	I(s)	SD_ D0_0	I(s)/O	$\overline{\text{CTS5}}$	I(s)/O	MMC_ D0	I(s)/O	LCD0_ DATA0	O	—	—	—	—	—	—	(7)
M4	Vcc																				
M9	Vss																				
M10	Vss																				
M11	Vss																				
M12	Vss																				
M13	Vss																				
M14	Vss																				
M19	PVcc																				
M20	P4_5	I(s)/O	—	—	LCD0_ DATA13	O	SSL10	I(s)/O	TIOC4B	I(s)/O	PWM2F	O	SSIWS 0	I(s)/O	—	—	DV0_ DATA13	I(s)	—	—	(7)
M21	P4_4	I(s)/O	—	—	LCD0_ DATA12	O	RSPCK1	I(s)/O	TIOC4A	I(s)/O	PWM2E	O	SSISCK0	I(s)/O	—	—	DV0_ DATA12	I(s)	—	—	(7)
M22	P10_7	I(s)/O	—	—	DV0_ DATA3	I(s)	TIOC0D	I(s)/O	PWM2H	O	ET_ TXD3	O	LCD0_ DATA16	O	VIO_D3	I(s)	—	—	—	—	(7)
N1	P7_13	I(s)/O	—	—	A5	O	SSIWS4	I(s)/O	ET_ MDIO	I(s)/O	—	—	—	—	—	—	TIOC4B	I(s)/O	IRQ5	I(s)	(7)
N2	P7_14	I(s)/O	—	—	A6	O	SSI DATA4	I(s)/O	ET_ CRS	I(s)	—	—	—	—	—	—	TIOC4C	I(s)/O	IRQ6	I(s)	(7)
N3	P7_15	I(s)/O	—	—	A7	O	RSPCK0	I(s)/O	ET_ RXCLK	I(s)	$\overline{\text{CTS5}}$	I(s)/O	SCI_ TXD0	O	—	—	TIOC4D	I(s)/O	—	—	(7)
N4	PVcc																				
N9	Vss																				
N10	Vss																				
N11	Vss																				
N12	Vss																				
N13	Vss																				
N14	Vss																				
N19	P10_4	I(s)/O	—	—	DV0_ DATA0	I(s)	TIOC0A	I(s)/O	PWM2E	O	ET_ TXD0	O	LCD0_ DATA19	O	VIO_D0	I(s)	—	—	—	—	(7)
N20	P10_5	I(s)/O	—	—	DV0_ DATA1	I(s)	TIOC0B	I(s)/O	PWM2F	O	ET_ TXD1	O	LCD0_ DATA18	O	VIO_D1	I(s)	—	—	—	—	(7)
N21	P10_6	I(s)/O	—	—	DV0_ DATA2	I(s)	TIOC0C	I(s)/O	PWM2G	O	ET_ TXD2	O	LCD0_ DATA17	O	VIO_D2	I(s)	—	—	—	—	(7)
N22	P4_3	I(s)/O	—	—	LCD0_ DATA11	O	TIOC0D	I(s)/O	$\overline{\text{FWE}}$	O	CAN3TX	O	RxD2	I(s)	—	—	MISO4	I(s)/O	MMC_ D7	I(s)/O	(7)
P1	P8_0	I(s)/O	—	—	A8	O	SSL00	I(s)/O	ET_ RXER	I(s)	SCK5	I(s)/O	SCI_ SCK0	I(s)/O	—	—	—	—	—	—	(7)
P2	P8_1	I(s)/O	—	—	A9	O	MOSI0	I(s)/O	ET_ RXDV	I(s)	TxD5	O	SCI_ RXD0	I(s)	—	—	—	—	—	—	(7)
P3	P8_2	I(s)/O	—	—	A10	O	MISO0	I(s)/O	AVB_ GPTP_ EXTERN	I(s)	RxD5	I(s)	IRQ0	I(s)	—	—	—	—	—	—	(7)
P4	PVcc																				
P9	Vss																				
P10	Vss																				

Ball Number	Port Function/ Dedicated Function		Mode Function		Function 1		Function 2		Function 3		Function 4		Function 5		Function 6		Function 7		Function 8		Simplified Circuit Diagram Figure 2.1
	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	
P11	Vss																				
P12	Vss																				
P13	Vss																				
P14	Vss																				
P19	Vss																				
P20	P4_0	I(s)/O	—	—	LCD0_ DATA8	O	TIOC0A	I(s)/O	$\overline{FRE}$	O	—	—	—	—	—	—	RSPCK4	I(s)/O	MMC_ D4	I(s)/O	(7)
P21	P4_2	I(s)/O	—	—	LCD0_ DATA10	O	TIOC0C	I(s)/O	FALE	O	CAN3RX	I(s)	TxD2	O	—	—	MOSI4	I(s)/O	MMC_ D6	I(s)/O	(7)
P22	P4_1	I(s)/O	—	—	LCD0_ DATA9	O	TIOC0B	I(s)/O	FCLE	O	—	—	SCK2	I(s)/O	—	—	SSL40	I(s)/O	MMC_ D5	I(s)/O	(7)
R1	P8_3	I(s)/O	—	—	A11	O	DV1_ DATA0	I(s)	RSPCK2	I(s)/O	$\overline{RTS5}$	I(s)/O	—	—	IRQ1	I(s)	SCK2	I(s)/O	—	—	(7)
R2	P8_4	I(s)/O	—	—	A12	O	DV1_ DATA1	I(s)	SSL20	I(s)/O	—	—	—	—	IERxD	I(s)	RxD2	I(s)	—	—	(7)
R3	P8_5	I(s)/O	—	—	A13	O	DV1_ DATA2	I(s)	MOSI2	I(s)/O	—	—	—	—	—	—	—	—	—	—	(7)
R4	Vcc																				
R19	Vcc																				
R20	P3_15	I(s)/O	—	—	LCD0_ DATA7	O	—	—	NAF7	I(s)/O	—	—	TRACE CTL	O	—	—	SD_ D2_1	I(s)/O	MMC_ D2	I(s)/O	(7)
R21	P3_14	I(s)/O	—	—	LCD0_ DATA6	O	—	—	NAF6	I(s)/O	—	—	TRACE CLK	O	—	—	SD_ D3_1	I(s)/O	MMC_ D3	I(s)/O	(7)
R22	P3_13	I(s)/O	—	—	LCD0_ DATA5	O	—	—	NAF5	I(s)/O	AUDIO_ XOUT	O	—	—	—	—	SD_ CMD_1	I(s)/O	MMC_ CMD	I(s)/O	(7)
T1	P11_8	I(s)/O	—	—	DV0_ DATA20	I(s)	SD_ CLK_0	O	$\overline{RTS5}$	I(s)/O	MMC_ CLK	O	LCD0_ TCON6	O	—	—	—	—	—	—	(7)
T2	P11_9	I(s)/O	—	—	DV0_ DATA21	I(s)	SD_ CMD_0	I(s)/O	SCK5	I(s)/O	MMC_ CMD	I(s)/O	LCD0_ TCON5	O	—	—	—	—	—	—	(7)
T3	P11_10	I(s)/O	—	—	DV0_ DATA22	I(s)	SD_ D3_0	I(s)/O	TxD5	O	MMC_ D3	I(s)/O	LCD0_ TCON4	O	—	—	—	—	—	—	(7)
T4	Vcc																				
T19	Vcc																				
T20	P3_10	I(s)/O	—	—	LCD0_ DATA2	O	—	—	NAF2	I(s)/O	—	—	TRACE DATA2	O	TIOC4C	I(s)/O	SD_ D1_1	I(s)/O	MMC_ D1	I(s)/O	(7)
T21	P3_11	I(s)/O	—	—	LCD0_ DATA3	O	—	—	NAF3	I(s)/O	—	—	TRACE DATA3	O	TIOC4D	I(s)/O	SD_ D0_1	I(s)/O	MMC_ D0	I(s)/O	(7)
T22	P3_12	I(s)/O	—	—	LCD0_ DATA4	O	—	—	NAF4	I(s)/O	—	—	—	—	—	—	SD_ CLK_1	O	MMC_ CLK	O	(7)
U1	Vss																				
U2	P8_6	I(s)/O	—	—	A14	O	DV1_ DATA3	I(s)	MISO2	I(s)/O	—	—	—	—	IETxD	O	TxD2	O	—	—	(7)
U3	P11_11	I(s)/O	—	—	DV0_ DATA23	I(s)	SD_ D2_0	I(s)/O	RxD5	I(s)	MMC_ D2	I(s)/O	LCD0_ TCON3	O	—	—	—	—	—	—	(7)
U4	P8_7	I(s)/O	—	—	A15	O	DV1_ DATA4	I(s)	AUDIO_ XOUT	O	IRQ5	I(s)	ET_ COL	I(s)	—	—	—	—	—	—	(7)
U19	Vcc																				
U20	JP0_1	I	—	—	TDO	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(6)
U21	TCK	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(2)
U22	Vss																				
V1	CKIO	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(5)
V2	P8_8	I(s)/O	—	—	A16	O	DV1_ DATA5	I(s)	SPBIO 00_1	I(s)/O	SPDIF_ IN	I(s)	TIOC1A	I(s)/O	PWM1A	O	TxD3	O	SSISCK5	I(s)/O	(7)
V3	P8_9	I(s)/O	—	—	A17	O	DV1_ DATA6	I(s)	SPBIO 10_1	I(s)/O	SPDIF_ OUT	O	TIOC1B	I(s)/O	PWM1B	O	RxD3	I(s)	SSIWS5	I(s)/O	(7)
V4	P8_13	I(s)/O	—	—	A21	O	—	—	SPBSSL_ 1	O	TIOC3D	I(s)/O	TxD5	O	PWM1F	O	SGOUT_3	O	SSIWS4	I(s)/O	(7)
V19	P3_8	I(s)/O	—	—	LCD0_ DATA0	O	—	—	NAF0	I(s)/O	—	—	TRACE DATA0	O	TIOC4A	I(s)/O	SD_ CD_1	I(s)	MMC_ CD	I(s)	(7)
V20	$\overline{TRST}$	I(s)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(3)
V21	JP0_0	I	—	—	TDI	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(2)
V22	TMS	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(6)

Ball Number	Port Function/ Dedicated Function		Mode Function		Function 1		Function 2		Function 3		Function 4		Function 5		Function 6		Function 7		Function 8		Simplified Circuit Diagram Figure 2.1
	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	
W1	Vss																				
W2	P8_10	I(s)/O	—	—	A18	O	DV1_ DATA7	I(s)	SPBIO 20_1	I(s)/O	TIOC3A	I(s)/O	CAN4TX	O	PWM1C	O	SGOUT_0	O	SSITxD5	O	(7)
W3	P8_11	I(s)/O	—	—	A19	O	—	—	SPBIO 30_1	I(s)/O	TIOC3B	I(s)/O	RxD5	I(s)	PWM1D	O	SGOUT_1	O	DV0_ CLK	I(s)	(7)
W4	PVcc																				
W5	PVcc																				
W6	PVcc																				
W7	Vss																				
W8	Vss																				
W9	Vcc																				
W10	Vcc																				
W11	Vss																				
W12	PVcc																				
W13	PVcc																				
W14	PLLVcc																				
W15	Vss																				
W16	Vss																				
W17	AVss																				
W18	AVcc																				
W19	PVcc																				
W20	P3_9	I(s)/O	—	—	LCD0_ DATA1	O	—	—	NAF1	I(s)/O	—	—	TRACE DATA1	O	TIOC4B	I(s)/O	SD_ WP_1	I(s)	IRQ6	I(s)	(7)
W21	AUDIO_X 2	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(10)
W22	AUDIO_X 1	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(10)
Y1	P8_12	I(s)/O	—	—	A20	O	—	—	SPBCLK_ 1	O	TIOC3C	I(s)/O	SCK5	I(s)/O	PWM1E	O	SGOUT_2	O	SSISCK4	I(s)/O	(7)
Y2	P8_14	I(s)/O	—	—	A22	O	SPBIO 01_0	I(s)/O	SPBIO 00_1	I(s)/O	TIOC2A	I(s)/O	RSPCK2	I(s)/O	PWM1G	O	TxD4	O	SSI DATA4	I(s)/O	(7)
Y3	PVcc																				
Y4	P3_7	I(s)/O	—	—	LCD0_ TCON6	O	—	—	SSITxD1	O	LCD1_ EXTCLK	I(s)	SCI_ $\overline{\text{CTS0}}$/ $\overline{\text{RTS0}}$	I(s)/O	TIOC3D	I(s)/O	$\overline{\text{CS1}}$	O	$\overline{\text{WDT}}$ OVF	O	(7)
Y5	P3_4	I(s)/O	—	—	LCD0_ TCON3	O	ET_ RXCLK	I(s)	SSISCK1	I(s)/O	AUDIO_ XOUT2	O	SCI_ SCK0	I(s)/O	TIOC3A	I(s)/O	SCK3	I(s)/O	—	—	(7)
Y6	P10_2	I(s)/O	—	—	DV0_ HSYNC	I(s)	TCLKC	I(s)	PWM2C	O	ET_ TXEN	O	LCD0_ DATA21	O	VIO_HD	I(s)	—	—	—	—	(7)
Y7	P3_2	I(s)/O	—	—	LCD0_ TCON1	O	ET_ TXEN	O	—	—	RxD2	I(s)	SCI_ RXD1	I(s)	TEND0	O	PWM2C	O	MOSI3	I(s)/O	(7)
Y8	$\overline{\text{RES}}$	I(s)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(1)
Y9	NMI	I(s)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(3)
Y10	Vss																				
Y11	VBUS1	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	#N/A
Y12	VBUS0	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	#N/A
Y13	USB AVcc																				
Y14	Vss																				
Y15	P0_0	I(s)	MD_ BOOT0	I(s)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(3)
Y16	P0_1	I(s)	MD_ BOOT1	I(s)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(3)
Y17	P1_10	I(s)	—	—	AN2	I(a)	—	—	IRQ4	I(s)	TCLKB	I(s)	—	—	—	—	—	—	—	—	(4)
Y18	P1_13	I(s)	—	—	AN5	I(a)	DV0_ HSYNC	I(s)	—	—	$\overline{\text{WAIT}}$	I(s)	—	—	—	—	—	—	—	—	(4)
Y19	P1_15	I(s)	—	—	AN7	I(a)	—	—	—	—	AVB_CAP TURE	I(s)	—	—	—	—	—	—	—	—	(4)
Y20	PVcc																				

Ball Number	Port Function/ Dedicated Function		Mode Function		Function 1		Function 2		Function 3		Function 4		Function 5		Function 6		Function 7		Function 8		Simplified Circuit Diagram Figure 2.1
	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	
Y21	VIDEO_X2	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(10)
Y22	VIDEO_X1	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(10)
AA1	P8_15	I(s)/O	—	—	A23	O	SPBIO11_0	I(s)/O	SPBIO10_1	I(s)/O	TIOC2B	I(s)/O	SSL20	I(s)/O	PWM1H	O	RxD4	I(s)	—	—	(7)
AA2	PVcc																				
AA3	P9_1	I(s)/O	—	—	A25	O	SPBIO31_0	I(s)/O	CAN0RX	I(s)	IRQ0	I(s)	MISO2	I(s)/O	—	—	—	—	—	—	(7)
AA4	P3_5	I(s)/O	—	—	LCD0_TCON4	O	ET_RXER	I(s)	SSIWS1	I(s)/O	AUDIO_XOUT3	O	SCI_TXD0	O	TIOC3B	I(s)/O	TxD3	O	—	—	(7)
AA5	P10_1	I(s)/O	—	—	DV0_VSYNC	I(s)	TCLKB	I(s)	PWM2B	O	ET_TXER	O	LCD0_DATA22	O	VIO_VD	I(s)	—	—	—	—	(7)
AA6	P3_3	I(s)/O	—	—	LCD0_TCON2	O	ET_MDIO	I(s)/O	IRQ4	I(s)	$\overline{BS}$	O	$\overline{SCI\_CTS1/RTS1}$	I(s)/O	DACK0	O	PWM2D	O	MISO3	I(s)/O	(7)
AA7	P3_1	I(s)/O	—	—	LCD0_TCON0	O	ET_TXER	O	IRQ6	I(s)	TxD2	O	SCI_TXD1	O	AUDIO_CLK	I(s)	PWM2B	O	SSL30	I(s)/O	(7)
AA8	RTC_X2	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(11)
AA9	P0_5	I(s)	—	—	RTC_X4	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(3), (10)
AA10	Vss																				
AA11	DM1	I/O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
AA12	DP0	I/O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
AA13	REFRIN	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
AA14	Vss																				
AA15	USB_X2	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(10)
AA16	XTAL	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(10)
AA17	P1_8	I(s)	—	—	AN0	I(a)	—	—	IRQ2	I(s)	DREQ0	I(s)	VIO_D14	I(s)	DV0_DATA14	I(s)	—	—	—	—	(4)
AA18	P1_11	I(s)	—	—	AN3	I(a)	—	—	IRQ5	I(s)	TCLKD	I(s)	—	—	—	—	—	—	—	—	(4)
AA19	P1_14	I(s)	—	—	AN6	I(a)	—	—	—	—	ET_COL	I(s)	—	—	—	—	—	—	—	—	(4)
AA20	AVcc																				
AA21	PVcc																				
AA22	BSCANP	I(s)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(1)
AB1	PVcc																				
AB2	P9_0	I(s)/O	—	—	A24	O	SPBIO21_0	I(s)/O	CAN0TX	O	TCLKC	I(s)	MOSI2	I(s)/O	—	—	—	—	—	—	(7)
AB3	P3_6	I(s)/O	—	—	LCD0_TCON5	O	ET_RXDV	I(s)	SSIRxD1	I(s)	—	—	SCI_RXD0	I(s)	TIOC3C	I(s)/O	RxD3	I(s)	—	—	(7)
AB4	P10_0	I(s)/O	—	—	DV0_CLK	I(s)	TCLKA	I(s)	PWM2A	O	ET_TXCLK	I(s)	LCD0_DATA23	O	VIO_CLK	I(s)	—	—	—	—	(7)
AB5	P10_3	I(s)/O	—	—	—	—	TCLKD	I(s)	PWM2D	O	ET_CRS	I(s)	LCD0_DATA20	O	VIO_FLD	I(s)	—	—	—	—	(7)
AB6	P3_0	I(s)/O	—	—	LCD0_CLK	O	ET_TXCLK	I(s)	IRQ2	I(s)	SCK2	I(s)/O	SCI_SCK1	I(s)/O	TxD2	O	PWM2A	O	RSPCK3	I(s)/O	(7)
AB7	Vss																				
AB8	RTC_X1	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(11)
AB9	P0_4	I(s)	—	—	RTC_X3	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(3), (10)
AB10	Vss																				
AB11	DP1	I/O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	#N/A
AB12	DM0	I/O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	#N/A
AB13	Vss																				
AB14	USB APVcc																				
AB15	USB_X1	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(10)
AB16	EXTAL	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(10)
AB17	Vss																				

Ball Number	Port Function/ Dedicated Function		Mode Function		Function 1		Function 2		Function 3		Function 4		Function 5		Function 6		Function 7		Function 8		Simplified Circuit Diagram Figure 2.1
	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	
AB18	P1_9	I(s)	—	—	AN1	I(a)	—	—	IRQ3	I(s)	—	—	VIO_ D15	I(s)	DV0_ DATA15	I(s)	—	—	—	—	(4)
AB19	P1_12	I(s)	—	—	AN4	I(a)	DV0_ VSYNC	I(s)	—	—	VIO_ FLD	I(s)	—	—	—	—	—	—	—	—	(4)
AB20	AVss																				
AB21	AVref																				
AB22	Vss																				

[Legend]
(s): Schmitt
(a): Analog
(o): Open drain

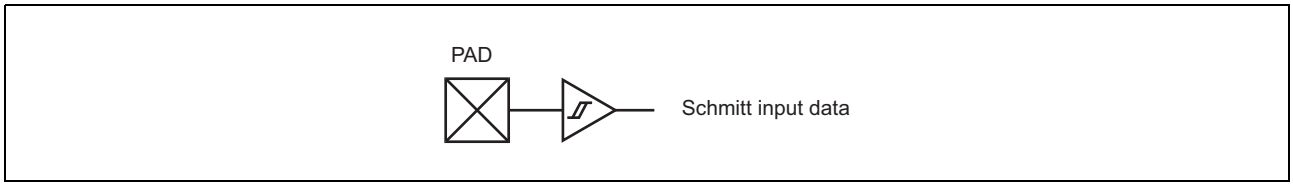


Figure 2.1 (1) Simplified Circuit Diagram (Schmitt Input Buffer)

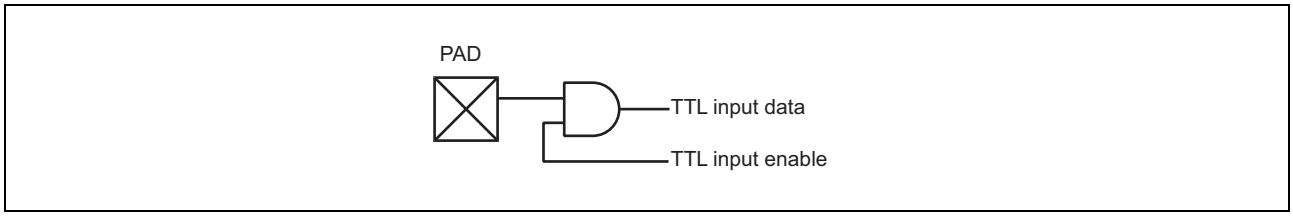


Figure 2.1 (2) Simplified Circuit Diagram (TTL AND Input Buffer)

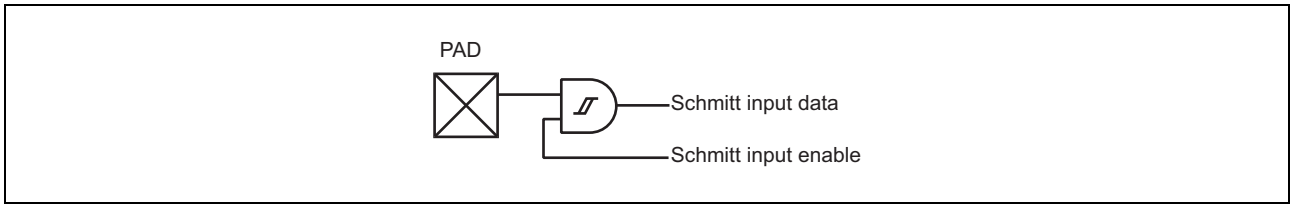


Figure 2.1 (3) Simplified Circuit Diagram (Schmitt AND Input Buffer)

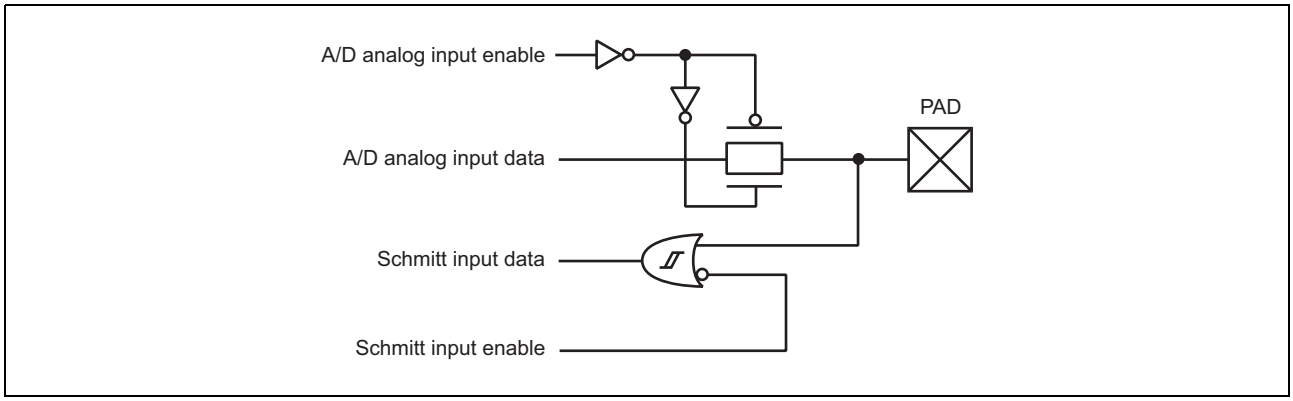


Figure 2.1 (4) Simplified Circuit Diagram (Schmitt OR Input and A/D Input Buffer)

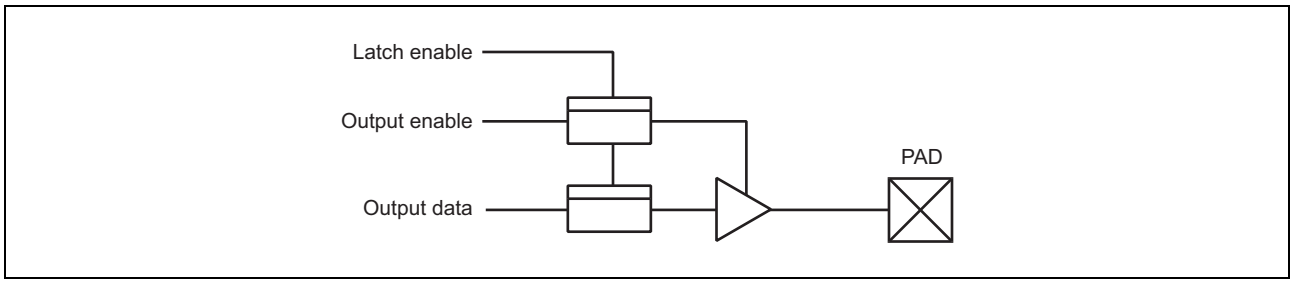


Figure 2.1 (5) Simplified Circuit Diagram (Output Buffer with Enable, with Latch)

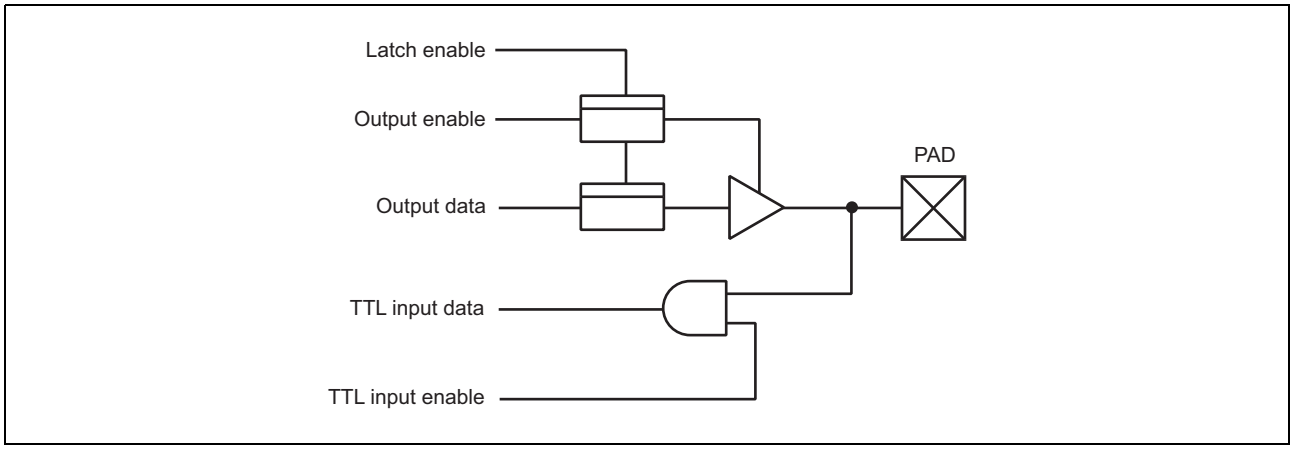


Figure 2.1 (6) Simplified Circuit Diagram (Bidirectional Buffer, TTL AND Input, with Latch)

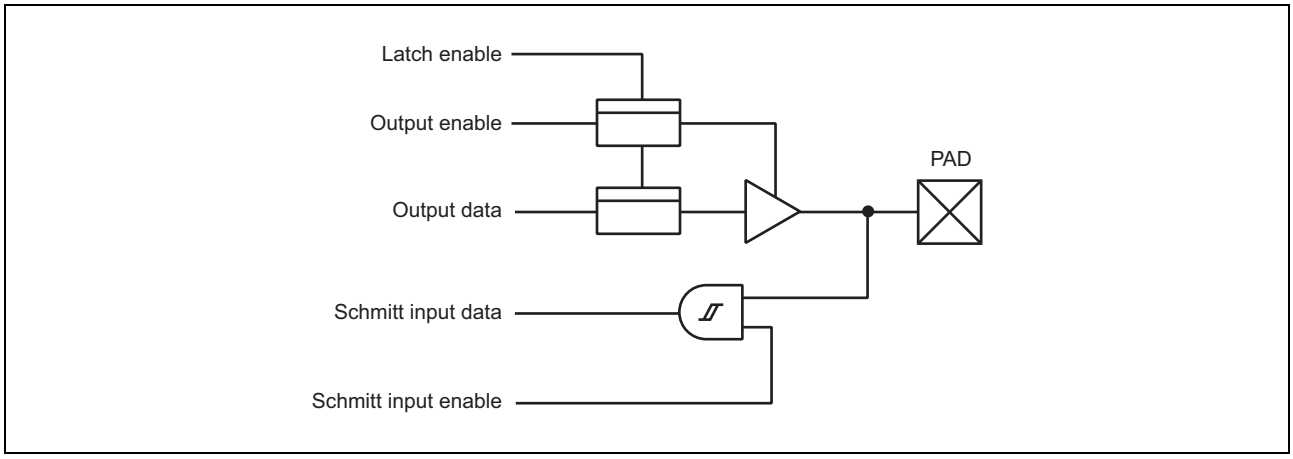


Figure 2.1 (7) Simplified Circuit Diagram (Bidirectional Buffer, Schmitt AND Input, with Latch)

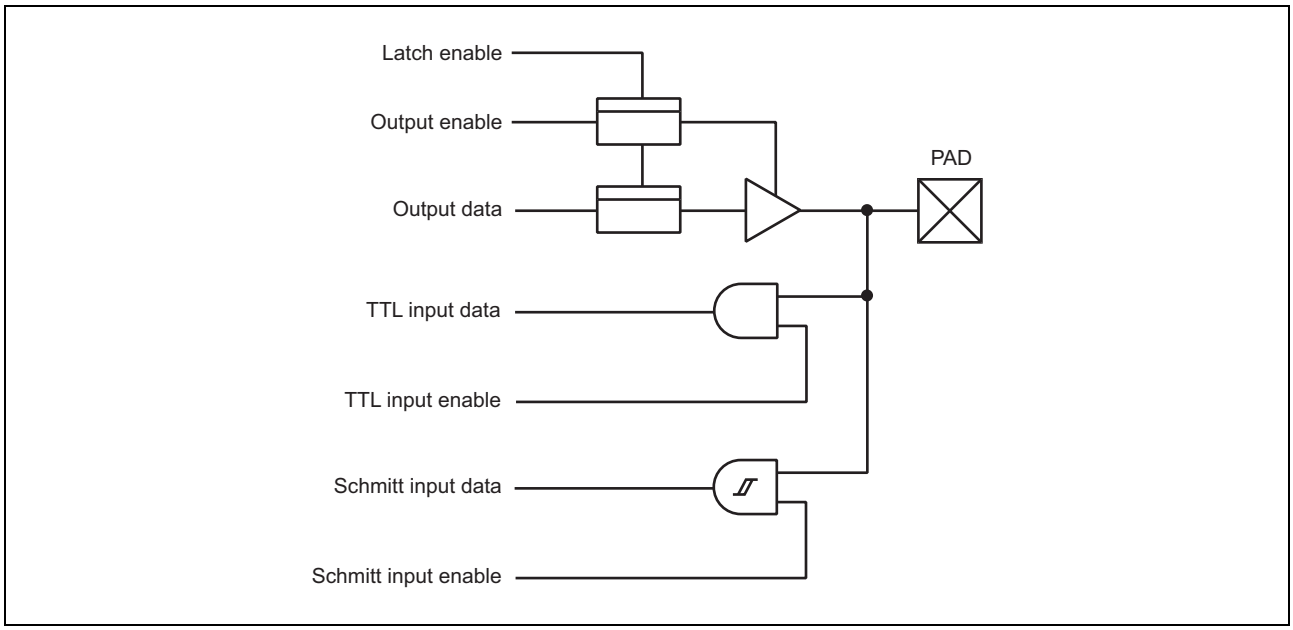


Figure 2.1 (8) Simplified Circuit Diagram (Bidirectional Buffer, TTL AND Input, Schmitt AND Input, with Latch)

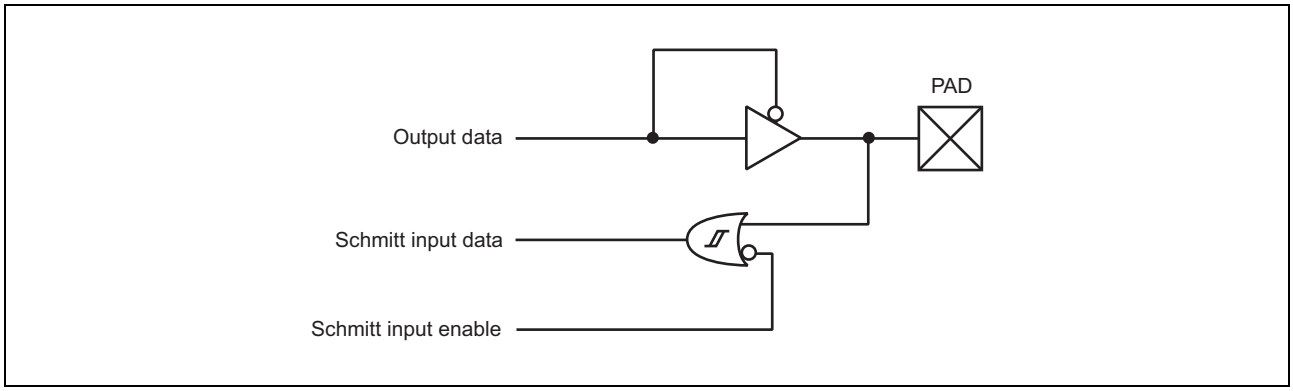


Figure 2.1 (9) Simplified Circuit Diagram (Open Drain Output and Schmitt OR Input Buffer)

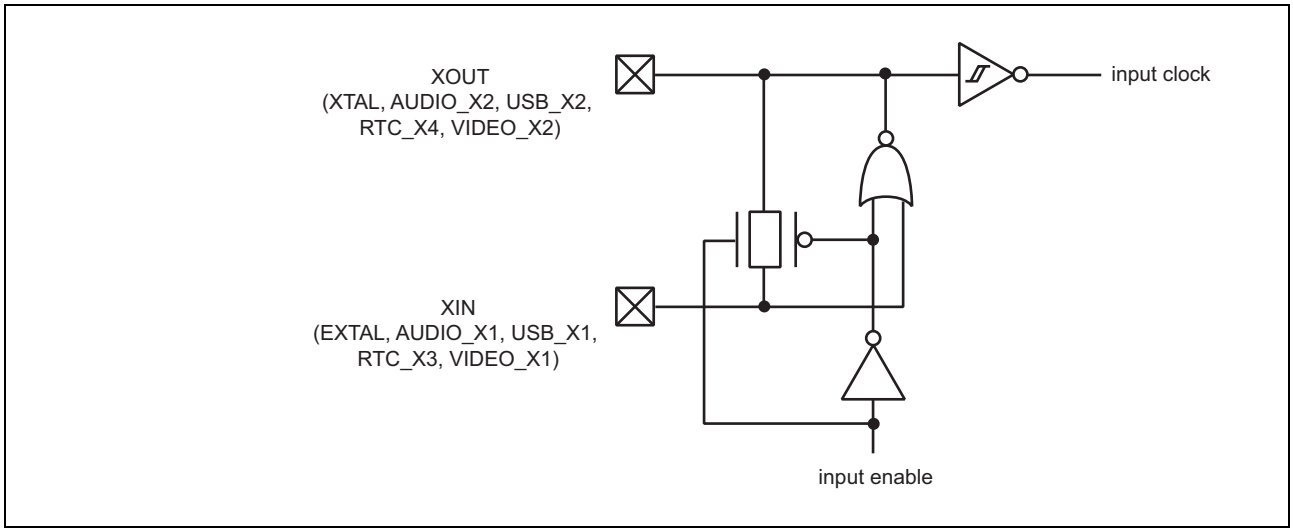


Figure 2.1 (10) Simplified Circuit Diagram (Oscillation Buffer 1)

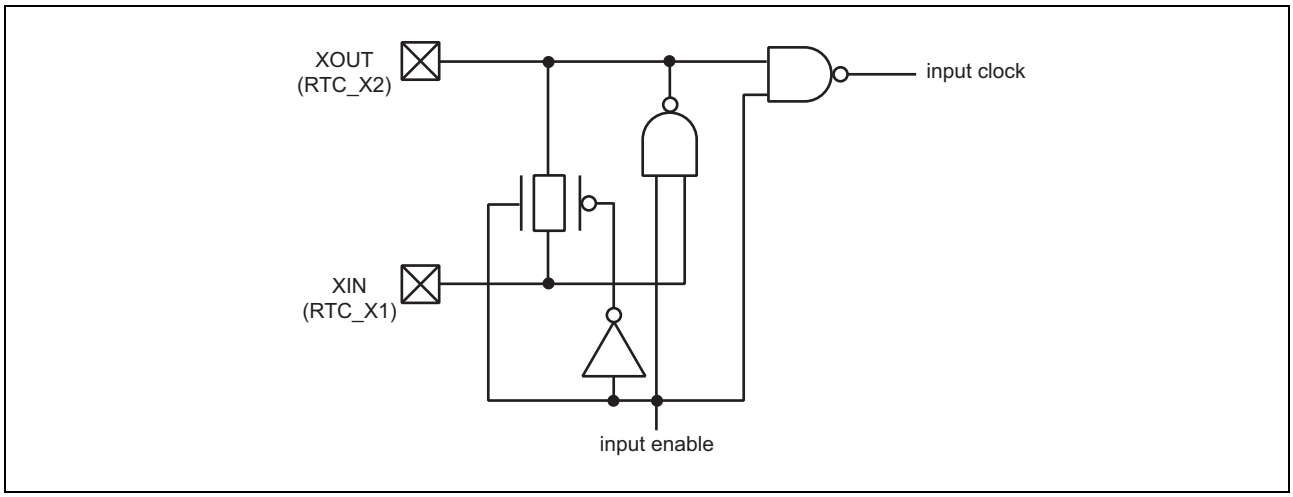


Figure 2.1 (11) Simplified Circuit Diagram (Oscillation Buffer 2)

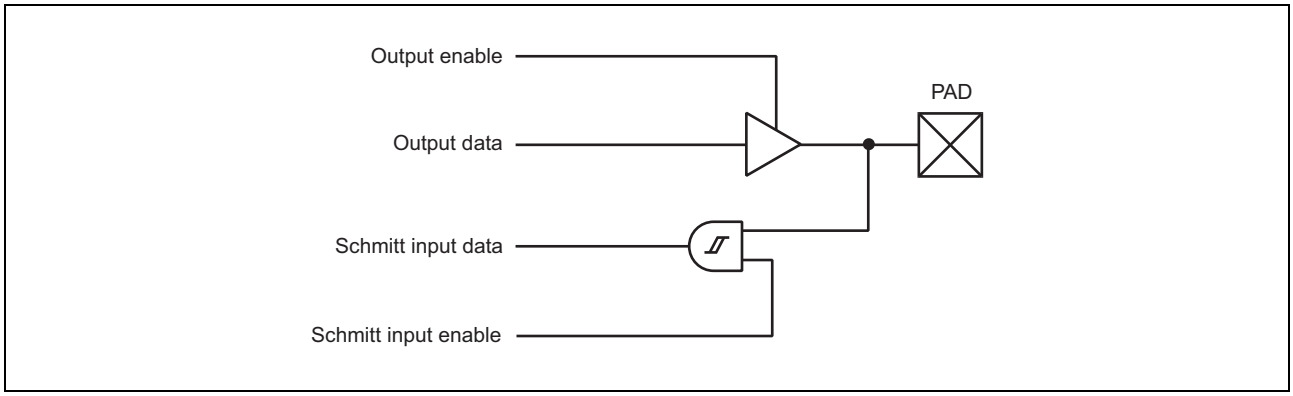


Figure 2.1 (12) Simplified Circuit Diagram (Bidirectional Buffer, Schmitt AND Input Buffer, No Latch)

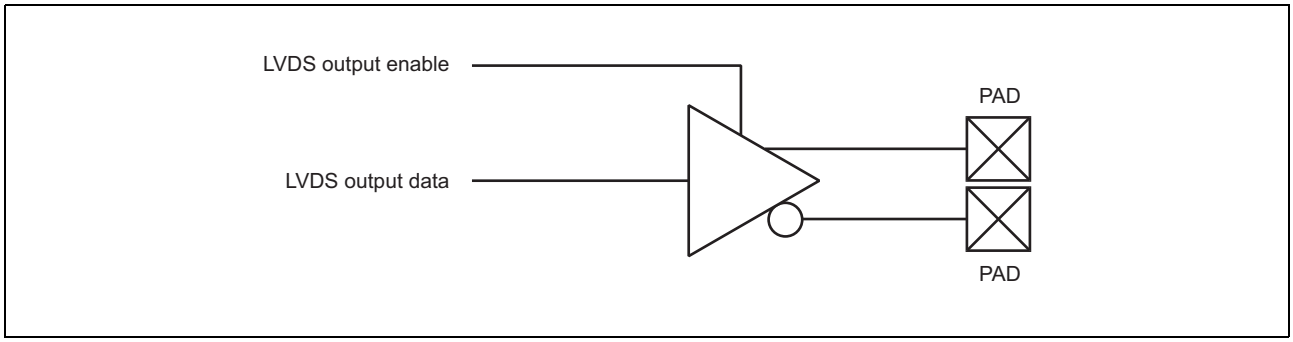
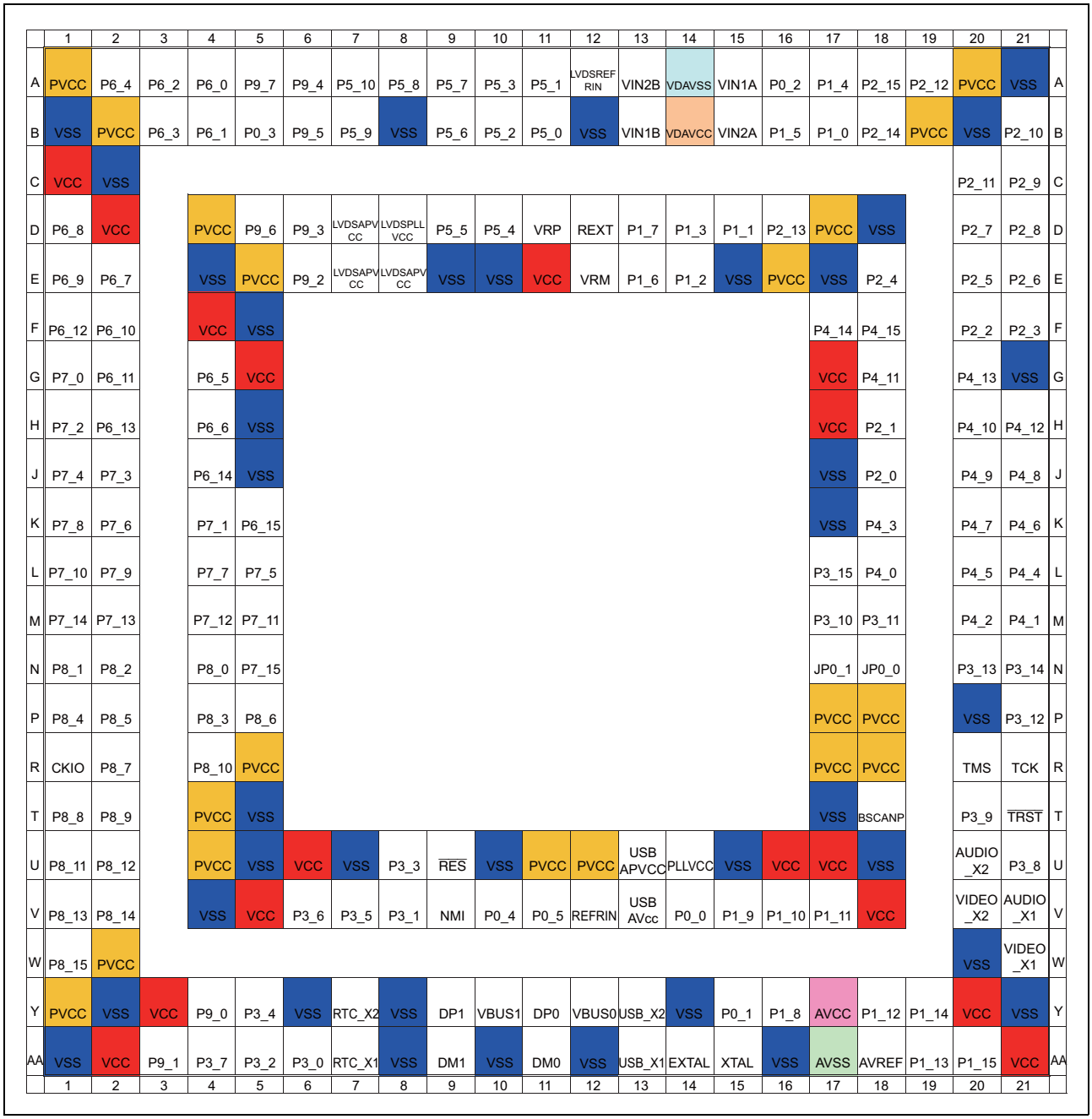


Figure 2.1 (13) Simplified Circuit Diagram (LVDS Output Buffer)

2.2 Pin Assignment



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	
A	PVCC	P6_4	P6_2	P6_0	P9_7	P9_4	P5_10	P5_8	P5_7	P5_3	P5_1	LVDSREF RIN	VIN2B	VDAVSS	VIN1A	P0_2	P1_4	P2_15	P2_12	PVCC	VSS	A
B	VSS	PVCC	P6_3	P6_1	P0_3	P9_5	P5_9	VSS	P5_6	P5_2	P5_0	VSS	VIN1B	VDAVCC	VIN2A	P1_5	P1_0	P2_14	PVCC	VSS	P2_10	B
C	VCC	VSS																		P2_11	P2_9	C
D	P6_8	VCC		PVCC	P9_6	P9_3	LVDSAPV CC	LVDSPLL VCC	P5_5	P5_4	VRP	REXT	P1_7	P1_3	P1_1	P2_13	PVCC	VSS		P2_7	P2_8	D
E	P6_9	P6_7		VSS	PVCC	P9_2	LVDSAPV CC	LVDSAPV CC	VSS	VSS	VCC	VRM	P1_6	P1_2	VSS	PVCC	VSS	P2_4		P2_5	P2_6	E
F	P6_12	P6_10		VCC	VSS												P4_14	P4_15		P2_2	P2_3	F
G	P7_0	P6_11		P6_5	VCC												VCC	P4_11		P4_13	VSS	G
H	P7_2	P6_13		P6_6	VSS												VCC	P2_1		P4_10	P4_12	H
J	P7_4	P7_3		P6_14	VSS												VSS	P2_0		P4_9	P4_8	J
K	P7_8	P7_6		P7_1	P6_15												VSS	P4_3		P4_7	P4_6	K
L	P7_10	P7_9		P7_7	P7_5												P3_15	P4_0		P4_5	P4_4	L
M	P7_14	P7_13		P7_12	P7_11												P3_10	P3_11		P4_2	P4_1	M
N	P8_1	P8_2		P8_0	P7_15												JP0_1	JP0_0		P3_13	P3_14	N
P	P8_4	P8_5		P8_3	P8_6												PVCC	PVCC		VSS	P3_12	P
R	CKIO	P8_7		P8_10	PVCC												PVCC	PVCC		TMS	TCK	R
T	P8_8	P8_9		PVCC	VSS												VSS	BSCANP		P3_9	$\overline{\text{TRST}}$	T
U	P8_11	P8_12		PVCC	VSS	VCC	VSS	P3_3	$\overline{\text{RES}}$	VSS	PVCC	PVCC	USB APVCC	PLLVCC	VSS	VCC	VCC	VSS		AUDIO _X2	P3_8	U
V	P8_13	P8_14		VSS	VCC	P3_6	P3_5	P3_1	NMI	P0_4	P0_5	REFRIN	USB AVcc	P0_0	P1_9	P1_10	P1_11	VCC		VIDEO _X2	AUDIO _X1	V
W	P8_15	PVCC																		VSS	VIDEO _X1	W
Y	PVCC	VSS	VCC	P9_0	P3_4	VSS	RTC_X2	VSS	DP1	VBUS1	DP0	VBUS0	USB_X2	VSS	P0_1	P1_8	AVCC	P1_12	P1_14	VCC	VSS	Y
AA	VSS	VCC	P9_1	P3_7	P3_2	P3_0	RTC_X1	VSS	DM1	VSS	DM0	VSS	USB_X1	EXTAL	XTAL	VSS	AVSS	AVREF	P1_13	P1_15	VCC	AA
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	

Figure 2.2 Pin Assignment of the 256-Pin BGA (Top Perspective View)

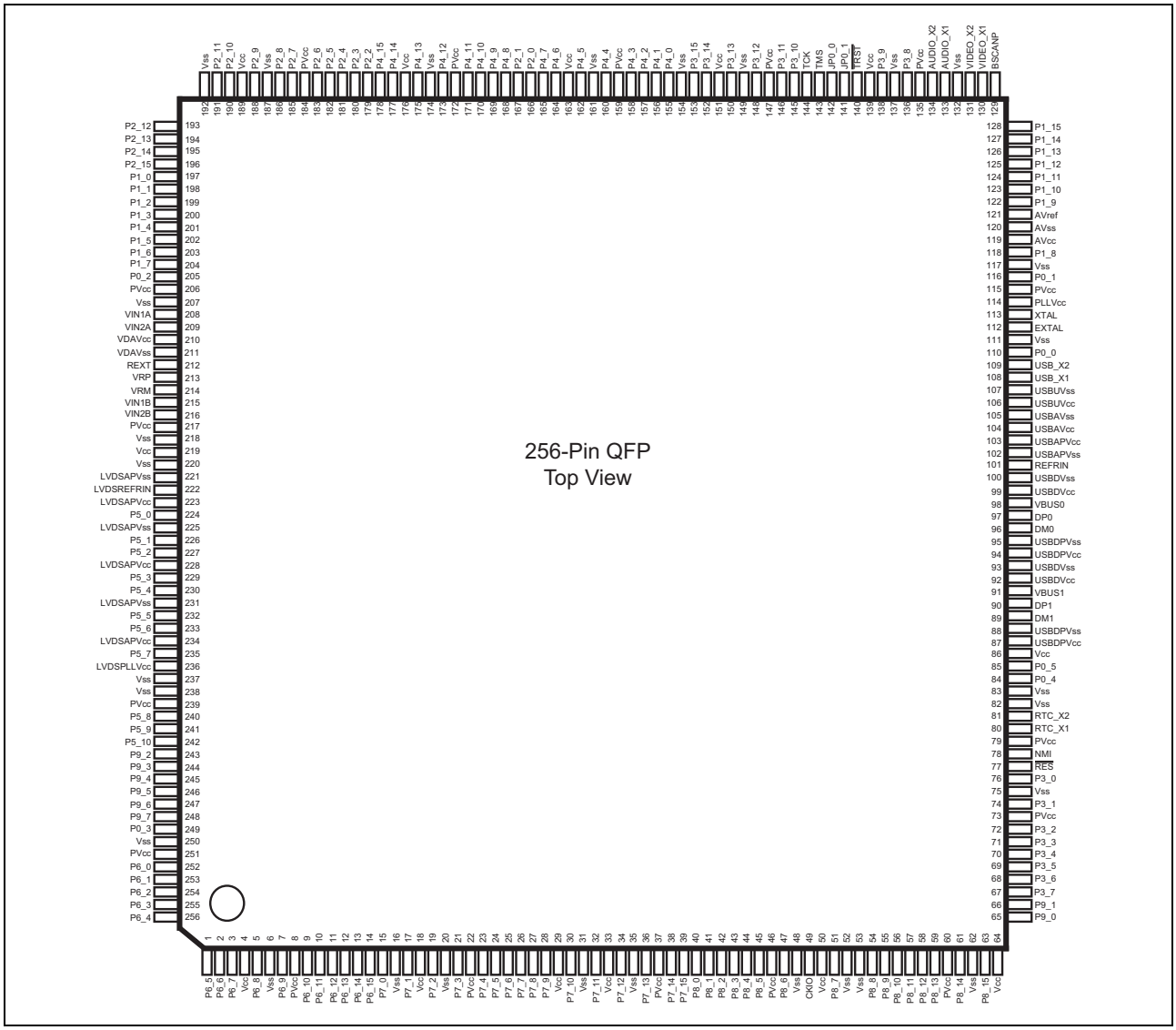
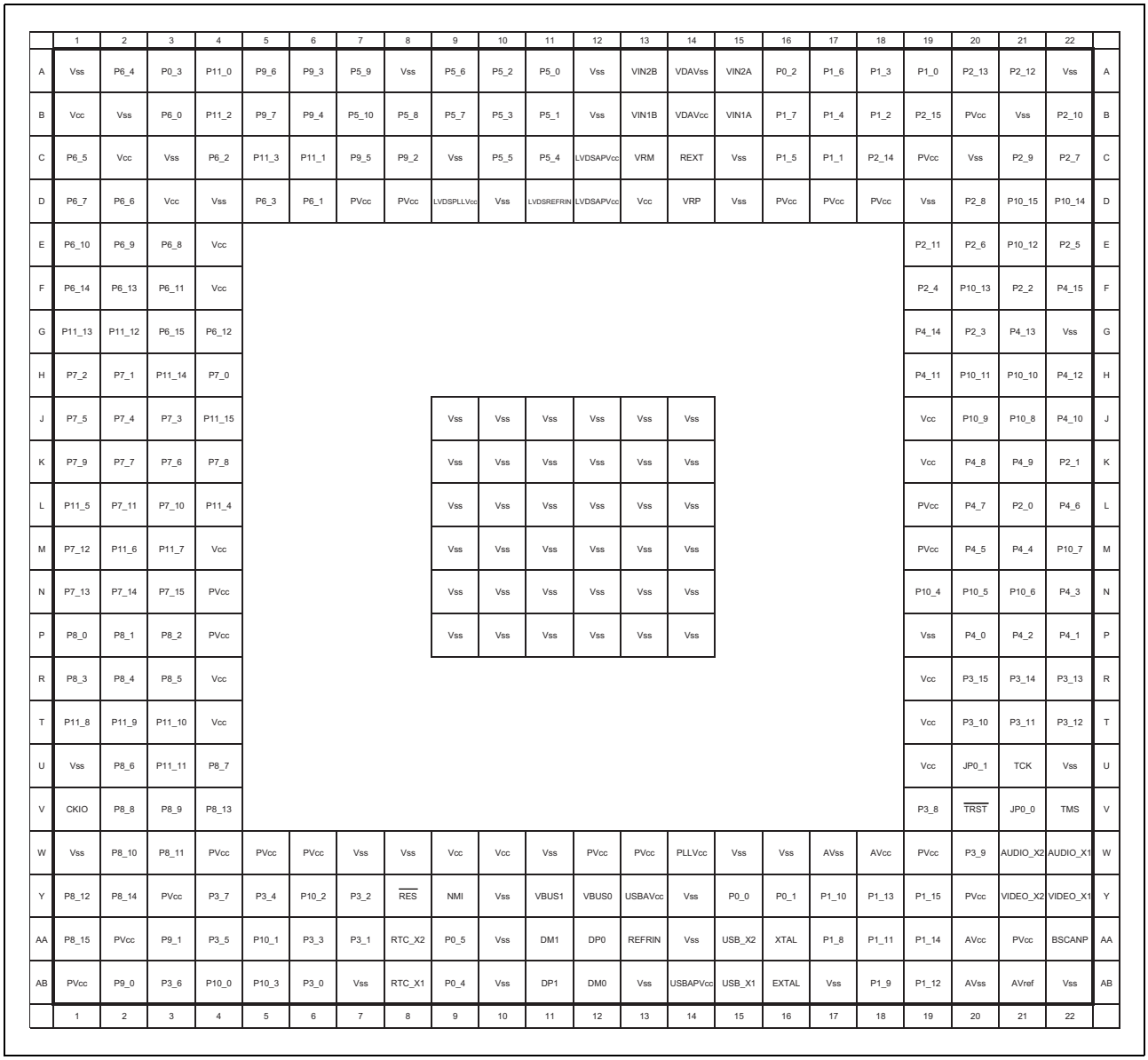


Figure 2.3 Pin Assignment of the 256-Pin QFP (Top Perspective View)



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	
A	Vss	P6_4	P0_3	P11_0	P9_6	P9_3	P5_9	Vss	P5_6	P5_2	P5_0	Vss	VIN2B	VDAVss	VIN2A	P0_2	P1_6	P1_3	P1_0	P2_13	P2_12	Vss	A
B	Vcc	Vss	P6_0	P11_2	P9_7	P9_4	P5_10	P5_8	P5_7	P5_3	P5_1	Vss	VIN1B	VDAVcc	VIN1A	P1_7	P1_4	P1_2	P2_15	PVcc	Vss	P2_10	B
C	P6_5	Vcc	Vss	P6_2	P11_3	P11_1	P9_5	P9_2	Vss	P5_5	P5_4	LVDSAPVcc	VRM	REXT	Vss	P1_5	P1_1	P2_14	PVcc	Vss	P2_9	P2_7	C
D	P6_7	P6_6	Vcc	Vss	P6_3	P6_1	PVcc	PVcc	LVDSPLLVcc	Vss	LVDSREFRIN	LVDSAPVcc	Vcc	VRP	Vss	PVcc	PVcc	PVcc	Vss	P2_8	P10_15	P10_14	D
E	P6_10	P6_9	P6_8	Vcc															P2_11	P2_6	P10_12	P2_5	E
F	P6_14	P6_13	P6_11	Vcc															P2_4	P10_13	P2_2	P4_15	F
G	P11_13	P11_12	P6_15	P6_12															P4_14	P2_3	P4_13	Vss	G
H	P7_2	P7_1	P11_14	P7_0															P4_11	P10_11	P10_10	P4_12	H
J	P7_5	P7_4	P7_3	P11_15					Vss	Vss	Vss	Vss	Vss	Vss					Vcc	P10_9	P10_8	P4_10	J
K	P7_9	P7_7	P7_6	P7_8					Vss	Vss	Vss	Vss	Vss	Vss					Vcc	P4_8	P4_9	P2_1	K
L	P11_5	P7_11	P7_10	P11_4					Vss	Vss	Vss	Vss	Vss	Vss					PVcc	P4_7	P2_0	P4_6	L
M	P7_12	P11_6	P11_7	Vcc					Vss	Vss	Vss	Vss	Vss	Vss					PVcc	P4_5	P4_4	P10_7	M
N	P7_13	P7_14	P7_15	PVcc					Vss	Vss	Vss	Vss	Vss	Vss					P10_4	P10_5	P10_6	P4_3	N
P	P8_0	P8_1	P8_2	PVcc					Vss	Vss	Vss	Vss	Vss	Vss					Vss	P4_0	P4_2	P4_1	P
R	P8_3	P8_4	P8_5	Vcc															Vcc	P3_15	P3_14	P3_13	R
T	P11_8	P11_9	P11_10	Vcc															Vcc	P3_10	P3_11	P3_12	T
U	Vss	P8_6	P11_11	P8_7															Vcc	JP0_1	TCK	Vss	U
V	CKIO	P8_8	P8_9	P8_13															P3_8	$\overline{\text{TRST}}$	JP0_0	TMS	V
W	Vss	P8_10	P8_11	PVcc	PVcc	PVcc	Vss	Vss	Vcc	Vcc	Vss	PVcc	PVcc	PLLVcc	Vss	Vss	AVss	AVcc	PVcc	P3_9	AUDIO_X2	AUDIO_X1	W
Y	P8_12	P8_14	PVcc	P3_7	P3_4	P10_2	P3_2	$\overline{\text{RES}}$	NMI	Vss	VBUS1	VBUS0	USBAVcc	Vss	P0_0	P0_1	P1_10	P1_13	P1_15	PVcc	VIDEO_X2	VIDEO_X1	Y
AA	P8_15	PVcc	P9_1	P3_5	P10_1	P3_3	P3_1	RTC_X2	P0_5	Vss	DM1	DP0	REFRIN	Vss	USB_X2	XTAL	P1_8	P1_11	P1_14	AVcc	PVcc	BSCANP	AA
AB	PVcc	P9_0	P3_6	P10_0	P10_3	P3_0	Vss	RTC_X1	P0_4	Vss	DP1	DM0	Vss	USBAPVcc	USB_X1	EXTAL	Vss	P1_9	P1_12	AVss	AVref	Vss	AB
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	

Figure 2.4 Pin Assignment of the 324-Pin BGA (Top Perspective View)

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3.1 Absolute Maximum Ratings

Item		Symbol	Value	Unit
Power supply voltage (I/O)		PV_{CC}	–0.3 to 4.2	V
Power supply voltage (Internal)		V_{CC}	–0.3 to 1.6	V
PLL power supply voltage		$PLLV_{CC}$	–0.3 to 1.6	V
Analog power supply voltage		AV_{CC}	–0.3 to 4.2	V
Analog reference voltage		AVref	–0.3 to AV_{CC} +0.3	V
USB transceiver analog power supply voltage (I/O)		$USBAPV_{CC}$	–0.3 to 4.2	V
USB transceiver digital power supply voltage (I/O) Note: Products in BGA packages do not have this pin.		$USBDPV_{CC}$	–0.3 to 4.2	V
USB transceiver analog power supply voltage (internal)		$USBAV_{CC}$	–0.3 to 1.6	V
USB transceiver digital power supply voltage (internal) Note: Products in BGA packages do not have this pin.		$USBDV_{CC}$	–0.3 to 1.6	V
Power supply for USB 480 MHz (internal) Note: Products in BGA packages do not have this pin.		$USBUV_{CC}$	–0.3 to 1.6	V
A/D converter power supply voltage for video signal input		$VDAV_{CC}$	–0.3 to 4.2	V
LVDS analog power supply voltage		$LVDSAPV_{CC}$	–0.3 to 4.2	V
LVDS PLL power supply voltage		$LVDSPLLV_{CC}$	–0.3 to 1.6	V
Input voltage	VBUS	V_{in}	–0.3 to 5.5	V
	Other input pins	V_{in}	–0.3- to 3.3-V power supply (PV_{CC}, AV_{CC}, $USBAPV_{CC}$, $USBDPV_{CC}$, $VDAV_{CC}$, $LVDSAPV_{CC}$) +0.3	V
Operating temperature	Ambient temperature	Ta	–40 to +85	°C
	Junction temperature	Tj	–40 to +125	°C
Storage temperature		T_{stg}	–55 to +125	°C

Caution: Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

3.2 Power-On/Power-Off Sequence

The 1.2-V power supply (V_{CC}, $PLLV_{CC}$, $USBAV_{CC}$, $USBDV_{CC}$, $USBUV_{CC}$, and $LVDSPLLV_{CC}$) and 3.3-V power supply (PV_{CC}, AV_{CC}, $USBAPV_{CC}$, $USBDPV_{CC}$, $VDAV_{CC}$, and $LVDSAPV_{CC}$) can be turned on and off in any order.
When turning on the power, be sure to drive both the $\overline{TRST}$ and $\overline{RES}$ pins low; otherwise, the output pins and input/output pins output undefined levels, resulting in system malfunction.
When turning off the power, drive the $\overline{TRST}$ and $\overline{RES}$ pins low if the undefined output may cause a problem.

3.3 DC Characteristics

- Conditions used to obtain DC characteristics (2) in Table 3.2 other than current consumption
  V_{CC} = USBDV_{CC}= USBUV_{CC} = 1.10 to 1.26 V, PV_{CC} = USBDPV_{CC} = 3.0 to 3.6 V, PLLV_{CC} = 1.10 to 1.26 V,
  AV_{CC} = 3.0 to 3.6 V, USBAPV_{CC} = 3.0 to 3.6 V, USBAV_{CC} = 1.10 to 1.26 V, VDAV_{CC} = 3.0 to 3.6 V,
  LVDSAPV_{CC} = 3.0 to 3.6 V, LVDSPLLV_{CC} = 1.10 to 1.26 V,
  V_{SS} = AV$_{SS}$ = USBDV_{SS} = USBAV_{SS} = USBDPV_{SS} = USBAPV_{SS} = USBUV_{SS} = VDAV_{SS} = LVDSAPV_{SS} = 0 V,
  Ta = –40 to 85 °C, Tj = –40 to 125 °C

- Conditions used to obtain DC characteristics (2) in Table 3.2 for current consumption
  V_{CC} = USBDV_{CC} = USBUV_{CC} = 1.18 V, PV_{CC} = USBDPV_{CC} = 3.3 V, PLLV_{CC} = 1.18 V, AV_{CC} = 3.3 V,
  USBAPV_{CC} = 3.3 V, USBAV_{CC} = 1.18 V, VDAV_{CC} = 3.3 V, LVDSAPV_{CC} = 3.3 V, LVDSPLLV_{CC} = 1.18 V,
  V_{SS} = AV$_{SS}$ = USBDV_{SS} = USBAV_{SS} = USBDPV_{SS} = USBAPV_{SS} = USBUV_{SS} = VDAV_{SS} = LVDSAPV_{SS} = 0 V,
  AVref = 3.3 V, VBUS = 5.0 V,
  Ta = –40 to 85 °C, Tj = –40 to 125 °C
  Iϕ = 400.00 MHz, Bϕ = 133.33 MHz, P1ϕ = 66.67 MHz, P0ϕ = 33.33 MHz

Note: Products in BGA packages do not have USBDV_{CC}, USBUV_{CC}, USBDPV_{CC}, USBDV_{SS}, USBAV_{SS}, USBDPV_{SS}, USBAPV_{SS}, USBUV_{SS}, and LVDSAPV_{SS} pins.

Table 3.2 DC Characteristics (1) [Common Items]

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Power supply voltage		PV_{CC}	3.0	3.3	3.6	V	
		V_{CC}	1.10	1.18	1.26	V	
PLL power supply voltage		PLLV_{CC}	1.10	1.18	1.26	V	
Analog power supply voltage		AV_{CC}	3.0	3.3	3.6	V	
USB power supply voltage Note: Products in BGA packages do not have USBDPVcc, USBDVcc, and USBUVcc pins.		USBAPV_{CC} USBDPV_{CC}	3.0	3.3	3.6	V	
		USBAV_{CC} USBDV_{CC} USBUV_{CC}	1.10	1.18	1.26	V	
A/D converter power supply voltage for video signal input		VDAV_{CC}	3.0	3.3	3.6	V	
LVDS analog power supply voltage		LVDSAPV_{CC}	3.0	3.3	3.6	V	
LVDS PLL power supply voltage		LVDSPLLV_{CC}	1.10	1.18	1.26	V	
Input leakage current	All input pins	$\|I_{in}\|$	—	—	1.0	µA	V_{in} = 0.5 to PV_{CC} – 0.5 V
Three-state leakage current	All input/output pins, all output pins (except P1_0 to P1_7) (off state)	$\|I_{STI}\|$	—	—	1.0	µA	V_{in} = 0.5 to PV_{CC} – 0.5 V
	P1_0 to P1_7		—	—	10	µA	
Input capacitance	all input/output pins, all input pins	Cin	—	—	10	pF	

Table 3.2 DC Characteristics (2) [Current Consumption]

Item		Power Supply	Symbol	Typ.	Max.	Unit	Test Conditions
Current consumption in normal operation		V_{CC}	I_{CC}	—	850	mA	
		$PLLV_{CC}$	$PLLI_{CC}$	—	8	mA	
		PV_{CC}	PI_{CC}	100*1	—	mA	
		AV_{CC}	AI_{CC}	—	4	mA	During A/D conversion
		AVref	AIref	—	1	mA	During A/D conversion
		$USBAV_{CC}$	UAI_{CC}	—	6	mA	When the USB host/function is in use.
		$USBDV_{CC}$ + $USBUV_{CC}$	UDI_{CC}*2	—	25	mA	In USB high-speed operation (2ch)
		$USBAPV_{CC}$	$UAPI_{CC}$	—	4	mA	When the USB host/function is in use.
		$USBDPV_{CC}$	$UDPI_{CC}$*3	70*1	—	mA	In USB high-speed operation (2ch)
		$VDAV_{CC}$	$VDAI_{CC}$	—	60	mA	
		$LVDSAPV_{CC}$	$LVDSAPI_{CC}$	—	48	mA	During LVDS transfer
		$LVDSPLLV_{CC}$	$LVDSPLLI_{CC}$	—	2.5	mA	
		VBUS	VI_{CC}	—	10	µA	
Current consumption in sleep mode		V_{CC}	Isleep	—	660	mA	
		For the other power supply, the current consumption is the same as in normal operation.					
Current consumption in software standby mode	Ta > 50 °C	V_{CC} + $PLLV_{CC}$ + $USBAV_{CC}$ + $USBDV_{CC}$ + $USBUV_{CC}$ + $LVDSPLLV_{CC}$	Isstby	72	320	mA	
		PV_{CC} + AV_{CC} + AVref + $USBAPV_{CC}$ + $USBDPV_{CC}$ + $VDAV_{CC}$ + $LVDSAPV_{CC}$	PIsstby	25	32	µA	
		VBUS	VIsstby	8	10	µA	
	Ta ≤ 50 °C	V_{CC} + $PLLV_{CC}$ + $USBAV_{CC}$ + $USBDV_{CC}$ + $USBUV_{CC}$ + $LVDSPLLV_{CC}$	Isstby	20	160	mA	
		PV_{CC} + AV_{CC} + AVref + $USBAPV_{CC}$ + $USBDPV_{CC}$ + $VDAV_{CC}$ + $LVDSAPV_{CC}$	PIsstby	18	21	µA	
		VBUS	VIsstby	8	10	µA	

Table 3.2 DC Characteristics (2) [Current Consumption]

Item		Power Supply	Symbol	Typ.	Max.	Unit	Test Conditions
Current consumption in deep standby mode	Ta > 50 °C	V_{CC} + $PLLV_{CC}$ + $USBAV_{CC}$ + $USBDV_{CC}$ + $USBUV_{CC}$ + $LVDSPLLV_{CC}$	Idstdby	124	180	µA	RAM 0 Kbytes retained, RTC_X1 selected
				148	204	µA	RAM 16 Kbytes retained, RTC_X1 selected
				164	228	µA	RAM 32 Kbytes retained, RTC_X1 selected
				200	276	µA	RAM 64 Kbytes retained, RTC_X1 selected
				289	372	µA	RAM 128 Kbytes retained, RTC_X1 selected
				When the EXTAL 13 MHz is selected, 5 µA and 7 µA are added to the "Typ." and "Max." values above, respectively. When the RTC_X3 is selected, 2 µA and 3 µA are added to the "Typ." and "Max." values above, respectively.			
		PV_{CC} + AV_{CC} + AVref + $USBAPV_{CC}$ + $USBDPV_{CC}$ $VDAV_{CC}$ + $LVDSAPV_{CC}$	PIdstby	18	26	µA	RTC is not operating
				25	36	µA	RTC_X1 selected
				0.6	—	mA	RTC_X3 selected, small gain*1
				1	—	mA	EXTAL 13 MHz selected, small gain*1
		VBUS	VIdstby	8	10	µA	
	Ta ≤ 50 °C	V_{CC} + $PLLV_{CC}$ + $USBAV_{CC}$ + $USBDV_{CC}$+ $USBUV_{CC}$+ $LVDSPLLV_{CC}$	Idstdby	40	70	µA	RAM 0 Kbytes retained, RTC_X1 selected
				50	90	µA	RAM 16 Kbytes retained, RTC_X1 selected
				60	110	µA	RAM 32 Kbytes retained, RTC_X1 selected
				80	150	µA	RAM 64 Kbytes retained, RTC_X1 selected
				120	230	µA	RAM 128 Kbytes retained, RTC_X1 selected
				When the EXTAL 13 MHz is selected, 5 µA and 7 µA are added to the "Typ." and "Max." values above, respectively. When the RTC_X3 is selected, 2 µA and 3 µA are added to the "Typ." and "Max." values above, respectively.			
		PV_{CC} + AV_{CC} + AVref + $USBAPV_{CC}$ + $USBDPV_{CC}$ + $VDAV_{CC}$ + $LVDSAPV_{CC}$	PIdstby	15	19	µA	RTC is not operating
				22	29	µA	RTC_X1 selected
				0.6	—	mA	RTC_X3 selected, small gain*1
				1	—	mA	EXTAL 13 MHz selected, small gain*1
		VBUS	VIdstby	8	10	µA	

Note 1. Reference value. The actual operating current greatly depends on the system (such as slow rising/falling edges caused by IO load and toggle frequency). Be sure to determine the value using the actual system.
Note 2. In the products in BGA packages, UDIcc is added to Icc.
Note 3. In the products in BGA packages, UDPIcc is added to PIcc.

Table 3.2 DC Characteristics (3) [Except I²C Bus Interface, and USB 2.0 Host/Function Module-Related Pins]

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input high voltage*		V_{IH}	2.2	—	PV_{CC} + 0.3	V	
Input low voltage*		V_{IL}	–0.3	—	0.8	V	
Schmitt trigger input characteristics		VT^+	$PV_{CC} \times 0.66$	—	—	V	
		VT^-	—	—	0.8	V	
		$VT^+ – VT^-$	0.2	—	—	V	
Output high voltage		V_{OH}	PV_{CC} – 0.5	—	—	V	I_{OH} = –2.0 mA
Output low voltage		V_{OL}	—	—	0.4	V	I_{OL} = 2.0 mA
RAM standby voltage	Software standby mode (large-capacity on-chip RAM)	V_{RAMS}	0.85	—	—	V	Measured with V_{CC} as parameter
	Deep standby mode (only the on-chip RAM for data retention)	V_{RAMD}	1.10	—	—	V	

Note: * Values for the input of data for boundary scanning through pins TMS, TCK, JP0_0, JP0_1, P2_0 to P2_15, and P6_0 to P6_15.

Table 3.2 DC Characteristics (4) [I²C Bus Interface Related Pins*]

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input high voltage	V_{IH}	$PV_{CC} \times 0.7$	—	PV_{CC} + 0.3	V	
Input low voltage	V_{IL}	–0.3	—	$PV_{CC} \times 0.3$	V	
Schmitt trigger input characteristics	$V_{IH} – V_{IL}$	$PV_{CC} \times 0.05$	—	—	V	
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 3.0 mA

Note: * The P1_0 to P1_7 pins are open-drain pins.

Table 3.2 DC Characteristics (5) [USB 2.0 Host/Function Module-Related Pins*]

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Reference resistance	R_{REF}	5.6 kΩ ± 1%	5.6 kΩ ± 1%	5.6 kΩ ± 1%		
Input high voltage (VBUS1, VBUS0)	V_{IH}	4.02	—	5.25	V	
Input low voltage (VBUS1, VBUS0)	V_{IL}	–0.3	—	0.5	V	
Input high voltage (USB_X1)	V_{IH}	PV_{CC} – 0.5	—	PV_{CC} + 0.3	V	
Input low voltage (USB_X1)	V_{IL}	–0.3	—	0.5	V	

Note: * REFRIN, VBUS1, VBUS0, USB_X1, and USB_X2 pins

Table 3.2 DC Characteristics (6) [USB 2.0 Host/Function Module-Related Pins* (Low-Speed, Full-Speed, and High-Speed Common Items)]

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
DP pull-up resistance (when function is selected)	R_{pu}	0.900	—	1.575	kΩ	In idle mode
		1.425	—	3.090	kΩ	In transmit/receive mode
DP and DM pull-down resistance (when host is selected)	R_{pd}	14.25	—	24.80	kΩ	

Note: * DP1, DP0, DM1, and DM pins

Table 3.2 DC Characteristics (7) [USB 2.0 Host/Function Module-Related Pins* (Low-Speed and Full-Speed)]

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input high voltage	V_{IH}	2.0	—	—	V	
Input low voltage	V_{IL}	—	—	0.8	V	
Differential input sensitivity	V_{DI}	0.2	—	—	V	| (DP) – (DM) |
Differential common mode range	V_{CM}	0.8	—	2.5	V	
Output high voltage	V_{OH}	2.8	—	3.6	V	I_{OH} = –200 μA
Output low voltage	V_{OL}	0.0	—	0.3	V	I_{OL} = 2 mA
Output signal crossover voltage	V_{CRS}	1.3	—	2.0	V	C_L = 50 pF (full-speed) C_L = 200 to 600 pF (low-speed)

Note: * DP1, DP0, DM1, and DM pins

Table 3.2 DC Characteristics (8) [USB 2.0 Host/Function Module-Related Pins* (High-Speed)]

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Squelch detection threshold voltage (differential voltage)	V_{HSSQ}	100	—	150	mV	
Common mode voltage range	V_{HSCM}	–50	—	500	mV	
Idle state	V_{HSOI}	–10.0	—	10.0	mV	
Output high voltage	V_{HSOH}	360	—	440	mV	
Output low voltage	V_{HSOL}	–10.0	—	10.0	mV	
Chirp J output voltage (difference)	V_{CHIRPJ}	700	—	1100	mV	
Chirp K output voltage (difference)	V_{CHIRPK}	–900	—	–500	mV	

Note: * DP1, DP0, DM1, and DM pins

Table 3.2 DC Characteristics (9) [LVDS-Related Pins*]

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Reference resistance	$R_{LVDSREF}$		5.6kΩ±1%			
Differential Output Voltage	VOD	250	350	450	mV	RL = 100Ω
Difference VOD between 'H' and 'L'	ΔVOD	—	—	50	mV	RL = 100Ω
Offset (Common Mode) Voltage	VOS	1.125	1.25	1.375	V	RL = 100Ω
Difference VOS between 'H' and 'L'	ΔVOS	—	—	50	mV	RL = 100Ω

Note: * LVDSREFRIN, TXCLKOUTP, TXCLKOUTM, TXOUT2P to TXOUT0P, and TXOUT2M to TXOUT0M pins

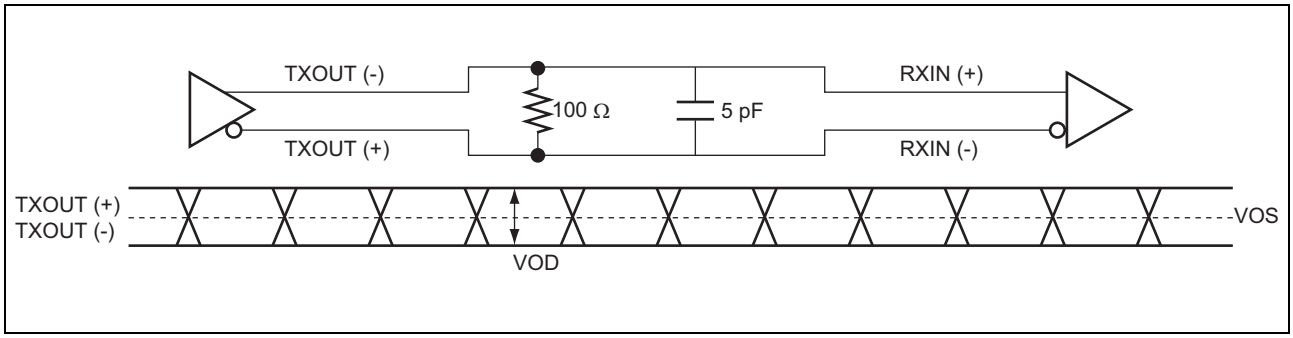


Figure 3.1 LVDS Output Waveform

Table 3.3 Permissible Output Currents

Item		Symbol	Min.	Typ.	Max.	Unit
Permissible output low current (per pin)	P1_0 to P1_7	I_{OL}	—	—	10	mA
	Output pins other than above		—		2	mA
Permissible output high current (per pin)		$-I_{OH}$	—	—	2	mA
Permissible output current (total)		ΣI_O	—	—	150	mA

Caution: To protect the LSI's reliability, do not exceed the output current values in Table 3.3.

3.4 AC Characteristics

Signals input to this LSI are basically handled as signals in synchronization with a clock. The setup and hold times for input pins must be followed.

Conditions for AC characteristics: V_{CC} = $USBDV_{CC}$ = $USBUV_{CC}$ = 1.10 to 1.26 V, PV_{CC} = $USBDPV_{CC}$ = 3.0 to 3.6 V, $PLLV_{CC}$ = 1.10 to 1.26 V, AV_{CC} = 3.0 to 3.6 V, $USBAPV_{CC}$ = 3.0 to 3.6 V, $USBAV_{CC}$ = 1.10 to 1.26 V, $VDAV_{CC}$ = 3.0 to 3.6 V, $LVDSAPV_{CC}$ = 3.0 to 3.6 V, $LVDSPLLV_{CC}$ = 1.10 to 1.26 V,
V_{SS} = AV_{SS} = $USBDV_{SS}$ = $USBAV_{SS}$ = $USBDPV_{SS}$ = $USBAPV_{SS}$ = $USBUV_{SS}$ = $VDAV_{SS}$ = $LVDSAPV_{SS}$ = 0 V,
Ta = –40 to 85 °C, Tj = –40 to 125 °C

Note: Products in BGA packages do not have $USBDV_{CC}$, $USBUV_{CC}$, $USBDPV_{CC}$, $USBDV_{SS}$, $USBAV_{SS}$, $USBDPV_{SS}$, $USBAPV_{SS}$, $USBUV_{SS}$, and $LVDSAPV_{SS}$ pins.

Table 3.4 Operating Frequency

Item		Symbol	Min.	Max.	Unit	Remarks
Operating frequency	CPU clock (Iϕ)	f	100.00	400.00	MHz	
	Image processing clock (Gϕ)		100.00	266.67	MHz	
	Internal bus clock (Bϕ)		100.00	133.33	MHz	
	Peripheral clock 1 (P1ϕ)		50.00	66.67	MHz	
	Peripheral clock 0 (P0ϕ)		25.00	33.33	MHz	

3.4.1 Clock Timing

Table 3.5 Clock Timing

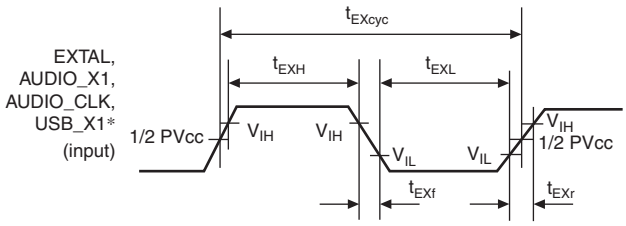
Item	Symbol	Min.	Max.	Unit	Figure
EXTAL clock input frequency (when the clock is supplied to USB 2.0 host/function module)	f_{EX}	12MHz ± 100ppm			Figure 3.2
EXTAL clock input frequency (when the clock isn't supplied to USB 2.0 host/function module)		10.00	13.33	MHz	
EXTAL clock input cycle time (when the clock isn't supplied to USB 2.0 host/function module)	t_{EXcyc}	75.00	100.00	ns	
AUDIO_X1 clock input frequency (crystal resonator connected)	f_{EX}	10.00	50.00	MHz	
AUDIO_X1 clock input cycle time (crystal resonator connected)	t_{EXcyc}	20.00	100.00	ns	
AUDIO_X1, AUDIO_CLK clock input frequency (external clock input)	f_{EX}	1.00	50.00	MHz	
AUDIO_X1, AUDIO_CLK clock input cycle time (external clock input)	t_{EXcyc}	20.00	1000.00	ns	
USB_X1 clock input frequency (when the 48-MHz clock is supplied to USB 2.0 host/function module and high-speed transfer function is used)	f_{EX}	48 MHz ±100 ppm			
USB_X1 clock input frequency (when the 48-MHz clock is supplied to USB 2.0 host/function module, high-speed transfer function is not used, and host controller function is used)		48 MHz ±500 ppm			
USB_X1 clock input frequency (when the 48-MHz clock is supplied to USB 2.0 host/function module, high-speed transfer function is not used, and host controller function is not used)		48 MHz ±2500 ppm			
VIDEO_X1 clock input frequency		27MHz ±50 ppm*1			
EXTAL, AUDIO_X1, AUDIO_CLK, USB_X1 clock input low pulse width	t_{EXL}	0.4	0.6	t_{EXcyc}	
VIDEO_X1 clock input low pulse width		0.45	0.55		
EXTAL, AUDIO_X1, AUDIO_CLK, USB_X1 clock input high pulse width	t_{EXH}	0.4	0.6	t_{EXcyc}	
VIDEO_X1 clock input high pulse width		0.45	0.55		
EXTAL, AUDIO_X1, AUDIO_CLK, USB_ X1 clock input rise time	t_{EXr}	—	4	ns	
VIDEO_X1 clock input rise time		—	3		
EXTAL, AUDIO_X1, AUDIO_CLK, USB_ X1 clock input fall time	t_{EXf}	—	4	ns	
VIDEO_X1 clock input fall time		—	3		
CKIO clock output frequency	f_{OP}	50.00	66.67	MHz	
CKIO clock output cycle time	t_{cyc}	15.00	20.00	ns	Figure 3.3 (1) and Figure 3.3 (2)
CKIO clock output low pulse width 1	t_{CKOL1}	$t_{cyc}/2 - t_{CKOr1}$	—	ns	Figure 3.3 (1)
CKIO clock output high pulse width 1	t_{CKOH1}	$t_{cyc}/2 - t_{CKOr1}$	—	ns	
CKIO clock output rise time 1	t_{CKOr1}	—	3	ns	
CKIO clock output fall time 1	t_{CKOf1}	—	3	ns	
CKIO clock output low pulse width 2	t_{CKOL2}	$t_{cyc}/2 - t_{CKOr2}$	—	ns	Figure 3.3 (2)
CKIO clock output high pulse width 2	t_{CKOH2}	$t_{cyc}/2 - t_{CKOr2}$	—	ns	
CKIO clock output rise time 2	t_{CKOr2}	—	2	ns	
CKIO clock output fall time 2	t_{CKOf2}	—	2	ns	

Table 3.5 Clock Timing

Item	Symbol	Min.	Max.	Unit	Figure
On-chip PLL circuit oscillation settling time	t_{POSC}	1	—	ms	Figure 3.4 and Figure 3.6 (1)
On-chip oscillation circuit oscillation settling time (RTC_X1)	t_{ROSC}	—	3*2	s	Figure 3.7
On-chip oscillation circuit oscillation settling time (RTC_X3)		—	10*2	ms	Figure 3.7
On-chip oscillation circuit oscillation settling time (other than above)		—	4*2	ms	Figure 3.4, Figure 3.6 (1), and Figure 3.7
Mode hold time	t_{MDH}	200	—	ns	Figure 3.4 and Figure 3.6 (1)
SSCG Stabilizing Time	tSSCG	1	—	us	Figure 3.5

Note 1. Reference value. The accuracy of the clock signal affects the quality of images output by the digital video decoder. Input clock signals that are as accurate as is possible.

Note 2. Settings for values smaller than the above specifications may be possible, as long as the values are confirmed through evaluation by the manufacturer of the oscillator.



Note: * When the clock is input on the EXTAL, AUDIO_X1, AUDIO_CLK, USB_X1, or VIDEO_X1

Figure 3.2 EXTAL, AUDIO_X1, AUDIO_CLK, USB_X1, and VIDEO_X1 Clock Input Timing

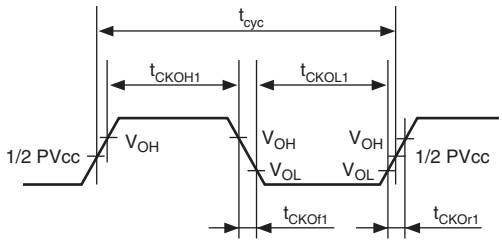


Figure 3.3 (1) CKIO Clock Output Timing 1

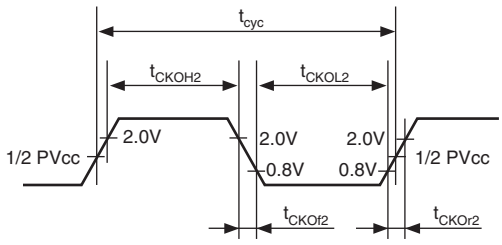


Figure 3.3 (2) CKIO Clock Output Timing 2

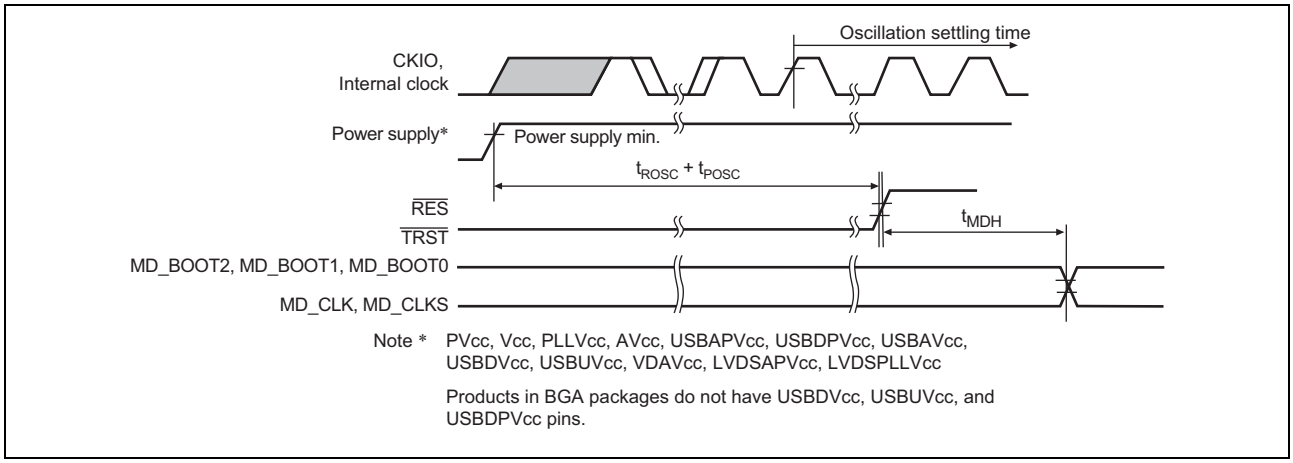


Figure 3.4 Power-On Oscillation Settling Time

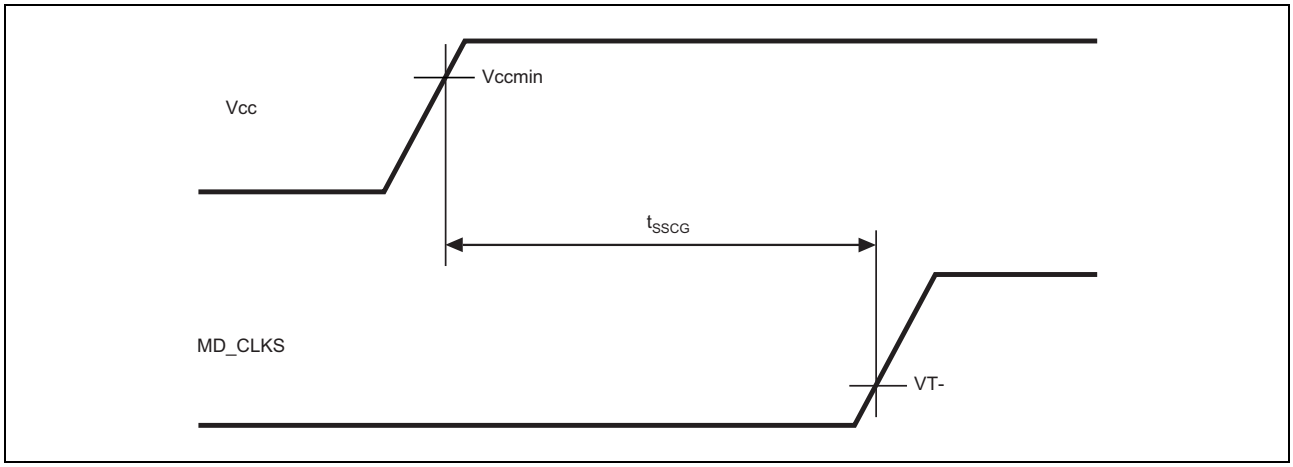


Figure 3.5 SSCG Stabilizing Time

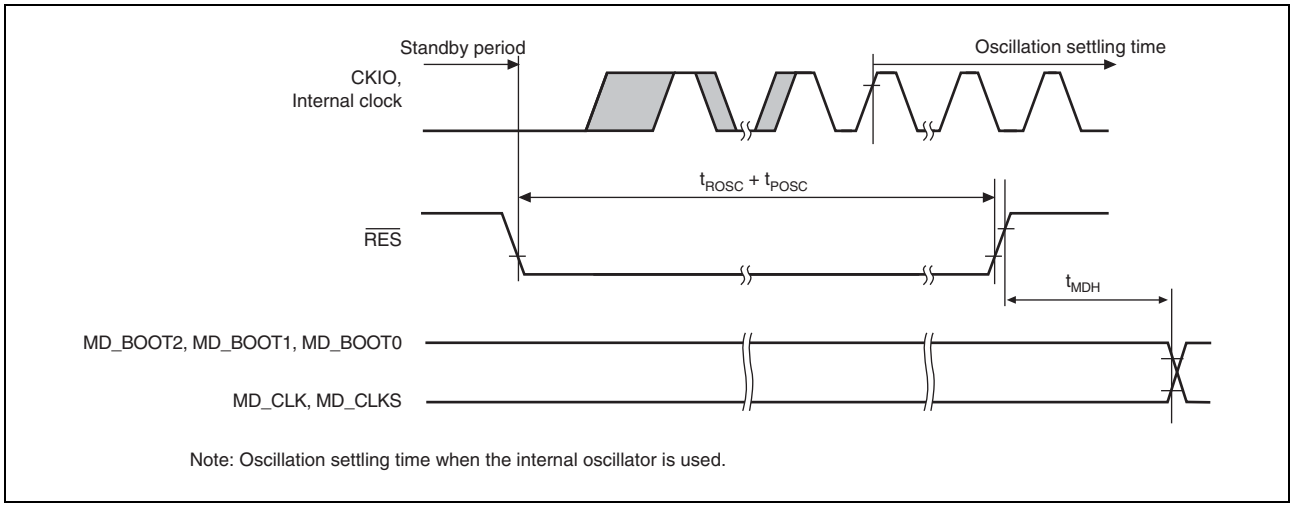


Figure 3.6 (1) Oscillation Settling Time on Return from Standby (Return by Reset)

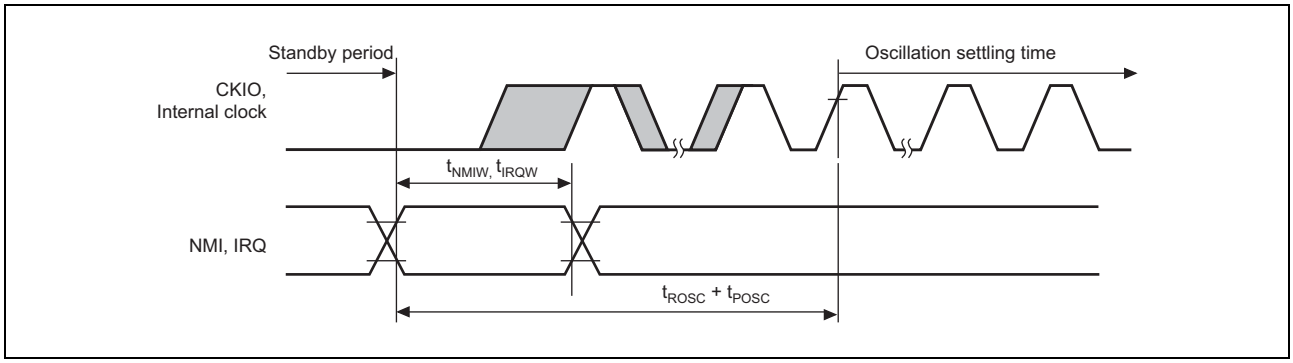
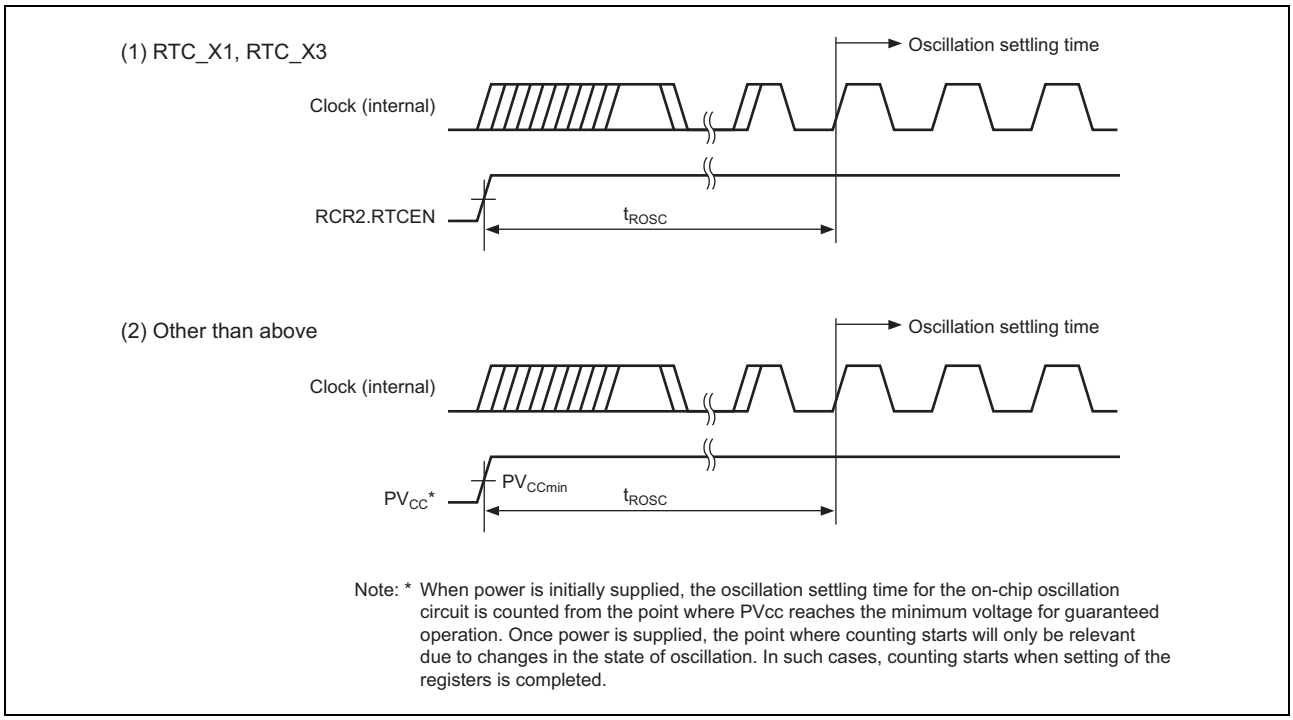


Figure 3.6 (2) Oscillation Settling Time on Return from Standby (Return by NMI or IRQ)



Note: * When power is initially supplied, the oscillation settling time for the on-chip oscillation circuit is counted from the point where PVcc reaches the minimum voltage for guaranteed operation. Once power is supplied, the point where counting starts will only be relevant due to changes in the state of oscillation. In such cases, counting starts when setting of the registers is completed.

Figure 3.7 On-chip Oscillation Circuit Oscillation Settling Time

3.4.2 Control Signal Timing

Table 3.6 Control Signal Timing

Item		Symbol	Min.	Max.	Unit	Figure
$\overline{\text{RES}}$ pulse width	Exit from standby mode	t_{RESW}	t_{ROSC} + t_{POSC}		ms	Figure 3.8 (1) Figure 3.6 (1)
	Other than above		20	—	t_{cyc}	
$\overline{\text{TRST}}$ pulse width		t_{TRSW}	20	—	t_{cyc}	
NMI pulse width		t_{NMIW}	20	—	t_{cyc}	Figure 3.8 (2) and Figure 3.6 (2)
IRQ pulse width		t_{IRQW}	20	—	t_{cyc}	
TINT pulse width		t_{TINTW}	20	—	t_{cyc}	
$\overline{\text{RES}}$ input rise time*1		t_{RSr}	—	500	µs	Figure 3.8 (3)
$\overline{\text{RES}}$ negating hold time*2		t_{RSNH}	0	—	ns	Figure 3.8 (4)

Note 1. Make sure that this specification is satisfied when the same signal is controlling the $\overline{\text{TRST}}$ and $\overline{\text{RES}}$ pins.
Note 2. Make sure that this specification is satisfied when different signals are controlling the $\overline{\text{TRST}}$ and $\overline{\text{RES}}$ pins.

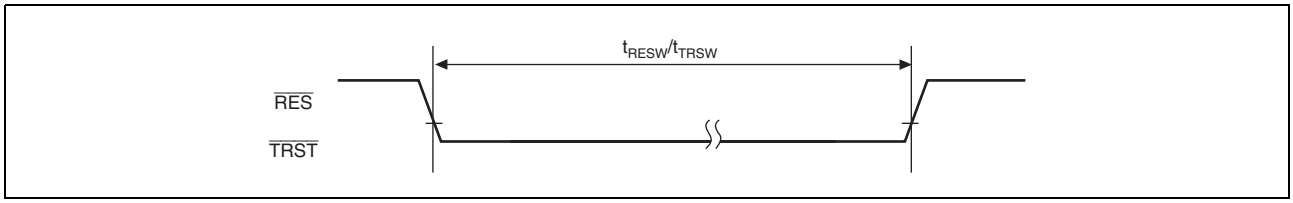


Figure 3.8 (1) Reset Input Timing 1

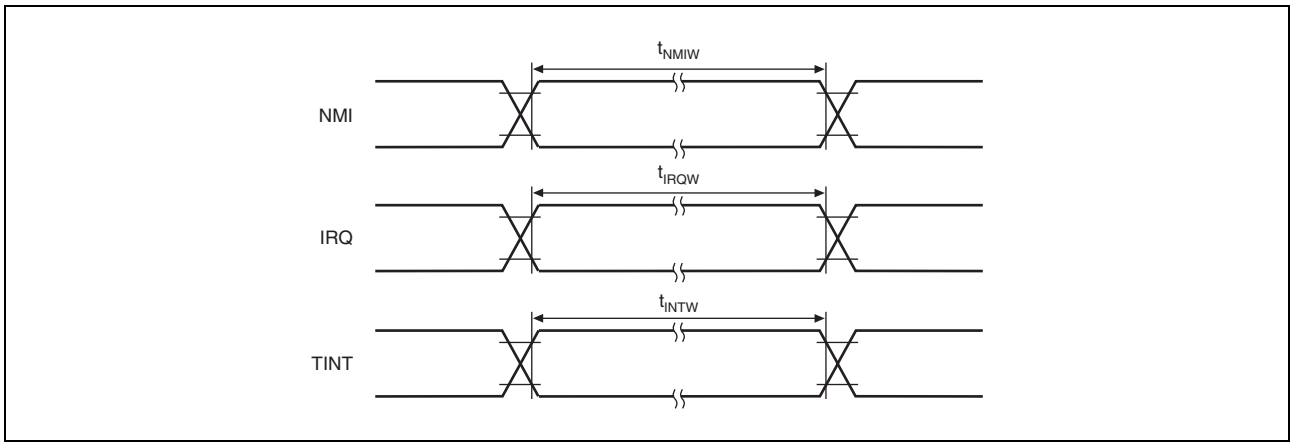


Figure 3.8 (2) Interrupt Signal Input Timing

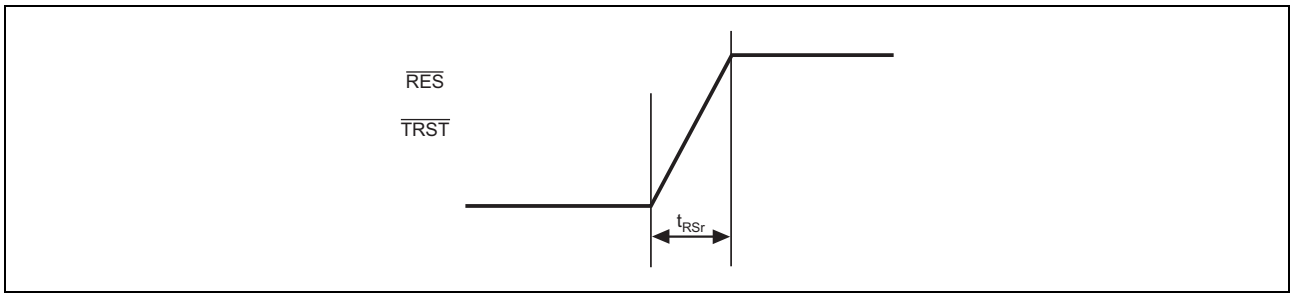


Figure 3.8 (3) Reset Input Timing 2

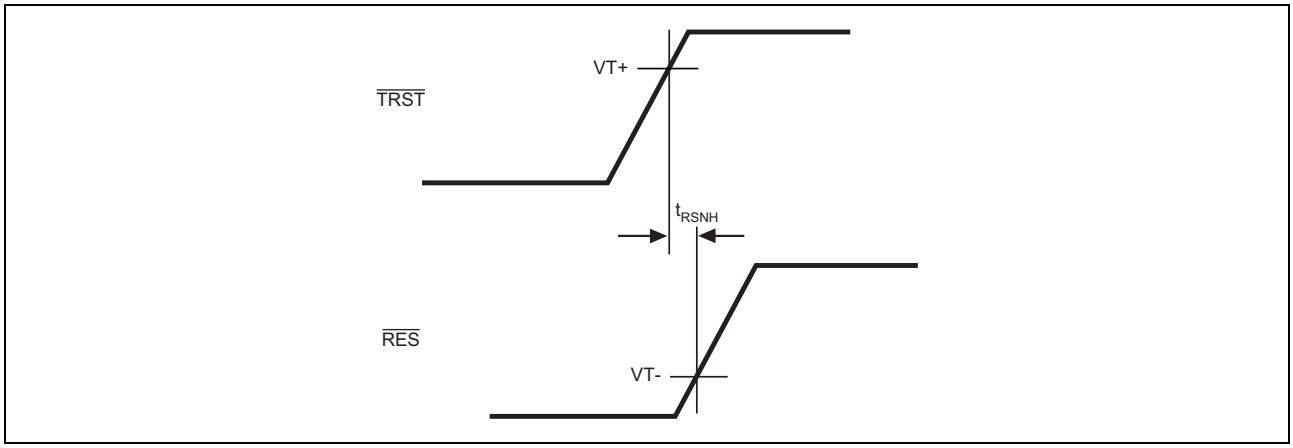


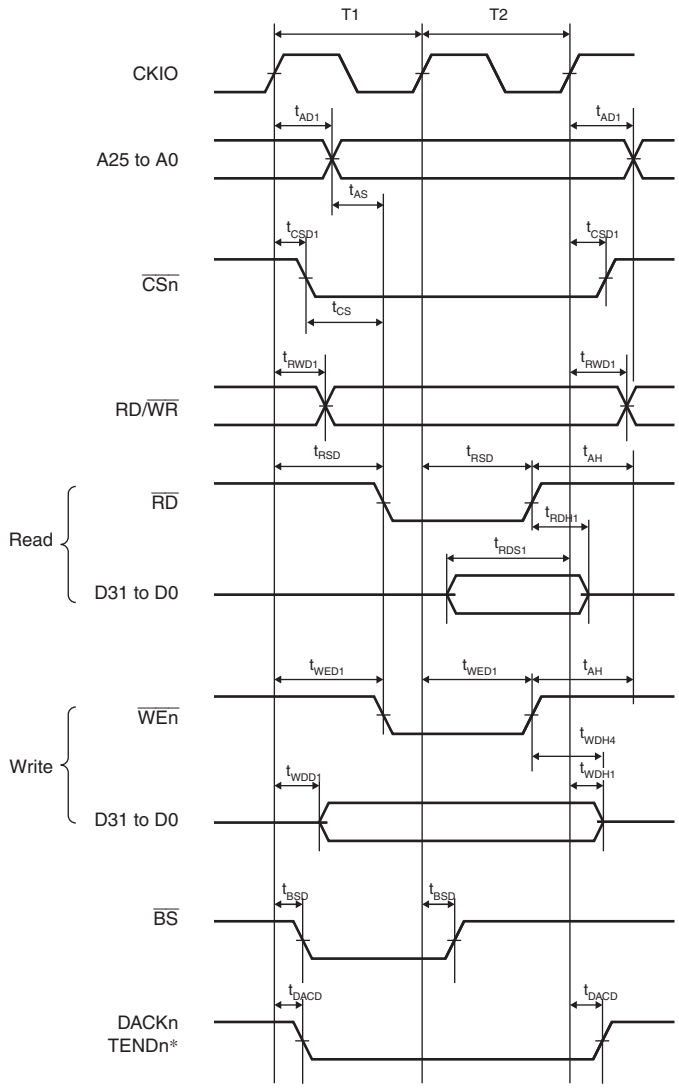
Figure 3.8 (4) Reset Input Timing 3

3.4.3 Bus Timing

Table 3.7 Bus Timing

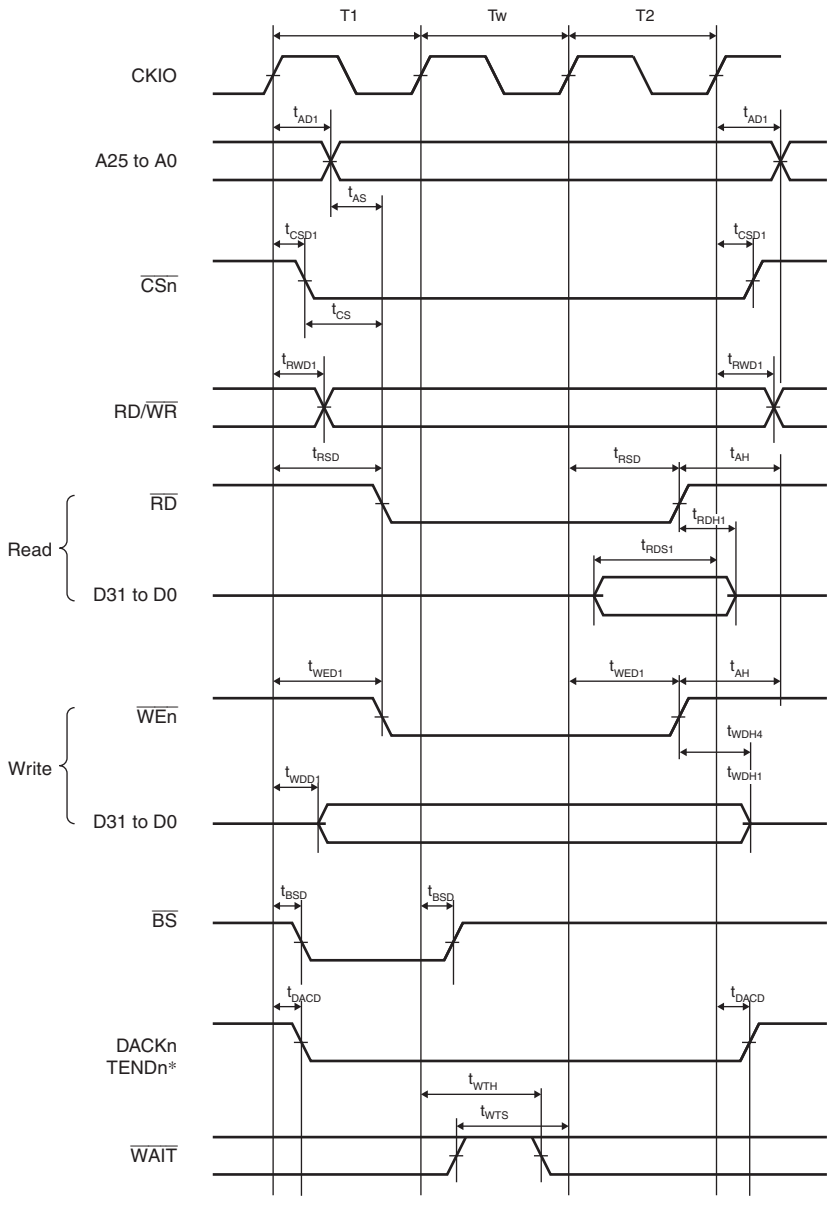
Item	Symbol	CKIO = 66.67 MHz*1 Min.	Max.	Unit	Figure
Address delay time 1	t_{AD1}	0/2*3	12	ns	Figure 3.9 to Figure 3.33
Address delay time 2	t_{AD2}	1/2t_{cyc}	1/2t_{cyc} + 12	ns	Figure 3.16
Address setup time	t_{AS}	0	—	ns	Figure 3.9 to Figure 3.12, Figure 3.16
Chip enable setup time	t_{CS}	0	—	ns	Figure 3.9 to Figure 3.12, Figure 3.16
Address hold time	t_{AH}	0	—	ns	Figure 3.9 to Figure 3.12
$\overline{BS}$ delay time	t_{BSD}	—	12	ns	Figure 3.9 to Figure 3.30
$\overline{CS}$ delay time 1	t_{CSD1}	0/2*3	12	ns	Figure 3.9 to Figure 3.33
Read write delay time 1	t_{RWD1}	0/2*3	12	ns	Figure 3.9 to Figure 3.33
Read strobe delay time	t_{RSD}	1/2t_{cyc}	1/2t_{cyc} + 12	ns	Figure 3.9 to Figure 3.16
Read data setup time 1	t_{RDS1}	1/2t_{cyc}+ 5	—	ns	Figure 3.9 to Figure 3.15
Read data setup time 2	t_{RDS2}	7	—	ns	Figure 3.17 to Figure 3.20, Figure 3.25 to Figure 3.27
Read data setup time 3	t_{RDS3}	1/2t_{cyc} + 5	—	ns	Figure 3.16
Read data hold time 1	t_{RDH1}	0	—	ns	Figure 3.9 to Figure 3.15
Read data hold time 2	t_{RDH2}	2	—	ns	Figure 3.17 to Figure 3.20, Figure 3.25 to Figure 3.27
Read data hold time 3	t_{RDH3}	0	—	ns	Figure 3.16
Write enable delay time 1	t_{WED1}	1/2t_{cyc}	1/2t_{cyc} + 12	ns	Figure 3.9 to Figure 3.14
Write enable delay time 2	t_{WED2}	—	12	ns	Figure 3.15
Write data delay time 1	t_{WDD1}	—	12	ns	Figure 3.9 to Figure 3.15
Write data delay time 2	t_{WDD2}	—	12	ns	Figure 3.21 to Figure 3.24, Figure 3.28 to Figure 3.30
Write data hold time 1	t_{WDH1}	1	—	ns	Figure 3.9 to Figure 3.15
Write data hold time 2	t_{WDH2}	2	—	ns	Figure 3.21 to Figure 3.24, Figure 3.28 to Figure 3.30
Write data hold time 4	t_{WDH4}	0	—	ns	Figure 3.9 to Figure 3.13
$\overline{WAIT}$ setup time	t_{WTS}	1/2t_{cyc} + 4.5	—	ns	Figure 3.10 to Figure 3.16
$\overline{WAIT}$ hold time	t_{WTH}	1/2t_{cyc} + 3.5	—	ns	Figure 3.10 to Figure 3.16
$\overline{RAS}$ delay time 1	t_{RASD1}	2	12	ns	Figure 3.17 to Figure 3.33
$\overline{CAS}$ delay time 1	t_{CASD1}	2	12	ns	Figure 3.17 to Figure 3.33
DQM delay time 1	t_{DQMD1}	2	12	ns	Figure 3.17 to Figure 3.30
CKE delay time 1	t_{CKED1}	2	12	ns	Figure 3.32
$\overline{AH}$ delay time	t_{AHD}	1/2t_{cyc}	1/2t_{cyc} + 12	ns	Figure 3.13
Multiplexed address delay time	t_{MAD}	—	12	ns	Figure 3.13
Multiplexed address hold time	t_{MAH}	1	—	ns	Figure 3.13
Address setup time for $\overline{AH}$	t_{AVVH}	1/2t_{cyc} – 2	—	ns	Figure 3.13
DACK, TEND delay time	t_{DACD}	Refer to the direct memory access controller timing		ns	Figure 3.9 to Figure 3.30

Note 1. The maximum value (fmax) of CKIO (external bus clock) depends on the number of wait cycles and the system configuration of your board.
Note 2. 1/2 t_{cyc} indicated in minimum and maximum values for the item of delay, setup, and hold times represents a half cycle from the rising edge with a clock. That is, 1/2 t_{cyc} describes a reference of the falling edge with a clock.
Note 3. Values when SDRAM is used.



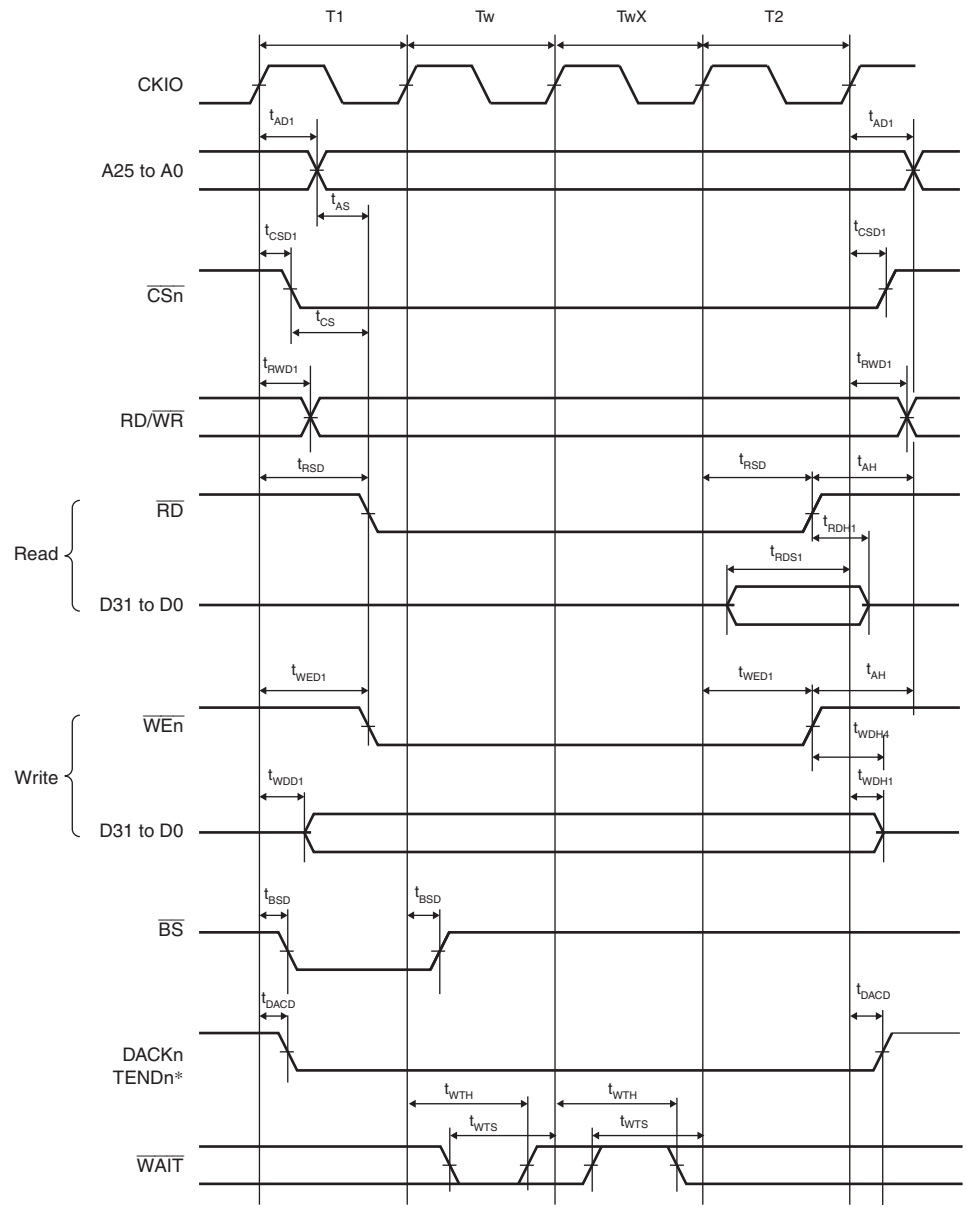
Note: * The waveform for DACKn and TENDn is when active low is specified.

Figure 3.9 Basic Bus Timing for Normal Space (No Wait)



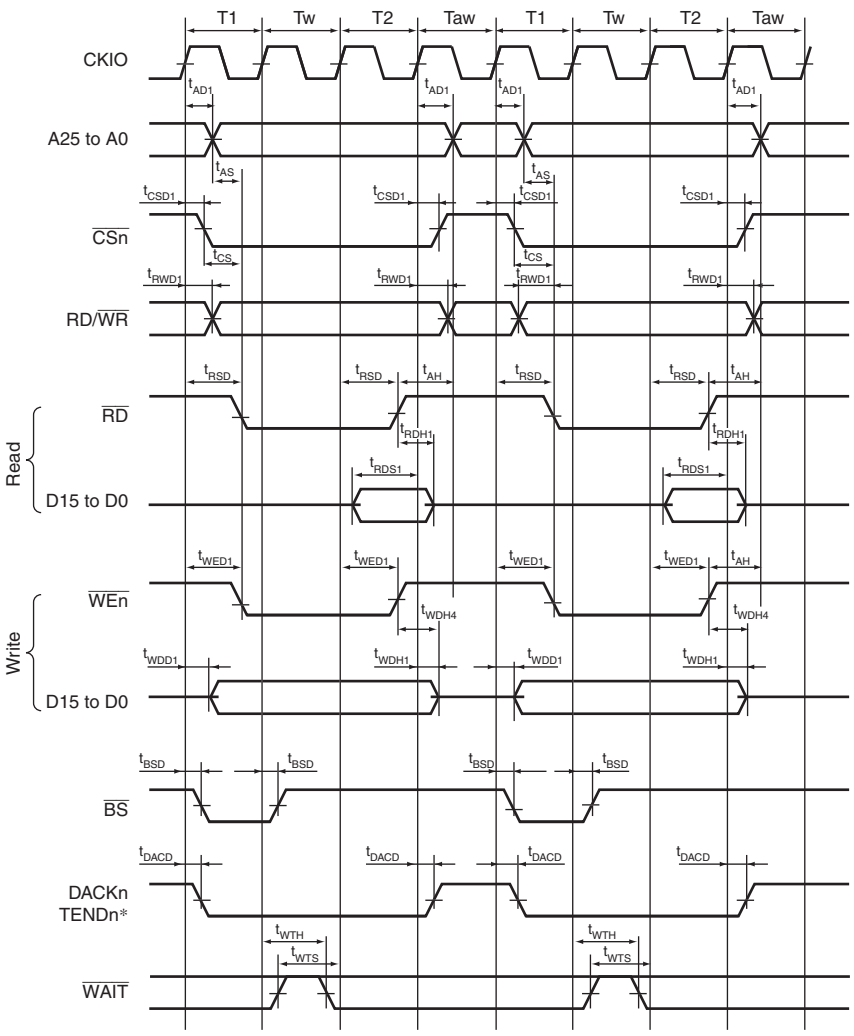
Note: * The waveform for DACKn and TENDn is when active low is specified.

Figure 3.10 Basic Bus Timing for Normal Space (One Software Wait Cycle)



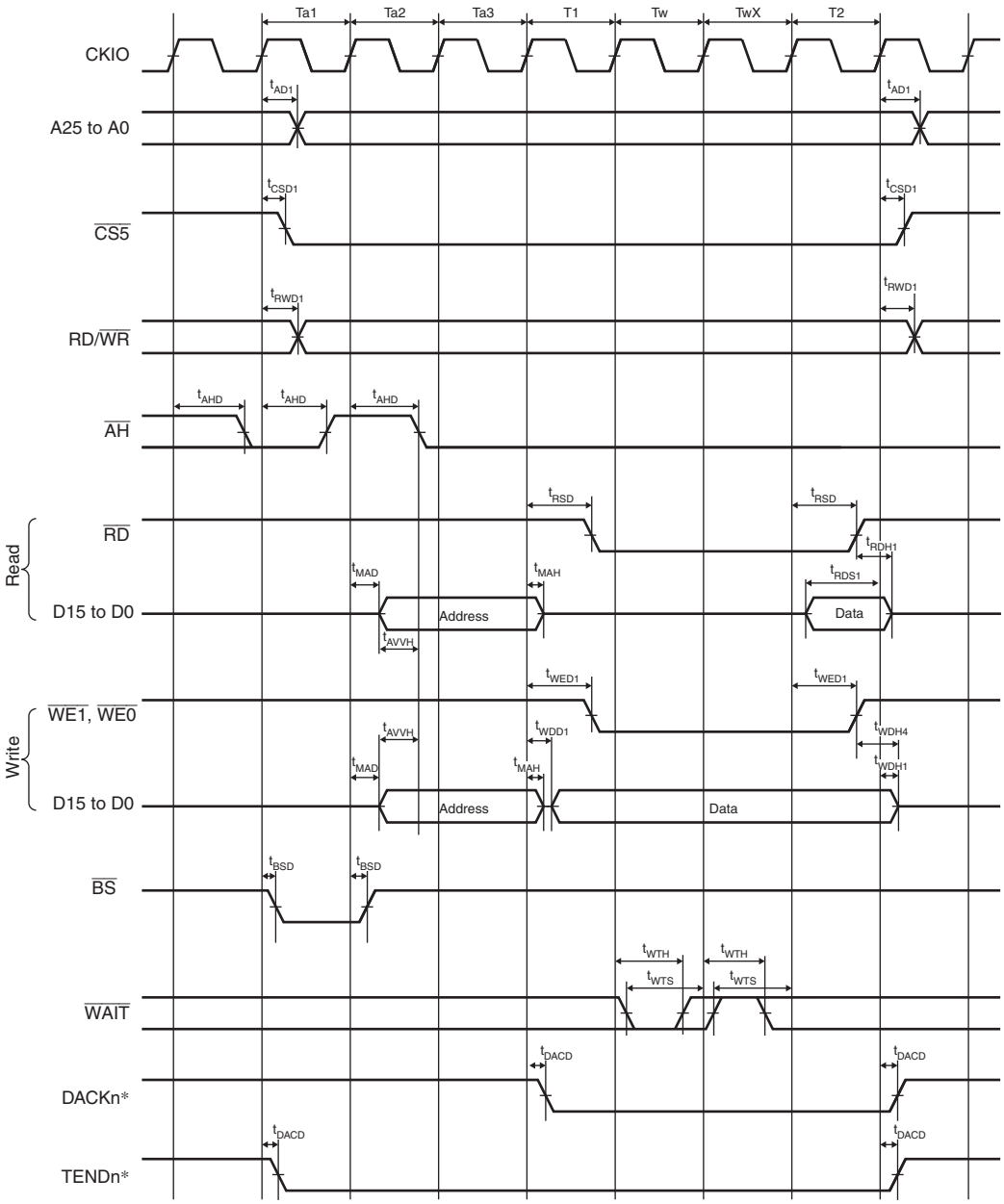
Note: * The waveform for DACKn and TENDn is when active low is specified.

Figure 3.11 Basic Bus Timing for Normal Space (One Software Wait Cycle, One External Wait Cycle)



Note: * The waveform for DACKn and TENDn is when active low is specified.

Figure 3.12 Basic Bus Timing for Normal Space (One Software Wait Cycle, External Wait Cycle Valid (WM Bit = 0), No Idle Cycle)



Note: * The waveform for DACKn and TENDn is when active low is specified.

Figure 3.13 MPX-I/O Interface Bus Cycle (Three Address Cycles, One Software Wait Cycle, One External Wait Cycle)

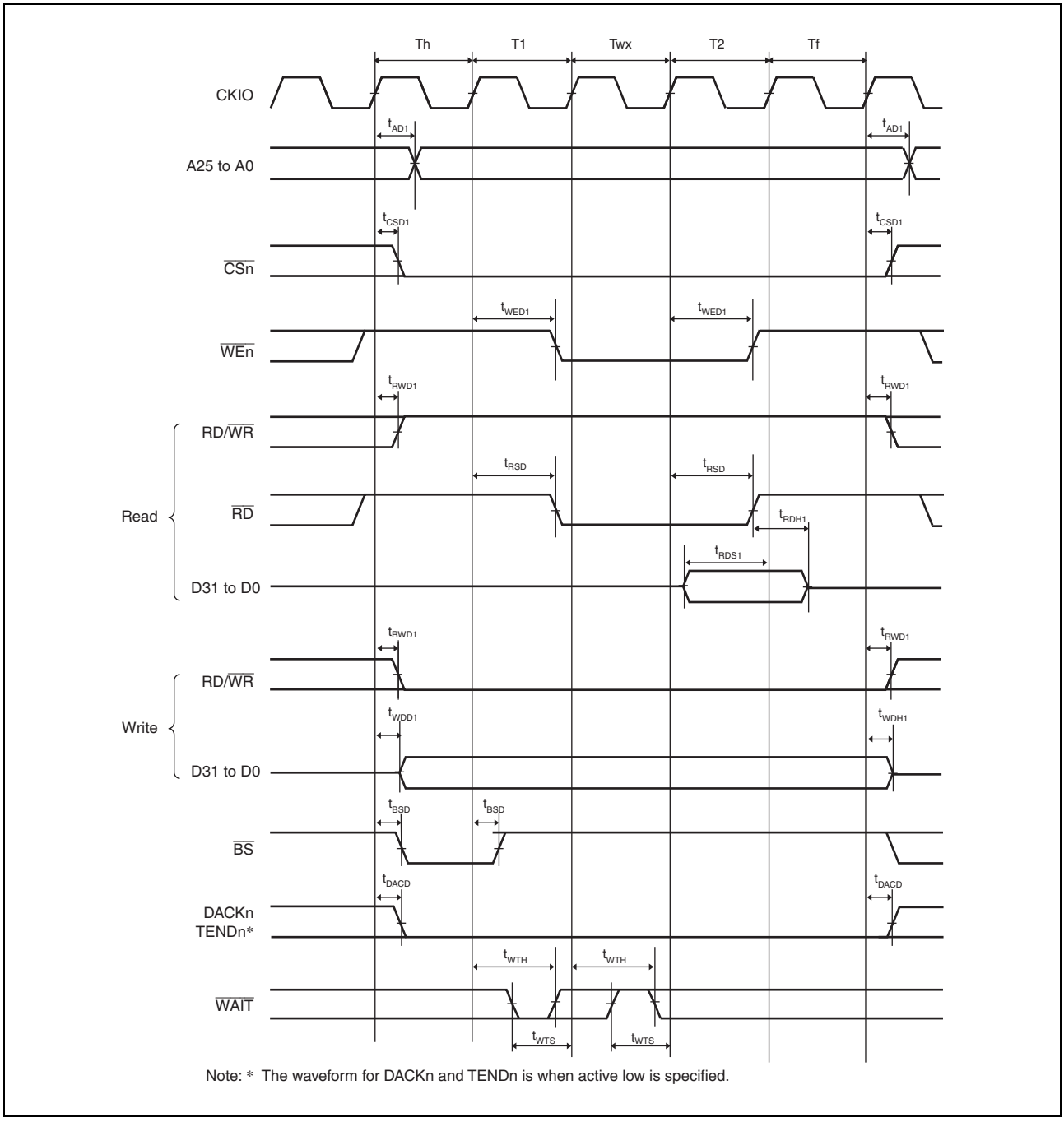


Figure 3.14 Bus Cycle of SRAM with Byte Selection (SW = 1 Cycle, HW = 1 Cycle, One Asynchronous External Wait Cycle, BAS = 0 (Write Cycle $\overline{UB}$/$\overline{LB}$ Control))

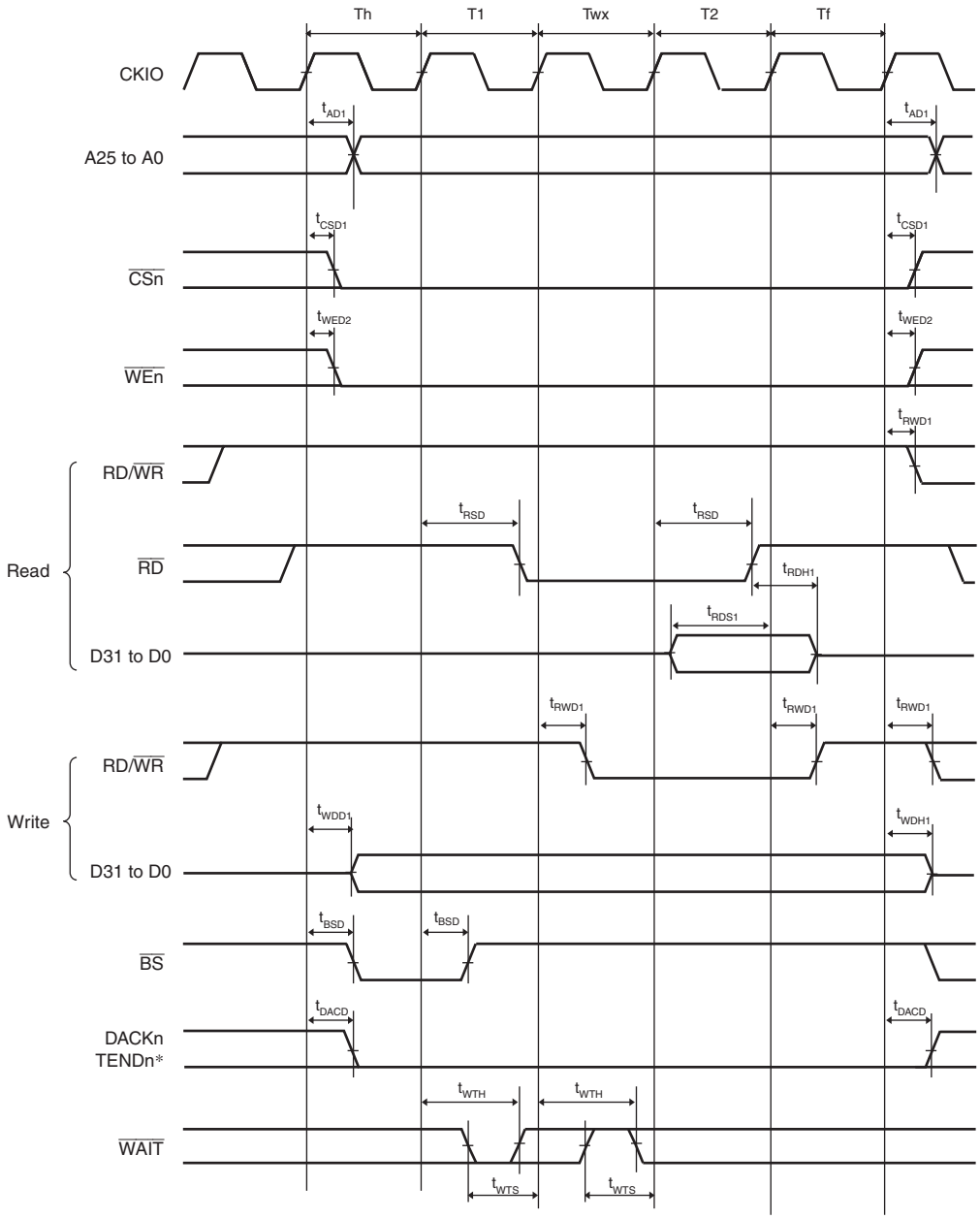
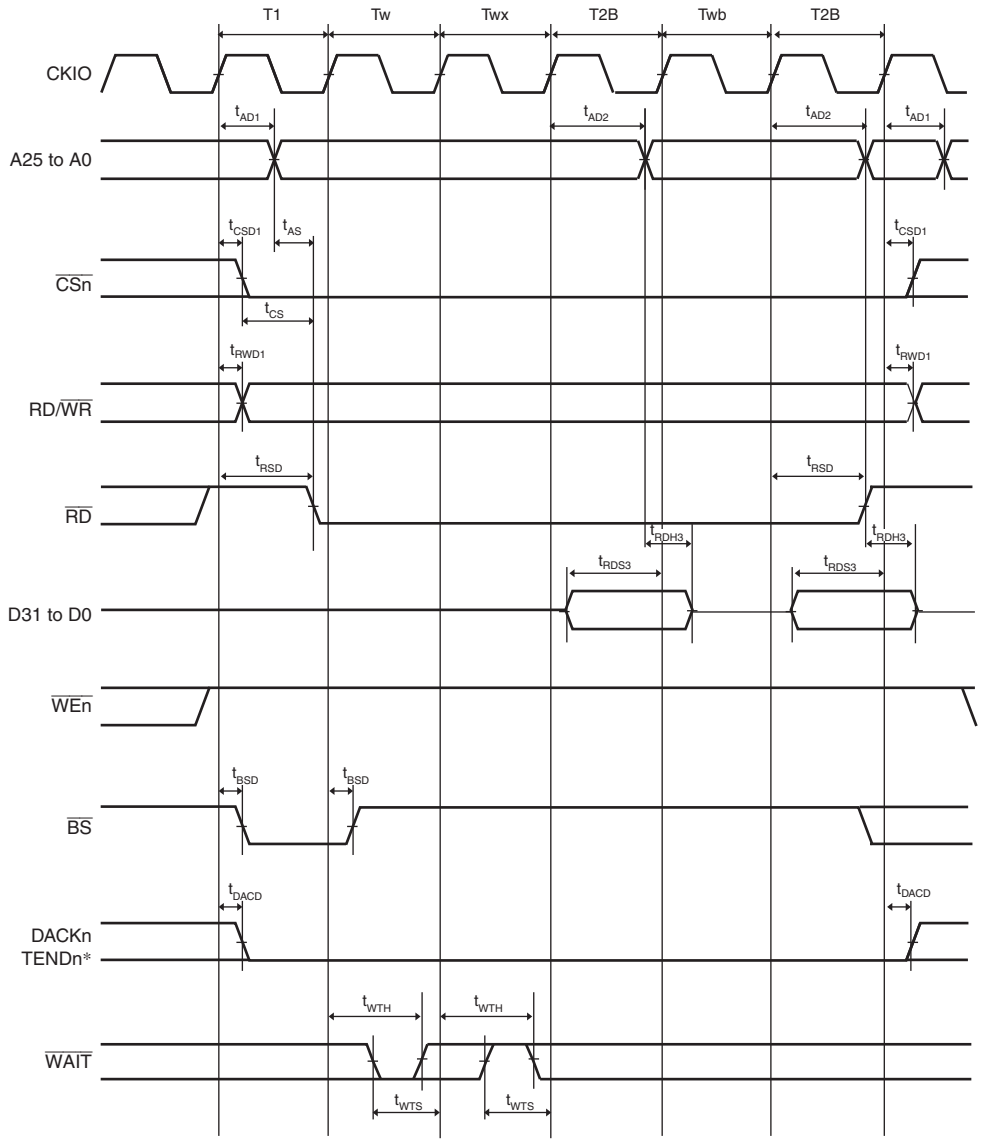
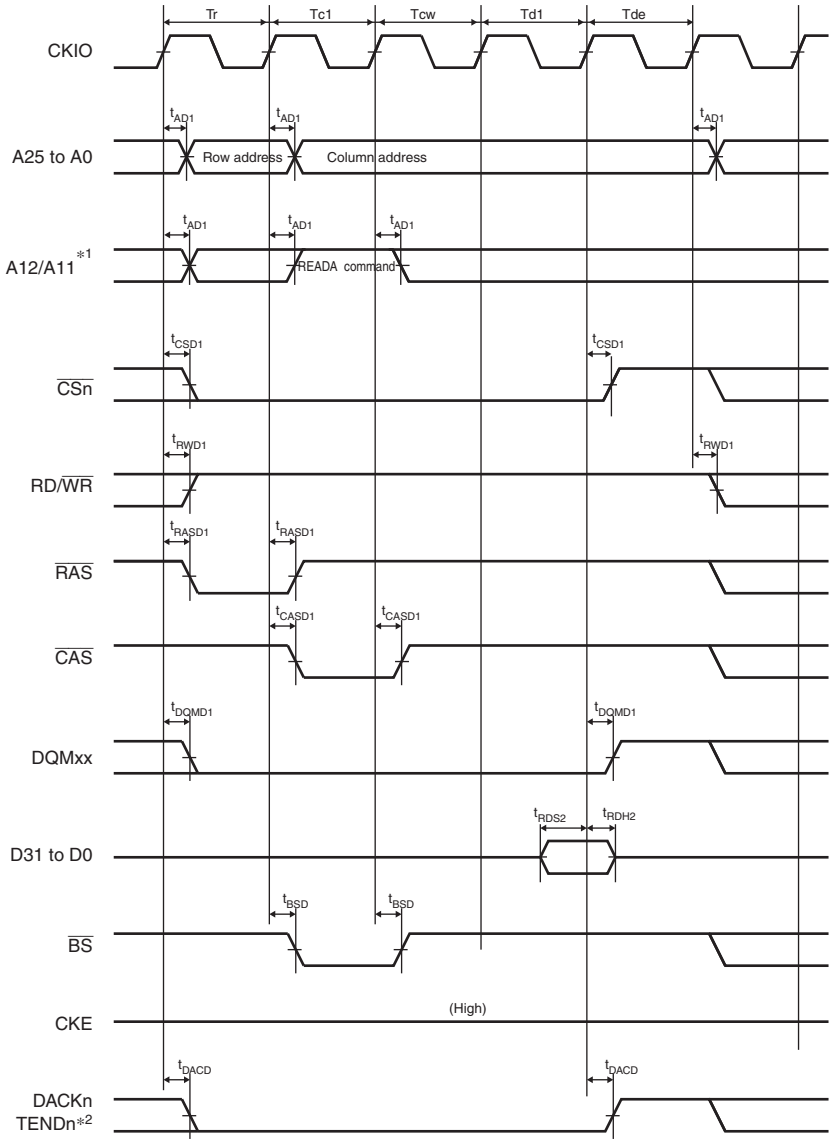


Figure 3.15 Bus Cycle of SRAM with Byte Selection (SW = 1 Cycle, HW = 1 Cycle, One Asynchronous External Wait Cycle, BAS = 1 (Write Cycle $\overline{WE}$ Control))



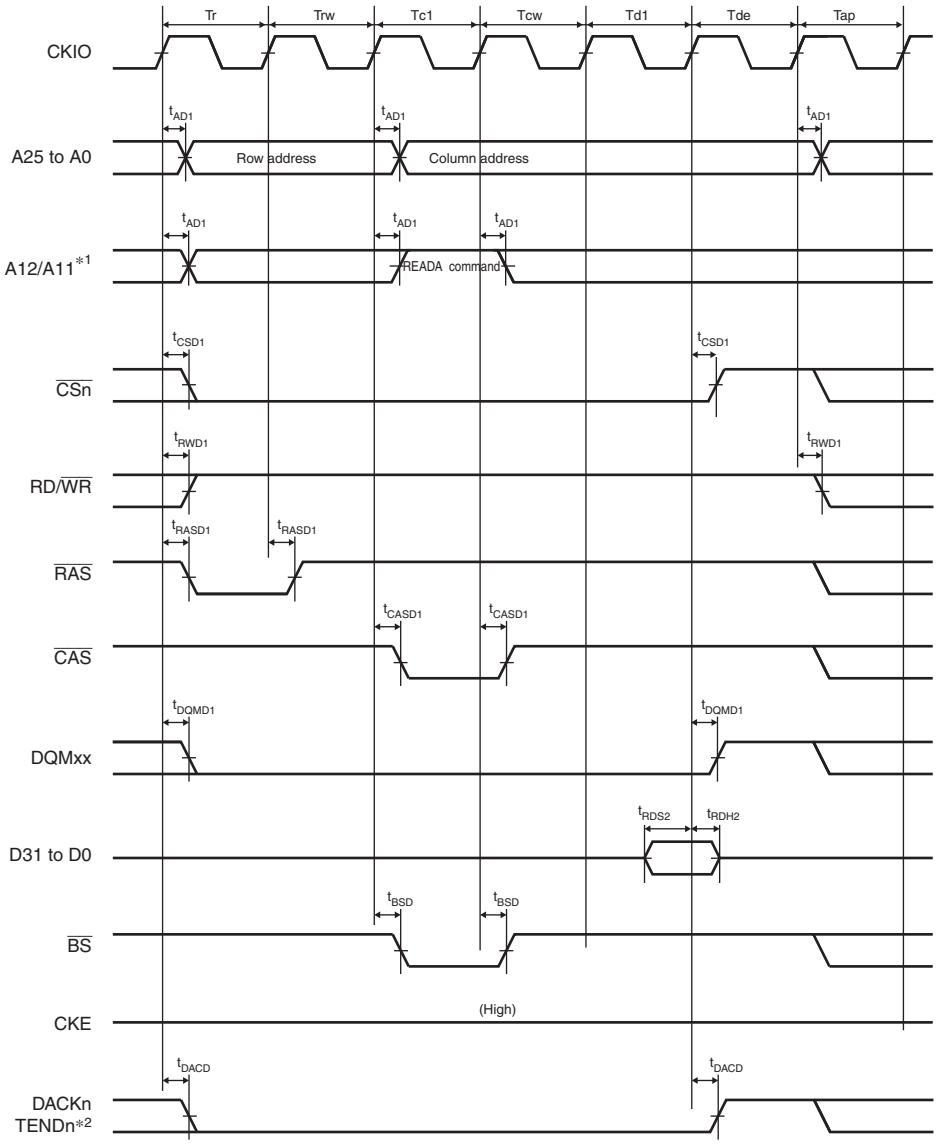
Note: * The waveform for DACKn and TENDn is when active low is specified.

Figure 3.16 Burst ROM Read Cycle (One Software Wait Cycle, One Asynchronous External Burst Wait Cycle, Two Burst)



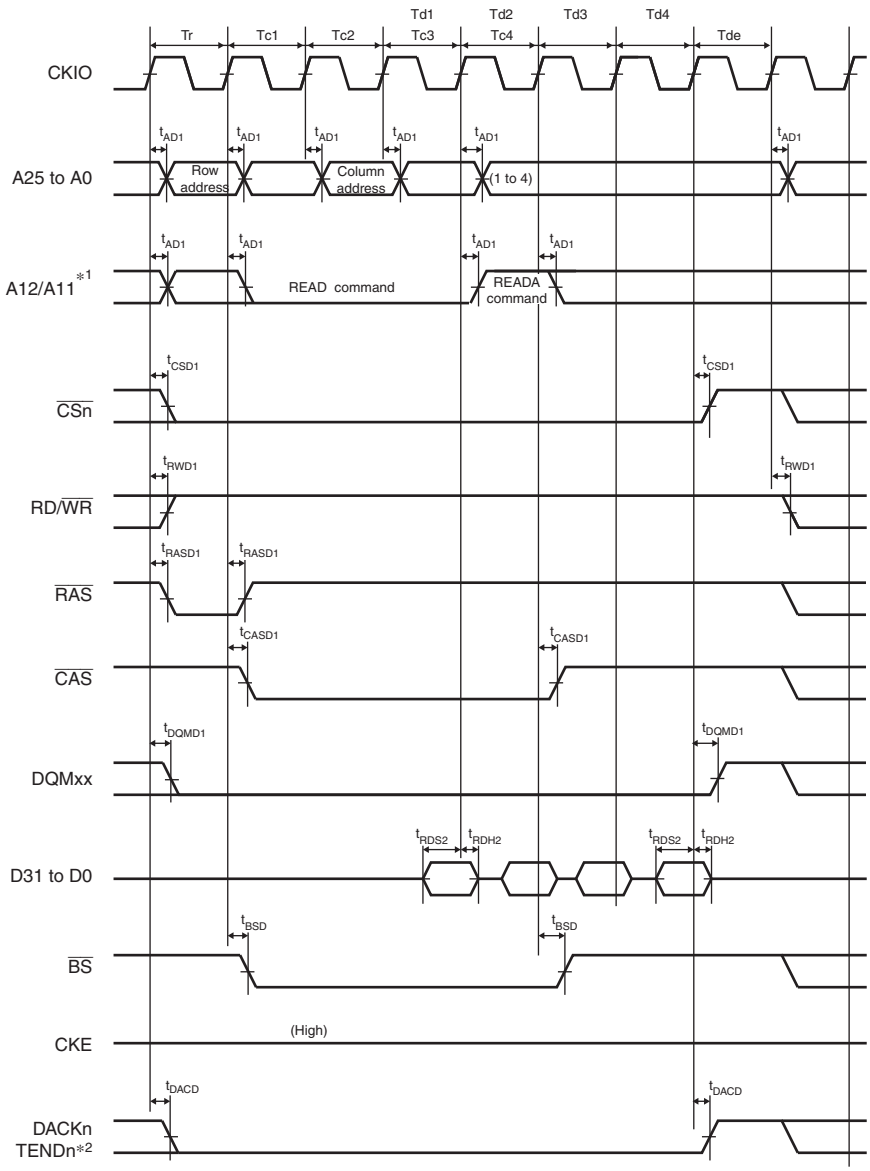
Notes: 1. An address pin to be connected to pin A10 of SDRAM.
2. The waveform for DACKn and TENDn is when active low is specified.

Figure 3.17 Synchronous DRAM Single Read Bus Cycle (Auto Precharge, CAS Latency 2, WTRCD = 0 Cycle, WTRP = 0 Cycle)



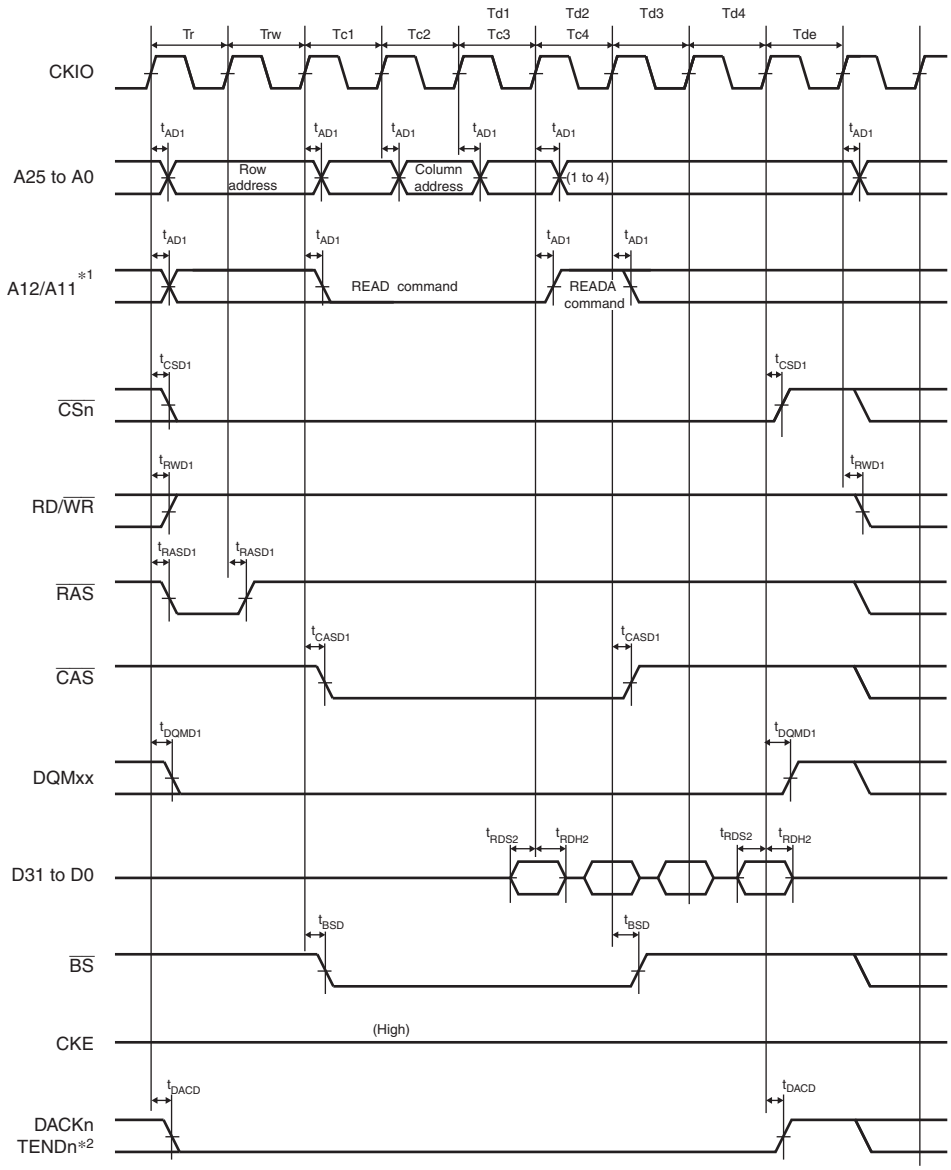
Notes: 1. An address pin to be connected to pin A10 of SDRAM.
2. The waveform for DACKn and TENDn is when active low is specified.

Figure 3.18 Synchronous DRAM Single Read Bus Cycle (Auto Precharge, CAS Latency 2, WTRCD = 1 Cycle, WTRP = 1 Cycle)



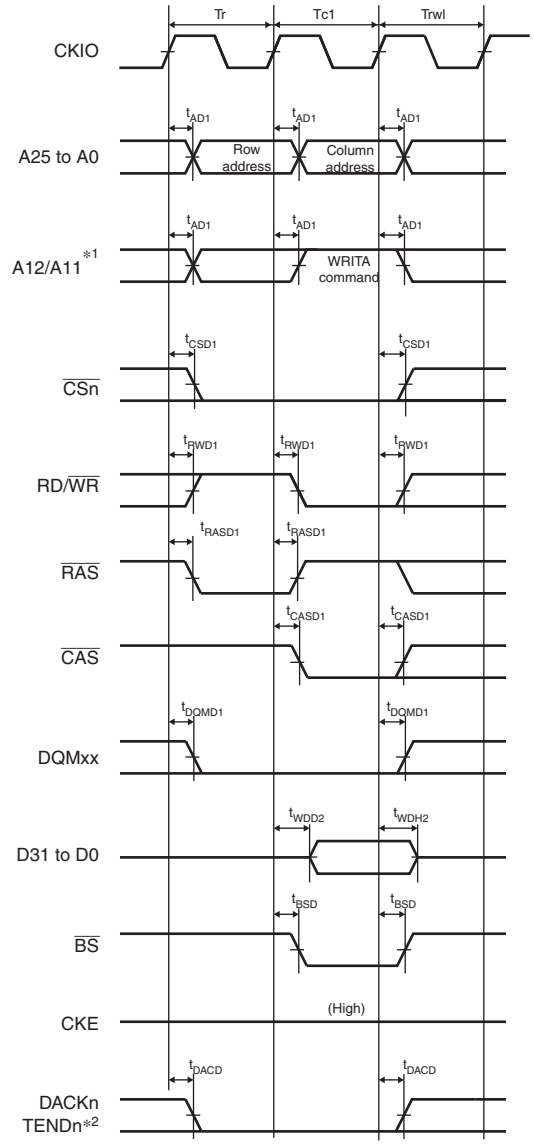
Notes: 1. An address pin to be connected to pin A10 of SDRAM.
2. The waveform for DACKn and TENDn is when active low is specified.

Figure 3.19 Synchronous DRAM Burst Read Bus Cycle (Four Read Cycles) (Auto Precharge, CAS Latency 2, WTRCD = 0 Cycle, WTRP = 1 Cycle)



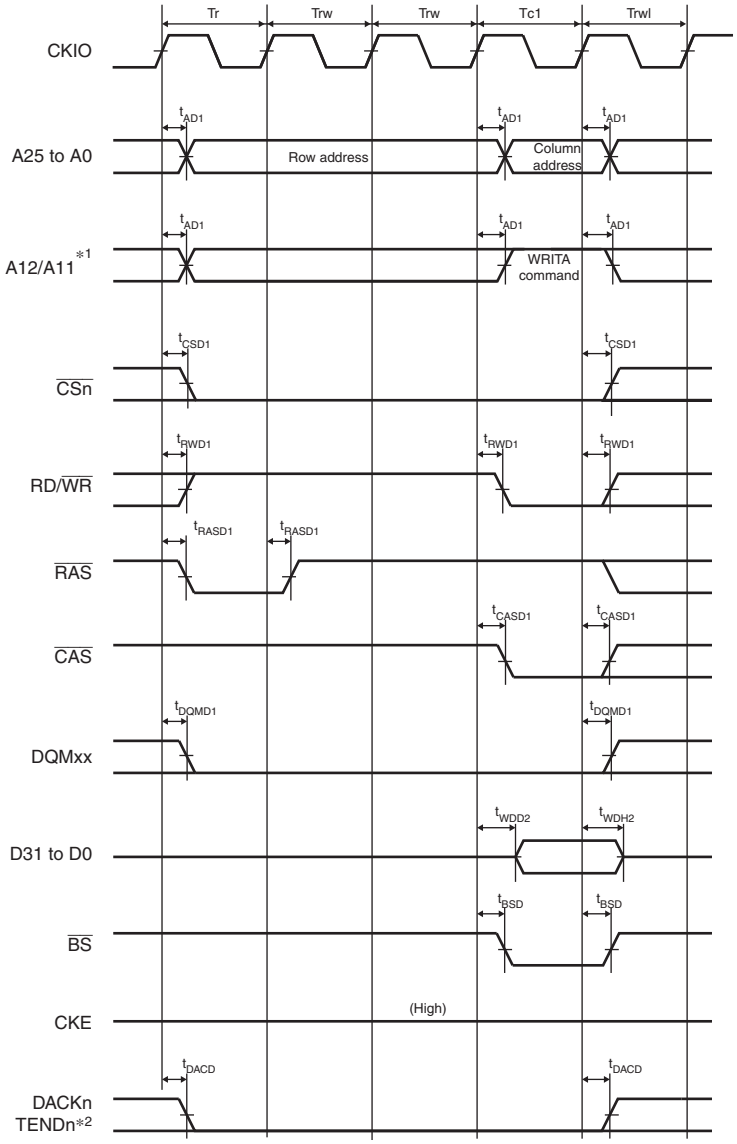
Notes: 1. An address pin to be connected to pin A10 of SDRAM.
2. The waveform for DACKn and TENDn is when active low is specified.

Figure 3.20 Synchronous DRAM Burst Read Bus Cycle (Four Read Cycles) (Auto Precharge, CAS Latency 2, WTRCD = 1 Cycle, WTRP = 0 Cycle)



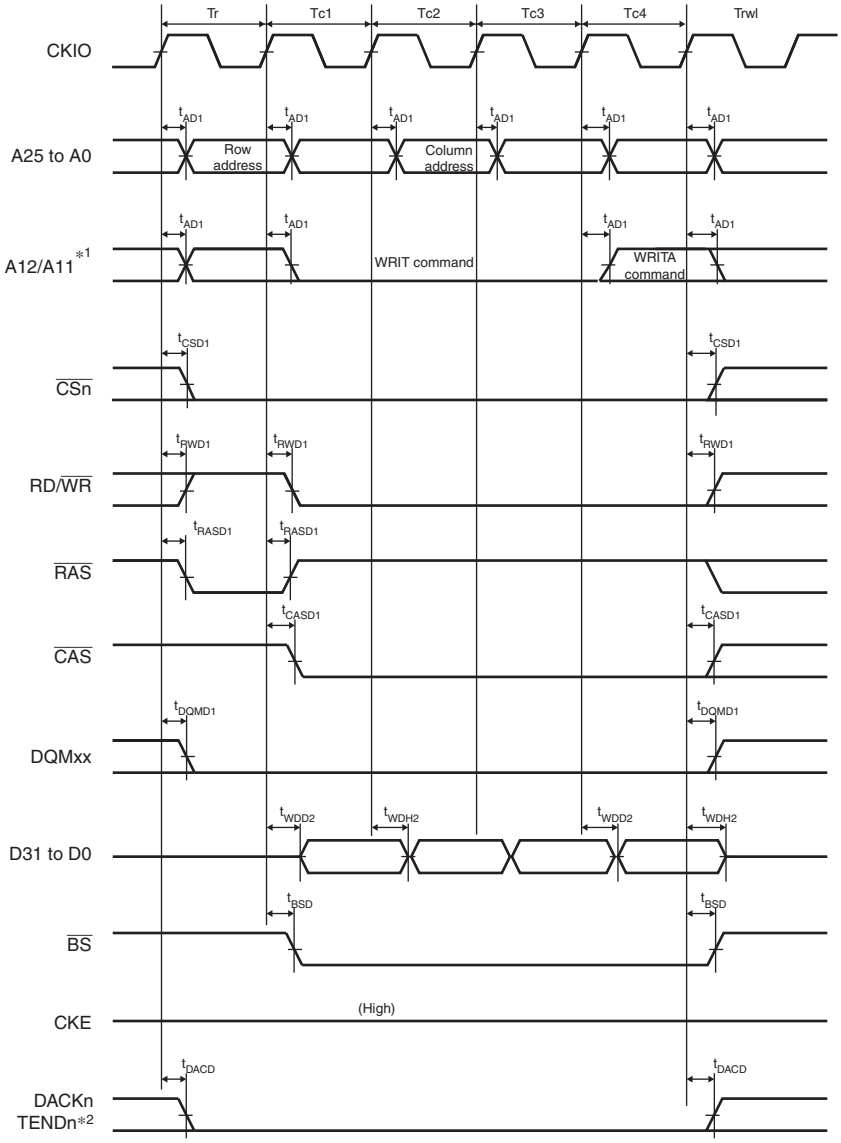
Notes: 1. An address pin to be connected to pin A10 of SDRAM.
2. The waveform for DACKn and TENDn is when active low is specified.

Figure 3.21 Synchronous DRAM Single Write Bus Cycle (Auto Precharge, TRWL = 1 Cycle)



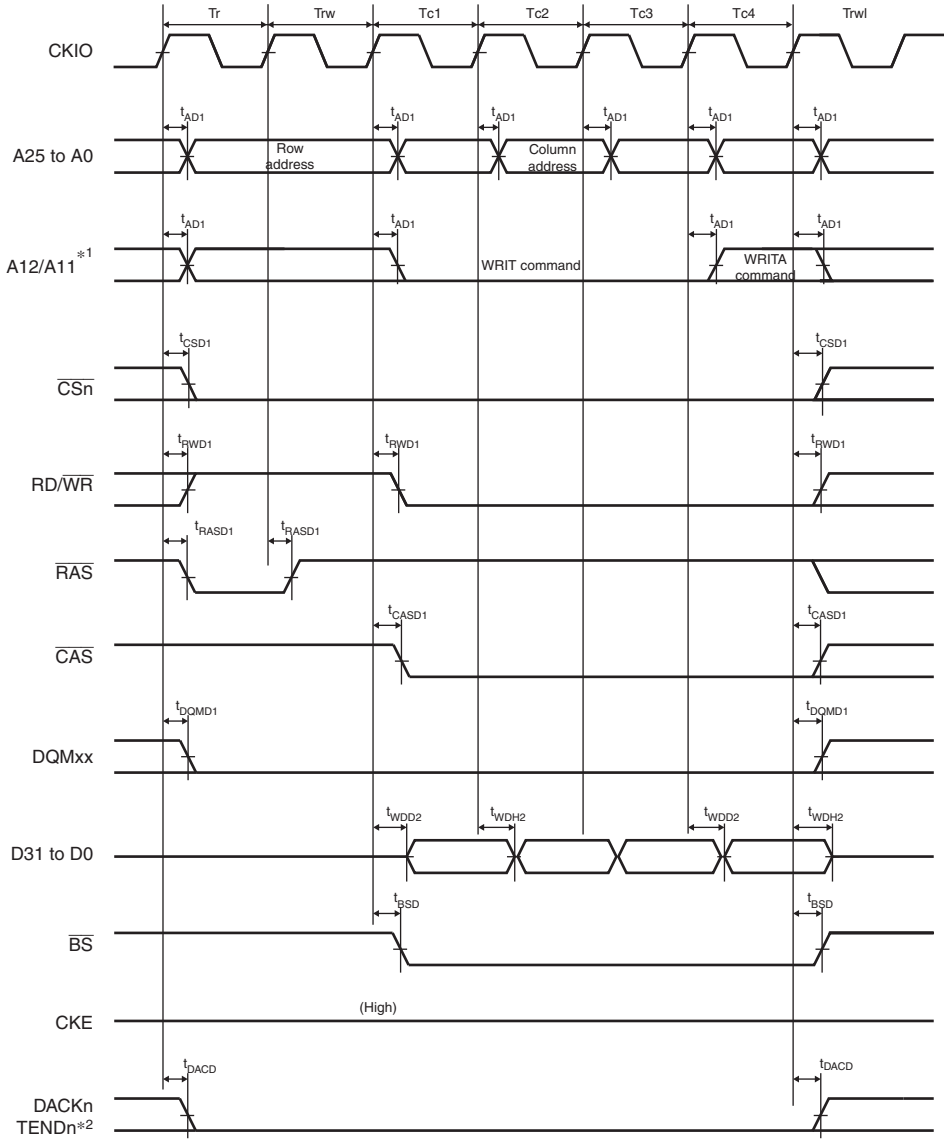
Notes: 1. An address pin to be connected to pin A10 of SDRAM.
2. The waveform for DACKn and TENDn is when active low is specified.

Figure 3.22 Synchronous DRAM Single Write Bus Cycle (Auto Precharge, WTRCD = 2 Cycles, TRWL = 1 Cycle)



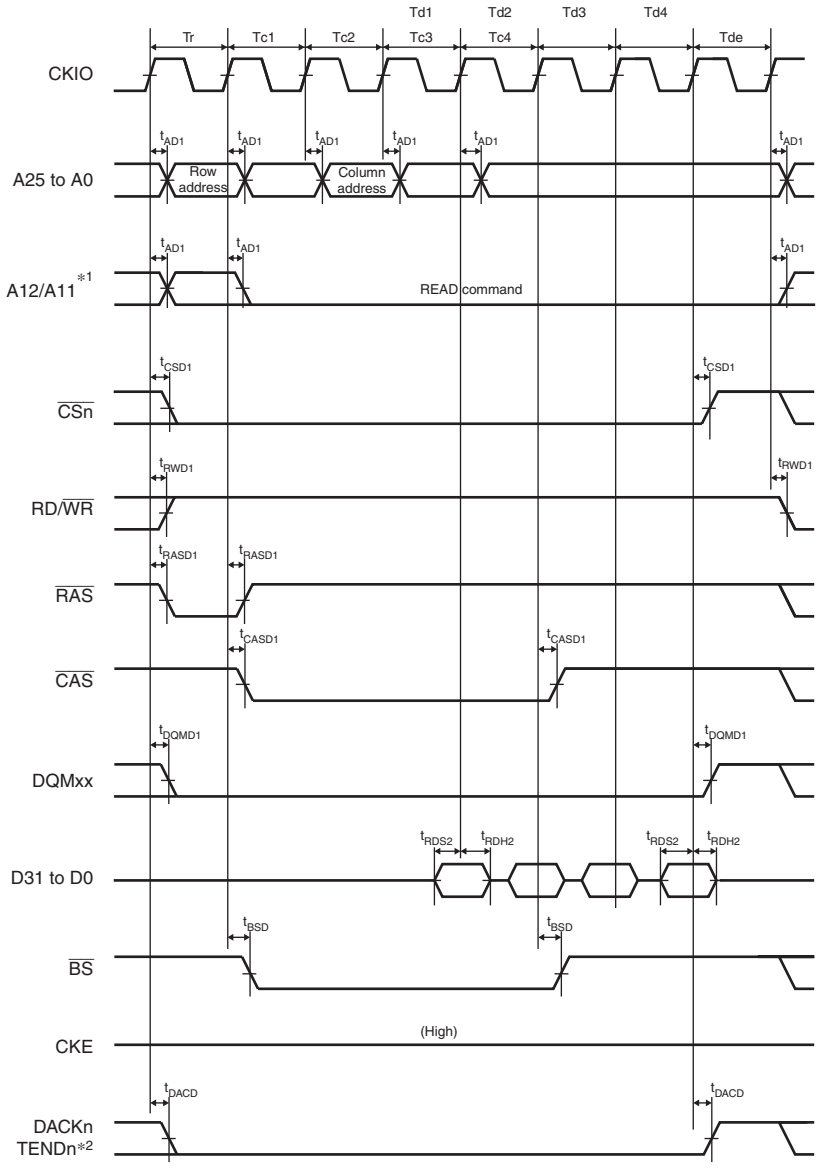
Notes: 1. An address pin to be connected to pin A10 of SDRAM.
2. The waveform for DACKn and TENDn is when active low is specified.

Figure 3.23 Synchronous DRAM Burst Write Bus Cycle (Four Write Cycles) (Auto Precharge, WTRCD = 0 Cycle, TRWL = 1 Cycle)



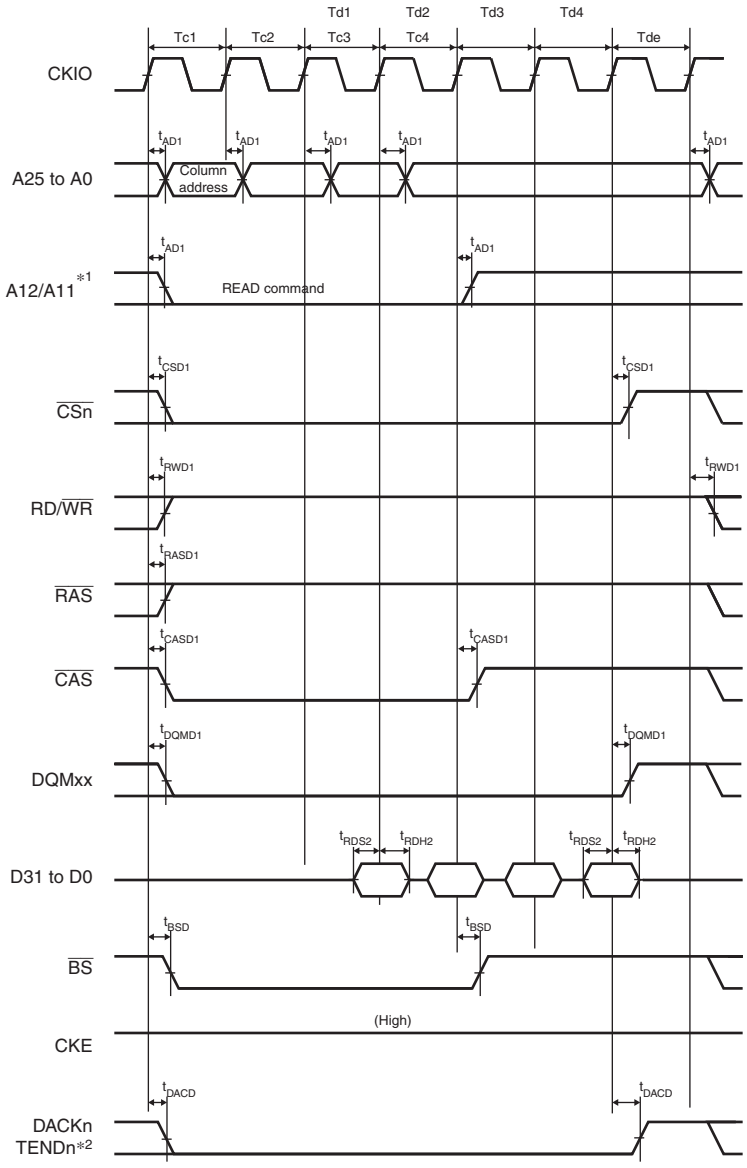
Notes: 1. An address pin to be connected to pin A10 of SDRAM.
2. The waveform for DACKn and TENDn is when active low is specified.

Figure 3.24 Synchronous DRAM Burst Write Bus Cycle (Four Write Cycles) (Auto Precharge, WTRCD = 1 Cycle, TRWL = 1 Cycle)



Notes: 1. An address pin to be connected to pin A10 of SDRAM.
2. The waveform for DACKn and TENDn is when active low is specified.

Figure 3.25 Synchronous DRAM Burst Read Bus Cycle (Four Read Cycles) (Bank Active Mode: ACT + READ Commands, CAS Latency 2, WTRCD = 0 Cycle)



Notes: 1. An address pin to be connected to pin A10 of SDRAM.
2. The waveform for DACKn and TENDn is when active low is specified.

Figure 3.26 Synchronous DRAM Burst Read Bus Cycle (Four Read Cycles) (Bank Active Mode: READ Command, Same Row Address, CAS Latency 2, WTRCD = 0 Cycle)

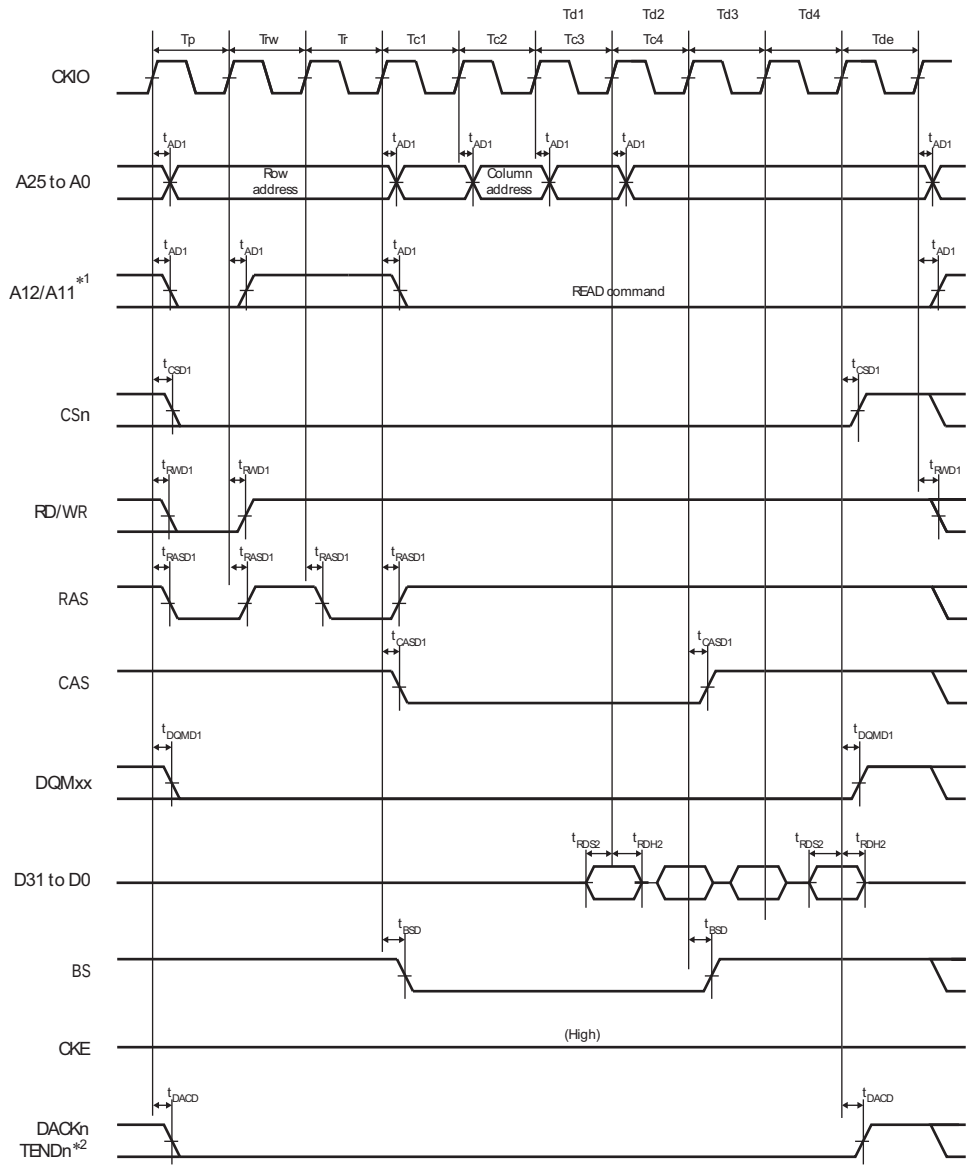
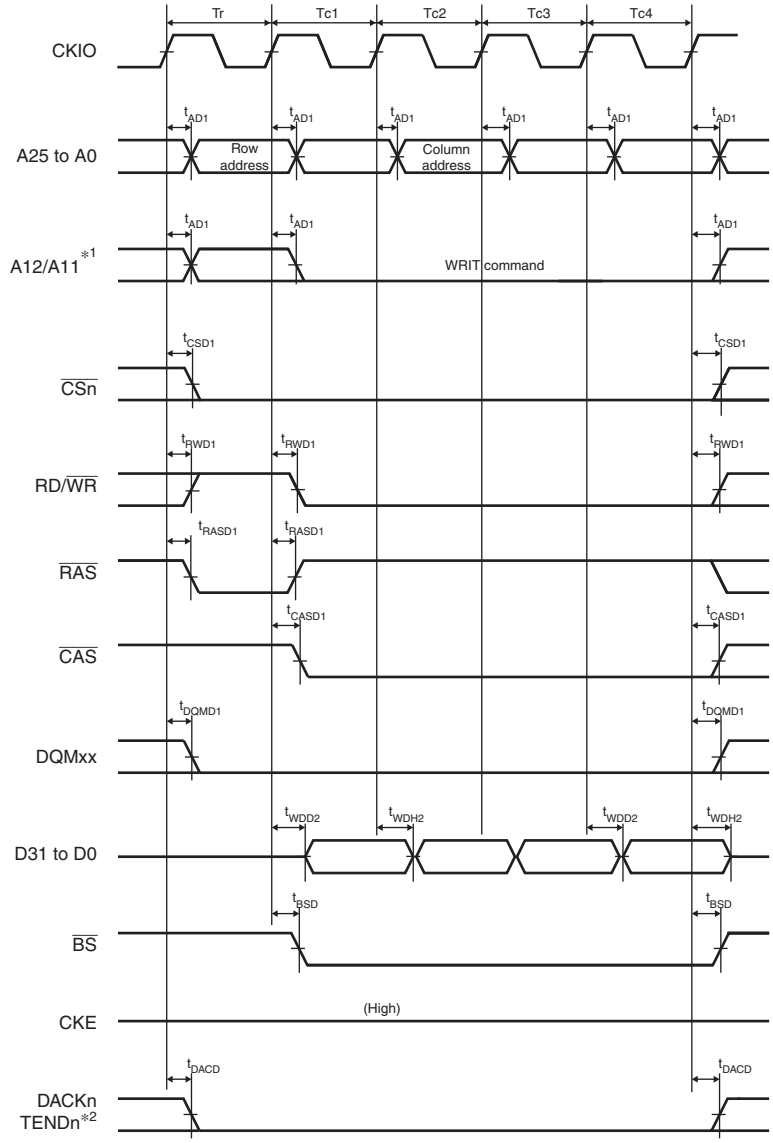
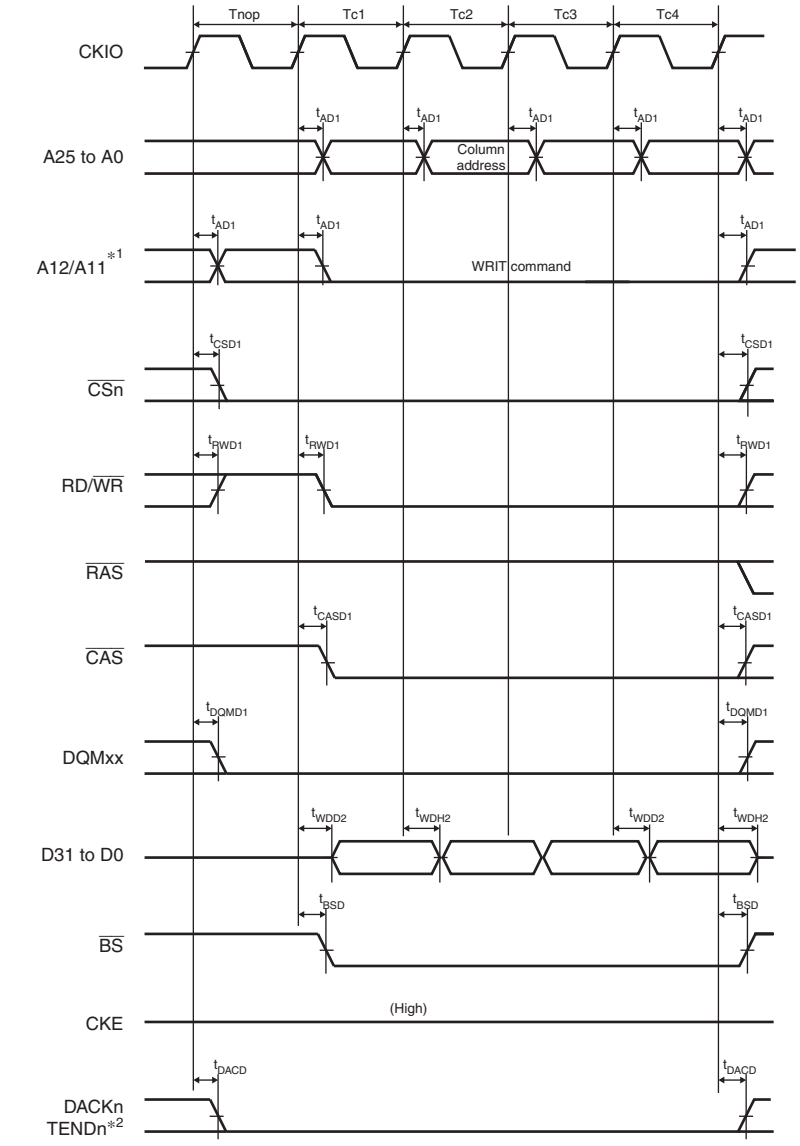


Figure 3.27 Synchronous DRAM Burst Read Bus Cycle (Four Read Cycles) (Bank Active Mode: PRE + ACT + READ Commands, Different Row Addresses, CAS Latency 2, WTRCD = 0 Cycle)



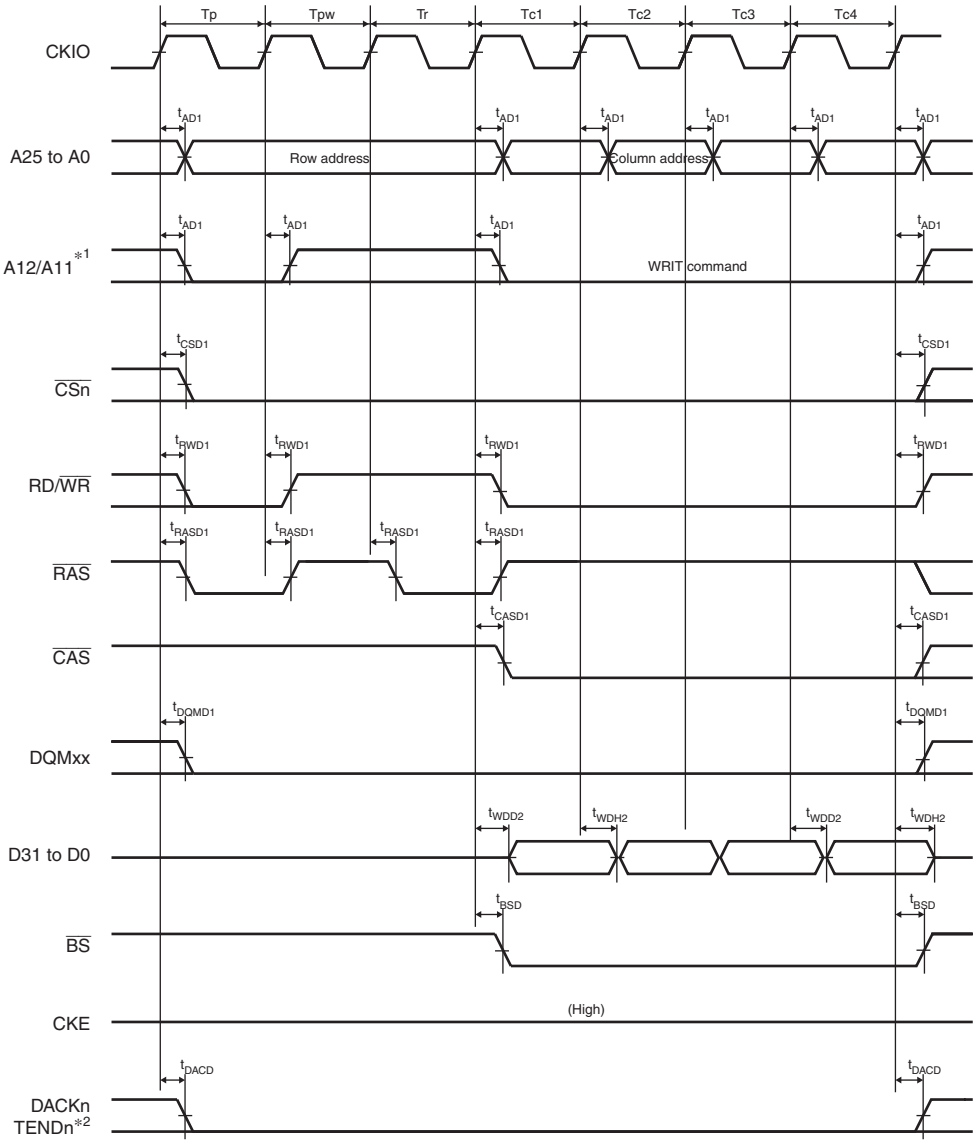
Notes: 1. An address pin to be connected to pin A10 of SDRAM.
2. The waveform for DACKn and TENDn is when active low is specified.

Figure 3.28 Synchronous DRAM Burst Write Bus Cycle (Four Write Cycles) (Bank Active Mode: ACT + WRITE Commands, WTRCD = 0 Cycle, TRWL = 0 Cycle)



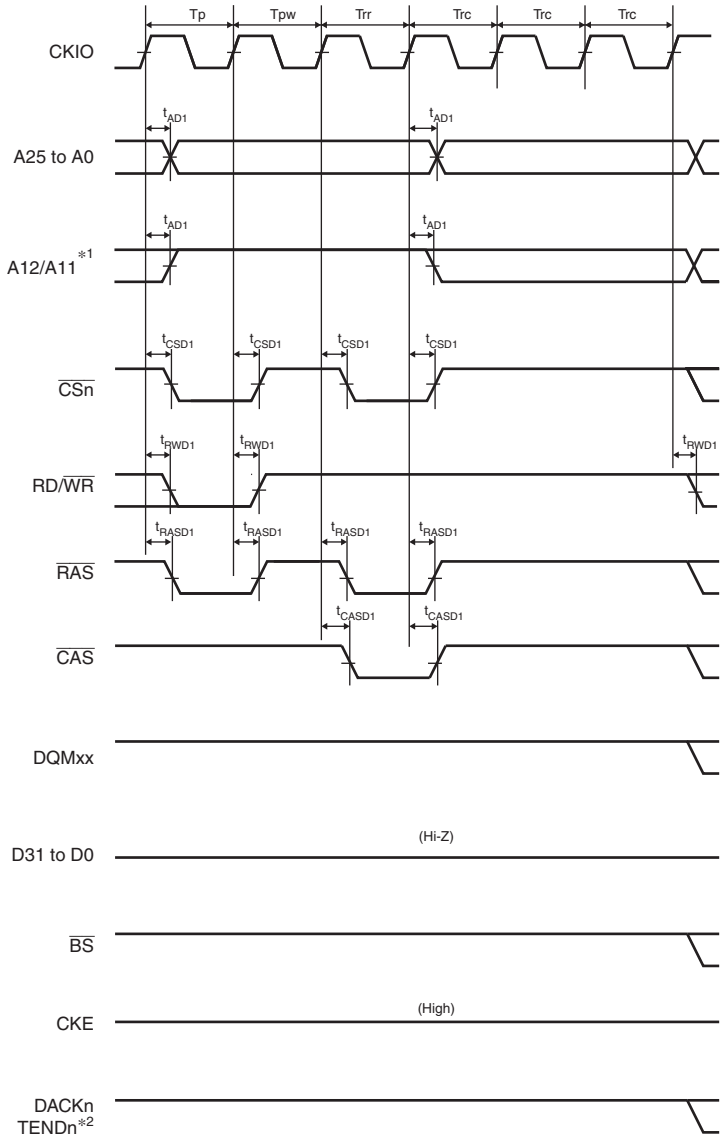
Notes: 1. An address pin to be connected to pin A10 of SDRAM.
2. The waveform for DACKn and TENDn is when active low is specified.

Figure 3.29 Synchronous DRAM Burst Write Bus Cycle (Four Write Cycles) (Bank Active Mode: WRITE Command, Same Row Address, WTRCD = 0 Cycle, TRWL = 0 Cycle)



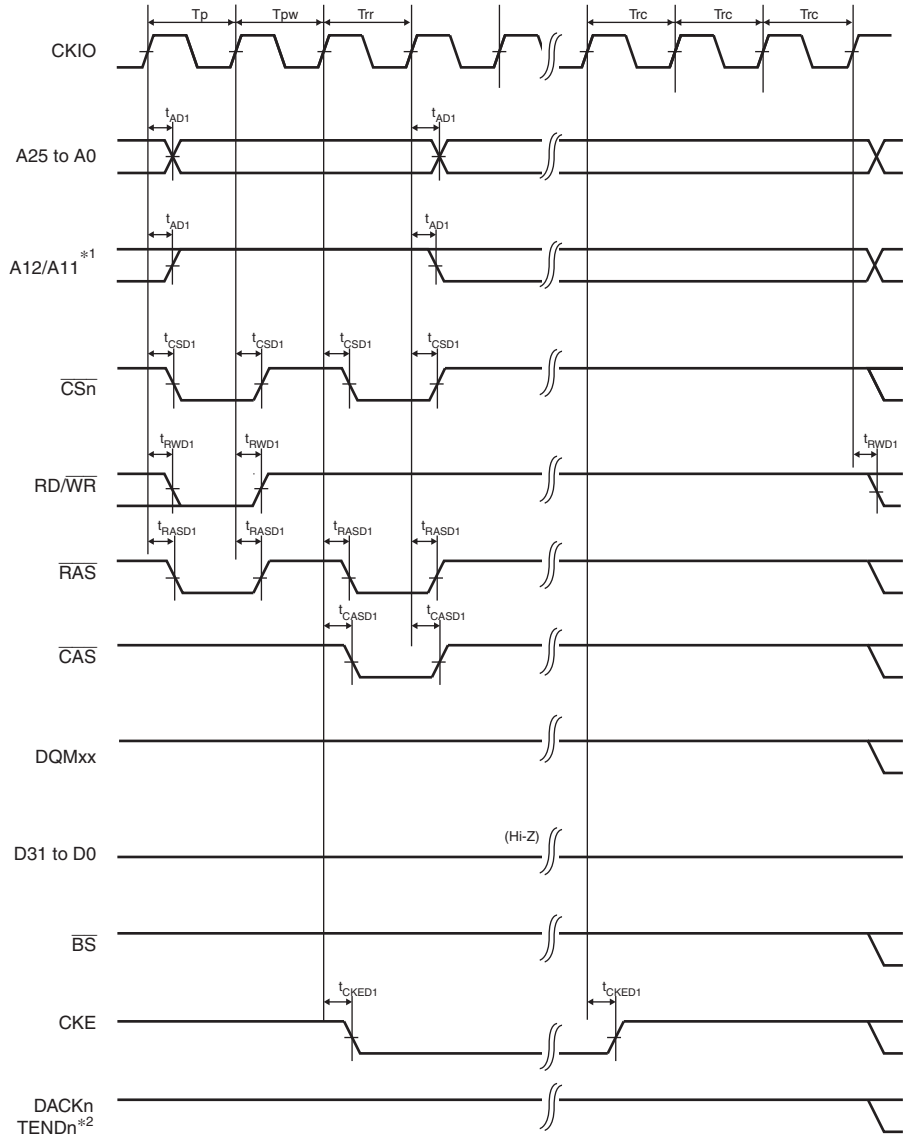
Notes: 1. An address pin to be connected to pin A10 of SDRAM.
2. The waveform for DACKn and TENDn is when active low is specified.

Figure 3.30 Synchronous DRAM Burst Write Bus Cycle (Four Write Cycles) (Bank Active Mode: PRE + ACT + WRITE Commands, Different Row Addresses, WTRCD = 0 Cycle, TRWL = 0 Cycle)



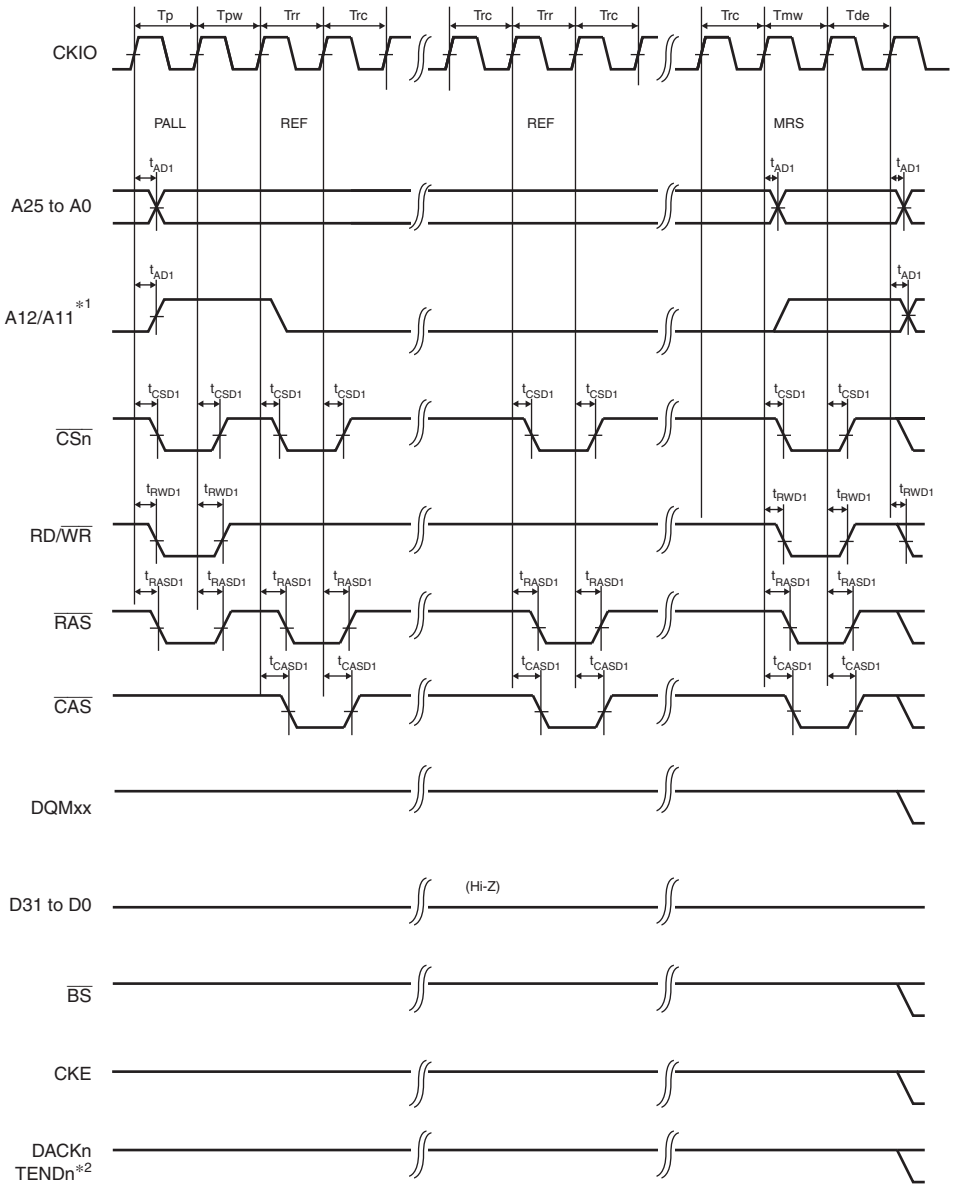
Notes: 1. An address pin to be connected to pin A10 of SDRAM.
2. The waveform for DACKn and TENDn is when active low is specified.

Figure 3.31 Synchronous DRAM Auto-Refreshing Timing (WTRP = 1 Cycle, WTRC = 3 Cycles)



Notes: 1. An address pin to be connected to pin A10 of SDRAM.
2. The waveform for DACKn and TENDn is when active low is specified.

Figure 3.32 Synchronous DRAM Self-Refreshing Timing (WTRP = 1 Cycle)



Notes: 1. An address pin to be connected to pin A10 of SDRAM.
2. The waveform for DACKn and TENDn is when active low is specified.

Figure 3.33 Synchronous DRAM Mode Register Write Timing (WTRP = 1 Cycle)

3.4.4 Direct Memory Access Controller Timing

Table 3.8 Direct Memory Access Controller Timing

Item	Symbol	Min.	Max.	Unit	Figure
DREQ setup time	t_{DRQS}	5.5	—	ns	Figure 3.34
DREQ hold time	t_{DRQH}	2.5	—		
DACK, TEND delay time	t_{DACD}	0	12		Figure 3.35

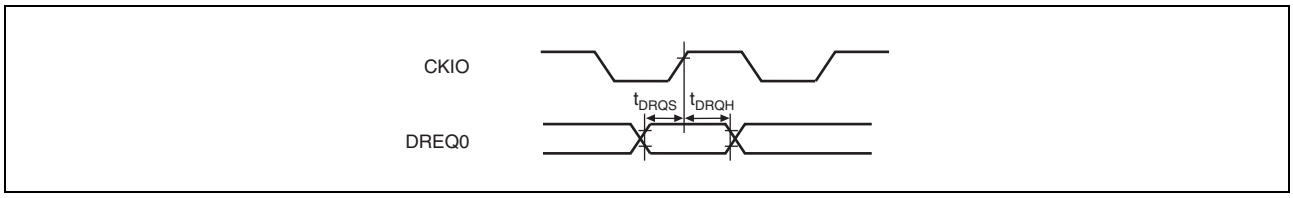


Figure 3.34 DREQ Input Timing

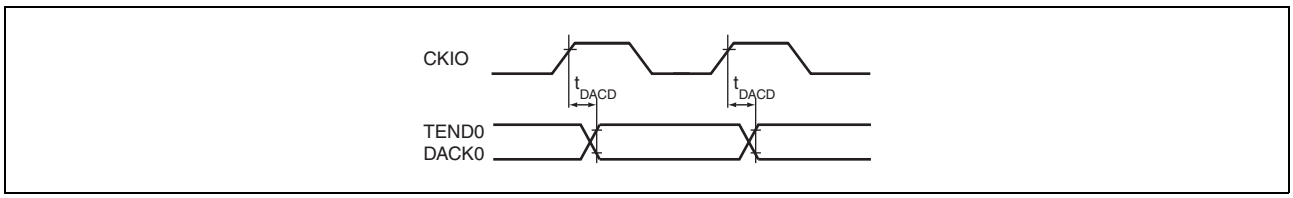


Figure 3.35 DACK, TEND Output Timing

3.4.5 Multi-Function Timer Pulse Unit 2 Timing

Table 3.9 Multi-Function Timer Pulse Unit 2 Timing

Item	Symbol	Min.	Max.	Unit	Figure
Timer clock pulse width (single edge)	$t_{TCKWH/L}$	1.5	—	t_{p0cyc}	Figure 3.36
Timer clock pulse width (both edges)	$t_{TCKWH/L}$	2.5	—	t_{p0cyc}	
Timer clock pulse width (phase counting mode)	$t_{TCKWH/L}$	2.5	—	t_{p0cyc}	

Note: t_{p0cyc} indicates peripheral clock (P0ϕ) cycle.

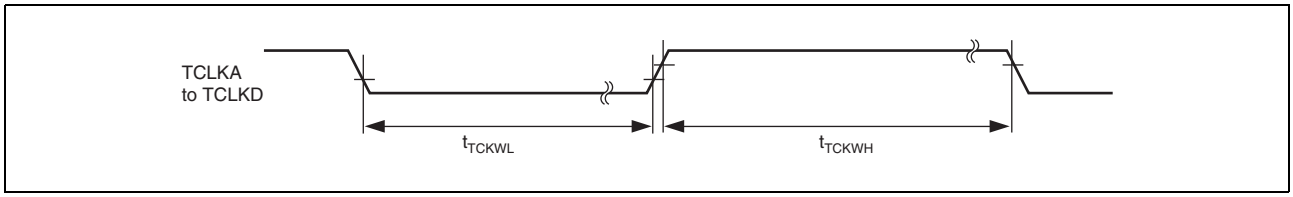


Figure 3.36 Clock Input Timing

3.4.6 Watchdog Timer Timing

Table 3.10 Watchdog Timer Timing

Item	Symbol	Min.	Max.	Unit	Figure
$\overline{\text{WDTOVF}}$ delay time	t_{WOVD}	—	100	ns	Figure 3.37

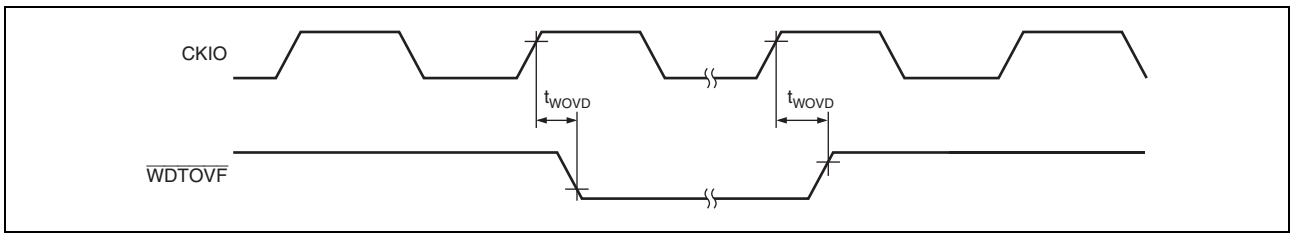


Figure 3.37 $\overline{\text{WDTOVF}}$ Output Timing

3.4.7 Serial Communication Interface with FIFO Timing

Table 3.11 Serial Communication Interface with FIFO Timing

Item		Symbol	Min.	Max.	Unit	Figure
Input clock cycle	(clocked synchronous)	t_{Scyc}	12	—	t_{p1cyc}	Figure 3.38
	(asynchronous)		4	—	t_{p1cyc}	
Input clock rise time		t_{SCKr}	—	1.5	t_{p1cyc}	
Input clock fall time		t_{SCKf}	—	1.5	t_{p1cyc}	
Input clock width		t_{SCKW}	0.4	0.6	t_{Scyc}	
Transmit data delay time (clocked synchronous)		t_{TXD}	—	3 t_{p1cyc} + 15	ns	Figure 3.39
Receive data setup time (clocked synchronous)		t_{RXS}	4 t_{p1cyc} + 15	—	ns	
Receive data hold time (clocked synchronous)		t_{RXH}	1 t_{p1cyc} + 15	—	ns	

Note: t_{p1cyc} indicates the peripheral clock 1 (P1ϕ) cycle.

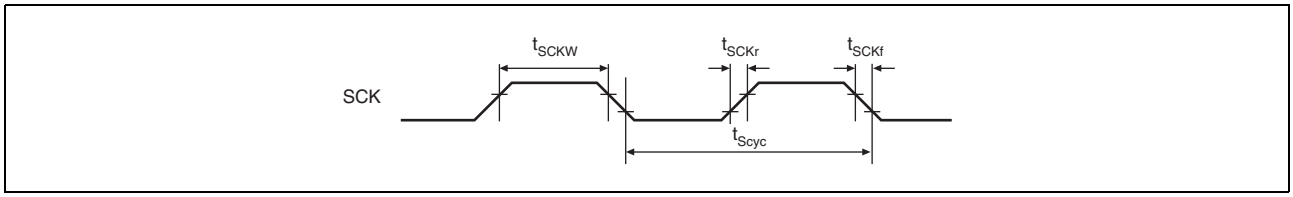


Figure 3.38 SCK Input Clock Timing

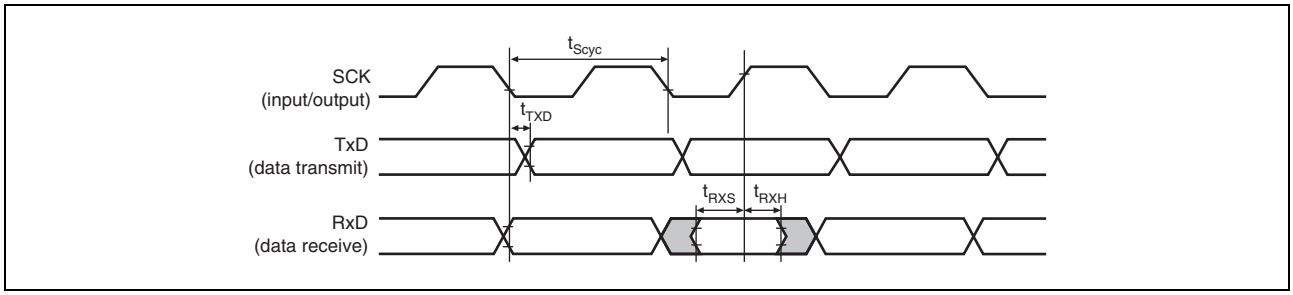


Figure 3.39 Transmit/Receive Data Input/Output Timing in Clocked Synchronous Mode

3.4.8 Serial Communication Interface Timing

Table 3.12 Serial Communication Interface Timing

Item		Symbol	Min.	Max.	Unit	Figure
Input clock cycle	(asynchronous)	t_{Scyc}	4	—	t_{p1cyc}	Figure 3.40
	(clocked synchronous)		6	—		
Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
Input clock rise time		t_{SCKr}	—	20	ns	
Input clock fall time		t_{SCKf}	—	20	ns	
Output clock cycle	(asynchronous)	t_{Scyc}	16	—	t_{p1cyc}	
	(clocked synchronous)		4	—		
Output clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
Output clock rise time		t_{SCKr}	—	20	ns	
Output clock fall time		t_{SCKf}	—	20	ns	
Transmit data delay time	(clocked synchronous)	t_{TXD}	—	40	ns	Figure 3.41
Receive data setup time	(clocked synchronous)	t_{RXS}	40	—	ns	
Receive data hold time	(clocked synchronous)	t_{RXH}	40	—	ns	

Note: t_{p1cyc} indicates the peripheral clock 1 (P1ϕ) cycle.

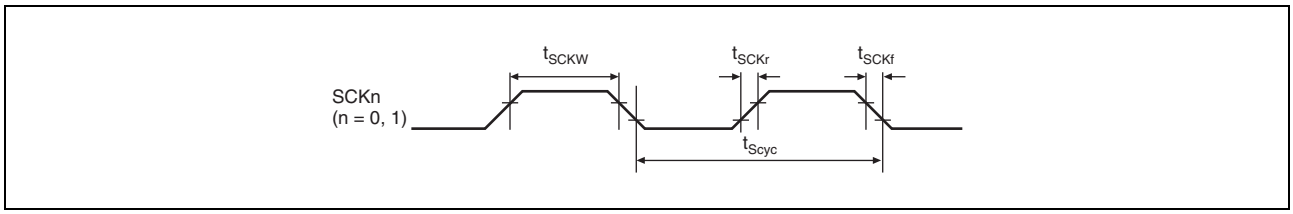


Figure 3.40 SCK Input Clock Timing

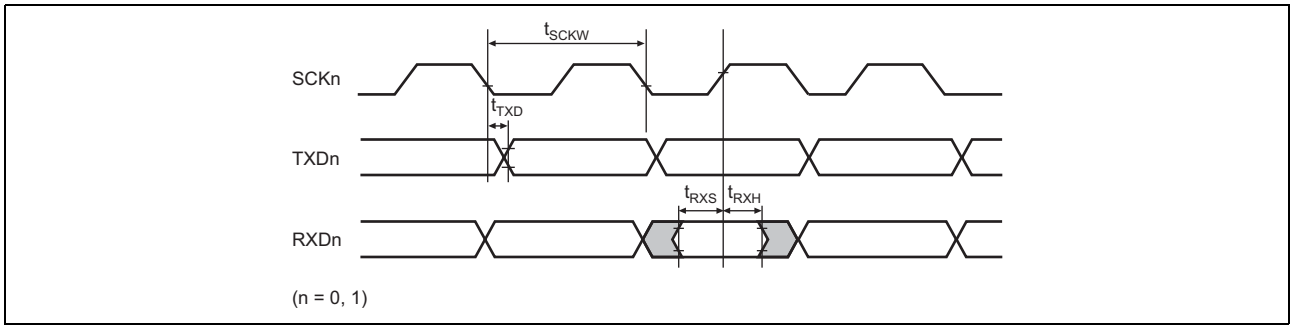


Figure 3.41 Transmit/Receive Data Input/Output Timing in Clocked Synchronous Mode

3.4.9 Renesas Serial Peripheral Interface Timing

Table 3.13 Renesas Serial Peripheral Interface Timing

Item		Symbol	Min.	Max.	Unit	Figure
RSPCK clock cycle	Master	t_{SPcyc}	2	4096	t_{cyc}	Figure 3.42
	Slave		8	4096		
RSPCK clock high pulse width	Master	t_{SPCKWH}	0.4	—	t_{SPcyc}	
	Slave		0.4	—		
RSPCK clock low pulse width	Master	t_{SPCKWL}	0.4	—	t_{SPcyc}	
	Slave		0.4	—		
Data input setup time	Master	t_{SU}	15	—	ns	Figure 3.43 to Figure 3.46
	Slave		0	—	t_{cyc}	
Data input hold time	Master	t_H	0	—	ns	
	Slave		4	—	t_{cyc}	
SSL setup time	Master	t_{LEAD}	1 × t_{SPcyc} – 20	8 × t_{SPcyc}	ns	
	Slave		4	—	t_{cyc}	
SSL hold time	Master	t_{LAG}	1 × t_{SPcyc}	8 × t_{SPcyc} + 20	ns	
	Slave		4	—	t_{cyc}	
Data output delay time	Master	t_{OD}	—	21	ns	
	Slave		—	4	t_{cyc}	
Data output hold time	Master	t_{OH}	5	—	ns	
	Slave		3	—	t_{cyc}	
Continuous transmission delay time	Master	t_{TD}	1 × t_{SPcyc} + 2 t_{cyc}	8 × t_{SPcyc} + 2 × t_{cyc}	ns	
	Slave		4 × t_{cyc}	—		
Slave access time		t_{SA}	—	4	t_{cyc}	Figure 3.45 and Figure 3.46
Slave out release time		t_{REL}	—	3	t_{cyc}	

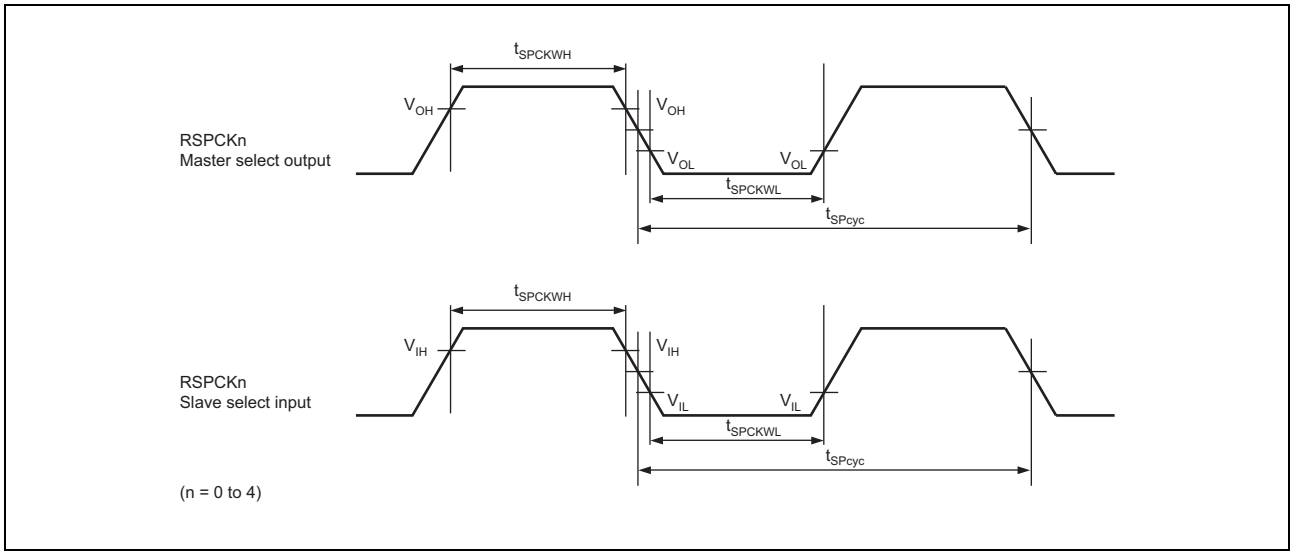


Figure 3.42 Clock Timing

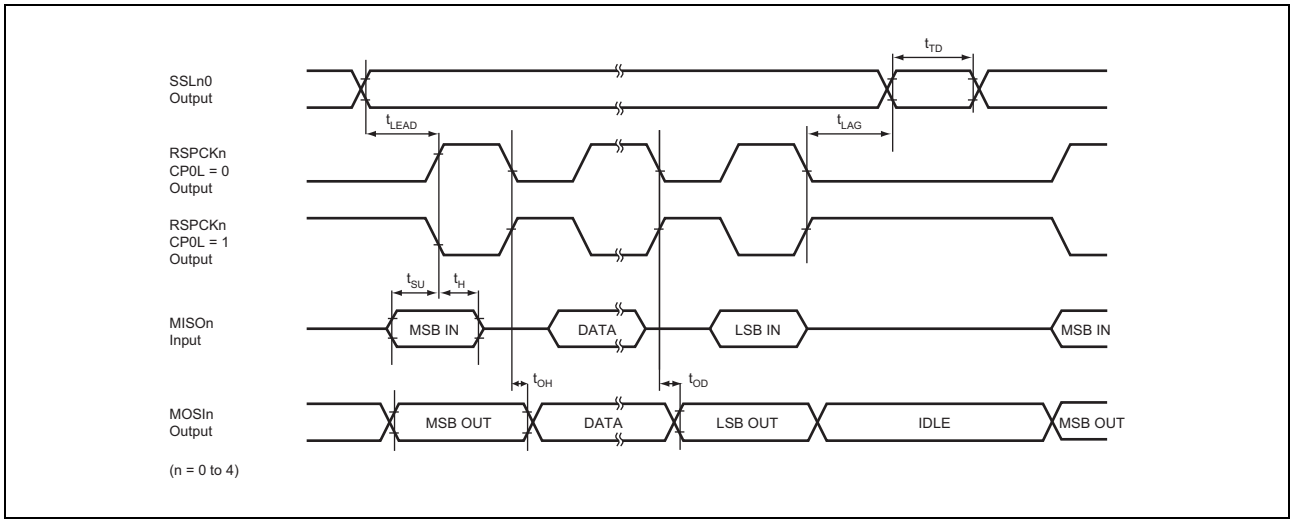


Figure 3.43 Transmission and Reception Timing (Master, CPHA = 0)

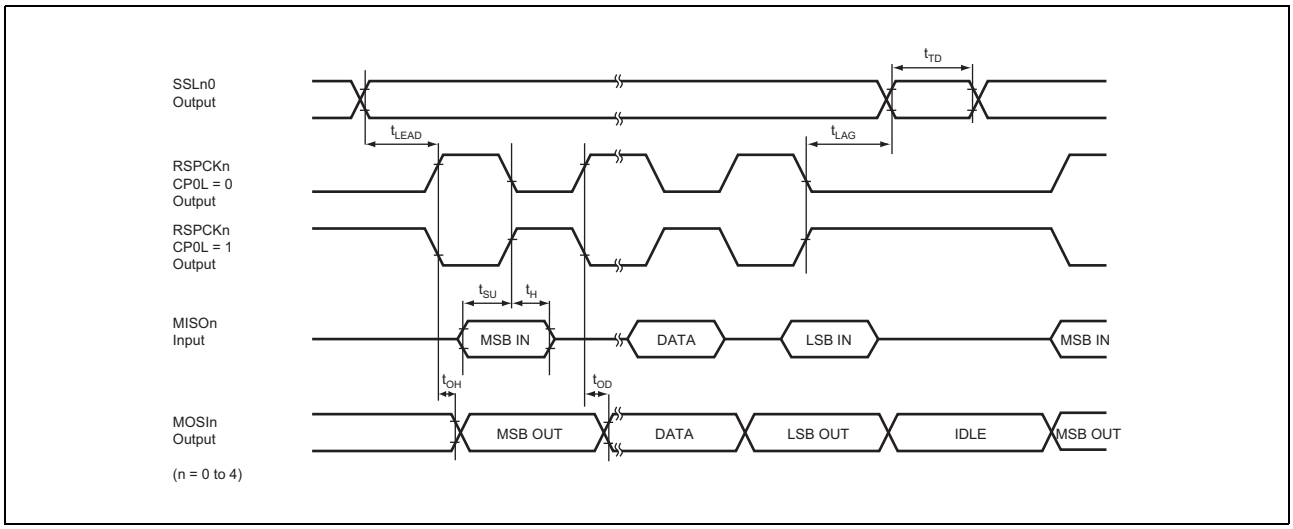


Figure 3.44 Transmission and Reception Timing (Master, CPHA = 1)

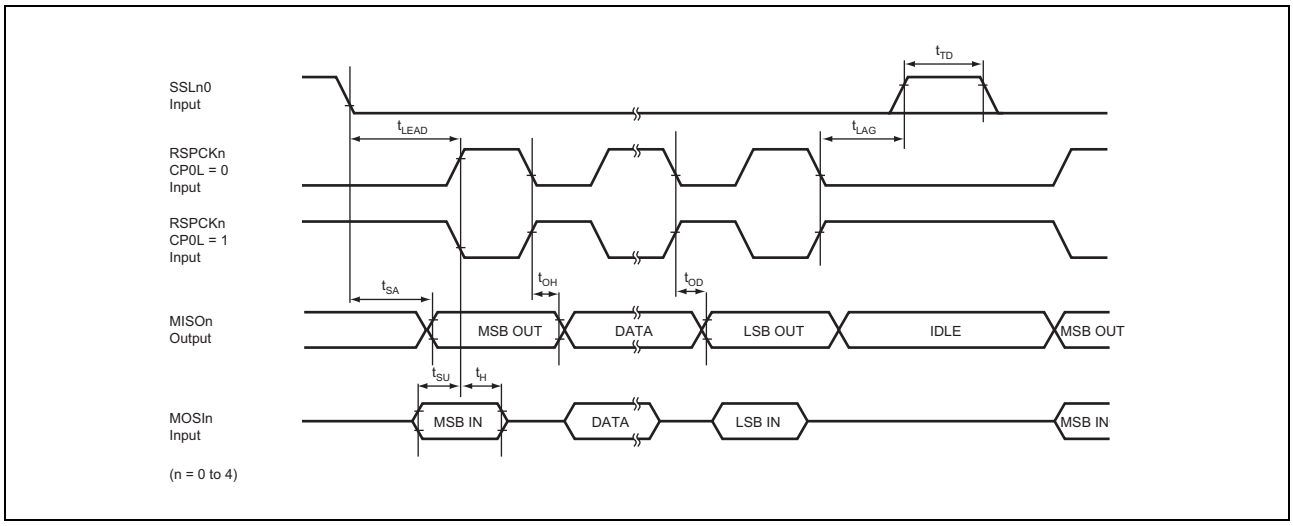


Figure 3.45 Transmission and Reception Timing (Slave, CPHA = 0)

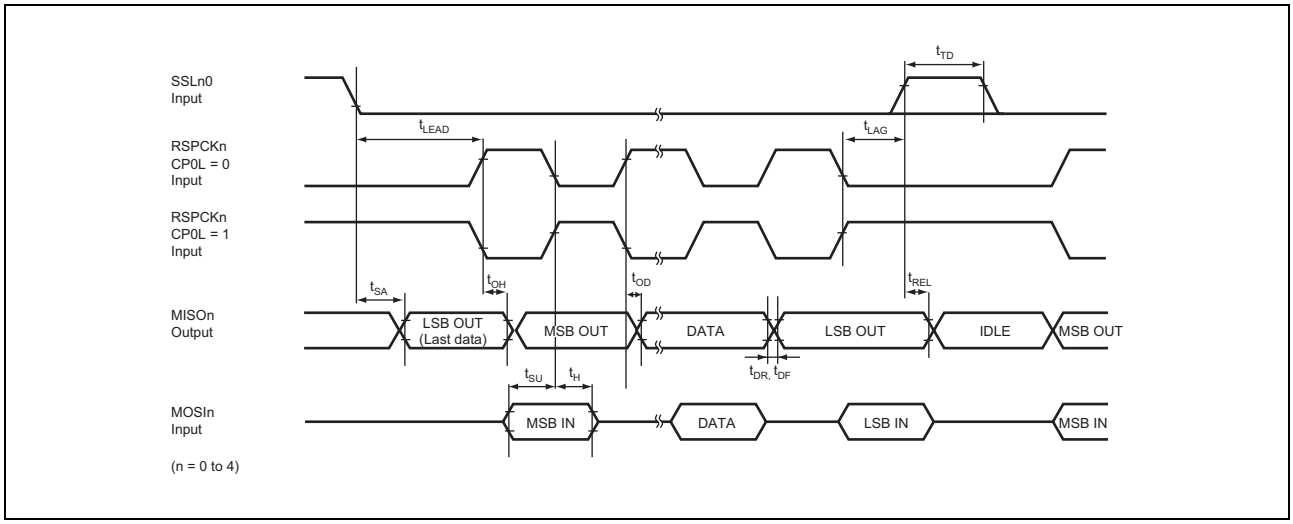


Figure 3.46 Transmission and Reception Timing (Slave, CPHA = 1)

3.4.10 SPI Multi I/O Bus Controller Timing

Table 3.14 SPI Multi I/O Bus Controller Timing

Item		Symbol	Min.	Max.	Unit	Figure
SPBCLK clock cycle		t_{SPBcyc}	2	4080	t_{bcyc}	Figure 3.47
SPBCLK high pulse width		t_{SPBWH}	0.475	0.525	t_{SPBcyc}	
SPBCLK low pulse width		t_{SPBWL}	0.475	0.525	t_{SPBcyc}	
SPBCLK rise time		t_{SPBR}	—	3	ns	
SPBCLK fall time		t_{SPBF}	—	3	ns	
Data input setup time	CKDLY = B'0100 (initial value)	t_{SU}	10.0	—	ns	Figure 3.48, Figure 3.49, Figure 3.50, and Figure 3.51
	CKDLY = B'1000		4.2	—		
Data input hold time	Common to CKDLY = B'0100 and B'1000	t_H	0.0	—	ns	
SSL setup time		t_{LEAD}	1 × t_{SPBcyc} – 3	8 × t_{SPBcyc} + 3	ns	
SSL hold time		t_{LAG}	1.5 × t_{SPBcyc} – 3	8.5 × t_{SPBcyc} + 3	ns	
Continuous transfer delay time		t_{TD}	1	8	t_{SPBcyc}	
Data output delay time	SPODLY = H'0000 (initial value)	t_{OD}	—	3.6	ns	
	SPODLY = H'6363		—	7.0		
Data output hold time	SPODLY = H'0000 (initial value)	t_{OH}	–1.6	—	ns	
	SPODLY= H'6363		1.0	—		
Data output buffer on time	SPODLY = H'0000 (initial value)	t_{BON}	—	3.6	ns	Figure 3.48, Figure 3.49, Figure 3.50, Figure 3.51, Figure 3.52, and Figure 3.53
	SPODLY = H'6363		—	7.0		
Data output buffer off time	SPODLY = H'0000 (initial value)	t_{BOFF}	–7.0	0	ns	
	SPODLY = H'6363		1.0	7.0		

Note: t_{bcyc} indicates the bus clock (Bϕ) cycle.

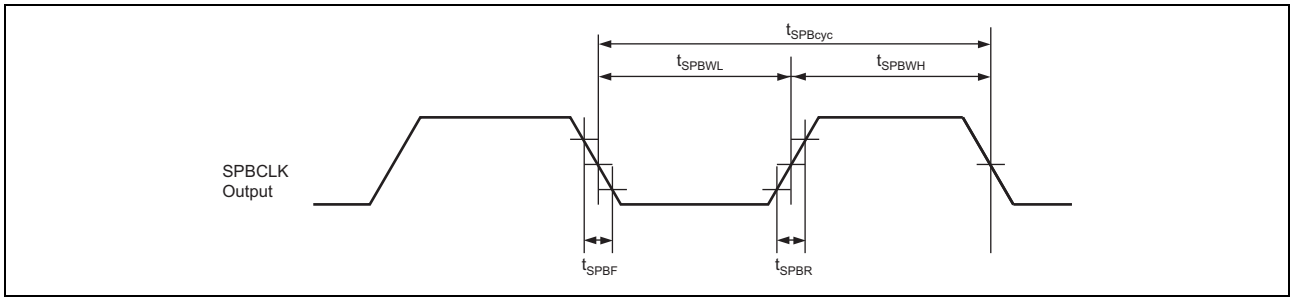


Figure 3.47 Clock Timing

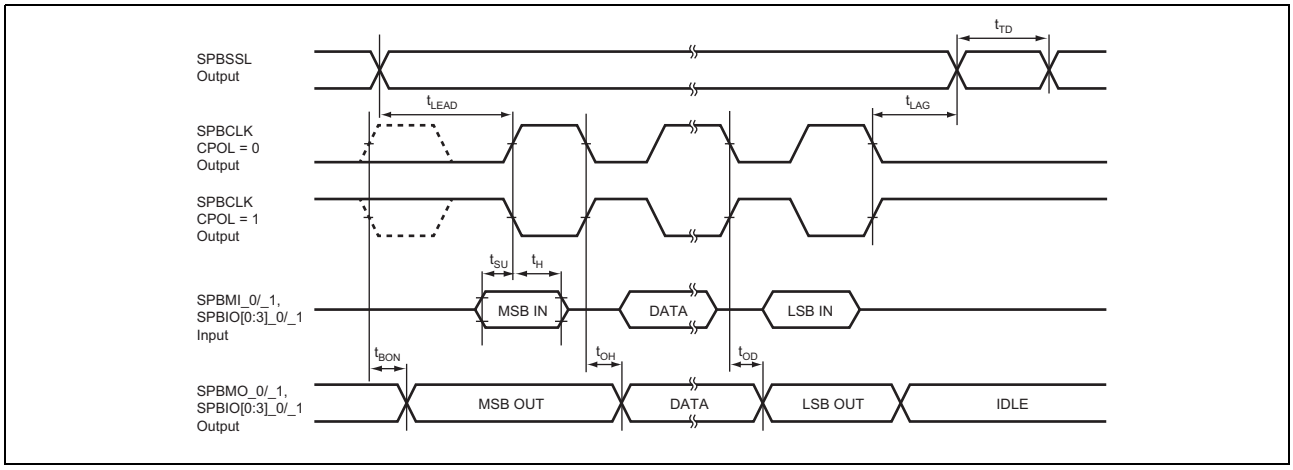


Figure 3.48 SDR Transfer Format Transmission and Reception Timing (CPHAT = 0, CPHAR = 0)

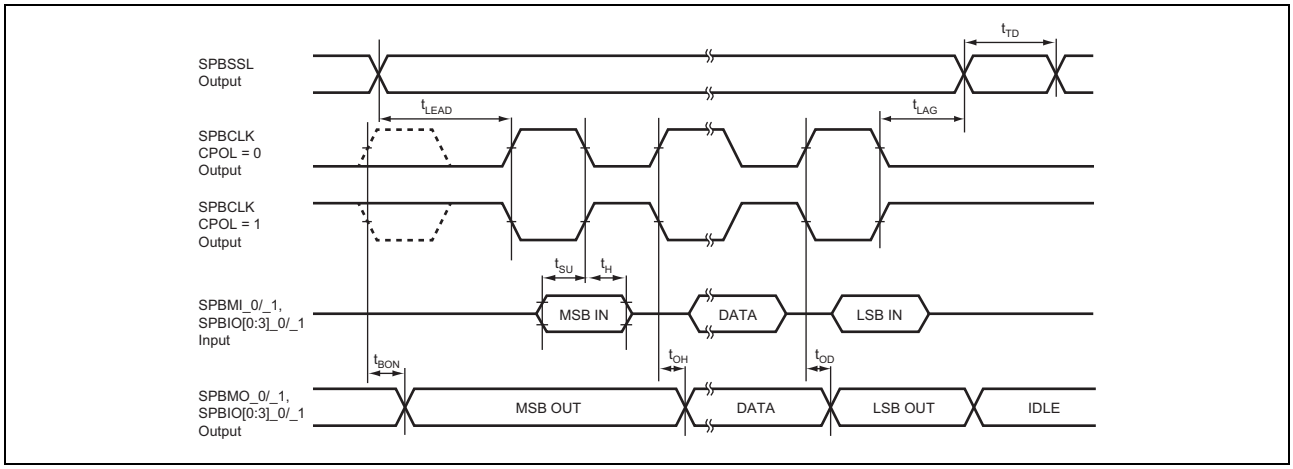


Figure 3.49 SDR Transfer Format Transmission and Reception Timing (CPHAT = 1, CPHAR = 1)

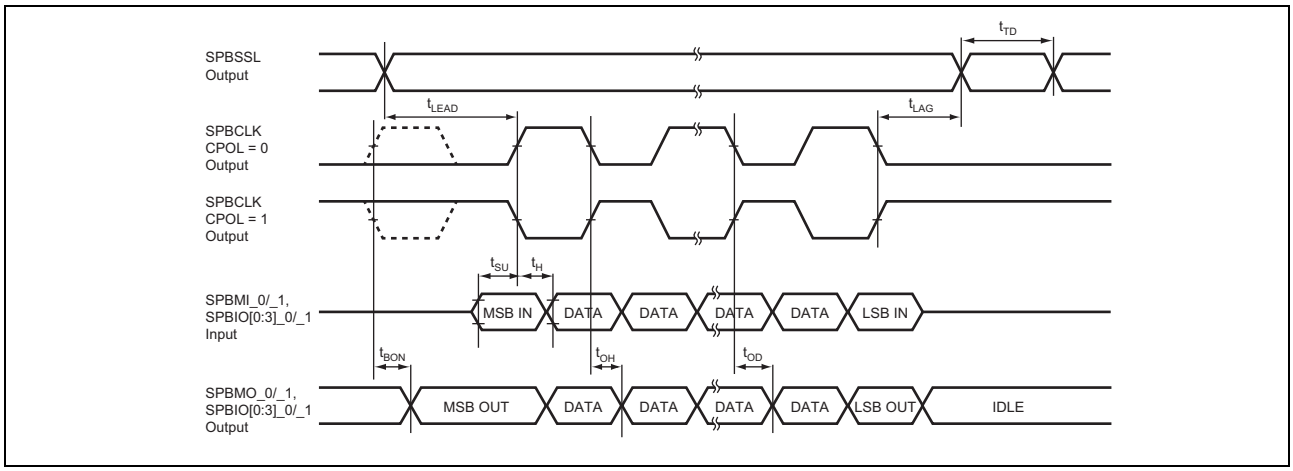


Figure 3.50 DDR Transfer Format Transmission and Reception Timing (CPHAT = 0, CPHAR = 0)

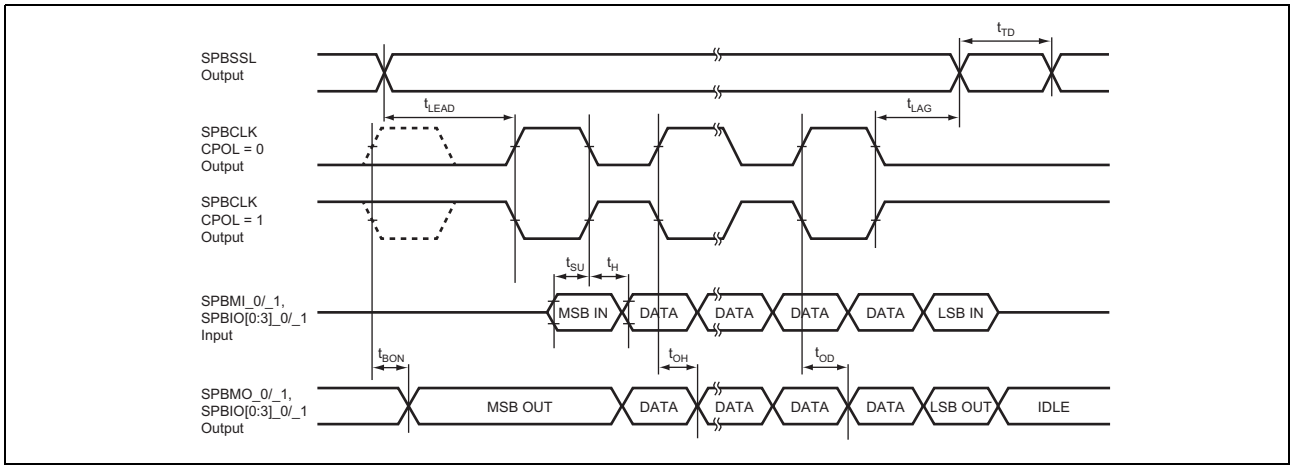


Figure 3.51 DDR Transfer Format Transmission and Reception Timing (CPHAT = 1, CPHAR = 1)

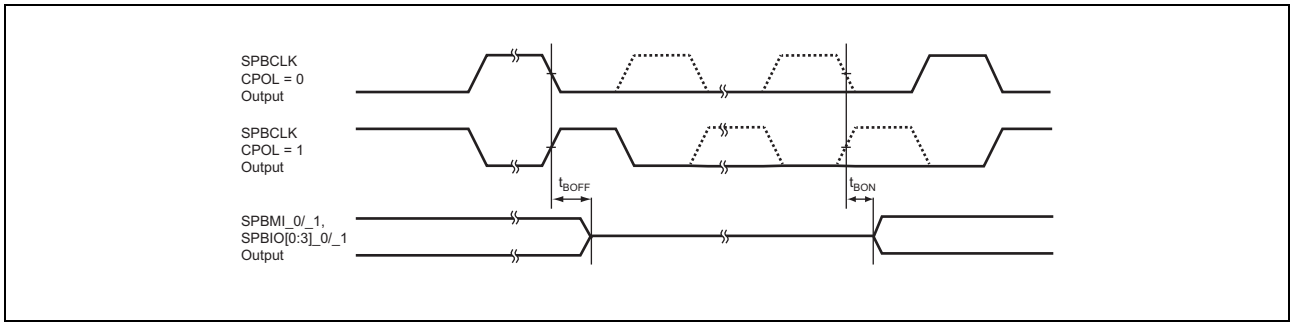


Figure 3.52 Timing for Switching the Buffers on and off (CPHAT = 0, CPHAR = 0)

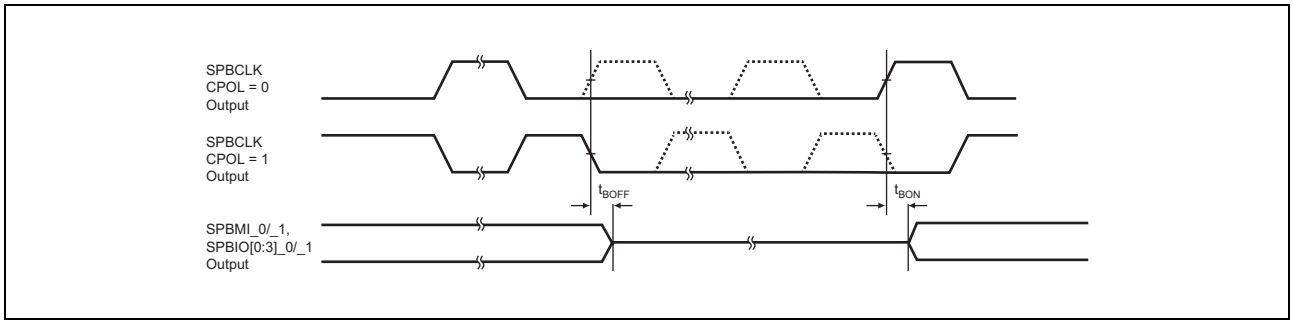


Figure 3.53 Timing for Switching the Buffers on and off (CPHAT = 1, CPHAR = 1)

3.4.11 I²C Bus Interface Timing

Table 3.15 I²C Bus Interface Timing

Item	Symbol	I/O	Standard mode (Sm)		Fast mode (Fm)		Unit
			Min.	Max.	Min.	Max.	
SCL clock frequency	f_{CLK}	I/O	0	100	0	400	kHz
Bus free time (between stop and start condition)	t_{BUF}	I/O	4.7	-	1.3	-	µs
Hold time*1	$t_{HD:STA}$	I/O	4.0	-	0.6	-	µs
Low period of SCL clock	t_{LOW}	I/O	4.7	-	1.3	-	µs
High period of SCL clock	t_{HIGH}	I/O	4.0	-	0.6	-	µs
Setup time for start/restart condition	$t_{SU:STA}$	I/O	4.7	-	0.6	-	µs
Data hold time (I²C bus device)	$t_{HD:DAT}$	I/O	0*2	-	0*2	-	µs
Data setup time	$t_{SU:DAT}$	I/O	250	-	100*3	-	ns
SDA and SCL signal rise time	t_R	Input	-	1000	20	300	ns
SDA and SCL signal fall time*3	t_F	Input	-	300	20 × (PV_{CC}/5.5 V)	300	ns
		Output	-	250	20 × (PV_{CC}/5.5 V)	250	ns
Setup time for STOP condition	$t_{SU:STO}$	I/O	4.0	-	0.6	-	µs
Capacitive load for each bus line	C_b	-	-	400*4	-	400*4	pF
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	Input	-	-	0	50*5	ns

In the above table and subsequently, SCL and SDA refer to the RIICnSCL and RIICnSDA signals, respectively.

Note 1. The first clock pulse is generated on the SCL line after the start condition has been issued and the hold time has elapsed.

Note 2. This module requires a minimum of 300 ns hold time internally for the SDA signal to handle the period over which the falling edge of SCL has not reached a defined level (time until the CnSCL signal reaches V_{IL} (max.) from V_{IH} (min.)).

Note 3. The fast-mode I²C bus device can be used in the standard mode I²C bus system. In this case, the minimum value of the data setup time ($t_{SU: DAT (min.)}$ 250 [ns]) must be satisfied.
If the system does not extend the low period of SCL clock (t_{LOW}), this condition is automatically satisfied. If the system extends the low period of SCL clock (t_{LOW}), transmit the subsequent data bit to the SDA line before the SCL line is released ($t_{R (max.)}$ + $t_{SU: DAT (min.)}$ = 1000 + 250 = 1250 [ns]: (standard mode I²C bus specification)).

Note 4. Total capacitance of one bus line. The allowable maximum bus capacitance may differ from this specification, depending on the actual operating voltage and frequency of an application. For techniques to cope with a large bus capacitance, see the I²C bus specification provided by NXP Semiconductors.

Note 5. Noise is removed by the analog and digital input filters. The level of noise reduction of the digital input filter is determined by the period of internal reference clock (IICφ) and the NF[1:0] bits in RIICnMR3. For details, refer to section 18, I²C Bus Interface, in the RZ/A1H Group, RZ/A1M Group User's Manual.

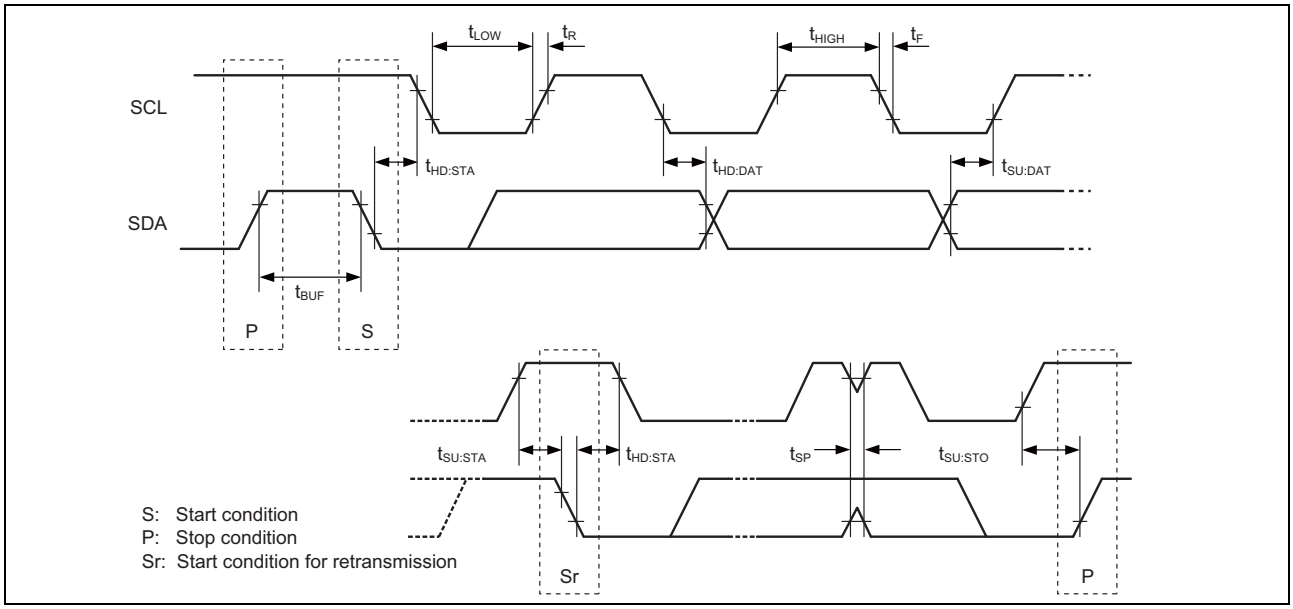


Figure 3.54 Input/Output Timing

3.4.12 Serial Sound Interface Timing

Table 3.16 Serial Sound Interface Timing

Item		Symbol	Min.	Max.	Unit	Remarks	Figure
Output clock cycle		t_O	80	64000	ns	Output	Figure 3.55
Input clock cycle		t_I	80	64000	ns	Input	
Clock high		t_{HC}	32	—	ns	Bidirectional	
Clock low		t_{LC}	32	—	ns		
Clock rise time		t_{RC}	—	25	ns	Output	
Delay	Noise canceler not in use	t_{DTR}	–5	25	ns		Figure 3.56, Figure 3.57, Figure 3.58, Figure 3.59, and Figure 3.60
	Noise canceler in use		10	45	ns		
Setup time		t_{SR}	25	—	ns		
Hold time		t_{HTR}	5	—	ns		

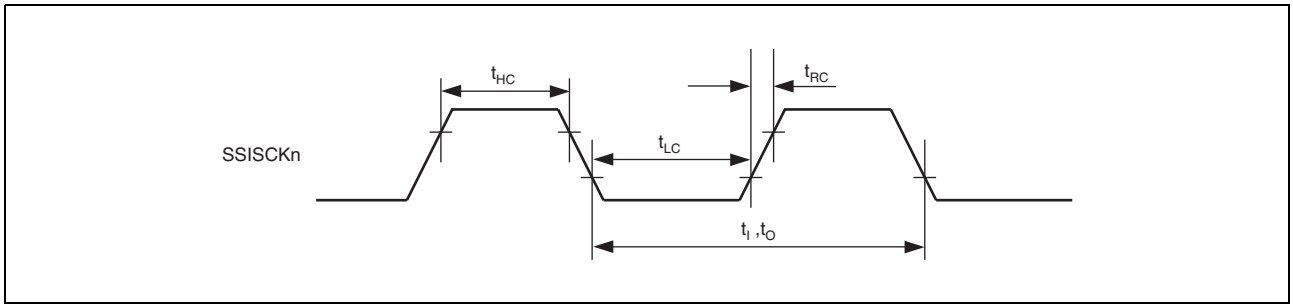


Figure 3.55 Clock Input/Output Timing

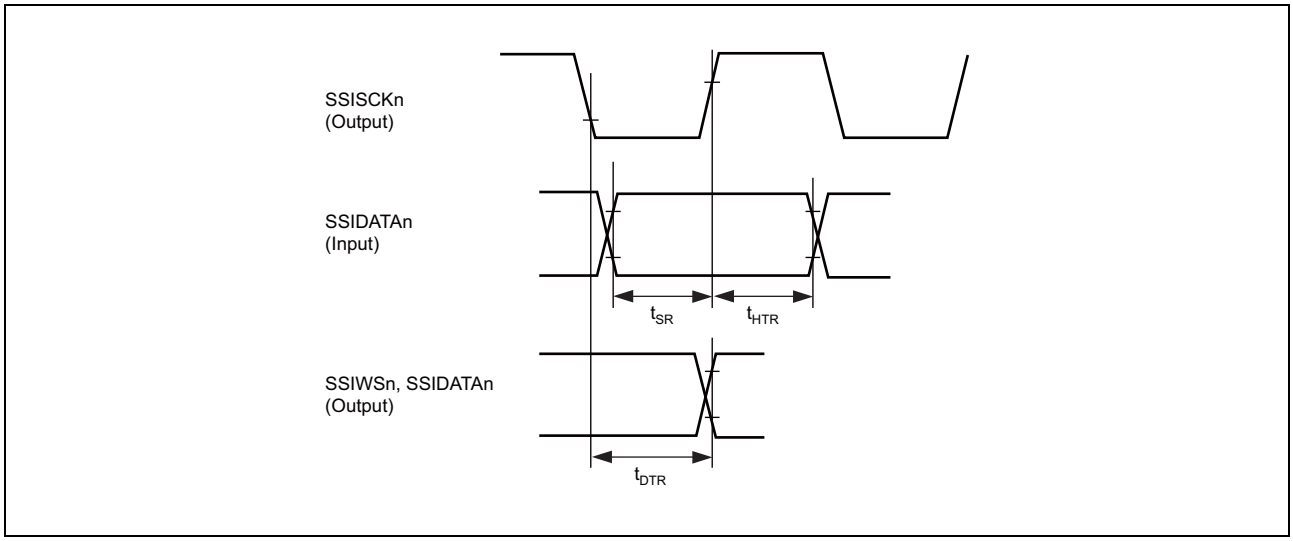


Figure 3.56 Transmission and Reception Timing (Master, SSICR_n.SCKP = 0)

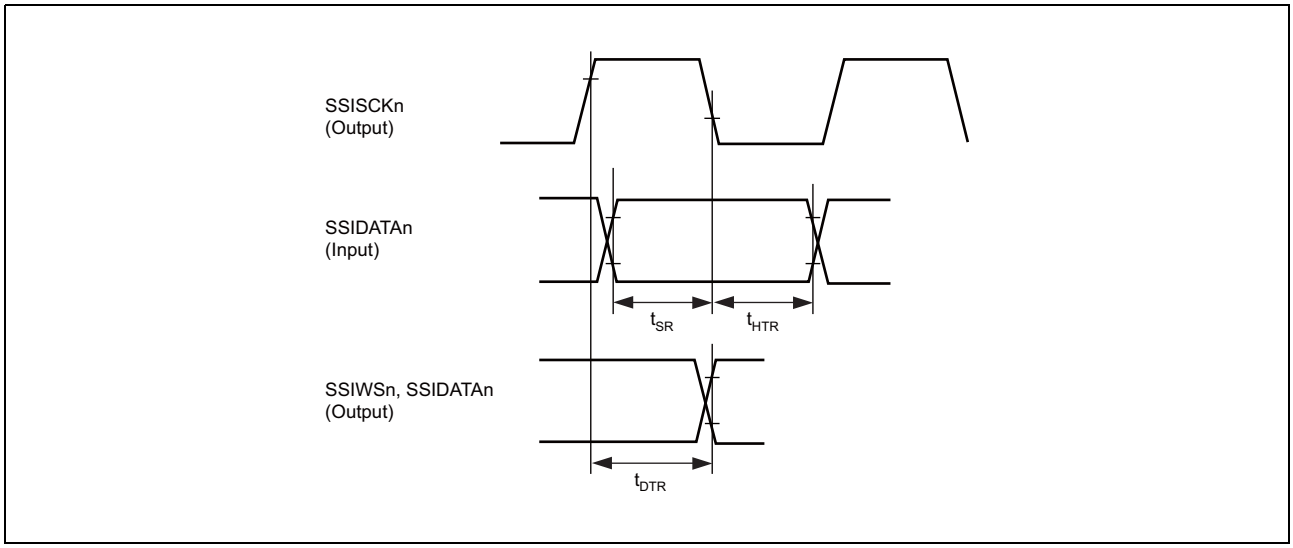


Figure 3.57 Transmission and Reception Timing (Master, SSICR_n.SCKP = 1)

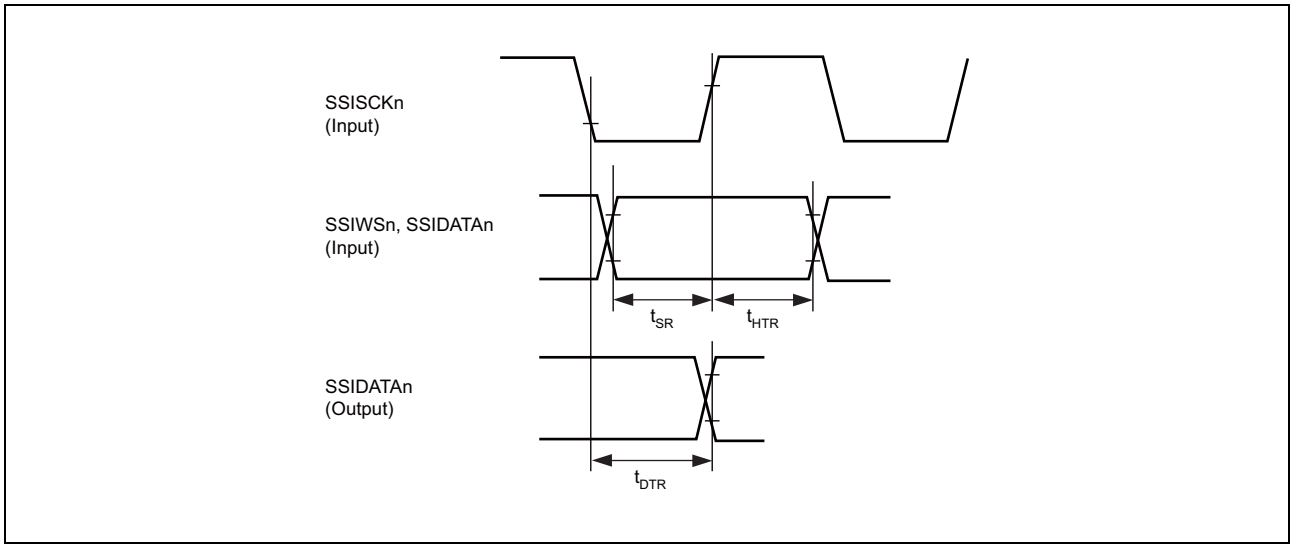


Figure 3.58 Transmission and Reception Timing (Slave, SSICR_n.SCKP = 0)

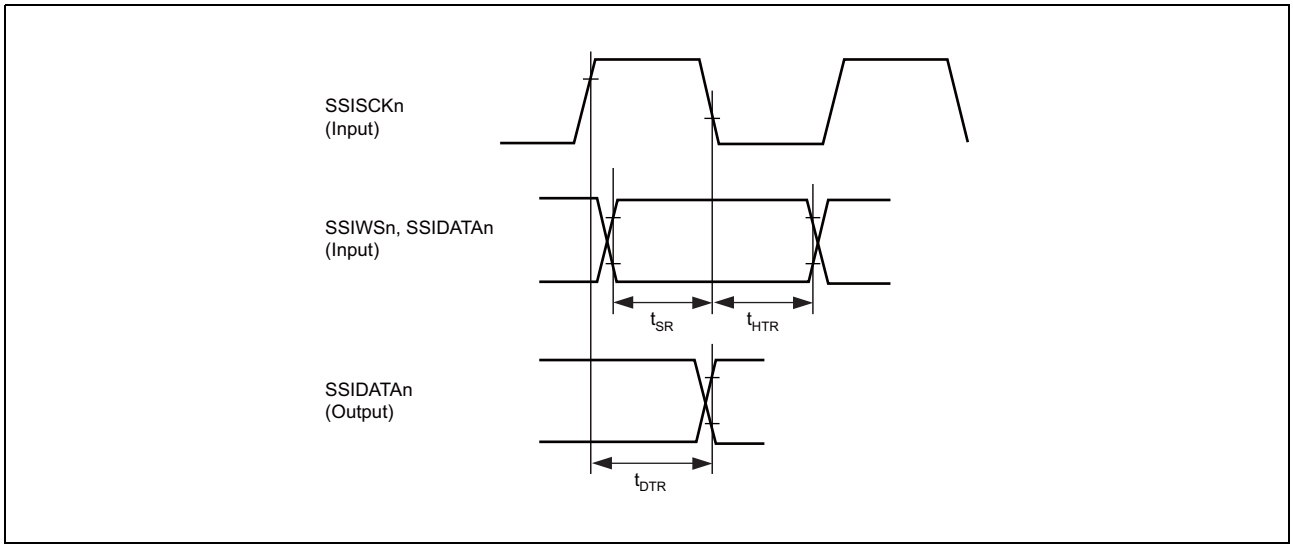
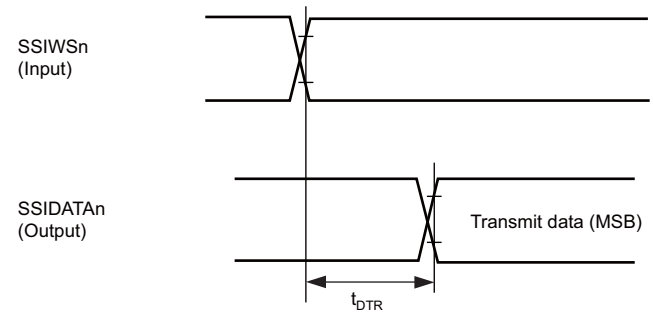


Figure 3.59 Transmission and Reception Timing (Slave, SSICR_n.SCKP = 1)



Note: MSB output timing of when either of the following condition a) or b) is satisfied in slave transmission.
a) SSICR_n.DEL = 1, SSICR_n.SDATA = 0
b) SSICR_n.DEL = 1, SSICR_n.SDATA = 1, with no padding bit

Figure 3.60 Transmission Timing (Slave, in Synchronization with SSIWSn)

3.4.13 Media Local Bus Timing

Table 3.17 Media Local Bus Timing

Item	Symbol	Min.	Typ	Max.	Unit	Remarks	Figure
Input clock frequency (256 × FS)	f_I	11.2640	12.2880	12.3136	MHz		Figure 3.61
Input clock cycle (256 × FS)	t_I	—	81	—	ns		
Input clock high level (256 × FS)	t_{HC}	30	36.5	—	ns		
Input clock low level (256 × FS)	t_{LC}	30	35.5	—	ns		
Input clock frequency (512 × FS)	f_I	22.5280	24.5760	24.6272	MHz		
Input clock cycle (512 × FS)	t_I	—	40	—	ns		
Input clock high level (512 × FS)	t_{HC}	14	16.5	—	ns		
Input clock low level (512 × FS)	t_{LC}	14	16.5	—	ns		
Input clock frequency (1024 × FS)	f_I	45.0560	49.1520	49.2544	MHz		
Input clock cycle (1024 × FS)	t_I	—	20.3	—	ns		
Input clock high level (1024 × FS)	t_{HC}	9.3	10.2	—	ns		
Input clock low level (1024 × FS)	t_{LC}	6.1	7.3	—	ns		
Input clock rise time	t_{RC}	—	—	1	ns	V_{IL} to V_{IH}	
Input clock fall time	t_{FC}	—	—	1	ns	V_{IH} to V_{IL}	
Delay time (clock signal rising)	t_{DTR}	—	—	8.0	ns	Output load: 20 pF	
Delay time (clock signal falling)	t_{DTF}	0	—	t_{LC}	ns		
Setup time	t_{SR}	1	—	—	ns		
Hold time	t_{HTR}	2	—	—	ns		

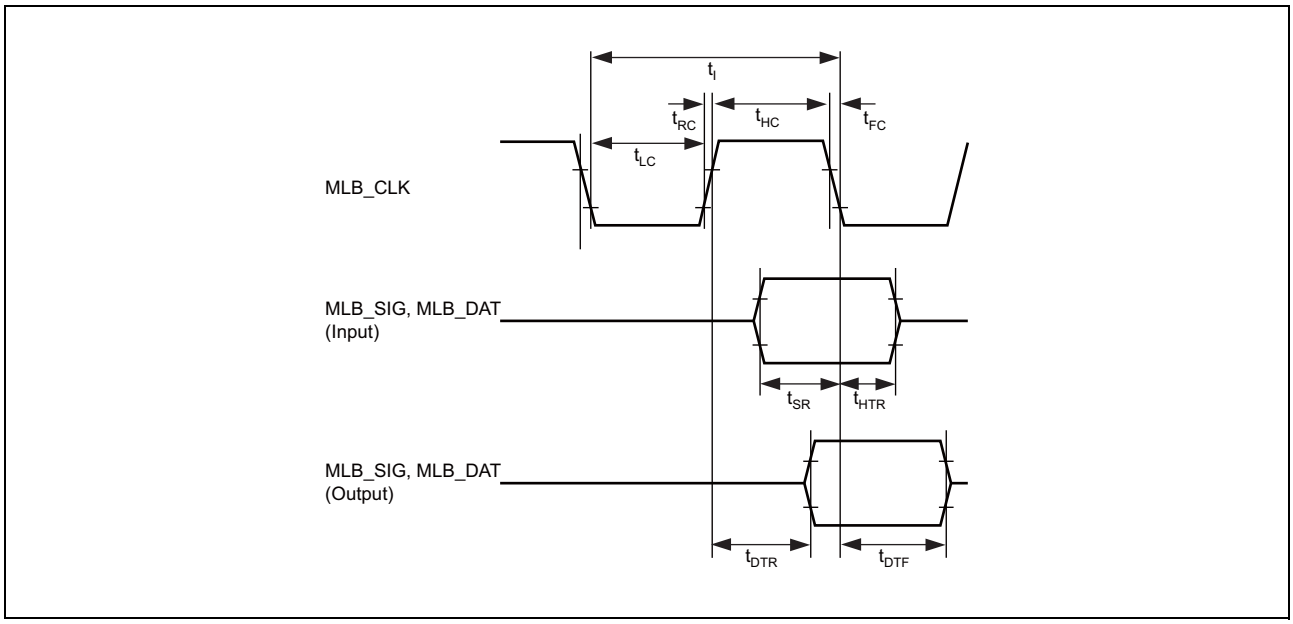


Figure 3.61 Interface Timing

3.4.14 CAN Interface Timing

Table 3.18 CAN Interface Timing

Item	Symbol	Min.	Max.	Unit	Figure
Internal delay time	tnode	—	100	ns	Figure 3.62
Transmission rate		—	1	Mbps	

Internal delay time (tnode) = Internal transfer delay time (toutput) + Internal receive delay time (tinput)

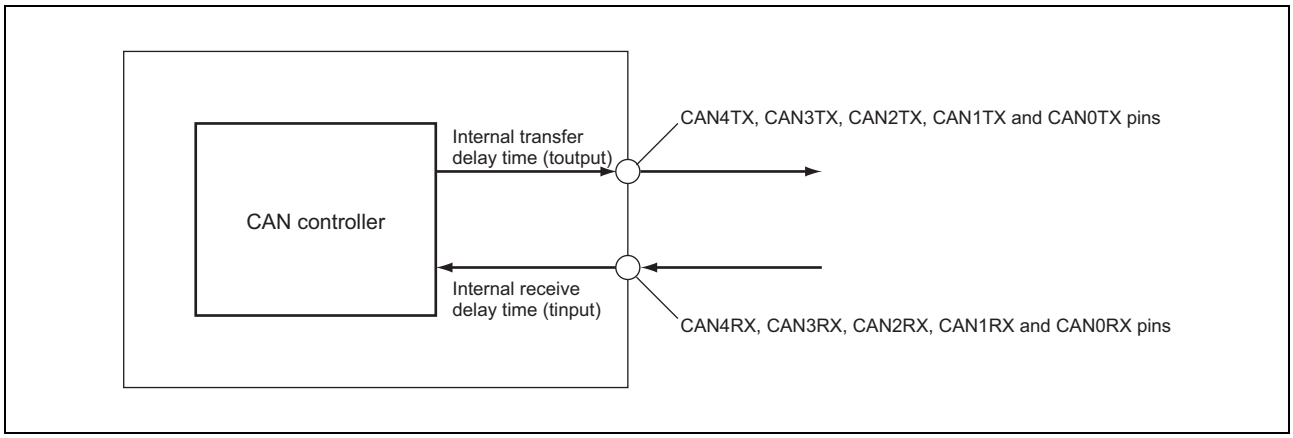


Figure 3.62 CAN Interface Condition

3.4.15 Ethernet Controller and EthernetAVB Timing

Table 3.19 Ethernet Controller Timing

Item	Symbol	Min.	Max.	Unit	Figure
ET_TXCLK cycle time	t_{Tcyc}	40	—	ns	Figure 3.63, Figure 3.64, Figure 3.65, Figure 3.66, and Figure 3.67
ET_TXCLK high level width	t_{TCKWH}	0.35 × t_{Tcyc}	—	ns	
ET_TXCLK low level width	t_{TCKWL}	0.35 × t_{Tcyc}	—	ns	
ET_TXEN output delay time	t_{TEND}	0	25	ns	
ET_TXD[3:0] output delay time	t_{TDD}	0	25	ns	
ET_RXCLK cycle time	t_{Rcyc}	40	—	ns	
ET_RXCLK high level width	t_{RCKWH}	0.35 × t_{Rcyc}	—	ns	
ET_RXCLK low level width	t_{RCKWL}	0.35 × t_{Rcyc}	—	ns	
ET_RXDV setup time	t_{RDVS}	10	—	ns	
ET_RXDV hold time	t_{RDVH}	10	—	ns	
ET_RXD[3:0] setup time	t_{RDDS}	10	—	ns	
ET_RXD[3:0] hold time	t_{RDDH}	10	—	ns	
ET_RXER setup time	t_{RERS}	10	—	ns	
ET_RXER hold time	t_{RERH}	10	—	ns	
AVB_GPTP_EXTERN cycle time	t_{Gcyc}	40	—	ns	
AVB_GPTP_EXTERN high level width	t_{GCKWH}	0.35 × t_{Gcyc}	—	ns	
AVB_GPTP_EXTERN low level width	t_{GCKWL}	0.35 × t_{Gcyc}	—	ns	
AVB_CAPTURE high level width	t_{CAPWH}	2 × t_{Ccyc}*	—	ns	

Note: * This is the cycle time of the clock selected by the CSEL bit in the AVB-DMAC mode register (CCC).

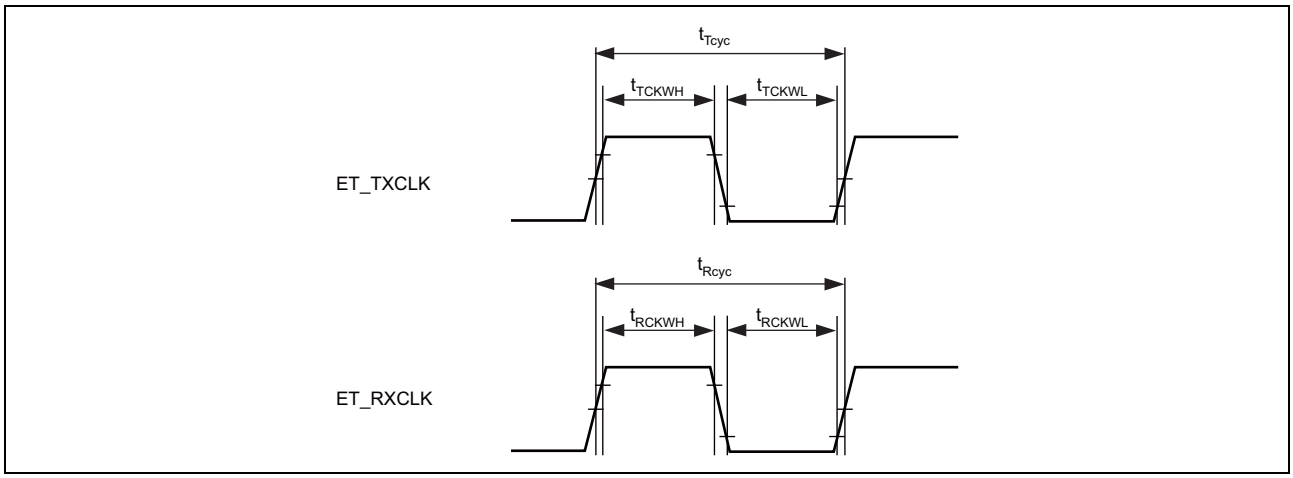


Figure 3.63 MII Clock Timing

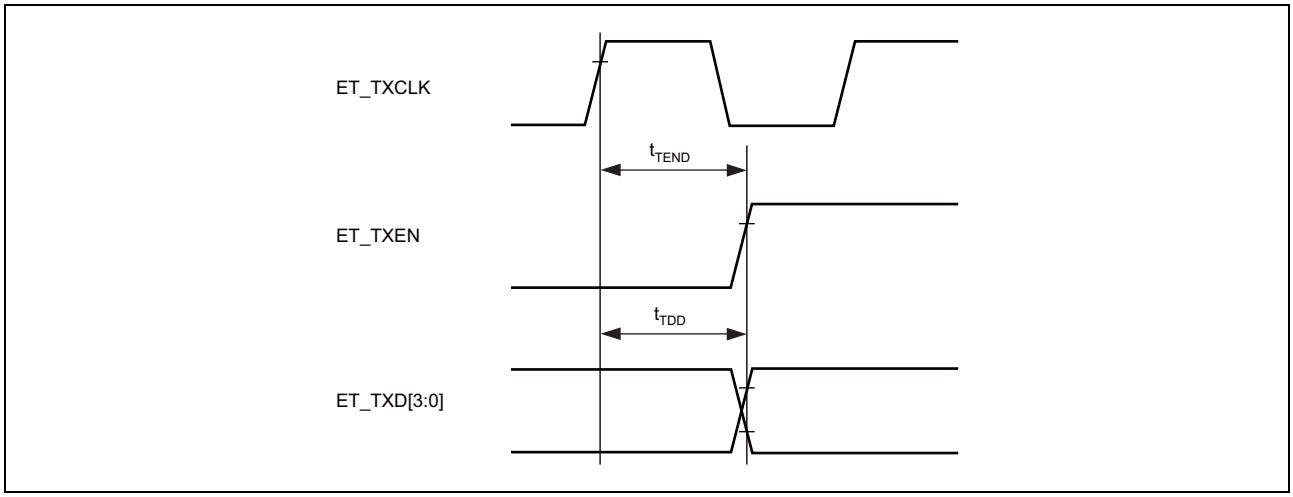


Figure 3.64 MII Transmit Data Timing

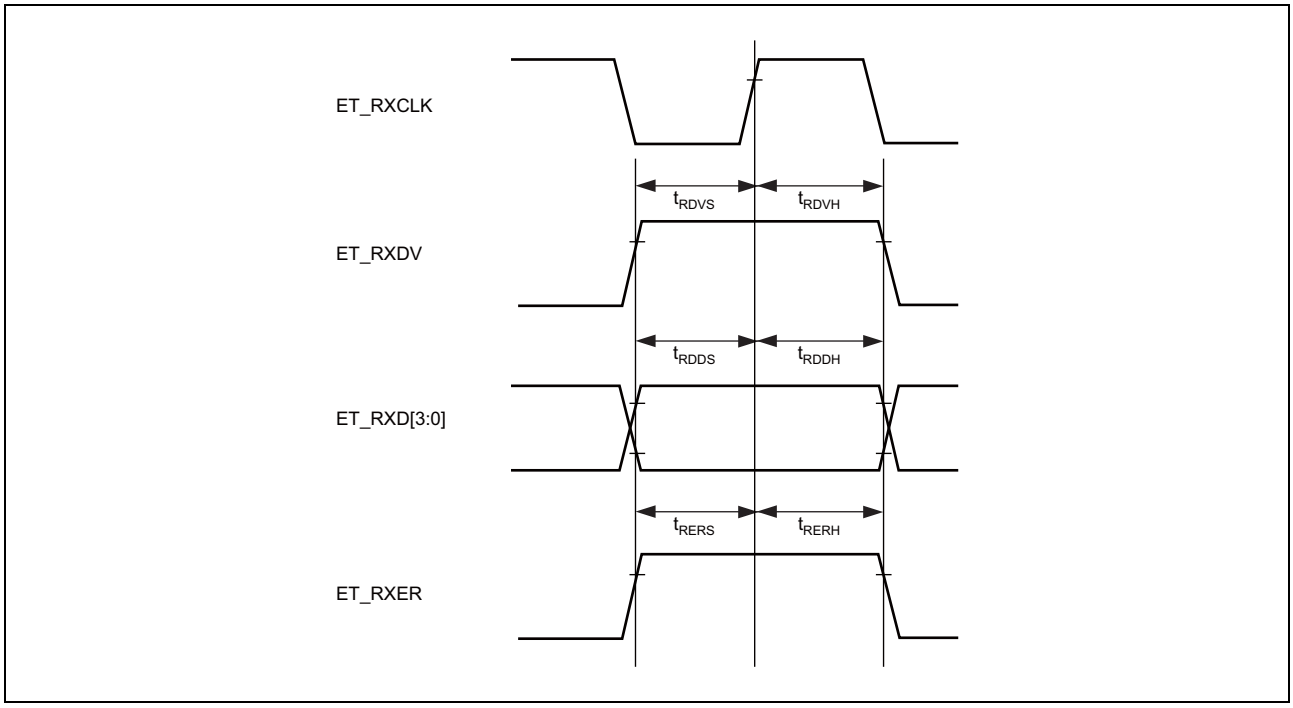


Figure 3.65 MII Receive Data Timing

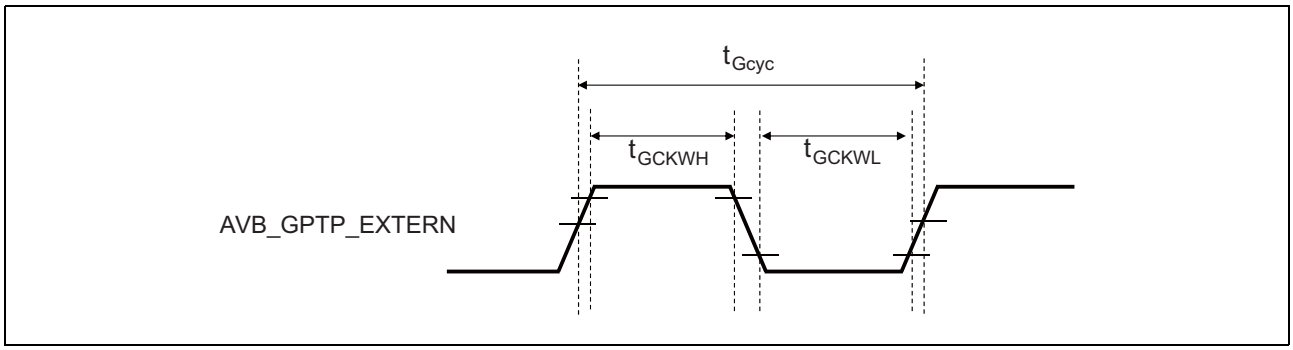


Figure 3.66 gPTP Timer External Clock Timing

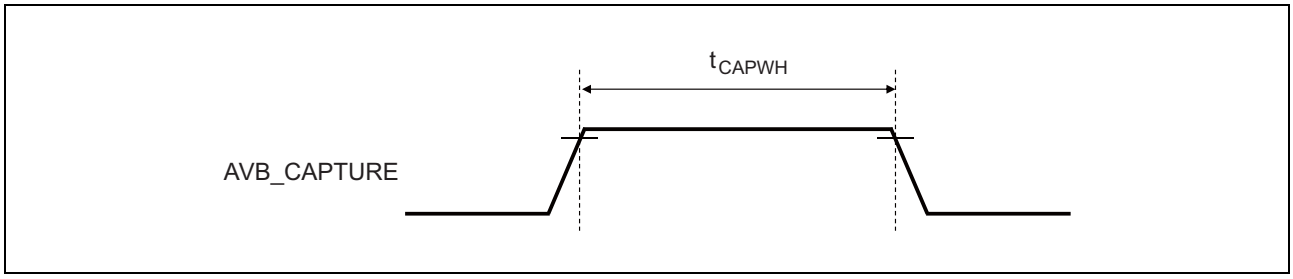


Figure 3.67 Timer Capture Signal Timing

3.4.16 A/D Converter Timing

Table 3.20 A/D Converter Timing

Module	Item	Symbol	Min.	Max.	Unit	Figure
A/D converter	Trigger input setup time	t_{TRGS}	17	—	ns	Figure 3.68

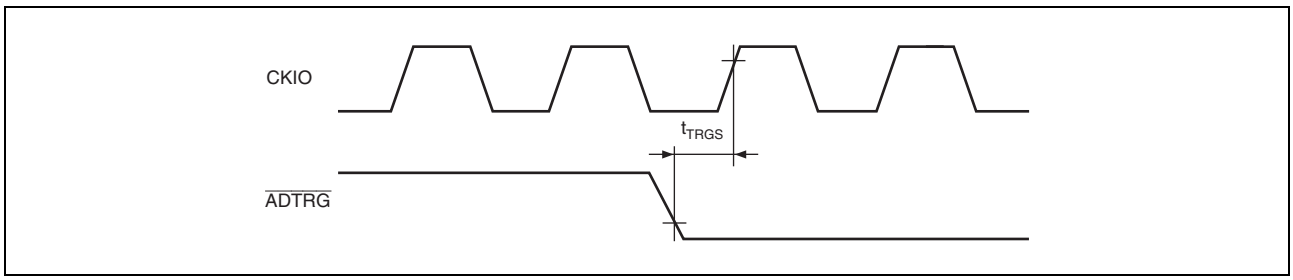


Figure 3.68 A/D Converter External Trigger Input Timing

3.4.17 NAND Type Flash Memory Controller Timing

Table 3.21 NAND Type Flash Memory Interface Timing

Item	Symbol	Min.	Max.	Unit	Figure
Command output setup time	t_{NCDS}	$2 \times t_{fcyc} - 10$	—	ns	Figure 3.69 and Figure 3.73
Command output hold time	t_{NCDH}	$1.5 \times t_{fcyc} - 5$	—	ns	
Data output setup time	t_{NDOS}	$0.5 \times t_{wfcyc} - 5$	—	ns	Figure 3.69, Figure 3.70, Figure 3.72, and Figure 3.73
Data output hold time	t_{NDOH}	$0.5 \times t_{wfcyc} - 10$	—	ns	
Command to address transition time 1	t_{NCDAD1}	$1.5 \times t_{fcyc} - 10$	—	ns	Figure 3.69 and Figure 3.70
Command to address transition time 2	t_{NCDAD2}	$2 \times t_{fcyc} - 10$	—	ns	Figure 3.70
$\overline{\text{FWE}}$ cycle time	t_{NWC}	$t_{wfcyc} - 5$	—	ns	Figure 3.70 and Figure 3.72
$\overline{\text{FWE}}$ low pulse width	t_{NWP}	$0.5 \times t_{wfcyc} - 5$	—	ns	Figure 3.69, Figure 3.70, Figure 3.72, and Figure 3.73
$\overline{\text{FWE}}$ high pulse width	t_{NWH}	$0.5 \times t_{wfcyc} - 5$	—	ns	Figure 3.70 and Figure 3.72
Address to ready/busy transition time	t_{NADRB}	—	$32 \times t_{p0cyc}$	ns	Figure 3.70 and Figure 3.71
Command to ready/busy transition time	t_{NCDRB}	—	$10 \times t_{p0cyc}$	ns	Figure 3.70 and Figure 3.71
Ready/busy to data read transition time 1	t_{NRBDR1}	$1.5 \times t_{fcyc}$	—	ns	Figure 3.71
Ready/busy to data read transition time 2	t_{NRBDR2}	$32 \times t_{p0cyc}$	—	ns	
$\overline{\text{FRE}}$ cycle time	t_{NSCC}	$t_{wfcyc} - 5$	—	ns	
$\overline{\text{FRE}}$ low pulse width	t_{NSP}	$0.5 \times t_{wfcyc} - 5$	—	ns	Figure 3.71 and Figure 3.73
$\overline{\text{FRE}}$ high pulse width	t_{NSPH}	$0.5 \times t_{wfcyc} - 5$	—	ns	Figure 3.71
Read data setup time	t_{NRDS}	16	—	ns	Figure 3.71 and Figure 3.73
Read data hold time	t_{NRDH}	5	—	ns	Figure 3.71 and Figure 3.73
Data write setup time	t_{NDWS}	$32 \times t_{p0cyc}$	—	ns	Figure 3.72
Command to status read transition time	t_{NCDSR}	$4 \times t_{fcyc}$	—	ns	Figure 3.73
Command output off to status read transition time	t_{NCDFSR}	$3.5 \times t_{fcyc}$	—	ns	
Status read setup time	t_{NSTS}	$2.5 \times t_{fcyc}$	—	ns	
$\overline{\text{FCE}}$ output setup time	t_{NCES}	$8 \times t_{p0cyc}$	—	ns	Figure 3.69

Note: t_{fcyc} indicates the period of one cycle of the FLCTL clock.
t_{wfcyc} indicates the period of one cycle of the FLCTL clock when the value of the NANDWF bit is 0. On the other hand, t_{wfcyc} indicates the period of two cycles of the FLCTL clock when the value of the NANDWF bit is 1.
t_{p0cyc} indicates the period of one cycle of the peripheral clock (P0ϕ).

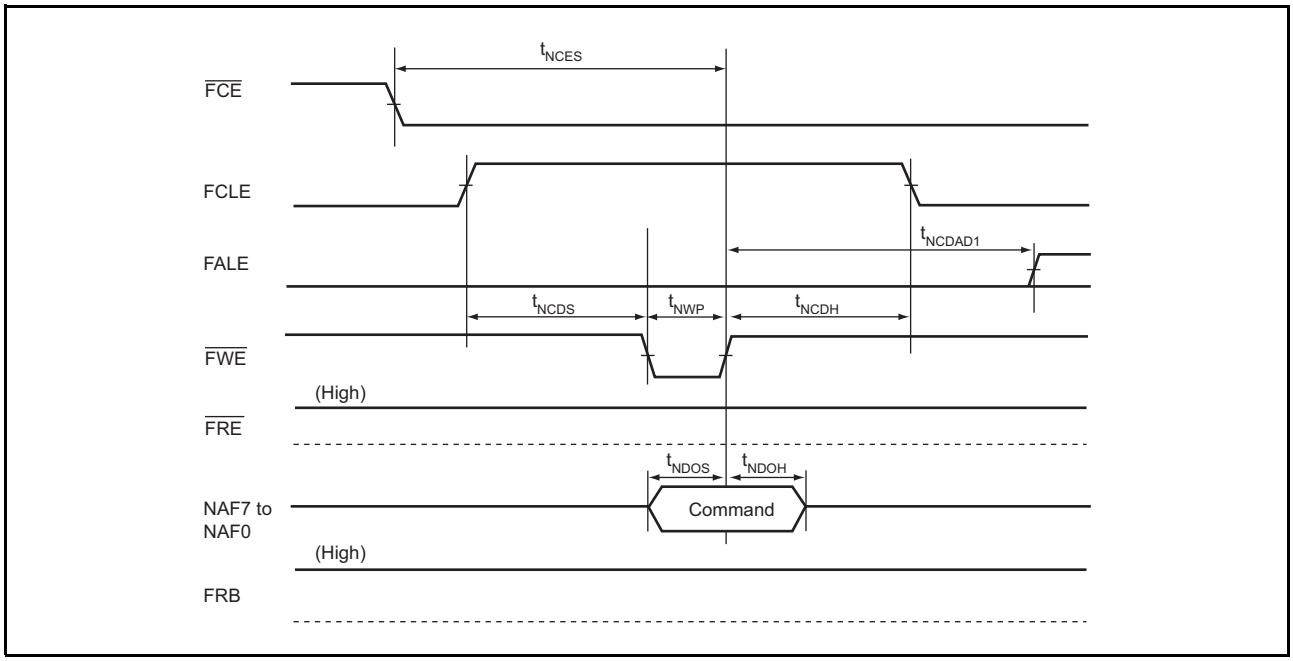


Figure 3.69 NAND Type Flash Memory Command Issuance Timing

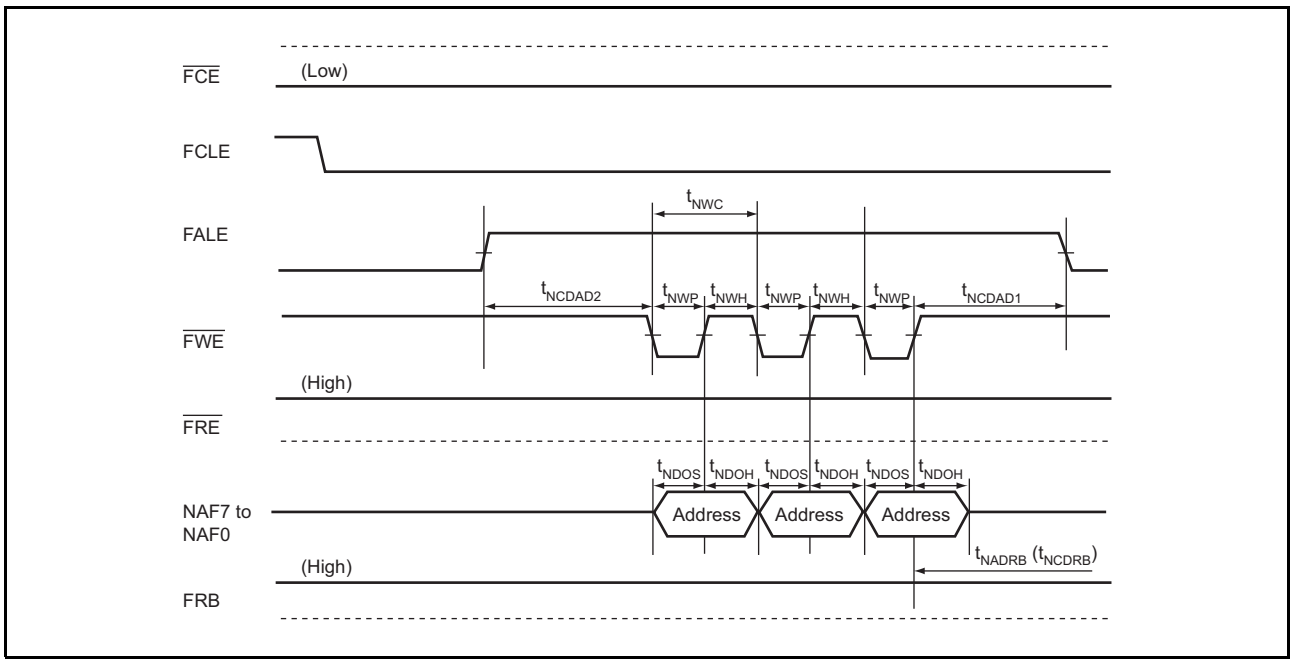


Figure 3.70 NAND Type Flash Memory Address Issuance Timing

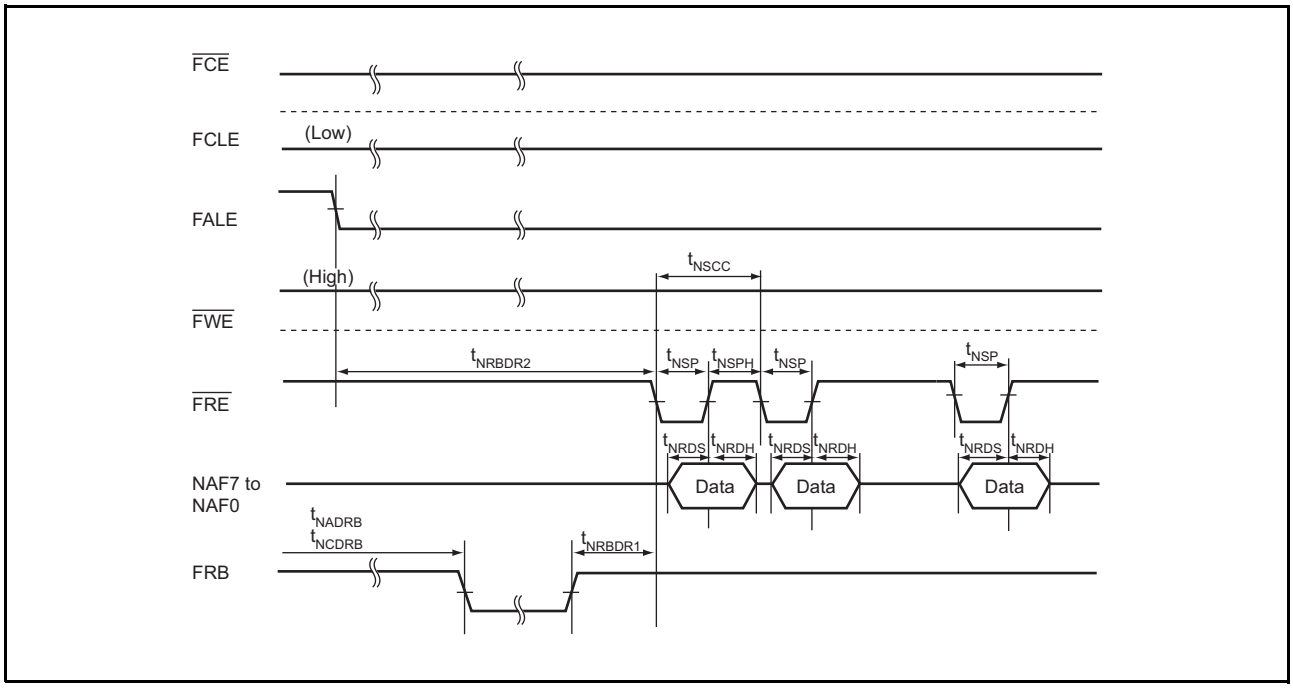


Figure 3.71 NAND Type Flash Memory Data Read Timing

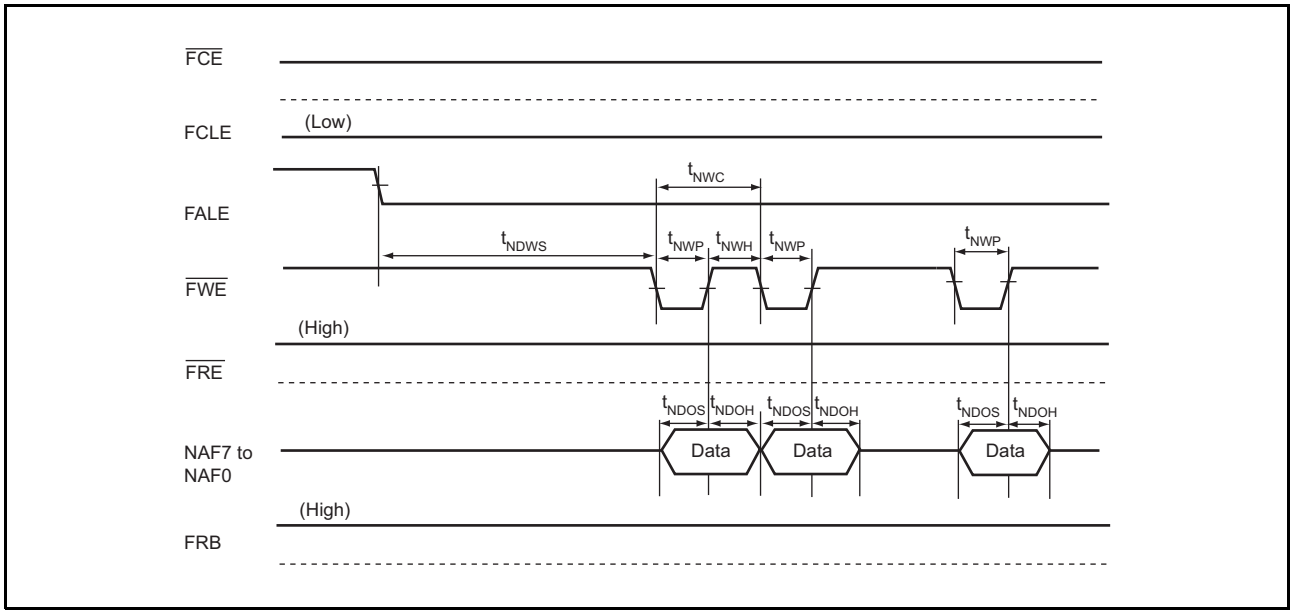


Figure 3.72 NAND Type Flash Memory Data Write Timing

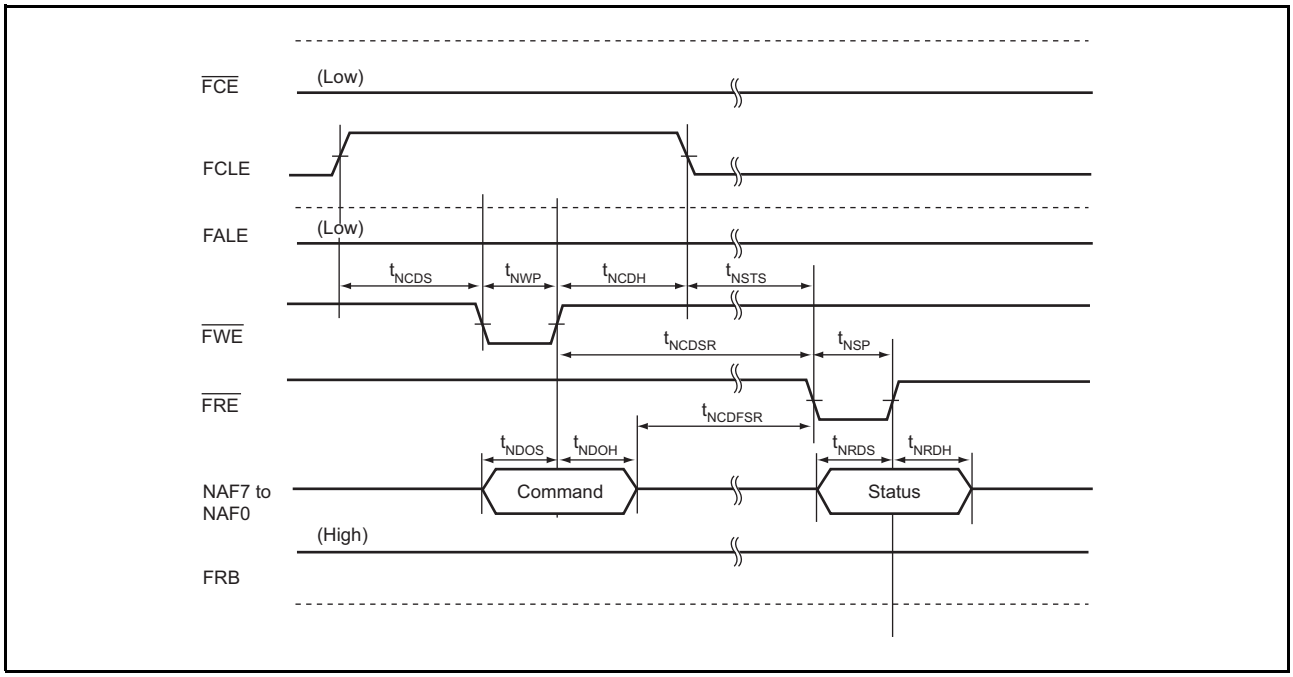


Figure 3.73 NAND Type Flash Memory Status Read Timing

3.4.18 USB 2.0 Host/Function Module Timing

Table 3.22 USB Transceiver Timing (Low-Speed)

Item	Symbol	Min.	Max.	Unit	Figure
Rise time	t_{LR}	75	300	ns	Figure 3.74
Fall time	t_{LF}	75	300	ns	
Rise/fall time lag	t_{LR}/t_{LF}	80	125	%	

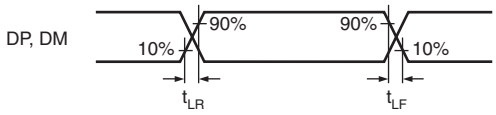


Figure 3.74 DP1, DP0, DM1, and DM0 Output Timing (Low-Speed)

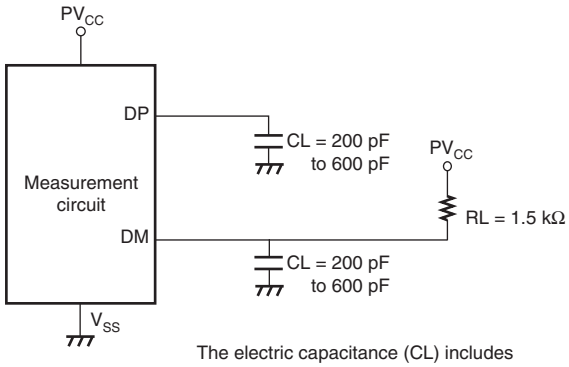


Figure 3.75 Measurement Circuit (Low-Speed)

Table 3.23 USB Transceiver Timing (Full-Speed)

Item	Symbol	Min.	Max.	Unit	Figure
Rise time	t_{FR}	4	20	ns	Figure 3.76
Fall time	t_{FF}	4	20	ns	
Rise/fall time lag	t_{FR}/t_{FF}	90	111.11	%	

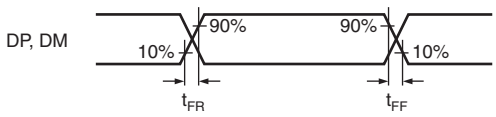
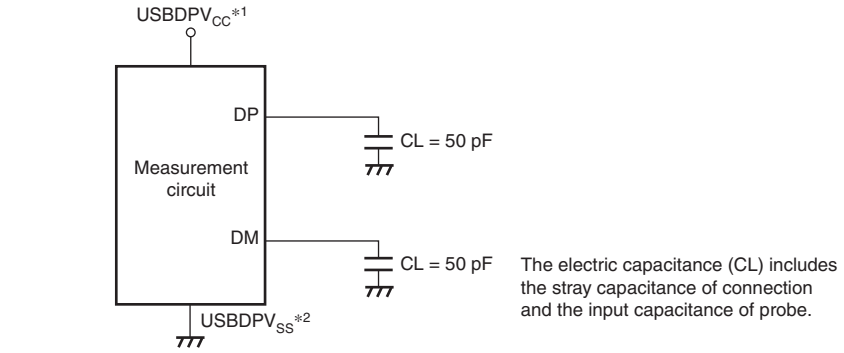


Figure 3.76 DP1, DP0, DM1, and DM0 Output Timing (Full-Speed)



Note 1. The PVcc pin is used in the products in BGA packages.
Note 2. The Vss pin is used in the products in BGA packages.

Figure 3.77 Measurement Circuit (Full-Speed)

Table 3.24 USB Transceiver Timing (High-Speed)

Item	Symbol	Min.	Max.	Unit	Figure
Rise time	t_{HSR}	500	—	ps	Figure 3.78
Fall time	t_{HSF}	500	—	ps	
Output driver resistance	Z_{HSDRV}	40.5	49.5	Ω	

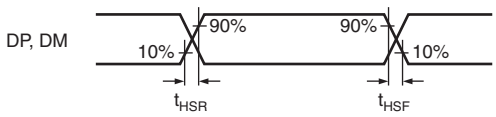
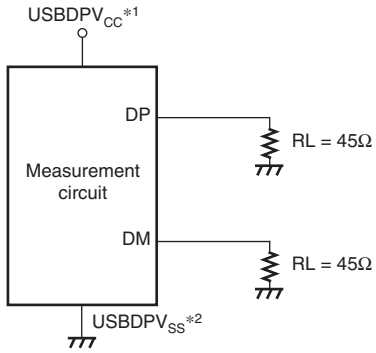


Figure 3.78 DP1, DP0, DM1, and DM0 Output Timing (High-Speed)



Note 1. The PVcc pin is used in the products in BGA packages.
Note 2. The Vss pin is used in the products in BGA packages.

Figure 3.79 Measurement Circuit (High-Speed)

3.4.19 Video Display Controller 5 Timing

Table 3.25 Video Display Controller 5 Timing

Item	Symbol	Min.	Max.	Unit	Figure
DV1_CLK and DV0_CLK input clock frequency	t_{Dcyc}	—	87.00	MHz	Figure 3.80
DV1_CLK and DV0_CLK input clock low pulse width	t_{WIL}	0.4	—	t_{Dcyc}	
DV1_CLK and DV0_CLK input clock high pulse width	t_{WIH}	0.4	—		
LCD1_EXTCLK and LCD0_EXTCLK input clock frequency	t_{Ecyc}	—	87.00	MHz	
LCD1_EXTCLK and LCD0_EXTCLK input clock low pulse width	t_{WIL}	0.4	—	t_{Ecyc}	
LCD1_EXTCLK and LCD0_EXTCLK input clock high pulse width	t_{WIH}	0.4	—		
LCD1_CLK and LCD0_CLK output clock frequency	t_{Lcyc}	—	87.00	MHz	Figure 3.81
LCD1_CLK and LCD0_CLK clock output low pulse width*1	t_{LOL}	t_{WIL} - 3.76	t_{WIL} + 3.76	ns	
LCD1_CLK and LCD0_CLK clock output high pulse width*1	t_{LOH}	t_{WIH} - 3.76	t_{WIH} + 3.76	ns	
LCD1_CLK and LCD0_CLK clock output low pulse width*2	t_{LOL}	$t_{Lcyc}/2$ - 1.12	$t_{Lcyc}/2$ + 1.12	ns	
LCD1_CLK and LCD0_CLK clock output high pulse width*2	t_{LOH}	$t_{Lcyc}/2$ - 1.12	$t_{Lcyc}/2$ + 1.12	ns	
LCD1_CLK and LCD0_CLK clock output rise time	t_{LOR}	—	3	ns	
LCD1_CLK and LCD0_CLK clock output fall time	t_{LOF}	—	3	ns	
Input data setup time	t_{VS}	2.5	—	ns	Figure 3.82
Input data hold time	t_{VH}	3.5	—	ns	
Output data delay time	t_{DD}	–3	3	ns	Figure 3.83

Note 1. This is the case when the video image clock or an external clock is selected as the clock for frequency division and the division ratio is set to 1/1.
Note 2. This is for cases other than when the video image clock or an external clock is selected as the clock for frequency division and the division ratio is set to 1/1.

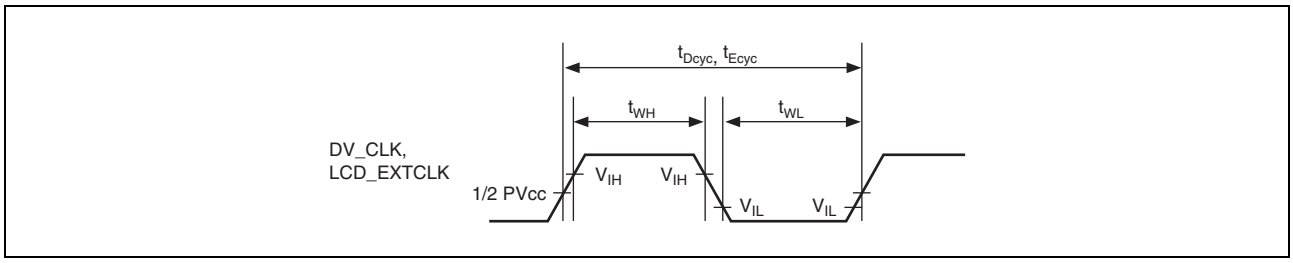


Figure 3.80 DV1_CLK, DV0_CLK, LCD1_EXTCLK, and LCD0_EXTCLK Clock Input Timing

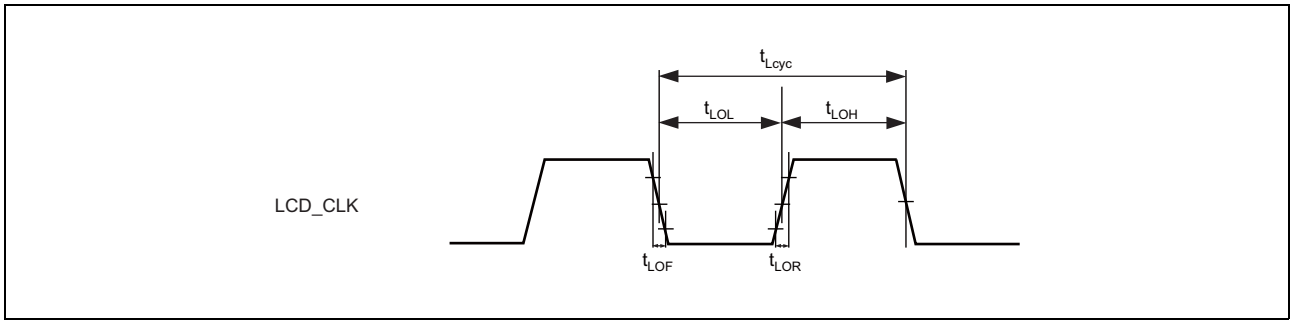


Figure 3.81 LCD1_CLK and LCD0_CLK Clock Output Timing

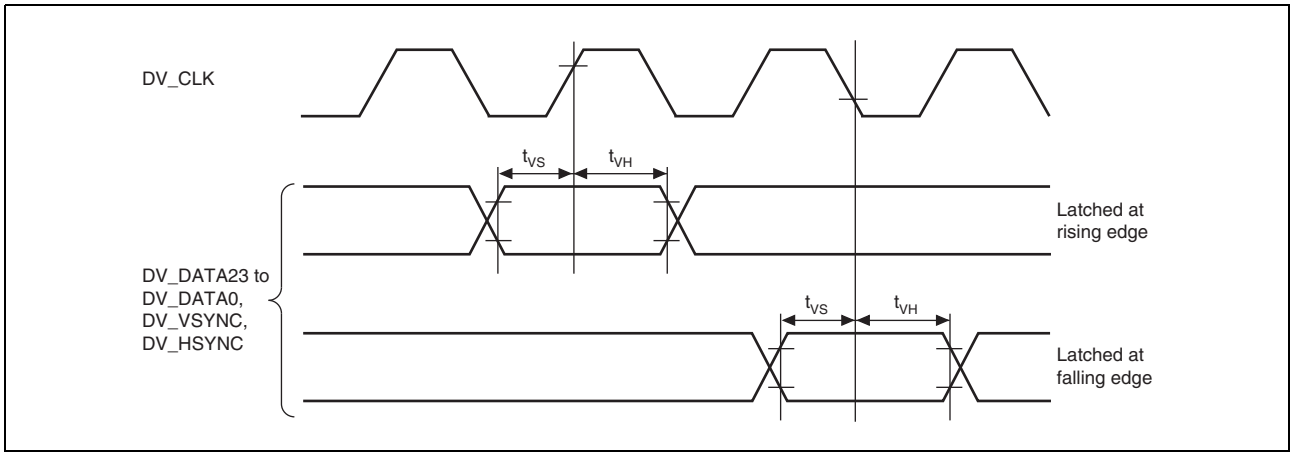


Figure 3.82 Video Input Timing

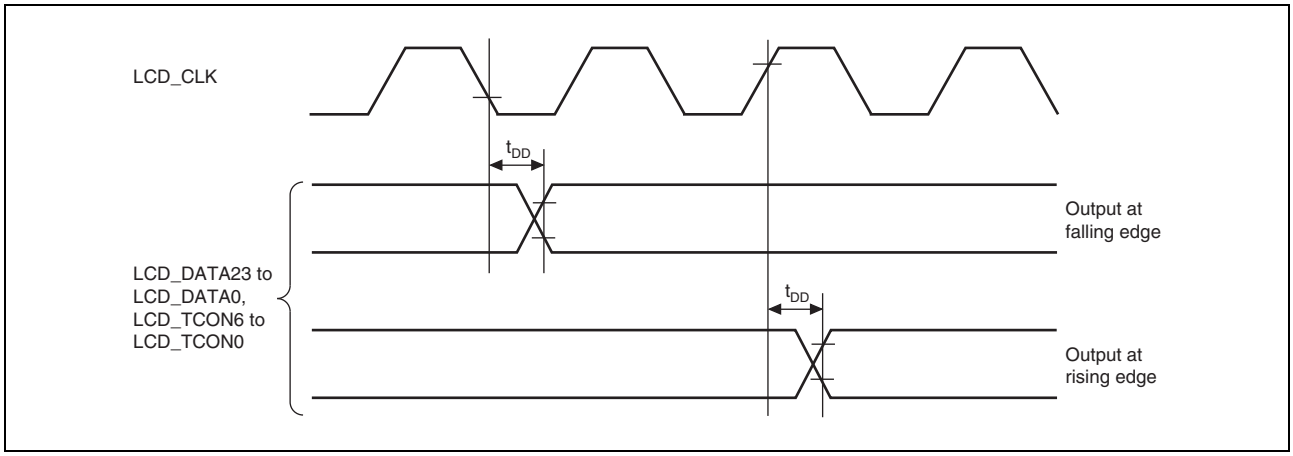


Figure 3.83 Display Output Timing

3.4.20 LVDS Timing

Table 3.26 LVDS Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Figure
Panel clock for LVDS output (LSI internal signal)	T	11.49 (87 MHz)	—	74.6 (13.4 MHz)	ns	Figure 3.84, Figure 3.85, and Figure 3.86
Rise time	LLHT		—	1.5	ns	
Fall time	LHLT	—	—	1.5	ns	
Transmitter Output Pulse Position for Bit1	TPPos1	-0.20	0	0.20	ns	
Transmitter Output Pulse Position for Bit0	TPPos0	T/7 - 0.20	T/7	T/7 + 0.20	ns	
Transmitter Output Pulse Position for Bit6	TPPos6	T × 2/7 - 0.20	T × 2/7	T × 2/7 + 0.20	ns	
Transmitter Output Pulse Position for Bit5	TPPos5	T × 3/7 - 0.20	T × 3/7	T × 3/7 + 0.20	ns	
Transmitter Output Pulse Position for Bit4	TPPos4	T × 4/7 - 0.20	T × 4/7	T × 4/7 + 0.20	ns	
Transmitter Output Pulse Position for Bit3	TPPos3	T × 5/7 - 0.20	T × 5/7	T × 5/7 + 0.20	ns	
Transmitter Output Pulse Position for Bit2	TPPos2	T × 6/7 - 0.20	T × 6/7	T × 6/7 + 0.20	ns	
TXOUT Inter Channel skew	TCCS	—	—	200	ps	

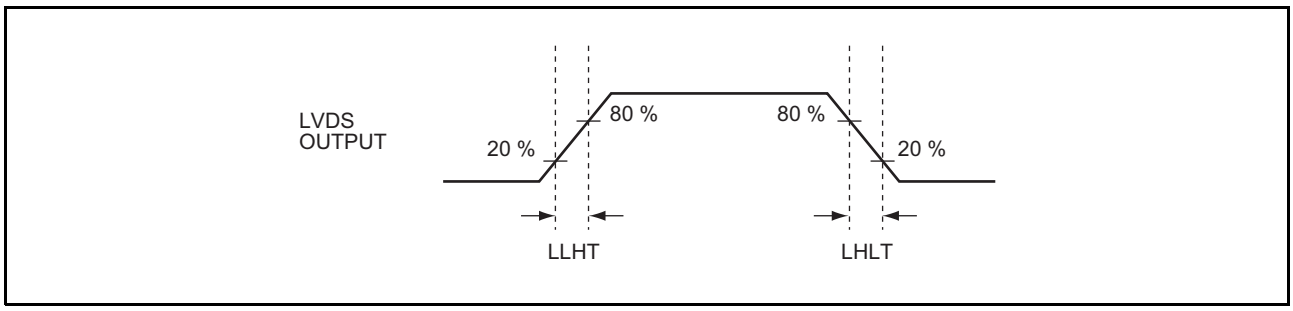


Figure 3.84 Transmitter LVDS Output Transition Time

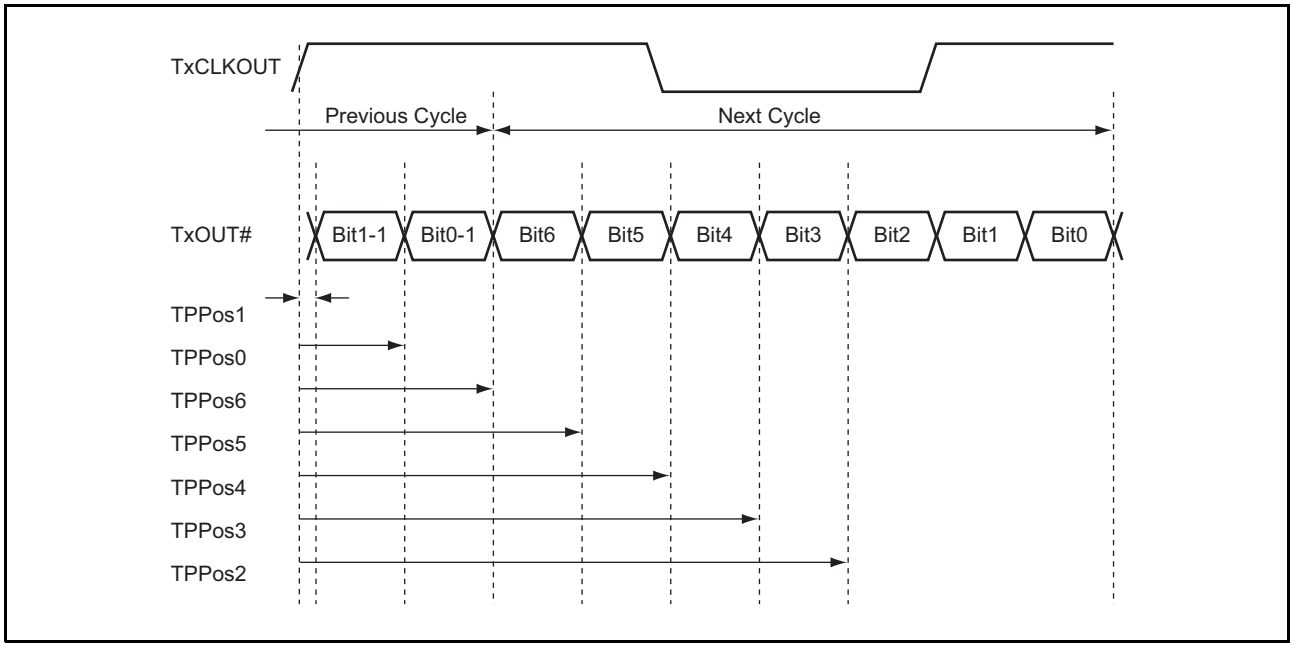


Figure 3.85 Transmitter LVDS Output Pulse Position Measurement

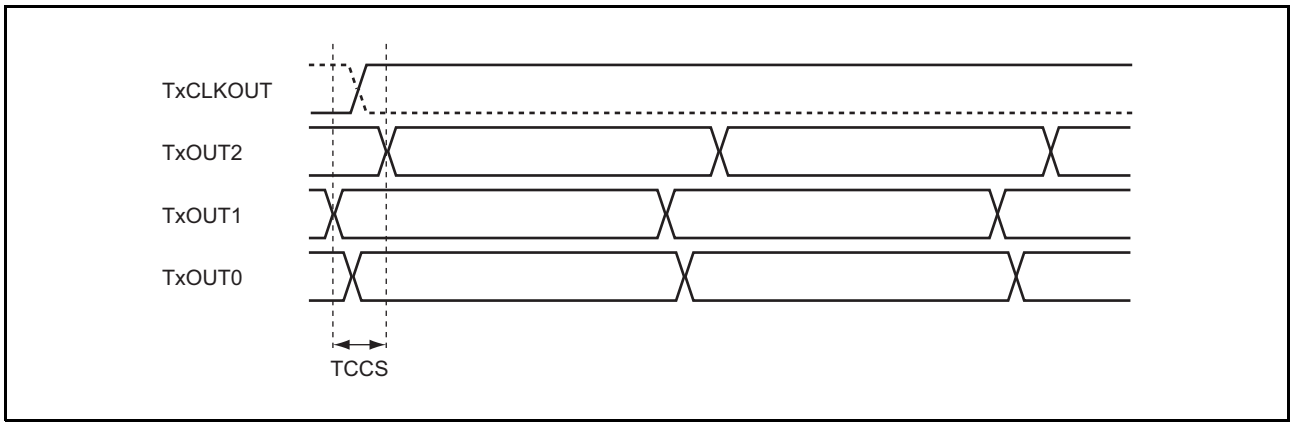


Figure 3.86 Transmitter Inter Channel Skew

3.4.21 Capture Engine Unit Module Signal Timing

Table 3.27 Capture Engine Unit Module Signal Timing

Item	Symbol	Min.	Max.	Unit	Figure
Vertical sync (VIO_VD) setup time	t_{VVDS}	2	—	ns	Figure 3.87
Vertical sync (VIO_VD) hold time	t_{VVDH}	3.5	—	ns	
Horizontal sync (VIO_HD) setup time	t_{VHDS}	2	—	ns	
Horizontal sync (VIO_HD) hold time	t_{VHDH}	3.5	—	ns	
Capture image data (VIO_D) setup time	t_{VDTS}	2	—	ns	
Capture image data (VIO_D) hold time	t_{VDTH}	3.5	—	ns	
Camera clock cycle	t_{VCYC}	—	87	MHz	
Camera clock high level	t_{VHW}	0.4 × t_{VCYC}	—	ns	
Camera clock low level	t_{VLW}	0.4 × t_{VCYC}	—	ns	
Field identification signal (VIO_FLD) setup time	t_{VFDS}	2	—	ns	
Field identification signal (VIO_FLD) hold time	t_{VFDH}	3.5	—	ns	

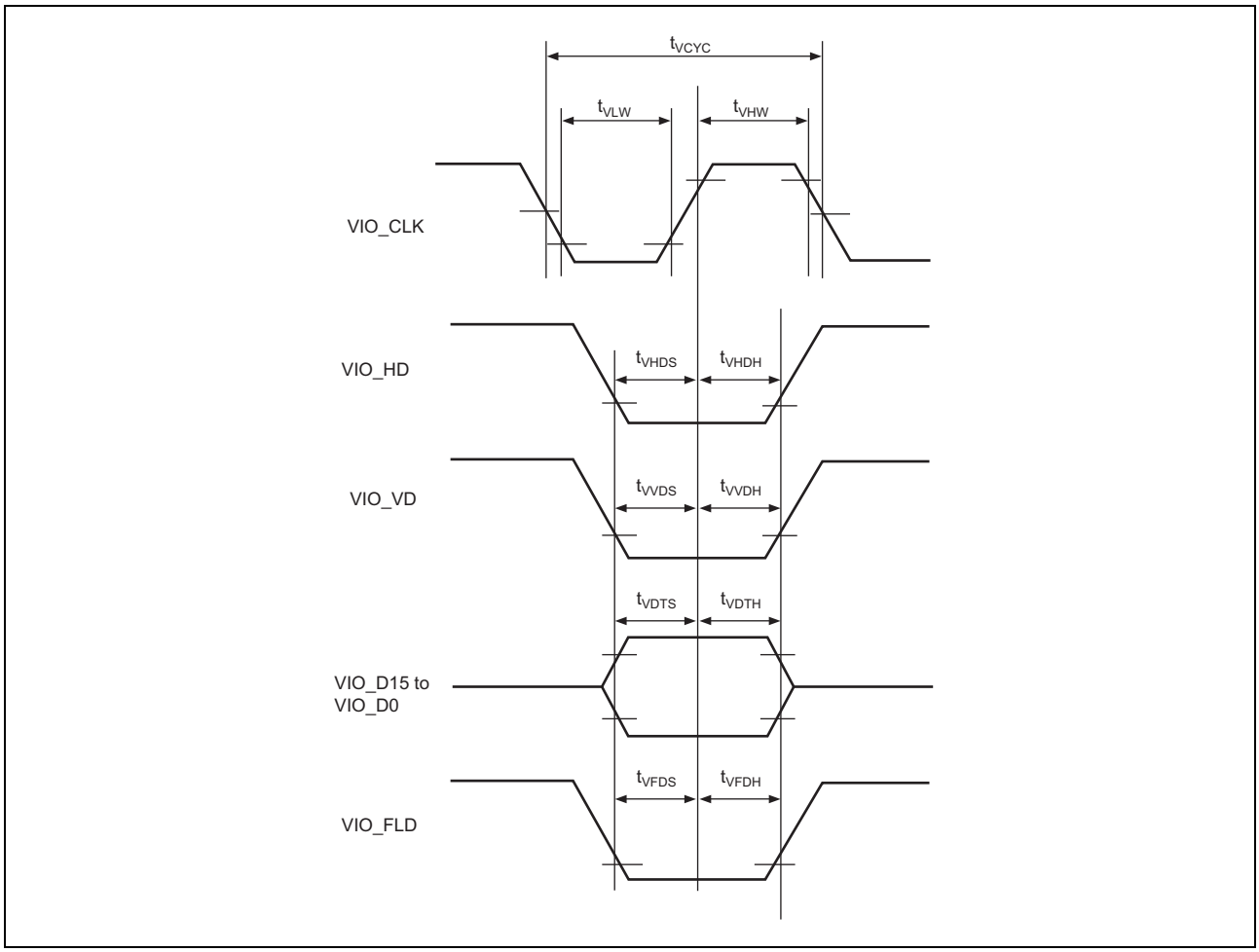


Figure 3.87 Capture Engine Unit Module Signal Timing

3.4.22 SD Host Interface Timing

Table 3.28 SD Host Interface Timing

Item	Symbol	Min.	Max.	Unit	Figure
SD_CLK clock cycle	t_{SDPP}	2 × t_{p1cyc}	—	ns	Figure 3.88
SD_CLK clock high level width	t_{SDWH}	0.4 × t_{SDPP}	—	ns	
SD_CLK clock low level width	t_{SDWL}	0.4 × t_{SDPP}	—	ns	
SD_CLK clock rise time	t_{SDLH}	—	3	ns	
SD_CLK clock fall time	t_{SDHL}	—	3	ns	
SD_CMD, SD_D3 to SD_D0 output data delay time (data transfer mode)	t_{SDODLY}	—	4	ns	
SD_CMD, SD_D3 to SD_D0 input data setup time	t_{SDISU}	7	—	ns	
SD_CMD, SD_D3 to SD_D0 input data hold time	t_{SDIH}	2	—	ns	

Note: • t_{p1cyc} indicates peripheral clock 1 (P1ϕ) cycle.

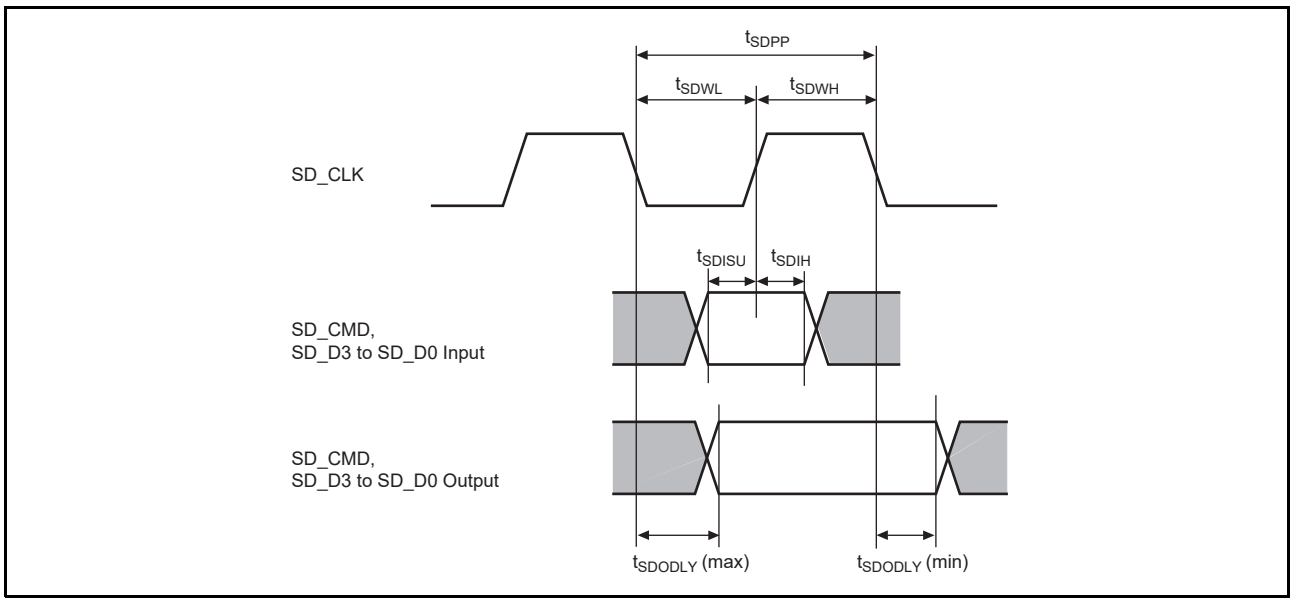


Figure 3.88 SD Host Interface

3.4.23 MMC Host Interface Timing

Table 3.29 MMC Host Interface Timing

Item	Symbol	Min.	Max.	Unit	Figure
MMC_CLK clock cycle	t_{MMCPP}	2 × t_{p1cyc}	—	ns	Figure 3.89
MMC_CLK clock high level width	t_{MMCWH}	6.5	—	ns	
MMC_CLK clock low level width	t_{MMCWL}	6.5	—	ns	
MMC_CLK clock rise time	t_{MMCLH}	—	3	ns	
MMC_CLK clock fall time	t_{MMCHL}	—	3	ns	
MMC_CMD, MMC_D7 to MMC_D0 output data delay time (data transfer mode)	$t_{MMCODLY}$	–6.5	6.5	ns	
MMC_CMD, MMC_D7 to MMC_D0 input data setup time	t_{MMCISU}	6.5	—	ns	
MMC_CMD, MMC_D7 to MMC_D0 input data hold time	t_{MMCIH}	2	—	ns	

Note: t_{p1cyc} indicates peripheral clock 1 (P1ϕ) cycle.

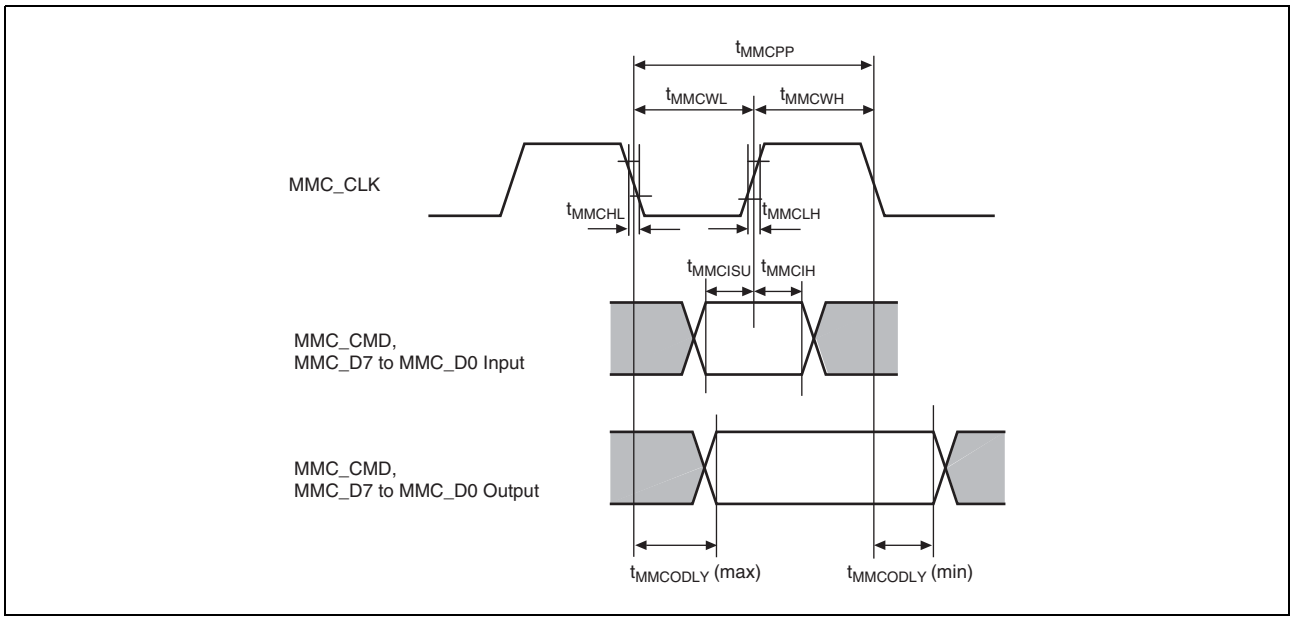


Figure 3.89 MMC Interface

3.4.24 General Purpose I/O Ports Timing

Table 3.30 General Purpose I/O Ports Timing

Item	Symbol	Min.	Max.	Unit	Figure
Output data delay time	t_{PORTD}	—	100	ns	Figure 3.90
Input data setup time	t_{PORTS}	100	—		
Input data hold time	t_{PORTH}	100	—		

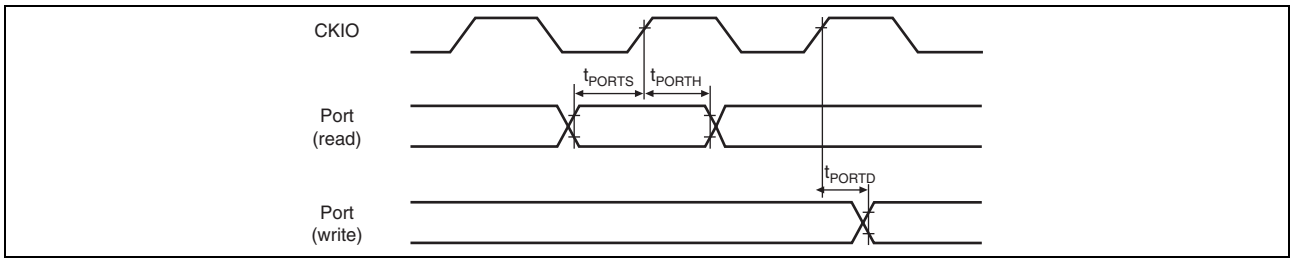


Figure 3.90 General I/O Ports Timing

3.4.25 Debugger Interface Timing

Table 3.31 Debugger Interface Timing

Item	Symbol	Min.	Max.	Unit	Figure
TCK cycle time	t_{TCKcyc}	50*1	—	ns	Figure 3.91
TCK high pulse width	t_{TCKH}	0.4	0.6	t_{TCKcyc}	
TCK low pulse width	t_{TCKL}	0.4	0.6	t_{TCKcyc}	
TDI setup time	t_{TDIS}	10	—	ns	Figure 3.92
TDI hold time	t_{TDIH}	10	—	ns	
TMS/SWDIO setup time	t_{TMSS}	10	—	ns	
TMS/SWDIO hold time	t_{TMSH}	10	—	ns	
SWDIO delay time	t_{SWDO}	—	16	ns	
TDO delay time	t_{TDOD}	—	16	ns	
Capture register setup time	t_{CAPTS}	10	—	ns	Figure 3.93
Capture register hold time	t_{CAPTH}	10	—	ns	
Update register delay time	$t_{UPDATED}$	—	20	ns	
Trace clock cycle	t_{TCYC}	30*2	—	ns	Figure 3.94 Output load: 15 pF
Trace clock high level	t_{THC}	12	—	ns	
Trace clock low level	t_{TLC}	12	—	ns	
Trace data delay time	t_{TDT}	3	0.3 × t_{TCYC} + 3	ns	

Note 1. Should be greater than the peripheral clock 0 (P0ϕ) cycle time.
Note 2. Generated by dividing the frequency of the peripheral clock (P1ϕ) by 2.

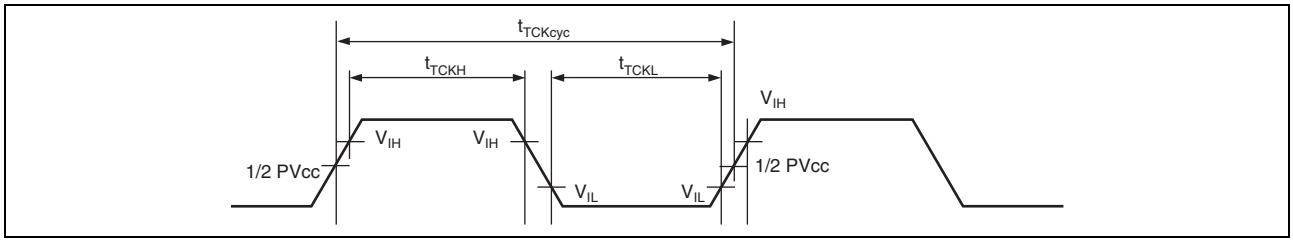


Figure 3.91 TCK Input Timing

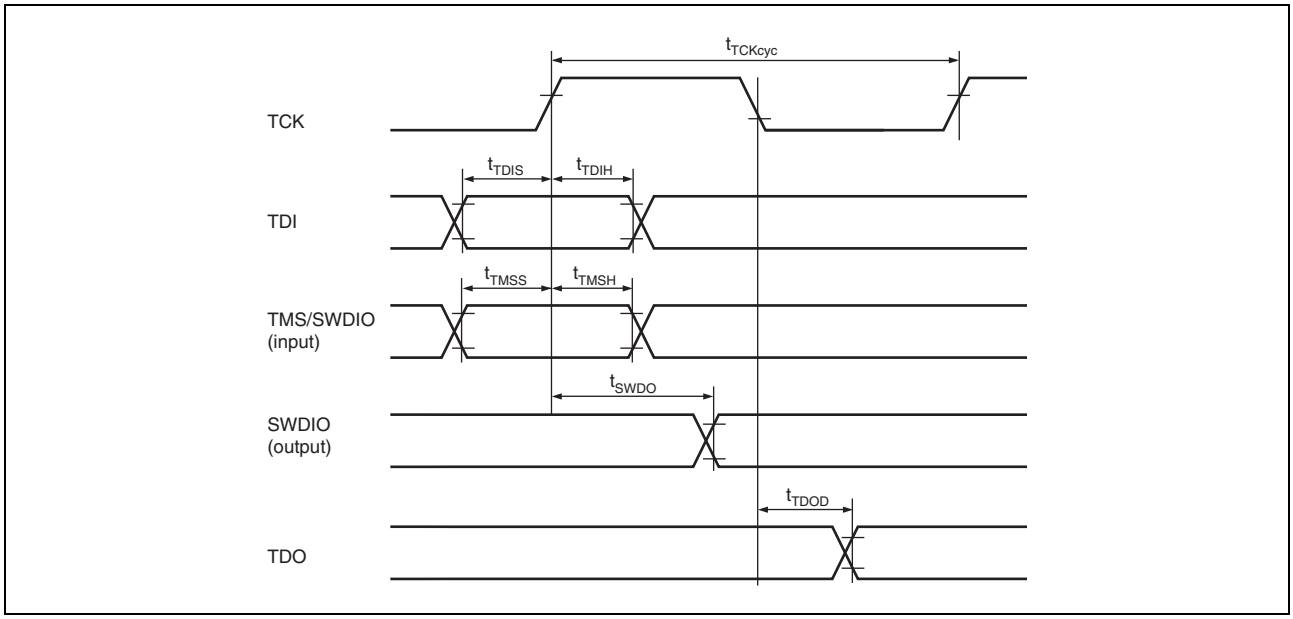


Figure 3.92 Data Transfer Timing

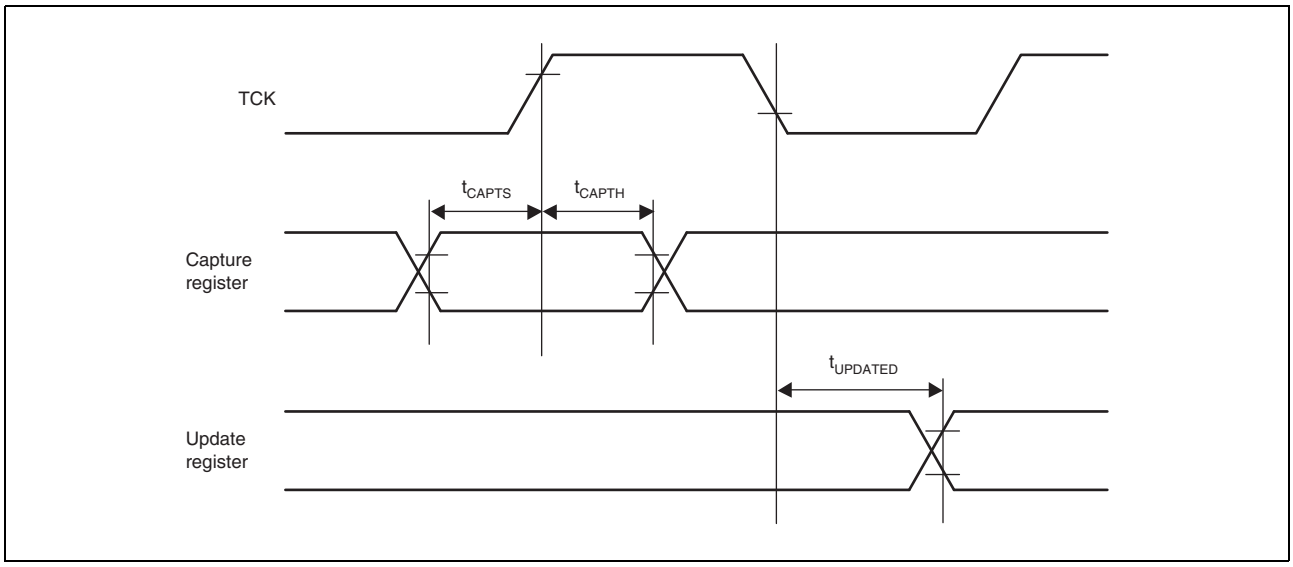


Figure 3.93 Boundary Scan Input/Output I/O Timing

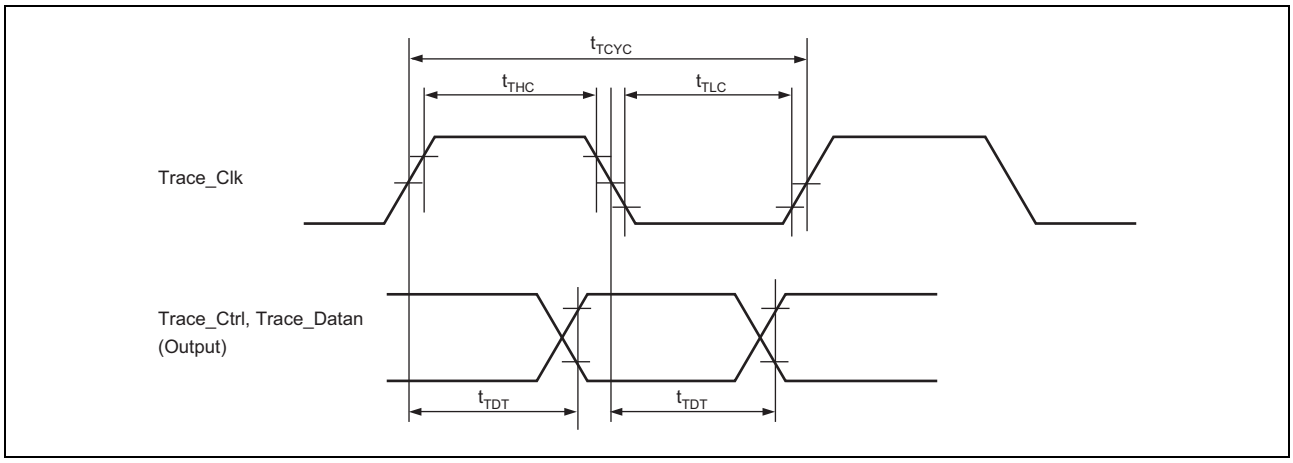


Figure 3.94 Trace Interface Timing

3.4.26 AC Characteristics Measurement Conditions

- I/O signal reference level: $PV_{CC}/2$, the minimum values of V_{IH}, $V_{T}+$, and V_{OH}, and the maximum values of V_{IL}, $V_{T}-$, and V_{OL} (refer to the individual timing chart)
- Input pulse level: PV_{CC}
- Input rise and fall times: 1 ns

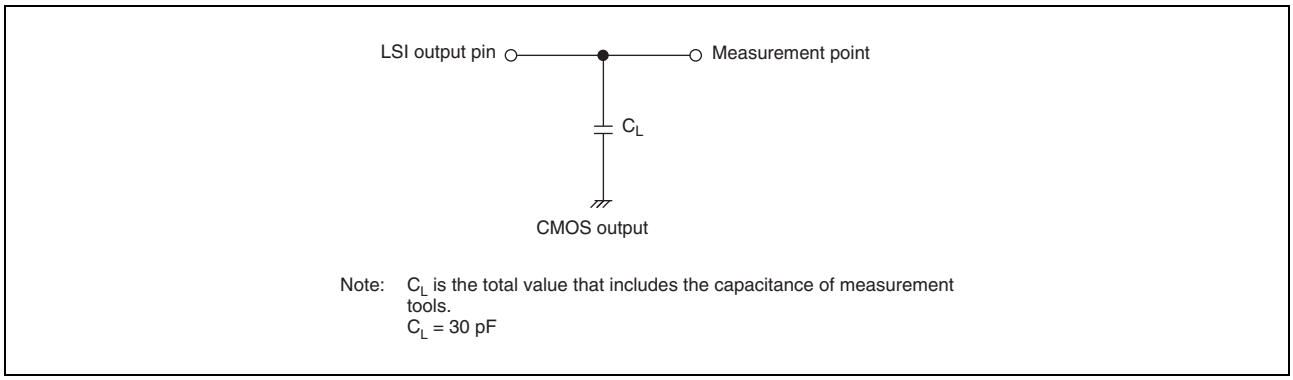


Figure 3.95 Output Load Circuit

3.5 A/D Converter Characteristics

Conditions: V_{CC} = $USBDV_{CC}$ = $USBUV_{CC}$ = 1.10 to 1.26 V, PV_{CC} = $USBDPV_{CC}$ = 3.0 to 3.6 V,
$PLLV_{CC}$ = 1.10 to 1.26 V, AV_{CC} = 3.0 to 3.6 V, $USBAPV_{CC}$ = 3.0 to 3.6 V, $USBAV_{CC}$ = 1.10 to 1.26 V,
$VDAV_{CC}$ = 3.0 to 3.6 V, $LVDSAPV_{CC}$ = 3.0 to 3.6 V, $LVDSPLLV_{CC}$ = 1.10 to 1.26 V,
V_{SS} = AV_{SS} = $USBDV_{SS}$ = $USBAV_{SS}$ = $USBDPV_{SS}$ = $USBAPV_{SS}$ = $USBUV_{SS}$ = $VDAV_{SS}$ = $LVDSAPV_{SS}$ = 0 V,
Ta = –40 to 85 °C, Tj = –40 to 125 °C

Note: Products in BGA packages do not have $USBDV_{CC}$, $USBUV_{CC}$, $USBDPV_{CC}$, $USBDV_{SS}$, $USBAV_{SS}$, $USBDPV_{SS}$, $USBAPV_{SS}$, $USBUV_{SS}$, and $LVDSAPV_{SS}$ pins.

Table 3.32 A/D Converter Characteristics

Item		Min.	Typ.	Max.	Unit
Resolution		12	12	12	bits
Conversion time	12-bit	5	—	—	µs
	10-bit				
Analog input capacitance		—	—	20	pF
Permissible signal-source impedance		—	—	3	kΩ
DNL	12-bit	—	—	±1.0	LSB
	10-bit	—	—	±1.0	LSB
INL	12-bit	—	—	±4.0	LSB
	10-bit	—	—	±4.0	LSB
Offset error	12-bit	—	—	±8.0	LSB
	10-bit	—	—	±2.0	LSB
Full-scale error	12-bit	—	—	±8.0	LSB
	10-bit	—	—	±2.0	LSB
Absolute accuracy	12-bit	—	—	±11.0	LSB
	10-bit	—	—	±5.0	LSB

3.6 Video Characteristics of A/D Converter for the Input of Video Signals

Conditions: V_{CC} = $USBDV_{CC}$ = $USBUV_{CC}$ = 1.10 to 1.26 V, PV_{CC} = $USBDPV_{CC}$ = 3.0 to 3.6 V, $PLLV_{CC}$ = 1.10 to 1.26 V, AV_{CC} = 3.0 to 3.6 V, $USBAPV_{CC}$ = 3.0 to 3.6 V, $USBAV_{CC}$ = 1.10 to 1.26 V, $VDAV_{CC}$ = 3.0 to 3.6 V, $LVDSAPV_{CC}$ = 3.0 to 3.6 V, $LVDSPLLV_{CC}$ = 1.10 to 1.26 V, V_{SS} = AV_{SS} = $USBDV_{SS}$ = $USBAV_{SS}$ = $USBDPV_{SS}$ = $USBAPV_{SS}$ = $USBUV_{SS}$ = $VDAV_{SS}$ = $LVDSAPV_{SS}$ = 0 V, Ta = –40 to 85 °C, Tj = –40 to 125 °C

Note: Products in BGA packages do not have $USBDV_{CC}$, $USBUV_{CC}$, $USBDPV_{CC}$, $USBDV_{SS}$, $USBAV_{SS}$, $USBDPV_{SS}$, $USBAPV_{SS}$, $USBUV_{SS}$, and $LVDSAPV_{SS}$ pins.

Table 3.33 Characteristics of A/D Converter for the Input of Video Signals (Reference Voltage)

Item	Min.	Typ.	Max.	Unit	Test Conditions
Reference voltage (VRP)	—	1.7	—	V	
Reference voltage (VRM)	—	0.9	—	V	

Table 3.34 Characteristics of A/D Converter for the Input of Video Signals (Clamping)

Item	Min.	Typ.	Max.	Unit	Test Conditions
Clamping voltage level	—	0.6	—	V	
Sink current	—	4.0	—	µA	
Source current	—	0.2	—	mA	

Table 3.35 Characteristics of A/D Converter for the Input of Video Signals (LPF)

Item	Min.	Typ.	Max.	Unit	Test Conditions
Cutoff frequency	- 3	—	—	dB	5.1 MHz

Table 3.36 Characteristics of A/D Converter for the Input of Video Signals (PGA)

Item	Min.	Typ.	Max.	Unit	Test Conditions
Number of gain steps	—	64	—	step	
Gain step width	—	0.1	—	dB	
Minimum gain	—	0	—	dB	
Maximum gain	—	6.02	—	dB	

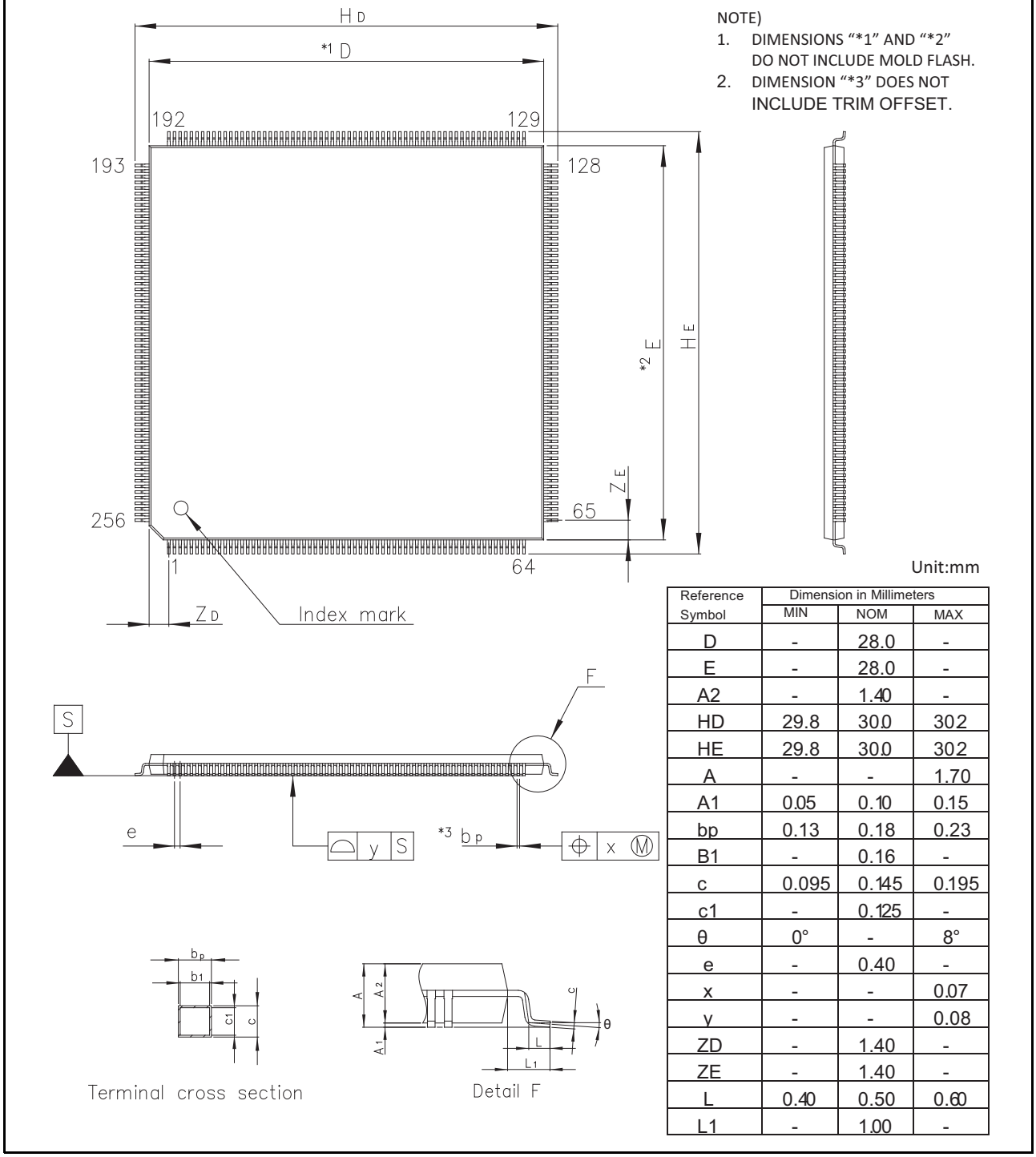
Table 3.37 Characteristics of A/D Converter for the Input of Video Signals (ADC)

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	—	10	—	bit	
A/D conversion range	—	1.6	—	Vpp	(VRP – VRM) × 2
Integral linearity error	—	—	± 5.0	LSB	ADC + PGA fs = 27 MHz
Differential linearity error	—	—	± 2.0	LSB	ADC + PGA fs = 27 MHz
S/N	—	54*	—	dB	fin = 1 MHz, fs = 27 MHz PGA_GAIN = 000000
S/(N + D)	—	51*	—	dB	fin = 1 MHz, fs = 27 MHz PGA_GAIN = 000000
Time for return from power saving mode	—	1	—	ms	

Note: * Reference value.

4. Package Dimensions

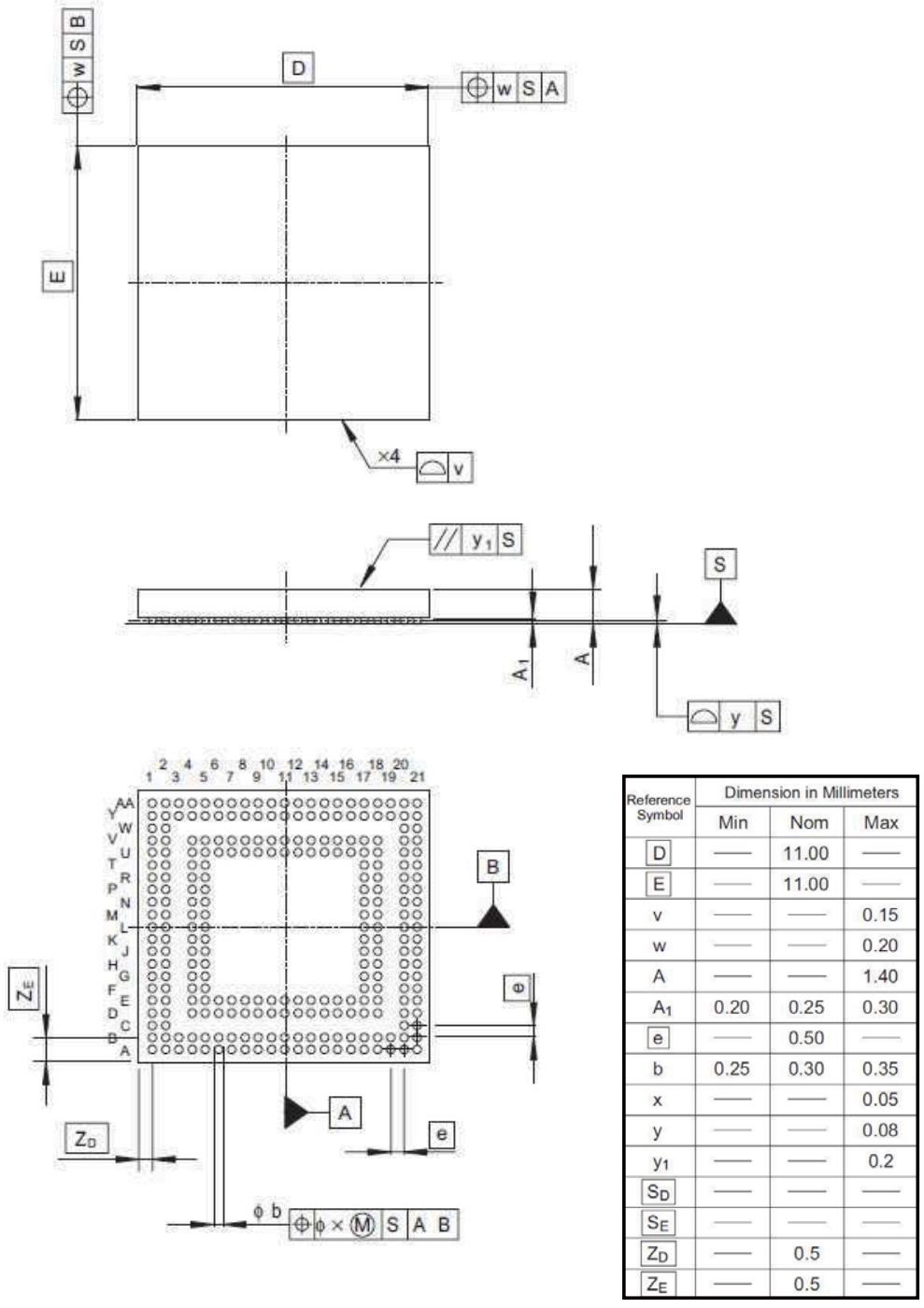
JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-LQFP256-2828-0.40	PLQP0256LB-A	FP-256B/FP-256BV	2.7g



Reference Symbol	Dimension in Millimeters		
	MIN	NOM	MAX
D	-	28.0	-
E	-	28.0	-
A2	-	1.40	-
HD	29.8	30.0	30.2
HE	29.8	30.0	30.2
A	-	-	1.70
A1	0.05	0.10	0.15
bp	0.13	0.18	0.23
B1	-	0.16	-
c	0.095	0.145	0.195
c1	-	0.125	-
θ	0°	-	8°
e	-	0.40	-
x	-	-	0.07
y	-	-	0.08
ZD	-	1.40	-
ZE	-	1.40	-
L	0.40	0.50	0.60
L1	-	1.00	-

Figure 4.1 Dimensions of 256-Pin QFP Package

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-LFBGA256-11x11-0.50	PLBG0256KA-B	-	0.3

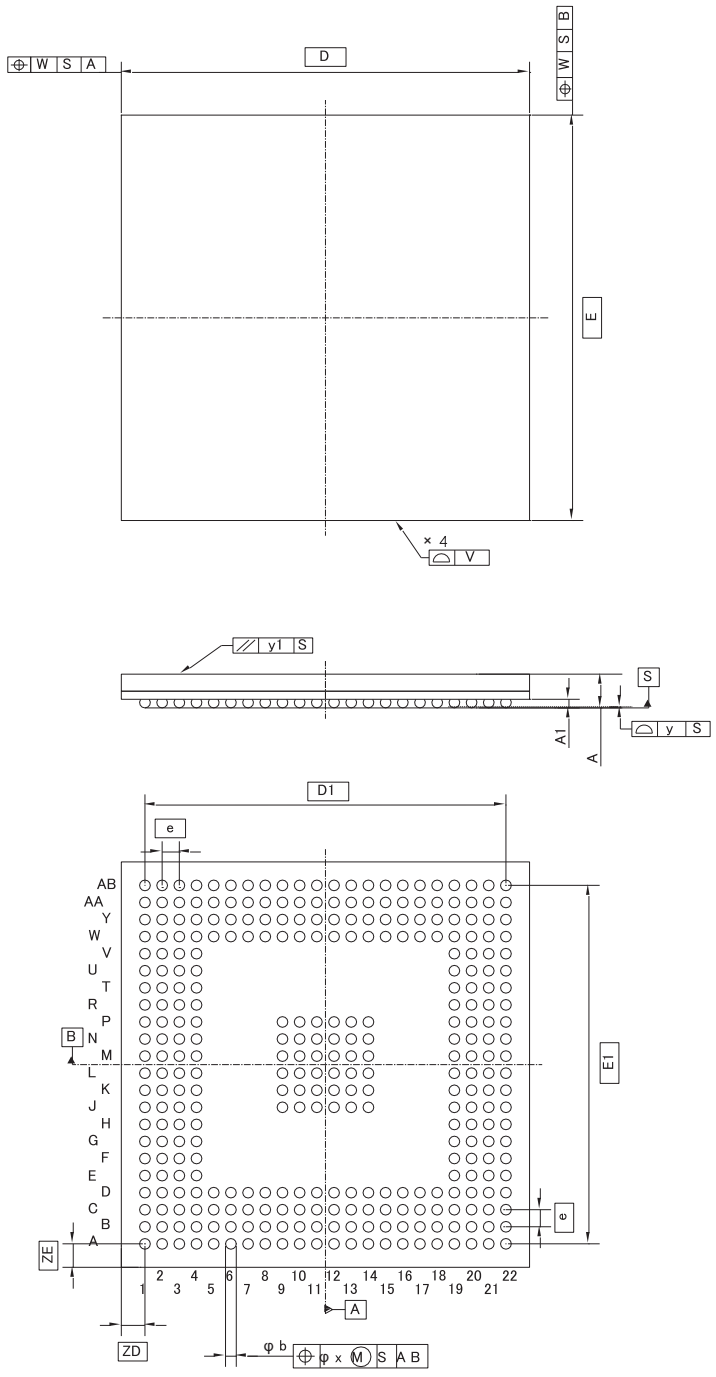


Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	11.00	—
E	—	11.00	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.40
A_1	0.20	0.25	0.30
e	—	0.50	—
b	0.25	0.30	0.35
x	—	—	0.05
y	—	—	0.08
y_1	—	—	0.2
S_D	—	—	—
S_E	—	—	—
Z_D	—	0.5	—
Z_E	—	0.5	—

Figure 4.2 Dimensions of 256-Pin BGA Package

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-FBGA324-19x19-0.80	PRBG0324GA-A	-	1.2

Unit:mm



Reference Symbol	Dimension in Millimeters		
	Min	Mon	Max
D	—	19.00	—
D1	—	16.80	—
E	—	19.00	—
E1	—	16.80	—
v	—	—	0.15
w	—	—	0.20
e	—	0.80	—
A	—	1.76	2.10
A1	0.35	0.40	0.45
b	0.45	0.50	0.55
x	—	—	0.08
y	—	—	0.10
y1	—	—	0.20
ZD	—	1.10	—
ZE	—	1.10	—

Figure 4.3 Dimensions of 324-Pin BGA Package

REVISION HISTORY	RZ/A1H Group, RZ/A1M Group Datasheet

Rev.	Date	Description	
		Page	Summary
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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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