RRW43110

Intelligent Synchronous Rectifier Controller Optimized for High-Power-Density Wide Output Voltage Range Applications

Description

The RRW43110 is an advanced synchronous rectifier (SR) controller that works with both MOSFET and GaN devices. With Renesas' proprietary lossless V_{DS} sensing technology, the RRW43110 is optimized to work with multiple topologies, such as half-wave LLC (HWLLC), and other half-bridge resonant converters, up to 300 kHz switching frequency.

The device works with an external power-switch device to replace the main rectifying diode on the secondary side of the power converter to achieve high efficiency. This versatility makes the RRW43110 ideal for the newest high power density power supply applications (3 W/cm^3) up to 500 W.

The RRW43110 has the ability to support a wide output voltage range up to 48 V or higher under all operating conditions to accommodate a wide array of power supply applications.

Moreover, the RRW43110 supports both low-power mode and sleep mode, which optimizes the efficiency at light load and no-load conditions.

Features

- Optimized to support topologies such as HWLLC, and other half-bridge resonant converters
- Support operating switching frequency up to 300 kHz
- Optimized lossless V_{DS}-based SR sensing
- Supports wide output voltage range up to 48 V or higher
- Supports both high-side and low-side synchronous rectification topologies
- Intelligent low power management achieves ultra-low no-load operating current
- 6-pin SOT23 package, supports compact system design

Applications

- Rapid-charging AC/DC adapters for smart phones, tablets, notebooks, and other portable devices.
- Power tools
- Electric bicycles
- Industrial power
- Home appliance
- Motor control

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1. Overview

1.1 Block Diagram

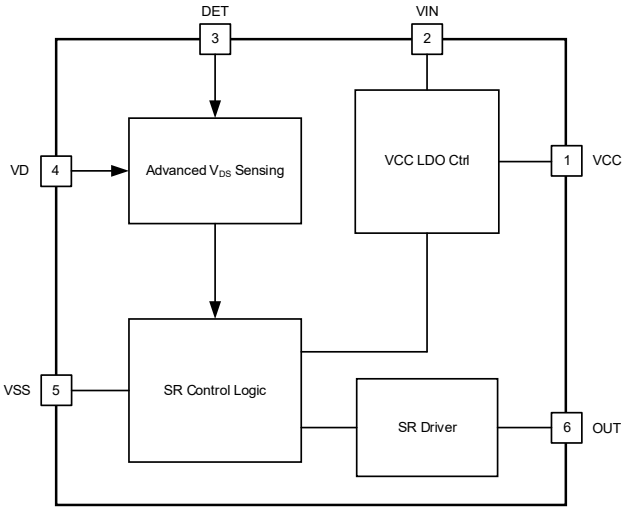


Figure 1. RRW43110 Functional Block Diagram

1.2 Typical Application

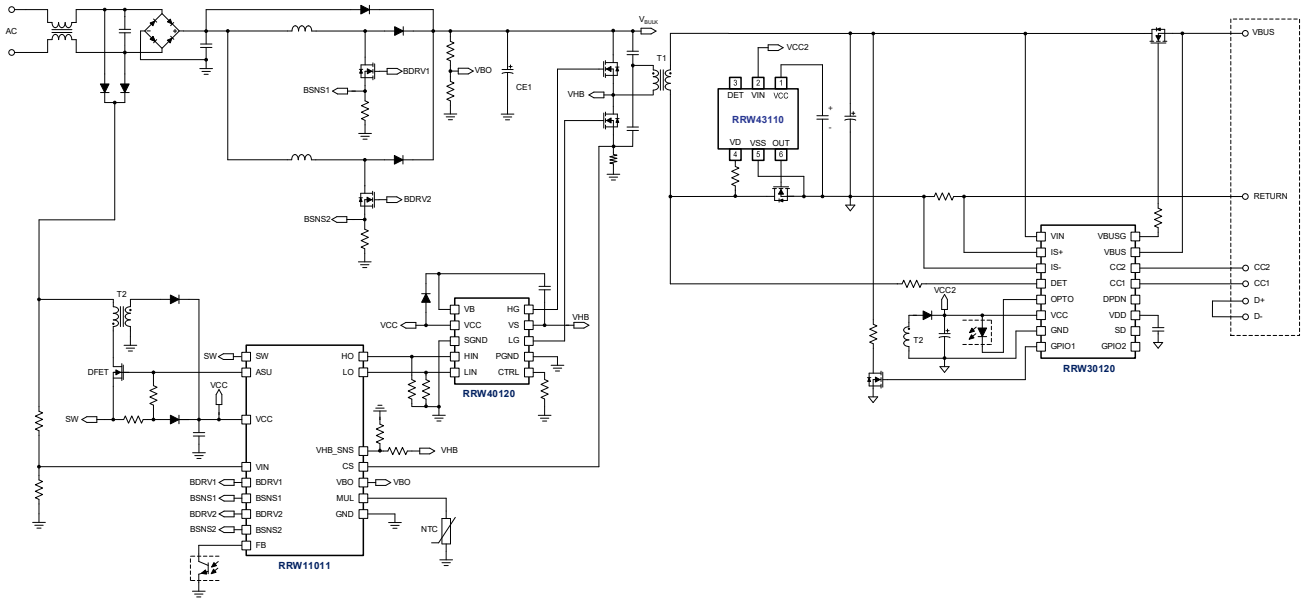


Figure 2. RRW43110 Application Circuit with RRW11011, RRW40120 and RWW30120

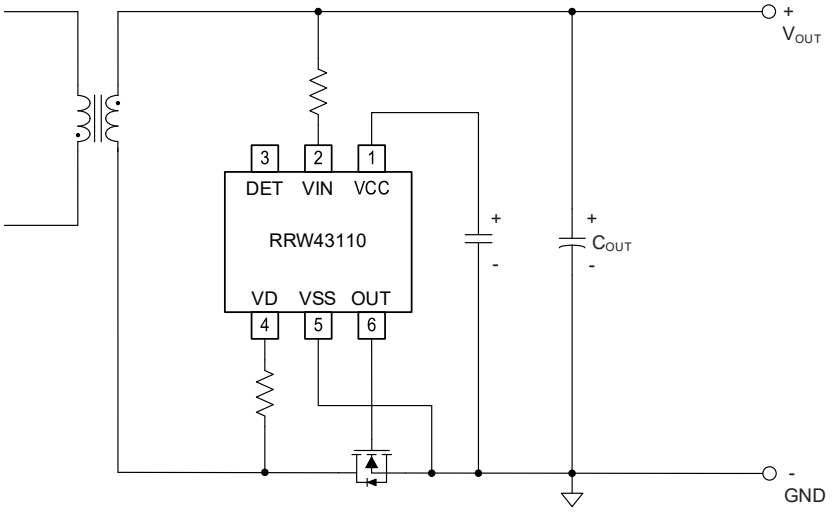


Figure 3. RRW43110 for SR Power Switch V_{DS} < 145V and Low-Side SR Applications with Direct VIN LDO Charging

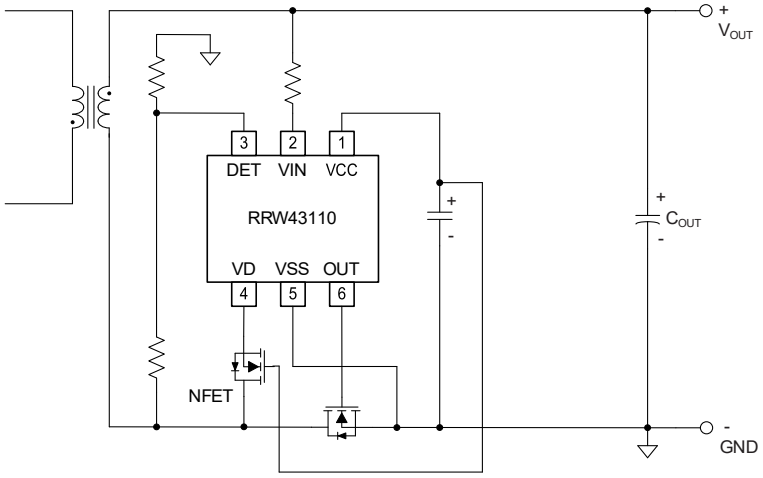


Figure 4. RRW43110 for SR Power Switch V_{DS} > 145V and Low-Side SR Applications with Direct VIN LDO Charging

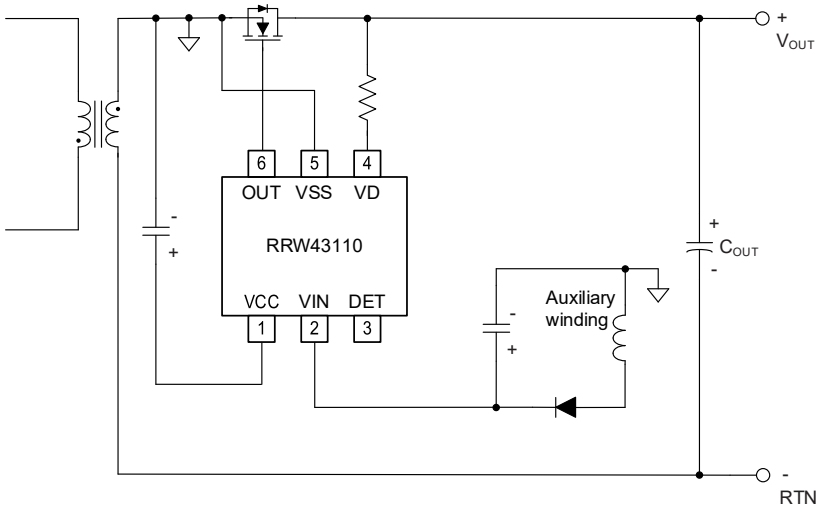


Figure 5. RRW43110 for SR Power Switch V_{DS} < 145V and High-Side SR Application with Auxiliary Winding Charging

2. Pin Information

2.1 Pin Assignments

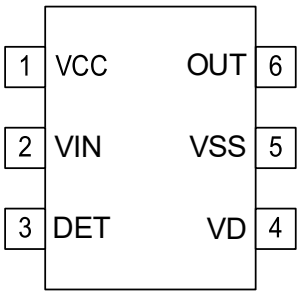


Figure 6. Top View 6-Pin SOT23 Package

2.2 Pin Descriptions

Pin Number	Pin Name	Type	Description
1	VCC	Power input	It provides voltage supply for internal logic circuit and SR power switch driver. Connect this pin to a capacitor.
2	VIN	Analog input	Connected to the output capacitor positive node or auxiliary winding output positive node.
3	DET	Analog input	It provides adaptive V_{DS} sensing function for $V_{DS} \geq 145$ V applications
4	VD	Analog input	It provides adaptive V_{DS} sensing function for $V_{DS} < 145$ V applications
5	VSS	IC GND	IC Ground
6	OUT	Analog output	Synchronous rectifier power switch gate driver

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Symbol	Minimum	Maximum	Unit
OUT pin voltage	V_G	-0.6	10	V
OUT pin peak pulldown current	I_G	-3		A
VCC voltage	V_{VCC}	-0.6	10	V
VD pin voltage	V_{VD}	-1.5	145	V
VIN pin voltage	V_{VIN}	-0.6	60	V
DET pin voltage	V_{DET}	-0.6	5.5	V
Storage Temperature Range	T_{ST}	-65	150	°C
ESD rating per JEDEC JESD22-A114		-	2000	V

3.2 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
VCC voltage	3	V_{VCC_OVP}	V
VD pin voltage	-1	135	V
VIN pin voltage	4	58	V
DET pin voltage	0	5	V
Junction temperature	-40	125	°C

3.3 Thermal Specifications

Parameter	Symbol	Condition	Typical Value	Unit
Thermal Resistance	θ_{JA}	Junction to ambient	208	°C/W

3.4 Electrical Specifications

V_{VCC} = 7.5 V, -40 °C ≤ T_A ≤ 85 °C, unless otherwise specified.

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
VCC Section						
Upper limit of VCC pin operating voltage	V_{VCC_UPPER}	Depending on product options		7.5/ 6		V
Operation current	I_{VCC}	V_{VCC} = 7.5 V, 100 kHz, with 2.2 µF cap		3.1		mA
		V_{VCC} = 7.5 V, 100 kHz, OUT pin floating		2.1		mA
Low power mode current	I_{VCC_LP}	Low power mode, V_{VCC} = 7.5 V, OUT pin floating		2.0		mA
Sleep mode current, no load	I_{VCC_SLEEP}	Sleep mode, V_{VCC} = 7.5 V, OUT pin floating		210		µA
V_{VCC} POR threshold	V_{VCC_POR}			3.3		V
V_{VCC} UVLO threshold	V_{VCC_ULVO}			2.75		V
V_{VCC} OVP protection threshold	V_{VCC_OVP}	V_{VCC} = 7.5 V		114% * V_{VCC_UPPER}		V
		V_{VCC} = 6 V		118% * V_{VCC_UPPER}		V
SR Gate Driver Section						
Gate pull-up resistor	R_{UP}			5.7		Ω
Gate pull-down resistor	R_{DOWN}			0.64		Ω
Maximum pull down current	$I_{PULLDOWN}$	V_{VCC} = 6 V, C_L = 4.5 nF		2.4		A
Gate high voltage	V_{G_H}			V_{CC} - 0.2		V
Gate low voltage	V_{G_L}				0.2	V
Gate rising time	t_{G_RISE}	10% V to 90% V, C_L = 4.5 nF (V_{VCC} = 5 V)			128	ns
Turn on propagation delay	t_{ON_DELAY}	Gate signal to 50% V, C_L = 4.5 nF (V_{VCC} = 5 V)			88	ns
Gate falling time	t_{G_FALL}	90% V to 10% V, C_L = 4.5 nF (V_{VCC} = 5 V)			22	ns
Turn off propagation delay	t_{OFF_DELAY}	Gate signal to 50% V C_L = 4.5 nF (V_{VCC} = 5 V)			25	ns
SR turn-on threshold	V_{ON_TH}	Depending on product options		-120/ -230		mV
SR turn-off threshold	V_{OFF_TH}			-3		mV
Minimum on-time	t_{ON_MIN}	Depending on product options		0.3/0.4/0.6/1		µs

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.
2. Compliance to limits is assured by characterization and design.

4. Functional Description

The RRW43110 is a synchronous rectifier controller that uses Renesas' proprietary lossless sensing technology to monitor the SR power device drain-to-source (V_{DS}) to determine the driver timing and regulates its gate voltage level.

The RRW43110 is optimized for high efficiency operation of a wide output voltage range applications up to 48 V or higher with minimum external components.

The RRW43110 enters low power mode or sleep mode when the switching frequency of the power converter is low. The operating current automatically decreases in order to reduce light load or no-load power loss of the whole system.

4.1 Pin Detail

4.1.1 Pin 1 – VCC

Output of the internal V_{VCC} LDO regulator. It provides bias voltage for the controller. A capacitor (typical 1 µF or 2.2 µF) must be connected between the VCC pin and GND. When an electrolytic capacitor is used, a decoupling capacitor of 0.1 µF or so should be connected between the VCC pin and GND.

4.1.2 Pin 2 – VIN

Connected to the output capacitor positive node or auxiliary winding output port.

4.1.3 Pin 3 – DET

Used for adaptive V_{DS} sensing function to support $V_{DS} \geq 145$ V applications.

4.1.4 Pin 4 – VD

Synchronous rectifier power-switch drain voltage sensing. Used for adaptive V_{DS} sensing function to support $V_{DS} < 145$ V applications. Connect this pin as close to the drain of the power switch as possible to avoid noise coupling from the traces.

4.1.5 Pin 5 – VSS

IC ground.

4.1.6 Pin 6 – OUT

Gate driver for the external synchronous MOSFET/GaN switch.

4.2 V_{DS} Sensing and Synchronous Rectifier Driving Scheme

The RRW43110 is a synchronous rectifier controller that uses Renesas' proprietary lossless sensing technology to monitor the drain-to-source voltage (V_{DS}) of the synchronous power switch to determine the driver turn-on timing. The RRW43110 is capable of analyzing V_{DS} waveform from VD pin or DET pin (depending on the product option) to analyze the primary main switch action.

The RRW43110 only enables SR turn-on detection when primary turn-off is confirmed. This avoids the synchronous rectifier power switch turn-on during transformer ringing and primary auxiliary switch on/off. When the SR turn-on is enabled, the RRW43110 turns on the synchronous rectifier power switch when the V_{DS} is below the V_{ON_TH}, indicating that a current is going through the body diode of the synchronous rectifier power switch. During the SR turn on event, the control logic enables the built-in SR driver to pull up the gate voltage of the synchronous rectifier power switch to the V_{VCC} voltage. The driver has a minimum on-time (t_{ON_MIN}) to avoid the noise from turning off the driver immediately.

The SR gate voltage driven to full V_{VCC} voltage can minimize the conduction loss during SR turn-on time. However, it has a drawback when operating at CCM condition. When a power converter works in CCM mode, the SR current slope at turn-off is high. Long delay caused by discharging the synchronous rectifier power switch

gate from full V_{VCC} voltage to its V_{GS_TH} level will result in the negative current of the secondary winding. This will significantly increase the turn-off power loss during CCM operation.

Therefore, after the minimum on-time, the driver disables the pull-up. In addition, with the intelligent regulation of the SR control block, RRW43110 samples and regulates V_{DS} voltage to V_{REG_TH}. When the V_{DS} voltage drops to V_{REG_TH}, RRW43110 reduces the gate voltage close to its V_{GS_TH} level (shown in Figure 7).

The SR driver is turned off when the V_{DS} reaches V_{OFF_T}., since the synchronous rectifier power switch gate voltage is already reduced close to the V_{GS_TH} threshold level and the synchronous rectifier power switch can be turned off with small delay. As a result, the turn off power loss at CCM mode can be greatly reduced. After the SR driver turns off, the V_{DS} rises.

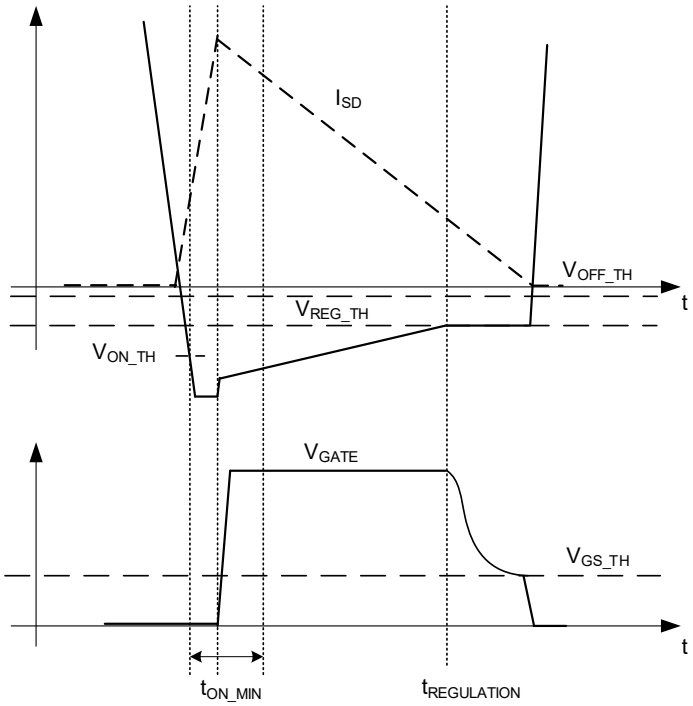


Figure 7. SR Power Switch Gate Voltage V_{GATE}

4.3 Sleep Mode

Based on V_{DS} sensing, the RRW43110 will detect the switching frequency of the power converter. When RRW43110 senses that the power converter does not switch for the pre-defined period, the RRW43110 will turn off most of its function blocks and enter sleep mode to reduce the IC current consumption. Once the power converter starts to switch again, RRW43110 will exit the sleep mode and re-enter the normal mode.

5. Application Information

The layout of the system printed circuit board (PCB) is very important for high performance of the controller IC in terms of accurate signal sensing and lower driving related loss.

Switching the active device on and off in the switch-mode power supply causes fast current and voltage change in the circuit. Such fast current change induces voltage transient on the parasitic impedance of the power devices, interconnect or circuit traces. This voltage transient may be picked up by the signal sensing circuit of the controller and may compromise its performance. Therefore, it is important to reduce this voltage transient by minimizing the parasitic impedance with proper layout. The critical components must be placed as close to each other as possible and be connected with wide and short traces.

Figure 8 shows the critical components and their connections on the secondary side of the power converter with a synchronous rectifier. The synchronous rectifier power switch and the output capacitor must be close to each

other. And the PCB trace between them must be wide and short. The VSS pin of the RRW43110 must be connected to the source of the power switch with single-point connection. If vias are used in the layout for the ground connection, it is recommended to use at least two vias in parallel to reduce their impedance.

To reduce the ringing at the turn-on and turn-off transient of the synchronous rectifier power switch, the gate driving current loop must be as small as possible.

The VCC pin capacitor (C_{VCC}) must be as close to the IC as possible. The traces connecting the capacitor to the IC pins should be as short as possible.

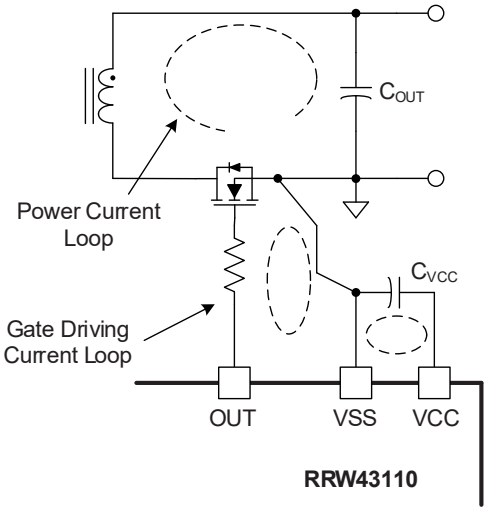


Figure 8. Power Loops at the Secondary Side of the Converter

Figure 9 shows the connection for V_{DS} voltage sensing via VD pin. It is important that the source of the synchronous rectifier power switch is directly connected to the VSS pin of the RRW43110. The VD pin must be connected as close to the drain of synchronous rectifier power switch as possible. The voltage sensing loops must be minimized to reduce the coupling of noise.

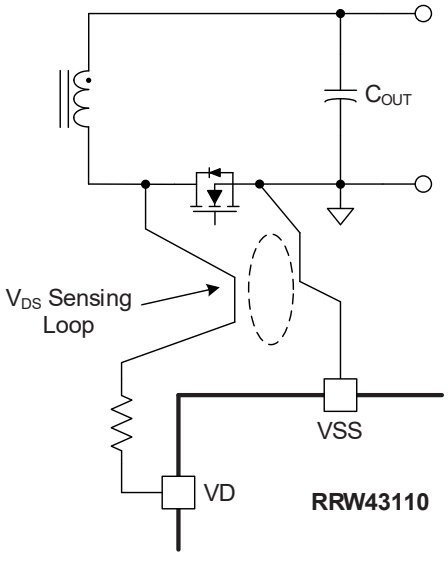
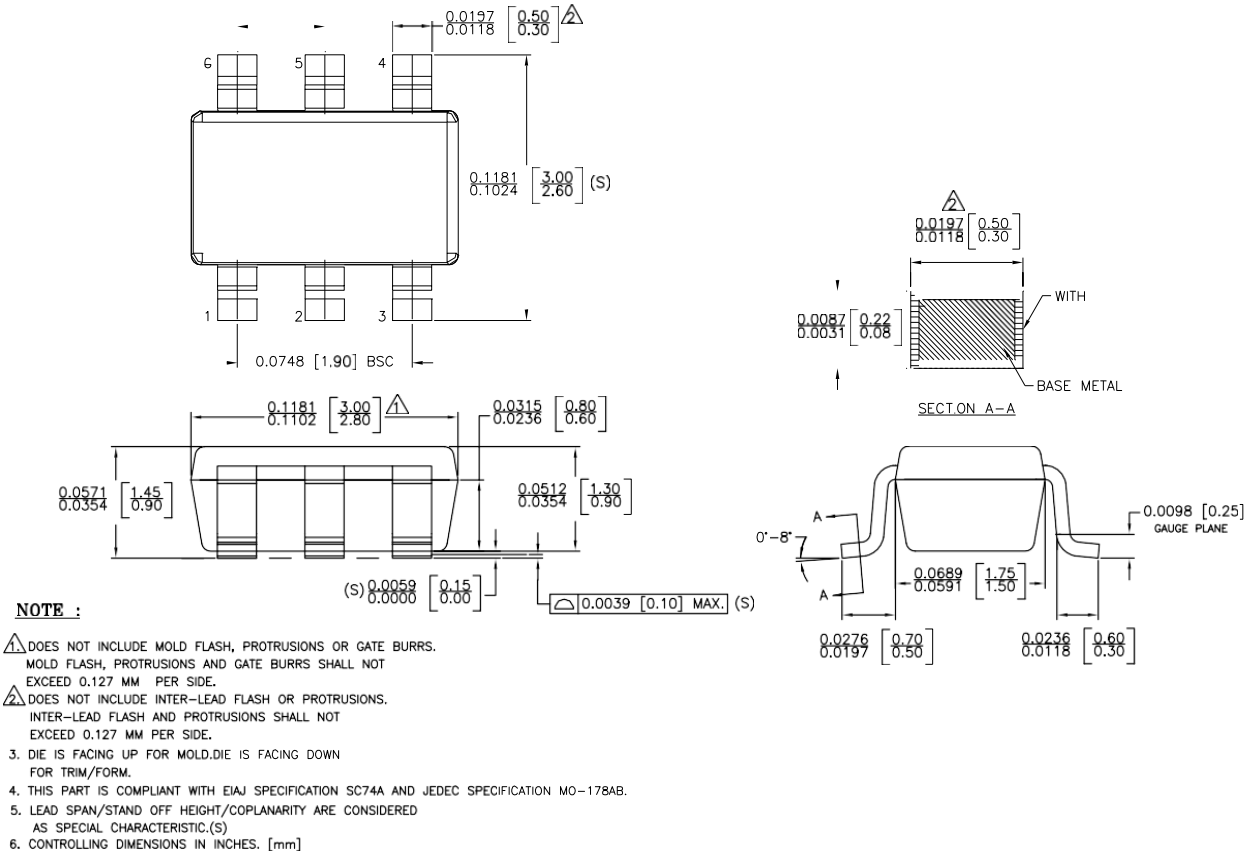


Figure 9. Voltage Sensing Loops at the Secondary Side of the Converter

6. Package Outline Drawings



NOTE :

1. DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.127 MM PER SIDE.
2. DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.127 MM PER SIDE.
3. DIE IS FACING UP FOR MOLD.DIE IS FACING DOWN FOR TRIM/FORM.
4. THIS PART IS COMPLIANT WITH EIAJ SPECIFICATION SC74A AND JEDEC SPECIFICATION MO-178AB.
5. LEAD SPAN/STAND OFF HEIGHT/COPLANARITY ARE CONSIDERED AS SPECIAL CHARACTERISTIC.(S)
6. CONTROLLING DIMENSIONS IN INCHES. [mm]

Figure 10. Package Outline Drawings

7. Ordering Information

Part Number	Options			Package	Carrier Type
	Minimum on-time	V_{VCC_UPPER} Voltage	Sleep Mode Enabled		
RRW43110-430	0.6 µs	7.5 V	Yes	SOT23-6	Tape and Reel (1)

Notes:

1: Tape and reel packing quantity is 3,000/reel. Minimum packing quantity is 3,000.

8. Revision History

Revision	Date	Description
0.03	Mar 2, 2026	Updated ordering information
0.02	Jun 5, 2025	Updated ordering information and recommended operating conditions
0.01	Apr 16, 2025	Initial release.

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