RRW40120

High Voltage Gate Driver for High-Side and Low-Side Switching Devices

Description

The RRW40120 is a high voltage and high frequency gate driver for high-side (HS) and low-side (LS) switching devices optimized for Renesas SuperGaN® FET and conventional power MOSFET. The driver IC includes an HS driver and an LS driver with independent input signals for maximum control flexibility. The HS and LS are also controlled independently with matching propagation delay. The RRW40120 is suitable for application circuits with HS and LS switching devices in topologies such as LLC, active clamp flyback, full-bridge, inverter and many variants from flyback, forward and resonant converters.

The RRW40120 accepts CMOS/TTL compatible signal for easy interfacing with various controllers and microcontrollers. Additionally, the driver features under voltage lockout (UVLO) and interlocking protections for reliable operation.

Features

- 600 V HS/LS Driver with 150 mA@12 V output optimized for SuperGaN® FET and MOSFET.
- CMTI ±50 V/ns
- Ultra-low power consumption
- Switching frequency up to 500 kHz
- Interlocking function for shoot-through protection
- UVLO protection for both channels

Applications

- *RapidChargingTM* AC/DC adapters
- TV power
- Power tools
- SSL applications
- Motor drive

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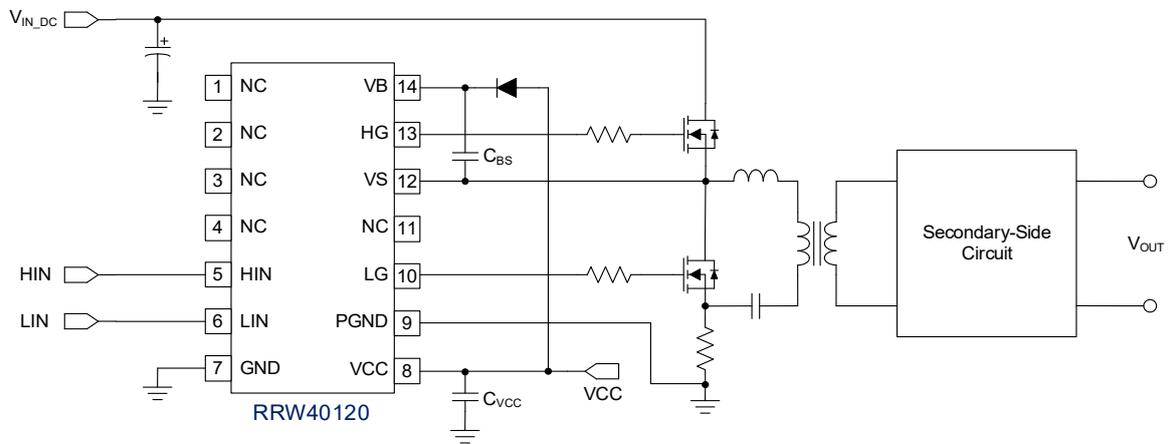
Figure 2. Simplified Application Schematic

2. Pin Information

2.1 Pin Assignments

RRW40120

1	NC	VB	14
2	NC	HG	13
3	NC	VS	12
4	NC	NC	11
5	HIN	LG	10
6	LIN	PGND	9
7	GND	VCC	8

Figure 3. 14 Pin SOIC Package

2.2 Pin Descriptions

Table 1. Pin Descriptions

Pin Number	Pin Name	Type	Description
1, 2, 3, 4, 11	NC	No Connect	Not connected
5	HIN	Analog input	High-side driver logic input
6	LIN	Analog input	Low-side driver logic input
7	GND	Ground	Signal ground
8	VCC	Power	IC power supply
9	PGND	Ground	Low-side return
10	LG	Analog output	Low-side gate drive output
12	VS	Analog input/output	High-side return
13	HG	Analog input/output	High-side gate drive output
14	VB	Analog input/output	High-side power supply

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Unit
Low-side power supply	V_{VCC}	-1	20	V
High-side power supply (V_{VS} referenced)	V_{BS}	-1	20	V
High-side power supply	V_{VB}	V_{VCC} - 5	700	V
High-side return voltage (GND referenced)	V_{VS}	-1	700	V
High-side gate drive output voltage	V_{HG}	V_{VS} - 0.5	V_{VB} + 0.5	V
Low-side output voltage	V_{LG}	-1	20	V
Input signal voltage (HIN/LIN)	V_{IN}	-1	5.5	V
Allowable V_{VS} transient (GND referenced)	dV_{VS}/dt	-50	50	V/ns
Allowable negative voltage on VS pin	V_{S_MIN}	-5		V
Junction temperature	T_{JMAX}	-40	+150	°C
Storage temperature range	T_{ST}	-55	+150	°C
Human body model (tested per JS-001-2017)	V_{ESDHBM}	-	±2000	V
Charged device model (tested per JS-002-2014)	V_{ESDCDM}	-	±1000	V
Latch-up (tested per JESD78E; Class 2, Level A)	-	-	±100	mA

3.2 Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Parameter	Symbol	Minimum	Maximum	Unit
Ambient temperature	T_A	-40	125	°C
Junction temperature	T_J	-40	150	°C
Supply voltage	V_{VCC}	10	18	V
Bootstrap supply voltage, V_{VB} - V_{VS}	V_{BS}	10	18	V
High-side return voltage	V_{VS}	-1	600	V

3.3 Thermal Specifications

Table 4. Thermal Specifications

Parameter	Package	Symbol	Condition	Typical Value	Unit
Thermal Resistance	SOIC-14 Package	θ_{JA}	Junction to ambient	TBD	°C/W
		θ_{JC}	Junction to case	TBD	

3.4 Electrical Specifications

Recommended operating conditions unless otherwise noted. V_{IN} = 0 V to 5 V, V_{VCC} = 15 V, C_{VCC} = C_{BS} = 4.7 µF, T_A = -40 °C to +125 °C, typical values are at T_A = +25 °C, unless otherwise specified.

Table 5. Electrical Specifications

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Low-side Driver Section power supply						
Start-up threshold	$V_{VCC(ST)}$	V_{VCC} rising	6.7	7.3	7.7	V
Under-voltage lockout threshold	$V_{VCC(UVL)}$	V_{VCC} falling	6	6.5	7	V
Quiescent VCC supply current	I_{QCC}	V_{VCC} = V_{BS} = 10 V, H_{IN} = L_{IN} =0 V		100		µA
Start-up current	$I_{VCC(ST)}$	V_{VCC} = 5 V, VB pin floats			10	µA
High-side Driver Section power supply						
V_{BS} supply start-up threshold	$V_{BS(ST)}$		6.7	7.3	7.7	V
V_{BS} supply under-voltage lockout threshold	$V_{BS(UVL)}$		6	6.5	7	V
Quiescent V_{BS} supply current	I_{QBS}	V_{VCC} = V_{BS} = 10 V, H_{IN} = L_{IN} =0 V,		30		µA
High-side leakage current	I_{LK}	V_B = H_G = V_S = 600 V, V_{VCC} = V_{HIN} = L_{IN} = 0 V	-	-	10	µA
Input section						
Logic high threshold for HIN/LIN pin	V_{IN+}		2.0	2.2	2.5	V
Logic low threshold HIN/LIN pin	V_{IN-}		0.9	1.1	1.5	V
HIN/LIN pin input bias current	I_{IN+}	VHIN/LIN = 5 V		12	18	µA
Clamped voltage at HIN and LIN pin	V_{IN_CLP}	@25 µA sinking current [1]		5.3		V
Output Driving						
HS Peak sourcing current for turn-on	$I_{O+(HS)}$	25 °C, V_{BS} = 12 V, V_{HG} = 0 V, V_{VS} referenced		150		mA
HS Peak sinking current for turn-off	$I_{O-(HS)}$	25 °C, V_{BS} = 12 V, V_{HG} = 12 V, V_{VS} referenced		1		A
LS Peak sourcing current for turn-on	$I_{O+(LS)}$	25 °C, V_{VCC} = 12 V, V_{LG} = 0 V		150		mA
LS Peak sinking current for turn-off	$I_{O-(LS)}$	25 °C, V_{VCC} = 12 V, V_{LG} = 12 V		1		A
Drive pin default pull down resistance	R_{PD}	Vo = 1 V		30		kΩ
Dynamic Characteristics						
Driving rise time	t_{R_M}	V_{BS} = V_{VCC} = 12 V,		50		ns

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
		C_{LOAD} = 1 nF, 10% ~ 90%				
Driving fall time	t_{F_M}	V_O = 12 V, C_{LOAD} = 1nF, 90%~ 10%		10		ns
High-side driver turn-on propagation delay	T_{ON_DHS}	V_{BS} = 12 V, C_{LOAD} = 10 pF time between 10% of rising edge		50		ns
High-side turn-off propagation delay	T_{OFF_DHS}	V_O = 12 V, C_{LOAD}= 10 pF, time between 10% of falling edge		50		ns
Low-side turn-on propagation delay	T_{ON_DLS}	V_{VCC} = 12 V, C_{LOAD} = 10 pF, time between 10% of rising edge		50		ns
Low-side turn-off propagation delay	T_{OFF_DLS}	V_O = 12 V, C_{LOAD} = 10 pF, time between 10% of falling edge		50		ns
Delay matching time (HS & LS turn-on/off)	T_{DM}	Same as above	-	-	20	ns

1. These parameters are not 100% tested. They are guaranteed by design.

4. Functional Description

4.1 Pin Detail

4.1.1 Pins 1, 2, 3, 4, 11 – NC

Not connected.

4.1.2 Pin 5 – HIN

Logic input for the high-side driver.

4.1.3 Pin 6 – LIN

Logic input for the low-side driver.

4.1.4 Pin 7 – GND

Signal ground.

4.1.5 Pin 8 – VCC

Power supply for the device during normal operation. The device starts up when V_{VCC} reaches 7.3 V (typical) and shuts down when V_{VCC} drops below 6.5 V (typical). A decoupling capacitor of 0.1 µF and so should be connected across VCC and GND.

4.1.6 Pin 9 – PGND

Low-side supply return.

4.1.7 Pin 10 – LG

Low-side gate driver output.

4.1.8 Pin 12 – VS

High-side power supply return.

4.1.9 Pin 13 – HG

High-side gate drive output.

4.1.10 Pin 14 – VB

High-side power supply. Bypass this pin to VS pin with a suitable capacitor to sustain bootstrap circuit operation, typically 10 times larger than gate capacitance.

4.2 Power Supply and Undervoltage Lockout Protection

The RRW40120 is supplied by V_{VCC} and V_{BS}. V_{VCC} supplies logic circuit and low-side output buffer. V_{BS} supplies high-side output buffer through a bootstrap capacitor C_{BS} between VB and VS pin, which is charged up by V_{VCC} through the external bootstrap diode.

The RRW40120 has internal under voltage-lockout (UVLO) protection feature on both V_{VCC} and V_{BS} power supplies. It ensures the device drives external power devices only when the gate supply voltage is sufficient for power devices to avoid excessive conduction losses.

When V_{VCC} drops below the $V_{VCC(UVL)}$ threshold, the UVLO circuit will set both LG and HG to be low, and shutdown the device. When V_{VCC} reaches $V_{VCC(ST)}$ again, the device will return to normal operation and set LG and HG based on inputs.

When V_{BS} drops below the $V_{BS(UVL)}$ threshold, the UVLO circuit will set HG to be low. V_{BS} reaches $V_{BS(ST)}$ again, the device will set HG based on HIN.

Both the V_{VCC} and V_{BS} UVLO circuits have hysteresis to prevent chatter due to ground noise in the power supply and to keep normal operation if there is a small drop in the power supply.

4.3   Logic Inputs

The RRW40120 has two logic inputs:

- HIN: high-side driver input
- LIN: low-side driver input.

The logic inputs are CMOS/TTL compatible for easy interfacing with various controllers and microcontrollers. Both logic inputs have internal 650 kΩ pull-down resistors, as shown in the block diagrams, which guarantee the input logic state is held in the low state whenever any of the input pins are in the floating condition.

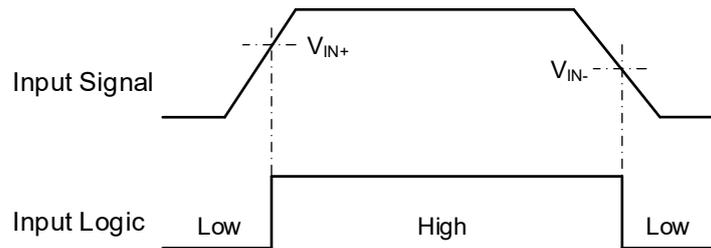Figure 4 shows the input signal to the RRW40120 and the corresponding logic state.

Figure 4. Input Logic State

4.4   Interlocking

The RRW40120 has interlocking function, which guarantees that when inputs HIN and LIN are both high, both outputs LG and HG will stay low.

Table 6 shows the input/output truth table of RRW40120.

Table 6. Input/Output Truth Table

Input		Output	
HIN	**LIN**	**HG**	**LG**
L	L	L	L
L	H	L	H
H	L	H	L
H	H	L	L

4.5   Switching Timing Relationships

Figure 5 shows the timing relationships between the input and output signals, including the definition of T_{ON_DHS}, T_{OFF_DHS}, T_{ON_DLS}, and T_{OFF_DLS}.
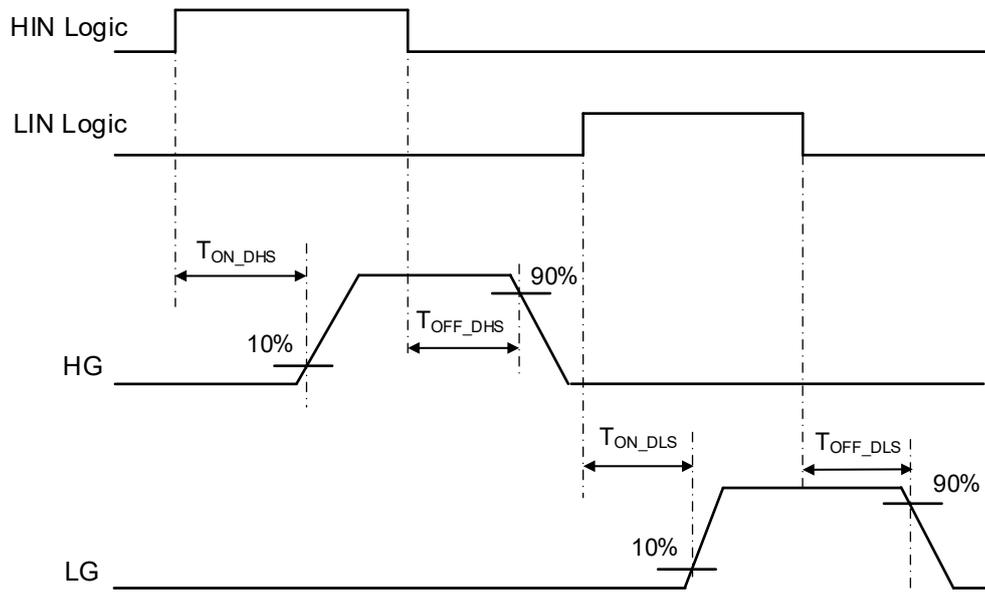

Figure 5. Input/Output Timing Relationships

5. Package Outline Drawings

SYMBOLS	MIN.	MAX.
A	1.35	1.75
A1	0.10	0.25
A2	1.25	1.50
b	0.33	0.51
c	0.19	0.25
D	8.55	8.75
E	5.80	6.20
E1	3.80	4.00
e	1.27 BSC	
L	0.40	1.27
h	0.25	0.50
$\theta°$	0	8

UNIT : mm

NOTES:
1. JEDEC OUTLINE : MS-012 AB
2. DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15mm, PER SIDE.
3. DIMENSIONS "E1" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25mm PER SIDE.
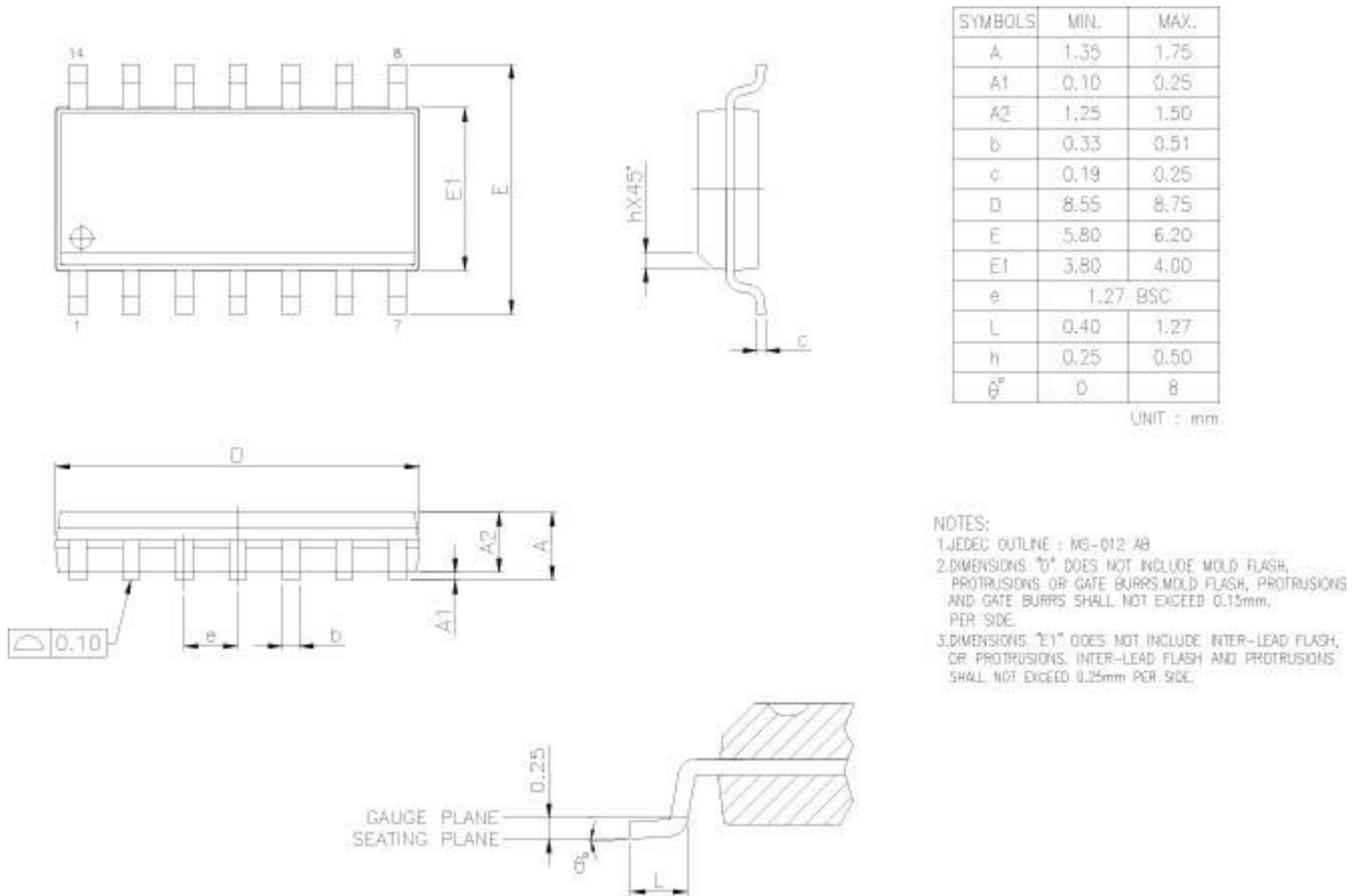
Figure 6. 14-Pin QFN Package

6. Ordering Information

Table 7. Ordering Information

Part Number	Driver Output Voltage	Pull-up Current (V_{VCC} = 12V)	Pull-down Current (V_{VCC} = 12V)	Package Description	Carrier Type
RRW40120-002	HS: V_{VCC}, LS: V_{BS}	150 mA	1 A	SOIC-14	Tape & Reel[1]

1. Tape & Reel packing quantity is 2,500/reel. Minimum packing quantity is 2,500.

7. Revision History

Revision	Date	Description
0.04	Feb 26, 2026	Updated format.
0.03	Sep 5, 2025	Updated recommended operating conditions.
0.02	Mar 17, 2025	Updated functional block diagram and simplified application schematic.
0.01	Feb 20, 2025	Initial release.

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