RL78/L23

RENESAS MCU

R01DS0502EJ0100
Rev.1.00
May 30, 2025

On-chip LCD controller/driver, true low-power platform, 50-μA/MHz operating current, 330-nA data retention current for 4 KB of RAM, up to 512-KB code flash memory and 32-KB RAM, up to 36 capacitive touch sensors, from 44 to 100 pins, 1.6-5.5 V

1. Outline

1.1 Features

Ultra-low power consumption technology
- V_{DD} = single power supply voltage of 1.6 to 5.5 V
- HALT mode
- STOP mode
  High-speed wakeup from the STOP mode is possible.
- SNOOZE mode

RL78 CPU core
- CISC architecture with 3-stage pipeline
- Minimum instruction execution time:
  Can be changed from high speed (0.03125 μs @ 32 MHz operation with the high-speed on-chip oscillator clock) to ultra-low speed (30.5 μs @ 32.768 kHz operation with the subsystem clock)
- Multiply/divide/multiply & accumulate instructions are supported.
- Address space: 1 MB
- General-purpose registers: (8-bit register × 8) × 4 banks
- On-chip RAM: 16 to 32 KB

Code flash memory
- Code flash memory:
  64 to 128 KB (single bank)
  256 KB (128 KB × 2 banks or a single 256-KB bank)
  512 KB (256 KB × 2 banks or a single 512-KB bank)
- Block size: 2 KB
- Prohibition of block erase and rewriting (security function)
- On-chip debugging
- Self-programming (with boot swapping and flash shield window)
- Bank programming: Enables updating of the program in one bank while the user program is running from the other bank.

Data flash memory
- Data flash memory: 8 KB
- Background operation (BGO):
  Instructions can be executed from the program memory while rewriting the data flash memory.
- Number of rewrites: 1,000,000 times (typ.)

High-speed on-chip oscillator
- Select from 64 MHz, 48 MHz, 32 MHz, 24 MHz, 16 MHz, 12 MHz, 8 MHz, 6 MHz, 4 MHz, 3 MHz, 2 MHz, or 1 MHz
- High accuracy: ±1.0%
  (V_{DD} = 1.6 to 5.5 V, T_A = -40 to +105°C)

Middle-speed on-chip oscillator
- Select from 4 MHz, 2 MHz, or 1 MHz (with adjustability)

Low-speed on-chip oscillator
- 32.768 kHz (typ.) (with adjustability)

Operating ambient temperature
- T_A = -40 to +105°C (3C: Industrial applications)

Power management and reset function
- On-chip power-on-reset (POR) circuit
- On-chip voltage detectors (LVD0 and LVD1)

Data transfer controller (DTC)
- Transfer modes:
  Normal transfer mode, repeat transfer mode, block transfer mode
- Activation sources: Activated by interrupt sources.
- Chain transfer function

SNOOZE mode sequencer (SMS)
- Calculations and comparison of values by the commands for use in processing by the sequencer can realize intermittent operations where the RL78/L23 does not have to return to normal operation.
- Sequentially handling a total of 32 processes with the use of desired commands from among 21 different ones
- The SNOOZE mode sequencer offers operation with low power consumption without using the CPU, flash memory, and RAM.

Logic and event link controller (ELCL)
- Event signals can be set up between specified peripheral functions.
- The signals can be generated by the input of multiple event signals to the logic circuit.
- Flip-flop circuits are incorporated to handle setting and resetting functions.

Serial interface
- Simplified SPI (CSI[Note]): 5 to 8 channels
- UART/UART (LIN-bus supported)/UARTA: 5 to 8 channels
- I^2C/Simplified I^2C: 8 to 10 channels

Timers
- 16-bit timer: 8 channels
  (with the output of remote control signals)
- 16-bit timer RJ: 1 or 2 channels
- 16-bit timers KB40, KB41, and KB42 (IH): 1 to 3 channels (with PWM output for IH)
- 32-bit interval timer:
  1 channel in 32-bit counter mode
  2 channels in 16-bit counter mode
  4 channels in 8-bit counter mode
- 8-bit interval timer: 4 to 8 units
- Realtime clock: 1 channel
  (counting of one second to 99 years, alarm interrupt, and clock correction)
- Watchdog timer: 1 channel (operates with the dedicated low-speed on-chip oscillator clock)
- External signal sampler: 1 channel
- Oscillation stop detector: 1 channel

LCD controller/driver
- Internal boosting, capacitive division, and external resistor division are switchable as methods of generating the driving voltage.
- Number of segment signal outputs: 19 to 56
- Number of common signal outputs: 4 to 8

A/D converter
- 8-/10-/12-bit resolution
- Analog input: 8 to 13 channels
- Internal reference voltage (1.48 V (typ.)) and temperature sensor

D/A converter
- 8-bit resolution
- Analog output:
  3 channels (one of the three interfaces is only for the internal reference voltage for the comparator)
- Output voltage: 0 V to V_{DD}
- Realtime output function

Comparator
- 1 or 2 channels
- Operating modes: Comparator high-speed mode and comparator low-speed mode
- The external reference voltage and the internal reference voltage or D/A converter output are selectable as the reference voltage.

Capacitive sensing unit
- Operating voltage condition: V_{DD} = 1.8 to 5.5 V
- Self-capacitance method: A single pin configures a single key, supporting up to 36 keys
- Mutual capacitance method: Matrix configuration with 8 × 8 pins, supporting up to 64 keys

Input/output port pins
- Number of port pins:
  40 to 95
  N-ch open-drain I/O (withstand voltage of 6 V): 2 to 4,
  N-ch open-drain I/O (VDD withstand voltage): 24 to 57,
  Controlled current drive pins: 4 to 8
- Can be set to N-ch open drain or TTL input buffer, and use of an on-chip pull-up resistor can be specified.
- Connectable to a device with different voltage (1.8 V, 2.5 V, or 3 V)

Others

- Key interrupt input
- Clock output/buzzer output controller
- BCD (binary-coded decimal) correction circuit

Note Although the CSI function is generally called SPI, it is also called CSI in this product, so it is referred to as such in this manual.

Remark The functions mounted depend on the product. For details, see **1.6 Outline of Functions**.

O ROM, RAM capacities

Flash ROM	Data flash	RAM	RL78/L23					
			44 pins	48 pins	52 pins	64 pins	80 pins	100 pins
512 KB	8 KB	32 KB	R7F100LFL	R7F100LGL	R7F100LJL	R7F100LLL	R7F100LML	R7F100LPL
256 KB	8 KB	32 KB	R7F100LFJ	R7F100LGJ	R7F100LJJ	R7F100LLJ	R7F100LMJ	R7F100LPJ
128 KB	8 KB	16 KB	R7F100LFG	R7F100LGG	R7F100LJG	R7F100LLG	R7F100LMG	R7F100LPG
64 KB	8 KB	16 KB	R7F100LFE	R7F100LGE	R7F100LJE	R7F100LLE	—	—

1.2 List of Part Numbers

Figure 1 - 1 Part Number, Memory Size, and Package of RL78/L23

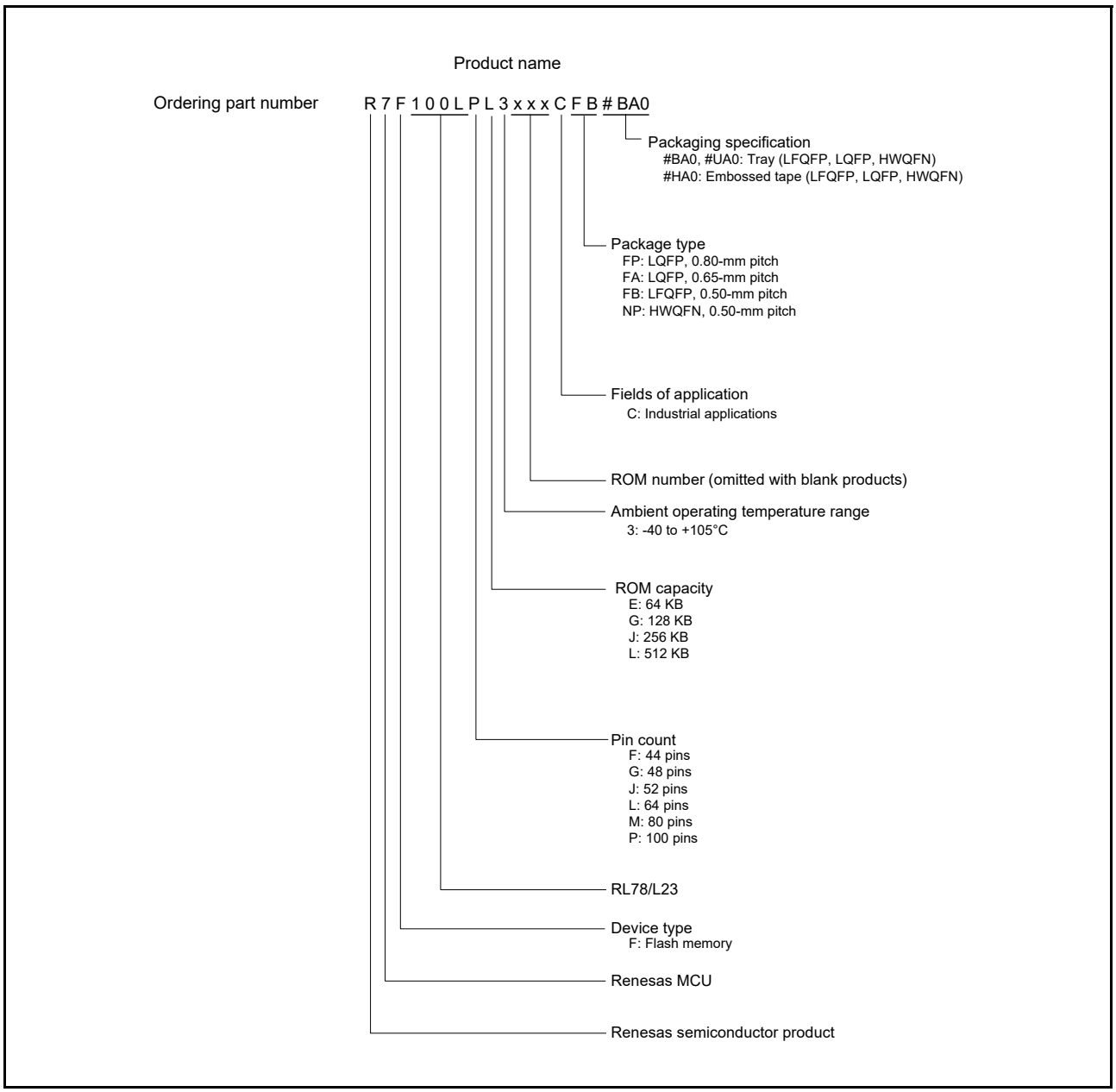


Table 1 - 1 List of Ordering Part Numbers

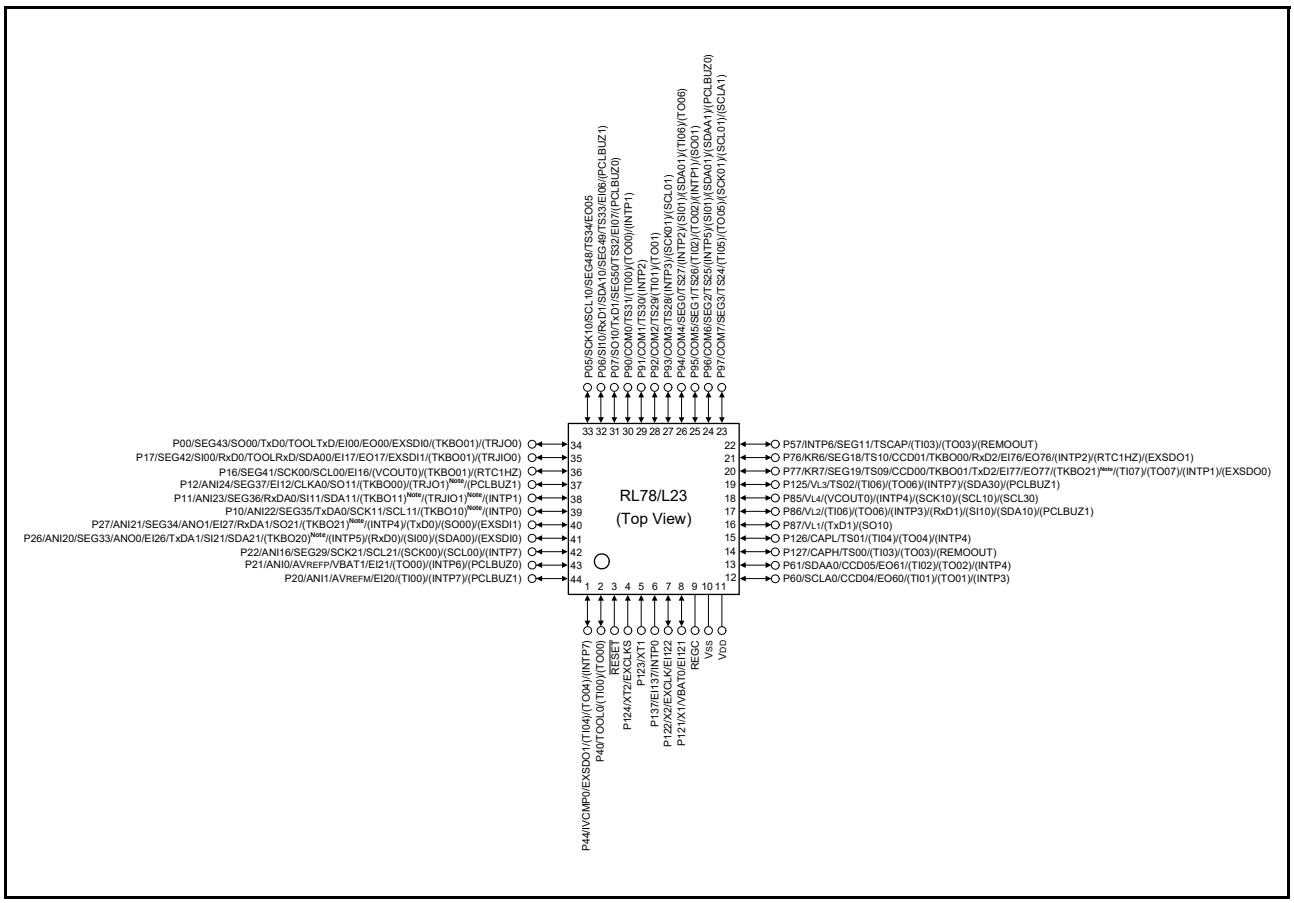
Pin count	Package	Fields of Application Note	Ordering Part Number		Renesas Code
			Product Name	Packaging Specification	
44	44-pin plastic LQFP (10 × 10 mm, 0.80-mm pitch)	C	R7F100LFL3CFP, R7F100LFJ3CFP, R7F100LFG3CFP, R7F100LFE3CFP	#BA0, #UA0, #HA0	PLQP0044GC-A
48	48-pin plastic LFQFP (7 × 7 mm, 0.50-mm pitch)	C	R7F100LGL3CFB, R7F100LGJ3CFB, R7F100LGG3CFB, R7F100LGE3CFB	#BA0, #UA0, #HA0	PLQP0048KB-B
	48-pin plastic HWQFN (7 × 7 mm, 0.50-mm pitch)	C	R7F100LGL3CNP, R7F100LGJ3CNP, R7F100LGG3CNP, R7F100LGE3CNP	#BA0, #UA0, #HA0	PWQN0048KC-A
52	52-pin plastic LQFP (10 × 10 mm, 0.65-mm pitch)	C	R7F100LJL3CFA, R7F100LJJ3CFA, R7F100LJG3CFA, R7F100LJE3CFA	#BA0, #UA0, #HA0	PLQP0052JA-A
64	64-pin plastic LQFP (12 × 12 mm, 0.65-mm pitch)	C	R7F100LLL3CFA, R7F100LLJ3CFA, R7F100LLG3CFA, R7F100LLE3CFA	#BA0, #UA0, #HA0	PLQP0064JB-A
	64-pin plastic LFQFP (10 × 10 mm, 0.50-mm pitch)	C	R7F100LLL3CFB, R7F100LLJ3CFB, R7F100LLG3CFB, R7F100LLE3CFB	#BA0, #UA0, #HA0	PLQP0064KB-C
80	80-pin plastic LQFP (14 × 14 mm, 0.65-mm pitch)	C	R7F100LML3CFA, R7F100LMJ3CFA, R7F100LMG3CFA	#BA0, #UA0, #HA0	PLQP0080JA-B
	80-pin plastic LFQFP (12 × 12 mm, 0.50-mm pitch)	C	R7F100LML3CFB, R7F100LMJ3CFB, R7F100LMG3CFB	#BA0, #UA0, #HA0	PLQP0080KB-B
100	100-pin plastic LFQFP (14 × 14 mm, 0.50-mm pitch)	C	R7F100LPL3CFB, R7F100LPJ3CFB, R7F100LPG3CFB	#BA0, #UA0, #HA0	PLQP0100KB-B
	100-pin plastic LQFP (14 × 20 mm, 0.65-mm pitch)	C	R7F100LPL3CFA, R7F100LPJ3CFA, R7F100LPG3CFA	#BA0, #UA0, #HA0	PLQP0100JC-A

Note For the fields of application, see **Figure 1 - 1 Part Number, Memory Size, and Package of RL78/L23**.

1.3 Pin Configuration (Top View)

1.3.1 44-pin products

- 44-pin plastic LQFP (10 × 10 mm, 0.80-mm pitch)



Note Not present in products with 128 or fewer Kbytes of code flash memory.

Caution **Connect the REGC pin to Vss via a capacitor (0.47 to 1 µF).**

Remark 1. For pin identification, see **1.4 Pin Identification**.

Remark 2. Pin functions in parentheses can be assigned via settings in the peripheral I/O redirection registers (PIORx). For details, see **4.3.10 Peripheral I/O redirection registers (PIORx)** in the RL78/L23 User's Manual.

Table 1 - 2 Multiplexed Pin Functions of the 44-pin Products (1/3)

Pin Number	I/O				Analog Circuits				HMIs			Timers					Communications Interfaces		
44LQFP	Digital port	Controlled current drive port	ELCL input/output port	Power supply, system clock, and debugging	A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	LCD controller/driver (LCD)	Interrupt	Key interrupt	Capacitive sensing unit (CTSU2La)	Timer array unit (TAU)	Timer RJ (TRJ)	16-bit timers KB40, KB41, and KB42	External signal sampler	Realtime clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
1	P44	—	—	—	—	—	IVCMP0	—	(INTP7)	—	—	(TI04)/ (TO04)	—	—	EXSDO1	—	—	—	—
2	P40	—	—	TOOL0	—	—	—	—	—	—	—	(TI00)/ (TO00)	—	—	—	—	—	—	—
3	—	—	—	$\overline{\text{RESET}}$	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
4	P124	—	—	XT2/ EXCLKS	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
5	P123	—	—	XT1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
6	P137	—	EI137	—	—	—	—	—	INTP0	—	—	—	—	—	—	—	—	—	—
7	P122	—	EI122	X2/EXCLK	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
8	P121	—	EI121	X1/VBAT0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
9	—	—	—	REGC	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
10	—	—	—	V_{SS}	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
11	—	—	—	V_{DD}	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
12	P60	CCD04	EO60	—	—	—	—	—	(INTP3)	—	—	(TI01)/ (TO01)	—	—	—	—	—	SCLA0	—
13	P61	CCD05	EO61	—	—	—	—	—	(INTP4)	—	—	(TI02)/ (TO02)	—	—	—	—	—	SDAA0	—
14	P127	—	—	—	—	—	—	CAPH	—	—	TS00	(TI03)/ (TO03)/ (REMOOUT)	—	—	—	—	—	—	—
15	P126	—	—	—	—	—	—	CAPL	(INTP4)	—	TS01	(TI04)/ (TO04)	—	—	—	—	—	—	—
16	P87	—	—	—	—	—	—	V_{L1}	—	—	—	—	—	—	—	—	(TxD1)/ (SO10)	—	—
17	P86	—	—	(PCLBUZ1)	—	—	—	V_{L2}	(INTP3)	—	—	(TI06)/ (TO06)	—	—	—	—	(RxD1)/ (SI10)/ (SDA10)	—	—
18	P85	—	—	—	—	—	(VCOUT0)	V_{L4}	(INTP4)	—	—	—	—	—	—	—	(SCK10)/ (SCL10)/ (SCL30)	—	—
19	P125	—	—	(PCLBUZ1)	—	—	—	V_{L3}	(INTP7)	—	TS02	(TI06)/ (TO06)	—	—	—	—	(SDA30)	—	—
20	P77	CCD00	EI77/ EO77	—	—	—	—	SEG19	(INTP1)	KR7	TS09	(TI07)/ (TO07)	—	TKBO01/ (TKBO21) **Note**	(EXSDO0)	—	TxD2	—	—
21	P76	CCD01	EI76/ EO76	—	—	—	—	SEG18	(INTP2)	KR6	TS10	—	—	TKBO00	(EXSDO1)	(RTC1HZ)	RxD2	—	—
22	P57	—	—	—	—	—	—	SEG11	INTP6	—	TSCAP	(TI03)/ (TO03)/ (REMOOUT)	—	—	—	—	—	—	—
23	P97	—	—	—	—	—	—	SEG3/ COM7	—	—	TS24	(TI05)/ (TO05)	—	—	—	—	(SCK01)/ (SCL01)	(SCLA1)	—

Table 1 - 2 Multiplexed Pin Functions of the 44-pin Products (2/3)

Pin Number	I/O			Power supply, system clock, and debugging	Analog Circuits				HMIs			Timers					Communications Interfaces		
44LQFP	Digital port	Controlled current drive port	ELCL input/output port		A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	LCD controller/driver (LCD)	Interrupt	Key interrupt	Capacitive sensing unit (CTSU2La)	Timer array unit (TAU)	Timer RJ (TRJ)	16-bit timers KB40, KB41, and KB42	External signal sampler	Realtime clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
24	P96	—	—	(PCLBUZ0)	—	—	—	SEG2/ COM6	(INTP5)	—	TS25	—	—	—	—	—	(SI01)/ (SDA01)	(SDAA1)	—
25	P95	—	—	—	—	—	—	SEG1/ COM5	(INTP1)	—	TS26	(TI02)/ (TO02)	—	—	—	—	(SO01)	—	—
26	P94	—	—	—	—	—	—	SEG0/ COM4	(INTP2)	—	TS27	(TI06)/ (TO06)	—	—	—	—	(SI01)/ (SDA01)	—	—
27	P93	—	—	—	—	—	—	COM3	(INTP3)	—	TS28	—	—	—	—	—	(SCK01)/ (SCL01)	—	—
28	P92	—	—	—	—	—	—	COM2	—	—	TS29	(TI01)/ (TO01)	—	—	—	—	—	—	—
29	P91	—	—	—	—	—	—	COM1	(INTP2)	—	TS30	—	—	—	—	—	—	—	—
30	P90	—	—	—	—	—	—	COM0	(INTP1)	—	TS31	(TI00)/ (TO00)	—	—	—	—	—	—	—
31	P07	—	EI07	(PCLBUZ0)	—	—	—	SEG50	—	—	TS32	—	—	—	—	—	SO10/ TxD1	—	—
32	P06	—	EI06	(PCLBUZ1)	—	—	—	SEG49	—	—	TS33	—	—	—	—	—	SI10/ RxD1/ SDA10	—	—
33	P05	—	EO05	—	—	—	—	SEG48	—	—	TS34	—	—	—	—	—	SCK10/ SCL10	—	—
34	P00	—	EI00/ EO00	TOOLTxD	—	—	—	SEG43	—	—	—	—	(TRJO0)	(TKBO01)	EXSDI0	—	SO00/ TxD0	—	—
35	P17	—	EI17/ EO17	TOOLRxD	—	—	—	SEG42	—	—	—	—	(TRJIO0)	(TKBO01)	EXSDI1	—	SI00/ RxD0/ SDA00	—	—
36	P16	—	EI16	—	—	—	(VCOUT0)	SEG41	—	—	—	—	—	(TKBO01)	—	(RTC1HZ)	SCK00/ SCL00	—	—
37	P12	—	EI12	(PCLBUZ1)	ANI24	—	—	SEG37	—	—	—	—	(TRJO1) **Note**	(TKBO00)	—	—	SO11	—	CLKA0
38	P11	—	—	—	ANI23	—	—	SEG36	(INTP1)	—	—	—	(TRJIO1) **Note**	(TKBO11) **Note**	—	—	SI11/ SDA11	—	RxDA0
39	P10	—	—	—	ANI22	—	—	SEG35	(INTP0)	—	—	—	—	(TKBO10) **Note**	—	—	SCK11/ SCL11	—	TxDA0
40	P27	—	EI27	—	ANI21	ANO1	—	SEG34	(INTP4)	—	—	—	—	(TKBO21) **Note**	(EXSDI1)	—	(TxD0)/ (SO00)/ SO21	—	RxDA1
41	P26	—	EI26	—	ANI20	ANO0	—	SEG33	(INTP5)	—	—	—	—	(TKBO20) **Note**	(EXSDI0)	—	SI21/ SDA21/ (RxD0)/ (SI00)/ (SDA00)	—	TxDA1
42	P22	—	—	—	ANI16	—	—	SEG29	(INTP7)	—	—	—	—	—	—	—	(SCK00)/ (SCL00)/ SCK21/ SCL21	—	—
43	P21	—	EI21	VBAT1/ (PCLBUZ0)	ANI0/ AVREFP	—	—	—	(INTP6)	—	—	(TO00)	—	—	—	—	—	—	—

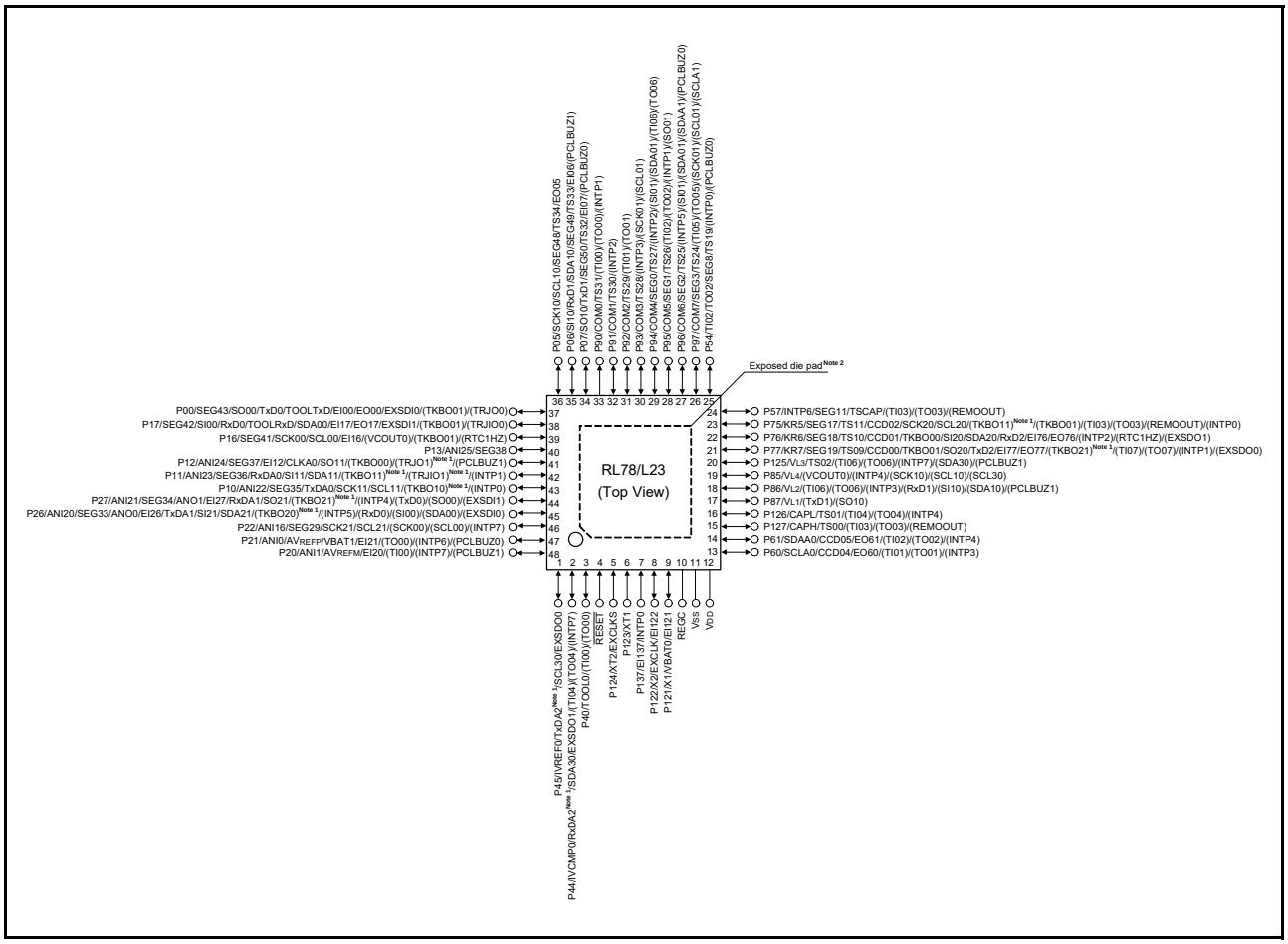
Table 1 - 2 Multiplexed Pin Functions of the 44-pin Products (3/3)

Pin Number	I/O			Power supply, system clock, and debugging	Analog Circuits				HMIs			Timers					Communications Interfaces		
44LQFP	Digital port	Controlled current drive port	ELCL input/output port		A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	LCD controller/driver (LCD)	Interrupt	Key interrupt	Capacitive sensing unit (CTSU2La)	Timer array unit (TAU)	Timer RJ (TRJ)	16-bit timers KB40, KB41, and KB42	External signal sampler	Realtime clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
44	P20	—	EI20	(PCLBUZ1)	ANI1/ AVREFM	—	—	—	(INTP7)	—	—	(TI00)	—	—	—	—	—	—	—

Note Not present in products with 128 or fewer Kbytes of code flash memory.

1.3.2 48-pin products

- 48-pin plastic LFQFP (7 × 7 mm, 0.50-mm pitch)
- 48-pin plastic HWQFN (7 × 7 mm, 0.50-mm pitch)



Note 1. Not present in products with 128 or fewer Kbytes of code flash memory.

Note 2. The 48-pin plastic LFQFP (7 × 7 mm, 0.50-mm pitch) products do not have an exposed die pad.

Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 µF).

Remark 1. For pin identification, see **1.4 Pin Identification**.

Remark 2. Pin functions in parentheses can be assigned via settings in the peripheral I/O redirection registers (PIORx). For details, see **4.3.10 Peripheral I/O redirection registers (PIORx)** in the RL78/L23 User's Manual.

Remark 3. For products in the HWQFN package, solder the exposed die pad to the printed circuit board. We recommend leaving the destination for mounting of the exposed die pad electrically open-circuit.

Table 1 - 3 Multiplexed Pin Functions of the 48-pin Products (1/3)

Pin Number	I/O				Analog Circuits				HMIs			Timers					Communications Interfaces		
48LFQFP, 48HWQFN	Digital port	Controlled current drive port	ELCL input/output port	Power supply, system clock, and debugging	A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	LCD controller/driver (LCD)	Interrupt	Key interrupt	Capacitive sensing unit (CTSU2La)	Timer array unit (TAU)	Timer RJ (TRJ)	16-bit timers KB40, KB41, and KB42	External signal sampler	Realtime clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
1	P45	—	—	—	—	—	IVREF0	—	—	—	—	—	—	—	EXSDO0	—	SCL30	—	TxDA2 **Note**
2	P44	—	—	—	—	—	IVCMP0	—	(INTP7)	—	—	(TI04)/ (TO04)	—	—	EXSDO1	—	SDA30	—	RxDA2 **Note**
3	P40	—	—	TOOL0	—	—	—	—	—	—	—	(TI00)/ (TO00)	—	—	—	—	—	—	—
4	—	—	—	$\overline{\text{RESET}}$	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
5	P124	—	—	XT2/ EXCLKS	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
6	P123	—	—	XT1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
7	P137	—	EI137	—	—	—	—	—	INTP0	—	—	—	—	—	—	—	—	—	—
8	P122	—	EI122	X2/EXCLK	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
9	P121	—	EI121	X1/VBAT0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
10	—	—	—	REGC	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
11	—	—	—	V_{SS}	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
12	—	—	—	V_{DD}	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
13	P60	CCD04	EO60	—	—	—	—	—	(INTP3)	—	—	(TI01)/ (TO01)	—	—	—	—	—	SCLA0	—
14	P61	CCD05	EO61	—	—	—	—	—	(INTP4)	—	—	(TI02)/ (TO02)	—	—	—	—	—	SDAA0	—
15	P127	—	—	—	—	—	—	CAPH	—	—	TS00	(TI03)/ (TO03)/ (REMOOUT)	—	—	—	—	—	—	—
16	P126	—	—	—	—	—	—	CAPL	(INTP4)	—	TS01	(TI04)/ (TO04)	—	—	—	—	—	—	—
17	P87	—	—	—	—	—	—	V_{L1}	—	—	—	—	—	—	—	—	(TxD1)/ (SO10)	—	—
18	P86	—	—	(PCLBUZ1)	—	—	—	V_{L2}	(INTP3)	—	—	(TI06)/ (TO06)	—	—	—	—	(RxD1)/ (SI10)/ (SDA10)	—	—
19	P85	—	—	—	—	—	(VCOUT0)	V_{L4}	(INTP4)	—	—	—	—	—	—	—	(SCK10)/ (SCL10)/ (SCL30)	—	—
20	P125	—	—	(PCLBUZ1)	—	—	—	V_{L3}	(INTP7)	—	TS02	(TI06)/ (TO06)	—	—	—	—	(SDA30)	—	—
21	P77	CCD00	EI77/ EO77	—	—	—	—	SEG19	(INTP1)	KR7	TS09	(TI07)/ (TO07)	—	TKBO01/ (TKBO21) **Note**	(EXSDO0)	—	SO20/ TxD2	—	—
22	P76	CCD01	EI76/ EO76	—	—	—	—	SEG18	(INTP2)	KR6	TS10	—	—	TKBO00	(EXSDO1)	(RTC1HZ)	SI20/ SDA20/ RxD2	—	—

Table 1 - 3 Multiplexed Pin Functions of the 48-pin Products (2/3)

Pin Number	I/O			Power supply, system clock, and debugging	Analog Circuits				HMIs			Timers					Communications Interfaces		
48LFQFP, 48HWQFN	Digital port	Controlled current drive port	ELCL input/output port		A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	LCD controller/driver (LCD)	Interrupt	Key interrupt	Capacitive sensing unit (CTSU2La)	Timer array unit (TAU)	Timer RJ (TRJ)	16-bit timers KB40, KB41, and KB42	External signal sampler	Realtime clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
23	P75	CCD02	—	—	—	—	—	SEG17	(INTP0)	KR5	TS11	(TI03)/ (TO03)/ (REMOOUT)	—	(TKBO11) **Note**/ (TKBO01)	—	—	SCK20/ SCL20	—	—
24	P57	—	—	—	—	—	—	SEG11	INTP6	—	TSCAP	(TI03)/ (TO03)/ (REMOOUT)	—	—	—	—	—	—	—
25	P54	—	—	(PCLBUZ0)	—	—	—	SEG8	(INTP0)	—	TS19	TI02/ TO02	—	—	—	—	—	—	—
26	P97	—	—	—	—	—	—	SEG3/ COM7	—	—	TS24	(TI05)/ (TO05)	—	—	—	—	(SCK01)/ (SCL01)	(SCLA1)	—
27	P96	—	—	(PCLBUZ0)	—	—	—	SEG2/ COM6	(INTP5)	—	TS25	—	—	—	—	—	(SI01)/ (SDA01)	(SDAA1)	—
28	P95	—	—	—	—	—	—	SEG1/ COM5	(INTP1)	—	TS26	(TI02)/ (TO02)	—	—	—	—	(SO01)	—	—
29	P94	—	—	—	—	—	—	SEG0/ COM4	(INTP2)	—	TS27	(TI06)/ (TO06)	—	—	—	—	(SI01)/ (SDA01)	—	—
30	P93	—	—	—	—	—	—	COM3	(INTP3)	—	TS28	—	—	—	—	—	(SCK01)/ (SCL01)	—	—
31	P92	—	—	—	—	—	—	COM2	—	—	TS29	(TI01)/ (TO01)	—	—	—	—	—	—	—
32	P91	—	—	—	—	—	—	COM1	(INTP2)	—	TS30	—	—	—	—	—	—	—	—
33	P90	—	—	—	—	—	—	COM0	(INTP1)	—	TS31	(TI00)/ (TO00)	—	—	—	—	—	—	—
34	P07	—	EI07	(PCLBUZ0)	—	—	—	SEG50	—	—	TS32	—	—	—	—	—	SO10/ TxD1	—	—
35	P06	—	EI06	(PCLBUZ1)	—	—	—	SEG49	—	—	TS33	—	—	—	—	—	SI10/ RxD1/ SDA10	—	—
36	P05	—	EO05	—	—	—	—	SEG48	—	—	TS34	—	—	—	—	—	SCK10/ SCL10	—	—
37	P00	—	EI00/ EO00	TOOLTxD	—	—	—	SEG43	—	—	—	—	(TRJO0)	(TKBO01)	EXSDI0	—	SO00/ TxD0	—	—
38	P17	—	EI17/ EO17	TOOLRxD	—	—	—	SEG42	—	—	—	—	(TRJIO0)	(TKBO01)	EXSDI1	—	SI00/ RxD0/ SDA00	—	—
39	P16	—	EI16	—	—	—	(VCOUT0)	SEG41	—	—	—	—	—	(TKBO01)	—	(RTC1HZ)	SCK00/ SCL00	—	—
40	P13	—	—	—	ANI25	—	—	SEG38	—	—	—	—	—	—	—	—	—	—	—
41	P12	—	EI12	(PCLBUZ1)	ANI24	—	—	SEG37	—	—	—	—	(TRJO1) **Note**	(TKBO00)	—	—	SO11	—	CLKA0
42	P11	—	—	—	ANI23	—	—	SEG36	(INTP1)	—	—	—	(TRJIO1) **Note**	(TKBO11) **Note**	—	—	SI11/ SDA11	—	RxDA0

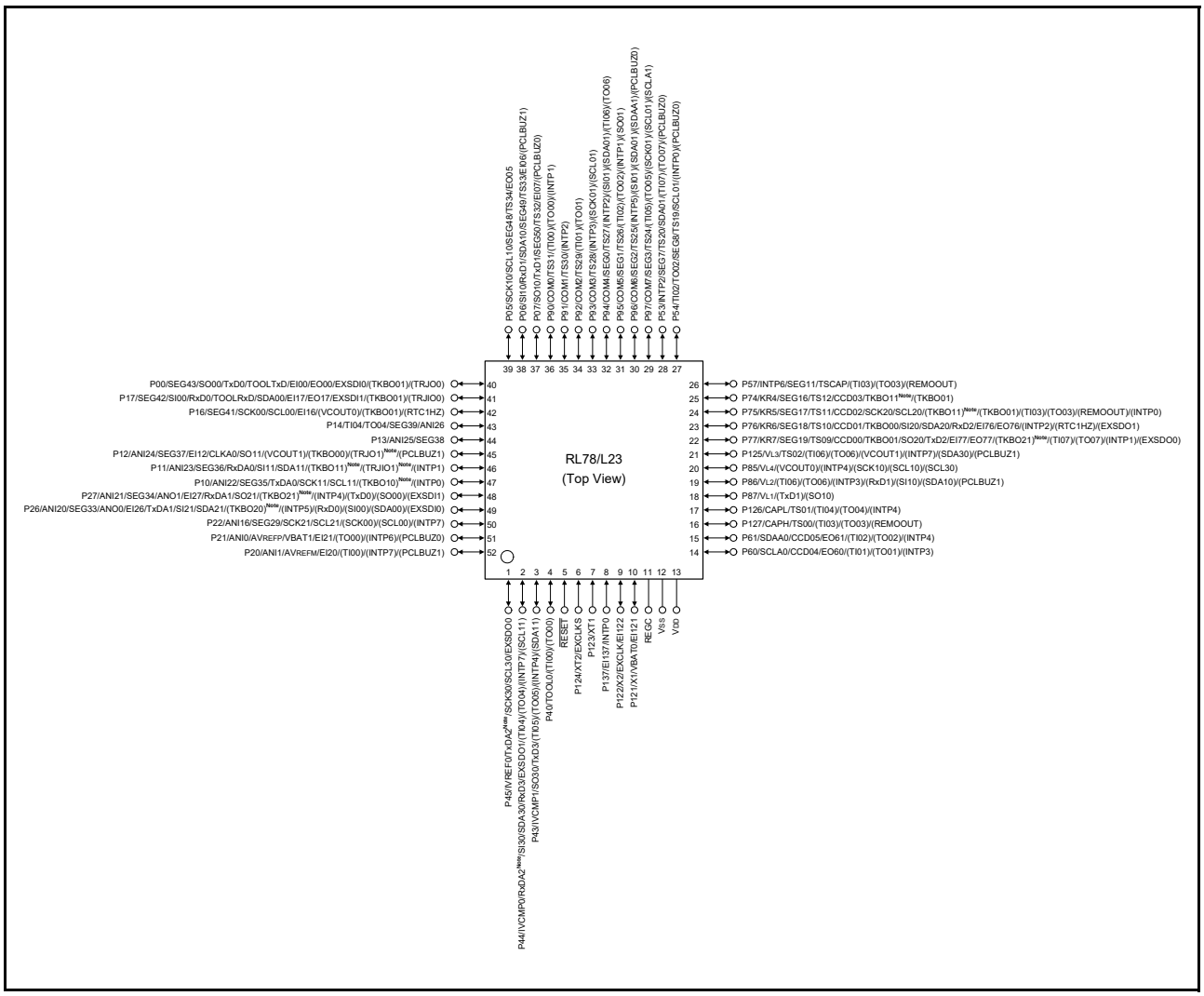
Table 1 - 3 Multiplexed Pin Functions of the 48-pin Products (3/3)

Pin Number	I/O			Power supply, system clock, and debugging	Analog Circuits				HMIs			Timers					Communications Interfaces		
48LFQFP, 48HWQFN	Digital port	Controlled current drive port	ELCL input/output port		A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	LCD controller/driver (LCD)	Interrupt	Key interrupt	Capacitive sensing unit (CTSU2La)	Timer array unit (TAU)	Timer RJ (TRJ)	16-bit timers KB40, KB41, and KB42	External signal sampler	Realtime clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
43	P10	—	—	—	ANI22	—	—	SEG35	(INTP0)	—	—	—	—	(TKBO10) **Note**	—	—	SCK11/ SCL11	—	TxDA0
44	P27	—	EI27	—	ANI21	ANO1	—	SEG34	(INTP4)	—	—	—	—	(TKBO21) **Note**	(EXSDI1)	—	(TxD0)/ (SO00)/ SO21	—	RxDA1
45	P26	—	EI26	—	ANI20	ANO0	—	SEG33	(INTP5)	—	—	—	—	(TKBO20) **Note**	(EXSDI0)	—	SI21/ SDA21/ (RxD0)/ (SI00)/ (SDA00)	—	TxDA1
46	P22	—	—	—	ANI16	—	—	SEG29	(INTP7)	—	—	—	—	—	—	—	(SCK00)/ (SCL00)/ SCK21/ SCL21	—	—
47	P21	—	EI21	VBAT1/ (PCLBUZ0)	ANI0/ AV_{REFP}	—	—	—	(INTP6)	—	—	(TO00)	—	—	—	—	—	—	—
48	P20	—	EI20	(PCLBUZ1)	ANI1/ AV_{REFM}	—	—	—	(INTP7)	—	—	(TI00)	—	—	—	—	—	—	—

Note Not present in products with 128 or fewer Kbytes of code flash memory.

1.3.3 52-pin products

- 52-pin plastic LQFP (10 × 10 mm, 0.65-mm pitch)



Note Not present in products with 128 or fewer Kbytes of code flash memory.

Caution **Connect the REGC pin to Vss via a capacitor (0.47 to 1 µF).**

Remark 1. For pin identification, see **1.4 Pin Identification**.

Remark 2. Pin functions in parentheses can be assigned via settings in the peripheral I/O redirection registers (PIORx). For details, see **4.3.10 Peripheral I/O redirection registers (PIORx)** in the RL78/L23 User's Manual.

Table 1 - 4 Multiplexed Pin Functions of the 52-pin Products (1/3)

Pin Number	I/O			Power supply, system clock, and debugging	Analog Circuits				HMIs			Timers					Communications Interfaces		
52LQFP	Digital port	Controlled current drive port	ELCL input/output port		A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	LCD controller/driver (LCD)	Interrupt	Key interrupt	Capacitive sensing unit (CTSU2La)	Timer array unit (TAU)	Timer RJ (TRJ)	16-bit timers KB40, KB41, and KB42	External signal sampler	Realtime clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
1	P45	—	—	—	—	—	IVREF0	—	—	—	—	—	—	—	EXSDO0	—	SCK30/ SCL30	—	TxDA2 **Note**
2	P44	—	—	—	—	—	IVCMP0	—	(INTP7)	—	—	(TI04)/ (TO04)	—	—	EXSDO1	—	SI30/ SDA30/ (SCL11)/ RxD3	—	RxDA2 **Note**
3	P43	—	—	—	—	—	IVCMP1	—	(INTP4)	—	—	(TI05)/ (TO05)	—	—	—	—	SO30/ (SDA11)/ TxD3	—	—
4	P40	—	—	TOOL0	—	—	—	—	—	—	—	(TI00)/ (TO00)	—	—	—	—	—	—	—
5	—	—	—	$\overline{\text{RESET}}$	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
6	P124	—	—	XT2/ EXCLKS	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
7	P123	—	—	XT1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
8	P137	—	EI137	—	—	—	—	—	INTP0	—	—	—	—	—	—	—	—	—	—
9	P122	—	EI122	X2/EXCLK	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
10	P121	—	EI121	X1/VBAT0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
11	—	—	—	REGC	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
12	—	—	—	V_{SS}	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
13	—	—	—	V_{DD}	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
14	P60	CCD04	EO60	—	—	—	—	—	(INTP3)	—	—	(TI01)/ (TO01)	—	—	—	—	—	SCLA0	—
15	P61	CCD05	EO61	—	—	—	—	—	(INTP4)	—	—	(TI02)/ (TO02)	—	—	—	—	—	SDAA0	—
16	P127	—	—	—	—	—	—	CAPH	—	—	TS00	(TI03)/ (TO03)/ (REMOOUT)	—	—	—	—	—	—	—
17	P126	—	—	—	—	—	—	CAPL	(INTP4)	—	TS01	(TI04)/ (TO04)	—	—	—	—	—	—	—
18	P87	—	—	—	—	—	—	V_{L1}	—	—	—	—	—	—	—	—	(TxD1)/ (SO10)	—	—
19	P86	—	—	(PCLBUZ1)	—	—	—	V_{L2}	(INTP3)	—	—	(TI06)/ (TO06)	—	—	—	—	(RxD1)/ (SI10)/ (SDA10)	—	—
20	P85	—	—	—	—	—	(VCOUT0)	V_{L4}	(INTP4)	—	—	—	—	—	—	—	(SCK10)/ (SCL10)/ (SCL30)	—	—
21	P125	—	—	(PCLBUZ1)	—	—	(VCOUT1)	V_{L3}	(INTP7)	—	TS02	(TI06)/ (TO06)	—	—	—	—	(SDA30)	—	—
22	P77	CCD00	EI77/ EO77	—	—	—	—	SEG19	(INTP1)	KR7	TS09	(TI07)/ (TO07)	—	TKBO01/ (TKBO21) **Note**	(EXSDO0)	—	SO20/ TxD2	—	—

Table 1 - 4 Multiplexed Pin Functions of the 52-pin Products (2/3)

Pin Number	I/O			Power supply, system clock, and debugging	Analog Circuits				HMIs			Timers					Communications Interfaces		
52LQFP	Digital port	Controlled current drive port	ELCL input/output port		A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	LCD controller/driver (LCD)	Interrupt	Key interrupt	Capacitive sensing unit (CTSU2La)	Timer array unit (TAU)	Timer RJ (TRJ)	16-bit timers KB40, KB41, and KB42	External signal sampler	Realtime clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
23	P76	CCD01	EI76/ EO76	—	—	—	—	SEG18	(INTP2)	KR6	TS10	—	—	TKBO00	(EXSDO1)	(RTC1HZ)	SI20/ SDA20/ RxD2	—	—
24	P75	CCD02	—	—	—	—	—	SEG17	(INTP0)	KR5	TS11	(TI03)/ (TO03)/ (REMOOUT)	—	(TKBO11) **Note**/ (TKBO01)	—	—	SCK20/ SCL20	—	—
25	P74	CCD03	—	—	—	—	—	SEG16	—	KR4	TS12	—	—	TKBO11 **Note**/ (TKBO01)	—	—	—	—	—
26	P57	—	—	—	—	—	—	SEG11	INTP6	—	TSCAP	(TI03)/ (TO03)/ (REMOOUT)	—	—	—	—	—	—	—
27	P54	—	—	(PCLBUZ0)	—	—	—	SEG8	(INTP0)	—	TS19	TI02/ TO02	—	—	—	—	SCL01	—	—
28	P53	—	—	(PCLBUZ0)	—	—	—	SEG7	INTP2	—	TS20	(TI07)/ (TO07)	—	—	—	—	SDA01	—	—
29	P97	—	—	—	—	—	—	SEG3/ COM7	—	—	TS24	(TI05)/ (TO05)	—	—	—	—	(SCK01)/ (SCL01)	(SCLA1)	—
30	P96	—	—	(PCLBUZ0)	—	—	—	SEG2/ COM6	(INTP5)	—	TS25	—	—	—	—	—	(SI01)/ (SDA01)	(SDAA1)	—
31	P95	—	—	—	—	—	—	SEG1/ COM5	(INTP1)	—	TS26	(TI02)/ (TO02)	—	—	—	—	(SO01)	—	—
32	P94	—	—	—	—	—	—	SEG0/ COM4	(INTP2)	—	TS27	(TI06)/ (TO06)	—	—	—	—	(SI01)/ (SDA01)	—	—
33	P93	—	—	—	—	—	—	COM3	(INTP3)	—	TS28	—	—	—	—	—	(SCK01)/ (SCL01)	—	—
34	P92	—	—	—	—	—	—	COM2	—	—	TS29	(TI01)/ (TO01)	—	—	—	—	—	—	—
35	P91	—	—	—	—	—	—	COM1	(INTP2)	—	TS30	—	—	—	—	—	—	—	—
36	P90	—	—	—	—	—	—	COM0	(INTP1)	—	TS31	(TI00)/ (TO00)	—	—	—	—	—	—	—
37	P07	—	EI07	(PCLBUZ0)	—	—	—	SEG50	—	—	TS32	—	—	—	—	—	SO10/ TxD1	—	—
38	P06	—	EI06	(PCLBUZ1)	—	—	—	SEG49	—	—	TS33	—	—	—	—	—	SI10/ RxD1/ SDA10	—	—
39	P05	—	EO05	—	—	—	—	SEG48	—	—	TS34	—	—	—	—	—	SCK10/ SCL10	—	—
40	P00	—	EI00/ EO00	TOOLTxD	—	—	—	SEG43	—	—	—	—	(TRJO0)	(TKBO01)	EXSDI0	—	SO00/ TxD0	—	—
41	P17	—	EI17/ EO17	TOOLRxD	—	—	—	SEG42	—	—	—	—	(TRJIO0)	(TKBO01)	EXSDI1	—	SI00/ RxD0/ SDA00	—	—

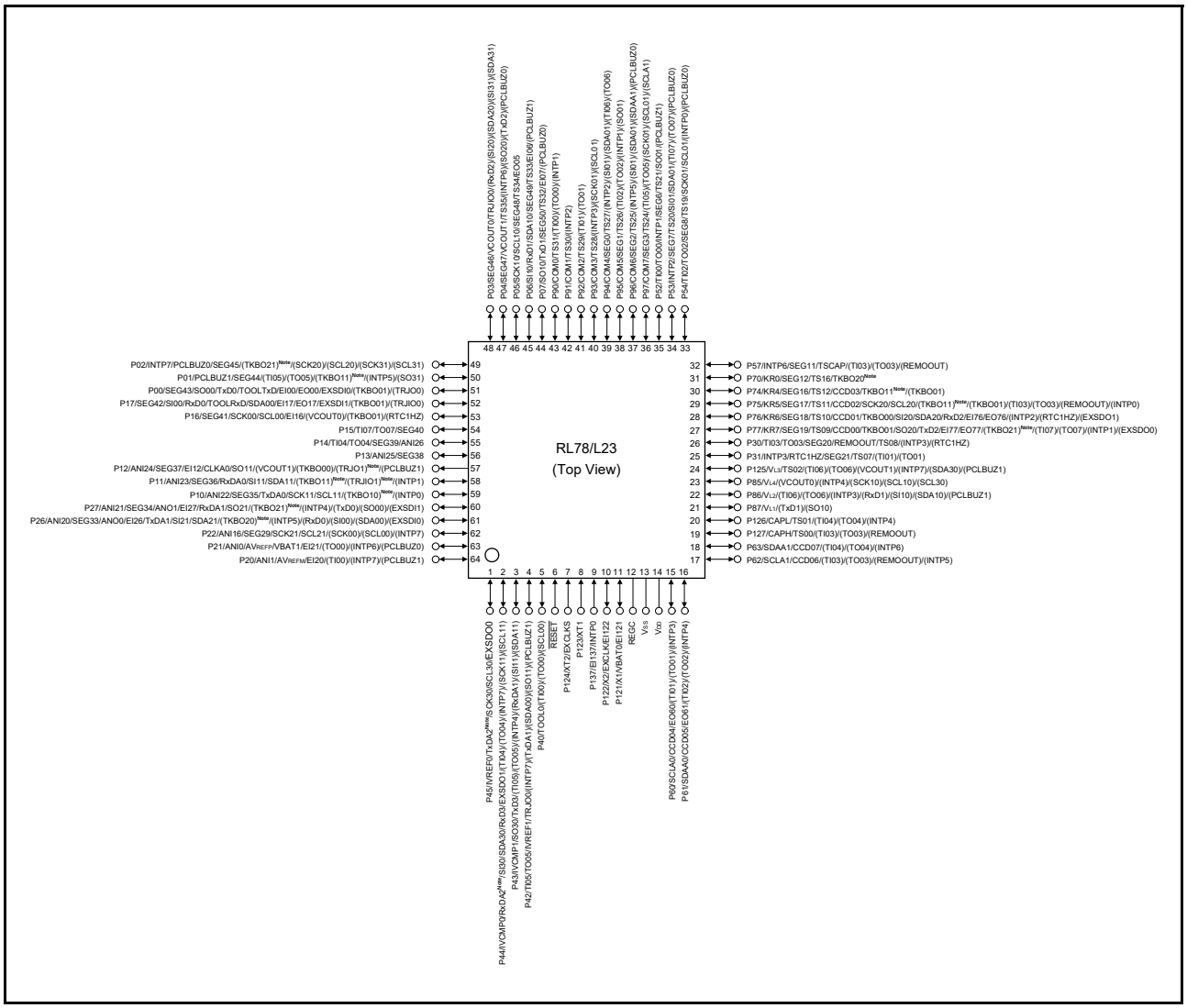
Table 1 - 4 Multiplexed Pin Functions of the 52-pin Products (3/3)

Pin Number	I/O			Power supply, system clock, and debugging	Analog Circuits				HMIs			Timers					Communications Interfaces		
52LQFP	Digital port	Controlled current drive port	ELCL input/output port		A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	LCD controller/driver (LCD)	Interrupt	Key interrupt	Capacitive sensing unit (CTSU2La)	Timer array unit (TAU)	Timer RJ (TRJ)	16-bit timers KB40, KB41, and KB42	External signal sampler	Realtime clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
42	P16	—	EI16	—	—	—	(VCOUT0)	SEG41	—	—	—	—	—	(TKBO01)	—	(RTC1HZ)	SCK00/ SCL00	—	—
43	P14	—	—	—	ANI26	—	—	SEG39	—	—	—	TI04/ TO04	—	—	—	—	—	—	—
44	P13	—	—	—	ANI25	—	—	SEG38	—	—	—	—	—	—	—	—	—	—	—
45	P12	—	EI12	(PCLBUZ1)	ANI24	—	(VCOUT1)	SEG37	—	—	—	—	(TRJO1) **Note**	(TKBO00)	—	—	SO11	—	CLKA0
46	P11	—	—	—	ANI23	—	—	SEG36	(INTP1)	—	—	—	(TRJIO1) **Note**	(TKBO11) **Note**	—	—	SI11/ SDA11	—	RxDA0
47	P10	—	—	—	ANI22	—	—	SEG35	(INTP0)	—	—	—	—	(TKBO10) **Note**	—	—	SCK11/ SCL11	—	TxDA0
48	P27	—	EI27	—	ANI21	ANO1	—	SEG34	(INTP4)	—	—	—	—	(TKBO21) **Note**	(EXSDI1)	—	(TxD0)/ (SO00)/ SO21	—	RxDA1
49	P26	—	EI26	—	ANI20	ANO0	—	SEG33	(INTP5)	—	—	—	—	(TKBO20) **Note**	(EXSDI0)	—	SI21/ SDA21/ (RxD0)/ (SI00)/ (SDA00)	—	TxDA1
50	P22	—	—	—	ANI16	—	—	SEG29	(INTP7)	—	—	—	—	—	—	—	(SCK00)/ (SCL00)/ SCK21/ SCL21	—	—
51	P21	—	EI21	VBAT1/ (PCLBUZ0)	ANI0/ AV_{REFP}	—	—	—	(INTP6)	—	—	(TO00)	—	—	—	—	—	—	—
52	P20	—	EI20	(PCLBUZ1)	ANI1/ AV_{REFM}	—	—	—	(INTP7)	—	—	(TI00)	—	—	—	—	—	—	—

Note Not present in products with 128 or fewer Kbytes of code flash memory.

1.3.4 64-pin products

- 64-pin plastic LQFP (12 × 12 mm, 0.65-mm pitch)
- 64-pin plastic LFQFP (10 × 10 mm, 0.50-mm pitch)



Note Not present in products with 128 or fewer Kbytes of code flash memory.

Caution **Connect the REGC pin to Vss via a capacitor (0.47 to 1 µF).**

Remark 1. For pin identification, see **1.4 Pin Identification**.

Remark 2. Pin functions in parentheses can be assigned via settings in the peripheral I/O redirection registers (PIORx). For details, see **4.3.10 Peripheral I/O redirection registers (PIORx)** in the RL78/L23 User's Manual.

Table 1 - 5 Multiplexed Pin Functions of the 64-pin Products (1/4)

Pin Number	I/O				Analog Circuits				HMIs			Timers					Communications Interfaces		
64LQFP, 64LFQFP	Digital port	Controlled current drive port	ELCL input/output port	Power supply, system clock, and debugging	A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	LCD controller/driver (LCD)	Interrupt	Key interrupt	Capacitive sensing unit (CTSU2La)	Timer array unit (TAU)	Timer RJ (TRJ)	16-bit timers KB40, KB41, and KB42	External signal sampler	Realtime clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
1	P45	—	—	—	—	—	IVREF0	—	—	—	—	—	—	—	EXSDO0	—	SCK30/ SCL30	—	TxDA2 **Note**
2	P44	—	—	—	—	—	IVCMP0	—	(INTP7)	—	—	(TI04)/ (TO04)	—	—	EXSDO1	—	SI30/ SDA30/ (SCL11)/ (SCK11)/ RxD3	—	RxDA2 **Note**
3	P43	—	—	—	—	—	IVCMP1	—	(INTP4)	—	—	(TI05)/ (TO05)	—	—	—	—	SO30/ (SI11)/ (SDA11)/ TxD3	—	(RxDA1)
4	P42	—	—	(PCLBUZ1)	—	—	IVREF1	—	(INTP7)	—	—	TI05/ TO05	TRJO0	—	—	—	(SDA00)/ (SO11)	—	(TxDA1)
5	P40	—	—	TOOL0	—	—	—	—	—	—	—	(TI00)/ (TO00)	—	—	—	—	(SCL00)	—	—
6	—	—	—	$\overline{\text{RESET}}$	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
7	P124	—	—	XT2/ EXCLKS	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
8	P123	—	—	XT1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
9	P137	—	EI137	—	—	—	—	—	INTP0	—	—	—	—	—	—	—	—	—	—
10	P122	—	EI122	X2/EXCLK	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
11	P121	—	EI121	X1/VBAT0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
12	—	—	—	REGC	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
13	—	—	—	V_{SS}	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
14	—	—	—	V_{DD}	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
15	P60	CCD04	EO60	—	—	—	—	—	(INTP3)	—	—	(TI01)/ (TO01)	—	—	—	—	—	SCLA0	—
16	P61	CCD05	EO61	—	—	—	—	—	(INTP4)	—	—	(TI02)/ (TO02)	—	—	—	—	—	SDAA0	—
17	P62	CCD06	—	—	—	—	—	—	(INTP5)	—	—	(TI03)/ (TO03)/ (REMOOUT)	—	—	—	—	—	SCLA1	—
18	P63	CCD07	—	—	—	—	—	—	(INTP6)	—	—	(TI04)/ (TO04)	—	—	—	—	—	SDAA1	—
19	P127	—	—	—	—	—	—	CAPH	—	—	TS00	(TI03)/ (TO03)/ (REMOOUT)	—	—	—	—	—	—	—
20	P126	—	—	—	—	—	—	CAPL	(INTP4)	—	TS01	(TI04)/ (TO04)	—	—	—	—	—	—	—
21	P87	—	—	—	—	—	—	V_{L1}	—	—	—	—	—	—	—	—	(TxD1)/ (SO10)	—	—
22	P86	—	—	(PCLBUZ1)	—	—	—	V_{L2}	(INTP3)	—	—	(TI06)/ (TO06)	—	—	—	—	(RxD1)/ (SI10)/ (SDA10)	—	—

Table 1 - 5 Multiplexed Pin Functions of the 64-pin Products (2/4)

Pin Number	I/O			Power supply, system clock, and debugging	Analog Circuits				HMIs			Timers					Communications Interfaces		
64LQFP, 64LFQFP	Digital port	Controlled current drive port	ELCL input/output port		A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	LCD controller/driver (LCD)	Interrupt	Key interrupt	Capacitive sensing unit (CTSU2La)	Timer array unit (TAU)	Timer RJ (TRJ)	16-bit timers KB40, KB41, and KB42	External signal sampler	Realtime clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
23	P85	—	—	—	—	—	(VCOUT0)	VL4	(INTP4)	—	—	—	—	—	—	—	(SCK10)/ (SCL10)/ (SCL30)	—	—
24	P125	—	—	(PCLBUZ1)	—	—	(VCOUT1)	VL3	(INTP7)	—	TS02	(TI06)/ (TO06)	—	—	—	—	(SDA30)	—	—
25	P31	—	—	—	—	—	—	SEG21	INTP3	—	TS07	(TI01)/ (TO01)	—	—	—	RTC1HZ	—	—	—
26	P30	—	—	—	—	—	—	SEG20	(INTP3)	—	TS08	TI03/ TO03/ REMOOUT	—	—	—	(RTC1HZ)	—	—	—
27	P77	CCD00	EI77/ EO77	—	—	—	—	SEG19	(INTP1)	KR7	TS09	(TI07)/ (TO07)	—	TKBO01/ (TKBO21) **Note**	(EXSDO0)	—	SO20/ TxD2	—	—
28	P76	CCD01	EI76/ EO76	—	—	—	—	SEG18	(INTP2)	KR6	TS10	—	—	TKBO00	(EXSDO1)	(RTC1HZ)	SI20/ SDA20/ RxD2	—	—
29	P75	CCD02	—	—	—	—	—	SEG17	(INTP0)	KR5	TS11	(TI03)/ (TO03)/ (REMOOUT)	—	(TKBO11) **Note**/ (TKBO01)	—	—	SCK20/ SCL20	—	—
30	P74	CCD03	—	—	—	—	—	SEG16	—	KR4	TS12	—	—	TKBO11 **Note**/ (TKBO01)	—	—	—	—	—
31	P70	—	—	—	—	—	—	SEG12	—	KR0	TS16	—	—	TKBO20 **Note**	—	—	—	—	—
32	P57	—	—	—	—	—	—	SEG11	INTP6	—	TSCAP	(TI03)/ (TO03)/ (REMOOUT)	—	—	—	—	—	—	—
33	P54	—	—	(PCLBUZ0)	—	—	—	SEG8	(INTP0)	—	TS19	TI02/ TO02	—	—	—	—	SCL01/ SCK01	—	—
34	P53	—	—	(PCLBUZ0)	—	—	—	SEG7	INTP2	—	TS20	(TI07)/ (TO07)	—	—	—	—	SI01/ SDA01	—	—
35	P52	—	—	(PCLBUZ1)	—	—	—	SEG6	INTP1	—	TS21	TI00/ TO00	—	—	—	—	SO01	—	—
36	P97	—	—	—	—	—	—	SEG3/ COM7	—	—	TS24	(TI05)/ (TO05)	—	—	—	—	(SCK01)/ (SCL01)	(SCLA1)	—
37	P96	—	—	(PCLBUZ0)	—	—	—	SEG2/ COM6	(INTP5)	—	TS25	—	—	—	—	—	(SI01)/ (SDA01)	(SDAA1)	—
38	P95	—	—	—	—	—	—	SEG1/ COM5	(INTP1)	—	TS26	(TI02)/ (TO02)	—	—	—	—	(SO01)	—	—
39	P94	—	—	—	—	—	—	SEG0/ COM4	(INTP2)	—	TS27	(TI06)/ (TO06)	—	—	—	—	(SI01)/ (SDA01)	—	—
40	P93	—	—	—	—	—	—	COM3	(INTP3)	—	TS28	—	—	—	—	—	(SCK01)/ (SCL01)	—	—
41	P92	—	—	—	—	—	—	COM2	—	—	TS29	(TI01)/ (TO01)	—	—	—	—	—	—	—

Table 1 - 5 Multiplexed Pin Functions of the 64-pin Products (3/4)

Pin Number	I/O			Power supply, system clock, and debugging	Analog Circuits				HMIs			Timers					Communications Interfaces		
64LQFP, 64LFQFP	Digital port	Controlled current drive port	ELCL input/output port		A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	LCD controller/driver (LCD)	Interrupt	Key interrupt	Capacitive sensing unit (CTSU2La)	Timer array unit (TAU)	Timer RJ (TRJ)	16-bit timers KB40, KB41, and KB42	External signal sampler	Realtime clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
42	P91	—	—	—	—	—	—	COM1	(INTP2)	—	TS30	—	—	—	—	—	—	—	—
43	P90	—	—	—	—	—	—	COM0	(INTP1)	—	TS31	(TI00)/ (TO00)	—	—	—	—	—	—	—
44	P07	—	EI07	(PCLBUZ0)	—	—	—	SEG50	—	—	TS32	—	—	—	—	—	SO10/ TxD1	—	—
45	P06	—	EI06	(PCLBUZ1)	—	—	—	SEG49	—	—	TS33	—	—	—	—	—	SI10/ RxD1/ SDA10	—	—
46	P05	—	EO05	—	—	—	—	SEG48	—	—	TS34	—	—	—	—	—	SCK10/ SCL10	—	—
47	P04	—	—	(PCLBUZ0)	—	—	VCOUT1	SEG47	(INTP6)	—	TS35	—	—	—	—	—	(TxD2)/ (SO20)	—	—
48	P03	—	—	—	—	—	VCOUT0	SEG46	—	—	—	—	TRJIO0	—	—	—	(SI31)/ (SDA31)/ (RxD2)/ (SI20)/ (SDA20)	—	—
49	P02	—	—	PCLBUZ0	—	—	—	SEG45	INTP7	—	—	—	—	(TKBO21) **Note**	—	—	(SCK31)/ (SCL31)/ (SCK20)/ (SCL20)	—	—
50	P01	—	—	PCLBUZ1	—	—	—	SEG44	(INTP5)	—	—	(TI05)/ (TO05)		(TKBO11) **Note**	—	—	(SO31)	—	—
51	P00	—	EI00/ EO00	TOOLTxD	—	—	—	SEG43	—	—	—	—	(TRJO0)	(TKBO01)	EXSDI0	—	SO00/ TxD0	—	—
52	P17	—	EI17/ EO17	TOOLRxD	—	—	—	SEG42	—	—	—	—	(TRJIO0)	(TKBO01)	EXSDI1	—	SI00/ RxD0/ SDA00	—	—
53	P16	—	EI16	—	—	—	(VCOUT0)	SEG41	—	—	—	—	—	(TKBO01)	—	(RTC1HZ)	SCK00/ SCL00	—	—
54	P15	—	—	—	—	—	—	SEG40	—	—	—	TI07/ TO07	—	—	—	—	—	—	—
55	P14	—	—	—	ANI26	—	—	SEG39	—	—	—	TI04/ TO04	—	—	—	—	—	—	—
56	P13	—	—	—	ANI25	—	—	SEG38	—	—	—	—	—	—	—	—	—	—	—
57	P12	—	EI12	(PCLBUZ1)	ANI24	—	(VCOUT1)	SEG37	—	—	—	—	(TRJO1) **Note**	(TKBO00)	—	—	SO11	—	CLKA0
58	P11	—	—	—	ANI23	—	—	SEG36	(INTP1)	—	—	—	(TRJIO1) **Note**	(TKBO11) **Note**	—	—	SI11/ SDA11	—	RxDA0
59	P10	—	—	—	ANI22	—	—	SEG35	(INTP0)	—	—	—	—	(TKBO10) **Note**	—	—	SCK11/ SCL11	—	TxDA0
60	P27	—	EI27	—	ANI21	ANO1	—	SEG34	(INTP4)	—	—	—	—	(TKBO21) **Note**	(EXSDI1)	—	(TxD0)/ (SO00)/ SO21	—	RxDA1

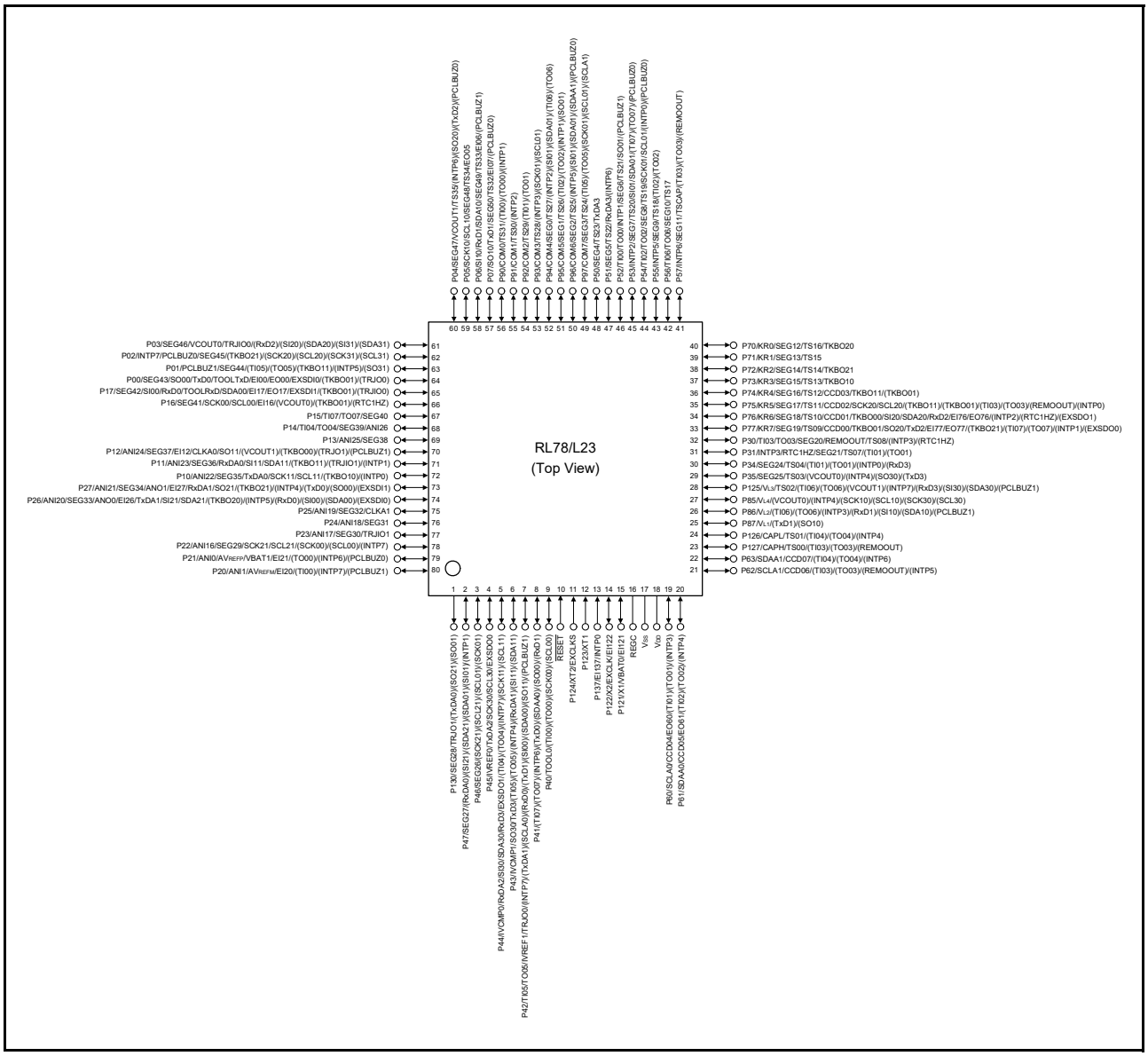
Table 1 - 5 Multiplexed Pin Functions of the 64-pin Products (4/4)

Pin Number	I/O			Power supply, system clock, and debugging	Analog Circuits				HMIs			Timers					Communications Interfaces		
64LQFP, 64LFQFP	Digital port	Controlled current drive port	ELCL input/output port		A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	LCD controller/driver (LCD)	Interrupt	Key interrupt	Capacitive sensing unit (CTSU2La)	Timer array unit (TAU)	Timer RJ (TRJ)	16-bit timers KB40, KB41, and KB42	External signal sampler	Realtime clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
61	P26	—	EI26	—	ANI20	ANO0	—	SEG33	(INTP5)	—	—	—	—	(TKBO20) **Note**	(EXSDI0)	—	SI21/ SDA21/ (RxD0)/ (SI00)/ (SDA00)	—	TxDA1
62	P22	—	—	—	ANI16	—	—	SEG29	(INTP7)	—	—	—	—	—	—	—	(SCK00)/ (SCL00)/ SCK21/ SCL21	—	—
63	P21	—	EI21	VBAT1/ (PCLBUZ0)	ANI0/ AVREFP	—	—	—	(INTP6)	—	—	(TO00)	—	—	—	—	—	—	—
64	P20	—	EI20	(PCLBUZ1)	ANI1/ AVREFM	—	—	—	(INTP7)	—	—	(TI00)	—	—	—	—	—	—	—

Note Not present in products with 128 or fewer Kbytes of code flash memory.

1.3.5 80-pin products

- 80-pin plastic LQFP (14 × 14 mm, 0.65-mm pitch)
- 80-pin plastic LFQFP (12 × 12 mm, 0.50-mm pitch)



Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 µF).

Remark 1. For pin identification, see **1.4 Pin Identification**.

Remark 2. Pin functions in parentheses can be assigned via settings in the peripheral I/O redirection registers (PIORx). For details, see **4.3.10 Peripheral I/O redirection registers (PIORx)** in the RL78/L23 User's Manual.

Table 1 - 6 Multiplexed Pin Functions of the 80-pin Products (1/4)

Pin Number	I/O			Power supply, system clock, and debugging	Analog Circuits				HMIs			Timers					Communications Interfaces		
80LQFP, 80LFQFP	Digital port	Controlled current drive port	ELCL input/output port		A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	LCD controller/driver (LCD)	Interrupt	Key interrupt	Capacitive sensing unit (CTSU2La)	Timer array unit (TAU)	Timer RJ (TRJ)	16-bit timers KB40, KB41, and KB42	External signal sampler	Realtime clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
1	P130	—	—	—	—	—	—	SEG28	—	—	—	—	TRJO1	—	—	—	(SO21)/ (SO01)	—	(TxDA0)
2	P47	—	—	—	—	—	—	SEG27	(INTP1)	—	—	—	—	—	—	—	(SI01)/ (SI21)/ (SDA01)/ (SDA21)	—	(RxDA0)
3	P46	—	—	—	—	—	—	SEG26	—	—	—	—	—	—	—	—	(SCL01)/ (SCK01)/ (SCK21)/ (SCL21)	—	—
4	P45	—	—	—	—	—	IVREF0	—	—	—	—	—	—	—	EXSDO0	—	SCK30/ SCL30	—	TxDA2
5	P44	—	—	—	—	—	IVCMP0	—	(INTP7)	—	—	(TI04)/ (TO04)	—	—	EXSDO1	—	SI30/ SDA30/ (SCL11)/ (SCK11)/ RxD3	—	RxDA2
6	P43	—	—	—	—	—	IVCMP1	—	(INTP4)	—	—	(TI05)/ (TO05)	—	—	—	—	SO30/ (SI11)/ (SDA11)/ TxD3	—	(RxDA1)
7	P42	—	—	(PCLBUZ1)	—	—	IVREF1	—	(INTP7)	—	—	TI05/ TO05	TRJO0	—	—	—	(SI00)/ (RxD0)/ (SDA00)/ (SO11)/ (TxD1)	(SCLA0)	(TxDA1)
8	P41	—	—	—	—	—	—	—	(INTP6)	—	—	(TI07)/ (TO07)	—	—	—	—	(SO00)/ (TxD0)/ (RxD1)	(SDAA0)	—
9	P40	—	—	TOOL0	—	—	—	—	—	—	—	(TI00)/ (TO00)	—	—	—	—	(SCL00)/ (SCK00)	—	—
10	—	—	—	$\overline{\text{RESET}}$	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
11	P124	—	—	XT2/ EXCLKS	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
12	P123	—	—	XT1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
13	P137	—	EI137	—	—	—	—	—	INTP0	—	—	—	—	—	—	—	—	—	—
14	P122	—	EI122	X2/EXCLK	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
15	P121	—	EI121	X1/VBAT0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
16	—	—	—	REGC	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
17	—	—	—	V_{SS}	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
18	—	—	—	V_{DD}	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
19	P60	CCD04	EO60	—	—	—	—	—	(INTP3)	—	—	(TI01)/ (TO01)	—	—	—	—	—	SCLA0	—
20	P61	CCD05	EO61	—	—	—	—	—	(INTP4)	—	—	(TI02)/ (TO02)	—	—	—	—	—	SDAA0	—
21	P62	CCD06	—	—	—	—	—	—	(INTP5)	—	—	(TI03)/ (TO03)/ (REMOOUT)	—	—	—	—	—	SCLA1	—
22	P63	CCD07	—	—	—	—	—	—	(INTP6)	—	—	(TI04)/ (TO04)	—	—	—	—	—	SDAA1	—

Table 1 - 6 Multiplexed Pin Functions of the 80-pin Products (2/4)

Pin Number	I/O			Power supply, system clock, and debugging	Analog Circuits				HMIs			Timers					Communications Interfaces		
80LQFP, 80LFQFP	Digital port	Controlled current drive port	ELCL input/output port		A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	LCD controller/driver (LCD)	Interrupt	Key interrupt	Capacitive sensing unit (CTSU2La)	Timer array unit (TAU)	Timer RJ (TRJ)	16-bit timers KB40, KB41, and KB42	External signal sampler	Realtime clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
23	P127	—	—	—	—	—	—	CAPH	—	—	TS00	(TI03)/ (TO03)/ (REMOOUT)	—	—	—	—	—	—	—
24	P126	—	—	—	—	—	—	CAPL	(INTP4)	—	TS01	(TI04)/ (TO04)	—	—	—	—	—	—	—
25	P87	—	—	—	—	—	—	V_{L1}	—	—	—	—	—	—	—	—	(TxD1)/ (SO10)	—	—
26	P86	—	—	(PCLBUZ1)	—	—	—	V_{L2}	(INTP3)	—	—	(TI06)/ (TO06)	—	—	—	—	(RxD1)/ (SI10)/ (SDA10)	—	—
27	P85	—	—	—	—	—	(VCOUT0)	V_{L4}	(INTP4)	—	—	—	—	—	—	—	(SCK10)/ (SCL10)/ (SCK30)/ (SCL30)	—	—
28	P125	—	—	(PCLBUZ1)	—	—	(VCOUT1)	V_{L3}	(INTP7)	—	TS02	(TI06)/ (TO06)	—	—	—	—	(SI30)/ (RxD3)/ (SDA30)	—	—
29	P35	—	—	—	—	—	(VCOUT0)	SEG25	(INTP4)	—	TS03	—	—	—	—	—	(SO30)/ (TxD3)	—	—
30	P34	—	—	—	—	—	—	SEG24	(INTP0)	—	TS04	(TI01)/ (TO01)	—	—	—	—	(RxD3)	—	—
31	P31	—	—	—	—	—	—	SEG21	INTP3	—	TS07	(TI01)/ (TO01)	—	—	—	RTC1HZ	—	—	—
32	P30	—	—	—	—	—	—	SEG20	(INTP3)	—	TS08	TI03/ TO03/ REMOOUT	—	—	—	(RTC1HZ)	—	—	—
33	P77	CCD00	EI77/ EO77	—	—	—	—	SEG19	(INTP1)	KR7	TS09	(TI07)/ (TO07)	—	TKBO01/ (TKBO21)	(EXSDO0)	—	SO20/ TxD2	—	—
34	P76	CCD01	EI76/ EO76	—	—	—	—	SEG18	(INTP2)	KR6	TS10	—	—	TKBO00	(EXSDO1)	(RTC1HZ)	SI20/ SDA20/ RxD2	—	—
35	P75	CCD02	—	—	—	—	—	SEG17	(INTP0)	KR5	TS11	(TI03)/ (TO03)/ (REMOOUT)	—	(TKBO11)/ (TKBO01)	—	—	SCK20/ SCL20	—	—
36	P74	CCD03	—	—	—	—	—	SEG16	—	KR4	TS12	—	—	TKBO11/ (TKBO01)	—	—	—	—	—
37	P73	—	—	—	—	—	—	SEG15	—	KR3	TS13	—	—	TKBO10	—	—	—	—	—
38	P72	—	—	—	—	—	—	SEG14	—	KR2	TS14	—	—	TKBO21	—	—	—	—	—
39	P71	—	—	—	—	—	—	SEG13	—	KR1	TS15	—	—	—	—	—	—	—	—
40	P70	—	—	—	—	—	—	SEG12	—	KR0	TS16	—	—	TKBO20	—	—	—	—	—
41	P57	—	—	—	—	—	—	SEG11	INTP6	—	TSCAP	(TI03)/ (TO03)/ (REMOOUT)	—	—	—	—	—	—	—

Table 1 - 6 Multiplexed Pin Functions of the 80-pin Products (3/4)

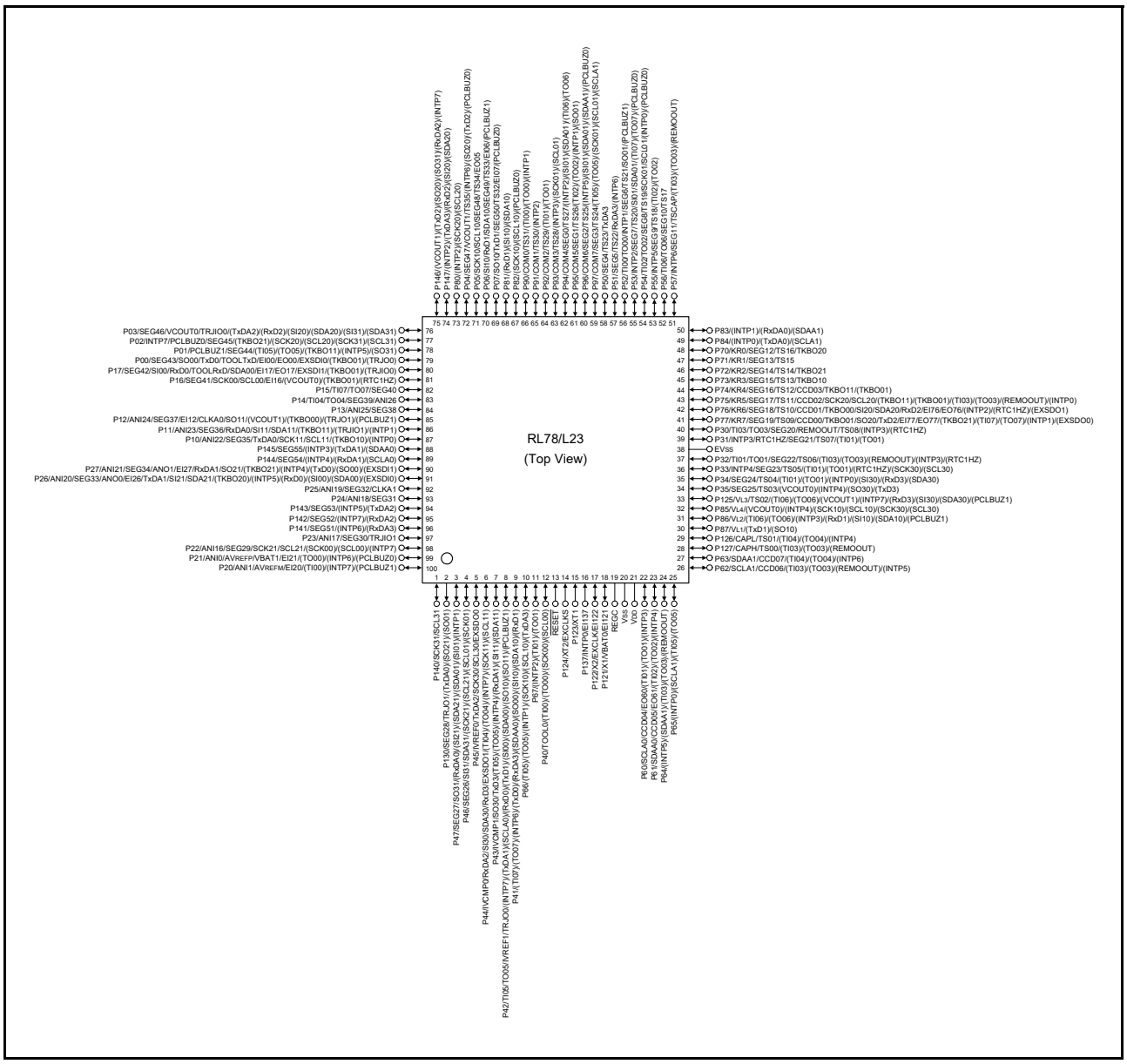
Pin Number	I/O			Power supply, system clock, and debugging	Analog Circuits				HMIs			Timers					Communications Interfaces		
80LQFP, 80LFQFP	Digital port	Controlled current drive port	ELCL input/output port		A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	LCD controller/driver (LCD)	Interrupt	Key interrupt	Capacitive sensing unit (CTSU2La)	Timer array unit (TAU)	Timer RJ (TRJ)	16-bit timers KB40, KB41, and KB42	External signal sampler	Realtime clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
42	P56	—	—	—	—	—	—	SEG10	—	—	TS17	TI06/ TO06	—	—	—	—	—	—	—
43	P55	—	—	—	—	—	—	SEG9	INTP5	—	TS18	(TI02)/ (TO02)	—	—	—	—	—	—	—
44	P54	—	—	(PCLBUZ0)	—	—	—	SEG8	(INTP0)	—	TS19	TI02/ TO02	—	—	—	—	SCL01/ SCK01	—	—
45	P53	—	—	(PCLBUZ0)	—	—	—	SEG7	INTP2	—	TS20	(TI07)/ (TO07)	—	—	—	—	SI01/ SDA01	—	—
46	P52	—	—	(PCLBUZ1)	—	—	—	SEG6	INTP1	—	TS21	TI00/ TO00	—	—	—	—	SO01	—	—
47	P51	—	—	—	—	—	—	SEG5	(INTP6)	—	TS22	—	—	—	—	—	—	—	RxDA3
48	P50	—	—	—	—	—	—	SEG4	—	—	TS23	—	—	—	—	—	—	—	TxDA3
49	P97	—	—	—	—	—	—	SEG3/ COM7	—	—	TS24	(TI05)/ (TO05)	—	—	—	—	(SCK01)/ (SCL01)	(SCLA1)	—
50	P96	—	—	(PCLBUZ0)	—	—	—	SEG2/ COM6	(INTP5)	—	TS25	—	—	—	—	—	(SI01)/ (SDA01)	(SDAA1)	—
51	P95	—	—	—	—	—	—	SEG1/ COM5	(INTP1)	—	TS26	(TI02)/ (TO02)	—	—	—	—	(SO01)	—	—
52	P94	—	—	—	—	—	—	SEG0/ COM4	(INTP2)	—	TS27	(TI06)/ (TO06)	—	—	—	—	(SI01)/ (SDA01)	—	—
53	P93	—	—	—	—	—	—	COM3	(INTP3)	—	TS28	—	—	—	—	—	(SCK01)/ (SCL01)	—	—
54	P92	—	—	—	—	—	—	COM2	—	—	TS29	(TI01)/ (TO01)	—	—	—	—	—	—	—
55	P91	—	—	—	—	—	—	COM1	(INTP2)	—	TS30	—	—	—	—	—	—	—	—
56	P90	—	—	—	—	—	—	COM0	(INTP1)	—	TS31	(TI00)/ (TO00)	—	—	—	—	—	—	—
57	P07	—	EI07	(PCLBUZ0)	—	—	—	SEG50	—	—	TS32	—	—	—	—	—	SO10/ TxD1	—	—
58	P06	—	EI06	(PCLBUZ1)	—	—	—	SEG49	—	—	TS33	—	—	—	—	—	SI10/ RxD1/ SDA10	—	—
59	P05	—	EO05	—	—	—	—	SEG48	—	—	TS34	—	—	—	—	—	SCK10/ SCL10	—	—
60	P04	—	—	(PCLBUZ0)	—	—	VCOUT1	SEG47	(INTP6)	—	TS35	—	—	—	—	—	(TxD2)/ (SO20)	—	—
61	P03	—	—	—	—	—	VCOUT0	SEG46	—	—	—	—	TRJIO0	—	—	—	(SI31)/ (SDA31)/ (RxD2)/ (SI20)/ (SDA20)	—	—
62	P02	—	—	PCLBUZ0	—	—	—	SEG45	INTP7	—	—	—	—	(TKBO21)	—	—	(SCK31)/ (SCL31)/ (SCK20)/ (SCL20)	—	—
63	P01	—	—	PCLBUZ1	—	—	—	SEG44	(INTP5)	—	—	(TI05)/ (TO05)		(TKBO11)	—	—	(SO31)	—	—

Table 1 - 6 Multiplexed Pin Functions of the 80-pin Products (4/4)

Pin Number	I/O			Power supply, system clock, and debugging	Analog Circuits				HMIs			Timers					Communications Interfaces		
80LQFP, 80LFQFP	Digital port	Controlled current drive port	ELCL input/output port		A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	LCD controller/driver (LCD)	Interrupt	Key interrupt	Capacitive sensing unit (CTSU2La)	Timer array unit (TAU)	Timer RJ (TRJ)	16-bit timers KB40, KB41, and KB42	External signal sampler	Realtime clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
64	P00	—	EI00/ EO00	TOOLTxD	—	—	—	SEG43	—	—	—	—	(TRJO0)	(TKBO01)	EXSDI0	—	SO00/ TxD0	—	—
65	P17	—	EI17/ EO17	TOOLRxD	—	—	—	SEG42	—	—	—	—	(TRJIO0)	(TKBO01)	EXSDI1	—	SI00/ RxD0/ SDA00	—	—
66	P16	—	EI16	—	—	—	(VCOUT0)	SEG41	—	—	—	—	—	(TKBO01)	—	(RTC1HZ)	SCK00/ SCL00	—	—
67	P15	—	—	—	—	—	—	SEG40	—	—	—	TI07/ TO07	—	—	—	—	—	—	—
68	P14	—	—	—	ANI26	—	—	SEG39	—	—	—	TI04/ TO04	—	—	—	—	—	—	—
69	P13	—	—	—	ANI25	—	—	SEG38	—	—	—	—	—	—	—	—	—	—	—
70	P12	—	EI12	(PCLBUZ1)	ANI24	—	(VCOUT1)	SEG37	—	—	—	—	(TRJO1)	(TKBO00)	—	—	SO11	—	CLKA0
71	P11	—	—	—	ANI23	—	—	SEG36	(INTP1)	—	—	—	(TRJIO1)	(TKBO11)	—	—	SI11/ SDA11	—	RxDA0
72	P10	—	—	—	ANI22	—	—	SEG35	(INTP0)	—	—	—	—	(TKBO10)	—	—	SCK11/ SCL11	—	TxDA0
73	P27	—	EI27	—	ANI21	ANO1	—	SEG34	(INTP4)	—	—	—	—	(TKBO21)	(EXSDI1)	—	(TxD0)/ (SO00)/ SO21	—	RxDA1
74	P26	—	EI26	—	ANI20	ANO0	—	SEG33	(INTP5)	—	—	—	—	(TKBO20)	(EXSDI0)	—	SI21/ SDA21/ (RxD0)/ (SI00)/ (SDA00)	—	TxDA1
75	P25	—	—	—	ANI19	—	—	SEG32	—	—	—	—	—	—	—	—	—	—	CLKA1
76	P24	—	—	—	ANI18	—	—	SEG31	—	—	—	—	—	—	—	—	—	—	—
77	P23	—	—	—	ANI17	—	—	SEG30	—	—	—	—	TRJIO1	—	—	—	—	—	—
78	P22	—	—	—	ANI16	—	—	SEG29	(INTP7)	—	—	—	—	—	—	—	(SCK00)/ (SCL00)/ SCK21/ SCL21	—	—
79	P21	—	EI21	VBAT1/ (PCLBUZ0)	ANI0/ AVREFP	—	—	—	(INTP6)	—	—	(TO00)	—	—	—	—	—	—	—
80	P20	—	EI20	(PCLBUZ1)	ANI1/ AVREFM	—	—	—	(INTP7)	—	—	(TI00)	—	—	—	—	—	—	—

1.3.6 100-pin products

- 100-pin plastic LFQFP (14 × 14 mm, 0.50-mm pitch)



Caution 1. Connect the EVSS pin to the same ground as the VSS pin.

Caution 2. Connect the REGC pin to VSS via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see **1.4 Pin Identification**.

Remark 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to connect the VSS and EVSS pins to separate ground lines.

Remark 3. Pin functions in parentheses can be assigned via settings in the peripheral I/O redirection registers (PIORx). For details, see **4.3.10 Peripheral I/O redirection registers (PIORx)** in the RL78/L23 User's Manual.

Table 1 - 7 Multiplexed Pin Functions of the 100-pin Products (1/5)

Pin Number	I/O			Power supply, system clock, and debugging	Analog Circuits				HMIs			Timers					Communications Interfaces		
100LFQFP	Digital port	Controlled current drive port	ELCL input/output port		A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	LCD controller/driver (LCD)	Interrupt	Key interrupt	Capacitive sensing unit (CTSU2La)	Timer array unit (TAU)	Timer RJ (TRJ)	16-bit timers KB40, KB41, and KB42	External signal sampler	Realtime clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
1	P140	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SCK31/ SCL31	—	—
2	P130	—	—	—	—	—	—	SEG28	—	—	—	—	TRJO1	—	—	—	(SO21)/ (SO01)	—	(TxDA0)
3	P47	—	—	—	—	—	—	SEG27	(INTP1)	—	—	—	—	—	—	—	SO31/ (SI01)/ (SI21)/ (SDA01)/ (SDA21)	—	(RxDA0)
4	P46	—	—	—	—	—	—	SEG26	—	—	—	—	—	—	—	—	SI31/ SDA31/ (SCL01)/ (SCK01)/ (SCK21)/ (SCL21)	—	—
5	P45	—	—	—	—	—	IVREF0	—	—	—	—	—	—	—	EXSDO0	—	SCK30/ SCL30	—	TxDA2
6	P44	—	—	—	—	—	IVCMP0	—	(INTP7)	—	—	(TI04)/ (TO04)	—	—	EXSDO1	—	SI30/ SDA30/ (SCL11)/ (SCK11)/ RxD3	—	RxDA2
7	P43	—	—	—	—	—	IVCMP1	—	(INTP4)	—	—	(TI05)/ (TO05)	—	—	—	—	SO30/ (SI11)/ (SDA11)/ TxD3	—	(RxDA1)
8	P42	—	—	(PCLBUZ1)	—	—	IVREF1	—	(INTP7)	—	—	TI05/ TO05	TRJO0	—	—	—	(SI00)/ (RxD0)/ (SDA00)/ (SO11)/ (TxD1)/ (SO10)	(SCLA0)	(TxDA1)
9	P41	—	—	—	—	—	—	—	(INTP6)	—	—	(TI07)/ (TO07)	—	—	—	—	(SI10)/ (SO00)/ (TxD0)/ (SDA10)/ (RxD1)	(SDAA0)	(RxDA3)
10	P66	—	—	—	—	—	—	—	(INTP1)	—	—	(TI05)/ (TO05)	—	—	—	—	(SCK10)/ (SCL10)	—	(TxDA3)
11	P67	—	—	—	—	—	—	—	(INTP2)	—	—	(TI01)/ (TO01)	—	—	—	—	—	—	—
12	P40	—	—	TOOL0	—	—	—	—	—	—	—	(TI00)/ (TO00)	—	—	—	—	(SCL00)/ (SCK00)	—	—
13	—	—	—	$\overline{\text{RESET}}$	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
14	P124	—	—	XT2/ EXCLKS	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
15	P123	—	—	XT1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
16	P137	—	EI137	—	—	—	—	—	INTP0	—	—	—	—	—	—	—	—	—	—
17	P122	—	EI122	X2/EXCLK	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
18	P121	—	EI121	X1/VBAT0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
19	—	—	—	REGC	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
20	—	—	—	V_{SS}	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
21	—	—	—	V_{DD}	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

Table 1 - 7 Multiplexed Pin Functions of the 100-pin Products (2/5)

Pin Number	I/O			Power supply, system clock, and debugging	Analog Circuits				HMIs			Timers					Communications Interfaces		
100LFQFP	Digital port	Controlled current drive port	ELCL input/output port		A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	LCD controller/driver (LCD)	Interrupt	Key interrupt	Capacitive sensing unit (CTSU2La)	Timer array unit (TAU)	Timer RJ (TRJ)	16-bit timers KB40, KB41, and KB42	External signal sampler	Realtime clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
22	P60	CCD04	EO60	—	—	—	—	—	(INTP3)	—	—	(TI01)/ (TO01)	—	—	—	—	—	SCLA0	—
23	P61	CCD05	EO61	—	—	—	—	—	(INTP4)	—	—	(TI02)/ (TO02)	—	—	—	—	—	SDAA0	—
24	P64	—	—	—	—	—	—	—	(INTP5)	—	—	(TI03)/ (TO03)/ (REMOOUT)	—	—	—	—	—	(SDAA1)	—
25	P65	—	—	—	—	—	—	—	(INTP0)	—	—	(TI05)/ (TO05)	—	—	—	—	—	(SCLA1)	—
26	P62	CCD06	—	—	—	—	—	—	(INTP5)	—	—	(TI03)/ (TO03)/ (REMOOUT)	—	—	—	—	—	SCLA1	—
27	P63	CCD07	—	—	—	—	—	—	(INTP6)	—	—	(TI04)/ (TO04)	—	—	—	—	—	SDAA1	—
28	P127	—	—	—	—	—	—	CAPH	—	—	TS00	(TI03)/ (TO03)/ (REMOOUT)	—	—	—	—	—	—	—
29	P126	—	—	—	—	—	—	CAPL	(INTP4)	—	TS01	(TI04)/ (TO04)	—	—	—	—	—	—	—
30	P87	—	—	—	—	—	—	V_{L1}	—	—	—	—	—	—	—	—	(TxD1)/ (SO10)	—	—
31	P86	—	—	(PCLBUZ1)	—	—	—	V_{L2}	(INTP3)	—	—	(TI06)/ (TO06)	—	—	—	—	(RxD1)/ (SI10)/ (SDA10)	—	—
32	P85	—	—	—	—	—	(VCOUT0)	V_{L4}	(INTP4)	—	—	—	—	—	—	—	(SCK10)/ (SCL10)/ (SCK30)/ (SCL30)	—	—
33	P125	—	—	(PCLBUZ1)	—	—	(VCOUT1)	V_{L3}	(INTP7)	—	TS02	(TI06)/ (TO06)	—	—	—	—	(SI30)/ (RxD3)/ (SDA30)	—	—
34	P35	—	—	—	—	—	(VCOUT0)	SEG25	(INTP4)	—	TS03	—	—	—	—	—	(SO30)/ (TxD3)	—	—
35	P34	—	—	—	—	—	—	SEG24	(INTP0)	—	TS04	(TI01)/ (TO01)	—	—	—	—	(SI30)/ (RxD3)/ (SDA30)	—	—
36	P33	—	—	—	—	—	—	SEG23	INTP4	—	TS05	(TI01)/ (TO01)	—	—	—	(RTC1HZ)	(SCK30)/ (SCL30)	—	—
37	P32	—	—	—	—	—	—	SEG22	(INTP3)	—	TS06	TI01/ TO01/ (TI03)/ (TO03)/ (REMOOUT)	—	—	—	(RTC1HZ)	—	—	—

Table 1 - 7 Multiplexed Pin Functions of the 100-pin Products (3/5)

Pin Number	I/O			Power supply, system clock, and debugging	Analog Circuits				HMIs			Timers					Communications Interfaces		
100LFQFP	Digital port	Controlled current drive port	ELCL input/output port		A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	LCD controller/driver (LCD)	Interrupt	Key interrupt	Capacitive sensing unit (CTSU2La)	Timer array unit (TAU)	Timer RJ (TRJ)	16-bit timers KB40, KB41, and KB42	External signal sampler	Realtime clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
38	—	—	—	EVSS	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
39	P31	—	—	—	—	—	—	SEG21	INTP3	—	TS07	(TI01)/ (TO01)	—	—	—	RTC1HZ	—	—	—
40	P30	—	—	—	—	—	—	SEG20	(INTP3)	—	TS08	TI03/ TO03/ REMOOUT	—	—	—	(RTC1HZ)	—	—	—
41	P77	CCD00	EI77/ EO77	—	—	—	—	SEG19	(INTP1)	KR7	TS09	(TI07)/ (TO07)	—	TKBO01/ (TKBO21)	(EXSDO0)	—	SO20/ TxD2	—	—
42	P76	CCD01	EI76/ EO76	—	—	—	—	SEG18	(INTP2)	KR6	TS10	—	—	TKBO00	(EXSDO1)	(RTC1HZ)	SI20/ SDA20/ RxD2	—	—
43	P75	CCD02	—	—	—	—	—	SEG17	(INTP0)	KR5	TS11	(TI03)/ (TO03)/ (REMOOUT)	—	(TKBO11)/ (TKBO01)	—	—	SCK20/ SCL20	—	—
44	P74	CCD03	—	—	—	—	—	SEG16	—	KR4	TS12	—	—	TKBO11/ (TKBO01)	—	—	—	—	—
45	P73	—	—	—	—	—	—	SEG15	—	KR3	TS13	—	—	TKBO10	—	—	—	—	—
46	P72	—	—	—	—	—	—	SEG14	—	KR2	TS14	—	—	TKBO21	—	—	—	—	—
47	P71	—	—	—	—	—	—	SEG13	—	KR1	TS15	—	—		—	—	—	—	—
48	P70	—	—	—	—	—	—	SEG12	—	KR0	TS16	—	—	TKBO20	—	—	—	—	—
49	P84	—	—	—	—	—	—	—	(INTP0)	—	—	—	—	—	—	—	—	(SCLA1)	(TxDA0)
50	P83	—	—	—	—	—	—	—	(INTP1)	—	—	—	—	—	—	—	—	(SDAA1)	(RxDA0)
51	P57	—	—	—	—	—	—	SEG11	INTP6	—	TSCAP	(TI03)/ (TO03)/ (REMOOUT)	—	—	—	—	—	—	—
52	P56	—	—	—	—	—	—	SEG10	—	—	TS17	TI06/ TO06	—	—	—	—	—	—	—
53	P55	—	—	—	—	—	—	SEG9	INTP5	—	TS18	(TI02)/ (TO02)	—	—	—	—	—	—	—
54	P54	—	—	(PCLBUZ0)	—	—	—	SEG8	(INTP0)	—	TS19	TI02/ TO02	—	—	—	—	SCL01/ SCK01	—	—
55	P53	—	—	(PCLBUZ0)	—	—	—	SEG7	INTP2	—	TS20	(TI07)/ (TO07)	—	—	—	—	SI01/ SDA01	—	—
56	P52	—	—	(PCLBUZ1)	—	—	—	SEG6	INTP1	—	TS21	TI00/ TO00	—	—	—	—	SO01	—	—
57	P51	—	—	—	—	—	—	SEG5	(INTP6)	—	TS22	—	—	—	—	—	—	—	RxDA3
58	P50	—	—	—	—	—	—	SEG4	—	—	TS23	—	—	—	—	—	—	—	TxDA3
59	P97	—	—	—	—	—	—	SEG3/ COM7	—	—	TS24	(TI05)/ (TO05)	—	—	—	—	(SCK01)/ (SCL01)	(SCLA1)	—
60	P96	—	—	(PCLBUZ0)	—	—	—	SEG2/ COM6	(INTP5)	—	TS25	—	—	—	—	—	(SI01)/ (SDA01)	(SDAA1)	—

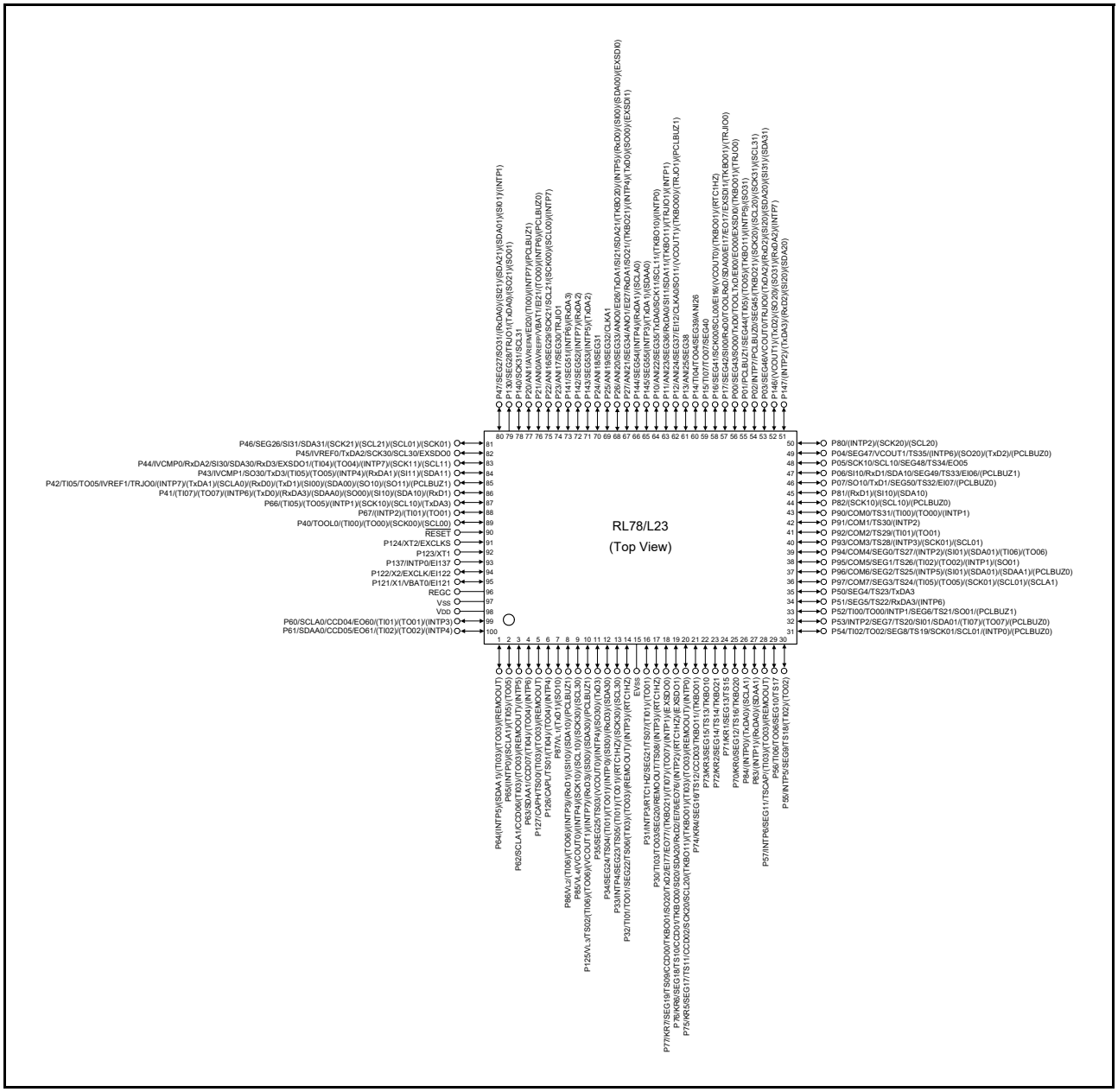
Table 1 - 7 Multiplexed Pin Functions of the 100-pin Products (4/5)

Pin Number	I/O			Power supply, system clock, and debugging	Analog Circuits				HMIs			Timers					Communications Interfaces		
100LFQFP	Digital port	Controlled current drive port	ELCL input/output port		A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	LCD controller/driver (LCD)	Interrupt	Key interrupt	Capacitive sensing unit (CTSU2La)	Timer array unit (TAU)	Timer RJ (TRJ)	16-bit timers KB40, KB41, and KB42	External signal sampler	Realtime clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
61	P95	—	—	—	—	—	—	SEG1/ COM5	(INTP1)	—	TS26	(TI02)/ (TO02)	—	—	—	—	(SO01)	—	—
62	P94	—	—	—	—	—	—	SEG0/ COM4	(INTP2)	—	TS27	(TI06)/ (TO06)	—	—	—	—	(SI01)/ (SDA01)	—	—
63	P93	—	—	—	—	—	—	COM3	(INTP3)	—	TS28	—	—	—	—	—	(SCK01)/ (SCL01)	—	—
64	P92	—	—	—	—	—	—	COM2	—	—	TS29	(TI01)/ (TO01)	—	—	—	—	—	—	—
65	P91	—	—	—	—	—	—	COM1	(INTP2)	—	TS30	—	—	—	—	—	—	—	—
66	P90	—	—	—	—	—	—	COM0	(INTP1)	—	TS31	(TI00)/ (TO00)	—	—	—	—	—	—	—
67	P82	—	—	(PCLBUZ0)	—	—	—	—	—	—	—	—	—	—	—	—	(SCK10)/ (SCL10)	—	—
68	P81	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(RxD1)/ (SI10)/ (SDA10)	—	—
69	P07	—	EI07	(PCLBUZ0)	—	—	—	SEG50	—	—	TS32	—	—	—	—	—	SO10/ TxD1	—	—
70	P06	—	EI06	(PCLBUZ1)	—	—	—	SEG49	—	—	TS33	—	—	—	—	—	SI10/ RxD1/ SDA10	—	—
71	P05	—	EO05	—	—	—	—	SEG48	—	—	TS34	—	—	—	—	—	SCK10/ SCL10	—	—
72	P04	—	—	(PCLBUZ0)	—	—	VCOUT1	SEG47	(INTP6)	—	TS35	—	—	—	—	—	(TxD2)/ (SO20)	—	—
73	P80	—	—	—	—	—	—	—	(INTP2)	—	—	—	—	—	—	—	(SCK20)/ (SCL20)	—	—
74	P147	—	—	—	—	—	—	—	(INTP2)	—	—	—	—	—	—	—	(RxD2)/ (SI20)/ (SDA20)	—	(TxDA3)
75	P146	—	—	—	—	—	(VCOUT1)	—	(INTP7)	—	—	—	—	—	—	—	(TxD2)/ (SO31)/ (SO20)	—	(RxDA2)
76	P03	—	—	—	—	—	VCOUT0	SEG46	—	—	—	—	TRJIO0	—	—	—	(SI31)/ (SDA31)/ (RxD2)/ (SI20)/ (SDA20)	—	(TxDA2)
77	P02	—	—	PCLBUZ0	—	—	—	SEG45	INTP7	—	—	—	—	(TKBO21)	—	—	(SCK31)/ (SCL31)/ (SCK20)/ (SCL20)	—	—
78	P01	—	—	PCLBUZ1	—	—	—	SEG44	(INTP5)	—	—	(TI05)/ (TO05)		(TKBO11)	—	—	(SO31)	—	—
79	P00	—	EI00/ EO00	TOOLTxD	—	—	—	SEG43	—	—	—	—	(TRJO0)	(TKBO01)	EXSDI0	—	SO00/ TxD0	—	—
80	P17	—	EI17/ EO17	TOOLRxD	—	—	—	SEG42	—	—	—	—	(TRJIO0)	(TKBO01)	EXSDI1	—	SI00/ RxD0/ SDA00	—	—

Table 1 - 7 Multiplexed Pin Functions of the 100-pin Products (5/5)

Pin Number	I/O			Power supply, system clock, and debugging	Analog Circuits				HMIs			Timers					Communications Interfaces		
100LFQFP	Digital port	Controlled current drive port	ELCL input/output port		A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	LCD controller/driver (LCD)	Interrupt	Key interrupt	Capacitive sensing unit (CTSU2La)	Timer array unit (TAU)	Timer RJ (TRJ)	16-bit timers KB40, KB41, and KB42	External signal sampler	Realtime clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
81	P16	—	EI16	—	—	—	(VCOUT0)	SEG41	—	—	—	—	—	(TKBO01)	—	(RTC1HZ)	SCK00/ SCL00	—	—
82	P15	—	—	—	—	—	—	SEG40	—	—	—	TI07/ TO07	—	—	—	—	—	—	—
83	P14	—	—	—	ANI26	—	—	SEG39	—	—	—	TI04/ TO04	—	—	—	—	—	—	—
84	P13	—	—	—	ANI25	—	—	SEG38	—	—	—	—	—	—	—	—	—	—	—
85	P12	—	EI12	(PCLBUZ1)	ANI24	—	(VCOUT1)	SEG37	—	—	—	—	(TRJO1)	(TKBO00)	—	—	SO11	—	CLKA0
86	P11	—	—	—	ANI23	—	—	SEG36	(INTP1)	—	—	—	(TRJIO1)	(TKBO11)	—	—	SI11/ SDA11	—	RxDA0
87	P10	—	—	—	ANI22	—	—	SEG35	(INTP0)	—	—	—	—	(TKBO10)	—	—	SCK11/ SCL11	—	TxDA0
88	P145	—	—	—	—	—	—	SEG55	(INTP3)	—	—	—	—	—	—	—	—	(SDAA0)	(TxDA1)
89	P144	—	—	—	—	—	—	SEG54	(INTP4)	—	—	—	—	—	—	—	—	(SCLA0)	(RxDA1)
90	P27	—	EI27	—	ANI21	ANO1	—	SEG34	(INTP4)	—	—	—	—	(TKBO21)	(EXSDI1)	—	(TxD0)/ (SO00)/ SO21	—	RxDA1
91	P26	—	EI26	—	ANI20	ANO0	—	SEG33	(INTP5)	—	—	—	—	(TKBO20)	(EXSDI0)	—	SI21/ SDA21/ (RxD0)/ (SI00)/ (SDA00)	—	TxDA1
92	P25	—	—	—	ANI19	—	—	SEG32	—	—	—	—	—	—	—	—	—	—	CLKA1
93	P24	—	—	—	ANI18	—	—	SEG31	—	—	—	—	—	—	—	—	—	—	—
94	P143	—	—	—	—	—	—	SEG53	(INTP5)	—	—	—	—	—	—	—	—	—	(TxDA2)
95	P142	—	—	—	—	—	—	SEG52	(INTP7)	—	—	—	—	—	—	—	—	—	(RxDA2)
96	P141	—	—	—	—	—	—	SEG51	(INTP6)	—	—	—	—	—	—	—	—	—	(RxDA3)
97	P23	—	—	—	ANI17	—	—	SEG30	—	—	—	—	TRJIO1	—	—	—	—	—	—
98	P22	—	—	—	ANI16	—	—	SEG29	(INTP7)	—	—	—	—	—	—	—	(SCK00)/ (SCL00)/ SCK21/ SCL21	—	—
99	P21	—	EI21	VBAT1/ (PCLBUZ0)	ANI0/ AVREFP	—	—	—	(INTP6)	—	—	(TO00)	—	—	—	—	—	—	—
100	P20	—	EI20	(PCLBUZ1)	ANI1/ AVREFM	—	—	—	(INTP7)	—	—	(TI00)	—	—	—	—	—	—	—

- 100-pin plastic LQFP (14 × 20 mm, 0.65-mm pitch)



Caution 1. Connect the EVss pin to the same ground as the Vss pin.

Caution 2. Connect the REGC pin to Vss via a capacitor (0.47 to 1 µF).

Remark 1. For pin identification, see **1.4 Pin Identification**.

Remark 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to connect the Vss and EVss pins to separate ground lines.

Remark 3. Pin functions in parentheses can be assigned via settings in the peripheral I/O redirection registers (PIORx). For details, see **4.3.10 Peripheral I/O redirection registers (PIORx)** in the RL78/L23 User's Manual.

Table 1 - 8 Multiplexed Pin Functions of the 100-pin Products (1/5)

Pin Number	I/O			Power supply, system clock, and debugging	Analog Circuits				HMIs			Timers					Communications Interfaces		
100LQFP	Digital port	Controlled current drive port	ELCL input/output port		A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	LCD controller/driver (LCD)	Interrupt	Key interrupt	Capacitive sensing unit (CTSU2La)	Timer array unit (TAU)	Timer RJ (TRJ)	16-bit timers KB40, KB41, and KB42	External signal sampler	Realtime clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
1	P64	—	—	—	—	—	—	—	(INTP5)	—	—	(TI03)/ (TO03)/ (REMOOUT)	—	—	—	—	—	(SDAA1)	—
2	P65	—	—	—	—	—	—	—	(INTP0)	—	—	(TI05)/ (TO05)	—	—	—	—	—	(SCLA1)	—
3	P62	CCD06	—	—	—	—	—	—	(INTP5)	—	—	(TI03)/ (TO03)/ (REMOOUT)	—	—	—	—	—	SCLA1	—
4	P63	CCD07	—	—	—	—	—	—	(INTP6)	—	—	(TI04)/ (TO04)	—	—	—	—	—	SDAA1	—
5	P127	—	—	—	—	—	—	CAPH	—	—	TS00	(TI03)/ (TO03)/ (REMOOUT)	—	—	—	—	—	—	—
6	P126	—	—	—	—	—	—	CAPL	(INTP4)	—	TS01	(TI04)/ (TO04)	—	—	—	—	—	—	—
7	P87	—	—	—	—	—	—	V_{L1}	—	—	—	—	—	—	—	—	(TxD1)/ (SO10)	—	—
8	P86	—	—	(PCLBUZ1)	—	—	—	V_{L2}	(INTP3)	—	—	(TI06)/ (TO06)	—	—	—	—	(RxD1)/ (SI10)/ (SDA10)	—	—
9	P85	—	—	—	—	—	(VCOUT0)	V_{L4}	(INTP4)	—	—	—	—	—	—	—	(SCK10)/ (SCL10)/ (SCK30)/ (SCL30)	—	—
10	P125	—	—	(PCLBUZ1)	—	—	(VCOUT1)	V_{L3}	(INTP7)	—	TS02	(TI06)/ (TO06)	—	—	—	—	(SI30)/ (RxD3)/ (SDA30)	—	—
11	P35	—	—	—	—	—	(VCOUT0)	SEG25	(INTP4)	—	TS03	—	—	—	—	—	(SO30)/ (TxD3)	—	—
12	P34	—	—	—	—	—	—	SEG24	(INTP0)	—	TS04	(TI01)/ (TO01)	—	—	—	—	(SI30)/ (RxD3)/ (SDA30)	—	—
13	P33	—	—	—	—	—	—	SEG23	INTP4	—	TS05	(TI01)/ (TO01)	—	—	—	(RTC1HZ)	(SCK30)/ (SCL30)	—	—
14	P32	—	—	—	—	—	—	SEG22	(INTP3)	—	TS06	TI01/ TO01/ (TI03)/ (TO03)/ (REMOOUT)	—	—	—	(RTC1HZ)	—	—	—
15	—	—	—	EVSS	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
16	P31	—	—	—	—	—	—	SEG21	INTP3	—	TS07	(TI01)/ (TO01)	—	—	—	RTC1HZ	—	—	—

Table 1 - 8 Multiplexed Pin Functions of the 100-pin Products (2/5)

Pin Number	I/O			Power supply, system clock, and debugging	Analog Circuits				HMIs			Timers					Communications Interfaces		
100LQFP	Digital port	Controlled current drive port	ELCL input/output port		A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	LCD controller/driver (LCD)	Interrupt	Key interrupt	Capacitive sensing unit (CTSU2La)	Timer array unit (TAU)	Timer RJ (TRJ)	16-bit timers KB40, KB41, and KB42	External signal sampler	Realtime clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
17	P30	—	—	—	—	—	—	SEG20	(INTP3)	—	TS08	TI03/ TO03/ REMOOUT	—	—	—	(RTC1HZ)	—	—	—
18	P77	CCD00	EI77/ EO77	—	—	—	—	SEG19	(INTP1)	KR7	TS09	(TI07)/ (TO07)	—	TKBO01/ (TKBO21)	(EXSDO0)	—	SO20/ TxD2	—	—
19	P76	CCD01	EI76/ EO76	—	—	—	—	SEG18	(INTP2)	KR6	TS10	—	—	TKBO00	(EXSDO1)	(RTC1HZ)	SI20/ SDA20/ RxD2	—	—
20	P75	CCD02	—	—	—	—	—	SEG17	(INTP0)	KR5	TS11	(TI03)/ (TO03)/ (REMOOUT)	—	(TKBO11)/ (TKBO01)	—	—	SCK20/ SCL20	—	—
21	P74	CCD03	—	—	—	—	—	SEG16	—	KR4	TS12	—	—	TKBO11/ (TKBO01)	—	—	—	—	—
22	P73	—	—	—	—	—	—	SEG15	—	KR3	TS13	—	—	TKBO10	—	—	—	—	—
23	P72	—	—	—	—	—	—	SEG14	—	KR2	TS14	—	—	TKBO21	—	—	—	—	—
24	P71	—	—	—	—	—	—	SEG13	—	KR1	TS15	—	—		—	—	—	—	—
25	P70	—	—	—	—	—	—	SEG12	—	KR0	TS16	—	—	TKBO20	—	—	—	—	—
26	P84	—	—	—	—	—	—	—	(INTP0)	—	—	—	—	—	—	—	—	(SCLA1)	(TxDA0)
27	P83	—	—	—	—	—	—	—	(INTP1)	—	—	—	—	—	—	—	—	(SDAA1)	(RxDA0)
28	P57	—	—	—	—	—	—	SEG11	INTP6	—	TSCAP	(TI03)/ (TO03)/ (REMOOUT)	—	—	—	—	—	—	—
29	P56	—	—	—	—	—	—	SEG10	—	—	TS17	TI06/ TO06	—	—	—	—	—	—	—
30	P55	—	—	—	—	—	—	SEG9	INTP5	—	TS18	(TI02)/ (TO02)	—	—	—	—	—	—	—
31	P54	—	—	(PCLBUZ0)	—	—	—	SEG8	(INTP0)	—	TS19	TI02/ TO02	—	—	—	—	SCL01/ SCK01	—	—
32	P53	—	—	(PCLBUZ0)	—	—	—	SEG7	INTP2	—	TS20	(TI07)/ (TO07)	—	—	—	—	SI01/ SDA01	—	—
33	P52	—	—	(PCLBUZ1)	—	—	—	SEG6	INTP1	—	TS21	TI00/ TO00	—	—	—	—	SO01	—	—
34	P51	—	—	—	—	—	—	SEG5	(INTP6)	—	TS22	—	—	—	—	—	—	—	RxDA3
35	P50	—	—	—	—	—	—	SEG4	—	—	TS23	—	—	—	—	—	—	—	TxDA3
36	P97	—	—	—	—	—	—	SEG3/ COM7	—	—	TS24	(TI05)/ (TO05)	—	—	—	—	(SCK01)/ (SCL01)	(SCLA1)	—
37	P96	—	—	(PCLBUZ0)	—	—	—	SEG2/ COM6	(INTP5)	—	TS25	—	—	—	—	—	(SI01)/ (SDA01)	(SDAA1)	—
38	P95	—	—	—	—	—	—	SEG1/ COM5	(INTP1)	—	TS26	(TI02)/ (TO02)	—	—	—	—	(SO01)	—	—

Table 1 - 8 Multiplexed Pin Functions of the 100-pin Products (3/5)

Pin Number	I/O			Power supply, system clock, and debugging	Analog Circuits				HMIs			Timers					Communications Interfaces		
100LQFP	Digital port	Controlled current drive port	ELCL input/output port		A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	LCD controller/driver (LCD)	Interrupt	Key interrupt	Capacitive sensing unit (CTSU2La)	Timer array unit (TAU)	Timer RJ (TRJ)	16-bit timers KB40, KB41, and KB42	External signal sampler	Realtime clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
39	P94	—	—	—	—	—	—	SEG0/ COM4	(INTP2)	—	TS27	(TI06)/ (TO06)	—	—	—	—	(SI01)/ (SDA01)	—	—
40	P93	—	—	—	—	—	—	COM3	(INTP3)	—	TS28	—	—	—	—	—	(SCK01)/ (SCL01)	—	—
41	P92	—	—	—	—	—	—	COM2	—	—	TS29	(TI01)/ (TO01)	—	—	—	—	—	—	—
42	P91	—	—	—	—	—	—	COM1	(INTP2)	—	TS30	—	—	—	—	—	—	—	—
43	P90	—	—	—	—	—	—	COM0	(INTP1)	—	TS31	(TI00)/ (TO00)	—	—	—	—	—	—	—
44	P82	—	—	(PCLBUZ0)	—	—	—	—	—	—	—	—	—	—	—	—	(SCK10)/ (SCL10)	—	—
45	P81	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(RxD1)/ (SI10)/ (SDA10)	—	—
46	P07	—	EI07	(PCLBUZ0)	—	—	—	SEG50	—	—	TS32	—	—	—	—	—	SO10/ TxD1	—	—
47	P06	—	EI06	(PCLBUZ1)	—	—	—	SEG49	—	—	TS33	—	—	—	—	—	SI10/ RxD1/ SDA10	—	—
48	P05	—	EO05	—	—	—	—	SEG48	—	—	TS34	—	—	—	—	—	SCK10/ SCL10	—	—
49	P04	—	—	(PCLBUZ0)	—	—	VCOUT1	SEG47	(INTP6)	—	TS35	—	—	—	—	—	(TxD2)/ (SO20)	—	—
50	P80	—	—	—	—	—	—	—	(INTP2)	—	—	—	—	—	—	—	(SCK20)/ (SCL20)	—	—
51	P147	—	—	—	—	—	—	—	(INTP2)	—	—	—	—	—	—	—	(RxD2)/ (SI20)/ (SDA20)	—	(TxDA3)
52	P146	—	—	—	—	—	(VCOUT1)	—	(INTP7)	—	—	—	—	—	—	—	(TxD2)/ (SO31)/ (SO20)	—	(RxDA2)
53	P03	—	—	—	—	—	VCOUT0	SEG46	—	—	—	—	TRJIO0	—	—	—	(SI31)/ (SDA31)/ (RxD2)/ (SI20)/ (SDA20)	—	(TxDA2)
54	P02	—	—	PCLBUZ0	—	—	—	SEG45	INTP7	—	—	—	—	(TKBO21)	—	—	(SCK31)/ (SCL31)/ (SCK20)/ (SCL20)	—	—
55	P01	—	—	PCLBUZ1	—	—	—	SEG44	(INTP5)	—	—	(TI05)/ (TO05)		(TKBO11)	—	—	(SO31)	—	—
56	P00	—	EI00/ EO00	TOOLTxD	—	—	—	SEG43	—	—	—	—	(TRJO0)	(TKBO01)	EXSDI0	—	SO00/ TxD0	—	—
57	P17	—	EI17/ EO17	TOOLRxD	—	—	—	SEG42	—	—	—	—	(TRJIO0)	(TKBO01)	EXSDI1	—	SI00/ RxD0/ SDA00	—	—
58	P16	—	EI16	—	—	—	(VCOUT0)	SEG41	—	—	—	—	—	(TKBO01)	—	(RTC1HZ)	SCK00/ SCL00	—	—

Table 1 - 8 Multiplexed Pin Functions of the 100-pin Products (4/5)

Pin Number	I/O			Power supply, system clock, and debugging	Analog Circuits				HMIs			Timers					Communications Interfaces		
100LQFP	Digital port	Controlled current drive port	ELCL input/output port		A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	LCD controller/driver (LCD)	Interrupt	Key interrupt	Capacitive sensing unit (CTSU2La)	Timer array unit (TAU)	Timer RJ (TRJ)	16-bit timers KB40, KB41, and KB42	External signal sampler	Realtime clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
59	P15	—	—	—	—	—	—	SEG40	—	—	—	TI07/ TO07	—	—	—	—	—	—	—
60	P14	—	—	—	ANI26	—	—	SEG39	—	—	—	TI04/ TO04	—	—	—	—	—	—	—
61	P13	—	—	—	ANI25	—	—	SEG38	—	—	—	—	—	—	—	—	—	—	—
62	P12	—	EI12	(PCLBUZ1)	ANI24	—	(VCOUT1)	SEG37	—	—	—	—	(TRJO1)	(TKBO00)	—	—	SO11	—	CLKA0
63	P11	—	—	—	ANI23	—	—	SEG36	(INTP1)	—	—	—	(TRJIO1)	(TKBO11)	—	—	SI11/ SDA11	—	RxDA0
64	P10	—	—	—	ANI22	—	—	SEG35	(INTP0)	—	—	—	—	(TKBO10)	—	—	SCK11/ SCL11	—	TxDA0
65	P145	—	—	—	—	—	—	SEG55	(INTP3)	—	—	—	—	—	—	—	—	(SDAA0)	(TxDA1)
66	P144	—	—	—	—	—	—	SEG54	(INTP4)	—	—	—	—	—	—	—	—	(SCLA0)	(RxDA1)
67	P27	—	EI27	—	ANI21	ANO1	—	SEG34	(INTP4)	—	—	—	—	(TKBO21)	(EXSDI1)	—	(TxD0)/ (SO00)/ SO21	—	RxDA1
68	P26	—	EI26	—	ANI20	ANO0	—	SEG33	(INTP5)	—	—	—	—	(TKBO20)	(EXSDI0)	—	SI21/ SDA21/ (RxD0)/ (SI00)/ (SDA00)	—	TxDA1
69	P25	—	—	—	ANI19	—	—	SEG32	—	—	—	—	—	—	—	—	—	—	CLKA1
70	P24	—	—	—	ANI18	—	—	SEG31	—	—	—	—	—	—	—	—	—	—	—
71	P143	—	—	—	—	—	—	SEG53	(INTP5)	—	—	—	—	—	—	—	—	—	(TxDA2)
72	P142	—	—	—	—	—	—	SEG52	(INTP7)	—	—	—	—	—	—	—	—	—	(RxDA2)
73	P141	—	—	—	—	—	—	SEG51	(INTP6)	—	—	—	—	—	—	—	—	—	(RxDA3)
74	P23	—	—	—	ANI17	—	—	SEG30	—	—	—	—	TRJIO1	—	—	—	—	—	—
75	P22	—	—	—	ANI16	—	—	SEG29	(INTP7)	—	—	—	—	—	—	—	(SCK00)/ (SCL00)/ SCK21/ SCL21	—	—
76	P21	—	EI21	VBAT1/ (PCLBUZ0)	ANI0/ AVREFP	—	—	—	(INTP6)	—	—	(TO00)	—	—	—	—	—	—	—
77	P20	—	EI20	(PCLBUZ1)	ANI1/ AVREFM	—	—	—	(INTP7)	—	—	(TI00)	—	—	—	—	—	—	—
78	P140	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SCK31/ SCL31	—	—
79	P130	—	—	—	—	—	—	SEG28	—	—	—	—	TRJO1	—	—	—	(SO21)/ (SO01)	—	(TxDA0)
80	P47	—	—	—	—	—	—	SEG27	(INTP1)	—	—	—	—	—	—	—	SO31/ (SI01)/ (SI21)/ (SDA01)/ (SDA21)	—	(RxDA0)

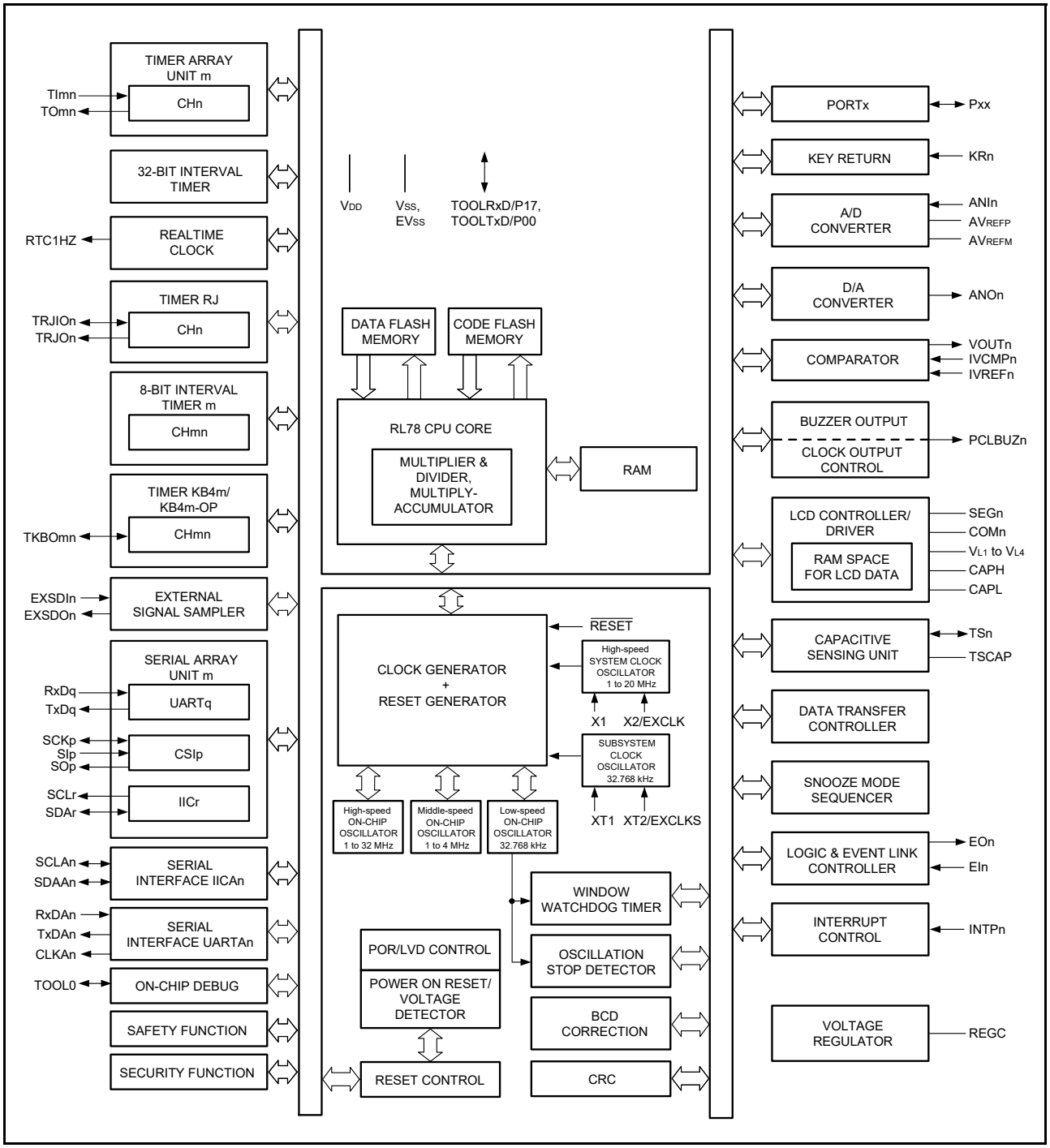
Table 1 - 8 Multiplexed Pin Functions of the 100-pin Products (5/5)

Pin Number	I/O			Power supply, system clock, and debugging	Analog Circuits				HMIs			Timers					Communications Interfaces		
100LQFP	Digital port	Controlled current drive port	ELCL input/output port		A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	LCD controller/driver (LCD)	Interrupt	Key interrupt	Capacitive sensing unit (CTSU2La)	Timer array unit (TAU)	Timer RJ (TRJ)	16-bit timers KB40, KB41, and KB42	External signal sampler	Realtime clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
81	P46	—	—	—	—	—	—	SEG26	—	—	—	—	—	—	—	—	SI31/ SDA31/ (SCL01)/ (SCK01)/ (SCK21)/ (SCL21)	—	—
82	P45	—	—	—	—	—	IVREF0	—	—	—	—	—	—	—	EXSDO0	—	SCK30/ SCL30	—	TxDA2
83	P44	—	—	—	—	—	IVCMP0	—	(INTP7)	—	—	(TI04)/ (TO04)	—	—	EXSDO1	—	SI30/ SDA30/ (SCL11)/ (SCK11)/ RxD3	—	RxDA2
84	P43	—	—	—	—	—	IVCMP1	—	(INTP4)	—	—	(TI05)/ (TO05)	—	—	—	—	SO30/ (SI11)/ (SDA11)/ TxD3	—	(RxDA1)
85	P42	—	—	(PCLBUZ1)	—	—	IVREF1	—	(INTP7)	—	—	TI05/ TO05	TRJO0	—	—	—	(SI00)/ (RxD0)/ (SDA00)/ (SO11)/ (TxD1)/ (SO10)	(SCLA0)	(TxDA1)
86	P41	—	—	—	—	—	—	—	(INTP6)	—	—	(TI07)/ (TO07)	—	—	—	—	(SI10)/ (SO00)/ (TxD0)/ (SDA10)/ (RxD1)	(SDAA0)	(RxDA3)
87	P66	—	—	—	—	—	—	—	(INTP1)	—	—	(TI05)/ (TO05)	—	—	—	—	(SCK10)/ (SCL10)	—	(TxDA3)
88	P67	—	—	—	—	—	—	—	(INTP2)	—	—	(TI01)/ (TO01)	—	—	—	—	—	—	—
89	P40	—	—	TOOL0	—	—	—	—	—	—	—	(TI00)/ (TO00)	—	—	—	—	(SCL00)/ (SCK00)	—	—
90	—	—	—	$\overline{\text{RESET}}$	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
91	P124	—	—	XT2/ EXCLKS	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
92	P123	—	—	XT1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
93	P137	—	EI137	—	—	—	—	—	INTP0	—	—	—	—	—	—	—	—	—	—
94	P122	—	EI122	X2/EXCLK	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
95	P121	—	EI121	X1/VBAT0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
96	—	—	—	REGC	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
97	—	—	—	V_{SS}	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
98	—	—	—	V_{DD}	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
99	P60	CCD04	EO60	—	—	—	—	—	(INTP3)	—	—	(TI01)/ (TO01)	—	—	—	—	—	SCLA0	—
100	P61	CCD05	EO61	—	—	—	—	—	(INTP4)	—	—	(TI02)/ (TO02)	—	—	—	—	—	SDAA0	—

1.4 Pin Identification

ANI0, ANI1, ANI16 to ANI26:	Analog input
ANO0, ANO1:	Analog output
AVREFM:	Analog reference voltage minus
AVREFP:	Analog reference voltage plus
CCD00 to CCD07:	Controlled current drive output
CLKA0, CLKA1:	Asynchronous serial clock output
CAPH, CAPL:	Capacitor for LCD
COM0 to COM7:	LCD common output
EI00, EI06, EI07, EI12, EI16, EI17, EI20, EI21, EI26, EI27, EI76, EI77, EI121, EI122, EI137:	Logic & event link controller input
EO00, EO05, EO17, EO60, EO61, EO76, EO77:	Logic & event link controller output
EVSS:	Ground for port
EXCLK:	External clock input (main system clock)
EXCLKS:	External clock input (subsystem clock)
EXSDI0, EXSDI1:	External signal sampler input
EXSDO0, EXSDO1:	External signal sampler clock output
INTP0 to INTP7:	Interrupt request from peripheral modules
IVCMP0, IVCMP1:	Comparator input
IVREF0, IVREF1:	Comparator reference input
KR0 to KR7:	Key return
P00 to P07:	Port 0
P10 to P17:	Port 1
P20 to P27:	Port 2
P30 to P35:	Port 3
P40 to P47:	Port 4
P50 to P57:	Port 5
P60 to P67:	Port 6
P70 to P77:	Port 7
P80 to P87:	Port 8
P90 to P97:	Port 9
P121 to P127:	Port 12
P130, P137:	Port 13
P140 to P147:	Port 14
PCLBUZ0, PCLBUZ1:	Programmable clock output/buzzer output
REGC:	Regulator capacitance
$\overline{\text{RESET}}$:	Reset
RTC1HZ:	Realtime clock correction clock (1 Hz) output
RxD0 to RxD3, RxDA0, RxDA1, RxDA2, RxDA3:	Receive data
SCLA0, SCLA1, SCK00, SCK01, SCK10, SCK11, SCK20, SCK21, SCK30, SCK31:	Serial clock input/output
SCL00, SCL01, SCL10, SCL11, SCL20, SCL21, SCL30, SCL31:	Serial clock output
SDAA0, SDAA1, SDA00, SDA01, SDA10, SDA11, SDA20, SDA21, SDA30, SDA31:	Serial data input/output
SEG0 to SEG55:	LCD segment output
SI00, SI01, SI10, SI11, SI20, SI21, SI30, SI31:	Serial data input
SO00, SO01, SO10, SO11, SO20, SO21, SO30, SO31:	Serial data output
TSCAP:	Touch sensor capacitance
TI00 to TI07:	Timer input
TO00 to TO07:	Timer output
TKBO00, TKBO01, TKBO10, TKBO11, TKBO20, TKBO21:	Timer KB4 output
TOOL0:	Data input/output for tool
TOOLRxD, TOOLTxD:	Data input/output for external device
TRJIO0, TRJIO1:	Timer input/output
TS00 to TS35:	Capacitive sensor
TxD0 to TxD3, TxDA0, TxDA1, TxDA2, TxDA3:	Transmit data
VBAT0, VBAT1:	Battery backup power supply
VCOUT0, VCOUT1:	Comparator output
VDD:	Power supply
VL1 to VL4:	LCD power supply
VSS:	Ground
X1, X2:	Crystal oscillator (main system clock)
XT1, XT2:	Crystal oscillator (subsystem clock)
REMOOUT:	Remote control output

1.5 Block Diagram



Remark m: Unit number, n: Channel number, p: CSI number, q: UART number, r: Simplified I^2C number, xx: Port number

1.6 Outline of Functions

Caution This outline describes the functions at the time when the peripheral I/O redirection registers (PIORx) are set to 00H.

(1/4)

Item		44-pin	48-pin	52-pin	64-pin	80-pin	100-pin
		R7F100LFx	R7F100LGx	R7F100LJx	R7F100LLx	R7F100LMx	R7F100LPx
Code flash memory		512 KB (256 KB × 2 banks or a single 512-KB bank) 256 KB (128 KB × 2 banks or a single 256-KB bank) 128 KB (single bank) 64 KB (single bank)				512 KB (256 KB × 2 banks or a single 512-KB bank) 256 KB (128 KB × 2 banks or a single 256-KB bank) 128 KB (single bank)	
Data flash memory		8 KB	8 KB	8 KB	8 KB	8 KB	8 KB
RAM		16 to 32 KB	16 to 32 KB	16 to 32 KB	16 to 32 KB	16 to 32 KB	16 to 32 KB
Address space		1 MB					
CPU/peripheral hardware clock frequency (f_{CLK})	Main system clock	HS (high-speed main) mode: 1 to 32 MHz (V_{DD} = 1.8 to 5.5 V) HS (high-speed main) mode: 1 to 4 MHz**Note 1** (V_{DD} = 1.6 to 5.5 V) LS (low-speed main) mode: 1 to 24 MHz (V_{DD} = 1.8 to 5.5 V) LS (low-speed main) mode: 1 to 4 MHz**Note 1** (V_{DD} = 1.6 to 5.5 V) LP (low-power main) mode: 1 to 2 MHz**Note 2** (V_{DD} = 1.6 to 5.5 V)					
	Subsystem clock	SUB mode: 32.768 kHz (V_{DD} = 1.6 to 5.5 V)					
Main system clock	High-speed system clock (f_{MX})	1 to 20 MHz					
	High-speed on-chip oscillator clock (f_{IH})	1 MHz, 2 MHz, 3 MHz, 4 MHz, 6 MHz, 8 MHz, 12 MHz, 16 MHz, 24 MHz, 32 MHz					
	Middle-speed on-chip oscillator clock (f_{IM})	1 MHz, 2 MHz, 4 MHz					
Subsystem clock	Subsystem clock X (f_{SX})	32.768 kHz (V_{DD} = 1.6 to 5.5 V)					
	Low-speed on-chip oscillator clock (f_{IL})	32.768 kHz (typ.)					
General-purpose registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)					
Minimum instruction execution time		0.03125 μs (at the 32-MHz operation with the high-speed on-chip oscillator clock (f_{IH}))					
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits, 16 bits × 16 bits), division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits) • Multiplication and accumulation (16 bits × 16 bits + 32 bits) • Rotate, barrel shift, and bit manipulation (set, reset, test, and Boolean operation), etc.					
I/O port	Total number of pins	40	44	48	60	76	95
	CMOS I/O	35 (N-ch open-drain I/O [V_{DD} withstand voltage]: 24)	39 (N-ch open-drain I/O [V_{DD} withstand voltage]: 27)	43 (N-ch open-drain I/O [V_{DD} withstand voltage]: 29)	53 (N-ch open-drain I/O [V_{DD} withstand voltage]: 35)	68 (N-ch open-drain I/O [V_{DD} withstand voltage]: 42)	87 (N-ch open-drain I/O [V_{DD} withstand voltage]: 57)
	CMOS input	3	3	3	3	3	3
	CMOS output	—	—	—	—	1	1
	N-ch open-drain I/O (withstand voltage: 6 V)	2	2	2	4	4	4
	Controlled current drive port	4	5	6	8	8	8

(2/4)

Item		44-pin	48-pin	52-pin	64-pin	80-pin	100-pin
		R7F100LFx	R7F100LGx	R7F100LJx	R7F100LLx	R7F100LMx	R7F100LPx
Timers	16-bit timer	8 channels					
	Watchdog timer	1 channel					
	Realtime clock (RTC)	1 channel					
	32-bit interval timer (TML32)	1 channel in 32-bit counter mode, 2 channels in 16-bit counter mode, 4 channels in 8-bit counter mode					
	8-bit interval timer	Products with 256 or 512 Kbytes of flash memory: 8 units Products with 64 or 128 Kbytes of flash memory: 4 units				8 units	
	16-bit timer RJ	Products with 256 or 512 Kbytes of flash memory: 2 channels Products with 64 or 128 Kbytes of flash memory: 1 channel				2 channels	
	16-bit timer KB4	Products with 256 or 512 Kbytes of flash memory: 3 channels Products with 64 or 128 Kbytes of flash memory: 1 channel				3 channels	
	External signal sampler	1 channel					
	Oscillation stop detector	1 channel					
	Timer output	6 channels (PWM outputs: 5Note 3), 8 channels (PWM outputs: 7Note 3)Note 4		8 channels (PWM outputs: 7Note 3)			
	RTC output	1 channel					
Clock output/buzzer output		2 channels					
		• 3.91 kHz, 7.81 kHz, 15.63 kHz, 2 MHz, 4 MHz, 8 MHz, 16 MHz (at the 32-MHz operation with the main system clock (f_{MAIN})) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (at the 32.768-kHz operation with the low-speed peripheral clock (f_{SXP}))					
8-/10-/12-bit resolution A/D converter		8 channels	9 channels	10 channels	10 channels	13 channels	13 channels
D/A converter		3 channels (one of the three interfaces is only for the internal reference voltage for the comparator)					
Comparator		1 channel		2 channels			

(3/4)

Item		44-pin	48-pin	52-pin	64-pin	80-pin	100-pin
		R7F100LFx	R7F100LGx	R7F100LJx	R7F100LLx	R7F100LMx	R7F100LPx
Serial interfaces		[44-pin products] • Simplified SPI (CSI): 2 channels[Note 4]/simplified I²C: 2 channels[Note 4]/UART: 1 channel • Simplified SPI (CSI): 2 channels/simplified I²C: 2 channels/UART: 1 channel • Simplified SPI (CSI): 1 channel/simplified I²C: 1 channel/UART (UART supporting LIN-bus): 1 channel • Simplified I²C: 1 channel[Note 4] [48-pin products] • Simplified SPI (CSI): 2 channels[Note 4]/simplified I²C: 2 channels[Note 4]/UART: 1 channel • Simplified SPI (CSI): 2 channels/simplified I²C: 2 channels/UART: 1 channel • Simplified SPI (CSI): 2 channels/simplified I²C: 2 channels/UART (UART supporting LIN-bus): 1 channel • Simplified I²C: 1 channel [52-pin products] • Simplified SPI (CSI): 2 channels[Note 4]/simplified I²C: 2 channels/UART: 1 channel • Simplified SPI (CSI): 2 channels/simplified I²C: 2 channels/UART: 1 channel • Simplified SPI (CSI): 2 channels/simplified I²C: 2 channels/UART (UART supporting LIN-bus): 1 channel • Simplified SPI (CSI): 1 channel/simplified I²C: 1 channel/UART: 1 channel [64- and 80-pin products] • Simplified SPI (CSI): 2 channels/simplified I²C: 2 channels/UART: 1 channel • Simplified SPI (CSI): 2 channels/simplified I²C: 2 channels/UART: 1 channel • Simplified SPI (CSI): 2 channels/simplified I²C: 2 channels/UART (UART supporting LIN-bus): 1 channel • Simplified SPI (CSI): 2 channels[Note 4]/simplified I²C: 2 channels[Note 4]/UART: 1 channel [100-pin products] • Simplified SPI (CSI): 2 channels/simplified I²C: 2 channels/UART: 1 channel • Simplified SPI (CSI): 2 channels/simplified I²C: 2 channels/UART: 1 channel • Simplified SPI (CSI): 2 channels/simplified I²C: 2 channels/UART (UART supporting LIN-bus): 1 channel • Simplified SPI (CSI): 2 channels/simplified I²C: 2 channels/UART: 1 channel				
	UARTA	2 channels	Products with 256 or 512 Kbytes of flash memory: 3 channels Products with 64 or 128 Kbytes of flash memory: 2 channels			4 channels	
	I²C bus	2 channels					
Data transfer controller (DTC)		48 sources (44- and 48-pin products with 64 to 128 Kbytes of flash memory) 49 sources (52- and 64-pin products with 64 to 128 Kbytes of flash memory) 51 sources (44-pin products with 256 to 512 Kbytes of flash memory) 53 sources (48-pin products with 256 to 512 Kbytes of flash memory) 54 sources (52- and 64-pin products with 256 to 512 Kbytes of flash memory) 56 sources (80- and 100-pin products with 128 to 512 Kbytes of flash memory)					
Logic and event link controller (ELCL)		1					
SNOOZE mode sequencer (SMS)		1					
Capacitive sensing unit		16	18	20	25	34	36
LCD controller/driver		Internal boosting, capacitive division, and external resistor division are switchable as methods of generating the driving voltage.					
	Segment signal outputs × common signal outputs	19 seg × 4 com 17 seg × 6 com 15 seg × 8 com	22 seg × 4 com 20 seg × 6 com 18 seg × 8 com	25 seg × 4 com 23 seg × 6 com 21 seg × 8 com	34 seg × 4 com 32 seg × 6 com 30 seg × 8 com	49 seg × 4 com 47 seg × 6 com 45 seg × 8 com	56 seg × 4 com 54 seg × 6 com 52 seg × 8 com
Vectored interrupt sources	Internal	47	49	50	50	52	52
	External	9	9	9	9	9	9
Key interrupt		2	3	4	5	8	8

(4/4)

Item		44-pin	48-pin	52-pin	64-pin	80-pin	100-pin
		R7F100LFx	R7F100LGx	R7F100LJx	R7F100LLx	R7F100LMx	R7F100LPx
Reset		• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detectors (LVD0 and LVD1) • Internal reset by illegal instruction execution**Note 5** • Internal reset by RAM parity error • Internal reset by illegal-memory access					
Power-on-reset circuit		Detection voltage • 1.50 V (typ.)					
Voltage detector	LVD0	Detection voltage • Rising edge: 1.69 V to 3.96 V (6 stages) • Falling edge: 1.65 V to 3.88 V (6 stages)					
	LVD1	Detection voltage • Rising edge: 1.67 V to 4.16 V (18 stages) • Falling edge: 1.63 V to 4.08 V (18 stages)					
On-chip debugging		Available (tracing supported)					
Power supply voltage		V_{DD} = 1.6 to 5.5 V					
Operating ambient temperature		T_A = –40 to +105°C (3C: Industrial applications)					

Note 1. Overwrite the flash memory during operation at 2 MHz or a lower frequency.

Note 2. When the flash memory is to be overwritten, switch to high-speed main (HS) mode or low-speed main (LS) mode.

Note 3. The number of PWM outputs varies depending on the setting of channels in use (the number of masters and slaves). For details, see **7.9.3 Operation for the multiple PWM output function** in the RL78/L23 User's Manual.

Note 4. This applies when the corresponding sets of bits in the peripheral I/O redirection registers (PIORx) have suitable non-0 values.

Note 5. In normal operation, executing the instruction code FFH triggers an internal reset, but this is not the case during emulation by the on-chip debugging emulator.

2. Electrical Characteristics

Caution 1. RL78 microcontrollers have on-chip debugging functionality for use in the development and evaluation of user systems. Do not use on-chip debugging with products designated as part of mass production, because using this function may cause the guaranteed number of times the flash memory is rewritten to be exceeded, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when on-chip debugging is used with products designated as part of mass production.

Caution 2. For products that do not have EV_{SS} pins, read EV_{SS} as V_{SS}.

Caution 3. The present pins differ depending on the products. For details, see section 2.1 Functions of Port Pins through section 2.2.1 Functions for each product in the RL78/L23 User's Manual.

2.1 Absolute Maximum Ratings

(1/2)

Item	Symbols	Conditions	Ratings	Unit
Supply voltage	V_{DD}		-0.5 to +6.5	V
	EV_{SS}		-0.5 to +0.3	V
REGC pin input voltage	V_{IREGC}	REGC	-0.3 to +2.1 and -0.3 to V_{DD} +0.3 **Note 1**	V
Input voltage	V_{I1}	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P125 to P127, P140 to P147	-0.3 to V_{DD} +0.3 **Note 2**	V
	V_{I2}	P60 to P63 (N-ch open-drain)	-0.3 to +6.5	V
	V_{I3}	P20, P21, P121 to P124, P137, EXCLK, EXCLKS, RESET	-0.3 to V_{DD} +0.3 **Note 2**	V
Output voltage	V_{O1}	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P125 to P127, P140 to P147	-0.3 to V_{DD} +0.3 **Note 2**	V
	V_{O2}	P20, P21, P121, P122	-0.3 to V_{DD} +0.3 **Note 2**	V
Analog input voltage	V_{AI1}	ANI16 to ANI26	-0.3 to V_{DD} +0.3 and -0.3 to AV_{REFP} +0.3 **Notes 2, 3**	V
	V_{AI2}	ANI0, ANI1	-0.3 to V_{DD} +0.3 and -0.3 to AV_{REFP} +0.3 **Notes 2, 3**	V

Note 1. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF). The listed value is the absolute maximum rating of the REGC pin. Only use the capacitor connection. Do not apply a specific voltage to this pin.

Note 2. This voltage must be no higher than 6.5 V.

Note 3. The voltage on a pin in use for A/D conversion must not exceed AV_{REFP} +0.3.

Caution **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

Remark 1. The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

Remark 2. AV_{REFP} refers to the positive reference voltage of the A/D converter.

Remark 3. The reference voltage is V_{SS}.

(2/2)

Item	Symbols	Conditions		Ratings	Unit
High-level output current	I_{OH1}	Per pin	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P125 to P127, P130, P140 to P147	-40	mA
		Total of all pins -170 mA	P40 to P47, P66, P67, P130, P140	-70	mA
			P00 to P07, P10 to P17, P22 to P27, P30 to P35, P50 to P57, P64, P65, P70 to P77, P80 to P87, P90 to P97, P125 to P127, P141 to P147	-100	mA
	I_{OH2}	Per pin	P20, P21, P121, P122	-5	mA
		Total of all pins		-20	mA
Low-level output current	I_{OL1}	Per pin	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P125 to P127, P130, P140 to P147	40 Note	mA
		Total of all pins 170 mA	P40 to P47, P66, P67, P130, P140	70	mA
			P00 to P07, P10 to P17, P22 to P27, P30 to P35, P50 to P57, P64, P65, P70 to P77, P80 to P87, P90 to P97, P125 to P127, P141 to P147	100	mA
	I_{OL2}	Per pin	P20, P21, P121, P122	10	mA
		Total of all pins		20	mA
Ambient operating temperature	T_A	In normal operation mode		-40 to +105	°C
		In flash memory programming mode		-40 to +105	
Storage temperature	T_{stg}			-65 to +150	°C

Note The rating for the following port pins is 80 mA when I_{OL1} = 40.0 mA is specified by the 40-mA port output control register (PTDC).
Pins P00, P05, and P16 of 44- to 52-pin products, and of 64-pin products with 64 to 128 Kbytes of flash ROM
Pins P07, P10, and P27 of 64-pin products with 256 to 512 Kbytes of flash ROM, and of 80- and 100-pin products

Caution **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

Remark The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

2.2 Characteristics of the Oscillators

2.2.1 Characteristics of the X1 oscillator

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Item	Resonator	Conditions	Min.	Typ.	Max.	Unit
X1 clock oscillation allowable input cycle time[Note]	Ceramic resonator/ crystal resonator		0.05		1	μs

Note The listed time and frequency indicate permissible ranges of the oscillator. For actual applications, request evaluation by the manufacturer of the oscillator circuit mounted on a board so you can use appropriate values. See AC Characteristics for instruction execution time.

Caution **Since the CPU is started by the high-speed on-chip oscillator clock after release from the reset state, the user should use the oscillation stabilization time counter status register (OSTC) to check the X1 clock oscillation stabilization time. Specify the values for the oscillation stabilization time in the OSTC register and the oscillation stabilization time select register (OSTS) after having sufficiently evaluated the oscillation stabilization time with the resonator to be used.**

2.2.2 Characteristics of the XT1 oscillator

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Item	Resonator	Conditions	Min.	Typ.	Max.	Unit
XT1 clock oscillation frequency (f_{XT})[Note]	Crystal resonator			32.768		kHz

Note The listed time and frequency indicate permissible ranges of the oscillator. For actual applications, request evaluation by the manufacturer of the oscillator circuit mounted on a board so you can use appropriate values. See AC Characteristics for instruction execution time.

2.2.3 Characteristics of the On-chip Oscillators

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Item	Symbols	Conditions		Min.	Typ.	Max.	Unit
High-speed on-chip oscillator clock frequency	f_{IH}			1		32	MHz
High-speed on-chip oscillator clock frequency accuracy		HIPREC = 1	-40 to +105°C	-1.0		+1.0	%
		HIPREC = 0 **Note 1**		-15		0	%
High-speed on-chip oscillator clock correction resolution					0.05		%
Middle-speed on-chip oscillator clock frequency **Note 2**	f_{IM}			1		4	MHz
Middle-speed on-chip oscillator clock frequency accuracy				-12		+12	%
Middle-speed on-chip oscillator clock correction resolution					0.15		%
Middle-speed on-chip oscillator frequency temperature coefficient						±0.17 **Note 3**	%/°C
Low-speed on-chip oscillator clock frequency **Note 2**	f_{IL}				32.768		kHz
Low-speed on-chip oscillator clock frequency accuracy				-15		+15	%
Low-speed on-chip oscillator clock correction resolution					0.3		%
Low-speed on-chip oscillator frequency temperature coefficient						±0.21 **Note 3**	%/°C

Note 1. The listed condition applies when the setting of the FRQSEL3 bit is 1.

Note 2. The listed values only indicate the characteristics of the oscillators. See AC Characteristics for instruction execution time.

Note 3. These values are the results of characteristic evaluation and are not checked for shipment.

2.3 DC Characteristics

2.3.1 Pin characteristics

(TA = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (1/7)

Item	Symbols	Conditions		Min.	Typ.	Max.	Unit
Allowable high-level output current**Note 1**	I_{OH1}	Per pin for P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P125 to P127, P130, P140 to P147	1.6 V ≤ V_{DD} ≤ 5.5 V			-10.0 **Note 2**	mA
		Total of P40 to P47, P66, P67, P130, P140 (when duty ≤ 70%**Note 3**)	4.0 V ≤ V_{DD} ≤ 5.5 V			-55.0 **Note 4**	mA
			2.7 V ≤ V_{DD} < 4.0 V			-10.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			-5.0	mA
			1.6 V ≤ V_{DD} < 1.8 V			-2.5	mA
		Total of P00 to P07, P10 to P17, P22 to P27, P30 to P35, P50 to P57, P64, P65, P70 to P77, P80 to P87, P90 to P97, P125 to P127, P141 to P147 (when duty ≤ 70%**Note 3**)	4.0 V ≤ V_{DD} ≤ 5.5 V			-80.0 **Note 5**	mA
			2.7 V ≤ V_{DD} < 4.0 V			-19.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			-10.0	mA
			1.6 V ≤ V_{DD} < 1.8 V			-5.0	mA
		Total of all pins (when duty ≤ 70%**Note 3**)	1.6 V ≤ V_{DD} ≤ 5.5 V			-135.0 **Note 6**	mA
	I_{OH2}	Per pin for P20, P21, P121, P122	4.0 V ≤ V_{DD} ≤ 5.5 V			-3.0 **Note 2**	mA
			2.7 V ≤ V_{DD} < 4.0 V			-1.0 **Note 2**	mA
			1.8 V ≤ V_{DD} < 2.7 V			-1.0 **Note 2**	mA
			1.6 V ≤ V_{DD} < 1.8 V			-0.5 **Note 2**	mA
		Total of all pins (when duty ≤ 70%**Note 3**)	4.0 V ≤ V_{DD} ≤ 5.5 V			-20.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			-10.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			-5.0	mA
			1.6 V ≤ V_{DD} < 1.8 V			-5.0	mA

Note 1. Device operation is guaranteed at the listed currents even if current is flowing from the V_{DD} pin to an output pin.

Note 2. The combination of these and other pins must also not exceed the value for maximum total current.

Note 3. The listed currents apply when the duty cycle is no greater than 70%. Use the following formula to calculate the output current when the duty cycle is greater than 70%, where n is the duty cycle.

- Total output current from the listed pins = (I_{OH} × 0.7)/(n × 0.01)

  Example when n = 80% and I_{OH} = -10.0 mA

  Total output current from the listed pins = (-10.0 × 0.7)/(80 × 0.01) ≈ -8.7 mA

  Note that the duty cycle has no effect on the current that is allowed to flow into a single pin. A current higher than the absolute maximum rating must not flow into a single pin.

(Notes, Caution, and Remark continue on the next page.)

Note 4. The maximum value is -30 mA with an ambient operating temperature range of +85°C to +105°C.

Note 5. The maximum value is -50 mA with an ambient operating temperature range of +85°C to +105°C.

Note 6. The maximum values are respectively -100 mA and -60 mA with an ambient operating temperature range of -40 to +85°C and of +85°C to +105°C.

Caution **The following pins do not output high-level signals in the N-ch open-drain mode: P00 to P07, P10, P11, P16, P17, P22, P26, P27, P33 to P35, P40 to P47, P50, P52 to P54, P64 to P66, P75 to P77, P80 to P87, P93 to P97, P125, P130, P140, and P143 to P147**

Remark The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (2/7)

Item	Symbols	Conditions		Min.	Typ.	Max.	Unit
Allowable low-level output current**Note 1**	I_{OL1}	Per pin for P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P125 to P127, P130, P140 to P147				20.0 **Notes 2, 3**	mA
		Per pin for P60 to P63				15.0 **Note 2**	mA
		Total of P40 to P47, P66, P67, P130, P140 (when duty ≤ 70%**Note 4**)	4.0 V ≤ V_{DD} ≤ 5.5 V			70.0 **Note 5**	mA
			2.7 V ≤ V_{DD} < 4.0 V			15.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			9.0	mA
			1.6 V ≤ V_{DD} < 1.8 V			4.5	mA
		Total of P00 to P07, P10 to P17, P22 to P27, P30 to P35, P50 to P57, P64, P65, P70 to P77, P80 to P87, P90 to P97, P125 to P127, P141 to P147 (when duty ≤ 70%**Note 4**)	4.0 V ≤ V_{DD} ≤ 5.5 V			80.0 **Note 5**	mA
			2.7 V ≤ V_{DD} < 4.0 V			35.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			20.0	mA
			1.6 V ≤ V_{DD} < 1.8 V			10.0	mA
		Total of all pins (when duty ≤ 70%**Note 4**)				150.0 **Note 6**	mA
	I_{OL2}	Per pin for P20, P21, P121, P122	4.0 V ≤ V_{DD} ≤ 5.5 V			8.5**Note 2**	mA
			2.7 V ≤ V_{DD} < 4.0 V			1.5**Note 2**	mA
			1.8 V ≤ V_{DD} < 2.7 V			0.6**Note 2**	mA
			1.6 V ≤ V_{DD} < 1.8 V			0.4**Note 2**	mA
		Total of all pins (when duty ≤ 70%**Note 4**)	4.0 V ≤ V_{DD} ≤ 5.5 V			20	mA
			2.7 V ≤ V_{DD} < 4.0 V			20	mA
			1.8 V ≤ V_{DD} < 2.7 V			15	mA
			1.6 V ≤ V_{DD} < 1.8 V			10	mA

Note 1. Device operation is guaranteed at the listed currents even if current is flowing from an output pin to the EV_{SS}, or V_{SS} pin.

Note 2. The combination of these and other pins must also not exceed the value for maximum total current.

Note 3. The maximum rating for the following port pins is 40 mA when I_{OL1} = 40.0 mA is specified by the 40-mA port output control register (PTDC).
Pins P00, P05, and P16 of 44- to 52-pin products, and of 64-pin products with 64 to 128 Kbytes of flash ROM
Pins P07, P10, and P27 of 64-pin products with 256 to 512 Kbytes of flash ROM, and of 80- and 100-pin products

Note 4. The listed currents apply when the duty cycle is no greater than 70%. Use the following formula to calculate the output current when the duty cycle is greater than 70%, where n is the duty cycle.
- Total output current from the listed pins = (I_{OL} × 0.7)/(n × 0.01)

Example when n = 80% and I_{OL} = 10.0 mA
Total output current from the listed pins = (10.0 × 0.7)/(80 × 0.01) ≈ 8.7 mA
Note that the duty cycle has no effect on the current that is allowed to flow into a single pin. A current higher than the absolute maximum rating must not flow into a single pin.

Note 5. The maximum value is 40 mA with an ambient operating temperature range of +85°C to +105°C.

Note 6. The maximum value is 80 mA with an ambient operating temperature range of +85°C to +105°C.

Remark The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (3/7)

Item	Symbols	Conditions		Min.	Typ.	Max.	Unit
Input voltage, high	V_{IH1}	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P125 to P127, P140 to P147	Normal input buffer	0.8 V_{DD}		V_{DD}	V
	V_{IH2}	P02, P03, P05, P06, P11, P16, P17, P22, P26, P27, P33, P34, P40 to P47, P51, P53, P54, P64 to P66, P75, P76, P80 to P86, P93, P94, P96, P97, P125, P140 to P142, P144 to P147	TTL input buffer 4.0 V ≤ V_{DD} ≤ 5.5 V	2.2		V_{DD}	V
			TTL input buffer 3.3 V ≤ V_{DD} < 4.0 V	2.0		V_{DD}	V
			TTL input buffer 1.6 V ≤ V_{DD} < 3.3 V	1.5		V_{DD}	V
	V_{IH3}	P20, P21		0.7 V_{DD}		V_{DD}	V
	V_{IH4}	P60 to P63		0.7 V_{DD}		6.0	V
	V_{IH5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0.8 V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P125 to P127, P140 to P147	Normal input buffer	0		0.2 V_{DD}	V
	V_{IL2}	P02, P03, P05, P06, P11, P16, P17, P22, P26, P27, P33, P34, P40 to P47, P51, P53, P54, P64 to P66, P75, P76, P80 to P86, P93, P94, P96, P97, P125, P140 to P142, P144 to P147	TTL input buffer 4.0 V ≤ V_{DD} ≤ 5.5 V	0		0.8	V
			TTL input buffer 3.3 V ≤ V_{DD} < 4.0 V	0		0.5	V
			TTL input buffer 1.6 V ≤ V_{DD} < 3.3 V	0		0.32	V
	V_{IL3}	P20, P21		0		0.3 V_{DD}	V
	V_{IL4}	P60 to P63		0		0.3 V_{DD}	V
	V_{IL5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0		0.2 V_{DD}	V

Caution **The maximum value of V_{IH} of the following pins is V_{DD}, even in the N-ch open-drain mode: P00 to P07, P10, P11, P16, P17, P22, P26, P27, P33 to P35, P40 to P47, P50, P52 to P54, P64 to P66, P75 to P77, P80 to P87, P93 to P97, P125, P130, P140, and P143 to P147.**

Remark The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (4/7)

Item	Symbols	Conditions		Min.	Typ.	Max.	Unit
Output voltage, high	V_{OH1}	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P125 to P127, P130, P140 to P147	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH1} = -10.0 mA	V_{DD} -1.5			V
			4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH1} = -3.0 mA	V_{DD} -0.7			V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OH1} = -2.0 mA	V_{DD} -0.6			V
			1.8 V ≤ V_{DD} ≤ 5.5 V, I_{OH1} = -1.5 mA	V_{DD} -0.5			V
			1.6 V ≤ V_{DD} < 5.5 V, I_{OH1} = -1.0 mA	V_{DD} -0.5			V
	V_{OH2}	P20, P21, P121, P122	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH2} = -3.0 mA	V_{DD} -0.7			V
			2.7 V ≤ V_{DD} < 4.0 V, I_{OH2} = -1.0 mA	V_{DD} -0.5			V
			1.8 V ≤ V_{DD} < 2.7 V, I_{OH2} = -1.0 mA	V_{DD} -0.5			V
			1.6 V ≤ V_{DD} < 1.8 V, I_{OH2} = -0.5 mA	V_{DD} -0.5			V

Caution **The following pins do not output high-level signals in the N-ch open-drain mode: P00 to P07, P10, P11, P16, P17, P22, P26, P27, P33 to P35, P40 to P47, P50, P52 to P54, P64 to P66, P75 to P77, P80 to P87, P93 to P97, P125, P130, P140, and P143 to P147**

Remark The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (5/7)

Item	Symbols	Conditions			Min.	Typ.	Max.	Unit
Output voltage, low	V_{OL1}	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P125 to P127, P130, P140 to P147	4.0 V ≤ V_{DD} ≤ 5.5 V	I_{OL1} = 20.0 mA			1.3	V
				I_{OL1} = 40.0 mA**Note**			1.3	V
			4.0 V ≤ V_{DD} ≤ 5.5 V	I_{OL1} = 8.5 mA			0.7	V
				I_{OL1} = 17.0 mA**Note**			0.7	V
			2.7 V ≤ V_{DD} ≤ 5.5 V	I_{OL1} = 3.0 mA			0.6	V
				I_{OL1} = 6.0 mA**Note**			0.6	V
			2.7 V ≤ V_{DD} ≤ 5.5 V	I_{OL1} = 1.5 mA			0.4	V
				I_{OL1} = 3.0 mA**Note**			0.4	V
			1.8 V ≤ V_{DD} ≤ 5.5 V	I_{OL1} = 0.6 mA			0.4	V
				I_{OL1} = 1.2 mA**Note**			0.4	V
			1.6 V ≤ V_{DD} ≤ 5.5 V	I_{OL1} = 0.3 mA			0.4	V
				I_{OL1} = 0.6 mA**Note**			0.4	V
	V_{OL2}	P20, P21, P121, P122	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL2} = 8.5 mA				0.7	V
			2.7 V ≤ V_{DD} < 4.0 V, I_{OL2} = 1.5 mA				0.5	V
			1.8 V ≤ V_{DD} < 2.7 V, I_{OL2} = 0.6 mA				0.4	V
			1.6 V ≤ V_{DD} < 1.8 V, I_{OL2} = 0.4 mA				0.4	V
	V_{OL3}	P60 to P63	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL3} = 15.0 mA				2.0	V
			4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL3} = 5.0 mA				0.4	V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OL3} = 3.0 mA				0.4	V
			1.8 V ≤ V_{DD} ≤ 5.5 V, I_{OL3} = 2.0 mA				0.4	V
			1.6 V ≤ V_{DD} ≤ 5.5 V, I_{OL3} = 1.0 mA				0.4	V

Note The listed value applies when I_{OL1} = 40.0 mA is specified for the following port pins by the 40-mA port output control register (PTDC).
Pins P00, P05, and P16 of 44- to 52-pin products, and of 64-pin products with 64 to 128 Kbytes of flash ROM
Pins P07, P10, and P27 of 64-pin products with 256 to 512 Kbytes of flash ROM, and of 80- and 100-pin products

Remark The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (6/7)

Item	Symbols	Conditions			Min.	Typ.	Max.	Unit
Output current[Note]	CCDIOL	P74 to P77, P60 to P63	CCSm = 01H	4.0 V ≤ V_{DD} ≤ 5.5 V	1.0	1.8	2.6	mA
				2.7 V ≤ V_{DD} < 4.0 V	0.8	1.5	2.3	mA
			CCSm = 02H	4.0 V ≤ V_{DD} ≤ 5.5 V	3.0	4.9	6.5	mA
				3.0 V ≤ V_{DD} < 4.0 V	2.7	4.3	5.9	mA
			CCSm = 03H	4.0 V ≤ V_{DD} ≤ 5.5 V	6.6	10.0	13.2	mA
				3.3 V ≤ V_{DD} < 4.0 V	6.0	9.1	12.1	mA
		P60 to P63	CCSm = 04H	4.0 V ≤ V_{DD} ≤ 5.5 V	10.2	15.0	19.8	mA
				3.3 V ≤ V_{DD} < 4.0 V	9.4	13.8	18.2	mA

Note The listed currents apply when the output current control function is enabled.

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (7/7)

Item	Symbols	Conditions		Min.	Typ.	Max.	Unit
Input leakage current, high	I_{LIH1}	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P125 to P127, P140 to P147	V_I = V_{DD}			0.5	μA
	I_{LIH2}	P20, P21, P137, $\overline{\text{RESET}}$	V_I = V_{DD}			0.5	μA
	I_{LIH3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V_I = V_{DD}			0.5	μA
Input leakage current, low	I_{LIL1}	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P125 to P127, P140 to P147	V_I = EV_{SS}			-0.5	μA
	I_{LIL2}	P20, P21, P137, $\overline{\text{RESET}}$	V_I = V_{SS}			-0.5	μA
	I_{LIL3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V_I = V_{SS}			-0.5	μA
On-chip pull-up resistance	R_U	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P121, P122, P125 to P127, P140 to P147	V_I = EV_{SS}, In input port	10	20	100	kΩ

Remark The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

2.3.2 Supply current characteristics

1. 44- to 64-pin products with 256 to 512 Kbytes of flash ROM and 80- to 100-pin products

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (1/4)

Item	Symbols	Conditions					Min.	Typ.	Max.	Unit
Supply current **Note 1**	I_{DD1}	Operating mode	HS (high-speed main) mode	f_{IH} = 32 MHz**Note 2**	Basic operation	V_{DD} = 5.0 V		1.6	—	mA
						V_{DD} = 1.8 V		1.6	—	
					Normal operation	V_{DD} = 5.0 V		3.5	5.9	mA
						V_{DD} = 1.8 V		3.5	5.9	
			LS (low-speed main) mode	f_{IH} = 24 MHz**Note 2**	Normal operation	V_{DD} = 5.0 V		2.6	4.5	mA
						V_{DD} = 1.8 V		2.6	4.5	
				f_{IH} = 16 MHz**Note 2**	Normal operation	V_{DD} = 5.0 V		1.9	3.2	mA
						V_{DD} = 1.8 V		1.9	3.2	
				f_{IM} = 4 MHz**Note 3**	Normal operation	V_{DD} = 5.0 V		0.5	0.9	mA
						V_{DD} = 1.6 V		0.5	0.9	
			LP (low-power main) mode	f_{IM} = 2 MHz**Note 3**	Normal operation	V_{DD} = 5.0 V		227	379	μA
						V_{DD} = 1.6 V		226	378	
				f_{IM} = 1 MHz**Note 3**	Normal operation	V_{DD} = 5.0 V		126	205	μA
						V_{DD} = 1.6 V		125	204	
			HS (high-speed main) mode	f_{MX} = 20 MHz**Note 4**, Square wave input	Normal operation	V_{DD} = 5.0 V		2.3	3.8	mA
						V_{DD} = 1.8 V		2.2	3.8	
			LS (low-speed main) mode	f_{MX} = 20 MHz**Note 4**, Square wave input	Normal operation	V_{DD} = 5.0 V		2.2	3.7	mA
						V_{DD} = 1.8 V		2.1	3.6	
				f_{MX} = 20 MHz**Note 4**, Resonator connection	Normal operation	V_{DD} = 5.0 V		2.3	3.9	mA
						V_{DD} = 1.8 V		2.3	3.8	
				f_{MX} = 10 MHz**Note 4**, Square wave input	Normal operation	V_{DD} = 5.0 V		1.1	1.9	mA
						V_{DD} = 1.8 V		1.1	1.9	
				f_{MX} = 10 MHz**Note 4**, Resonator connection	Normal operation	V_{DD} = 5.0 V		1.2	2.1	mA
						V_{DD} = 1.8 V		1.2	2.1	
				f_{MX} = 8 MHz**Note 4**, Square wave input	Normal operation	V_{DD} = 5.0 V		0.9	1.5	mA
						V_{DD} = 1.8 V		0.9	1.5	
				f_{MX} = 8 MHz**Note 4**, Resonator connection	Normal operation	V_{DD} = 5.0 V		1.0	1.7	mA
						V_{DD} = 1.8 V		1.0	1.7	

Note 1. The listed currents are the total currents flowing into V_{DD}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, V_{SS}, or EV_{SS}. In the HS (high-speed main), LS (low-speed main), and LP (low-power main) modes, the currents in the Typ. column do not include the operating currents of the peripheral modules. The currents in the Max. column include the operating currents of the PCLBUZ, TAU, SAU, and IICA modules. The operating currents of other peripheral modules are not included.

Note 2. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 3. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

(Note and Remarks are listed on the next page.)

Note 4. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Remark 1. f_{IH}: High-speed on-chip oscillator clock frequency
Remark 2. f_{IM}: Middle-speed on-chip oscillator clock frequency
Remark 3. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
Remark 4. The typical value for the ambient operating temperature (T_A) is +25°C unless otherwise specified.

1. 44- to 64-pin products with 256 to 512 Kbytes of flash ROM and 80- to 100-pin products

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (2/4)

Item	Symbols	Conditions					Min.	Typ.	Max.	Unit
Supply current **Note 1**	I_{DD1}	Operating mode	Subsystem clock operation mode	f_{SUB} = 32.768 kHz **Note 2**, Low-speed on-chip oscillator operation	Normal operation	T_A = -40°C		3.8	6.7	μA
						T_A = +25°C		4.2	7.0	
						T_A = +50°C		4.7	12.1	
						T_A = +70°C		5.6	25.5	
						T_A = +85°C		6.8	41.0	
						T_A = +105°C		10.8	87.2	
				f_{SUB} = 32.768 kHz **Note 3**, Square wave input	Normal operation	T_A = -40°C		4.0	7.3	μA
						T_A = +25°C		4.2	8.2	
						T_A = +50°C		4.7	13.4	
						T_A = +70°C		5.5	26.7	
						T_A = +85°C		6.7	42.8	
						T_A = +105°C		10.7	89.3	
				f_{SUB} = 32.768 kHz **Note 3**, Resonator connection	Normal operation	T_A = -40°C		3.9	6.9	μA
						T_A = +25°C		4.1	7.3	
						T_A = +50°C		4.5	12.4	
						T_A = +70°C		5.3	25.6	
						T_A = +85°C		6.5	41.1	
						T_A = +105°C		10.2	87.0	

Note 1. The listed currents are the total currents flowing into V_{DD}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, V_{SS}, or EV_{SS}. In the subsystem clock operation mode, the currents in the Typ. and Max. columns do not include the operating currents of the peripheral modules.

Note 2. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped.

Note 3. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, middle-speed on-chip oscillator, and low-speed on-chip oscillator are stopped, and the low power consumption oscillation 3 is specified (AMPHS1, AMPHS0 = 1, 1).

Remark 1. f_{IL}: Low-speed on-chip oscillator clock frequency

Remark 2. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

1. 44- to 64-pin products with 256 to 512 Kbytes of flash ROM and 80- to 100-pin products

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (3/4)

Item	Symbols	Conditions				Min.	Typ.	Max.	Unit
Supply current**Note 1**	I_{DD2} **Note 2**	HALT mode	HS (high-speed main) mode	f_{IH} = 32 MHz**Note 3**	V_{DD} = 5.0 V		0.61	2.24	mA
					V_{DD} = 1.8 V		0.60	2.23	
			LS (low-speed main) mode	f_{IH} = 24 MHz**Note 3**	V_{DD} = 5.0 V		0.51	1.74	mA
					V_{DD} = 1.8 V		0.50	1.73	
				f_{IH} = 16 MHz**Note 3**	V_{DD} = 5.0 V		0.47	1.33	mA
					V_{DD} = 1.8 V		0.47	1.32	
				f_{IM} = 4 MHz**Note 4**	V_{DD} = 5.0 V		0.09	0.31	mA
					V_{DD} = 1.6 V		0.09	0.30	
			LP (low-power main) mode	f_{IM} = 2 MHz**Note 4**	V_{DD} = 5.0 V		38	140	μA
					V_{DD} = 1.6 V		37	138	
				f_{IM} = 1 MHz**Note 4**	V_{DD} = 5.0 V		32	86	μA
					V_{DD} = 1.6 V		31	85	
			HS (high-speed main) mode	f_{MX} = 20 MHz**Note 5**, Square wave input	V_{DD} = 5.0 V		0.21	1.19	mA
					V_{DD} = 1.8 V		0.14	1.10	
			LS (low-speed main) mode	f_{MX} = 20 MHz**Note 5**, Square wave input	V_{DD} = 5.0 V		0.20	1.17	mA
					V_{DD} = 1.8 V		0.14	1.10	
				f_{MX} = 20 MHz**Note 5**, Resonator connection	V_{DD} = 5.0 V		0.51	1.56	mA
					V_{DD} = 1.8 V		0.49	1.54	
				f_{MX} = 10 MHz**Note 5**, Square wave input	V_{DD} = 5.0 V		0.15	0.65	mA
					V_{DD} = 1.8 V		0.12	0.61	
				f_{MX} = 10 MHz**Note 5**, Resonator connection	V_{DD} = 5.0 V		0.30	0.84	mA
					V_{DD} = 1.8 V		0.29	0.82	
				f_{MX} = 8 MHz**Note 5**, Square wave input	V_{DD} = 5.0 V		0.13	0.54	mA
					V_{DD} = 1.8 V		0.10	0.50	
				f_{MX} = 8 MHz**Note 5**, Resonator connection	V_{DD} = 5.0 V		0.26	0.70	mA
					V_{DD} = 1.8 V		0.25	0.68	

Note 1. The listed currents are the total currents flowing into V_{DD}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, V_{SS}, or EV_{SS}. In the HS (high-speed main), LS (low-speed main), and LP (low-power main) modes, the currents in the Typ. column do not include the operating currents of the peripheral modules. The currents in the Max. column include the operating currents of the PCLBUZ, TAU, SAU, and IICA modules. The operating currents of other peripheral modules are not included.

Note 2. The listed currents apply when the HALT instruction has been fetched from the flash memory for execution.

Note 3. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 4. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 5. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

(Remarks are listed on the next page.)

Remark 1. f_{IH}: High-speed on-chip oscillator clock frequency
Remark 2. f_{IM}: Middle-speed on-chip oscillator clock frequency
Remark 3. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
Remark 4. The typical value for the ambient operating temperature (T_A) is +25°C unless otherwise specified.

1. 44- to 64-pin products with 256 to 512 Kbytes of flash ROM and 80- to 100-pin products

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (4/4)

Item	Symbols	Conditions				Min.	Typ.	Max.	Unit
Supply current **Note 1**	I_{DD2} **Note 2**	HALT mode	Subsystem clock operation mode	f_{SUB} = 32.768 kHz **Note 3**, Low-speed on-chip oscillator operation	T_A = -40°C		0.76	3.30	μA
					T_A = +25°C		0.90	3.38	
					T_A = +50°C		1.12	8.20	
					T_A = +70°C		1.61	21.16	
					T_A = +85°C		2.53	36.29	
					T_A = +105°C		5.39	81.33	
				f_{SUB} = 32.768 kHz, Square wave input **Note 4**	T_A = -40°C		0.41	3.39	μA
					T_A = +25°C		0.63	4.23	
					T_A = +50°C		0.87	9.24	
					T_A = +70°C		1.38	22.24	
					T_A = +85°C		2.35	38.01	
					T_A = +105°C		5.22	83.22	
				f_{SUB} = 32.768 kHz, Resonator connection **Note 5**	T_A = -40°C		0.36	3.04	μA
					T_A = +25°C		0.50	3.32	
					T_A = +50°C		0.72	8.19	
					T_A = +70°C		1.22	21.12	
					T_A = +85°C		2.11	36.33	
					T_A = +105°C		4.92	81.12	
	I_{DD3}	STOP mode	RAMSDMD = 0, RAMSDS = 0 **Note 6**		T_A = -40°C		0.24	2.20	μA
					T_A = +25°C		0.34	2.20	
					T_A = +50°C		0.55	7.00	
					T_A = +70°C		1.06	20.00	
					T_A = +85°C		1.92	35.00	
					T_A = +105°C		4.76	80.00	
			RAMSDMD = 1, RAMSDS = 1 **Note 7**		T_A = -40°C		0.23	2.20	μA
					T_A = +25°C		0.33	2.20	
					T_A = +50°C		0.51	7.00	
					T_A = +70°C		0.91	17.00	
					T_A = +85°C		1.66	30.00	
					T_A = +105°C		4.06	70.00	
			RAMSDMD = 1, RAMSDS = 1, 128-Hz realtime clock operation **Note 8**		T_A = -40°C		0.28	2.30	μA
					T_A = +25°C		0.40	2.30	
					T_A = +50°C		0.60	7.10	
					T_A = +70°C		0.99	17.10	
					T_A = +85°C		1.76	30.10	
					T_A = +105°C		4.16	70.10	

(Notes and Remarks are listed on the next page.)

Note 1. The listed currents are the total currents flowing into V_{DD}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, V_{SS}, or EV_{SS}. In the subsystem clock operation mode, the currents in the Typ. and Max. columns do not include the operating currents of the peripheral modules.

Note 2. The listed currents apply when the HALT instruction has been fetched from the flash memory for execution.

Note 3. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped.

Note 4. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and low-speed on-chip oscillator are stopped.

Note 5. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and low-speed on-chip oscillator are stopped, and the setting of RTCLPC is 1, and the low power consumption oscillation 3 is specified (AMPHS1, AMPHS0 = 1, 1).

Note 6. The listed currents with this setting allow retention of the contents of the entire RAM area. The listed currents apply when the low-speed on-chip oscillator and subsystem clock oscillation are stopped. For the current for operation of the subsystem clock in the STOP mode, refer to that in the HALT mode.

Note 7. The listed currents with this setting allow retention of the contents of a specified 4-Kbyte area of the RAM. The listed currents apply when the low-speed on-chip oscillator and subsystem clock oscillation are stopped.

Note 8. The listed currents with this setting allow retention of the contents of a specified 4-Kbyte area of the RAM. The listed currents apply when the low-speed on-chip oscillator is stopped, the setting of RTCLPC is 1, and the low power consumption oscillation 3 is specified (AMPHS1, AMPHS0 = 1, 1). The current flowing into the RTC is included.

Remark 1. f_{IL}: Low-speed on-chip oscillator clock frequency

Remark 2. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

2. Peripheral functions (common to all products)

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (1/3)

Item	Symbols	Conditions		Min.	Typ.	Max.	Unit
High-speed on-chip oscillator operating current	I_{FIH} **Note 1**				345		μA
Middle-speed on-chip oscillator operating current	I_{FIM} **Note 1**				20		μA
Low-speed on-chip oscillator operating current	I_{FIL} **Note 1**				0.3		μA
RTC operating current	I_{RTC} **Notes 1, 2, 3**	f_{RTCCLK} = 32.768 kHz			0.005		μA
		f_{RTCCLK} = 128 Hz			0.002		μA
32-bit interval timer operating current	I_{IT} **Notes 1, 2, 4**				0.04		μA
8-bit interval timers operating current	I_{TMT} **Notes 1, 2, 5**	f_{SUB} = 32.768 kHz, f_{MAIN} stopped	8-bit counter mode × 2 ch operation		0.08		μA
			16-bit counter mode operation		0.06		μA
Timer RJ operating current	I_{TMRJ} **Note 6**	f_{SUB} = 32.768 kHz, f_{MAIN} stopped, per unit			0.14		μA
16-bit timers KB40, KB41, and KB42 operating current	I_{TMKB} **Note 7**	Standalone mode, timer output disabled, f_{HOCO} = 64 MHz, per unit			530		μA
External signal sampler operating current	I_{EXSD} **Note 8**	f_{SUB} = 32.768 kHz, f_{MAIN} stopped			0.03		μA
Watchdog timer operating current	I_{WDT} **Notes 1, 2, 9**	f_{IL} = 32.768 kHz (typ.)			0.32		μA
Oscillation stop detector operating current	I_{OSDC} **Note 1**				0.02		μA
A/D converter operating current	I_{ADC} **Notes 1, 10**	When conversion at maximum speed	Normal mode, AV_{REFP} = V_{DD} = 5.0 V		0.95	1.6	mA
			Low voltage mode, AV_{REFP} = V_{DD} = 3.0 V		0.5	0.75	mA
AV_{REFP} current	I_{ADREF} **Note 11**	AV_{REFP} = 5.0 V			52		μA
A/D converter internal reference voltage current	I_{ADREF} **Note 1**				114		μA
Temperature sensor operating current	I_{TMPS} **Note 1**				110		μA
D/A converter operating current	I_{DAC} **Notes 1, 12**	Per channel			150		μA
Comparator operating current	I_{CMP} **Notes 1, 13**				6		μA
LVD operating current	I_{LVD0} **Notes 1, 14**				0.02		μA
	I_{LVD1} **Notes 1, 14**				0.02		μA

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (2/3)

Item	Symbols	Conditions			Min.	Typ.	Max.	Unit
Self-programming operating current	I_{FSP} **Notes 1, 15**					2.5	12.2	mA
Data flash rewrite operating current	I_{BGO} **Notes 1, 16**					2.5	12.2	mA
SNOOZE mode sequencer operating current	I_{SMS} **Notes 1, 17**	f_{IH} = 32 MHz	44- to 64-pin products with 256 to 512 Kbytes of flash ROM and 80- and 100-pin products			1.5		mA
		f_{IL} = 32.768 kHz	44- to 64-pin products with 256 to 512 Kbytes of flash ROM and 80- and 100-pin products			1.6		µA
SNOOZE operating current	I_{SNOZ} **Note 1**	f_{IH} = 32 MHz	ADC is in use	The ADC is shifting from the STOP mode to the SNOOZE mode.**Note 18**		0.6	0.81	mA
				The ADC is operating in the low-voltage mode. AV_{REFP} = V_{DD} = 3.0 V		1.2	1.56	mA
			Simplified SPI (CSI)/UART is in use			0.7	0.92	mA
			SMS**Note 19**	44- to 64-pin products with 256 to 512 Kbytes of flash ROM and 80- and 100-pin products		2.0		mA
Low-speed peripheral clock supply current	I_{SXP} **Notes 1, 20**	RTCLPC = 0				0.22		µA
Output current control operating current	I_{CCDA} **Notes 1, 21**	The setting of the CCDE register is not 00H.				100		µA
	I_{CCDP} **Notes 22, 23**	Per single controlled current drive port pin		Setting of the low-level output current: Hi-Z		30		µA
				Setting of the low-level output current: 2 to 15 mA		200		µA
Operating current of the true random number generator	I_{TRNG} **Note 1**					1.1		mA

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (3/3)

Item	Symbols	Conditions			Min.	Typ.	Max.	Unit
LCD operating current	I_{LCD1} **Notes 1, 24, 25**	External resistance division method	f_{LCD} = f_{SUB} LCD clock = 128 Hz 1/3 bias, four time slices	V_{DD} = 5.0 V V_{L4} = 5.00 V		0.02		μA
	I_{LCD2}**Note 1**	Internal voltage boosting method	f_{LCD} = f_{SUB} LCD clock = 128 Hz 1/3 bias, four time slices, V_{L1} reference	V_{DD} = 3.0 V V_{L4} = 3.03 V (V_{LCD4-0} = 04H)		0.74		μA
				V_{DD} = 5.0 V V_{L4} = 5.01 V (V_{LCD4-0} = 18H)		1.03		μA
			f_{LCD} = f_{SUB} LCD clock = 128 Hz 1/3 bias, four time slices, V_{L2} reference**Note 26**	V_{DD} = 3.0 V V_{L4} = 3.03 V (V_{LCD4-0} = 04H)		0.63		μA
				V_{DD} = 5.0 V V_{L4} = 5.03 V (V_{LCD4-0} = 18H)		0.83		μA
	I_{LCD3}**Note 1**	Capacitor split method	f_{LCD} = f_{SUB} LCD clock = 128 Hz 1/3 bias, four time slices, V_{DD} reference	V_{DD} = 3.0 V V_{L4} = 3.00 V		0.14		μA
			f_{LCD} = f_{SUB} LCD clock = 128 Hz 1/3 bias, four time slices, V_{L4} reference	V_{DD} = 5.0 V V_{L4} = 3.04 V		0.63		μA

Note 1. This current flows into V_{DD}.

Note 2. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, and high-speed system clock are stopped.

Note 3. This current flows into the realtime clock (RTC). It does not include the operating current of the low-speed on-chip oscillator or the XT1 oscillator. The supply current of the RL78 microcontrollers is the sum of either I_{DD1} or I_{DD2}, and I_{RTC}, when the realtime clock is operating or in the HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be included in the supply current. I_{DD2} in the subsystem clock operation mode includes the operating current of the realtime clock.

Note 4. This current only flows to the 32-bit interval timer. It does not include the operating current of the low-speed on-chip oscillator or the XT1 oscillator. The supply current of the RL78 microcontrollers is the sum of either I_{DD1} or I_{DD2}, and I_{IT}, when the 32-bit interval timer is operating or in the HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be included in the supply current.

Note 5. This current only flows to the 8-bit interval timer. It does not include the operating current of the XT1 oscillator. The supply current of the RL78 microcontrollers is the sum of either I_{DD1} or I_{DD2} and I_{TMT} when the 8-bit interval timer is operating or in the HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be included in the supply current.

Note 6. This current only flows to the timer RJ. It does not include the operating current of the XT1 oscillator. The supply current of the RL78 microcontrollers is the sum of either I_{DD1} or I_{DD2} and I_{TMRJ} when the timer RJ is operating or in the HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be included in the supply current.

Note 7. This current only flows to the 16-bit timers KB40, KB41, and KB42. It does not include the operating current of the high-speed on-chip oscillator. The supply current of the RL78 microcontrollers is the sum of either I_{DD1} or I_{DD2} and I_{TMKB} when the 16-bit timers KB40, KB41, and KB42 are operating or in the HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be included in the supply current.

Note 8. This current only flows to the external signal sampler. It does not include the operating current of the low-speed on-chip oscillator, XT1 oscillator, or 8-bit interval timer. The supply current of the RL78 microcontrollers is the sum of either I_{DD1} or I_{DD2} and I_{EXSD} when the external signal sampler is operating or in the HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be included in the supply current.

Note 9. This current only flows to the watchdog timer. It includes the operating current of the low-speed on-chip oscillator. The supply current of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{WDT} when the watchdog timer is operating.

Note 10. This current only flows to the A/D converter. The supply current of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter is operating or in the HALT mode.

Note 11. This current flows into AV_{REFP}.

Note 12. This current only flows to the D/A converter. The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and I_{DAC}, when the D/A converter is operating or in the HALT mode.

Note 13. This current only flows to the comparator. The supply current of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{CMP} when the comparator is in operation.

Note 14. This current only flows to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{LVD} when the LVD circuit is in operation.

Note 15. This current only flows during self-programming.

Note 16. This current only flows while the data flash memory is being rewritten.

Note 17. This current only flows into the SNOOZE mode sequencer. Note that the operating current of the low-speed on-chip oscillator and the XT1 oscillator are not included. The supply current of the RL78 microcontrollers is the sum of either I_{DD1} or I_{DD2}, and I_{SMS}, when the SNOOZE mode sequencer is operating or in the HALT mode.

Note 18. For shift time to the SNOOZE mode, see **27.3.3 SNOOZE mode** in the RL78/L23 User's Manual.

Note 19. The listed values apply when the SNOOZE mode sequencer is in normal operation equivalent to I_{DD1}. They do not include the current flowing into the peripheral functions other than the SNOOZE mode sequencer.

Note 20. This current is added to the supply current in the HALT mode when the setting of RTCLPC is 0 in the STOP mode, or when the setting of RTCLPC is 0 with the subsystem clock X (f_{SX}) selected as the CPU clock, while the subsystem clock X (f_{SX}) is oscillating.

Note 21. This current is added to the supply current when the output voltage control port is set.

Note 22. This current does not include the current flowing into the I/O port pins.

Note 23. This current flows to V_{DD}.

Note 24. This current only flows to the LCD controller/driver. The supply current of the RL78 microcontrollers is the sum of the supply current (I_{DD1} or I_{DD2}) and LCD operating current (I_{LCD1}, I_{LCD2}, or I_{LCD3}) when the LCD controller/driver is operating while the MCU is operating or in the HALT mode. It does not include the current flowing into the LCD panel. The values in the Typ. and Max. columns apply under the following conditions.

- Setting 20 pins as the segment function and blinking all
- Selecting f_{SUB} when LCD clock = 128 Hz (LCDC0 = 07H)
- Setting four time slices and 1/3 bias

Note 25. This current does not include the current flowing into the external division resistor when the external resistance division method is in use.

Note 26. In addition to these conditions, V_{L2} (Max.) + 0.1 V ≤ V_{DD} must be satisfied. For details, see **2.6.8.2 Internal voltage boosting method**.

Remark 1. f_{IL}: Low-speed on-chip oscillator clock frequency

Remark 2. f_{SX}: Subsystem clock X frequency

Remark 3. f_{CLK}: CPU/peripheral hardware clock frequency

Remark 4. The typical value for the ambient operating temperature (T_A) is +25°C unless otherwise specified.

2.4 AC Characteristics

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (1/2)

Item	Symbols	Conditions			Min.	Typ.	Max.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{MAIN}) operation	HS (high-speed main) mode	1.8 V ≤ V_{DD} ≤ 5.5 V	0.03125		1	μs
				1.6 V ≤ V_{DD} ≤ 1.8 V	0.25		1	μs
			LS (low-speed main) mode	1.8 V ≤ V_{DD} ≤ 5.5 V	0.04167		1	μs
				1.6 V ≤ V_{DD} ≤ 1.8 V	0.25		1	μs
			LP (low-power main) mode	1.6 V ≤ V_{DD} ≤ 5.5 V	0.5		1	μs
		Subsystem clock (f_{SUB}) operation		1.6 V ≤ V_{DD} ≤ 5.5 V	26.041	30.5	31.3	μs
		In the self programming mode	HS (high-speed main) mode	1.8 V ≤ V_{DD} ≤ 5.5 V	0.03125		1	μs
				1.6 V ≤ V_{DD} ≤ 1.8 V	0.5		1	μs
			LS (low-speed main) mode	1.8 V ≤ V_{DD} ≤ 5.5 V	0.04167		1	μs
				1.6 V ≤ V_{DD} ≤ 1.8 V	0.5		1	μs
External system clock frequency	f_{EX}	1.8 V ≤ V_{DD} ≤ 5.5 V			1		20	MHz
		1.6 V ≤ V_{DD} < 1.8 V			1		4	MHz
	f_{EXS}				32		38.4	kHz
External system clock input high-level width, low-level width	t_{EXH}, t_{EXL}	1.8 V ≤ V_{DD} ≤ 5.5 V			24			ns
		1.6 V ≤ V_{DD} < 1.8 V			120			ns
	t_{EXHS}, t_{EXLS}				13.7			μs
TI00 to TI07 input high-level width, low-level width	t_{TIH}, t_{TIL}				1/f_{MCK} +10			ns
Timer RJ input cycle	t_C	TRJIO0, TRJIO1		2.7 V ≤ V_{DD} < 5.5 V	100			ns
				1.8 V ≤ V_{DD} < 2.7 V	300			ns
				1.6 V ≤ V_{DD} < 1.8 V	500			ns
Timer RJ Input high-level width, low-level width	t_{TJIH}, t_{TJIL}	TRJIO0, TRJIO1		2.7 V ≤ V_{DD} < 5.5 V	40			ns
				1.8 V ≤ V_{DD} < 2.7 V	120			ns
				1.6 V ≤ V_{DD} < 1.8 V	200			ns
TO00 to TO07, TKBO00, TKBO01, TKBO10, TKBO11, TKBO20, TKBO21, TRJIO0, TRJIO1, TRJO0, and TRJO1 output frequency	f_{TO}	HS (high-speed main) mode, LS (low-speed main) mode		4.0 V ≤ V_{DD} ≤ 5.5 V			16	MHz
				2.7 V ≤ V_{DD} < 4.0 V			8	MHz
				1.8 V ≤ V_{DD} < 2.7 V			4	MHz
				1.6 V ≤ V_{DD} < 1.8 V			2	MHz
		LP (low-power main) mode		1.6 V ≤ V_{DD} ≤ 5.5 V			2	MHz
PCLBUZ0, PCLBUZ1 output frequency	f_{PCL}	HS (high-speed main) mode, LS (low-speed main) mode		4.0 V ≤ V_{DD} ≤ 5.5 V			16	MHz
				2.7 V ≤ V_{DD} < 4.0 V			8	MHz
				1.8 V ≤ V_{DD} < 2.7 V			4	MHz
				1.6 V ≤ V_{DD} < 1.8 V			2	MHz
		LP (low-power main) mode		1.6 V ≤ V_{DD} < 5.5 V			2	MHz

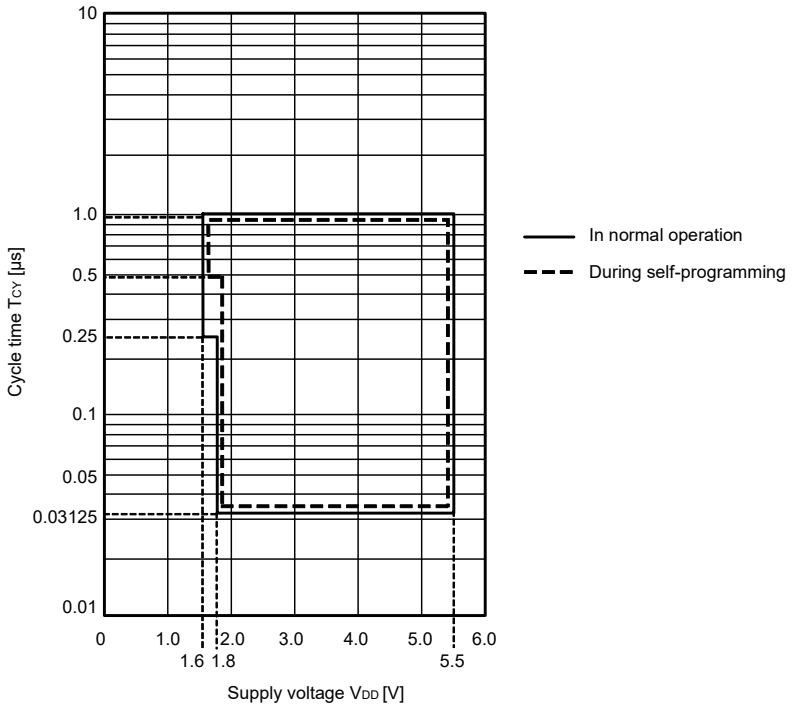
(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (2/2)

Item	Symbols	Conditions		Min.	Typ.	Max.	Unit
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}	INTP0 to INTP7	1.6 V ≤ V_{DD} ≤ 5.5 V	1			µs
Key-input high-level width, low-level width	t_{KRH}, t_{KRL}	KR0 to KR7	1.8 V ≤ V_{DD} ≤ 5.5 V	250			ns
			1.6 V ≤ V_{DD} < 1.8 V	1			µs
$\overline{\text{RESET}}$ low-level width	t_{RSL}			10			µs

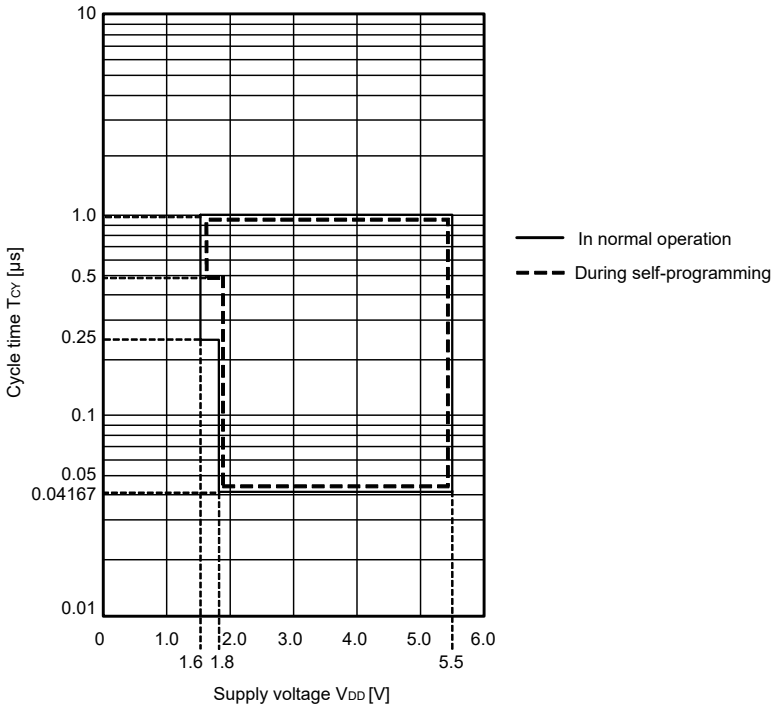
Remark f_{MCK}: Timer array unit operating clock frequency
To set this operating clock, use the CKSmn0 and CKSmn1 bits of the timer mode register mn (TMRmn) (m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7).

Minimum Instruction Execution Time during Main System Clock Operation

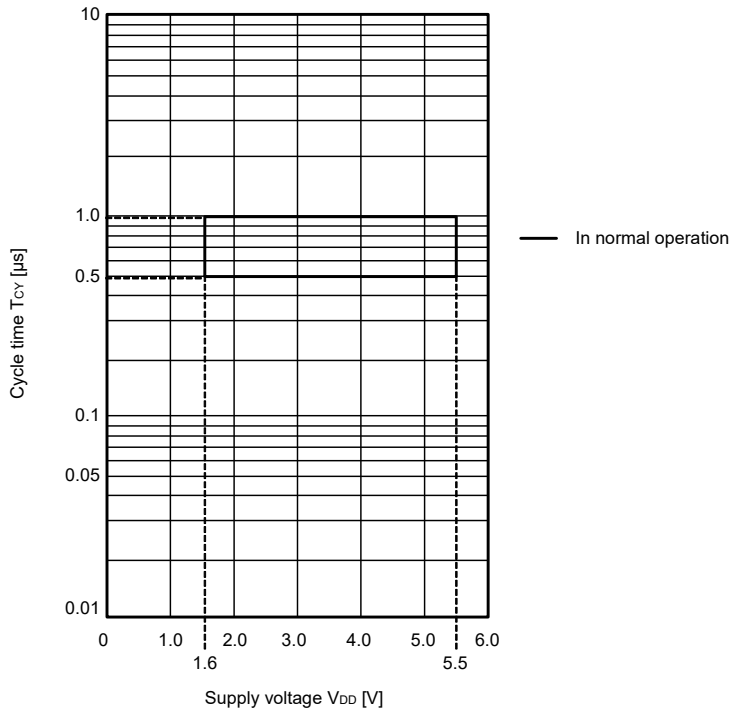
TCY vs VDD (HS (high-speed main) mode)



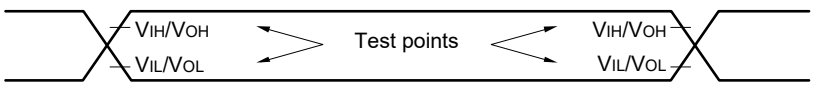
TCY vs VDD (LS (low-speed main) mode)



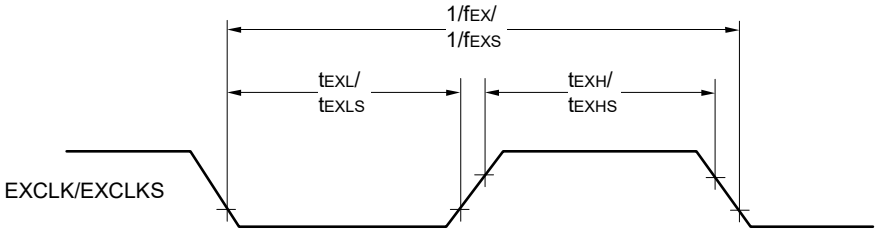
TCY vs VDD (LP (low-power main) mode)



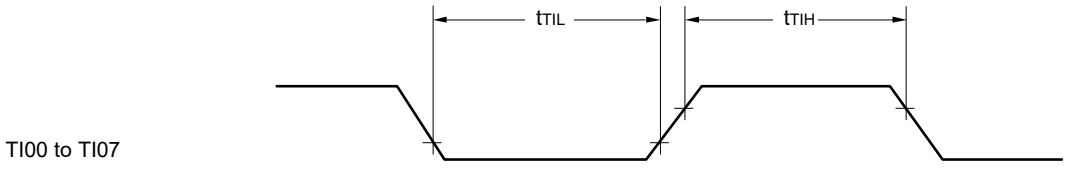
AC Timing Test Points

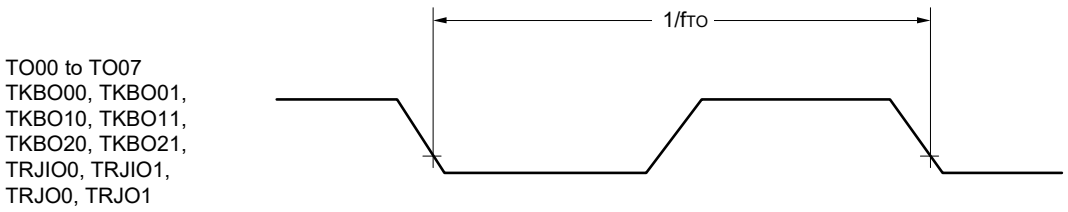


External System Clock Timing

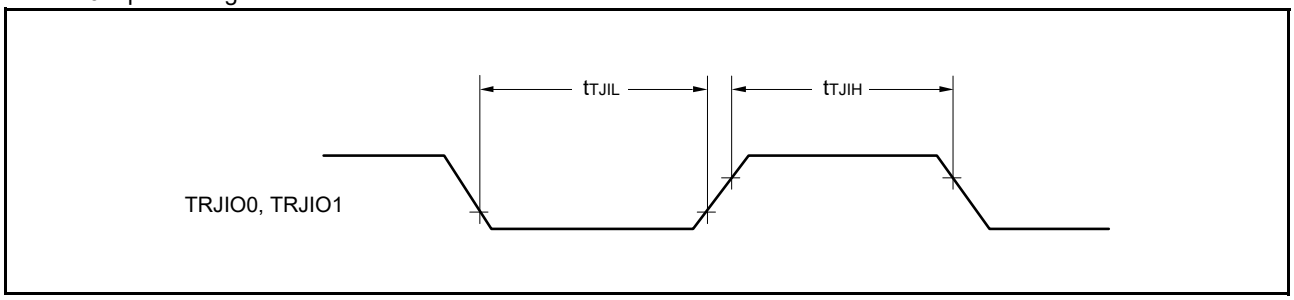


TI/TO Timing

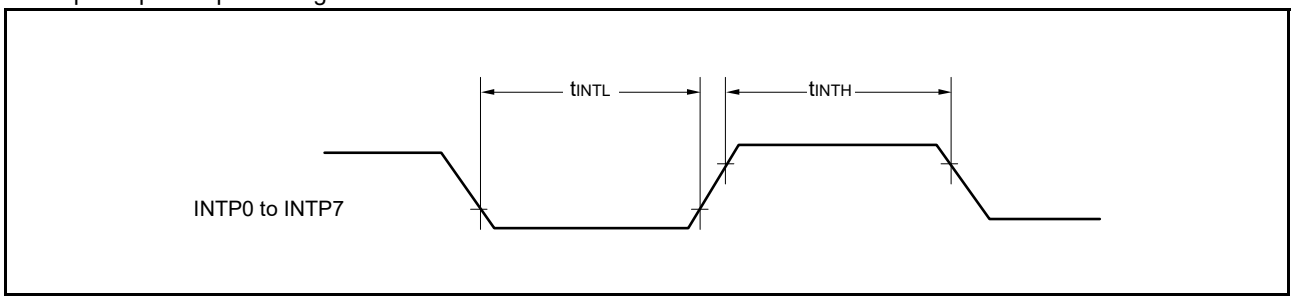




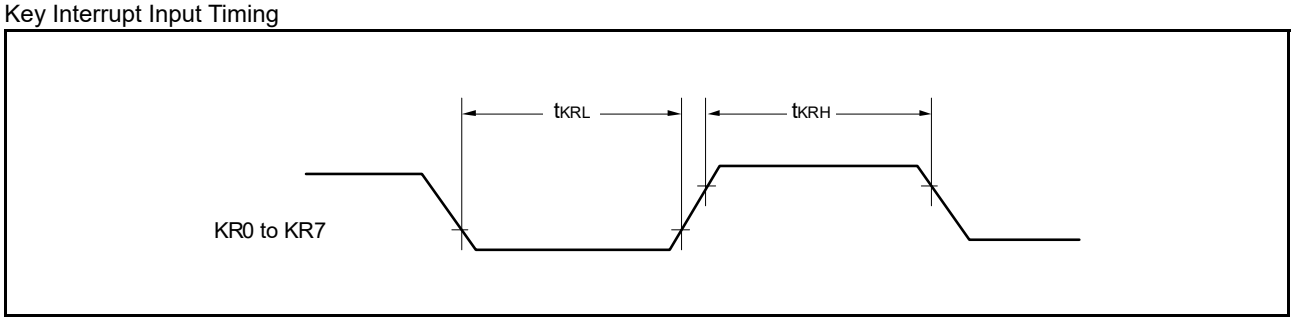
Timer RJ Input Timing



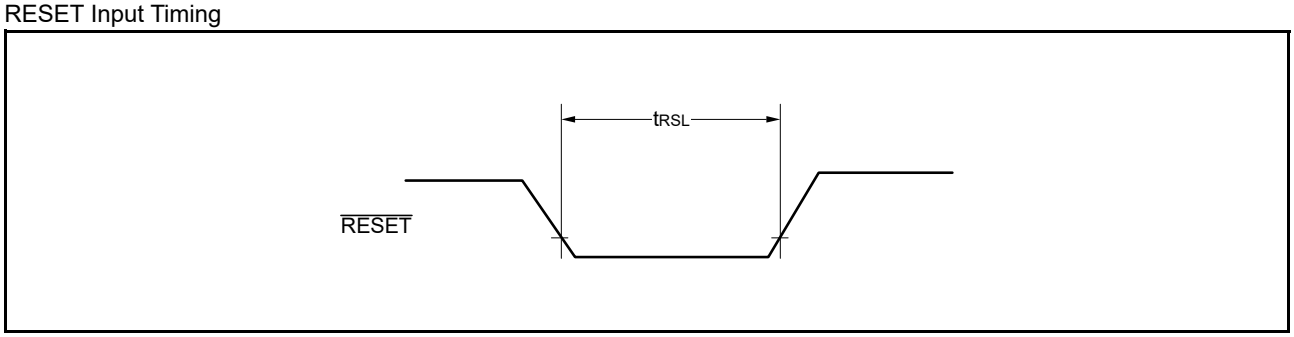
Interrupt Request Input Timing



Key Interrupt Input Timing

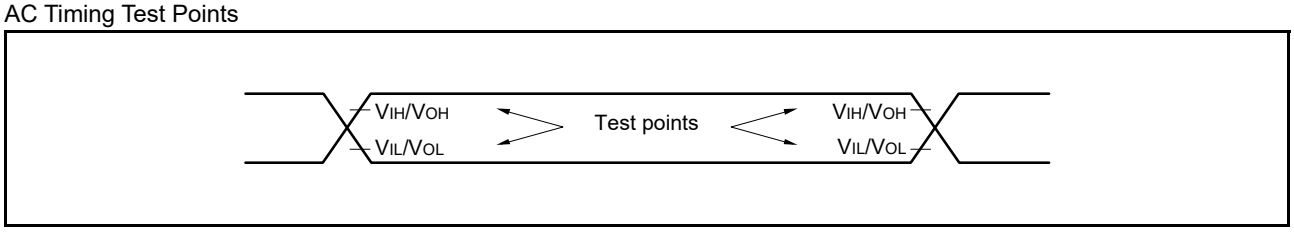


$\overline{\text{RESET}}$ Input Timing



2.5 Characteristics of the Peripheral Functions

AC Timing Test Points



2.5.1 Serial array unit

1. In UART communications with devices operating at same voltage levels

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Item	Symbols	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LP (low-power main) mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Transfer rate **Note 1**		1.6 V ≤ V_{DD} ≤ 5.5 V		f_{MCK}/6		f_{MCK}/6		f_{MCK}/6	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} **Note 2**		5.3		4		0.33	Mbps

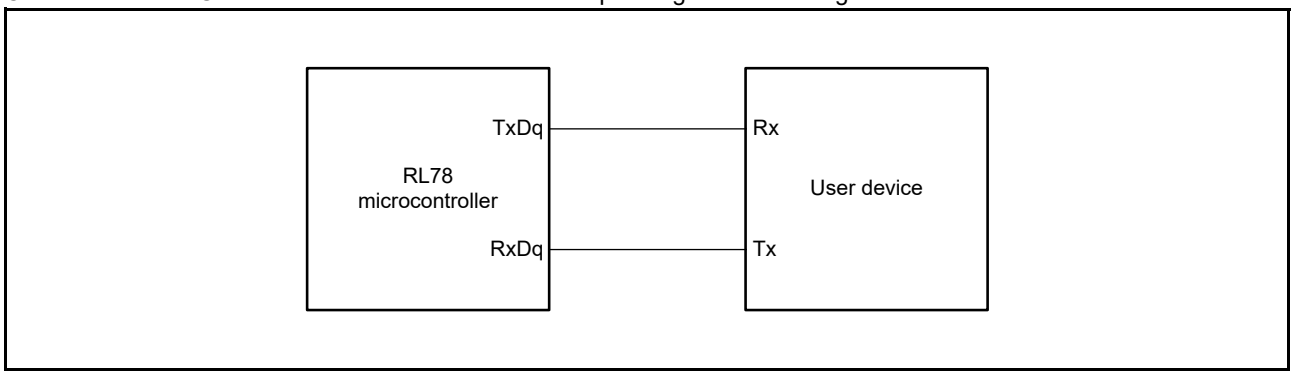
Note 1. The transfer rate in the SNOOZE mode is within the range from 4800 to 9600 bps.

Note 2. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are as follows.

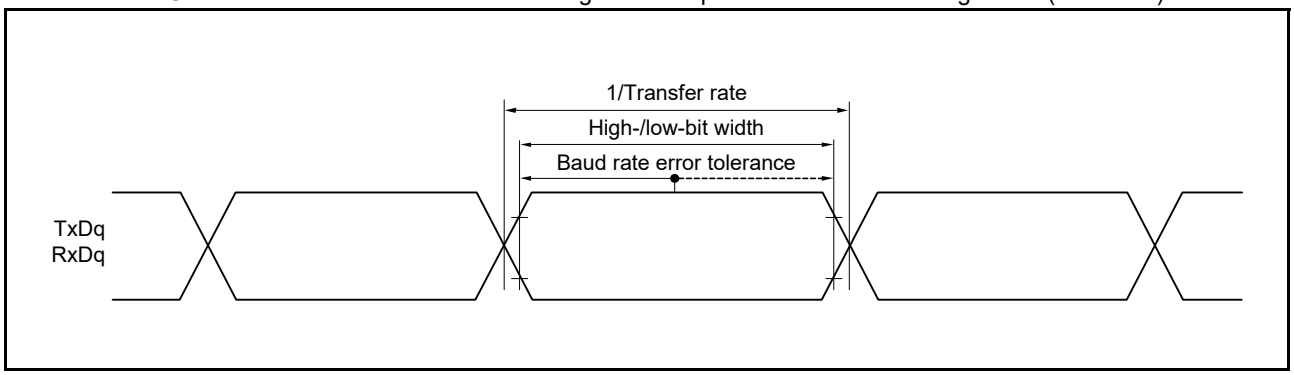
HS (high-speed main) mode : 32 MHz (1.8 V ≤ V_{DD} ≤ 5.5 V)
4 MHz (1.6 V ≤ V_{DD} ≤ 5.5 V)
LS (low-speed main) mode : 24 MHz (1.8 V ≤ V_{DD} ≤ 5.5 V)
4 MHz (1.6 V ≤ V_{DD} ≤ 5.5 V)
LP (low-power main) mode : 2 MHz (1.6 V ≤ V_{DD} ≤ 5.5 V)

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Connection in the UART communications with devices operating at same voltage levels



Bit width in the UART communications when interfacing devices operate at the same voltage level (reference)



Remark 1. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0 to 9, 12 to 14)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
To set this operating clock, set the CKSmn bit in the serial mode register mn (SMRmn) (m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13).

2. In simplified SPI (CSI) communications in the master mode with devices operating at same voltage levels with the internal SCKp clock (the ratings below are only applicable to CSI00)

(T_A = -40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Item	Symbols	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LP (low-power main) mode		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 2/f_{CLK}$	4.0 V ≤ V_{DD} ≤ 5.5 V	62.5		83.3		1000		ns
			2.7 V ≤ V_{DD} ≤ 5.5 V	83.3		125		1000		ns
SCKp high-level width, low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2 -7		t_{KCY1}/2 -10		t_{KCY1}/2 -50		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2 -10		t_{KCY1}/2 -15		t_{KCY1}/2 -50		ns
SIp setup time to the rising of SCKp **Note 1**	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V		23		33		110		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V		33		50		110		ns
SIp hold time from the rising of SCKp **Note 1**	t_{KSI1}	2.7 V ≤ V_{DD} ≤ 5.5 V		10		10		10		ns
Delay time from the falling of SCKp to an SOp output **Note 2**	t_{KSO1}	2.7 V ≤ V_{DD} ≤ 5.5 V, C = 20 pF **Note 3**			10		10		10	ns

Note 1. This is for when the settings are DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. When the settings are DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0, this is the setup time to or from the falling of SCKp.

Note 2. This is for when the settings are DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. When the settings are DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0, this is the delay time to the rising of SCKp.

Note 3. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using the port input mode register g (PIMg) and the port output mode register g (POMg).

Remark 1. The listed times are only valid when the peripheral I/O redirect function of CSI00 is not in use.

Remark 2. p: CSI number (p = 00), g: PIM and POM number (g = 1), m: Unit number (m = 0), n: Channel number (n = 0)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn) (m: Unit number, n: Channel number (mn = 00).

3. In simplified SPI (CSI) communications in the master mode with devices operating at same voltage levels with the internal SCKp clock

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Item	Symbols	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LP (low-power main) mode		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 4/f_{CLK}$	2.7 V ≤ V_{DD} ≤ 5.5 V	125		166		2000		ns
			2.4 V ≤ V_{DD} ≤ 5.5 V	250		250		2000		ns
			1.8 V ≤ V_{DD} ≤ 5.5 V	500		500		2000		ns
			1.6 V ≤ V_{DD} ≤ 5.5 V	1000		1000		2000		ns
SCKp high-level width, low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2 -12		t_{KCY1}/2 -21		t_{KCY1}/2 -50		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2 -18		t_{KCY1}/2 -25		t_{KCY1}/2 -50		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2 -38		t_{KCY1}/2 -38		t_{KCY1}/2 -50		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2 -50		t_{KCY1}/2 -50		t_{KCY1}/2 -50		ns
		1.6 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2 -100		t_{KCY1}/2 -100		t_{KCY1}/2 -100		ns
SIp setup time to the rising of SCKp **Note 1**	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V		44		54		110		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V		44		54		110		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		75		75		110		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V		110		110		110		ns
		1.6 V ≤ V_{DD} ≤ 5.5 V		220		220		220		ns
SIp hold time from the rising of SCKp **Note 1**	t_{KSI1}	1.6 V ≤ V_{DD} ≤ 5.5 V		19		19		19		ns
Delay time from the falling of SCKp to an SOp output **Note 2**	t_{KSO1}	1.6 V ≤ V_{DD} ≤ 5.5 V, C = 30 pF **Note 3**			25		25		25	ns

Note 1. This is for when the settings are DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. When the settings are DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0, this is the setup time to or from the falling of SCKp.

Note 2. This is for when the settings are DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. When the settings are DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0, this is the delay time to the rising of SCKp.

Note 3. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using the port input mode register g (PIMg) and the port output mode register g (POMg).

Remark 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), g: PIM and POM number (g = 0 to 9, 12 to 14), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn) (m: Unit number, n: Channel number = 00 to 03, 10 to 13).

4. In simplified SPI (CSI) communications in the slave mode with devices operating at same voltage levels with the SCKp external clock

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (1/2)

Item	Symbols	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LP (low-power main) mode		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
SCKp cycle time **Note 1**	t_{KCY2}	4.0 V ≤ V_{DD} ≤ 5.5 V	20 MHz < f_{MCK}	8/f_{MCK}		8/f_{MCK}		—		ns
			f_{MCK} ≤ 20 MHz	6/f_{MCK}		6/f_{MCK}		6/f_{MCK}		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V	16 MHz < f_{MCK}	8/f_{MCK}		8/f_{MCK}		—		ns
			f_{MCK} ≤ 16 MHz	6/f_{MCK}		6/f_{MCK}		6/f_{MCK}		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		6/f_{MCK} and 500		6/f_{MCK} and 500		6/f_{MCK} and 500		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V		6/f_{MCK} and 750		6/f_{MCK} and 750		6/f_{MCK} and 750		ns
		1.6 V ≤ V_{DD} ≤ 5.5 V		6/f_{MCK} and 1500		6/f_{MCK} and 1500		6/f_{MCK} and 1500		ns
SCKp high-level width, low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ V_{DD} ≤ 5.5 V		t_{KCY2}/2 -7		t_{KCY2}/2 -7		t_{KCY2}/2 -7		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V		t_{KCY2}/2 -8		t_{KCY2}/2 -8		t_{KCY2}/2 -8		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V		t_{KCY2}/2 -18		t_{KCY2}/2 -18		t_{KCY2}/2 -18		ns
		1.6 V ≤ V_{DD} ≤ 5.5 V		t_{KCY2}/2 -66		t_{KCY2}/2 -66		t_{KCY2}/2 -66		ns

(Notes, Caution, and Remarks are listed on the next page.)

4. In simplified SPI (CSI) communications in the slave mode with devices operating at same voltage levels with the SCKp external clock

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (2/2)

Item	Symbols	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LP (low-power main) mode		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
SIp setup time to the rising of SCKp**Note 2**	t_{SIK2}	2.7 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK} +20		1/f_{MCK} +30		1/f_{MCK} +30		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK} +30		1/f_{MCK} +30		1/f_{MCK} +30		ns
		1.6 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK} +40		1/f_{MCK} +40		1/f_{MCK} +40		ns
SIp hold time from the rising of SCKp **Note 2**	t_{KSI2}	1.8 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK} +31		1/f_{MCK} +31		1/f_{MCK} +31		ns
		1.6 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK} +250		1/f_{MCK} +250		1/f_{MCK} +250		ns
Delay time from the falling of SCKp to an SOp output**Note 3**	t_{KSO2}	C = 30 pF **Note 4**	2.7 V ≤ V_{DD} ≤ 5.5 V		2/f_{MCK} +44		2/f_{MCK} +110		2/f_{MCK} +110	ns
			2.4 V ≤ V_{DD} ≤ 5.5 V		2/f_{MCK} +75		2/f_{MCK} +110		2/f_{MCK} +110	ns
			1.8 V ≤ V_{DD} ≤ 5.5 V		2/f_{MCK} +110		2/f_{MCK} +110		2/f_{MCK} +110	ns
			1.6 V ≤ V_{DD} ≤ 5.5 V		2/f_{MCK} +220		2/f_{MCK} +220		2/f_{MCK} +220	ns

Note 1. Transfer rate in the SNOOZE mode is 1 Mbps at the maximum.

Note 2. This is for when the settings are DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. When the settings are DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0, this is the setup time to or from the falling of SCKp.

Note 3. This is for when the settings are DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. When the settings are DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0, this is the delay time to the rising of SCKp.

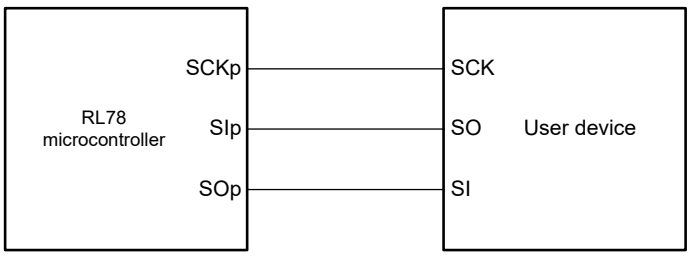
Note 4. C is the load capacitance of the SOp output line.

Caution Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using the port input mode register g (PIMg) and the port output mode register g (POMg).

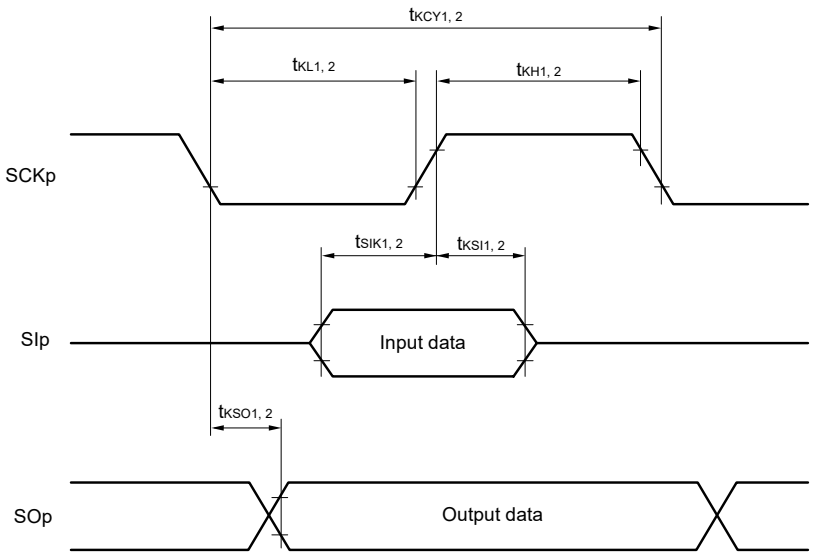
Remark 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), g: PIM and POM number (g = 0 to 9, 12 to 14),
m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn) (m: Unit number, n: Channel number = 00 to 03, 10 to 13).

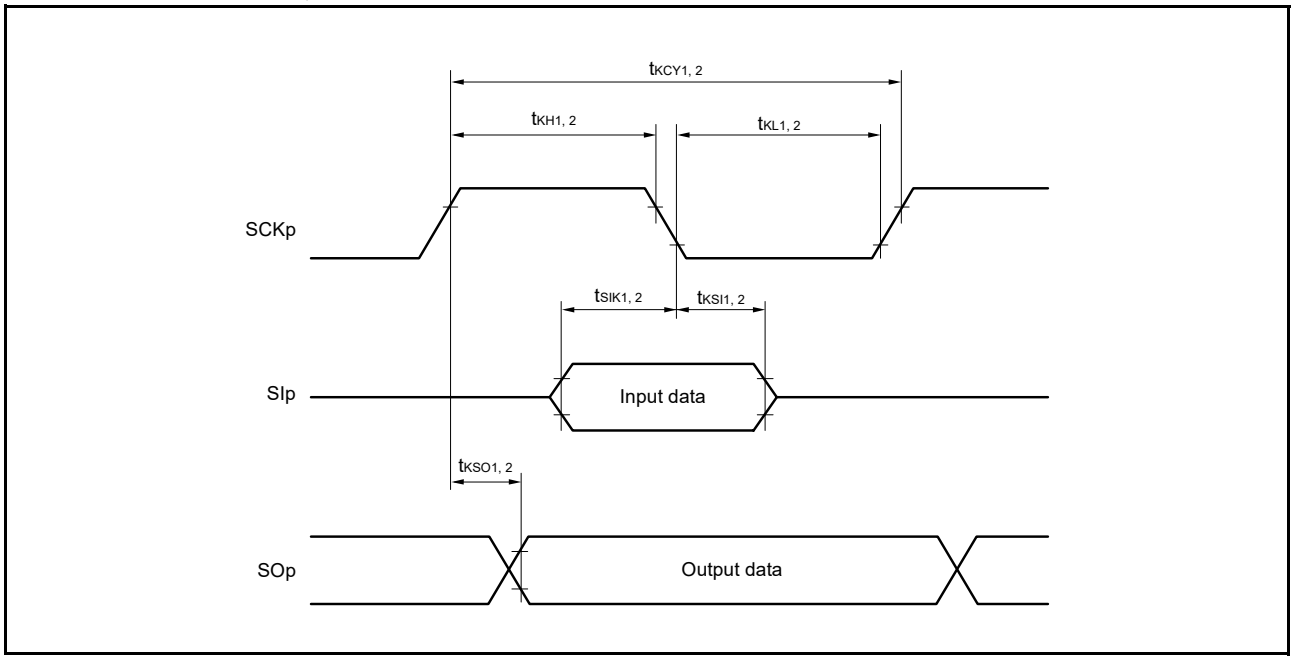
Connection in the simplified SPI (CSI) communications with devices operating at same voltage levels



Timing of serial transfer in the simplified SPI (CSI) communications with devices operating at same voltage levels when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1



Timing of serial transfer in the simplified SPI (CSI) communications with devices operating at same voltage levels when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0



Remark p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

5. In simplified I²C communications with devices operating at same voltage levels

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (1/2)

Item	Symbols	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LP (low-power main) mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
SCLr clock frequency	f_{SCL}	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ		1000 Note 1		1000 Note 1		400 Note 1	kHz
		1.8 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ		400 Note 1		400 Note 1		400 Note 1	kHz
		1.8 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ		300 Note 1		300 Note 1		300 Note 1	kHz
		1.6 V ≤ V_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ		250 Note 1		250 Note 1		250 Note 1	kHz
Hold time when SCLr is low	t_{LOW}	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	475		475		1150		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1150		1150		1150		ns
		1.8 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1550		1550		1550		ns
		1.6 V ≤ V_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	1850		1850		1850		ns
Hold time when SCLr is high	t_{HIGH}	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	475		475		1150		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1150		1150		1150		ns
		1.8 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1550		1550		1550		ns
		1.6 V ≤ V_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	1850		1850		1850		ns

(Notes and Caution are listed on the next page, and Remarks are listed on page 87.)

5. In simplified I²C communications with devices operating at same voltage levels

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (2/2)

Item	Symbols	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LP (low-power main) mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	1/f_{MCK} +85 **Note 2**		1/f_{MCK} +85 **Note 2**		1/f_{MCK} +145 **Note 2**		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1/f_{MCK} +145 **Note 2**		1/f_{MCK} +145 **Note 2**		1/f_{MCK} +145 **Note 2**		ns
		1.8 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1/f_{MCK} +230 **Note 2**		1/f_{MCK} +230 **Note 2**		1/f_{MCK} +230 **Note 2**		ns
		1.6 V ≤ V_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	1/f_{MCK} +290 **Note 2**		1/f_{MCK} +290 **Note 2**		1/f_{MCK} +290 **Note 2**		ns
Data hold time (transmission)	$t_{HD:DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	0	305	0	305	0	305	ns
		1.8 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	0	355	0	355	0	355	ns
		1.8 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	0	405	0	405	0	405	ns
		1.6 V ≤ V_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	0	405	0	405	0	405	ns

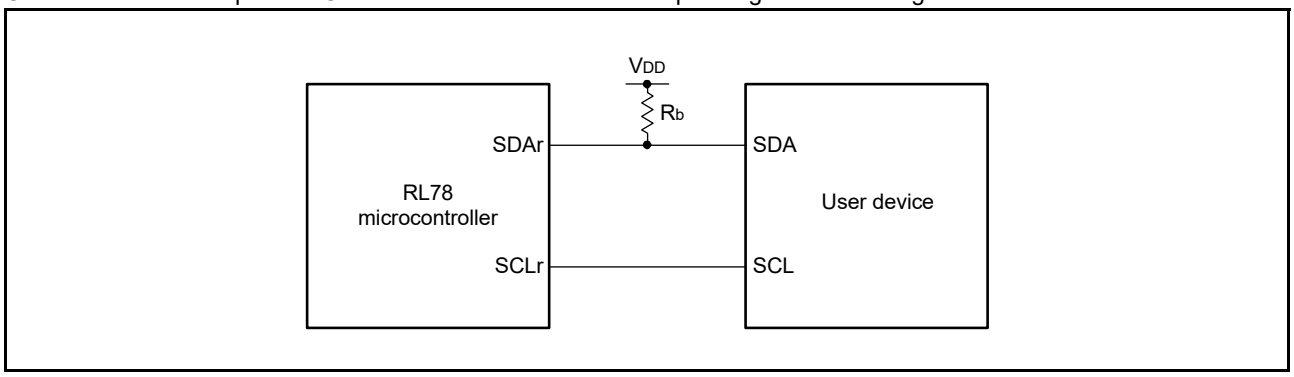
Note 1. The listed times must be no greater than f_{MCK}/4.

Note 2. Set f_{MCK} so that it will not exceed the hold time when SCLr is low or high.

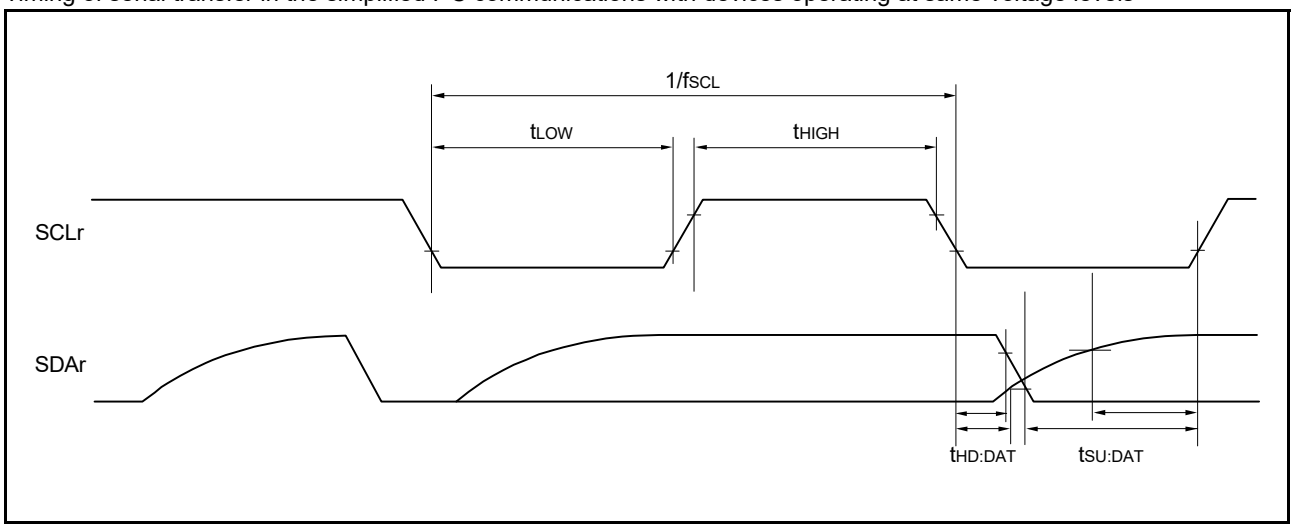
Caution Select the normal input buffer and N-ch open-drain output (withstand voltage of V_{DD}) mode for the SDAr pin, and normal output mode for the SCLr pin by using the port input mode register g (PIMg) and port output mode register h (POMh).

(Remarks are listed on the next page.)

Connection in the simplified I2C communications with devices operating at same voltage levels



Timing of serial transfer in the simplified I2C communications with devices operating at same voltage levels



Remark 1. R_b[Ω]: Communication line (SDAr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance

Remark 2. r: IIC number (r = 00, 01, 10, 11, 20, 21, 30, 31), g: PIM number (g = 0 to 9, 12, 14), h: POM number (h = 0 to 9, 12 to 14)

Remark 3. f_{MCK}: Operation clock frequency of the serial array unit
To set this operating clock, use the CKSmn bit in the SMRmn register (m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13).

6. In UART communications with devices operating at different voltage levels (1.8 V, 2.5 V, 3 V)

(T_A = -40 to +105°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (1/2)

Item	Symbols	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LP (low-power main) mode		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
Transfer rate		Reception	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		f_{MCK}/6 **Note 1**		f_{MCK}/6 **Note 1**		f_{MCK}/6 **Note 1**	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} **Note 2**		5.3		4		0.33	Mbps
			2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		f_{MCK}/6 **Note 1**		f_{MCK}/6 **Note 1**		f_{MCK}/6 **Note 1**	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} **Note 2**		5.3		4		0.33	Mbps
			1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V		f_{MCK}/6 **Notes 1, 3**		f_{MCK}/6 **Notes 1, 3**		f_{MCK}/6 **Notes 1, 3**	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} **Note 2**		5.3		4		0.33	Mbps

Note 1. Transfer rate in the SNOOZE mode is within the range from 4800 to 9600 bps.

Note 2. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:

HS (high-speed main) mode : 32 MHz (1.8 V ≤ V_{DD} ≤ 5.5 V)
4 MHz (1.6 V ≤ V_{DD} ≤ 5.5 V)
LS (low-speed main) mode : 24 MHz (1.8 V ≤ V_{DD} ≤ 5.5 V)
4 MHz (1.6 V ≤ V_{DD} ≤ 5.5 V)
LP (low-power main) mode : 2 MHz (1.6 V ≤ V_{DD} ≤ 5.5 V)

Note 3. Use this rate with EV_{DD0} ≥ V_b.

Caution Select the TTL input buffer for the RxDq pin, and the N-ch open-drain output (withstand voltage of V_{DD}) mode for the TxDq pin by using the port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with the TTL input buffer selected.

Remark 1. V_b[V]: Communication line voltage

Remark 2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0 to 9, 12 to 14)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn) (m: Unit number, n: Channel number = 00 to 03, 10 to 13).

6. In UART communications with devices operating at different voltage levels (1.8 V, 2.5 V, 3 V)

(T_A = -40 to +105°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (2/2)

Item	Symbols	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LP (low-power main) mode		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
Transfer rate		Transmission	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		**Note 1**		**Note 1**		**Note 1**	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 1.4 kΩ, V_b = 2.7 V		2.8 **Note 2**		2.8 **Note 2**		2.8 **Note 2**	Mbps
			2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		**Note 3**		**Note 3**		**Note 3**	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 2.7 kΩ, V_b = 2.3 V		1.2 **Note 4**		1.2 **Note 4**		1.2 **Note 4**	Mbps
			1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V		**Notes 5, 6**		**Notes 5, 6**		**Notes 5, 6**	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 5.5 kΩ, V_b = 1.6 V		0.43 **Note 7**		0.43 **Note 7**		0.43 **Note 7**	Mbps

Note 1. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 4.0 V ≤ V_{DD} ≤ 5.5 V and 2.7 V ≤ Vb ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

Note 2. This rate is calculated as an example when the conditions described in the Conditions column are met. See **Note 1** above to calculate the maximum transfer rate under conditions of the customer.

(Notes and Caution continue in the next page.)

Note 3. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 2.7 V ≤ V_{DD} < 4.0 V and 2.3 V ≤ Vb ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

Note 4. This rate is calculated as an example when the conditions described in the Conditions column are met. See **Note 3** above to calculate the maximum transfer rate under conditions of the customer.

Note 5. Use this rate with $V_{DD} \geq V_b$.

Note 6. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 1.8 V ≤ V_{DD} < 3.3 V and 1.6 V ≤ Vb ≤ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

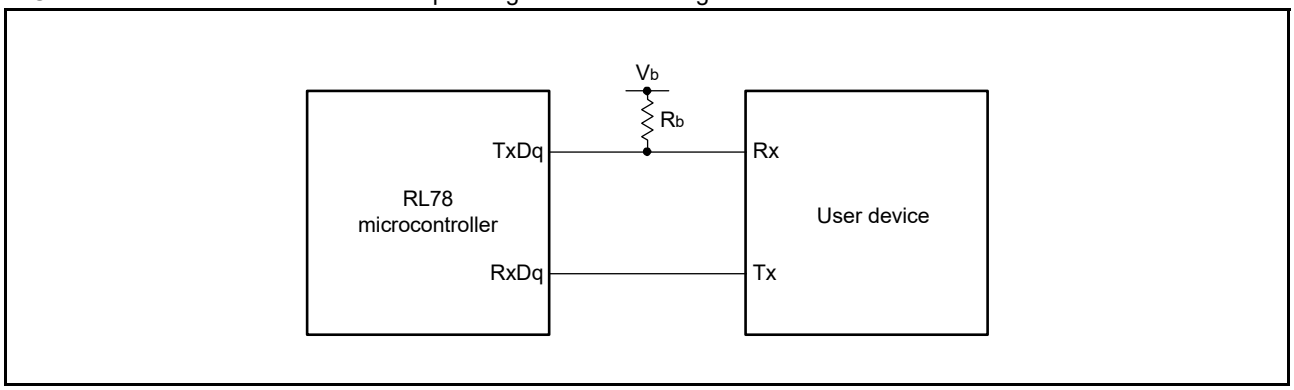
$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

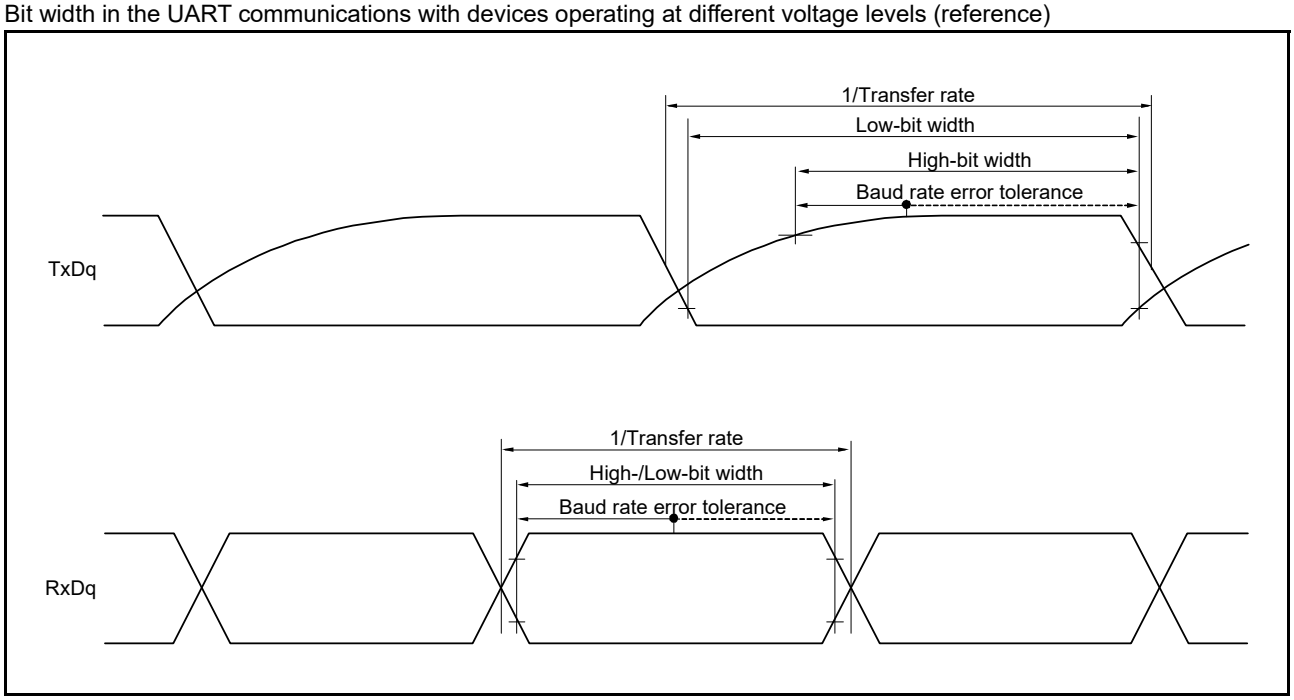
Note 7. This rate is calculated as an example when the conditions described in the Conditions column are met. See **Note 6** above to calculate the maximum transfer rate under conditions of the customer.

Caution Select the TTL input buffer for the RxDq pin, and the N-ch open-drain output (withstand voltage of V_{DD}) mode for the TxDq pin by using the port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with the TTL input buffer selected.

In UART communications with devices operating at different voltage levels



Bit width in the UART communications with devices operating at different voltage levels (reference)



Remark 1. R_b[Ω]: Communication line (TxDq) pull-up resistance, C_b[F]: Communication line (TxDq) load capacitance, V_b[V]: Communication line voltage

Remark 2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0 to 9, 12 to 14)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn) (m: Unit number, n: Channel number = 00 to 03, 10 to 13).

7. In simplified SPI (CSI) communications in the master mode with devices operating at different voltage levels (2.5 V or 3 V) with the internal SCKp clock (the ratings below are only applicable to CSI00)

(T_A = -40 to +105°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (1/2)

Item	Symbols	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LP (low-power main) mode		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
SCKp cycle time	t_{KCY1}	t_{KCY1} ≥ 2/f_{CLK}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ	200		200		2300		ns
			2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ	300		300		2300		ns
SCKp high-level width	t_{KH1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		t_{KCY1}/2 -50		t_{KCY1}/2 -50		t_{KCY1}/2 -50		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		t_{KCY1}/2 -120		t_{KCY1}/2 -120		t_{KCY1}/2 -120		ns
SCKp low-level width	t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		t_{KCY1}/2 -7		t_{KCY1}/2 -7		t_{KCY1}/2 -50		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		t_{KCY1}/2 -10		t_{KCY1}/2 -10		t_{KCY1}/2 -50		ns
SIp setup time to the rising of SCKp **Note 1**	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		58		58		479		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		121		121		479		ns
SIp hold time from the rising of SCKp **Note 1**	t_{KSI1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		10		10		10		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		10		10		10		ns
Delay time from the falling of SCKp to an SOp output **Note 1**	t_{KSO1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ			60		60		60	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ			130		130		130	ns

(Notes, Caution, and Remarks are listed on the next page.)

7. In simplified SPI (CSI) communications in the master mode with devices operating at different voltage levels (2.5 V or 3 V) with the internal SCKp clock (the ratings below are only applicable to CSI00)

(T_A = -40 to +105°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (2/2)

Item	Symbols	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LP (low-power main) mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
SIp setup time to the falling of SCKp**Note 2**	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ	23		23		110		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ	33		33		110		ns
SIp hold time from the falling of SCKp**Note 2**	t_{KSI1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ	10		10		10		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ	10		10		10		ns
Delay time from the rising of SCKp to an SOp output**Note 2**	t_{KSO1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		10		10		10	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		10		10		10	ns

Note 1. This setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

Note 2. This setting applies when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the SIp pin, and the N-ch open-drain output (withstand voltage of V_{DD}) mode for the SOp and SCKp pins by using the port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with the TTL input buffer selected.

Remark 1. R_b[Ω]: Communication line (SCKp, SOp) pull-up resistance, C_b[F]: Communication line (SCKp, SOp) load capacitance, V_b[V]: Communication line voltage

Remark 2. p: CSI number (p = 00), g: PIM and POM number (g = 1), m: Unit number (m = 0), n: Channel number (n = 0)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn) (m: Unit number, n: Channel number = 00).

Remark 4. The listed times are only valid when the peripheral I/O redirect function of CSI00 is not in use.

8. In simplified SPI (CSI) communications in the master mode with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V) with the internal SCKp clock

(T_A = -40 to +105°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (1/3)

Item	Symbols	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LP (low-power main) mode		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
SCKp cycle time	t_{KCY1}	t_{KCY1} ≥ 4/f_{CLK}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	300		300		2300		ns
			2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	500		500		2300		ns
			1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V**Note**, C_b = 30 pF, R_b = 5.5 kΩ	1150		1150		2300		ns
SCKp high-level width	t_{KH1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		t_{KCY1}/2 -75		t_{KCY1}/2 -75		t_{KCY1}/2 -75		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		t_{KCY1}/2 -170		t_{KCY1}/2 -170		t_{KCY1}/2 -170		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V**Note**, C_b = 30 pF, R_b = 5.5 kΩ		t_{KCY1}/2 -458		t_{KCY1}/2 -458		t_{KCY1}/2 -458		ns
SCKp low-level width	t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		t_{KCY1}/2 -12		t_{KCY1}/2 -12		t_{KCY1}/2 -50		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		t_{KCY1}/2 -18		t_{KCY1}/2 -18		t_{KCY1}/2 -50		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V**Note**, C_b = 30 pF, R_b = 5.5 kΩ		t_{KCY1}/2 -50		t_{KCY1}/2 -50		t_{KCY1}/2 -50		ns

Note Use this rate with V_{DD} ≥ V_b.

Caution Select the TTL input buffer for the SIp pin, and the N-ch open-drain output (withstand voltage of V_{DD}) mode for the SOp and SCKp pins by using the port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with the TTL input buffer selected.

(Remarks are listed on page 97.)

8. In simplified SPI (CSI) communications in the master mode with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V) with the internal SCKp clock

(T_A = -40 to +105°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (2/3)

Item	Symbols	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LP (low-power main) mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
SIp setup time to the rising of SCKp**Note 1**	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	81		81		479		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	177		177		479		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V**Note 2**, C_b = 30 pF, R_b = 5.5 kΩ	479		479		479		ns
SIp hold time from the rising of SCKp**Note 1**	t_{KSI1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	19		19		19		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	19		19		19		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V**Note 2**, C_b = 30 pF, R_b = 5.5 kΩ	19		19		19		ns
Delay time from the falling of SCKp to an SOp output**Note 1**	t_{KSO1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		100		100		100	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		195		195		195	ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V**Note 2**, C_b = 30 pF, R_b = 5.5 kΩ		483		483		483	ns

Note 1. This setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

Note 2. Use this value with V_{DD} ≥ V_b.

Caution Select the TTL input buffer for the SIp pin, and the N-ch open-drain output (withstand voltage of V_{DD}) mode for the SOp and SCKp pins by using the port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with the TTL input buffer selected.

(Remarks are listed on page 97.)

8. In simplified SPI (CSI) communications in the master mode with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V) with the internal SCKp clock

(T_A = -40 to +105°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (3/3)

Item	Symbols	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LP (low-power main) mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
SIp setup time to the falling of SCKp**Note 1**	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	44		44		110		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	44		44		110		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V**Note 2**, C_b = 30 pF, R_b = 5.5 kΩ	110		110		110		ns
SIp hold time from the falling of SCKp**Note 1**	t_{KSI1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	19		19		19		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	19		19		19		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V**Note 2**, C_b = 30 pF, R_b = 5.5 kΩ	19		19		19		ns
Delay time from the rising of SCKp to an SOp output**Note 1**	t_{KSO1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		25		25		25	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		25		25		25	ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V**Note 2**, C_b = 30 pF, R_b = 5.5 kΩ		25		25		25	ns

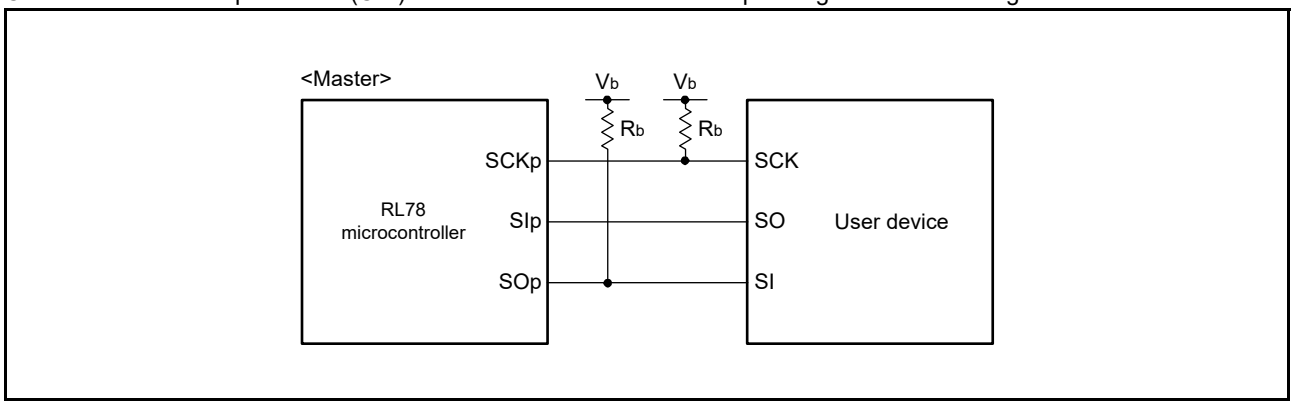
Note 1. This setting applies when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. Use this value with $V_{DD} \geq V_b$.

Caution Select the TTL input buffer for the SIp pin, and the N-ch open-drain output (withstand voltage of V_{DD}) mode for the SOp and SCKp pins by using the port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with the TTL input buffer selected.

(Remarks are listed on the next page.)

Connection in the simplified SPI (CSI) communications with devices operating at different voltage levels

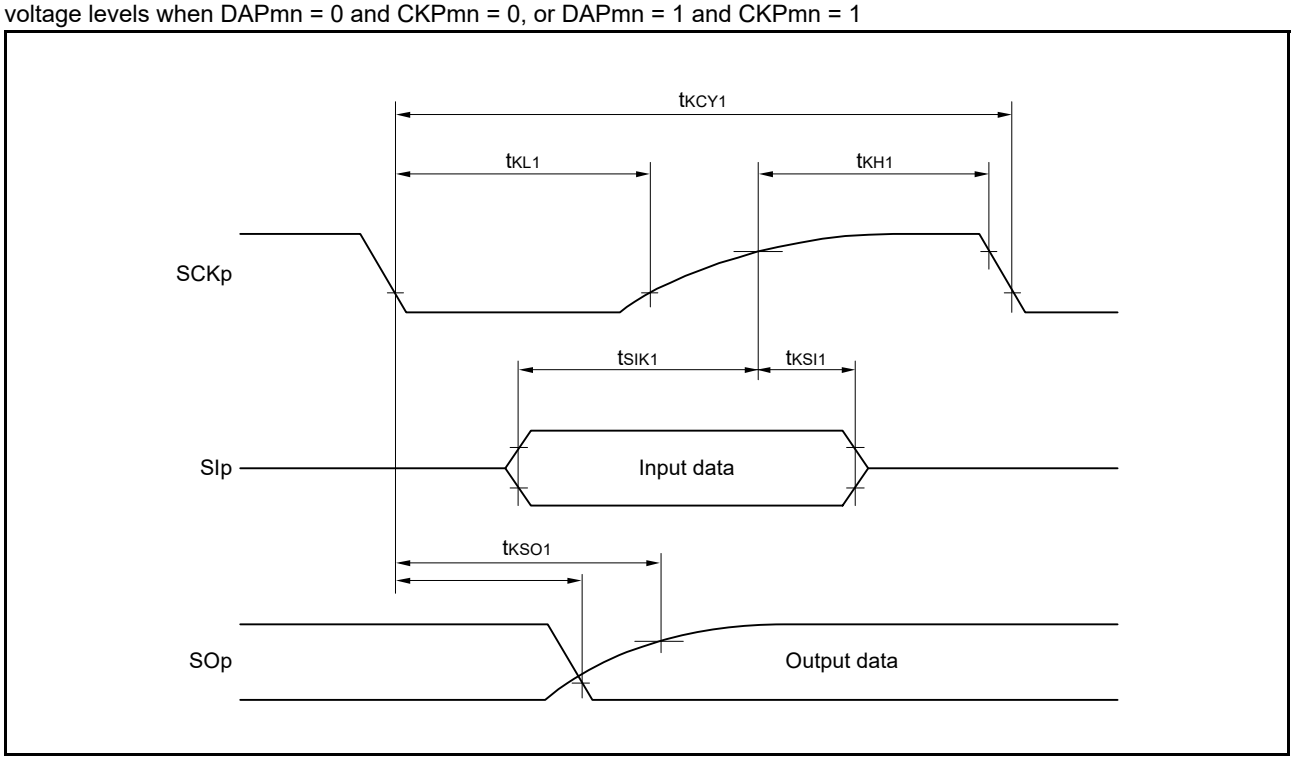


Remark 1. R_b[Ω]: Communication line (SCKp, SOp) pull-up resistance, C_b[F]: Communication line (SCKp, SOp) load capacitance, V_b[V]: Communication line voltage

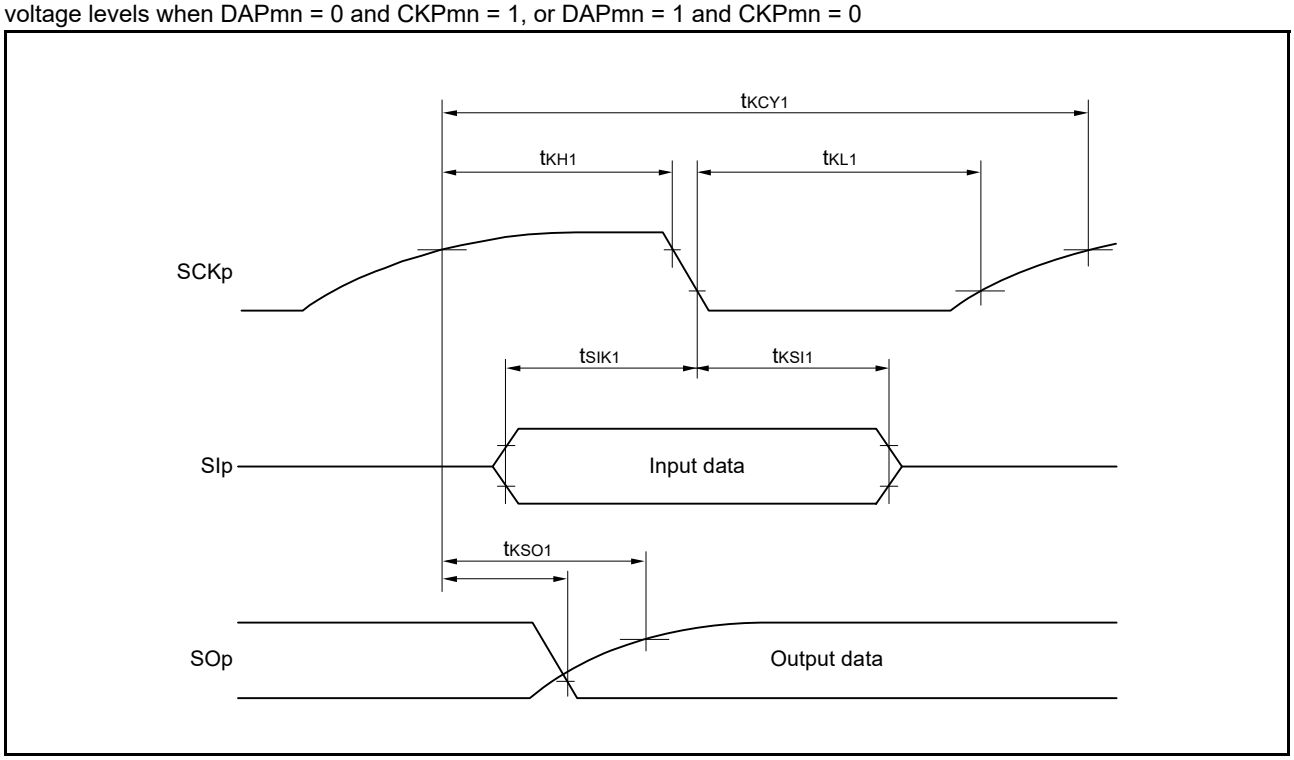
Remark 2. p: CSI number (p = 00, 01, 10, 20, 30, 31), g: PIM and POM number (g = 0 to 9, 12 to 14), m: Unit number, n: Channel number (mn = 00 to 02, 10, 12, 13)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn) (m: Unit number, n: Channel number = 00).

Timing of serial transfer in the simplified SPI (CSI) communications in the master mode with devices operating at different voltage levels when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1



Timing of serial transfer in the simplified SPI (CSI) communications in the master mode with devices operating at different voltage levels when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0



Remark p: CSI number (p = 00, 01, 10, 20, 30, 31), g: PIM and POM number (g = 0 to 9, 12 to 14), m: Unit number, n: Channel number (mn = 00 to 02, 10, 12, 13)

9. In simplified SPI (CSI) communications in the slave mode with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V) with the external SCKp clock

(T_A = -40 to +105°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (1/2)

Item	Symbols	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LP (low-power main) mode		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
SCKp cycle time**Note 1**	t_{KCY2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V	24 MHz < f_{MCK}	14/f_{MCK}		—		—		ns
			20 MHz < f_{MCK} ≤ 24 MHz	12/f_{MCK}		12/f_{MCK}		—		ns
			8 MHz < f_{MCK} ≤ 20 MHz	10/f_{MCK}		10/f_{MCK}		—		ns
			4 MHz < f_{MCK} ≤ 8 MHz	8/f_{MCK}		8/f_{MCK}		—		ns
			f_{MCK} ≤ 4 MHz	6/f_{MCK}		6/f_{MCK}		10/f_{MCK}		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V	24 MHz < f_{MCK}	20/f_{MCK}		—		—		ns
			20 MHz < f_{MCK} ≤ 24 MHz	16/f_{MCK}		16/f_{MCK}		—		ns
			16 MHz < f_{MCK} ≤ 20 MHz	14/f_{MCK}		14/f_{MCK}		—		ns
			8 MHz < f_{MCK} ≤ 16 MHz	12/f_{MCK}		12/f_{MCK}		—		ns
			4 MHz < f_{MCK} ≤ 8 MHz	8/f_{MCK}		8/f_{MCK}		—		ns
			f_{MCK} ≤ 4 MHz	6/f_{MCK}		6/f_{MCK}		10/f_{MCK}		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V **Note 2**	24 MHz < f_{MCK}	48/f_{MCK}		—		—		ns
			20 MHz < f_{MCK} ≤ 24 MHz	36/f_{MCK}		36/f_{MCK}		—		ns
			16 MHz < f_{MCK} ≤ 20 MHz	32/f_{MCK}		32/f_{MCK}		—		ns
			8 MHz < f_{MCK} ≤ 16 MHz	26/f_{MCK}		26/f_{MCK}		—		ns
			4 MHz < f_{MCK} ≤ 8 MHz	16/f_{MCK}		16/f_{MCK}		—		ns
			f_{MCK} ≤ 4 MHz	10/f_{MCK}		10/f_{MCK}		10/f_{MCK}		ns

(Notes and Caution are listed on the next page, and Remarks are listed on page 101.)

9. In simplified SPI (CSI) communications in the slave mode with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V) with the external SCKp clock

(T_A = -40 to +105°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (2/2)

Item	Symbols	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LP (low-power main) mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
SCKp high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V	t_{KCY2}/2 -12		t_{KCY2}/2 -12		t_{KCY2}/2 -50		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V	t_{KCY2}/2 -18		t_{KCY2}/2 -18		t_{KCY2}/2 -50		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V**Note 2**	t_{KCY2}/2 -50		t_{KCY2}/2 -50		t_{KCY2}/2 -50		ns
SIp setup time to the rising of SCKp**Note 3**	t_{SIK2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V	1/f_{MCK} +20		1/f_{MCK} +20		1/f_{MCK} +30		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V	1/f_{MCK} +20		1/f_{MCK} +20		1/f_{MCK} +30		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V**Note 2**	1/f_{MCK} +30		1/f_{MCK} +30		1/f_{MCK} +30		ns
SIp hold time from the rising of SCKp**Note 3**	t_{KSI2}		1/f_{MCK} +31		1/f_{MCK} +31		1/f_{MCK} +31		ns
Delay time from the falling of SCKp to an SOp output**Note 4**	t_{KSO2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		2/f_{MCK} +120		2/f_{MCK} +120		2/f_{MCK} +573	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		2/f_{MCK} +214		2/f_{MCK} +214		2/f_{MCK} +573	ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V**Note 2**, C_b = 30 pF, R_b = 5.5 kΩ		2/f_{MCK} +573		2/f_{MCK} +573		2/f_{MCK} +573	ns

Note 1. Transfer rate in the SNOOZE mode: 1 Mbps (max.)

Note 2. Use this rate with V_{DD} ≥ V_b.

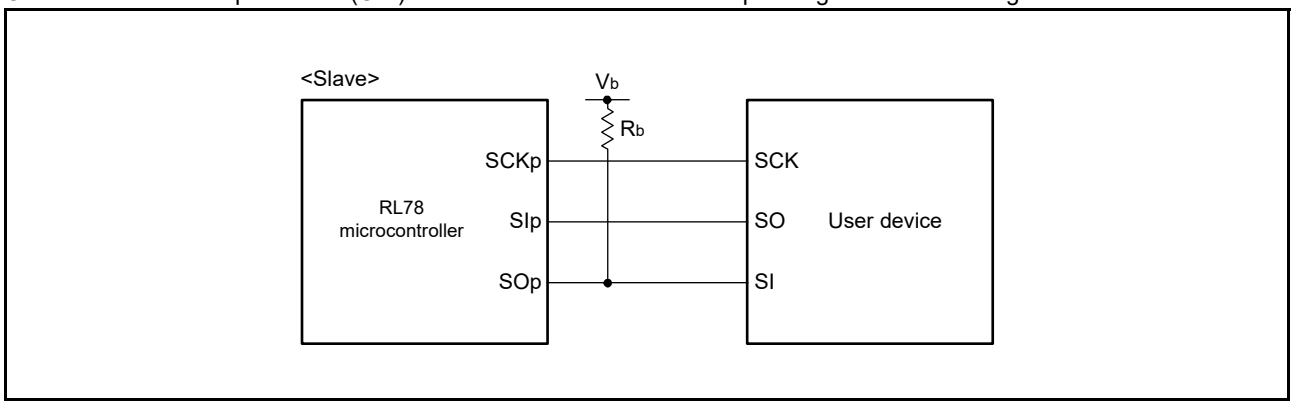
Note 3. This is for when the settings are DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. When the settings are DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0, this is the setup time to or from the falling of SCKp.

Note 4. This is for when the settings are DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. When the settings are DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0, this is the delay time to the rising of SCKp.

Caution Select the TTL input buffer for the SIp and SCKp pins, and the N-ch open-drain output (withstand voltage of V_{DD}) mode for the SOp pin by using the port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with the TTL input buffer selected.

(Remarks are listed on the next page.)

Connection in the simplified SPI (CSI) communications with devices operating at different voltage levels

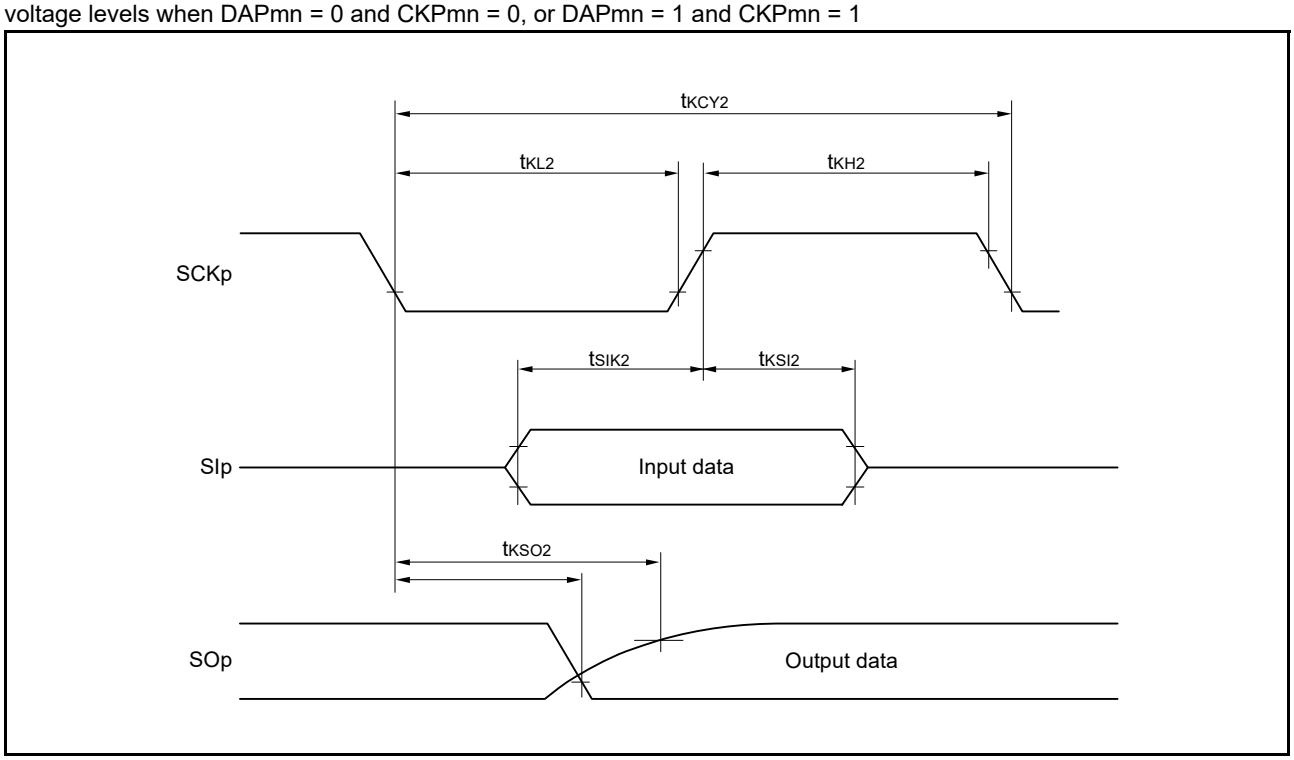


Remark 1. R_b[Ω]: Communication line (SOp) pull-up resistance, C_b[F]: Communication line (SOp) load capacitance, V_b[V]: Communication line voltage

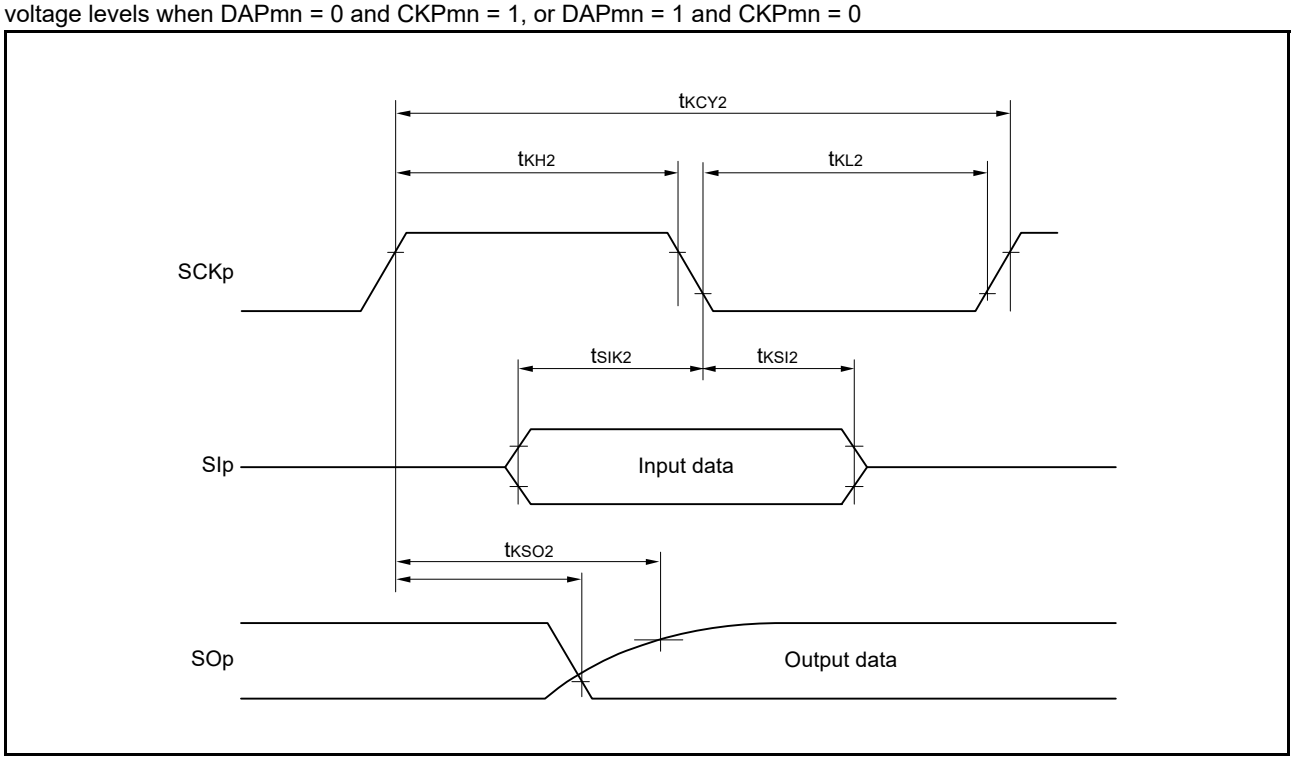
Remark 2. p: CSI number (p = 00, 01, 10, 20, 30, 31), g: PIM and POM number (g = 0 to 9, 12 to 14), m: Unit number, n: Channel number (mn = 00 to 02, 10, 12, 13)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn) (m: Unit number, n: Channel number = 00, 01, 02, 10, 12 and 13).

Timing of serial transfer in the simplified SPI (CSI) communications in the slave mode with devices operating at different voltage levels when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1



Timing of serial transfer in the simplified SPI (CSI) communications in the slave mode with devices operating at different voltage levels when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0



Remark p: CSI number (p = 00, 01, 10, 20, 30, 31), g: PIM and POM number (g = 0 to 9, 12 to 14), m: Unit number, n: Channel number (mn = 00 to 02, 10, 12, 13)

10. Simplified I²C communications with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V)

(T_A = -40 to +105°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (1/2)

Item	Symbols	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LP (low-power main) mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
SCLr clock frequency	f_{SCL}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ		1000 Note 1		1000 Note 1		300 Note 1	kHz
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ		1000 Note 1		1000 Note 1		300 Note 1	kHz
		4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ		400 Note 1		400 Note 1		300 Note 1	kHz
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ		400 Note 1		400 Note 1		300 Note 1	kHz
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 100 pF, R_b = 5.5 kΩ		300 Note 1		300 Note 1		300 Note 1	kHz
Hold time when SCLr is low	t_{LOW}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	475		475		1550		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	475		475		1550		ns
		4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	1150		1550		1550		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	1150		1550		1550		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 100 pF, R_b = 5.5 kΩ	1550		1550		1550		ns
Hold time when SCLr is high	t_{HIGH}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	245		245		610		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	200		200		610		ns
		4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	675		675		610		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	600		600		610		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 100 pF, R_b = 5.5 kΩ	610		610		610		ns

10. Simplified I²C communications with devices operating at different voltage levels (1.8 V, 2.5 V, and 3 V)

(T_A = -40 to +105°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (2/2)

Item	Symbols	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LP (low-power main) mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Data setup time (reception)	$t_{SU:DAT}$	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	1/f_{MCK} +135 **Note 3**		1/f_{MCK} +135 **Note 3**		1/f_{MCK} +190 **Note 3**		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	1/f_{MCK} +135 **Note 3**		1/f_{MCK} +135 **Note 3**		1/f_{MCK} +190 **Note 3**		ns
		4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	1/f_{MCK} +190 **Note 3**		1/f_{MCK} +190 **Note 3**		1/f_{MCK} +190 **Note 3**		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	1/f_{MCK} +190 **Note 3**		1/f_{MCK} +190 **Note 3**		1/f_{MCK} +190 **Note 3**		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V **Note 2**, C_b = 100 pF, R_b = 5.5 kΩ	1/f_{MCK} +190 **Note 3**		1/f_{MCK} +190 **Note 3**		1/f_{MCK} +190 **Note 3**		ns
Data hold time (transmission)	$t_{HD:DAT}$	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	0	305	0	305	0	305	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	0	305	0	305	0	305	ns
		4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	0	355	0	355	0	355	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	0	355	0	355	0	355	ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V **Note 2**, C_b = 100 pF, R_b = 5.5 kΩ	0	405	0	405	0	405	ns

Note 1. The listed times must be no greater than f_{MCK}/4.

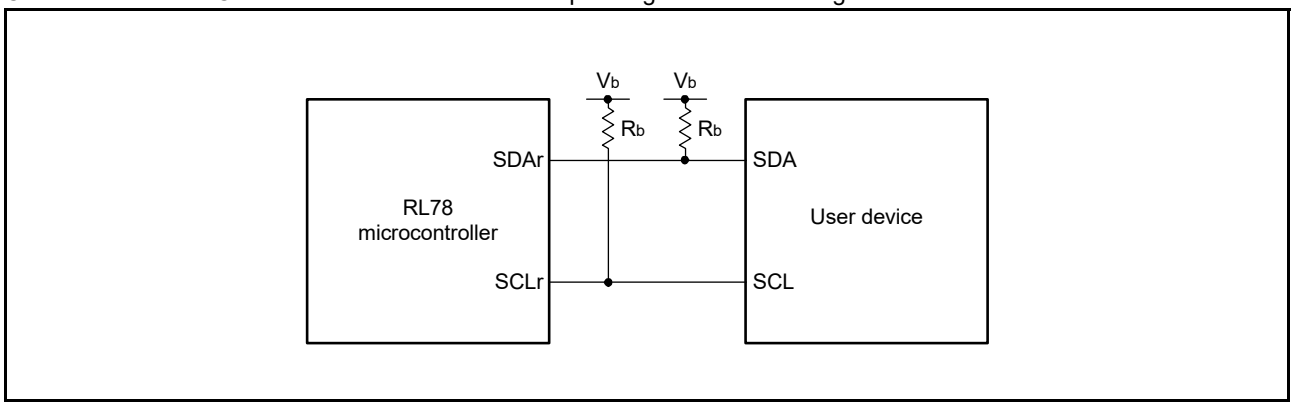
Note 2. Use this rate with V_{DD} ≥ V_b.

Note 3. Set f_{MCK} so that it will not exceed the hold time when SCLr is low or high.

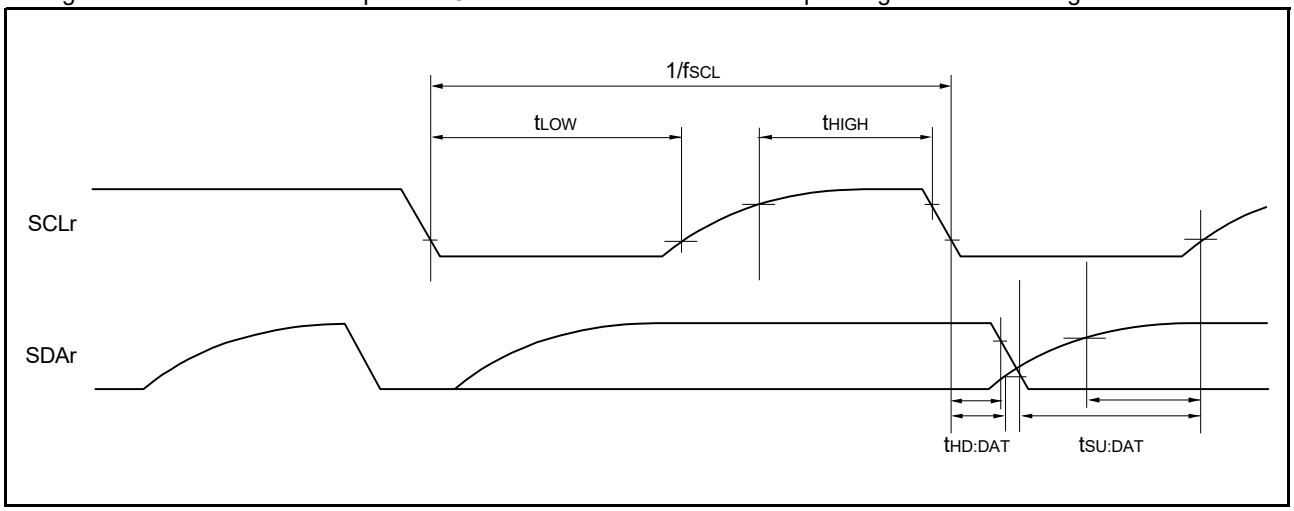
Caution Select the TTL input buffer and N-ch open-drain output (withstand voltage of V_{DD}) mode for the SDAr pin, and the N-ch open-drain output (withstand voltage of V_{DD}) mode for the SCLr pin by using the port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

Connection in the I2C communications with devices operating at different voltage levels



Timing of serial transfer in the simplified I2C communications with devices operating at different voltage levels



Remark 1. R_b[Ω]: Communication line (SDAr, SCLr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance, V_b[V]: Communication line voltage

Remark 2. r: IIC number (r = 00, 01, 10, 20, 30, 31), g: PIM and POM number (g = 0 to 9, 12 to 14)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
To set this operating clock, use the CKSmn bit in the SMRmn register (m: Unit number, n: Channel number (mn = 00 to 02, 10, 12, 13).

2.5.2 Serial interface UARTA

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Item	Symbols	Conditions	Min.	Typ.	Max.	Unit
Transfer rate			200	0	153600	bps

Caution Select the normal input buffer for the RxDAq pin, and the normal output mode for the TxDAq pin by using the port input mode register g (PIMg) and port output mode register h (POMh).

Remark 1. g: PIM number (g = 1, 2, 4, 5, 8, 14), h: POM number (h= 0 to 2, 4 to 6, 8, 13, 14)
Remark 2. q = 0 to 3

2.5.3 Serial interface IICA

1. I^2C standard mode

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Item	Symbols	Conditions	Min.	Typ.	Max.	Unit
SCLA0 clock frequency	f_{SCL}	Standard mode: f_{CLK} ≥ 1 MHz	0		100	kHz
Setup time of restart condition	$t_{SU:STA}$		4.7			μs
Hold time[Note 1]	$t_{HD:STA}$		4.0			μs
Hold time when SCLA0 is low	t_{LOW}		4.7			μs
Hold time when SCLA0 is high	t_{HIGH}		4.0			μs
Data setup time (reception)	$t_{SU:DAT}$		250			ns
Data hold time (transmission)[Note 2]	$t_{HD:DAT}$		0		3.45	μs
Setup time of stop condition	$t_{SU:STO}$		4.0			μs
Bus-free time	t_{BUF}		4.7			μs

Note 1. The first clock pulse is generated after this period when the start or restart condition is detected.

Note 2. The maximum value of $t_{HD:DAT}$ applies to normal transfer. The clock stretching will be inserted on reception of an acknowledgment (ACK) signal.

Remark 1. The maximum value of communication line capacitance (C_b) and communication line pull-up resistor (R_b) are as follows.
C_b = 400 pF, R_b = 2.7 kΩ

Remark 2. n = 0, 1

2. I^2C fast mode

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Item	Symbols	Conditions	Min.	Typ.	Max.	Unit
SCLAn clock frequency	f_{SCL}	Fast mode: f_{CLK} ≥ 3.5 MHz 1.8 V ≤ V_{DD} ≤ 5.5 V	0		400	kHz
Setup time of restart condition	$t_{SU:STA}$	1.8 V ≤ V_{DD} ≤ 5.5 V	0.6			µs
Hold time**Note 1**	$t_{HD:STA}$	1.8 V ≤ V_{DD} ≤ 5.5 V	0.6			µs
Hold time when SCLAn is low	t_{LOW}	1.8 V ≤ V_{DD} ≤ 5.5 V	1.3			µs
Hold time when SCLAn is high	t_{HIGH}	1.8 V ≤ V_{DD} ≤ 5.5 V	0.6			µs
Data setup time (reception)	$t_{SU:DAT}$	1.8 V ≤ V_{DD} ≤ 5.5 V	100			ns
Data hold time (transmission)**Note 2**	$t_{HD:DAT}$	1.8 V ≤ V_{DD} ≤ 5.5 V	0		0.9	µs
Setup time of stop condition	$t_{SU:STO}$	1.8 V ≤ V_{DD} ≤ 5.5 V	0.6			µs
Bus-free time	t_{BUF}	1.8 V ≤ V_{DD} ≤ 5.5 V	1.3			µs

Note 1. The first clock pulse is generated after this period when the start or restart condition is detected.

Note 2. The maximum value of $t_{HD:DAT}$ applies to normal transfer. The clock stretching will be inserted on reception of an acknowledgment (ACK) signal.

Remark 1. The maximum value of communication line capacitance (C_b) and communication line pull-up resistor (R_b) are as follows.
C_b = 320 pF, R_b = 1.1 kΩ

Remark 2. n = 0, 1

3. I^2C fast mode plus

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Item	Symbols	Conditions	Min.	Typ.	Max.	Unit
SCLAn clock frequency	f_{SCL}	Fast mode plus: f_{CLK} ≥ 10 MHz 2.7 V ≤ V_{DD} ≤ 5.5 V	0		1000	kHz
Setup time of restart condition	$t_{SU:STA}$	2.7 V ≤ V_{DD} ≤ 5.5 V	0.26			µs
Hold time[Note 1]	$t_{HD:STA}$	2.7 V ≤ V_{DD} ≤ 5.5 V	0.26			µs
Hold time when SCLAn is low	t_{LOW}	2.7 V ≤ V_{DD} ≤ 5.5 V	0.5			µs
Hold time when SCLAn is high	t_{HIGH}	2.7 V ≤ V_{DD} ≤ 5.5 V	0.26			µs
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V	50			ns
Data hold time (transmission)[Note 2]	$t_{HD:DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V	0		0.45	µs
Setup time of stop condition	$t_{SU:STO}$	2.7 V ≤ V_{DD} ≤ 5.5 V	0.26			µs
Bus-free time	t_{BUF}	2.7 V ≤ V_{DD} ≤ 5.5 V	0.5			µs

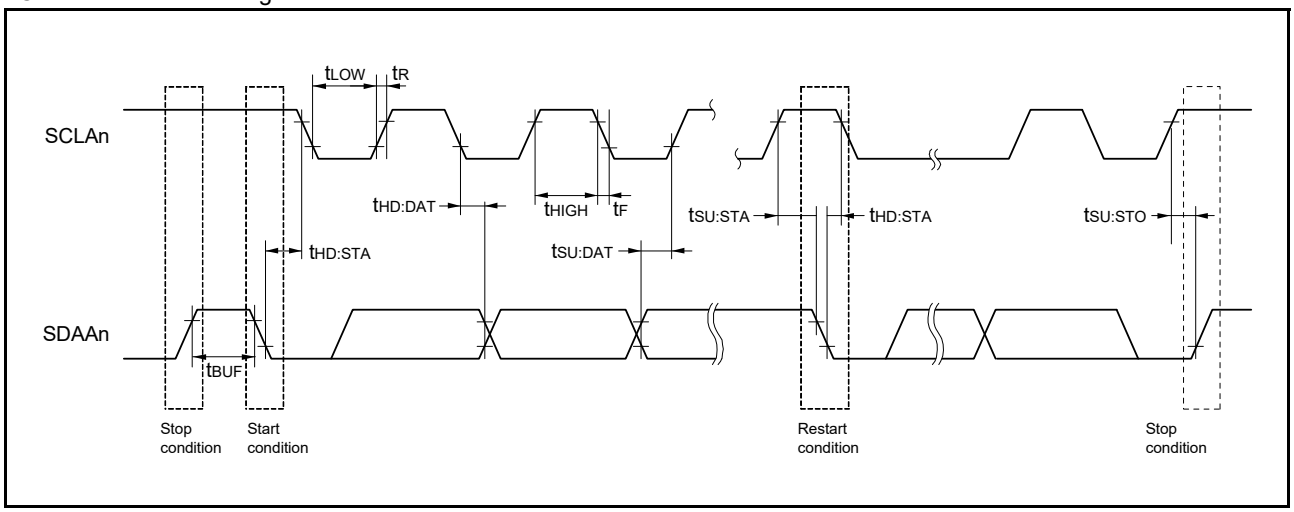
Note 1. The first clock pulse is generated after this period when the start or restart condition is detected.

Note 2. The maximum value of $t_{HD:DAT}$ applies to normal transfer. The clock stretching will be inserted on reception of an acknowledgment (ACK) signal.

Remark 1. The maximum value of communication line capacitance (C_b) and communication line pull-up resistor (R_b) are as follows.
C_b = 120 pF, R_b = 1.1 kΩ

Remark 2. n = 0, 1

IICA serial transfer timing



Remark n = 0, 1

2.6 Analog Characteristics

2.6.1 A/D converter characteristics

1. Normal modes 1 and 2

(T_A = -40 to +105°C, 2.4 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V,
reference voltage (+) = AV_{REFP} (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AV_{REFM} (ADREFM = 1),
target pins: ANI16 to ANI26)

Item	Symbols	Conditions	Min.	Typ.	Max.	Unit
Resolution	RES				12	bit
Conversion clock	f_{AD}		1		32	MHz
Overall error Notes 1, 2, 3, 4, 5	AINL	4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±1.8	±4.1	LSB
		2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±2.1	±4.2	LSB
		2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±2.4	±4.7	LSB
Conversion time Notes 5, 6	t_{CONV}	4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V	2.0			µs
		2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V	2.0			µs
		2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V	2.0			µs
Zero-scale error Notes 1, 2, 3, 4, 5, 7	E_{ZS}	4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±0.01	±0.06	%FSR
		2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±0.02	±0.09	%FSR
		2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±0.03	±0.11	%FSR
Full-scale error Notes 1, 2, 3, 4, 5, 7	E_{FS}	4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±0.02	±0.09	%FSR
		2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±0.03	±0.11	%FSR
		2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±0.03	±0.11	%FSR
Analog input voltage	V_{AIN}		0		AV_{REFP}	V

Note 1. This value does not include the quantization error (±1/2 LSB).

Note 2. The values in the column Max. only apply in the case of a normal distribution with ±3σ variation from the mean.

Note 3. We do not inspect the characteristics of the A/D converter before shipment. The listed values are only results of evaluation.

Note 4. When AV_{REFP} < V_{DD}, the maximum values are as follows.

Overall error/zero-scale error/full-scale error: Add (±0.75 LSB × (V_{DD} voltage (V) - AV_{REFP} voltage (V)) to the maximum value.

Integral linearity error: Add (±0.2 LSB × (V_{DD} voltage (V) - AV_{REFP} voltage (V)) to the maximum value.

Note 5. The listed values apply when the conversion resolution is set to 12 bits.

Note 6. When the internal reference voltage or the temperature sensor output voltage is selected as the target for conversion, the sampling time must be at least 5 µs. Accordingly, use standard mode 2 with the longer sampling time.

Note 7. This value is indicated as a ratio (%FSR) to the full-scale value.

(T_A = -40 to +105°C, 2.4 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V,
reference voltage (+) = AV_{REFP} (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AV_{REFM} (ADREFM = 1),
target pins: internal reference voltage and temperature sensor output voltage)

Item	Symbols	Conditions		Min.	Typ.	Max.	Unit
Resolution	RES			8		12	bit
Conversion clock	f_{AD}			1		32	MHz
Overall error Notes 1, 2, 3, 4	AINL	12-bit resolution	4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±7.5	LSB
			2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±9.0	LSB
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±9.0	LSB
Conversion time Note 5	t_{CONV}	12-bit resolution	4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V	2.0			µs
			2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V	2.0			µs
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V	2.0			µs
Zero-scale error Notes 1, 2, 3, 4, 6	E_{ZS}	12-bit resolution	4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.17	%FSR
			2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.21	%FSR
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.21	%FSR
Full-scale error Notes 1, 2, 3, 4, 6	E_{FS}	12-bit resolution	4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.17	%FSR
			2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.21	%FSR
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.21	%FSR
Integral linearity error Notes 1, 3, 4	ILE	12-bit resolution	4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±3.0	LSB
			2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±3.0	LSB
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±3.0	LSB
Differential linearity error Note 1	DLE	12-bit resolution	4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±1.0		LSB
			2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±1.0		LSB
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±1.0		LSB
Analog input voltage	V_{AIN}			0		AV_{REFP}	V

Note 1. This value does not include the quantization error (±1/2 LSB).

Note 2. When pins ANI16 to ANI26 are selected as the target pins for conversion or the TSCAP voltage of the CTSU is to be A/D converted, the maximum values are as follows.
Overall error: Add ±3 LSB to the maximum value.
Zero-scale/full-scale error: Add ±0.04%FSR to the maximum value.

Note 3. When reference voltage (+) = V_{DD} and reference voltage (-) = V_{SS}, the maximum values are as follows.
Overall error: Add ±10 LSB to the maximum value.
Zero-scale/full-scale error: Add ±0.25%FSR to the maximum value.
Integral linearity error: Add ±4 LSB to the maximum value.

Note 4. When AV_{REFP} < V_{DD}, the maximum values are as follows.
Overall error/zero-scale error/full-scale error: Add (±0.75 LSB × (V_{DD} voltage (V) - AV_{REFP} voltage (V)) to the maximum value.
Integral linearity error: Add (±0.2 LSB × (V_{DD} voltage (V) - AV_{REFP} voltage (V)) to the maximum value.

Note 5. When the internal reference voltage or the temperature sensor output voltage is selected as the target for conversion, the sampling time must be at least 5 µs. Accordingly, use standard mode 2 with the longer sampling time.

Note 6. This value is indicated as a ratio (%FSR) to the full-scale value.

2. Low-voltage modes 1 and 2

(T_A = -40 to +105°C, 1.6 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V,
reference voltage (+) = AV_{REFP} (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AV_{REFM} (ADREFM = 1),
target pins: internal reference voltage[Note 1] and temperature sensor output voltage[Note 1])

Item	Symbols	Conditions		Min.	Typ.	Max.	Unit
Resolution	RES			8		12	bit
Conversion clock	f_{AD}			1		24	MHz
Overall error[Notes 2, 3, 4, 5]	AINL	12-bit resolution	2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±9	LSB
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±9	LSB
			1.8 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±11.5	LSB
			1.6 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±12.0	LSB
Conversion time[Note 6]	t_{CONV}	12-bit resolution	2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V	3.33			µs
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V	5.0			µs
			1.8 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V	10.0			µs
			1.6 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V	20.0			µs
Zero-scale error[Notes 2, 3, 4, 5, 7]	E_{ZS}	12-bit resolution	2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.21	%FSR
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.21	%FSR
			1.8 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.27	%FSR
			1.6 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.28	%FSR
Full-scale error[Notes 2, 3, 4, 5, 7]	E_{FS}	12-bit resolution	2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.21	%FSR
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.21	%FSR
			1.8 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.27	%FSR
			1.6 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.28	%FSR
Integral linearity error[Notes 2, 4, 5]	ILE	12-bit resolution	2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±4.0	LSB
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±4.0	LSB
			1.8 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±4.5	LSB
			1.6 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±4.5	LSB
Differential linearity error[Note 2]	DLE	12-bit resolution	2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±1.5		LSB
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±1.5		LSB
			1.8 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±2.0		LSB
			1.6 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±2.0		LSB
Analog input voltage	V_{AIN}			0		AV_{REFP}	V

Note 1. If the internal reference voltage, temperature sensor output voltage, or TSCAP voltage of the CTSU is to be A/D converted, V_{DD} must be at least 1.8 V.

Note 2. This value does not include the quantization error (±1/2 LSB).

Note 3. When pins ANI16 to ANI26 are selected as the target pins for conversion or the TSCAP voltage of the CTSU is to be A/D converted, the maximum values are as follows. If the CTSU TSCAP voltage is to be A/D converted, V_{DD} must be at least 1.8 V.
Overall error: Add ±3 LSB to the maximum value.
Zero-scale/full-scale error: Add ±0.04%FSR to the maximum value.

Note 4. When reference voltage (+) = V_{DD} and reference voltage (-) = V_{SS}, the maximum values are as follows.
Overall error: Add ±10 LSB to the maximum value.
Zero-scale/full-scale error: Add ±0.25%FSR to the maximum value.
Integral linearity error: Add ±4 LSB to the maximum value.

Note 5. When AV_{REFP} < V_{DD}, the maximum values are as follows.
Overall error/zero-scale error/full-scale error: Add (±0.75 LSB × (V_{DD} voltage (V) - AV_{REFP} voltage (V)) to the maximum value.
Integral linearity error: Add (±0.2 LSB × (V_{DD} voltage (V) - AV_{REFP} voltage (V)) to the maximum value.

Note 6. When the internal reference voltage or the temperature sensor output voltage is selected as the target for conversion, the sampling time must be at least 5 μs. Accordingly, use standard mode 2 with the longer sampling time, and use the conversion clock (f_{AD}) of no more than 16 MHz.

Note 7. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When the internal reference voltage is selected as reference voltage (+)

(T_A = -40 to +105°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, low-voltage modes 1 and 2,
reference voltage (+) = internal reference voltage (ADREFP1 = 1, ADREFP0 = 0),
reference voltage (-) = AV_{REFM} (ADREFM = 1)

Item	Symbols	Conditions	Min.	Typ.	Max.	Unit
Resolution	RES		8			bit
Conversion clock	f_{AD}	1.8 V ≤ V_{DD} ≤ 5.5 V	1		2	MHz
Zero-scale error**Notes 1, 2, 3**	E_{ZS}	1.8 V ≤ V_{DD} ≤ 5.5 V			±0.6	%FSR
Integral linearity error**Notes 1, 3**	ILE	1.8 V ≤ V_{DD} ≤ 5.5 V			±2.0	LSB
Differential linearity error**Note 1**	DLE	1.8 V ≤ V_{DD} ≤ 5.5 V		±1.0		LSB
Analog input voltage	V_{AIN}		0		V_{BGR} **Note 4**	V

Note 1. This value does not include the quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. When reference voltage (-) is selected as V_{SS}, the maximum values are as follows.
Zero-scale error: Add ±0.35%FSR to the maximum value.
Integral linearity error: Add ±0.5 LSB to the maximum value.

Note 4. See **2.6.2 Temperature sensor/internal reference voltage characteristics**.

2.6.2 Temperature sensor/internal reference voltage characteristics

(T_A = -40 to +105°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Item	Symbols	Conditions	Min.	Typ.	Max.	Unit
Temperature sensor output voltage	V_{TMPS25}	Setting ADS register = 80H, T_A = +25°C		1.05		V
Internal reference voltage	V_{BGR}	Setting ADS register = 81H	1.42	1.48	1.54	V
Temperature coefficient	F_{VTMPS}	Temperature dependency of the temperature sensor voltage		-3.3		mV/°C
Operation stabilization wait time	t_{AMP}		5			μs

2.6.3 D/A converter characteristics

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Item	Symbols	Conditions		Min.	Typ.	Max.	Unit
Resolution	RES					8	bit
Overall error	AINL	Rload = 8 MΩ	1.8 V ≤ V_{DD} ≤ 5.5 V			±2.5	LSB
		Rload = 4 MΩ	1.8 V ≤ V_{DD} ≤ 5.5 V			±2.5	LSB
Settling time	t_{SET}	Cload = 20 pF	2.7 V ≤ V_{DD} ≤ 5.5 V			3	μs
			1.6 V ≤ V_{DD} ≤ 5.5 V			6	μs

2.6.4 Comparator characteristics

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Item	Symbols	Conditions		Min.	Typ.	Max.	Unit
Input voltage range	I_{VREF}	Input to the IVREF0 and IVREF1 pins C0LVL = 0, C1LVL = 0		0		V_{DD} -1.4	V
		Input to the IVREF0 and IVREF1 pins C0LVL = 1, C1LVL = 1		1.4		V_{DD}	V
	I_{VCMP}	Input to the IVCMP0 and IVCMP1 pins		-0.3		V_{DD} +0.3	V
Output delay	td	V_{DD} = 3.0 V, Input slew rate > 1 V/μs	High-speed mode			1.5	μs
			Low-speed mode		3.0		μs
Offset voltage	V_{IOCMP}	High-speed mode				50	mV
		Low-speed mode				40	mV
Operation stabilization wait time	t_{CMP}			30			μs
Internal reference voltage[Note]	V_{BGR2}	Internal reference voltage		1.4		1.6	V
	V_{DA2}	D/A converter 2 output + comparator offset voltage	1.8 V ≤ V_{DD} ≤ 5.5 V			V_{DD} × (DACS2)/ 256 + V_{IOCMP}	V
D/A converter 2 settling time	t_{SET2}	When changing the DACS2 settings	2.7 V ≤ V_{DD} ≤ 5.5			3	μs
			1.6 V ≤ V_{DD} ≤ 5.5 V			6	μs

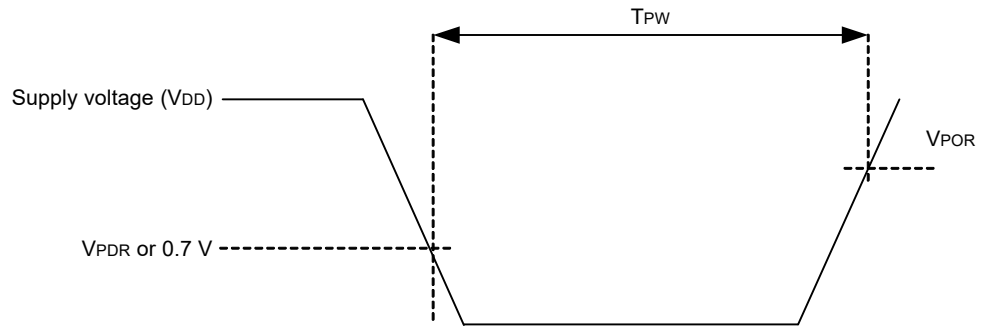
Note The internal reference voltage can be selected as comparator reference voltage only when 1.8 V ≤ V_{DD} ≤ 5.5 V.

2.6.5 POR circuit characteristics

(T_A = -40 to +105°C, V_{SS} = 0 V)

Item	Symbols	Conditions	Min.	Typ.	Max.	Unit
Detection voltage	V_{POR}, V_{PDR}		1.43	1.50	1.57	V
Minimum pulse width[Note]	T_{PW}		300			μs

Note This width is the minimum time required for a POR reset when V_{DD} falls below V_{PDR}. This width is also the minimum time required for a POR reset from when V_{DD} falls below 0.7 V to when V_{DD} exceeds V_{POR} in the STOP mode or while the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



2.6.6 LVD circuit characteristics

1. LVD0 Detection Voltage in the Reset Mode and Interrupt Mode

(T_A = -40 to +105°C, $V_{PDR} \leq V_{DD} \leq 5.5$ V, V_{SS} = 0 V)

Item		Symbols	Conditions	Min.	Typ.	Max.	Unit
Detection voltage	Supply voltage level	V_{LVD00}	The power supply voltage is rising.	3.84	3.96	4.08	V
			The power supply voltage is falling.	3.76	3.88	4.00	V
		V_{LVD01}	The power supply voltage is rising.	2.88	2.97	3.06	V
			The power supply voltage is falling.	2.82	2.91	3.00	V
		V_{LVD02}	The power supply voltage is rising.	2.59	2.67	2.75	V
			The power supply voltage is falling.	2.54	2.62	2.70	V
		V_{LVD03}	The power supply voltage is rising.	2.31	2.38	2.45	V
			The power supply voltage is falling.	2.26	2.33	2.40	V
		V_{LVD04}	The power supply voltage is rising.	1.84	1.90	1.95	V
			The power supply voltage is falling.	1.80	1.86	1.91	V
		V_{LVD05}	The power supply voltage is rising.	1.64	1.69	1.74	V
			The power supply voltage is falling.	1.60	1.65	1.70	V
Minimum pulse width		t_{LW}		500			µs
Detection delay time						500	µs

2. LVD1 Detection Voltage of Reset Mode and Interrupt Mode

(T_A = -40 to +105°C, $V_{PDR} \leq V_{DD} \leq 5.5$ V, V_{SS} = 0 V)

Item		Symbols	Conditions	Min.	Typ.	Max.	Unit
Detection voltage	Supply voltage level	V_{LVD10}	The power supply voltage is rising.	4.08	4.16	4.24	V
			The power supply voltage is falling.	4.00	4.08	4.16	V
		V_{LVD11}	The power supply voltage is rising.	3.88	3.96	4.04	V
			The power supply voltage is falling.	3.80	3.88	3.96	V
		V_{LVD12}	The power supply voltage is rising.	3.68	3.75	3.82	V
			The power supply voltage is falling.	3.60	3.67	3.74	V
		V_{LVD13}	The power supply voltage is rising.	3.48	3.55	3.62	V
			The power supply voltage is falling.	3.40	3.47	3.54	V
		V_{LVD14}	The power supply voltage is rising.	3.28	3.35	3.42	V
			The power supply voltage is falling.	3.20	3.27	3.34	V
		V_{LVD15}	The power supply voltage is rising.	3.07	3.13	3.19	V
			The power supply voltage is falling.	3.00	3.06	3.12	V
		V_{LVD16}	The power supply voltage is rising.	2.91	2.97	3.03	V
			The power supply voltage is falling.	2.85	2.91	2.97	V
		V_{LVD17}	The power supply voltage is rising.	2.76	2.82	2.87	V
			The power supply voltage is falling.	2.70	2.76	2.81	V
		V_{LVD18}	The power supply voltage is rising.	2.61	2.66	2.71	V
			The power supply voltage is falling.	2.55	2.60	2.65	V
		V_{LVD19}	The power supply voltage is rising.	2.45	2.50	2.55	V
			The power supply voltage is falling.	2.40	2.45	2.50	V
		V_{LVD110}	The power supply voltage is rising.	2.35	2.40	2.45	V
			The power supply voltage is falling.	2.30	2.35	2.40	V
		V_{LVD111}	The power supply voltage is rising.	2.25	2.30	2.34	V
			The power supply voltage is falling.	2.20	2.25	2.29	V
		V_{LVD112}	The power supply voltage is rising.	2.15	2.20	2.24	V
			The power supply voltage is falling.	2.10	2.15	2.19	V
		V_{LVD113}	The power supply voltage is rising.	2.05	2.09	2.13	V
			The power supply voltage is falling.	2.00	2.04	2.08	V
		V_{LVD114}	The power supply voltage is rising.	1.94	1.98	2.02	V
			The power supply voltage is falling.	1.90	1.94	1.98	V
		V_{LVD115}	The power supply voltage is rising.	1.84	1.88	1.91	V
			The power supply voltage is falling.	1.80	1.84	1.87	V
		V_{LVD116}	The power supply voltage is rising.	1.74	1.78	1.81	V
			The power supply voltage is falling.	1.70	1.74	1.77	V
		V_{LVD117}	The power supply voltage is rising.	1.64	1.67	1.70	V
			The power supply voltage is falling.	1.60	1.63	1.66	V
Minimum pulse width		t_{LW}		500			µs
Detection delay time						500	µs

2.6.7 Power supply voltage rising slope characteristics

(T_A = -40 to +105°C, V_{SS} = 0 V)

Item	Symbols	Conditions	Min.	Typ.	Max.	Unit
Power supply voltage rising slope	SV_{DD}				54	V/ms

Caution Make sure to keep the internal reset state by the LVD0 circuit or an external reset until V_{DD} reaches the operating voltage range shown in AC characteristics.

2.6.8 LCD characteristics

2.6.8.1 External resistance division method

1. Static display mode

(T_A = -40 to +105°C, V_{L4} (Min.) ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Item	Symbols	Conditions	Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L4}		2.0		V_{DD}	V

2. 1/2 bias method, 1/4 bias method

(T_A = -40 to +105°C, V_{L4} (Min.) ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Item	Symbols	Conditions	Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L4}		2.7		V_{DD}	V

3. 1/3 bias method

(T_A = -40 to +105°C, V_{L4} (Min.) ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Item	Symbols	Conditions	Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L4}		2.5		V_{DD}	V

2.6.8.2 Internal voltage boosting method

1. 1/3 bias method, V_{L1} reference (MDSET2 to MDSET0 = 001B, LBAS1 to LBAS0 = 01B)

(T_A = -40 to +105°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Item	Symbols	Conditions		Min.	Typ.	Max.	Unit
V_{L1} output voltage	V_{L1}	C1 to C4**Note 1** = 0.47 μF	V_{LCD4-0} = 04H	0.97	1.01	1.04	V
			V_{LCD4-0} = 05H	1.00	1.04	1.08	V
			V_{LCD4-0} = 06H	1.04	1.07	1.11	V
			V_{LCD4-0} = 07H	1.07	1.11	1.14	V
			V_{LCD4-0} = 08H	1.10	1.14	1.18	V
			V_{LCD4-0} = 09H	1.13	1.17	1.21	V
			V_{LCD4-0} = 0AH	1.16	1.21	1.25	V
			V_{LCD4-0} = 0BH	1.20	1.24	1.28	V
			V_{LCD4-0} = 0CH	1.23	1.27	1.32	V
			V_{LCD4-0} = 0DH	1.26	1.31	1.35	V
			V_{LCD4-0} = 0EH	1.29	1.34	1.38	V
			V_{LCD4-0} = 0FH	1.33	1.37	1.42	V
			V_{LCD4-0} = 10H	1.36	1.40	1.45	V
			V_{LCD4-0} = 11H	1.39	1.44	1.49	V
			V_{LCD4-0} = 12H	1.42	1.47	1.52	V
			V_{LCD4-0} = 13H	1.45	1.50	1.55	V
			V_{LCD4-0} = 14H	1.49	1.54	1.59	V
			V_{LCD4-0} = 15H	1.52	1.57	1.62	V
			V_{LCD4-0} = 16H	1.55	1.60	1.66	V
			V_{LCD4-0} = 17H	1.58	1.64	1.69	V
			V_{LCD4-0} = 18H	1.61	1.67	1.73	V
			V_{LCD4-0} = 19H	1.65	1.70	1.76	V
			V_{LCD4-0} = 1AH	1.68	1.74	1.79	V
V_{L2} output voltage	V_{L2}	C1 to C4**Note 1** = 0.47 μF		$2V_{L1}$ -5%	$2V_{L1}$	$2V_{L1}$	V
V_{L4} output voltage	V_{L4}	C1 to C4**Note 1** = 0.47 μF		$3V_{L1}$ -6%	$3V_{L1}$	$3V_{L1}$	V
Reference voltage setup time **Note 2**	t_{VWAIT1}			10			ms
Voltage boost wait time**Note 3**	t_{VWAIT2}	C1 to C4**Note 1** = 0.47 μF		500			ms

Note 1. C1 to C4 are the capacitors that are to be connected to the LCD drive voltage pins of the MCU.
C1 is to be connected between CAPH and CAPL.
C2 is to be connected between V_{L1} and GND.
C3 is to be connected between V_{L2} and GND.
C4 is to be connected between V_{L4} and GND.
C1 = C2 = C3 = C4 = 0.47 μF ±30%

Note 2. This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected (MDSET2 to MDSET0 = 001B) if the default reference voltage is used) until voltage boosting starts (VLCON = 1).

Note 3. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

2. 1/3 bias method, V_{L2} reference (MDSET2 to MDSET0 = 101B, LBAS1 to LBAS0 = 01B)

(T_A = -40 to +105°C, V_{L2} (Max.) + 0.1 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Item	Symbols	Conditions		Min.	Typ.	Max.	Unit
V_{L1} output voltage	V_{L1}	C1 to C4**Note 1** = 0.47 μF		1/2V_{L2} -5%	1/2V_{L2}	1/2V_{L2}	V
V_{L2} output voltage	V_{L2}	C1 to C4**Note 1** = 0.47 μF	V_{LCD4-0} = 04H	1.94	2.02	2.11	V
			V_{LCD4-0} = 05H	2.00	2.09	2.18	V
			V_{LCD4-0} = 06H	2.07	2.16	2.25	V
			V_{LCD4-0} = 07H	2.13	2.22	2.32	V
			V_{LCD4-0} = 08H	2.19	2.29	2.39	V
			V_{LCD4-0} = 09H	2.26	2.36	2.46	V
			V_{LCD4-0} = 0AH	2.32	2.42	2.53	V
			V_{LCD4-0} = 0BH	2.39	2.49	2.59	V
			V_{LCD4-0} = 0CH	2.45	2.56	2.66	V
			V_{LCD4-0} = 0DH	2.51	2.62	2.73	V
			V_{LCD4-0} = 0EH	2.58	2.69	2.80	V
			V_{LCD4-0} = 0FH	2.64	2.76	2.87	V
			V_{LCD4-0} = 10H	2.70	2.82	2.94	V
			V_{LCD4-0} = 11H	2.77	2.89	3.01	V
			V_{LCD4-0} = 12H	2.83	2.96	3.08	V
			V_{LCD4-0} = 13H	2.90	3.02	3.15	V
			V_{LCD4-0} = 14H	2.96	3.09	3.22	V
			V_{LCD4-0} = 15H	3.02	3.15	3.29	V
			V_{LCD4-0} = 16H	3.09	3.22	3.35	V
			V_{LCD4-0} = 17H	3.15	3.29	3.42	V
			V_{LCD4-0} = 18H	3.21	3.35	3.49	V
			V_{LCD4-0} = 19H	3.28	3.42	3.56	V
			V_{LCD4-0} = 1AH	3.34	3.49	3.63	V
V_{L4} output voltage	V_{L4}	C1 to C4**Note 1** = 0.47 μF		3/2V_{L2} -6%	3/2V_{L2}	3/2V_{L2}	V
Reference voltage setup time **Note 2**	t_{VWAIT1}			10			ms
Voltage boost wait time**Note 3**	t_{VWAIT2}	C1 to C4**Note 1** = 0.47 μF		500			ms

Note 1. C1 to C4 are the capacitors that are to be connected to the LCD drive voltage pins of the MCU.
C1 is to be connected between CAPH and CAPL.
C2 is to be connected between V_{L1} and GND.
C3 is to be connected between V_{L2} and GND.
C4 is to be connected between V_{L4} and GND.
C1 = C2 = C3 = C4 = 0.47 μF ±30%

Note 2. This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected (MDSET2 to MDSET0 = 101B) if the default reference voltage is used) until voltage boosting starts (VLCON = 1).

Note 3. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

3. 1/4 bias method, V_{L1} reference (MDSET2 to MDSET0 = 001B, LBAS1 to LBAS0 = 10B)

(T_A = -40 to +105°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Item	Symbols	Conditions		Min.	Typ.	Max.	Unit
V_{L1} output voltage	V_{L1}	C1 to C5[Note 1] = 0.47 μF	V_{LCD4-0} = 04H	0.97	1.01	1.04	V
			V_{LCD4-0} = 05H	1.00	1.04	1.08	V
			V_{LCD4-0} = 06H	1.04	1.07	1.11	V
			V_{LCD4-0} = 07H	1.07	1.11	1.14	V
			V_{LCD4-0} = 08H	1.10	1.14	1.18	V
			V_{LCD4-0} = 09H	1.13	1.17	1.21	V
			V_{LCD4-0} = 0AH	1.16	1.21	1.25	V
			V_{LCD4-0} = 0BH	1.20	1.24	1.28	V
			V_{LCD4-0} = 0CH	1.23	1.27	1.32	V
			V_{LCD4-0} = 0DH	1.26	1.31	1.35	V
V_{L2} output voltage	V_{L2}	C1 to C5[Note 1] = 0.47 μF		2V_{L1} -5%	2V_{L1}	2V_{L1}	V
V_{L3} output voltage	V_{L3}	C1 to C5[Note 1] = 0.47 μF		3V_{L1} -6%	3V_{L1}	3V_{L1}	V
V_{L4} output voltage	V_{L4}	C1 to C5[Note 1] = 0.47 μF		4V_{L1} -6%	4V_{L1}	4V_{L1}	V
Reference voltage setup time Note 2	t_{VWAIT1}			10			ms
Voltage boost wait time[Note 3]	t_{VWAIT2}	C1 to C5[Note 1] = 0.47 μF		500			ms

Note 1. C1 to C5 are the capacitors that are to be connected to the LCD drive voltage pins of the MCU.
C1 is to be connected between CAPH and CAPL.
C2 is to be connected between V_{L1} and GND.
C3 is to be connected between V_{L2} and GND.
C4 is to be connected between V_{L3} and GND.
C5 is to be connected between V_{L4} and GND.
C1 = C2 = C3 = C4 = C5 = 0.47 μF ±30%

Note 2. This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected (MDSET2 to MDSET0 = 001B) if the default reference voltage is used) until voltage boosting starts (VLCON = 1).

Note 3. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

2.6.8.3 Capacitor split method

1. 1/3 bias method, V_{DD} reference (MDSET2 to MDSET0 = 010B, LBAS1 to LBAS0 = 01B)

(T_A = -40 to +105°C, 2.2 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Item	Symbols	Conditions	Min.	Typ.	Max.	Unit
V_{L4} output voltage	V_{L4}	C1 to C4 = 0.47 μF Note 1		V_{DD}		V
V_{L2} output voltage	V_{L2}	C1 to C4 = 0.47 μF Note 1	2/3V_{L4} -3%	2/3V_{L4}	2/3V_{L4} +3%	V
V_{L1} output voltage	V_{L1}	C1 to C4 = 0.47 μF Note 1	1/3V_{L4} -3%	1/3V_{L4}	1/3V_{L4} +3%	V
Capacitor split wait time Note 2	t_{VWAIT}		100			ms

Note 1. C1 to C4 are the capacitors that are to be connected to the LCD drive voltage pins of the MCU.
C1 is to be connected between CAPH and CAPL.
C2 is to be connected between V_{L1} and GND.
C3 is to be connected between V_{L2} and GND.
C4 is to be connected between V_{L4} and GND. This is required when the voltage generation method is switched to the internal voltage boosting method.
C1 = C2 = C3 = C4 = 0.47 μF ±30%

Note 2. This is the wait time from when voltage bucking is started (VLCON = 1) until display is enabled (LCDON = 1).

2. 1/3 bias method, VL4 reference (MDSET2 to MDSET0 = 110B, LBAS1 to LBAS0 = 01B)

(T_A = -40 to +105°C, 3.2 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Item	Symbols	Conditions	Min.	Typ.	Max.	Unit
V_{L4} output voltage	V_{L4}	C1 to C4 = 0.47 μF Note 1	2.89	3.04	3.20	V
V_{L2} output voltage	V_{L2}	C1 to C4 = 0.47 μF Note 1	1.89	2.03	2.17	V
V_{L1} output voltage	V_{L1}	C1 to C4 = 0.47 μF Note 1	0.94	1.01	1.08	V
Reference voltage setup time Note 2	t_{VWAIT1}		10			ms
Capacitor split wait time Note 3	t_{VWAIT}		100			ms

Note 1. C1 to C4 are the capacitors that are to be connected to the LCD drive voltage pins of the MCU.
C1 is to be connected between CAPH and CAPL.
C2 is to be connected between V_{L1} and GND.
C3 is to be connected between V_{L2} and GND.
C4 is to be connected between V_{L4} and GND.
C1 = C2 = C3 = C4 = 0.47 μF ±30%

Note 2. The time required to wait from when the capacitor split method is selected (MDSET2 to MDSET0 = 110B) until voltage bucking starts (VLCON = 1).

Note 3. This is the wait time from when voltage bucking is started (VLCON = 1) until display is enabled (LCDON = 1).

3. 1/4 bias method, VDD reference (MDSET2 to MDSET0 = 010B, LBAS1 to LBAS0 = 10B)

(T_A = -40 to +105°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Item	Symbols	Conditions	Min.	Typ.	Max.	Unit
V_{L4} output voltage	V_{L4}	C1 to C5 = 0.47 μF Note 1		V_{DD}		V
V_{L3} output voltage	V_{L3}	C1 to C5 = 0.47 μF Note 1	3/4V_{L4} -3%	3/4V_{L4}	3/4V_{L4} +3%	V
V_{L2} output voltage	V_{L2}	C1 to C5 = 0.47 μF Note 1	1/2V_{L4} -3%	1/2V_{L4}	1/2V_{L4} +3%	V
V_{L1} output voltage	V_{L1}	C1 to C5 = 0.47 μF Note 1	1/4V_{L4} -3%	1/4V_{L4}	1/4V_{L4} +3%	V
Capacitor split wait time Note 2	t_{VWAIT}		100			ms

Note 1. C1 to C5 are the capacitors that are to be connected to the LCD drive voltage pins of the MCU.
C1 is to be connected between CAPH and CAPL.
C2 is to be connected between V_{L1} and GND.
C3 is to be connected between V_{L2} and GND.
C4 is to be connected between V_{L3} and GND. This is required when the voltage generation method is switched to the internal voltage boosting method.
C5 is to be connected between V_{L4} and GND.
C1 = C2 = C3 = C4 = C5 = 0.47 μF ±30%

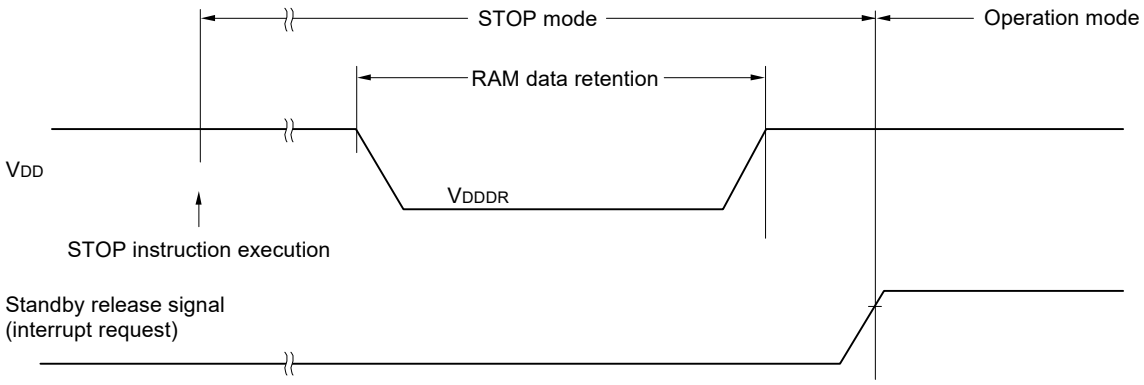
Note 2. This is the wait time from when voltage bucking is started (VLCON = 1) until display is enabled (LCDON = 1).

2.7 RAM Data Retention Characteristics

(T_A = -40 to +105°C, V_{SS} = 0V)

Item	Symbols	Conditions	Min.	Typ.	Max.	Unit
Data retention supply voltage	V_{DDDR}		1.43[Note]		5.5	V

Note This voltage depends on the POR detection voltage. When the voltage drops, the data in RAM are retained until a POR is applied, but are not retained following a POR.



2.8 Flash Memory Programming Characteristics

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Item	Symbols	Conditions	Min.	Typ.	Max.	Unit
CPU/peripheral hardware clock frequency	f_{CLK}		1		32	MHz
Number of code flash rewrites[Notes 1, 2, 3]	C_{erwr}	Retained for 10 years T_A = +85°C[Note 4]	10,000			Times
		Retained for 20 years T_A = +85°C[Note 4]	1,000			
Number of data flash rewrites[Notes 1, 2, 3]		Retained for 1 year T_A = +25°C		1,000,000		
		Retained for 5 years T_A = +85°C[Note 4]	100,000			
		Retained for 20 years T_A = +85°C[Note 4]	10,000			

Note 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

Note 2. The listed numbers of times apply when the flash memory programmer or self-programming function is in use.

Note 3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

Note 4. This temperature is the average value at which data are retained.

1. Code flash memory

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Item		Symbols	f_{CLK} = 1 MHz			f_{CLK} = 2 MHz, 3 MHz			4 MHz ≤ f_{CLK} < 8 MHz			8 MHz ≤ f_{CLK} < 32 MHz			f_{CLK} = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	4 bytes	t_{P4}	—	74.7	656.5	—	51.0	464.6	—	41.7	384.8	—	37.1	346.2	—	34.2	321.9	µs
Erasure time	2 Kbytes	t_{E2K}	—	10.4	312.2	—	7.7	258.5	—	6.4	231.8	—	5.8	218.4	—	5.6	214.4	ms
Blank checking time	4 bytes	t_{BC4}	—	—	38.4	—	—	19.2	—	—	13.1	—	—	10.2	—	—	8.3	µs
	2 Kbytes	t_{BC2K}	—	—	2618.9	—	—	1309.5	—	—	658.3	—	—	332.8	—	—	234.1	µs
Time taken to forcibly stop the erasure		t_{SED}	—	—	18.0	—	—	14.0	—	—	12.0	—	—	11.0	—	—	10.3	µs
Security setting time		t_{AWSSAS}	—	18.2	526.2	—	14.4	469.2	—	12.5	441.1	—	11.6	427.1	—	11.3	422.6	ms
Time until programming starts following cancellation of the STOP instruction		—	20	—	—	20	—	—	20	—	—	20	—	—	20	—	—	µs

Caution The listed values do not include the time until the operations of the flash memory start following execution of an instruction by software.

2. Data flash memory

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Item		Symbols	f_{CLK} = 1 MHz			f_{CLK} = 2 MHz, 3 MHz			4 MHz ≤ f_{CLK} < 8 MHz			8 MHz ≤ f_{CLK} < 32 MHz			f_{CLK} = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	1 byte	t_{P4}	—	74.7	656.5	—	51.0	464.6	—	41.7	384.8	—	37.1	346.2	—	34.2	321.9	µs
Erasure time	256 bytes	t_{E2K}	—	7.8	259.2	—	6.4	232.0	—	5.8	218.5	—	5.5	211.8	—	5.4	209.7	ms
Blank checking time	1 byte	t_{BC4}	—	—	38.4	—	—	19.2	—	—	13.1	—	—	10.2	—	—	8.3	µs
	256 bytes	t_{BC2K}	—	—	1326.1	—	—	663.1	—	—	335.1	—	—	171.2	—	—	121.0	µs
Time taken to forcibly stop the erasure		t_{SED}	—	—	18.0	—	—	14.0	—	—	12.0	—	—	11.0	—	—	10.3	µs
Time until programming starts following cancellation of the STOP instruction		—	20	—	—	20	—	—	20	—	—	20	—	—	20	—	—	µs
Time until reading starts following setting DFLEN to 1		—	0.25	—	—	0.25	—	—	0.25	—	—	0.25	—	—	0.25	—	—	µs

Caution The listed values do not include the time until the operations of the flash memory start following execution of an instruction by software.

2.9 Dedicated Flash Memory Programmer Communication (UART)

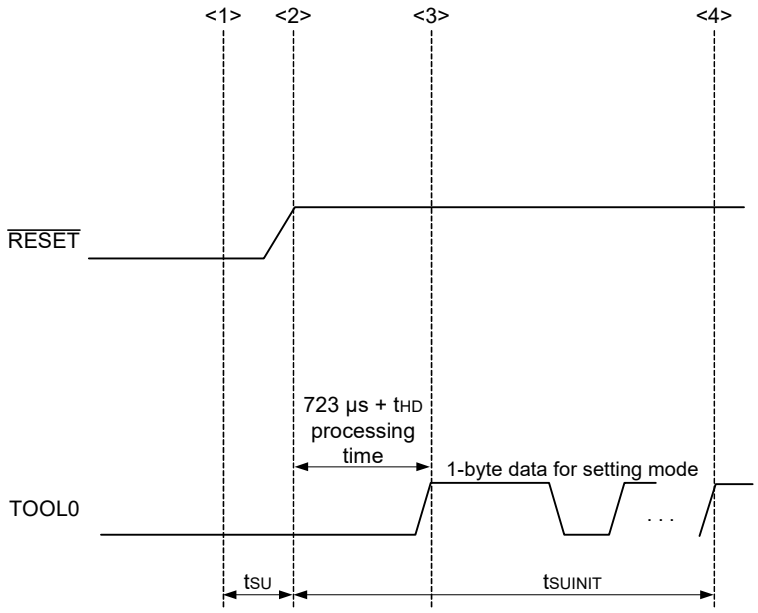
(T_A = -40 to +105°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Item	Symbols	Conditions	Min.	Typ.	Max.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

2.10 Timing of Entry to Flash Memory Programming Modes

(T_A = -40 to +105°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Item	Symbols	Conditions	Min.	Typ.	Max.	Unit
Time to complete the communication for the initial setting after the external reset is released	t_{SUINIT}	POR and LVD reset must be released before the external reset is released.			100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	t_{SU}	POR and LVD reset must be released before the external reset is released.	10			μs
Time to hold the TOOL0 pin at the low level after the external reset is released (the processing time of the firmware to control the flash memory is not included)	t_{HD}	POR and LVD reset must be released before the external reset is released.	1			ms



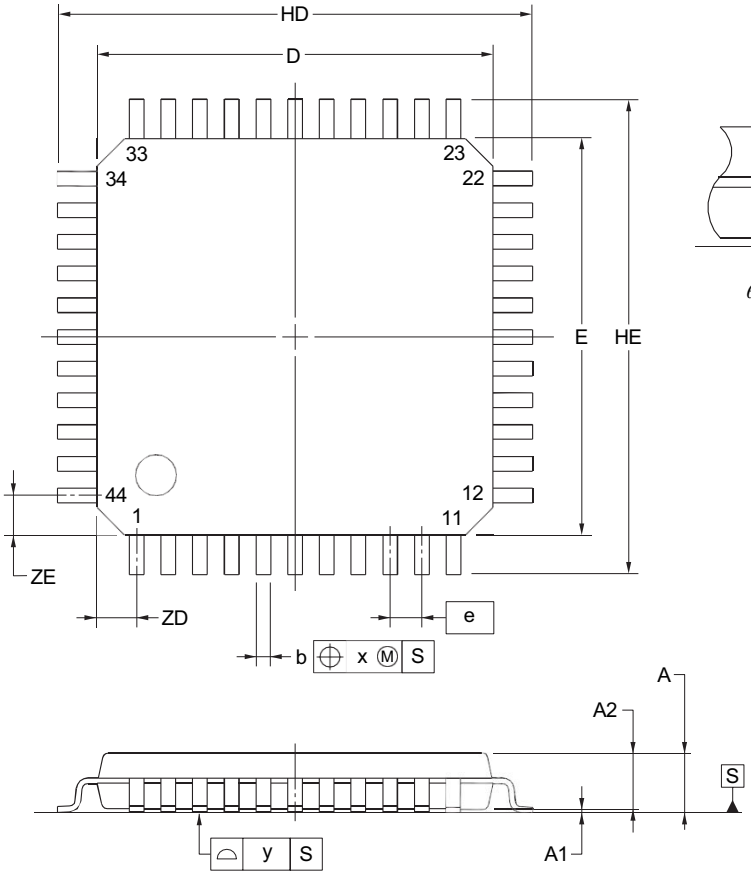
<1> The low level is input to the TOOL0 pin.
<2> The external reset is released. Note that the POR and LVD reset must be released before the external reset is released.
<3> The TOOL0 pin is set to the high level.
<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t_{SUINIT} : The time during which the communications for the initial setting must be completed within 100 ms after the external reset is released.
t_{SU} : Time to release the external reset after the TOOL0 pin is set to the low level
t_{HD} : Time to hold the TOOL0 pin at the low level after the external reset is released. It does not include the processing time of the firmware to control the flash memory.

3. Package Drawings

3.1 44-pin Products

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP44-10x10-0.80	PLQP0044GC-A	P44GB-80-UES-2	0.36



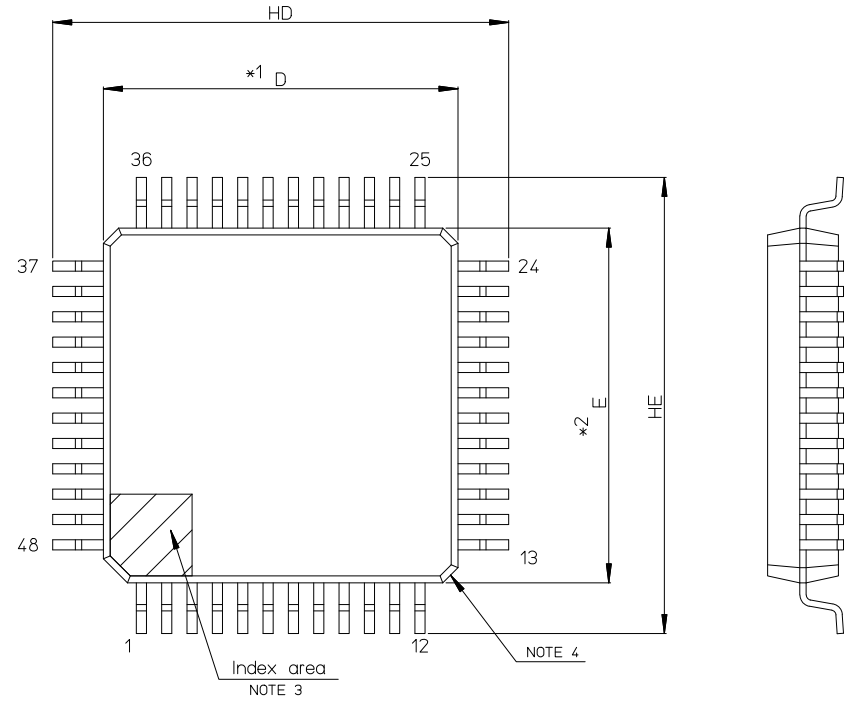
(UNIT:mm)

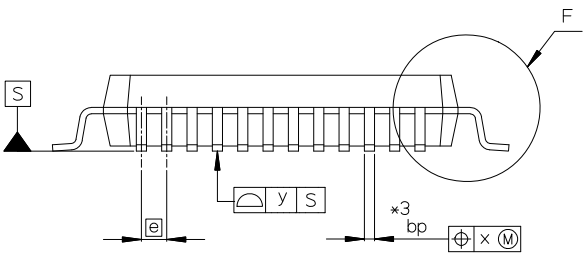
ITEM	DIMENSIONS
D	10.00±0.20
E	10.00±0.20
HD	12.00±0.20
HE	12.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	$0.37^{+0.08}_{-0.07}$
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.80
x	0.20
y	0.10
ZD	1.00
ZE	1.00

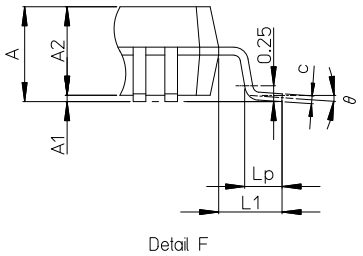
NOTE
Each lead centerline is located within 0.20 mm of its true position at maximum material condition.

3.2 48-pin Products

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP48-7x7-0.50	PLQP0048KB-B	——	0.2g





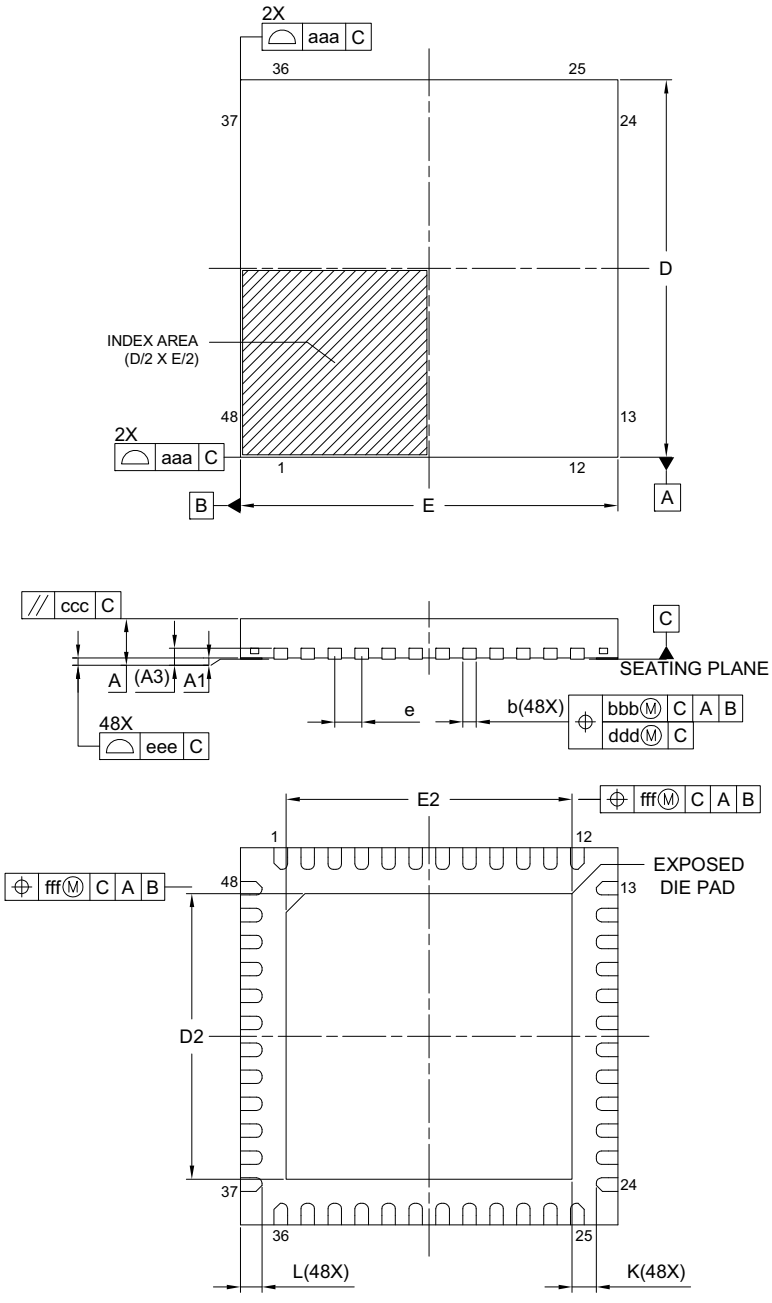


Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL; SIZE MAY VARY.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A2	——	1.4	——
HD	8.8	9.0	9.2
HE	8.8	9.0	9.2
A	——	——	1.7
A1	0.05	——	0.15
bp	0.17	0.20	0.27
c	0.09	——	0.20
θ	0°	3.5°	8°
e	——	0.5	——
x	——	——	0.08
y	——	——	0.08
Lp	0.45	0.6	0.75
L1	——	1.0	——

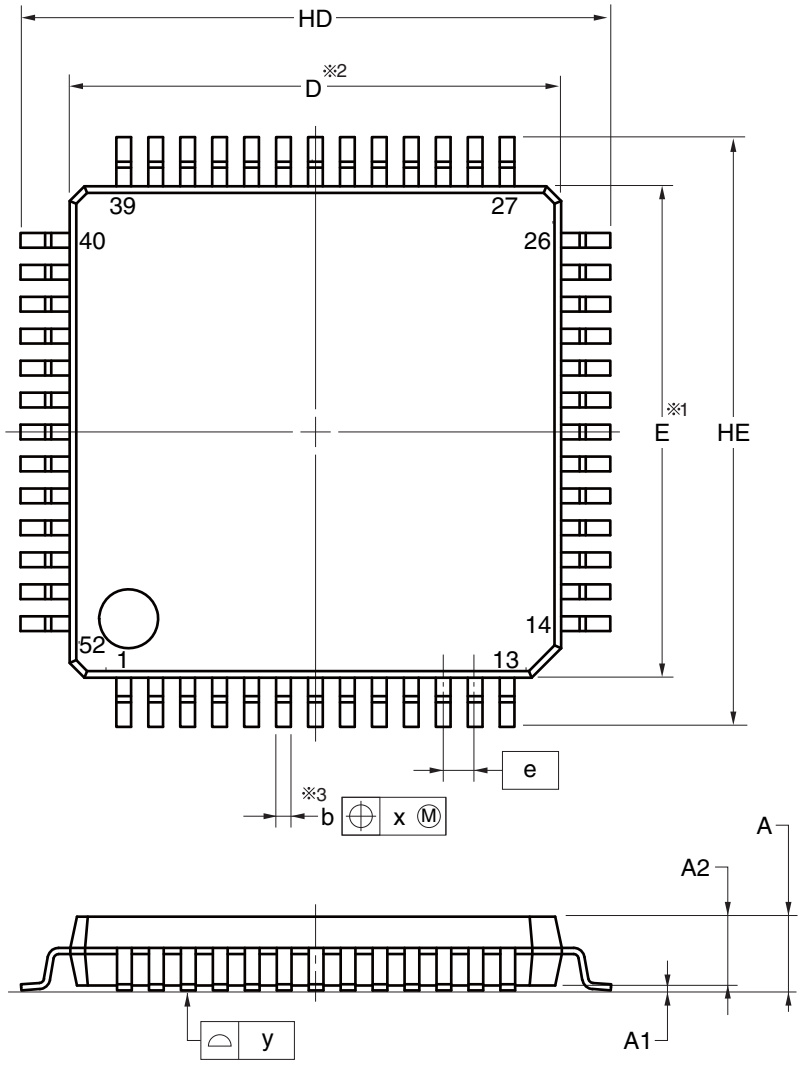
JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HWQFN048-7x7-0.50	PWQN0048KC-A	0.13 g

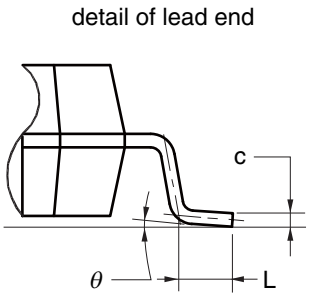


Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A_1	0.00	0.02	0.05
A_3		0.203 REF.	
b	0.20	0.25	0.30
D		7.00 BSC	
E		7.00 BSC	
e		0.50 BSC	
L	0.30	0.40	0.50
K	0.20	—	—
D_2	5.25	5.30	5.35
E_2	5.25	5.30	5.35
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

3.3 52-pin Products

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP52-10x10-0.65	PLQP0052JA-A	P52GB-65-GBS-1	0.3





(UNIT:mm)

ITEM	DIMENSIONS
D	10.00±0.10
E	10.00±0.10
HD	12.00±0.20
HE	12.00±0.20
A	1.70 MAX.
A1	0.10±0.05
A2	1.40
b	0.32±0.05
c	0.145±0.055
L	0.50±0.15
θ	0° to 8°
e	0.65
x	0.13
y	0.10

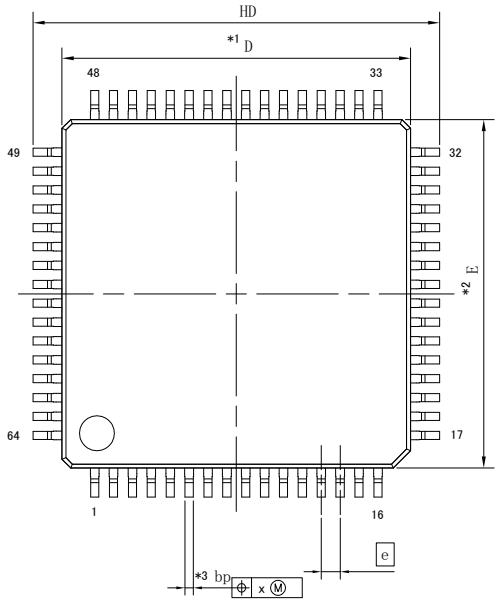
NOTE

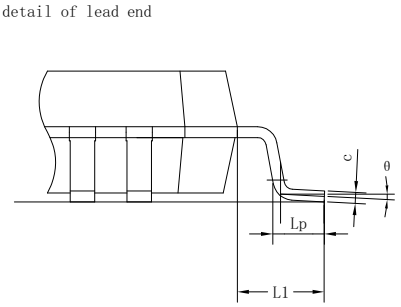
1.Dimensions "※1" and "※2" do not include mold flash.

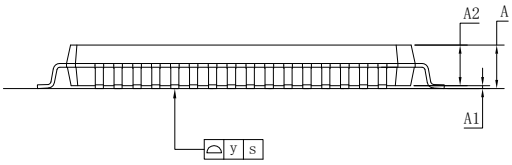
2.Dimension "※3" does not include trim offset.

3.4 64-pin Products

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-LQFP64-12x12-0.65	PLQP0064JB-A	0.50





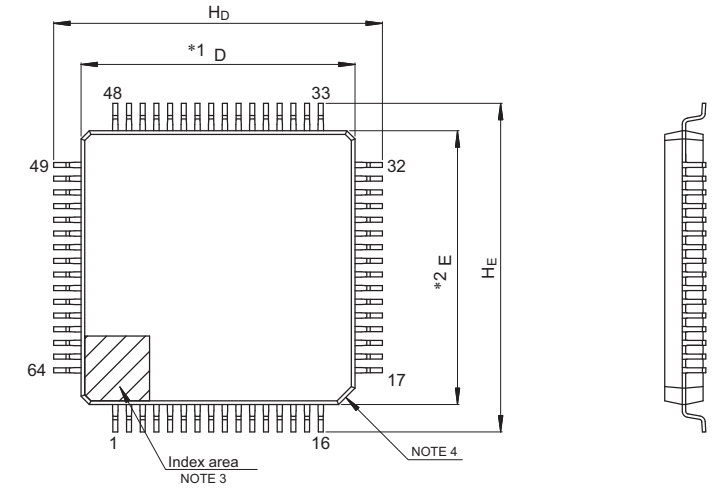


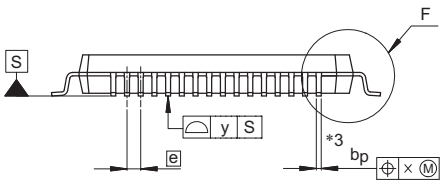
NOTE
1.DIMENSIONS "*1" AND "*2"DO NOT INCLUDE MOLD FLASH.
2.DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

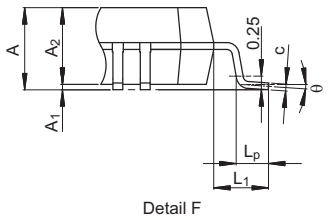
Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
E	11.90	12.00	12.10
D	11.90	12.00	12.10
A_2	—	1.40	—
H_D	13.80	14.00	14.20
H_E	13.80	14.00	14.20
A	—	—	1.70
A_1	0.05	—	0.15
Lp	0.45	0.60	0.75
L1	—	1.00	—
b_p	0.27	0.32	0.37
c	0.09	—	0.20
e	—	0.65	—
θ	0.00	3.50	8.00
x	—	—	0.08
y	—	—	0.08

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP64-10x10-0.50	PLQP0064KB-C	—	0.3

Unit: mm







Detail F

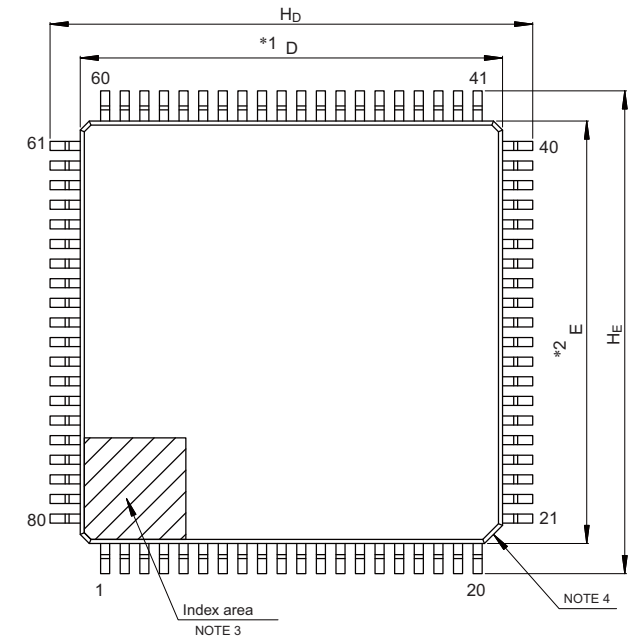
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

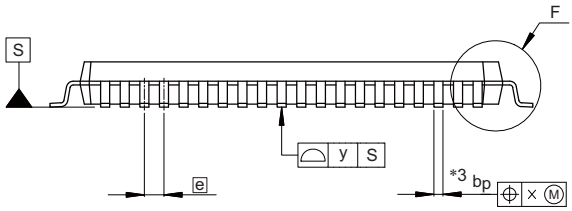
3.5 80-pin Products

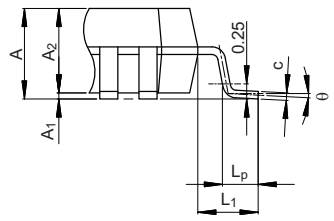
JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LQFP80-14x14-0.65	PLQP0080JA-B	—	0.6

Unit: mm



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.



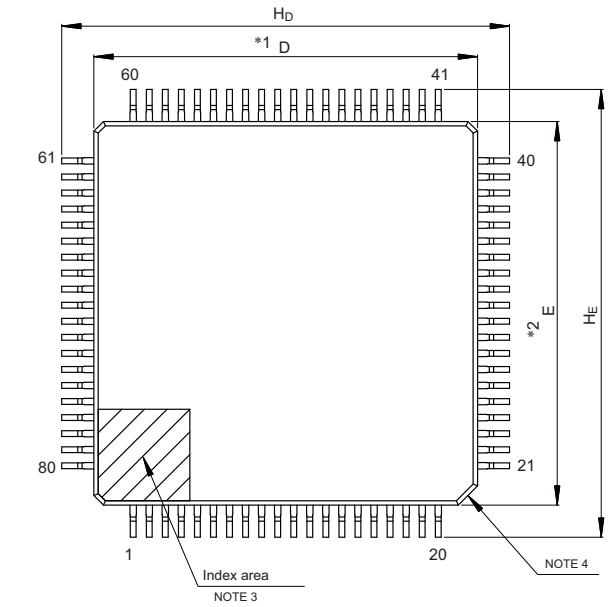


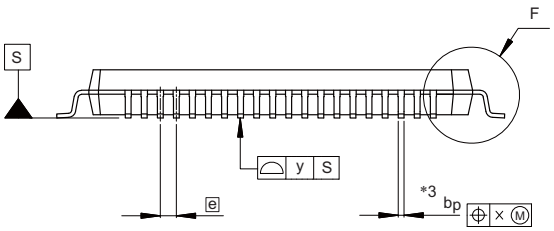
Detail F

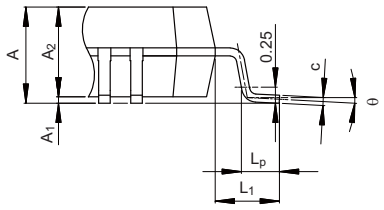
Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.22	0.30	0.38
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
L_p	0.45	0.6	0.75
L_1	—	1.0	—

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP80-12x12-0.50	PLQP0080KB-B	—	0.5

Unit: mm







Detail F

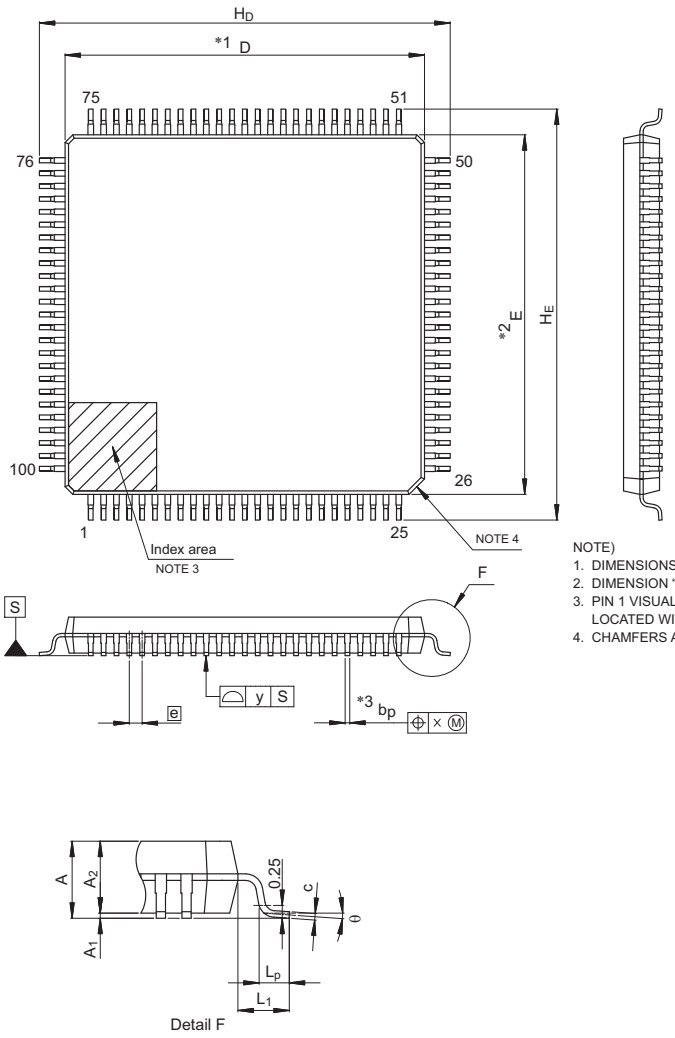
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	11.9	12.0	12.1
E	11.9	12.0	12.1
A_2	—	1.4	—
H_D	13.8	14.0	14.2
H_E	13.8	14.0	14.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

3.6 100-pin Products

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP100-14x14-0.50	PLQP0100KB-B	—	0.6

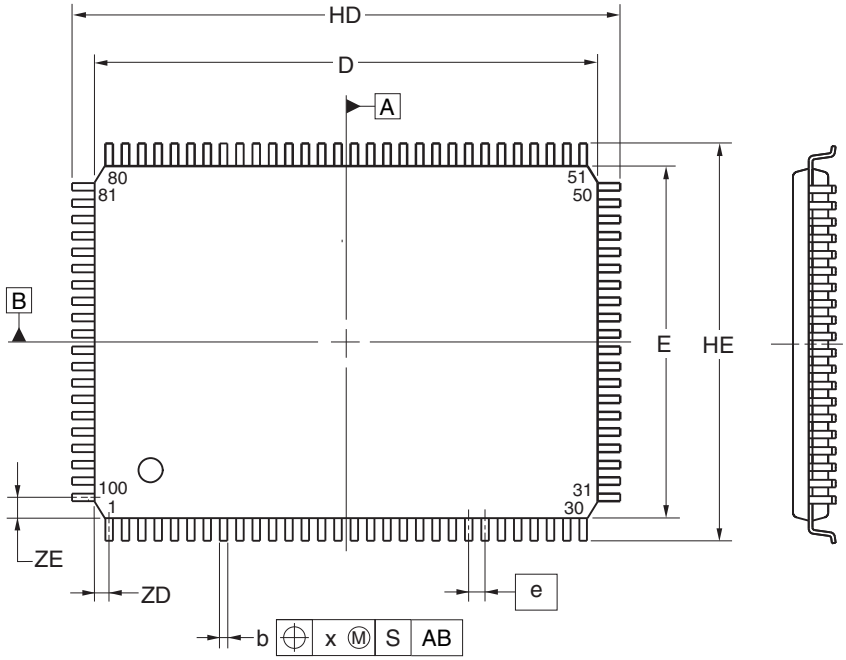
Unit: mm

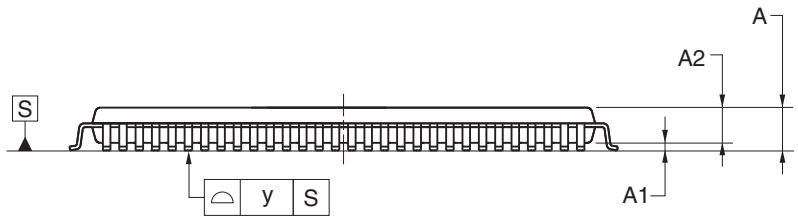


NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

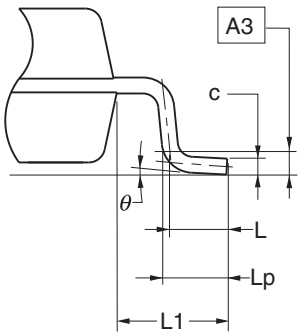
Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP100-14x20-0.65	PLQP0100JC-A	P100GF-65-GBN-1	0.92





detail of lead end



(UNIT:mm)

ITEM	DIMENSIONS
D	20.00±0.20
E	14.00±0.20
HD	22.00±0.20
HE	16.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	$0.32^{+0.08}_{-0.07}$
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.65
x	0.13
y	0.10
ZD	0.575
ZE	0.825

REVISION HISTORY	RL78/L23 Datasheet

Rev.	Date	Description	
		Page	Summary
1.00	May 30, 2025	—	First edition issued

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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