RH850/U2A

Renesas microcontroller

Section 1 Overview

The RH850/U2A-EVA is an emulation device of RH850/U2A16 (516 pins), RH850/U2A16 (373 pins), RH850/U2A16 (292 pins), RH850/U2A8 (373 pins), RH850/U2A8 (292 pins), RH850/U2A6 (292 pins), RH850/U2A6 (176 pins), RH850/U2A6 (156 pins) and RH850/U2A6 (144 pins) production devices which are the single-chip microcontroller RH850 series from Renesas Electronics.

This section describes an overview of the RH850/U2A-EVA (516 pins), RH850/U2A16 (516 pins), RH850/U2A16 (373 pins), RH850/U2A16 (292 pins), RH850/U2A8 (373 pins), RH850/U2A8 (292 pins), RH850/U2A6 (292 pins), RH850/U2A6 (176 pins), RH850/U2A6 (156 pins) and RH850/U2A6 (144 pins).

1.1 Outline

This product is a 32-bit single-chip microcontroller that incorporates multiple CPUs of the RH850 Series, code flash, data flash, RAM, DMA controllers, high-speed communication interfaces including CAN, FlexRay, Ethernet, RHSIF, LIN, SENT, PSI5S, PSI5, peripheral functions including A/D converters, timer units and many communication interfaces that are used in the automotive applications. This product also conforms to the Automotive Safety Integrity Level (ASIL) that is highly demanded in the recent automotive field (ASIL D level).

(1) Includes multiple RH850 cores

This product contains multi RH850G4MH2 cores (each CPU is referred to as CPU0 to CPU3 (U2A8, U2A6: CPU0 to CPU1) hereafter). Each CPU supports RISC-type instruction sets and have significantly improved the instruction execution speed with basic instructions (one clock cycle per instruction) and the optimized 10-stage pipeline configurations. Furthermore, this product also supports multiplication instructions using a 32-bit hardware multiplier, saturated product-sum operation instructions, and bit manipulation instructions as instructions best suited for various fields. In addition, this product also support CPU virtualization function.

Two-byte basic instructions and high-level language instructions improve object code efficiency for the C compiler and reduce the program size. Furthermore, this product is suited for advanced real-time control applications by offering a high-speed response time including the processing time of the on-chip interrupt controller.

(2) On-chip code flash and data flash

This product incorporates a 16-MB (U2A8: 8MB, U2A6: 6MB) code flash allowing high-speed accesses, which enables each CPU to access this flash memory efficiently. This memory can be reprogrammed while it is placed on an application system. This can shorten the system development period and significantly improve the serviceability after the system is delivered.

This product also has a 576-KB (U2A8: 320-KB, U2A6: 256-KB) data flash that is available for storing EEPROM data.

(3) Rich peripheral functionality

This microcontroller supports common communication interfaces such as SPI (CSI), I^2C as well as automotive oriented communication interfaces such as Ethernet, RHSIF, FlexRay, CAN-FD, LIN, CXPI, SENT, PSI5, PSI5S. As internal peripheral modules, this microcontroller have A/D Converter, Long-Term System Counter, Generic Timer Module, timer units and dedicated Peripheral Interconnect module which connects the functionalities of these peripherals. It also has the global standard on-chip Nexus JTAG as a debug interface. This allows construction of systems without the need to provide these functions externally, which reduces cost, quantity of components, and PCB footprint.

(4) Functional safety support

This product equips several dedicated functionalities including the Dual Core Lock Step configuration for the CPU, the memory protection with ECC, the bus protection with ECC/EDC, the peripheral module protection, and voltage / clock monitors to support the functional safety standard (ISO26262) required in the automotive applications.

(5) Security support

This product provides various security features and utilizes the Intelligent Cryptographic Unit/Master (ICUMHA) as an on-chip Hardware Security Module (HSM).

1.2 Application Fields

- Automotive field (including body control and chassis & safety)

1.3 Ordering Information

Table 1.1 Product Name List (1/2)

Name	Package	On-Chip ROM	Operating Temperature (Tj)	External Oscillator	Maximum Operating Frequency	MSPI restriction *1	SVR restriction *3	Note
R7F702Z19AEDBG (RH850/U2A-EVA)	Plastic FBGA-516 0.8-mm ball pitch 25 mm × 25 mm (RENESAS code*2 = PRBG0516GC-A)	16 MB	max. 160°C	16/20/24/40 MHz	400 MHz	Yes	No	*4
R7F702Z19BFDBG (RH850/U2A-EVA)	Plastic FBGA-516 0.8-mm ball pitch 25 mm × 25 mm (RENESAS code*2 = PRBG0516GC-A)	16 MB	max. 160°C	16/20/24/40 MHz	400 MHz	No	No	—
R7F702300EBBG-C (RH850/U2A16)	Plastic FBGA-516 0.8-mm ball pitch 25 mm × 25 mm (RENESAS code*2 = PRBG0516GC-A)	16 MB	max. 150°C	16/20/24/40 MHz	400 MHz	Yes	Yes	*4
R7F702300EBBB-C (RH850/U2A16)	Plastic FBGA-373 0.8-mm ball pitch 21 mm × 21 mm	16 MB	max. 150°C	16/20/24/40 MHz	400 MHz	Yes	Yes	*4
R7F702300EABA-C (RH850/U2A16)	Plastic FBGA-292 0.8-mm ball pitch 17 mm × 17 mm	16 MB	max. 160°C	16/20/24/40 MHz	400 MHz	Yes	Yes	*4
R7F702300AEBBC-C (RH850/U2A16)	Plastic FBGA-516 0.8-mm ball pitch 25 mm × 25 mm (RENESAS code*2 = PRBG0516GD-A	16 MB	max. 150°C	16/20/24/40 MHz	400 MHz	No	Yes	*4
R7F702300AEBBB-C (RH850/U2A16)	Plastic FBGA-373 0.8-mm ball pitch 21 mm × 21 mm	16 MB	max. 150°C	16/20/24/40 MHz	400 MHz	No	Yes	*4
R7F702300AFABA-C (RH850/U2A16)	Plastic FBGA-292 0.8-mm ball pitch 17 mm × 17 mm	16 MB	max. 160°C	16/20/24/40 MHz	400 MHz	No	Yes	*4
R7F702300BEBBC-C (RH850/U2A16)	Plastic FBGA-516 0.8-mm ball pitch 25 mm × 25 mm (RENESAS code*2 = PRBG0516GD-A)	16 MB	max. 150°C	16/20/24/40 MHz	400 MHz	No	No	—
R7F702300BEBBB-C (RH850/U2A16)	Plastic FBGA-373 0.8-mm ball pitch 21 mm × 21 mm	16 MB	max. 150°C	16/20/24/40 MHz	400 MHz	No	No	—
R7F702300BFABA-C (RH850/U2A16)	Plastic FBGA-292 0.8-mm ball pitch 17 mm × 17 mm	16 MB	max. 160°C	16/20/24/40 MHz	400 MHz	No	No	—
R7F702301EBBA-C (RH850/U2A8)	Plastic FBGA-373 0.8-mm ball pitch 21 mm × 21 mm	8 MB	max. 150°C	16/20/24/40 MHz	400 MHz	Yes	Yes	*4
R7F702301EABG-C (RH850/U2A8)	Plastic FBGA-292 0.8-mm ball pitch 17 mm × 17 mm	8 MB	max. 160°C	16/20/24/40 MHz	400 MHz	Yes	Yes	*4
R7F702301AEBBA-C (RH850/U2A8)	Plastic FBGA-373 0.8-mm ball pitch 21 mm × 21 mm	8 MB	max. 150°C	16/20/24/40 MHz	400 MHz	No	Yes	*4
R7F702301AFABG-C (RH850/U2A8)	Plastic FBGA-292 0.8-mm ball pitch 17 mm × 17 mm	8 MB	max. 160°C	16/20/24/40 MHz	400 MHz	No	Yes	*4
R7F702301BEBBA-C (RH850/U2A8)	Plastic FBGA-373 0.8-mm ball pitch 21 mm × 21 mm	8 MB	max. 150°C	16/20/24/40 MHz	400 MHz	No	No	—
R7F702301BFABG-C (RH850/U2A8)	Plastic FBGA-292 0.8-mm ball pitch 17 mm × 17 mm	8 MB	max. 160°C	16/20/24/40 MHz	400 MHz	No	No	—
R7F702302FABB-C (RH850/U2A6)	Plastic FBGA-292 0.8-mm ball pitch 17 mm × 17 mm	6 MB	max. 160°C	16/20/24/40 MHz	400 MHz	No	No	—

Table 1.1 Product Name List (2/2)

Name	Package	On-Chip ROM	Operating Temperature (Tj)	External Oscillator	Maximum Operating Frequency	MSPI restriction *1	SVR restriction *3	Note
R7F702302FAFK-C (RH850/U2A6)	Plastic HLQFP-176 0.5 mm pin pitch 24 mm × 24 mm	6 MB	max. 160°C	16/20/24/40 MHz	400 MHz	No	No	—
R7F702302FABD-C (RH850/U2A6)	Plastic LFBGA-156 0.65 mm ball pitch 10 mm × 10 mm	6 MB	max. 160°C	16/20/24/40 MHz	400 MHz	No	No	—
R7F702302FAFM-C (RH850/U2A6)	Plastic HLQFP-144 0.4 mm pin pitch 16 mm × 16 mm	6 MB	max. 160°C	16/20/24/40 MHz	400 MHz	No	No	—

Note 1. Refer to RH850/U2A-EVA Group User's Manual: Hardware **Section 19.8, MSPI restrictions**.

Note 2. Refer to **Section 4.1, Package Outline**.

Note 3. Refer to RH850/U2A-EVA Group User's Manual: Hardware **Section 10.10, SVR restriction**.

Note 4. As sales of these products is limited, please contact your sales representative first when considering these products for purchasing and project development.

FBGA is hereafter referred to as BGA unless the complete abbreviation is required.

The RH850/U2A-EVA series has 21 variants. Select the proper product according to the table below.

Table 1.2 RH850/U2A-EVA List

Frequency	Package					
	FBGA-516	FBGA-373	FBGA-292	HLQFP-176	LFBGA-156	HLQFP-144
400 MHz	R7F702Z19AEDBG (RH850/U2A-EVA)*1 R7F702Z19BFDBG (RH850/U2A-EVA) R7F702300EBBG-C (RH850/U2A16)*1 R7F702300AEBBC-C (RH850/U2A16)*1 R7F702300BEBBC-C (RH850/U2A16)	R7F702300EBBB-C (RH850/U2A16)*1 R7F702300AEBBB-C (RH850/U2A16)*1 R7F702300BEBBB-C (RH850/U2A16) R7F702301EBBA-C (RH850/U2A8)*1 R7F702301AEBBA-C (RH850/U2A8)*1 R7F702301BEBBA-C (RH850/U2A8)	R7F702300EABA-C (RH850/U2A16)*1 R7F702300AFABA-C (RH850/U2A16)*1 R7F702300BFABA-C (RH850/U2A16) R7F702301EABG-C (RH850/U2A8)*1 R7F702301AFABG-C (RH850/U2A8)*1 R7F702301BFABG-C (RH850/U2A8) R7F702302FABB-C (RH850/U2A6)	R7F702302FAFK-C (RH850/U2A6)	R7F702302FABD-C (RH850/U2A6)	R7F702302FAFM-C (RH850/U2A6)

Note 1. As sales of these products is limited, contact your sales representative first when considering these products for purchasing and project development.

1.4 Differences in the Specifications of RH850/U2A-EVA Products

The table below lists the differences in the specifications of RH850/U2A-EVA products.

(1/3)

Product			RH850/U2A-EVA 516 pins	RH850/U2A16 516 pins	RH850/U2A16 373 pins	RH850/U2A16 292 pins	RH850/U2A8 373 pins	RH850/U2A8 292 pins	RH850/U2A6 292 pins	RH850/U2A6 176 pins	RH850/U2A6 156 pins	RH850/U2A6 144 pins
CPU	Frequency		400	400	400	400	400	400	400	400	400	400
	Main Core		4	4	4	4	2	2	2	2	2	2
	Lockstep		4	4	4	4	2	2	2	2	2	2
	FPU		4	4	4	4	2	2	2	2	2	2
	Instruction Cache per core (for Code Flash)		16 KB (PBS 4w)	16 KB (PBS 4w)	16 KB (PBS 4w)	16 KB (PBS 4w)	16 KB (PBS 4w)	16 KB (PBS 4w)	16 KB (PBS 4w)	16 KB (PBS 4w)	16 KB (PBS 4w)	16 KB (PBS 4w)
	Data Buffer per core (for Code Flash)		4 lines (256 bit/ line)	4 lines (256 bit/ line)	4 lines (256 bit/ line)	4 lines (256 bit/ line)	4 lines (256 bit/ line)	4 lines (256 bit/ line)	4 lines (256 bit/ line)	4 lines (256 bit/ line)	4 lines (256 bit/ line)	4 lines (256 bit/ line)
	MPU regions per core		32	32	32	32	32	32	32	32	32	32
	IPIR	Unit	1	1	1	1	1	1	1	1	1	1
	BARR	Unit	1	1	1	1	1	1	1	1	1	1
	TPTM	Unit	1	1	1	1	1	1	1	1	1	1
RAM	Total RAM (Local RAM + Cluster RAM)		3584 KB	3584 KB	3584 KB	3584 KB	1792 KB	1792 KB	768 KB	768 KB	768 KB	768 KB
	Local RAM per core		64 KB	64 KB	64 KB	64 KB	64 KB	64 KB	64 KB	64 KB	64 KB	64 KB
	Cluster RAM (CRAM)	Total Size (Retention RAM included)	3328 KB	3328 KB	3328 KB	3328 KB	1664 KB	1664 KB	640 KB	640 KB	640 KB	640 KB
		Retention RAM (included in CRAM)	256 KB	256 KB	256 KB	256 KB	128 KB	128 KB	128 KB	128 KB	128 KB	128 KB
	Cluster Emulation RAM		2 MB (1 MB for each cluster 0 & 1)	No	No	No	No	No	32 KB (cluster 0)	32 KB (cluster 0)	32 KB (cluster 0)	32 KB (cluster 0)
	Global Emulation RAM		2 MB	No	No	No	No	No	No	No	No	No
	Instrumentation RAM		96 KB	No	No	No	No	No	No	No	No	No
	Trace RAM		64 KB	No	No	No	No	No	32 KB	32 KB	32 KB	32 KB
Flash	Code Flash		16 MB	16 MB	16 MB	16 MB	8 MB	8 MB	6 MB	6 MB	6 MB	6 MB
	Data Flash	Total Size	576 KB	576 KB	576 KB	576 KB	320 KB	320 KB	256 KB	256 KB	256 KB	256 KB
		Dedicated ICUMHA	64 KB	64 KB	64 KB	64 KB	64 KB	64 KB	64 KB	64 KB	64 KB	64 KB
DMA	sDMAC	Channels	32	32	32	32	32	32	32	32	32	32
	DTS	Channels	128	128	128	128	128	128	128	128	128	128
I/O port			301	301	221	165	221	165	165	129	77	97
Timer	ENCA	Units	2	2	2	2	2	2	2	1	No	1
	OSTM	Units	10	10	10	10	8	8	8	8	8	8
	WDTB	Units	5	5	5	5	3	3	3	3	3	3
	LTSC	Unit	1	1	1	1	1	1	1	1	1	1
	SWDT	Unit	1	1	1	1	1	1	1	1	1	1
	GTM	Unit	1	1	1	1	1	1	1	1	1	1
	TAPA	Units	4	4	4	4	4	4	4	3	2	2
	TPBA	Units	2	2	2	2	2	2	2	2	2	2
	TAUD	Units	3	3	3	3	3	3	3	3	3	3
	TAUJ	Units	4	4	4	4	4	4	4	4	4	4
	TSG3	Units	2	2	2	2	2	2	2	2	1	1
	PWM-Diag	Units	96	96	96	96	96	96	96	76	50	64
	RTCA	Unit	1	1	1	1	1	1	1	1	1	1

(2/3)

Product			RH850/U2A-EVA 516 pins	RH850/U2A16 516 pins	RH850/U2A16 373 pins	RH850/U2A16 292 pins	RH850/U2A8 373 pins	RH850/U2A8 292 pins	RH850/U2A6 292 pins	RH850/U2A6 176 pins	RH850/U2A6 156 pins	RH850/U2A6 144 pins
Communication	SCI3	Units	3	3	3	3	3	3	No	No	No	No
	RLIN3	Units	24	24	24	12	24	12	12	12	8	10
	CXPI	Units	4	4	4	4	4	4	No	No	No	No
	MSPI	Units	10	10	9	6	9	6	6	6	6	4
	RHSIF	Unit	1	1	1	1	1	1	No	No	No	No
	RS-CANFD	Units [Channels]	2 [16ch]	2 [16ch]	2 [16ch]	2 [16ch]	2 [16ch]	2 [16ch]	2 [12ch]	2 [11ch]	2 [8ch]	2 [7ch]
	FlexRay	Units [Channels]	2 [4ch]	2 [4ch]	2 [4ch]	2 [4ch]	2 [4ch]	2 [4ch]	1 [2ch]	1 [2ch]	1 [2ch]	1 [2ch]
	Ethernet	Channel (100Mb/1Gb)	1/1	1/1	1/1	1/1	1/1	1/1	1/0	1/0	No	1/0
		ETNB0 (MII/RMII/SGMII)	Yes/Yes/No	Yes/Yes/No	Yes/Yes/No	Yes/Yes/No	Yes/Yes/No	Yes/Yes/No	Yes/Yes/No	Yes/Yes/No	No/No/No	Yes/Yes/No
		ETNB1 (MII/RMII/SGMII)	Yes/No/Yes	Yes/No/Yes	No/No/Yes	No/No/Yes	No/No/Yes	No/No/Yes	No/No/No	No/No/No	No/No/No	No/No/No
	RSENT	Units	8	8	8	8	8	8	8	8	8	6
	PSI5	Channels	4	4	4	4	4	4	4	4	4	3
	PSI5S	Units	2	2	2	2	2	2	2	1	1	1
	RIIC	Units	2	2	2	2	2	2	2	2	2	1
	eMMC	Unit	1	1	1	1	1	1	1	1	No	No
	SFMA	Unit	1	1	1	1	1	1	1	1	No	No
Safety	ASIL level		N/A	D	D	D	D	D	D	D	D	D
	ECM		Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	CRC(KCRC)	Units	8	8	8	8	8	8	8	8	8	8
	Clock Monitor		Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	Error injection for self-diagnosis of several safety mechanisms		Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	LBIST		Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	MBIST		Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	Bus ECC		Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
ADC	ADCJ	Units	3	3	3	3	3	3	3	3	2	3
		ADCJ0/1/2 (Channels) (High accuracy inputs)	20/20/20	20/20/20	20/20/20	20/20/5	20/20/20	20/20/5	20/20/5	14/14/5	8/8/0	10/10/0
		ADCJ0/1/2 (Low accuracy inputs)	10/14/10	10/14/10	10/14/10	10/14/10	10/14/10	10/14/10	10/14/10	10/14/7	6/7/0	3/10/6
		Total inputs	94	94	94	79	94	79	79	64	29	39
		Virtual channels per unit	64	64	64	64	64	64	64	64	64	64
		ADC timers	2	2	2	2	2	2	2	2	2	2
Debug	Nexus-JTAG		Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	Trace I/F (Aurora)		4 lanes	No	No	No	No	No	No	No	No	No
	Low Pin Debug I/F (4-pin)		Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	Bypass I/F (AUDR)		Yes	No	No	No	No	No	No	No	No	No
Security	Basic Hardware Protection (BHP)		Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	ICUMHA		Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	Secure RAM		64 KB	64 KB	64 KB	64 KB	64 KB	64 KB	64 KB	64 KB	64 KB	64 KB
	Secure Data Flash		64 KB	64 KB	64 KB	64 KB	64 KB	64 KB	64 KB	64 KB	64 KB	64 KB
	Code Flash Protection		Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
System Control	Temp Sensor		Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	Voltage Monitor		Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	LPS		Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes

(3/3)

Product		RH850/ U2A-EVA 516 pins	RH850/ U2A16 516 pins	RH850/ U2A16 373 pins	RH850/ U2A16 292 pins	RH850/ U2A8 373 pins	RH850/ U2A8 292 pins	RH850/ U2A6 292 pins	RH850/ U2A6 176 pins	RH850/ U2A6 156 pins	RH850/ U2A6 144 pins
Package*1	BGA516	Yes	Yes	No	No	No	No	No	No	No	No
	BGA373	No	No	Yes	No	Yes	No	No	No	No	No
	BGA292	No	No	No	Yes	No	Yes	Yes	No	No	No
	HLQFP176	No	No	No	No	No	No	No	Yes	No	No
	BGA156	No	No	No	No	No	No	No	No	Yes	No
	HLQFP144	No	No	No	No	No	No	No	No	No	Yes

Note 1. For product names, refer to **Section 1.3, Ordering Information**.

1.5 Pin Connection Diagram (Top View)

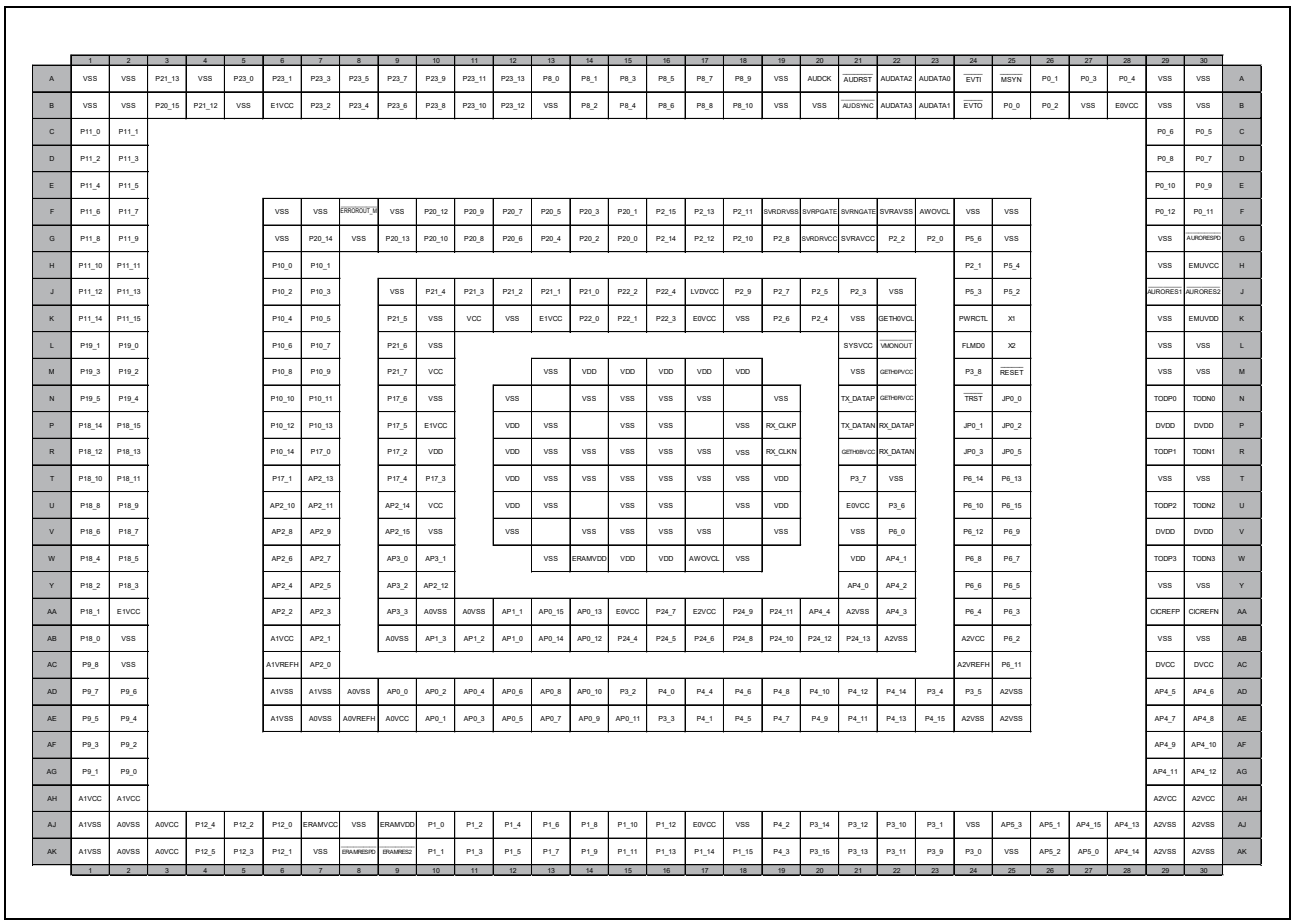
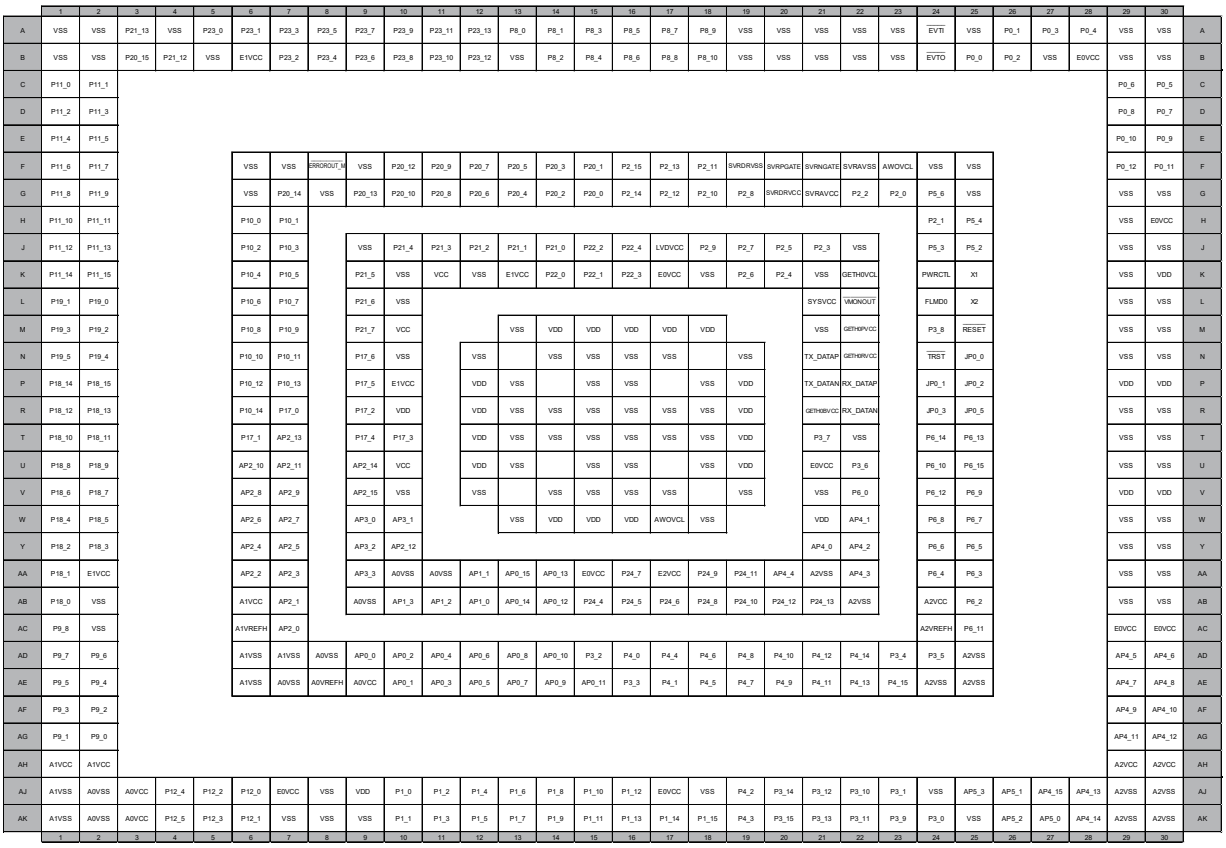


Figure 1.1 Pin Connection Diagram (BGA516 U2A-EVA)

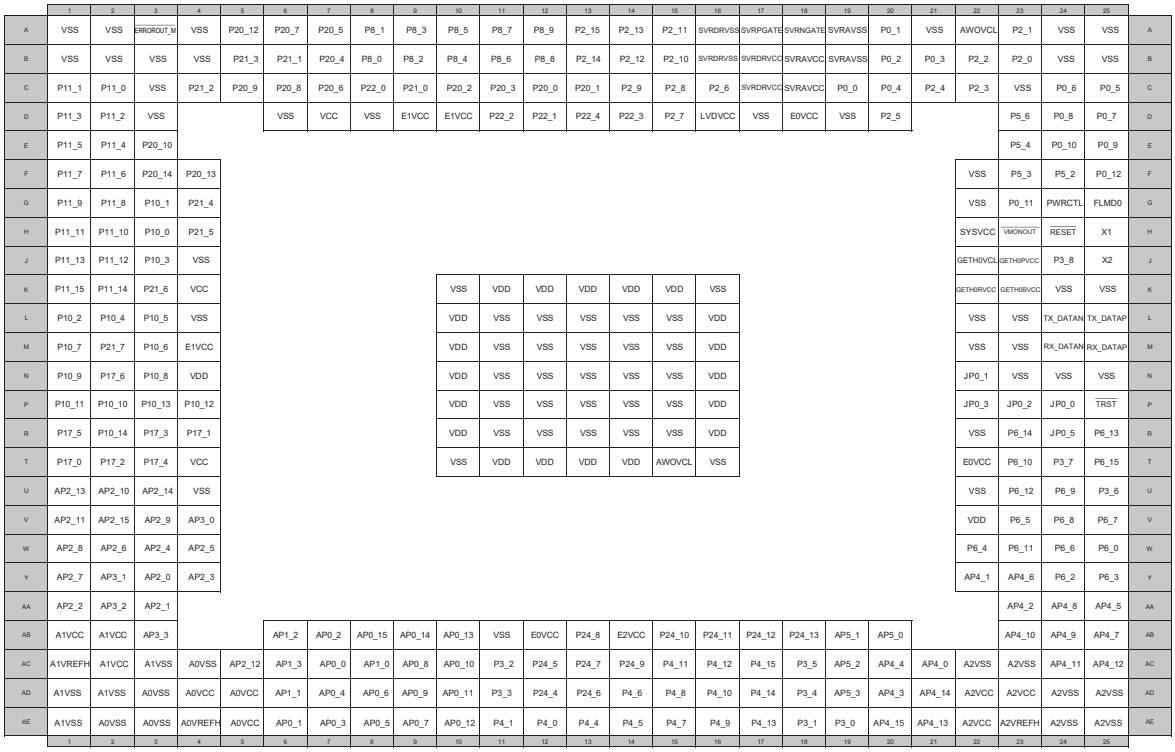


	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	
A	VSS	VSS	P21_13	VSS	P23_0	P23_1	P23_3	P23_5	P23_7	P23_9	P23_11	P23_13	P8_0	P8_1	P8_3	P8_5	P8_7	P8_9	VSS	VSS	VSS	VSS	VSS	EVTI	VSS	P0_1	P0_3	P0_4	VSS	VSS	A
B	VSS	VSS	P20_15	P21_12	VSS	E1VCC	P23_2	P23_4	P23_6	P23_8	P23_10	P23_12	VSS	P8_2	P8_4	P8_6	P8_8	P8_10	VSS	VSS	VSS	VSS	VSS	EVTO	P0_0	P0_2	VSS	E0VCC	VSS	VSS	B
C	P11_0	P11_1																											P0_6	P0_5	C
D	P11_2	P11_3																											P0_8	P0_7	D
E	P11_4	P11_5																											P0_10	P0_9	E
F	P11_6	P11_7																											P0_12	P0_11	F
G	P11_8	P11_9																											VSS	VSS	G
H	P11_10	P11_11																											VSS	E0VCC	H
J	P11_12	P11_13																											VSS	VSS	J
K	P11_14	P11_15																											VSS	VDD	K
L	P19_1	P19_0																											VSS	VSS	L
M	P19_3	P19_2																											VSS	VSS	M
N	P19_5	P19_4																											VSS	VSS	N
P	P18_14	P18_15																											VDD	VDD	P
R	P18_12	P18_13																											VSS	VSS	R
T	P18_10	P18_11																											VSS	VSS	T
U	P18_8	P18_9																											VSS	VSS	U
V	P18_6	P18_7																											VDD	VDD	V
W	P18_4	P18_5																											VSS	VSS	W
Y	P18_2	P18_3																											VSS	VSS	Y
AA	P18_1	E1VCC																											VSS	VSS	AA
AB	P18_0	VSS																											VSS	VSS	AB
AC	P9_8	VSS																											E0VCC	E0VCC	AC
AD	P9_7	P9_6																											AP4_5	AP4_6	AD
AE	P9_5	P9_4																											AP4_7	AP4_8	AE
AF	P9_3	P9_2																											AP4_9	AP4_10	AF
AG	P9_1	P9_0																											AP4_11	AP4_12	AG
AH	A1VCC	A1VCC																											A2VCC	A2VCC	AH
AJ	A1VSS	A0VSS	A0VCC	P12_4	P12_2	P12_0	E0VCC	VSS	VDD	P1_0	P1_2	P1_4	P1_6	P1_8	P1_10	P1_12	E0VCC	VSS	P4_2	P3_14	P3_12	P3_10	P3_1	VSS	AP5_3	AP5_1	AP4_15	AP4_13	A2VSS	A2VSS	AJ
AK	A1VSS	A0VSS	A0VCC	P12_5	P12_3	P12_1	VSS	VSS	VSS	P1_1	P1_3	P1_5	P1_7	P1_9	P1_11	P1_13	P1_14	P1_15	P4_3	P3_15	P3_13	P3_11	P3_9	P3_0	VSS	AP5_2	AP5_0	AP4_14	A2VSS	A2VSS	AK
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	

	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
F	VSS	VSS	ERROROUT_M	VSS	P20_12	P20_9	P20_7	P20_5	P20_3	P20_1	P2_15	P2_13	P2_11	SVRDRVSS	SVRPGATE	SVRNGATE	SVRAVSS	AWOVCL	VSS	VSS
G	VSS	P20_14	VSS	P20_13	P20_10	P20_8	P20_6	P20_4	P20_2	P20_0	P2_14	P2_12	P2_10	P2_8	SVRDRVCC	SVRAVCC	P2_2	P2_0	P5_6	VSS
H	P10_0	P10_1																	P2_1	P5_4
J	P10_2	P10_3		VSS	P21_4	P21_3	P21_2	P21_1	P21_0	P22_2	P22_4	LVDVCC	P2_9	P2_7	P2_5	P2_3	VSS		P5_3	P5_2
K	P10_4	P10_5		P21_5	VSS	VCC	VSS	E1VCC	P22_0	P22_1	P22_3	E0VCC	VSS	P2_6	P2_4	VSS	GETH0VCL		PWRCTL	X1
L	P10_6	P10_7		P21_6	VSS											SYSVCC	VMONOUT		FLMD0	X2
M	P10_8	P10_9		P21_7	VCC			VSS	VDD	VDD	VDD	VDD	VDD			VSS	GETH0PVCC		P3_8	RESET
N	P10_10	P10_11		P17_6	VSS		VSS		VSS	VSS	VSS	VSS		VSS		TX_DATAP	GETH0PVCC		TRST	JP0_0
P	P10_12	P10_13		P17_5	E1VCC		VDD	VSS		VSS	VSS		VSS	VDD		TX_DATAN	RX_DATAP		JP0_1	JP0_2
R	P10_14	P17_0		P17_2	VDD		VDD	VSS	VSS	VSS	VSS	VSS	VSS	VDD		GETH0BVCC	RX_DATAN		JP0_3	JP0_5
T	P17_1	AP2_13		P17_4	P17_3		VDD	VSS	VSS	VSS	VSS	VSS	VSS	VDD		P3_7	VSS		P6_14	P6_13
U	AP2_10	AP2_11		AP2_14	VCC		VDD	VSS		VSS	VSS		VSS	VDD		E0VCC	P3_6		P6_10	P6_15
V	AP2_8	AP2_9		AP2_15	VSS		VSS		VSS	VSS	VSS	VSS		VSS		VSS	P6_0		P6_12	P6_9
W	AP2_6	AP2_7		AP3_0	AP3_1			VSS	VDD	VDD	VDD	AWOVCL	VSS			VDD	AP4_1		P6_8	P6_7
Y	AP2_4	AP2_5		AP3_2	AP2_12											AP4_0	AP4_2		P6_6	P6_5
AA	AP2_2	AP2_3		AP3_3	A0VSS	A0VSS	AP1_1	AP0_15	AP0_13	E0VCC	P24_7	E2VCC	P24_9	P24_11	AP4_4	A2VSS	AP4_3		P6_4	P6_3
AB	A1VCC	AP2_1		A0VSS	AP1_3	AP1_2	AP1_0	AP0_14	AP0_12	P24_4	P24_5	P24_6	P24_8	P24_10	P24_12	P24_13	A2VSS		A2VCC	P6_2
AC	A1VREFH	AP2_0																	A2VREFH	P6_11
AD	A1VSS	A1VSS	A0VSS	AP0_0	AP0_2	AP0_4	AP0_6	AP0_8	AP0_10	P3_2	P4_0	P4_4	P4_6	P4_8	P4_10	P4_12	P4_14	P3_4	P3_5	A2VSS
AE	A1VSS	A0VSS	A0VREFH	A0VCC	AP0_1	AP0_3	AP0_5	AP0_7	AP0_9	AP0_11	P3_3	P4_1	P4_5	P4_7	P4_9	P4_11	P4_13	P4_15	A2VSS	A2VSS

Note: The pin location of RX_DATAP, RX_DATAN, TX_DATAP and TX_DATAN is defined by the Option Byte 14.
For details, refer to RH850/U2A-EVA Group User's Manual: Hardware **Section 51.12.20, OPBT14 — Option Byte 14**.

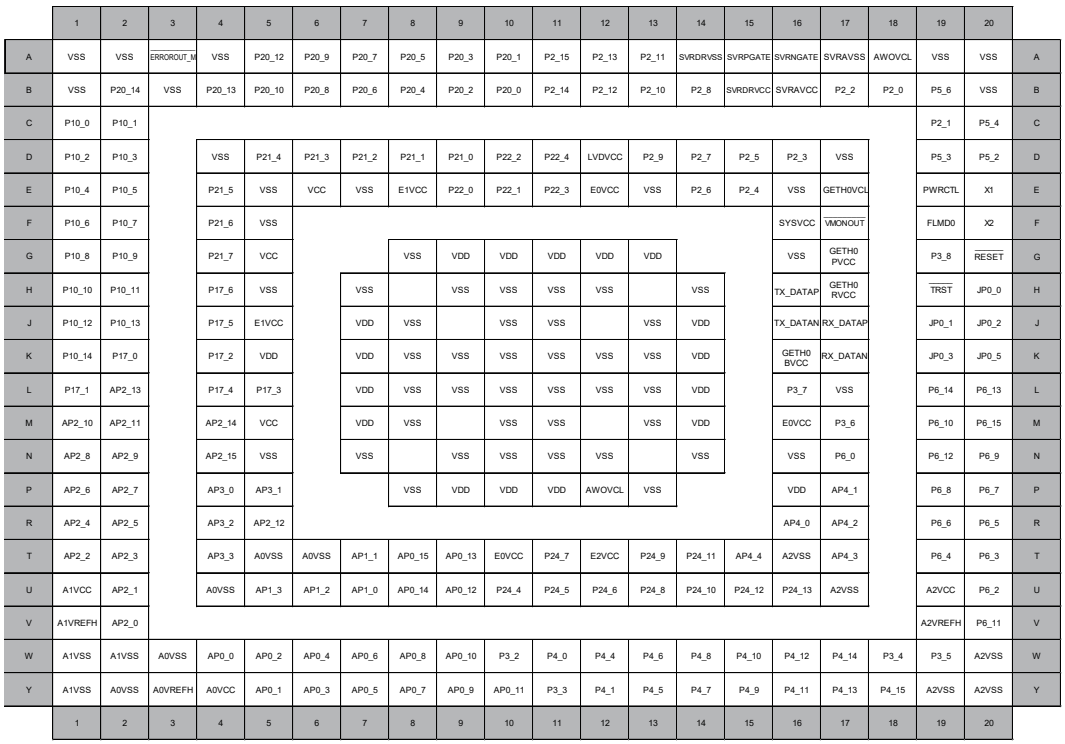
Figure 1.2 Pin Connection Diagram (BGA516 U2A16)



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	
A	VSS	VSS	ERROROUT_M	VSS	P20_12	P20_7	P20_5	P8_1	P8_3	P8_5	P8_7	P8_9	P2_15	P2_13	P2_11	SVRDRVSS	SVRPGATE	SVRNGATE	SVRAVSS	P0_1	VSS	AWOVCL	P2_1	VSS	VSS	A
B	VSS	VSS	VSS	VSS	P21_3	P21_1	P20_4	P8_0	P8_2	P8_4	P8_6	P8_8	P2_14	P2_12	P2_10	SVRDRVSS	SVRDRVCC	SVRAVCC	SVRAVSS	P0_2	P0_3	P2_2	P2_0	VSS	VSS	B
C	P11_1	P11_0	VSS	P21_2	P20_9	P20_8	P20_6	P22_0	P21_0	P20_2	P20_3	P20_0	P20_1	P2_9	P2_8	P2_6	SVRDRVCC	SVRAVCC	P0_0	P0_4	P2_4	P2_3	VSS	P0_6	P0_5	C
D	P11_3	P11_2	VSS			VSS	VCC	VSS	E1VCC	E1VCC	P22_2	P22_1	P22_4	P22_3	P2_7	LVDVCC	VSS	E0VCC	VSS	P2_5			P5_6	P0_8	P0_7	D
E	P11_5	P11_4	P20_10																				P5_4	P0_10	P0_9	E
F	P11_7	P11_6	P20_14	P20_13																		VSS	P5_3	P5_2	P0_12	F
G	P11_9	P11_8	P10_1	P21_4																		VSS	P0_11	PWRCTL	FLMD0	G
H	P11_11	P11_10	P10_0	P21_5																		SYSVCC	VMONOUT	RESET	X1	H
J	P11_13	P11_12	P10_3	VSS																		GETH0VCL	GETH0PVCC	P3_8	X2	J
K	P11_15	P11_14	P21_6	VCC						VSS	VDD	VDD	VDD	VDD	VDD	VSS						GETH0RVCC	GETH0BVCC	VSS	VSS	K
L	P10_2	P10_4	P10_5	VSS						VDD	VSS	VSS	VSS	VSS	VSS	VDD						VSS	VSS	TX_DATAN	TX_DATAP	L
M	P10_7	P21_7	P10_6	E1VCC						VDD	VSS	VSS	VSS	VSS	VSS	VDD						VSS	VSS	RX_DATAN	RX_DATAP	M
N	P10_9	P17_6	P10_8	VDD						VDD	VSS	VSS	VSS	VSS	VSS	VDD						JP0_1	VSS	VSS	VSS	N
P	P10_11	P10_10	P10_13	P10_12						VDD	VSS	VSS	VSS	VSS	VSS	VDD						JP0_3	JP0_2	JP0_0	TRST	P
R	P17_5	P10_14	P17_3	P17_1						VDD	VSS	VSS	VSS	VSS	VSS	VDD						VSS	P6_14	JP0_5	P6_13	R
T	P17_0	P17_2	P17_4	VCC						VSS	VDD	VDD	VDD	VDD	AWOVCL	VSS						E0VCC	P6_10	P3_7	P6_15	T
U	AP2_13	AP2_10	AP2_14	VSS																		VSS	P6_12	P6_9	P3_6	U
V	AP2_11	AP2_15	AP2_9	AP3_0																		VDD	P6_5	P6_8	P6_7	V
W	AP2_8	AP2_6	AP2_4	AP2_5																		P6_4	P6_11	P6_6	P6_0	W
Y	AP2_7	AP3_1	AP2_0	AP2_3																		AP4_1	AP4_6	P6_2	P6_3	Y
AA	AP2_2	AP3_2	AP2_1																				AP4_2	AP4_8	AP4_5	AA
AB	A1VCC	A1VCC	AP3_3			AP1_2	AP0_2	AP0_15	AP0_14	AP0_13	VSS	E0VCC	P24_8	E2VCC	P24_10	P24_11	P24_12	P24_13	AP5_1	AP5_0			AP4_10	AP4_9	AP4_7	AB
AC	A1VREFH	A1VCC	A1VSS	A0VSS	AP2_12	AP1_3	AP0_0	AP1_0	AP0_8	AP0_10	P3_2	P24_5	P24_7	P24_9	P4_11	P4_12	P4_15	P3_5	AP5_2	AP4_4	AP4_0	A2VSS	A2VSS	AP4_11	AP4_12	AC
AD	A1VSS	A1VSS	A0VSS	A0VCC	A0VCC	AP1_1	AP0_4	AP0_6	AP0_9	AP0_11	P3_3	P24_4	P24_6	P4_6	P4_8	P4_10	P4_14	P3_4	AP5_3	AP4_3	AP4_14	A2VCC	A2VCC	A2VSS	A2VSS	AD
AE	A1VSS	A0VSS	A0VSS	A0VREFH	A0VCC	AP0_1	AP0_3	AP0_5	AP0_7	AP0_12	P4_1	P4_0	P4_4	P4_5	P4_7	P4_9	P4_13	P3_1	P3_0	AP4_15	AP4_13	A2VCC	A2VREFH	A2VSS	A2VSS	AE
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	

Note: The pin location of RX_DATAP, RX_DATAN, TX_DATAP and TX_DATAN is defined by the Option Byte 14.
For details, refer to RH850/U2A-EVA Group User's Manual: Hardware **Section 51.12.20, OPBT14 — Option Byte 14**.

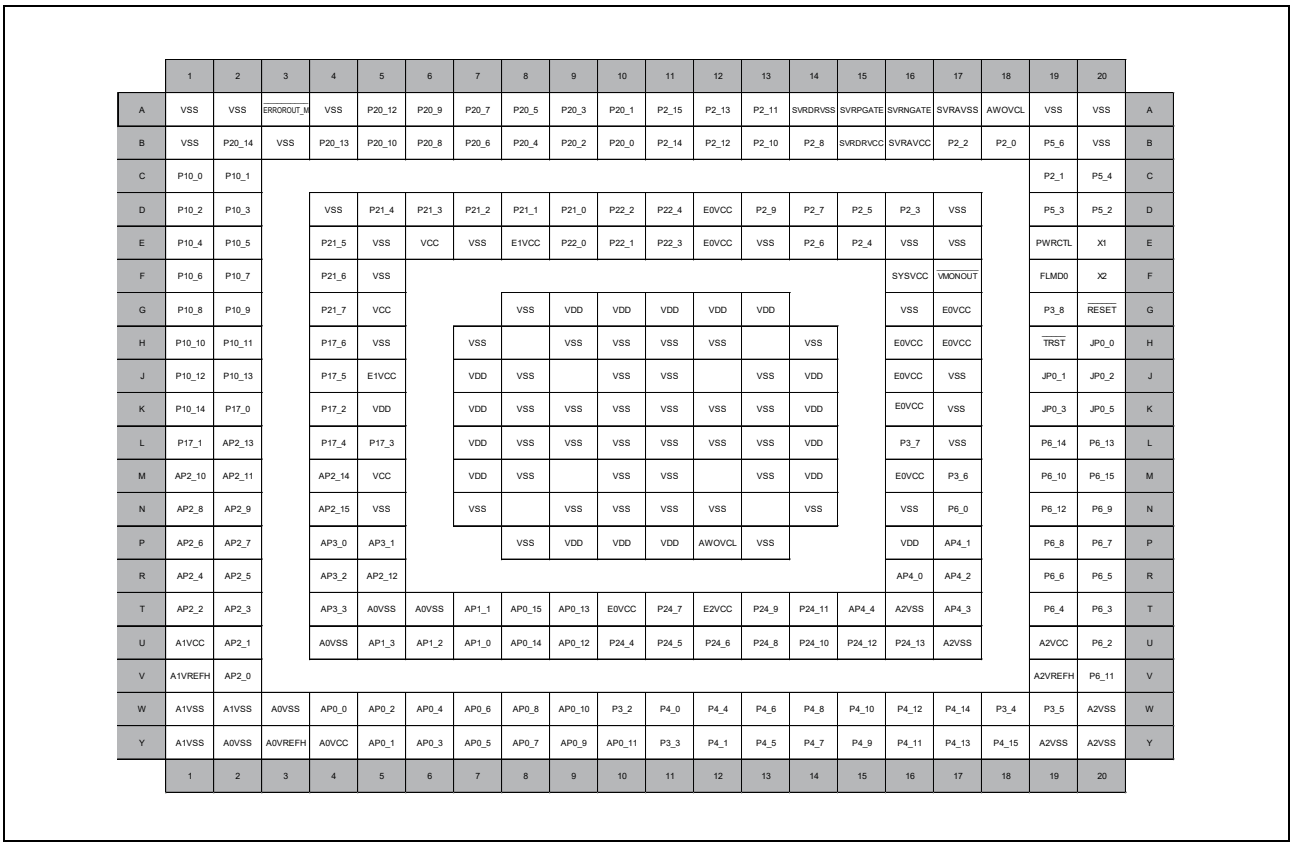
Figure 1.3 Pin Connection Diagram (BGA373 U2A16/U2A8)



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	VSS	VSS	$\overline{\text{ERROROUT\_M}}$	VSS	P20_12	P20_9	P20_7	P20_5	P20_3	P20_1	P2_15	P2_13	P2_11	SVRDRVSS	SVRPGATE	SVRNGATE	SVRAVSS	AWOVCL	VSS	VSS	A
B	VSS	P20_14	VSS	P20_13	P20_10	P20_8	P20_6	P20_4	P20_2	P20_0	P2_14	P2_12	P2_10	P2_8	SVRDRVCC	SVRAVCC	P2_2	P2_0	P5_6	VSS	B
C	P10_0	P10_1																	P2_1	P5_4	C
D	P10_2	P10_3		VSS	P21_4	P21_3	P21_2	P21_1	P21_0	P22_2	P22_4	LVDVCC	P2_9	P2_7	P2_5	P2_3	VSS		P5_3	P5_2	D
E	P10_4	P10_5		P21_5	VSS	VCC	VSS	E1VCC	P22_0	P22_1	P22_3	E0VCC	VSS	P2_6	P2_4	VSS	GETH0VCL		PWRCTL	X1	E
F	P10_6	P10_7		P21_6	VSS											SYSVCC	$\overline{\text{VMONOUT}}$		FLMD0	X2	F
G	P10_8	P10_9		P21_7	VCC			VSS	VDD	VDD	VDD	VDD	VDD			VSS	GETH0 PVCC		P3_8	$\overline{\text{RESET}}$	G
H	P10_10	P10_11		P17_6	VSS		VSS		VSS	VSS	VSS	VSS		VSS		TX_DATAP	GETH0 RVCC		$\overline{\text{TRST}}$	JP0_0	H
J	P10_12	P10_13		P17_5	E1VCC		VDD	VSS		VSS	VSS		VSS	VDD		TX_DATAN	RX_DATAP		JP0_1	JP0_2	J
K	P10_14	P17_0		P17_2	VDD		VDD	VSS	VSS	VSS	VSS	VSS	VSS	VDD		GETH0 BVCC	RX_DATAN		JP0_3	JP0_5	K
L	P17_1	AP2_13		P17_4	P17_3		VDD	VSS	VSS	VSS	VSS	VSS	VSS	VDD		P3_7	VSS		P6_14	P6_13	L
M	AP2_10	AP2_11		AP2_14	VCC		VDD	VSS		VSS	VSS		VSS	VDD		E0VCC	P3_6		P6_10	P6_15	M
N	AP2_8	AP2_9		AP2_15	VSS		VSS		VSS	VSS	VSS	VSS		VSS		VSS	P6_0		P6_12	P6_9	N
P	AP2_6	AP2_7		AP3_0	AP3_1			VSS	VDD	VDD	VDD	AWOVCL	VSS			VDD	AP4_1		P6_8	P6_7	P
R	AP2_4	AP2_5		AP3_2	AP2_12											AP4_0	AP4_2		P6_6	P6_5	R
T	AP2_2	AP2_3		AP3_3	A0VSS	A0VSS	AP1_1	AP0_15	AP0_13	E0VCC	P24_7	E2VCC	P24_9	P24_11	AP4_4	A2VSS	AP4_3		P6_4	P6_3	T
U	A1VCC	AP2_1		A0VSS	AP1_3	AP1_2	AP1_0	AP0_14	AP0_12	P24_4	P24_5	P24_6	P24_8	P24_10	P24_12	P24_13	A2VSS		A2VCC	P6_2	U
V	A1VREFH	AP2_0																	A2VREFH	P6_11	V
W	A1VSS	A1VSS	A0VSS	AP0_0	AP0_2	AP0_4	AP0_6	AP0_8	AP0_10	P3_2	P4_0	P4_4	P4_6	P4_8	P4_10	P4_12	P4_14	P3_4	P3_5	A2VSS	W
Y	A1VSS	A0VSS	A0VREFH	A0VCC	AP0_1	AP0_3	AP0_5	AP0_7	AP0_9	AP0_11	P3_3	P4_1	P4_5	P4_7	P4_9	P4_11	P4_13	P4_15	A2VSS	A2VSS	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

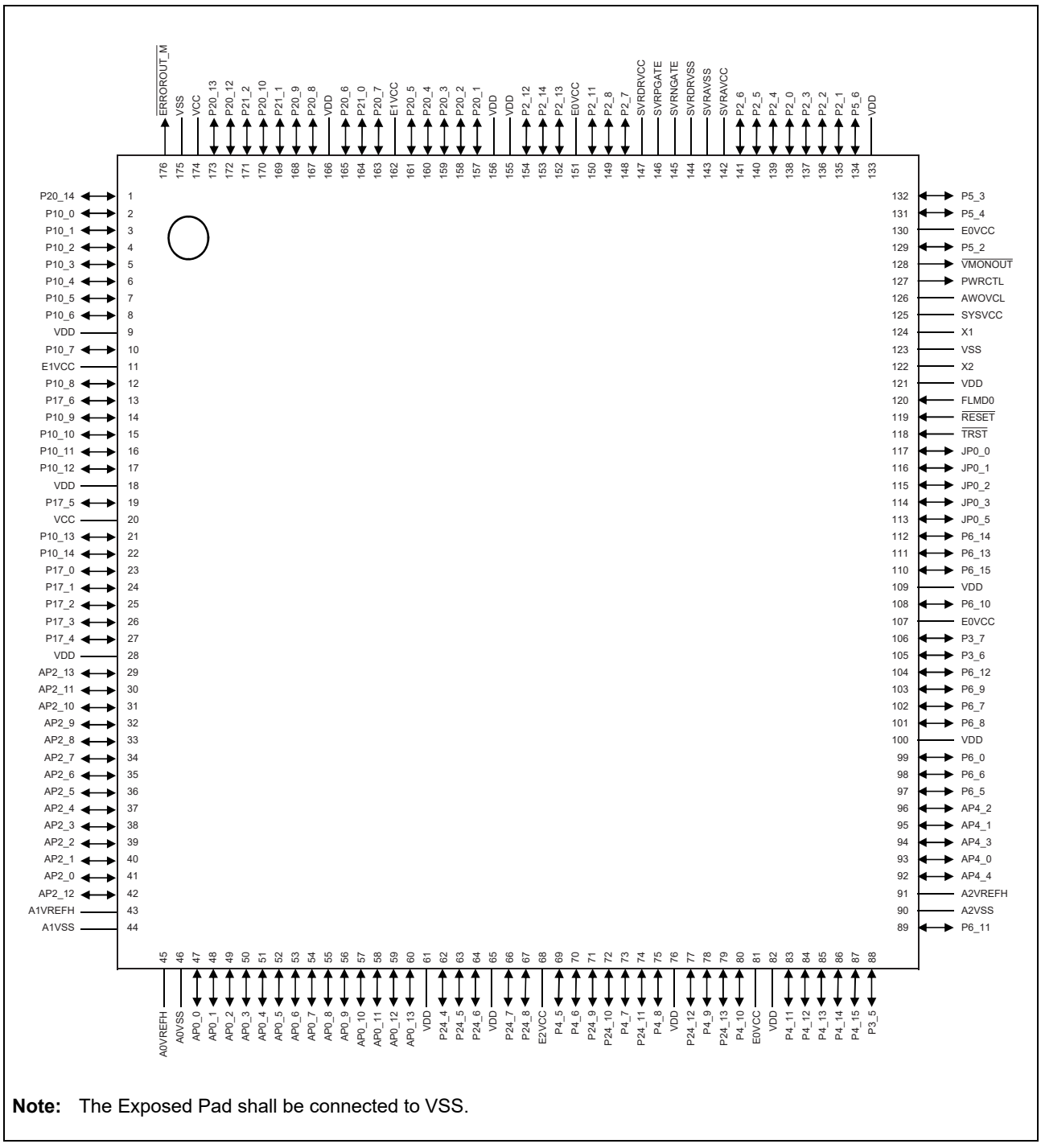
Note: The pin location of RX_DATAP, RX_DATAN, TX_DATAP and TX_DATAN is defined by the Option Byte 14.
For details, refer to RH850/U2A-EVA Group User's Manual: Hardware **Section 51.12.20, OPBT14 — Option Byte 14**.

Figure 1.4 Pin Connection Diagram (BGA292 U2A16/U2A8)



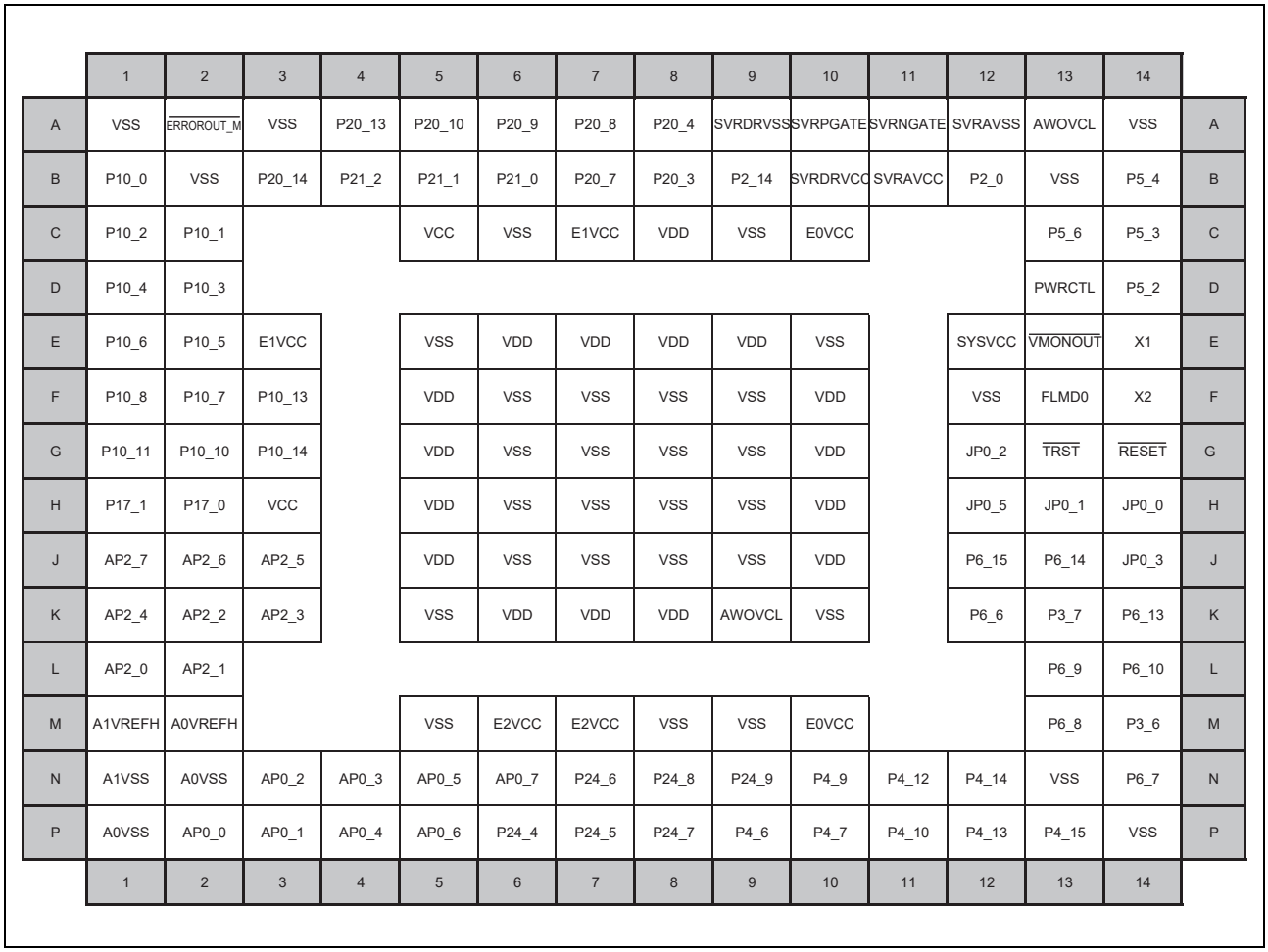
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	VSS	VSS	ERROROUT_M	VSS	P20_12	P20_9	P20_7	P20_5	P20_3	P20_1	P2_15	P2_13	P2_11	SVRDRVSS	SVRPGATE	SVRNGATE	SVRAVSS	AWOVCL	VSS	VSS	A
B	VSS	P20_14	VSS	P20_13	P20_10	P20_8	P20_6	P20_4	P20_2	P20_0	P2_14	P2_12	P2_10	P2_8	SVRDRVCC	SVRAVCC	P2_2	P2_0	P5_6	VSS	B
C	P10_0	P10_1																	P2_1	P5_4	C
D	P10_2	P10_3		VSS	P21_4	P21_3	P21_2	P21_1	P21_0	P22_2	P22_4	E0VCC	P2_9	P2_7	P2_5	P2_3	VSS		P5_3	P5_2	D
E	P10_4	P10_5		P21_5	VSS	VCC	VSS	E1VCC	P22_0	P22_1	P22_3	E0VCC	VSS	P2_6	P2_4	VSS	VSS		PWRCTL	X1	E
F	P10_6	P10_7		P21_6	VSS											SYSVCC	VMONOUT		FLMD0	X2	F
G	P10_8	P10_9		P21_7	VCC			VSS	VDD	VDD	VDD	VDD	VDD			VSS	E0VCC		P3_8	RESET	G
H	P10_10	P10_11		P17_6	VSS		VSS		VSS	VSS	VSS	VSS		VSS		E0VCC	E0VCC		TRST	JP0_0	H
J	P10_12	P10_13		P17_5	E1VCC		VDD	VSS		VSS	VSS		VSS	VDD		E0VCC	VSS		JP0_1	JP0_2	J
K	P10_14	P17_0		P17_2	VDD		VDD	VSS	VSS	VSS	VSS	VSS	VSS	VDD		E0VCC	VSS		JP0_3	JP0_5	K
L	P17_1	AP2_13		P17_4	P17_3		VDD	VSS	VSS	VSS	VSS	VSS	VSS	VDD		P3_7	VSS		P6_14	P6_13	L
M	AP2_10	AP2_11		AP2_14	VCC		VDD	VSS		VSS	VSS		VSS	VDD		E0VCC	P3_6		P6_10	P6_15	M
N	AP2_8	AP2_9		AP2_15	VSS		VSS		VSS	VSS	VSS	VSS		VSS		VSS	P6_0		P6_12	P6_9	N
P	AP2_6	AP2_7		AP3_0	AP3_1			VSS	VDD	VDD	VDD	AWOVCL	VSS			VDD	AP4_1		P6_8	P6_7	P
R	AP2_4	AP2_5		AP3_2	AP2_12											AP4_0	AP4_2		P6_6	P6_5	R
T	AP2_2	AP2_3		AP3_3	A0VSS	A0VSS	AP1_1	AP0_15	AP0_13	E0VCC	P24_7	E2VCC	P24_9	P24_11	AP4_4	A2VSS	AP4_3		P6_4	P6_3	T
U	A1VCC	AP2_1		A0VSS	AP1_3	AP1_2	AP1_0	AP0_14	AP0_12	P24_4	P24_5	P24_6	P24_8	P24_10	P24_12	P24_13	A2VSS		A2VCC	P6_2	U
V	A1VREFH	AP2_0																	A2VREFH	P6_11	V
W	A1VSS	A1VSS	A0VSS	AP0_0	AP0_2	AP0_4	AP0_6	AP0_8	AP0_10	P3_2	P4_0	P4_4	P4_6	P4_8	P4_10	P4_12	P4_14	P3_4	P3_5	A2VSS	W
Y	A1VSS	A0VSS	A0VREFH	A0VCC	AP0_1	AP0_3	AP0_5	AP0_7	AP0_9	AP0_11	P3_3	P4_1	P4_5	P4_7	P4_9	P4_11	P4_13	P4_15	A2VSS	A2VSS	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

Figure 1.5 Pin Connection Diagram (BGA292 U2A6)



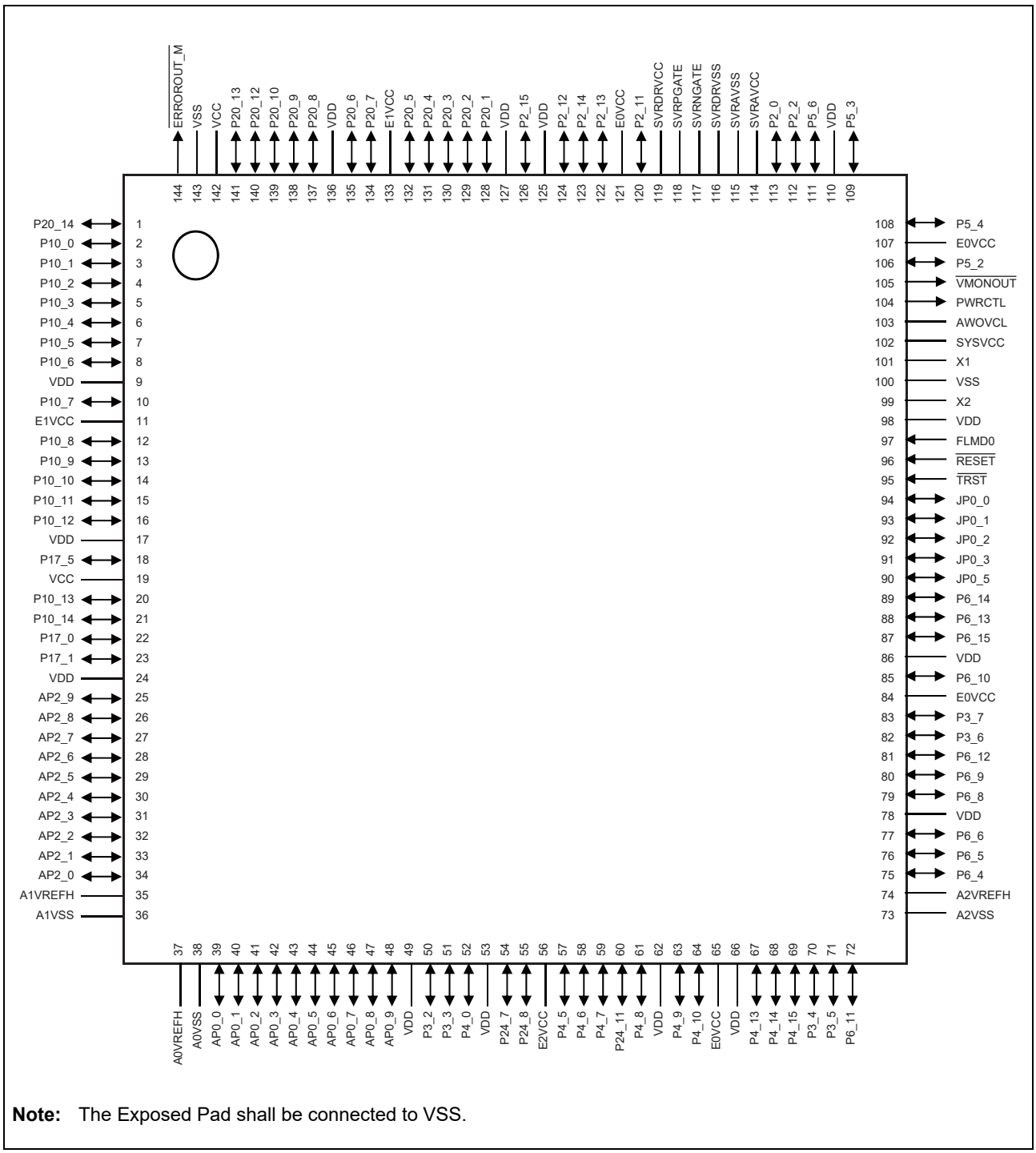
Note: The Exposed Pad shall be connected to VSS.

Figure 1.6 Pin Connection Diagram (QFP176 U2A6)



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	VSS	$\overline{\text{ERROROUT\_M}}$	VSS	P20_13	P20_10	P20_9	P20_8	P20_4	SVRDRVSS	SVRPGATE	SVRNGATE	SVRAVSS	AWOVCL	VSS	A
B	P10_0	VSS	P20_14	P21_2	P21_1	P21_0	P20_7	P20_3	P2_14	SVRDRVCC	SVRAVCC	P2_0	VSS	P5_4	B
C	P10_2	P10_1			VCC	VSS	E1VCC	VDD	VSS	E0VCC			P5_6	P5_3	C
D	P10_4	P10_3											PWRCTL	P5_2	D
E	P10_6	P10_5	E1VCC		VSS	VDD	VDD	VDD	VDD	VSS		SYSVCC	$\overline{\text{VMONOUT}}$	X1	E
F	P10_8	P10_7	P10_13		VDD	VSS	VSS	VSS	VSS	VDD		VSS	FLMD0	X2	F
G	P10_11	P10_10	P10_14		VDD	VSS	VSS	VSS	VSS	VDD		JP0_2	$\overline{\text{TRST}}$	$\overline{\text{RESET}}$	G
H	P17_1	P17_0	VCC		VDD	VSS	VSS	VSS	VSS	VDD		JP0_5	JP0_1	JP0_0	H
J	AP2_7	AP2_6	AP2_5		VDD	VSS	VSS	VSS	VSS	VDD		P6_15	P6_14	JP0_3	J
K	AP2_4	AP2_2	AP2_3		VSS	VDD	VDD	VDD	AWOVCL	VSS		P6_6	P3_7	P6_13	K
L	AP2_0	AP2_1											P6_9	P6_10	L
M	A1VREFH	A0VREFH			VSS	E2VCC	E2VCC	VSS	VSS	E0VCC			P6_8	P3_6	M
N	A1VSS	A0VSS	AP0_2	AP0_3	AP0_5	AP0_7	P24_6	P24_8	P24_9	P4_9	P4_12	P4_14	VSS	P6_7	N
P	A0VSS	AP0_0	AP0_1	AP0_4	AP0_6	P24_4	P24_5	P24_7	P4_6	P4_7	P4_10	P4_13	P4_15	VSS	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Figure 1.7 Pin Connection Diagram (BGA156 U2A6)



Note: The Exposed Pad shall be connected to VSS.

Figure 1.8 Pin Connection Diagram (QFP144 U2A6)

1.6 Functional Block Configuration

Internal Block Diagram

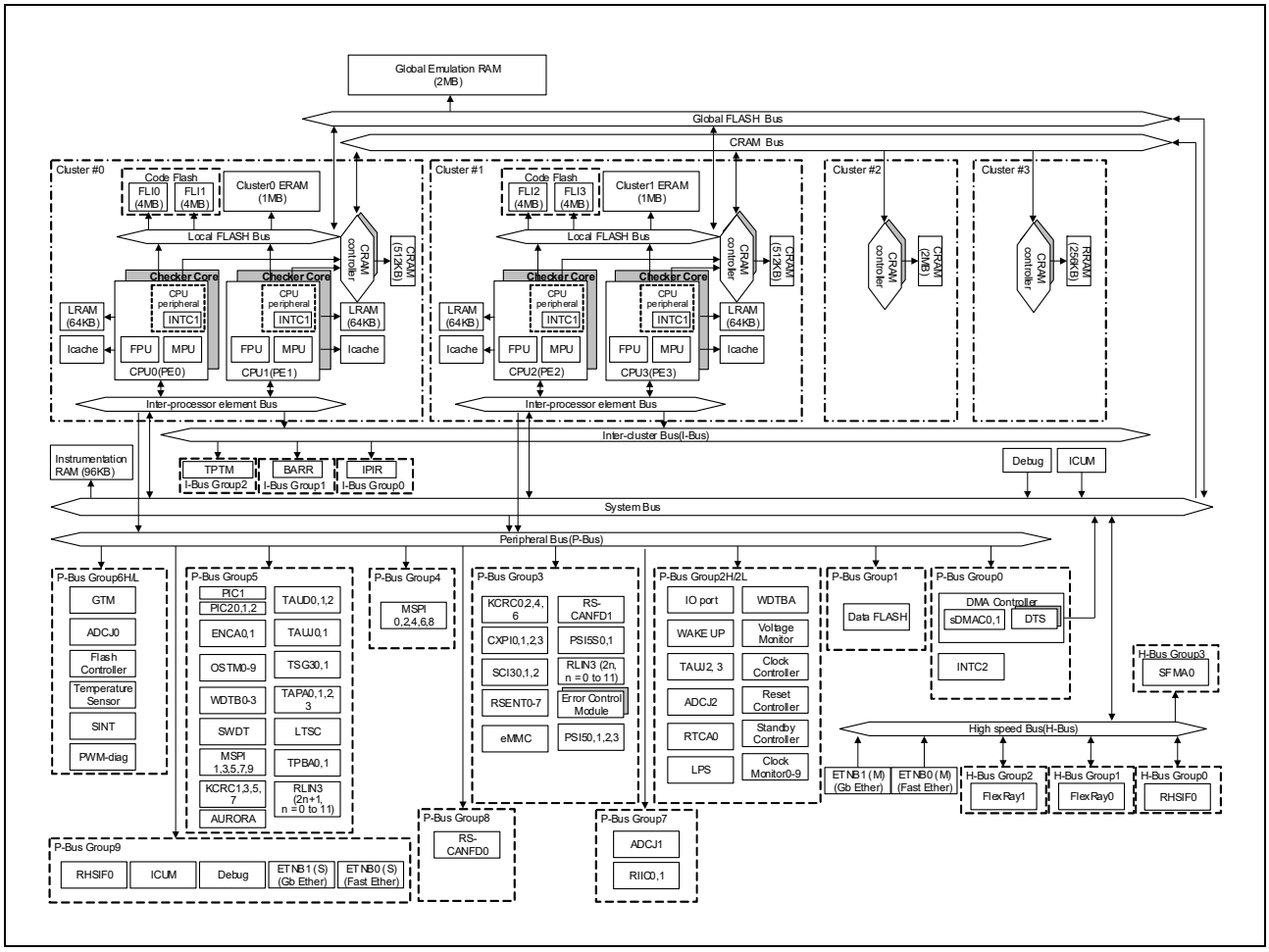


Figure 1.9 Internal Block Diagram (U2A-EVA 516 pins)

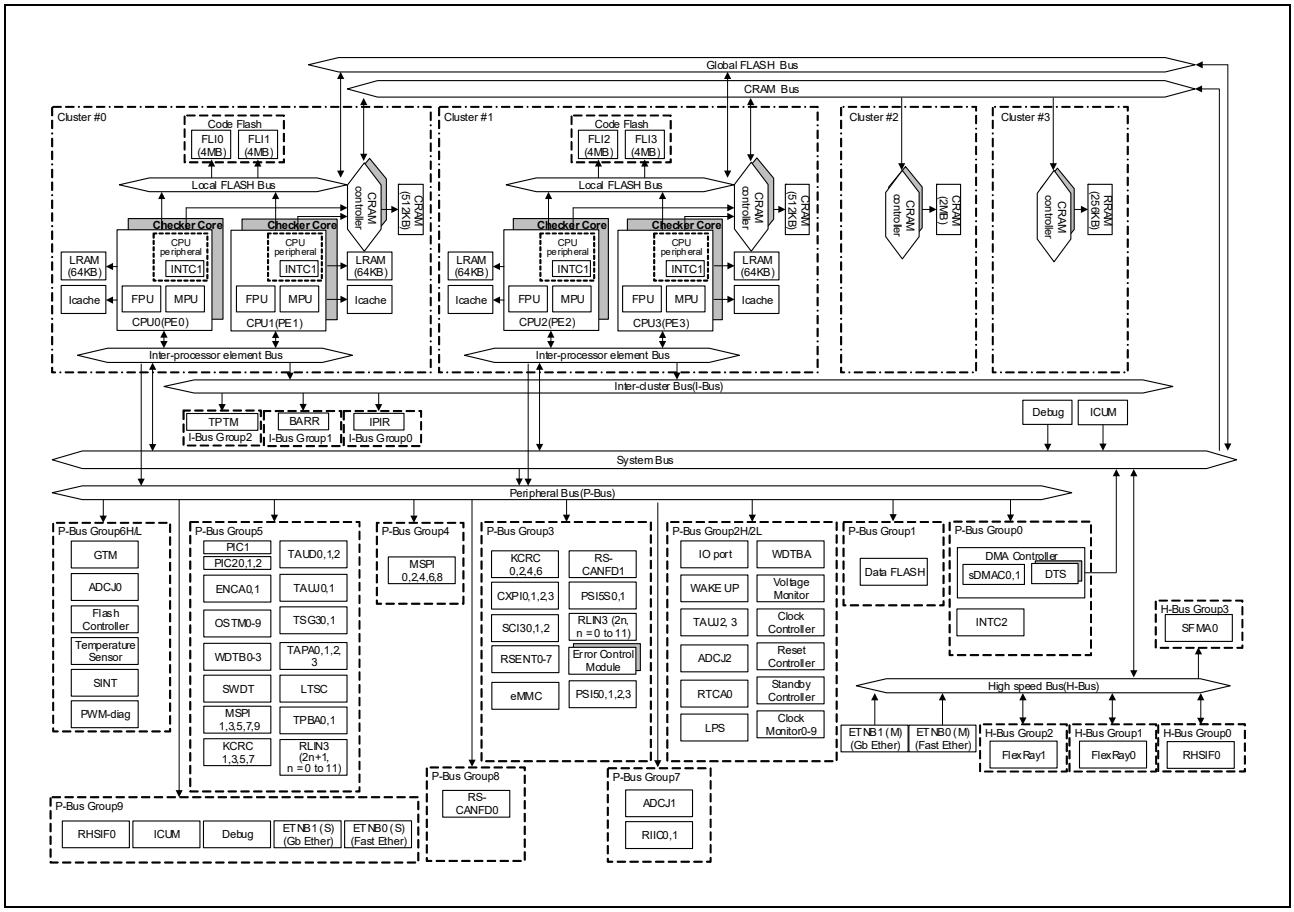


Figure 1.10 Internal Block Diagram (U2A16 516 pins)

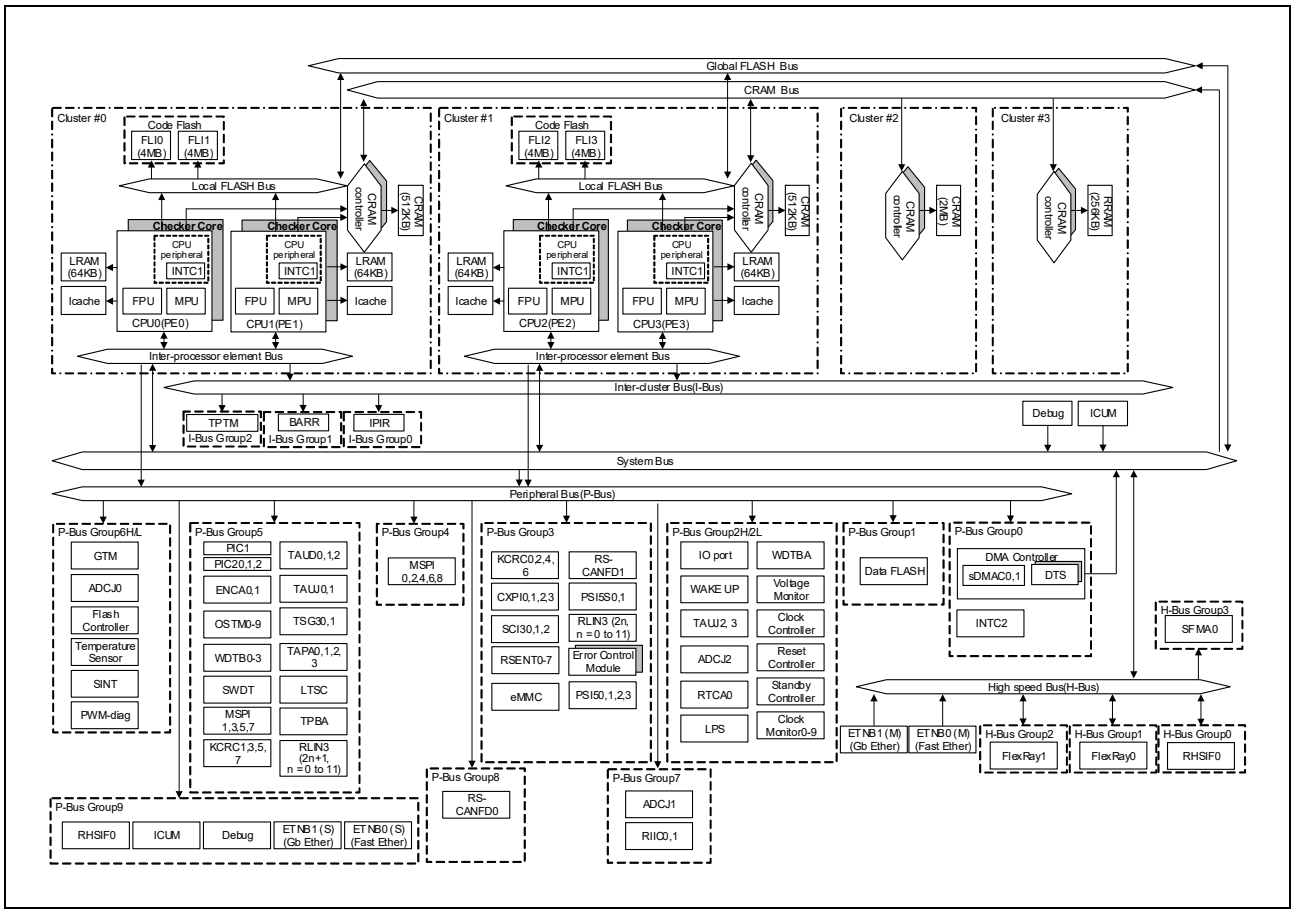


Figure 1.11 Internal Block Diagram (U2A16 373 pins)

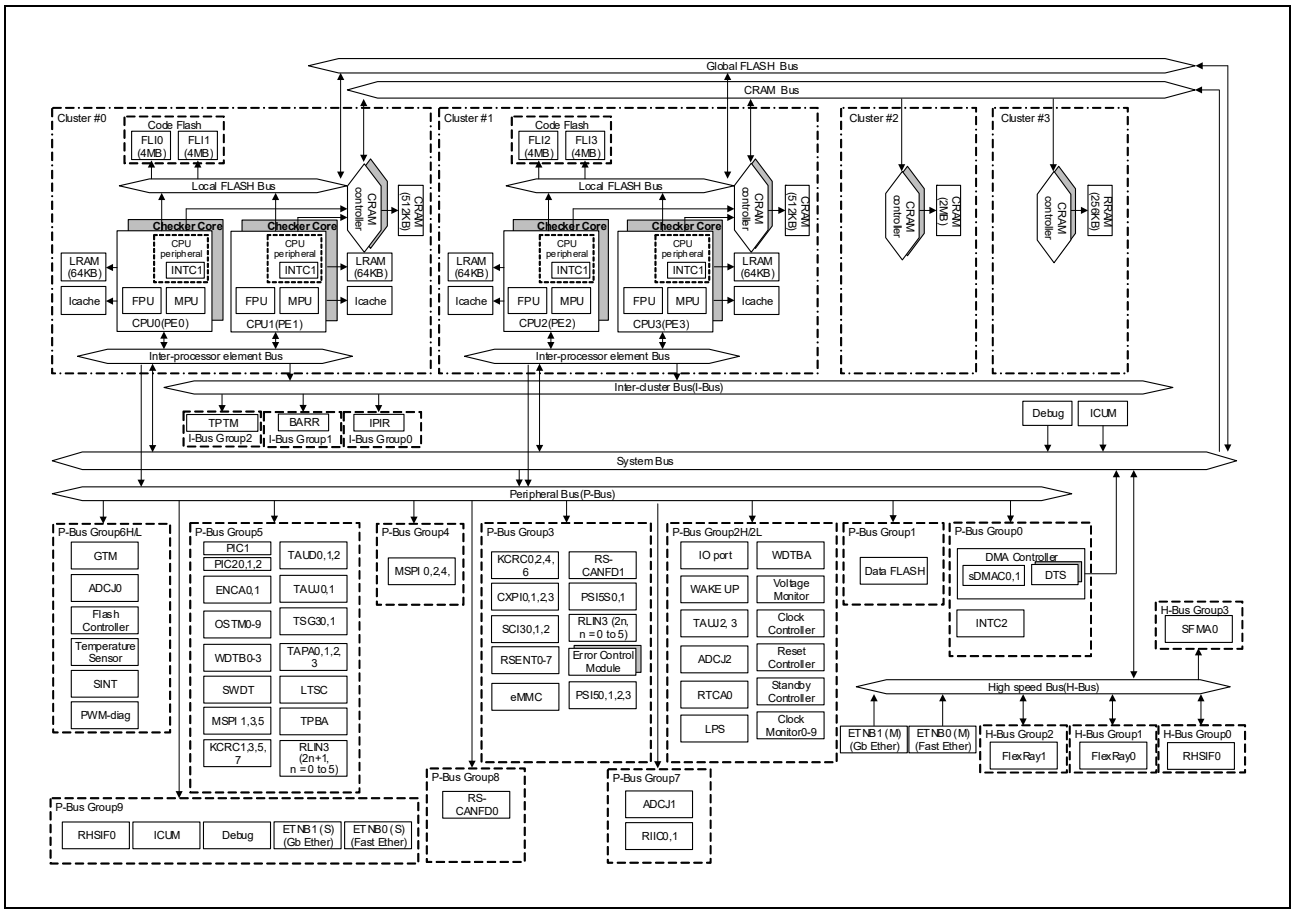


Figure 1.12 Internal Block Diagram (U2A16 292 pins)

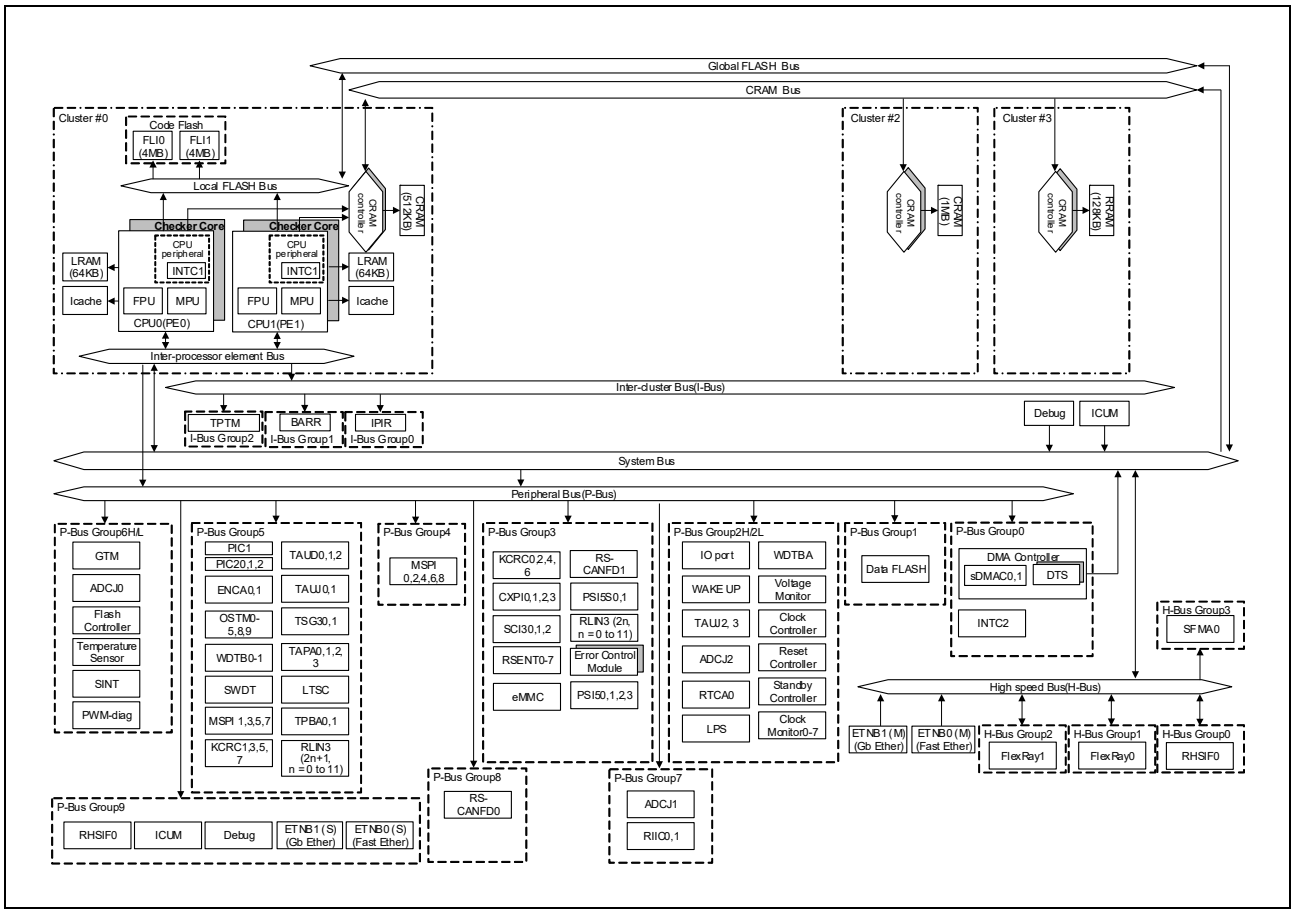


Figure 1.13 Internal Block Diagram (U2A8 373 pins)

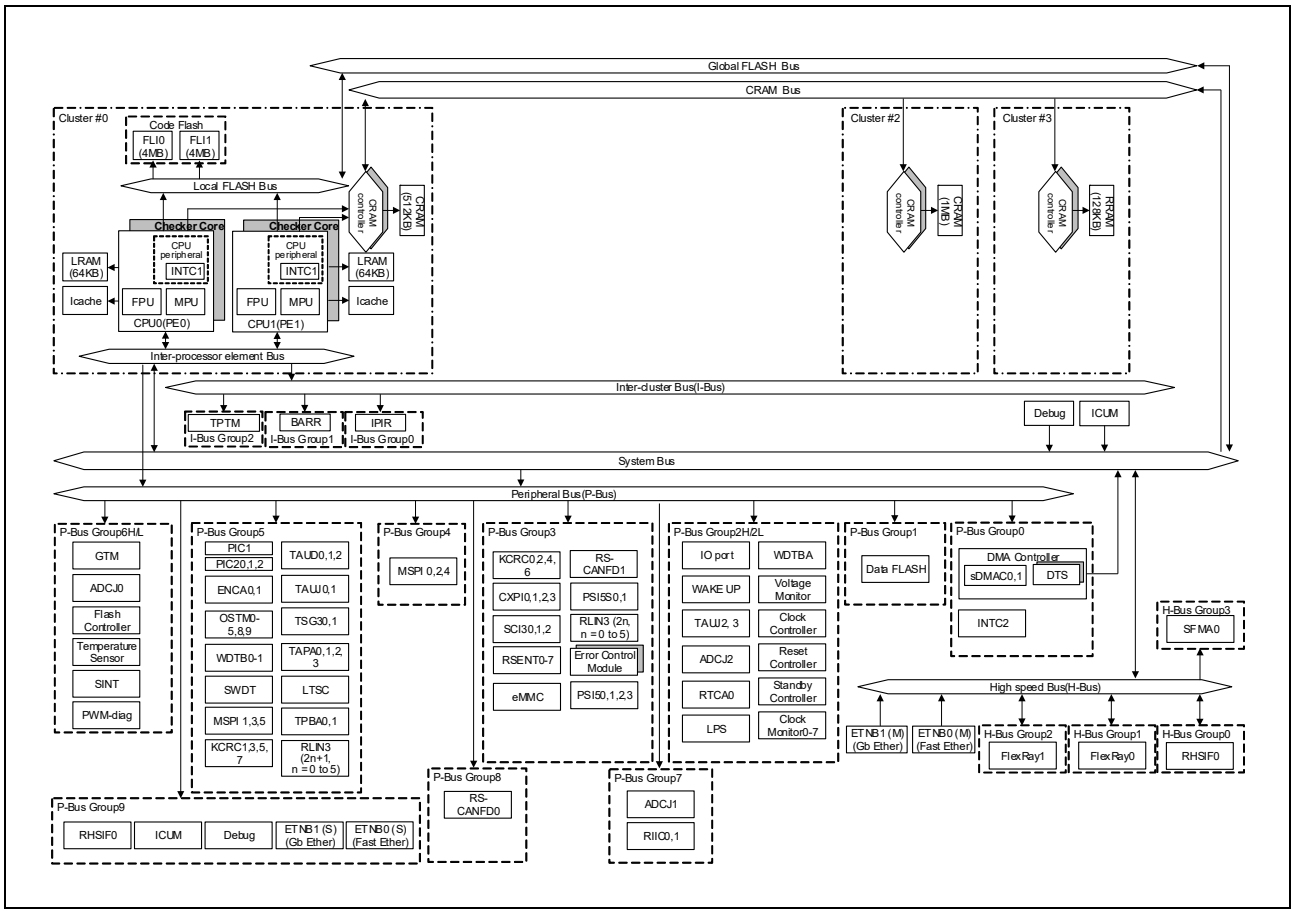


Figure 1.14 Internal Block Diagram (U2A8 292 pins)

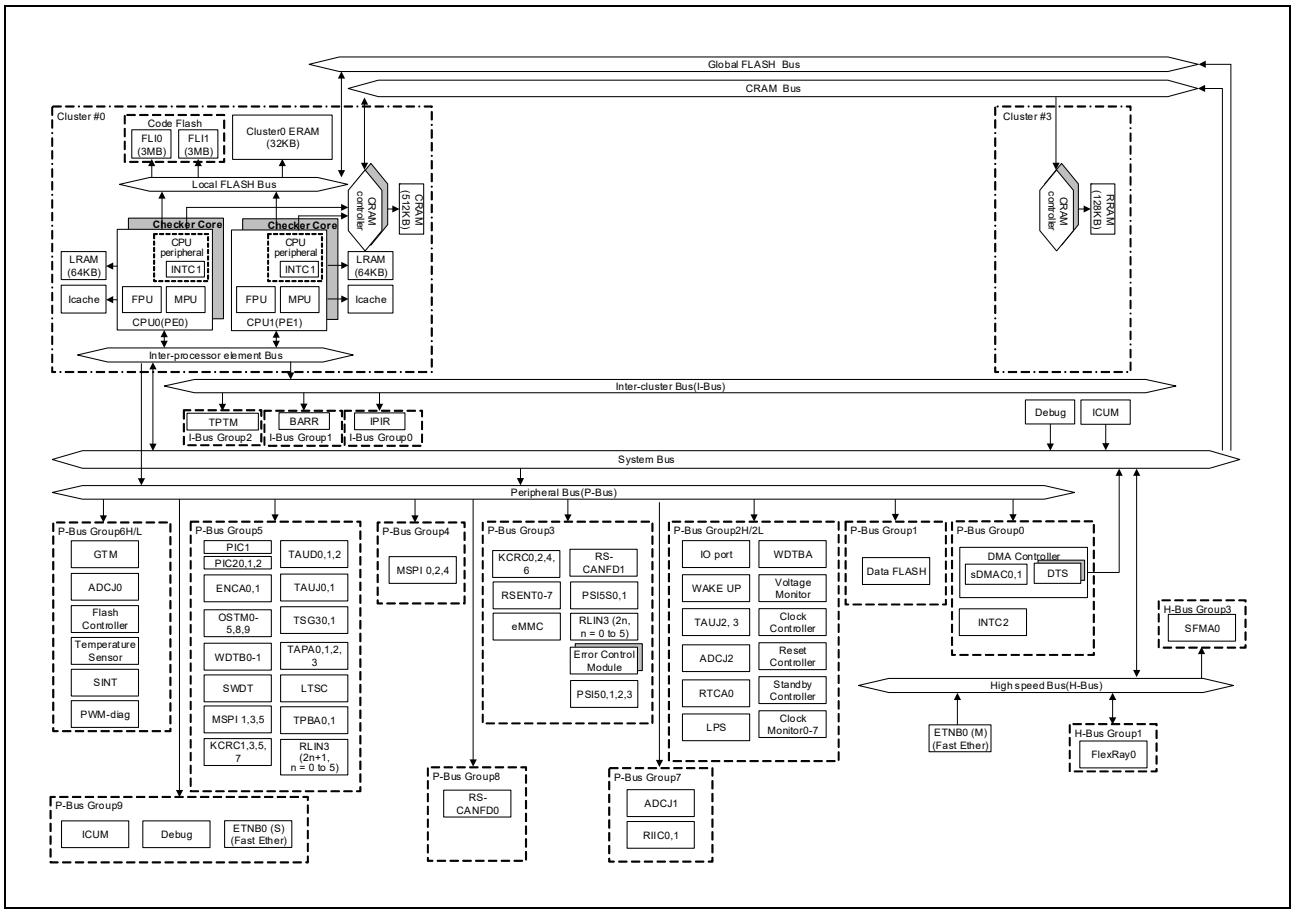


Figure 1.15 Internal Block Diagram (U2A6 292 pins)

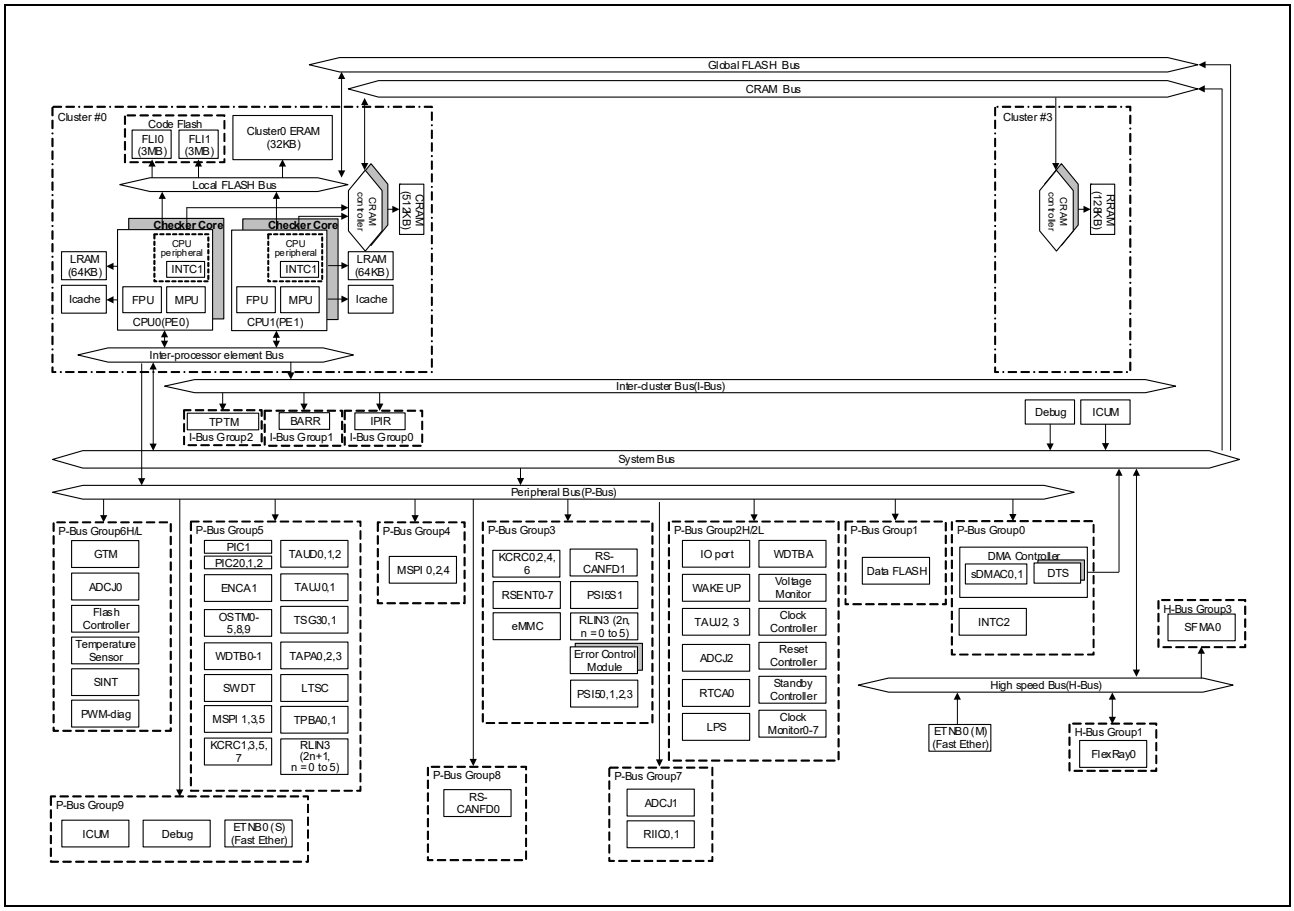


Figure 1.16 Internal Block Diagram (U2A6 176 pins)

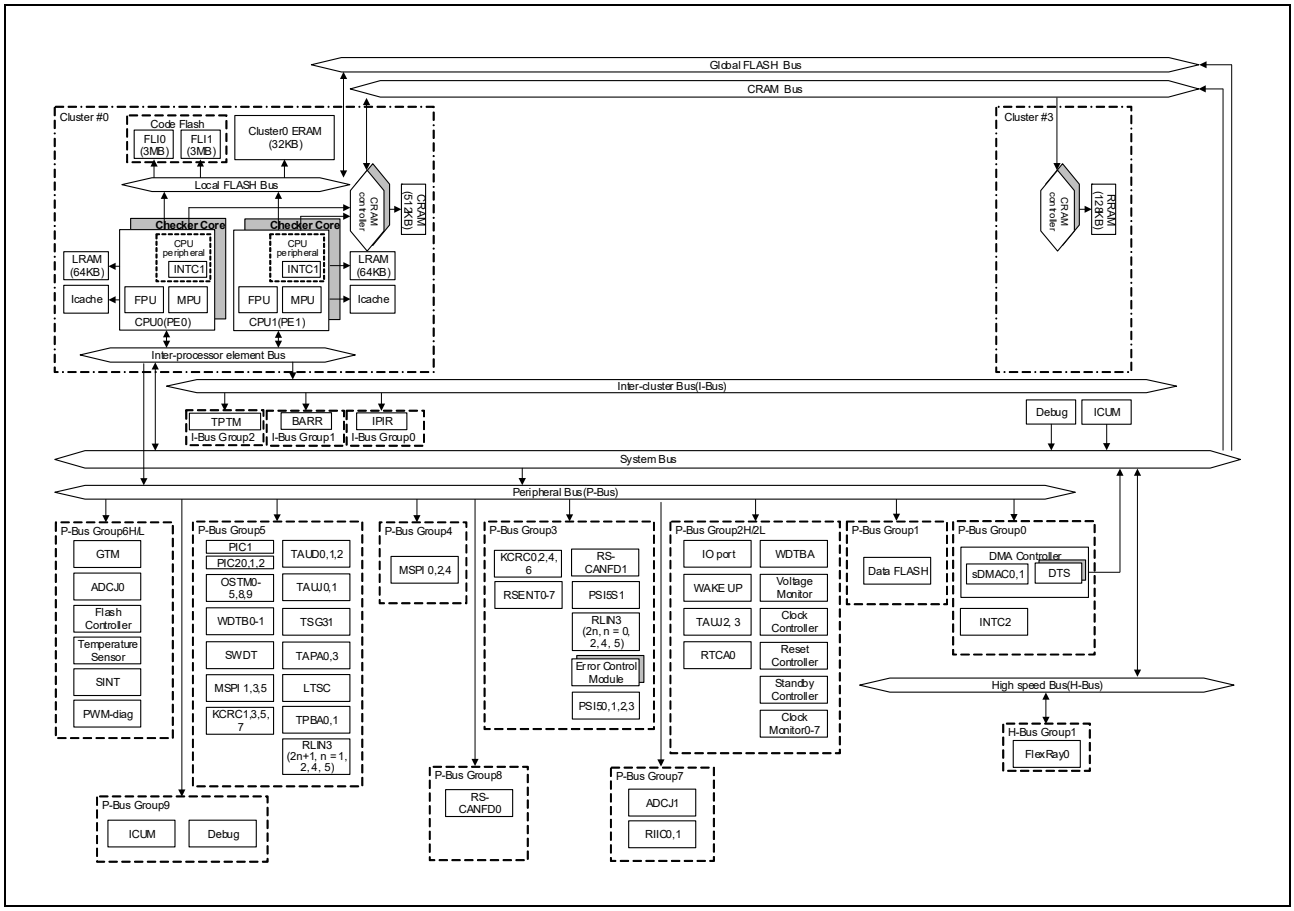


Figure 1.17 Internal Block Diagram (U2A6 156 pins)

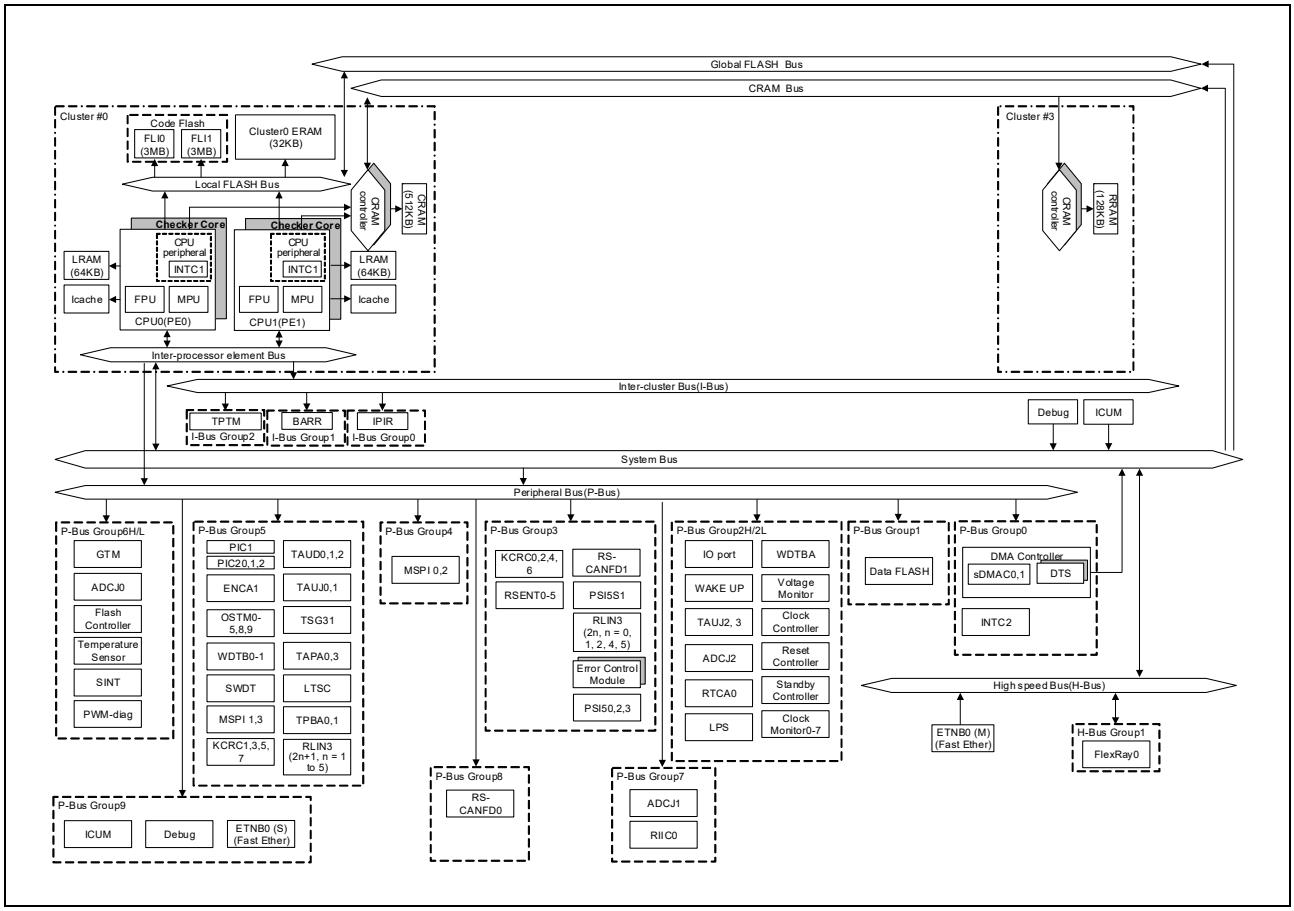


Figure 1.18 Internal Block Diagram (U2A6 144 pins)

Each CPU has its own set of CPU peripherals. These CPU peripherals are assigned to the common address: CPU peripheral (self), separately from their respective address. For example, access by CPU0 to a register of a CPU peripheral (self) is to the register in the CPU peripheral of CPU0; access by CPU1 to a register of a CPU peripheral (self) is to the register in the CPU peripheral of CPU1.

Section 2 Pin Functions

2.1 Pin List

2.1.1 Pin List and Function assignment

For detailed information, refer to Appendix “E02_01_List_of_Pin_Assignment.xlsx”.

2.1.2 Pin Function name

Table 2.1 Pin Function Name Definition (1/35)

Category	Function name	I/O	Explanation	RH850/ U2A-EVA (BGA516)	RH850/ U2A16 (BGA516)	RH850/ U2A16 (BGA373)	RH850/ U2A16 (BGA292)	RH850/ U2A8 (BGA373)	RH850/ U2A8 (BGA292)	RH850/ U2A6 (BGA292)	RH850/ U2A6 (QFP176)	RH850/ U2A6 (BGA156)	RH850/ U2A6 (QFP144)
Port	JP0_0	IO	Port of JTAG port group 0	√	√	√	√	√	√	√	√	√	√
	JP0_1	IO		√	√	√	√	√	√	√	√	√	√
	JP0_2	IO		√	√	√	√	√	√	√	√	√	√
	JP0_3	IO		√	√	√	√	√	√	√	√	√	√
	JP0_5	IO		√	√	√	√	√	√	√	√	√	√
	P0_0	IO	Port of port group 0	√	√	√		√					
	P0_1	IO		√	√	√		√					
	P0_2	IO		√	√	√		√					
	P0_3	IO		√	√	√		√					
	P0_4	IO		√	√	√		√					
	P0_5	IO		√	√	√		√					
	P0_6	IO		√	√	√		√					
	P0_7	IO		√	√	√		√					
	P0_8	IO		√	√	√		√					
	P0_9	IO		√	√	√		√					
	P0_10	IO		√	√	√		√					
	P0_11	IO		√	√	√		√					
	P0_12	IO		√	√	√		√					
	P1_0	IO	Port of port group 1	√	√								
	P1_1	IO		√	√								
	P1_2	IO		√	√								
	P1_3	IO		√	√								
	P1_4	IO		√	√								
	P1_5	IO		√	√								
	P1_6	IO		√	√								
	P1_7	IO		√	√								
	P1_8	IO		√	√								
	P1_9	IO		√	√								
	P1_10	IO		√	√								
	P1_11	IO		√	√								
	P1_12	IO		√	√								
	P1_13	IO		√	√								
	P1_14	IO		√	√								
	P1_15	IO		√	√								
	P2_0	IO	Port of port group 2	√	√	√	√	√	√	√	√	√	√
	P2_1	IO		√	√	√	√	√	√	√	√		
	P2_2	IO		√	√	√	√	√	√	√	√		√
	P2_3	IO		√	√	√	√	√	√	√	√		
	P2_4	IO		√	√	√	√	√	√	√	√		
	P2_5	IO		√	√	√	√	√	√	√	√		
	P2_6	IO		√	√	√	√	√	√	√	√		
	P2_7	IO		√	√	√	√	√	√	√	√		
	P2_8	IO		√	√	√	√	√	√	√	√		

Table 2.1 Pin Function Name Definition (2/35)

Category	Function name	I/O	Explanation	RH850/ U2A-EVA (BGA516)	RH850/ U2A16 (BGA516)	RH850/ U2A16 (BGA373)	RH850/ U2A16 (BGA292)	RH850/ U2A8 (BGA373)	RH850/ U2A8 (BGA292)	RH850/ U2A6 (BGA292)	RH850/ U2A6 (QFP176)	RH850/ U2A6 (BGA156)	RH850/ U2A6 (QFP144)
Port	P2_9	IO	Port of port group 2	√	√	√	√	√	√	√			
	P2_10	IO		√	√	√	√	√	√	√			
	P2_11	IO		√	√	√	√	√	√	√	√		√
	P2_12	IO		√	√	√	√	√	√	√	√		√
	P2_13	IO		√	√	√	√	√	√	√	√		√
	P2_14	IO		√	√	√	√	√	√	√	√	√	√
	P2_15	IO		√	√	√	√	√	√	√			√
	P3_0	IO	Port of port group 3	√	√	√		√					
	P3_1	IO		√	√	√		√					
	P3_2	IO		√	√	√	√	√	√	√			√
	P3_3	IO		√	√	√	√	√	√	√			√
	P3_4	IO		√	√	√	√	√	√	√			√
	P3_5	IO		√	√	√	√	√	√	√	√		√
	P3_6	IO		√	√	√	√	√	√	√	√	√	√
	P3_7	IO		√	√	√	√	√	√	√	√	√	√
	P3_8	IO		√	√	√	√	√	√	√			
	P3_9	IO		√	√								
	P3_10	IO		√	√								
	P3_11	IO		√	√								
	P3_12	IO		√	√								
	P3_13	IO		√	√								
	P3_14	IO		√	√								
	P3_15	IO		√	√								
	P4_0	IO	Port of port group 4	√	√	√	√	√	√	√			√
	P4_1	IO		√	√	√	√	√	√	√			
	P4_2	IO		√	√								
	P4_3	IO		√	√								
	P4_4	IO		√	√	√	√	√	√	√			
	P4_5	IO		√	√	√	√	√	√	√	√		√
	P4_6	IO		√	√	√	√	√	√	√	√	√	√
	P4_7	IO		√	√	√	√	√	√	√	√	√	√
	P4_8	IO		√	√	√	√	√	√	√	√		√
	P4_9	IO		√	√	√	√	√	√	√	√	√	√
	P4_10	IO		√	√	√	√	√	√	√	√	√	√
	P4_11	IO		√	√	√	√	√	√	√	√		
	P4_12	IO		√	√	√	√	√	√	√	√	√	
	P4_13	IO		√	√	√	√	√	√	√	√	√	√
	P4_14	IO		√	√	√	√	√	√	√	√	√	√
	P4_15	IO		√	√	√	√	√	√	√	√	√	√
	P5_2	IO	Port of port group 5	√	√	√	√	√	√	√	√	√	√
	P5_3	IO		√	√	√	√	√	√	√	√	√	√
	P5_4	IO		√	√	√	√	√	√	√	√	√	√
	P5_6	IO		√	√	√	√	√	√	√	√	√	√

Table 2.1 Pin Function Name Definition (3/35)

Category	Function name	I/O	Explanation	RH850/ U2A-EVA (BGA516)	RH850/ U2A16 (BGA516)	RH850/ U2A16 (BGA373)	RH850/ U2A16 (BGA292)	RH850/ U2A8 (BGA373)	RH850/ U2A8 (BGA292)	RH850/ U2A6 (BGA292)	RH850/ U2A6 (QFP176)	RH850/ U2A6 (BGA156)	RH850/ U2A6 (QFP144)
Port	P6_0	IO	Port of port group 6	√	√	√	√	√	√	√	√		
	P6_2	IO		√	√	√	√	√	√	√			
	P6_3	IO		√	√	√	√	√	√	√			
	P6_4	IO		√	√	√	√	√	√	√			√
	P6_5	IO		√	√	√	√	√	√	√	√		√
	P6_6	IO		√	√	√	√	√	√	√	√	√	√
	P6_7	IO		√	√	√	√	√	√	√	√	√	
	P6_8	IO		√	√	√	√	√	√	√	√	√	√
	P6_9	IO		√	√	√	√	√	√	√	√	√	√
	P6_10	IO		√	√	√	√	√	√	√	√	√	√
	P6_11	IO		√	√	√	√	√	√	√	√		√
	P6_12	IO		√	√	√	√	√	√	√	√		√
	P6_13	IO		√	√	√	√	√	√	√	√	√	√
	P6_14	IO		√	√	√	√	√	√	√	√	√	√
	P6_15	IO		√	√	√	√	√	√	√	√	√	√
	P8_0	IO	Port of port group 8	√	√	√		√					
	P8_1	IO		√	√	√		√					
	P8_2	IO		√	√	√		√					
	P8_3	IO		√	√	√		√					
	P8_4	IO		√	√	√		√					
	P8_5	IO		√	√	√		√					
	P8_6	IO		√	√	√		√					
	P8_7	IO		√	√	√		√					
	P8_8	IO		√	√	√		√					
	P8_9	IO		√	√	√		√					
	P8_10	IO		√	√								
	P9_0	IO	Port of port group 9	√	√								
	P9_1	IO		√	√								
	P9_2	IO		√	√								
	P9_3	IO		√	√								
	P9_4	IO		√	√								
	P9_5	IO		√	√								
	P9_6	IO		√	√								
	P9_7	IO		√	√								
	P9_8	IO		√	√								
	P10_0	IO	Port of port group 10	√	√	√	√	√	√	√	√	√	√
	P10_1	IO		√	√	√	√	√	√	√	√	√	√
	P10_2	IO		√	√	√	√	√	√	√	√	√	√
	P10_3	IO		√	√	√	√	√	√	√	√	√	√
	P10_4	IO		√	√	√	√	√	√	√	√	√	√
	P10_5	IO		√	√	√	√	√	√	√	√	√	√
	P10_6	IO		√	√	√	√	√	√	√	√	√	√
	P10_7	IO		√	√	√	√	√	√	√	√	√	√
	P10_8	IO		√	√	√	√	√	√	√	√	√	√
	P10_9	IO		√	√	√	√	√	√	√	√		√

Table 2.1 Pin Function Name Definition (4/35)

Category	Function name	I/O	Explanation	RH850/ U2A-EVA (BGA516)	RH850/ U2A16 (BGA516)	RH850/ U2A16 (BGA373)	RH850/ U2A16 (BGA292)	RH850/ U2A8 (BGA373)	RH850/ U2A8 (BGA292)	RH850/ U2A6 (BGA292)	RH850/ U2A6 (QFP176)	RH850/ U2A6 (BGA156)	RH850/ U2A6 (QFP144)
Port	P10_10	IO	Port of port group 10	√	√	√	√	√	√	√	√	√	√
	P10_11	IO		√	√	√	√	√	√	√	√	√	√
	P10_12	IO		√	√	√	√	√	√	√	√		√
	P10_13	IO		√	√	√	√	√	√	√	√	√	√
	P10_14	IO		√	√	√	√	√	√	√	√	√	√
	P11_0	IO	Port of port group 11	√	√	√		√					
	P11_1	IO		√	√	√		√					
	P11_2	IO		√	√	√		√					
	P11_3	IO		√	√	√		√					
	P11_4	IO		√	√	√		√					
	P11_5	IO		√	√	√		√					
	P11_6	IO		√	√	√		√					
	P11_7	IO		√	√	√		√					
	P11_8	IO		√	√	√		√					
	P11_9	IO		√	√	√		√					
	P11_10	IO		√	√	√		√					
	P11_11	IO		√	√	√		√					
	P11_12	IO		√	√	√		√					
	P11_13	IO		√	√	√		√					
	P11_14	IO		√	√	√		√					
	P11_15	IO		√	√	√		√					
	P12_0	IO	Port of port group 12	√	√								
	P12_1	IO		√	√								
	P12_2	IO		√	√								
	P12_3	IO		√	√								
	P12_4	IO		√	√								
	P12_5	IO		√	√								
	P17_0	IO	Port of port group 17	√	√	√	√	√	√	√	√	√	√
	P17_1	IO		√	√	√	√	√	√	√	√	√	√
	P17_2	IO		√	√	√	√	√	√	√	√		
	P17_3	IO		√	√	√	√	√	√	√	√		
	P17_4	IO		√	√	√	√	√	√	√	√		
	P17_5	IO		√	√	√	√	√	√	√	√		√
	P17_6	IO		√	√	√	√	√	√	√	√		
	P18_0	IO	Port of port group 18	√	√								
	P18_1	IO		√	√								
	P18_2	IO		√	√								
	P18_3	IO		√	√								
	P18_4	IO		√	√								
	P18_5	IO		√	√								
	P18_6	IO		√	√								
	P18_7	IO		√	√								
	P18_8	IO		√	√								
	P18_9	IO		√	√								
	P18_10	IO		√	√								

Table 2.1 Pin Function Name Definition (5/35)

Category	Function name	I/O	Explanation	RH850/ U2A-EVA (BGA516)	RH850/ U2A16 (BGA516)	RH850/ U2A16 (BGA373)	RH850/ U2A16 (BGA292)	RH850/ U2A8 (BGA373)	RH850/ U2A8 (BGA292)	RH850/ U2A6 (BGA292)	RH850/ U2A6 (QFP176)	RH850/ U2A6 (BGA156)	RH850/ U2A6 (QFP144)
Port	P18_11	IO	Port of port group 18	√	√								
	P18_12	IO		√	√								
	P18_13	IO		√	√								
	P18_14	IO		√	√								
	P18_15	IO		√	√								
	P19_0	IO	Port of port group 19	√	√								
	P19_1	IO		√	√								
	P19_2	IO		√	√								
	P19_3	IO		√	√								
	P19_4	IO		√	√								
	P19_5	IO		√	√								
	P20_0	IO	Port of port group 20	√	√	√	√	√	√	√			
	P20_1	IO		√	√	√	√	√	√	√	√		√
	P20_2	IO		√	√	√	√	√	√	√	√		√
	P20_3	IO		√	√	√	√	√	√	√	√	√	√
	P20_4	IO		√	√	√	√	√	√	√	√	√	√
	P20_5	IO		√	√	√	√	√	√	√	√		√
	P20_6	IO		√	√	√	√	√	√	√	√		√
	P20_7	IO		√	√	√	√	√	√	√	√	√	√
	P20_8	IO		√	√	√	√	√	√	√	√	√	√
	P20_9	IO		√	√	√	√	√	√	√	√	√	√
	P20_10	IO		√	√	√	√	√	√	√	√	√	√
	P20_12	IO		√	√	√	√	√	√	√	√		√
	P20_13	IO		√	√	√	√	√	√	√	√	√	√
	P20_14	IO		√	√	√	√	√	√	√	√	√	√
	P20_15	IO		√	√								
	P21_0	IO	Port of port group 21	√	√	√	√	√	√	√	√	√	
	P21_1	IO		√	√	√	√	√	√	√	√	√	
	P21_2	IO		√	√	√	√	√	√	√	√	√	
	P21_3	IO		√	√	√	√	√	√	√			
	P21_4	IO		√	√	√	√	√	√	√			
	P21_5	IO		√	√	√	√	√	√	√			
	P21_6	IO		√	√	√	√	√	√	√			
	P21_7	IO		√	√	√	√	√	√	√			
	P21_12	IO		√	√								
	P21_13	IO		√	√								
	P22_0	IO	Port of port group 22	√	√	√	√	√	√	√			
	P22_1	IO		√	√	√	√	√	√	√			
	P22_2	IO		√	√	√	√	√	√	√			
	P22_3	IO		√	√	√	√	√	√	√			
	P22_4	IO		√	√	√	√	√	√	√			
	P23_0	IO	Port of port group 23	√	√								
	P23_1	IO		√	√								
	P23_2	IO		√	√								
	P23_3	IO		√	√								

Table 2.1 Pin Function Name Definition (6/35)

Category	Function name	I/O	Explanation	RH850/ U2A-EVA (BGA516)	RH850/ U2A16 (BGA516)	RH850/ U2A16 (BGA373)	RH850/ U2A16 (BGA292)	RH850/ U2A8 (BGA373)	RH850/ U2A8 (BGA292)	RH850/ U2A6 (BGA292)	RH850/ U2A6 (QFP176)	RH850/ U2A6 (BGA156)	RH850/ U2A6 (QFP144)
Port	P23_4	IO	Port of port group 23	√	√								
	P23_5	IO		√	√								
	P23_6	IO		√	√								
	P23_7	IO		√	√								
	P23_8	IO		√	√								
	P23_9	IO		√	√								
	P23_10	IO		√	√								
	P23_11	IO		√	√								
	P23_12	IO		√	√								
	P23_13	IO		√	√								
	P24_4	IO	Port of port group 24	√	√	√	√	√	√	√	√	√	
	P24_5	IO		√	√	√	√	√	√	√	√	√	
	P24_6	IO		√	√	√	√	√	√	√	√	√	
	P24_7	IO		√	√	√	√	√	√	√	√	√	√
	P24_8	IO		√	√	√	√	√	√	√	√	√	√
	P24_9	IO		√	√	√	√	√	√	√	√	√	
	P24_10	IO		√	√	√	√	√	√	√	√		
	P24_11	IO		√	√	√	√	√	√	√	√		√
	P24_12	IO		√	√	√	√	√	√	√	√		
	P24_13	IO		√	√	√	√	√	√	√	√		
	AP0_0	IO	Port of analog port group 0	√	√	√	√	√	√	√	√	√	√
	AP0_1	IO		√	√	√	√	√	√	√	√	√	√
	AP0_2	IO		√	√	√	√	√	√	√	√	√	√
	AP0_3	IO		√	√	√	√	√	√	√	√	√	√
	AP0_4	IO		√	√	√	√	√	√	√	√	√	√
	AP0_5	IO		√	√	√	√	√	√	√	√	√	√
	AP0_6	IO		√	√	√	√	√	√	√	√	√	√
	AP0_7	IO		√	√	√	√	√	√	√	√	√	√
	AP0_8	IO		√	√	√	√	√	√	√	√		√
	AP0_9	IO		√	√	√	√	√	√	√	√		√
	AP0_10	IO		√	√	√	√	√	√	√	√		
	AP0_11	IO		√	√	√	√	√	√	√	√		
	AP0_12	IO		√	√	√	√	√	√	√	√		
	AP0_13	IO		√	√	√	√	√	√	√	√		
	AP0_14	IO		√	√	√	√	√	√	√			
	AP0_15	IO		√	√	√	√	√	√	√			
	AP1_0	IO	Port of analog port group 1	√	√	√	√	√	√	√			
	AP1_1	IO		√	√	√	√	√	√	√			
	AP1_2	IO		√	√	√	√	√	√	√			
	AP1_3	IO		√	√	√	√	√	√	√			
	AP2_0	IO	Port of analog port group 2	√	√	√	√	√	√	√	√	√	√
	AP2_1	IO		√	√	√	√	√	√	√	√	√	√
	AP2_2	IO		√	√	√	√	√	√	√	√	√	√
	AP2_3	IO		√	√	√	√	√	√	√	√	√	√
	AP2_4	IO		√	√	√	√	√	√	√	√	√	√

Table 2.1 Pin Function Name Definition (7/35)

Category	Function name	I/O	Explanation	RH850/ U2A-EVA (BGA516)	RH850/ U2A16 (BGA516)	RH850/ U2A16 (BGA373)	RH850/ U2A16 (BGA292)	RH850/ U2A8 (BGA373)	RH850/ U2A8 (BGA292)	RH850/ U2A6 (BGA292)	RH850/ U2A6 (QFP176)	RH850/ U2A6 (BGA156)	RH850/ U2A6 (QFP144)
Port	AP2_5	IO	Port of analog port group 2	√	√	√	√	√	√	√	√	√	√
	AP2_6	IO		√	√	√	√	√	√	√	√	√	√
	AP2_7	IO		√	√	√	√	√	√	√	√	√	√
	AP2_8	IO		√	√	√	√	√	√	√	√		√
	AP2_9	IO		√	√	√	√	√	√	√	√		√
	AP2_10	IO		√	√	√	√	√	√	√	√		
	AP2_11	IO		√	√	√	√	√	√	√	√		
	AP2_12	IO		√	√	√	√	√	√	√	√		
	AP2_13	IO		√	√	√	√	√	√	√	√		
	AP2_14	IO		√	√	√	√	√	√	√			
	AP2_15	IO		√	√	√	√	√	√	√			
	AP3_0	IO	Port of analog port group 3	√	√	√	√	√	√	√			
	AP3_1	IO		√	√	√	√	√	√	√			
	AP3_2	IO		√	√	√	√	√	√	√			
	AP3_3	IO		√	√	√	√	√	√	√			
	AP4_0	IO	Port of analog port group 4	√	√	√	√	√	√	√	√		
	AP4_1	IO		√	√	√	√	√	√	√	√		
	AP4_2	IO		√	√	√	√	√	√	√	√		
	AP4_3	IO		√	√	√	√	√	√	√	√		
	AP4_4	IO		√	√	√	√	√	√	√	√		
	AP4_5	IO		√	√	√		√					
	AP4_6	IO		√	√	√		√					
	AP4_7	IO		√	√	√		√					
	AP4_8	IO		√	√	√		√					
	AP4_9	IO		√	√	√		√					
	AP4_10	IO		√	√	√		√					
	AP4_11	IO		√	√	√		√					
	AP4_12	IO		√	√	√		√					
	AP4_13	IO		√	√	√		√					
	AP4_14	IO		√	√	√		√					
	AP4_15	IO		√	√	√		√					
	AP5_0	IO	Port of analog port group 5	√	√	√		√					
	AP5_1	IO		√	√	√		√					
	AP5_2	IO		√	√	√		√					
	AP5_3	IO		√	√	√		√					

Table 2.1 Pin Function Name Definition (8/35)

Category	Function name	I/O	Explanation	RH850/ U2A-EVA (BGA516)	RH850/ U2A16 (BGA516)	RH850/ U2A16 (BGA373)	RH850/ U2A16 (BGA292)	RH850/ U2A8 (BGA373)	RH850/ U2A8 (BGA292)	RH850/ U2A6 (BGA292)	RH850/ U2A6 (QFP176)	RH850/ U2A6 (BGA156)	RH850/ U2A6 (QFP144)
Interrupts	NMI	I	Non maskable interrupt	√	√	√	√	√	√	√	√	√	√
	INTP0	I	Maskable external interrupt	√	√	√	√	√	√	√	√	√	√
	INTP1	I		√	√	√	√	√	√	√	√	√	√
	INTP2	I		√	√	√	√	√	√	√	√	√	√
	INTP3	I		√	√	√	√	√	√	√	√	√	√
	INTP4	I		√	√	√	√	√	√	√	√	√	√
	INTP5	I		√	√	√	√	√	√	√	√	√	
	INTP6	I		√	√	√	√	√	√	√	√	√	√
	INTP7	I		√	√	√	√	√	√	√	√	√	√
	INTP8	I		√	√	√	√	√	√	√	√	√	√
	INTP9	I	Maskable external interrupt	√	√	√	√	√	√	√	√	√	
	INTP10	I		√	√	√	√	√	√	√	√	√	√
	INTP11	I		√	√	√	√	√	√	√	√	√	
	INTP12	I		√	√	√	√	√	√	√	√		√
	INTP13	I		√	√	√	√	√	√	√	√		
	INTP14	I		√	√	√	√	√	√	√	√		
	INTP15	I		√	√	√	√	√	√	√	√		
	INTP16	I		√	√	√	√	√	√	√	√	√	√
	INTP17	I		√	√	√	√	√	√	√	√	√	√
	INTP18	I		√	√	√	√	√	√	√	√		√
	INTP19	I		√	√	√	√	√	√	√	√	√	√
	INTP20	I		√	√	√	√	√	√	√	√	√	√
	INTP21	I		√	√	√	√	√	√	√	√	√	√
	INTP22	I		√	√	√	√	√	√	√	√		√
	INTP23	I		√	√	√	√	√	√	√	√	√	√
	INTP24	I		√	√	√	√	√	√	√	√	√	√
	INTP25	I		√	√	√	√	√	√	√	√	√	√
	INTP26	I		√	√	√	√	√	√	√	√	√	√
	INTP27	I		√	√	√	√	√	√	√	√	√	√
	INTP28	I		√	√	√	√	√	√	√			
	INTP29	I		√	√	√	√	√	√	√	√		√
	INTP30	I		√	√	√	√	√	√	√	√	√	√
	INTP31	I		√	√	√	√	√	√	√	√	√	√
	INTP32	I		√	√	√	√	√	√	√	√		√
	INTP33	I		√	√	√	√	√	√	√	√	√	√
	INTP34	I		√	√	√	√	√	√	√	√	√	√
	INTP35	I		√	√	√	√	√	√	√	√		
	INTP36	I		√	√	√	√	√	√	√	√	√	√
	INTP37	I		√	√	√	√	√	√	√	√	√	√
	INTP38	I		√	√	√		√					
	INTP39	I		√	√	√		√					

Table 2.1 Pin Function Name Definition (9/35)

Category	Function name	I/O	Explanation	RH850/U2A-EVA (BGA516)	RH850/U2A16 (BGA516)	RH850/U2A16 (BGA373)	RH850/U2A16 (BGA292)	RH850/U2A8 (BGA373)	RH850/U2A8 (BGA292)	RH850/U2A6 (BGA292)	RH850/U2A6 (QFP176)	RH850/U2A6 (BGA156)	RH850/U2A6 (QFP144)
System Control	FLMD0	I	Operating mode select pin	√	√	√	√	√	√	√	√	√	√
	FLMD1	I		√	√	√	√	√	√	√	√	√	√
	FLMD2	I		√	√	√	√	√	√	√	√	√	√
	MODE0	I		√	√	√	√	√	√	√	√	√	√
	$\overline{\text{RESET}}$	I	Terminal reset	√	√	√	√	√	√	√	√	√	√
	$\overline{\text{RESETOUT}}$	O	Reset output	√	√	√	√	√	√	√	√	√	√
	X1	I	Main oscillator resonator connections	√	√	√	√	√	√	√	√	√	√
	X2	O		√	√	√	√	√	√	√	√	√	√
	EXTCLK0O	O	Clock controller output	√	√	√	√	√	√	√	√	√	√
	EXTCLK1O	O		√	√	√	√	√	√	√	√	√	√
	PWRCTL	O	ISOVDD power control output signal	√	√	√	√	√	√	√	√	√	√
	SVRPGATE	O	SVR gate drive for the high-side PMOSFET	√	√	√	√	√	√	√	√	√	√
	SVRNGATE	O	SVR gate drive for the low-side NMOSFET	√	√	√	√	√	√	√	√	√	√
	$\overline{\text{VMONOUT}}$	O	Voltage monitor error detection output signal	√	√	√	√	√	√	√	√	√	√
LPS	DPO	O	Port output signal for digital input	√	√	√	√	√	√	√	√		√
	APO	O	Port output signal for analog input	√	√	√	√	√	√	√	√		√
	SELDP0	O	External multiplexer select output signal for digital port	√	√	√	√	√	√	√	√		√
	SELDP1	O		√	√	√	√	√	√	√	√		√
	SELDP2	O		√	√	√	√	√	√	√	√		√
	DPIN0	I	Digital port input signal	√	√	√	√	√	√	√	√		√
	DPIN1	I		√	√	√	√	√	√	√	√		√
	DPIN2	I		√	√	√	√	√	√	√	√		√
	DPIN3	I		√	√	√		√					
	DPIN4	I		√	√	√		√					
	DPIN5	I		√	√	√		√					
	DPIN6	I		√	√	√		√					
	DPIN7	I		√	√	√		√					
	DPIN8	I		√	√	√		√					
	DPIN9	I		√	√	√		√					
	DPIN10	I		√	√	√		√					
	DPIN11	I		√	√	√	√	√	√	√	√		√
	DPIN12	I		√	√	√	√	√	√	√	√		√
	DPIN13	I		√	√	√		√					
	DPIN14	I		√	√	√		√					
	DPIN15	I		√	√								
	DPIN16	I		√	√								
	DPIN17	I		√	√								
	DPIN18	I		√	√								
	DPIN19	I		√	√								

Table 2.1 Pin Function Name Definition (10/35)

Category	Function name	I/O	Explanation	RH850/ U2A-EVA (BGA516)	RH850/ U2A16 (BGA516)	RH850/ U2A16 (BGA373)	RH850/ U2A16 (BGA292)	RH850/ U2A8 (BGA373)	RH850/ U2A8 (BGA292)	RH850/ U2A6 (BGA292)	RH850/ U2A6 (QFP176)	RH850/ U2A6 (BGA156)	RH850/ U2A6 (QFP144)
LPS	DPIN20	I	Digital port input signal	√	√								
	DPIN21	I		√	√								
	DPIN22	I		√	√								
	DPIN23	I		√	√								
SFMA	SFMA0CLK	O	SFMA0 clock	√	√	√	√	√	√	√	√		
	SFMA0SSL	O	SFMA0 slave select	√	√	√	√	√	√	√	√		
	SFMA0IO0	IO	SFMA0 master data input / output	√	√	√	√	√	√	√	√		
	SFMA0IO1	IO		√	√	√	√	√	√	√	√		
	SFMA0IO2	IO		√	√	√	√	√	√	√	√		
	SFMA0IO3	IO		√	√	√	√	√	√	√	√		
MMCA	MMCA0CLK	O	MMCA0 clock	√	√	√	√	√	√	√	√		
	MMCA0CMD	IO	MMCA0 command / response	√	√	√	√	√	√	√	√		
	MMCA0DAT0	IO	MMCA0 data	√	√	√	√	√	√	√	√		
	MMCA0DAT1	IO		√	√	√	√	√	√	√	√		
	MMCA0DAT2	IO		√	√	√	√	√	√	√	√		
	MMCA0DAT3	IO		√	√	√	√	√	√	√	√		
	MMCA0DAT4	IO		√	√	√	√	√	√	√	√		
	MMCA0DAT5	IO		√	√	√	√	√	√	√	√		
	MMCA0DAT6	IO		√	√	√	√	√	√	√	√		
	MMCA0DAT7	IO		√	√	√	√	√	√	√	√		
MSPI	MSPI0SC	IO	MSPI0 serial clock input/output	√	√	√	√	√	√	√	√	√	√
	MSPI0SI	I	MSPI0 receive data input	√	√	√	√	√	√	√	√	√	√
	MSPI0SO	O	MSPI0 transmit data output	√	√	√	√	√	√	√	√	√	√
	$\overline{\text{MSPI0SSI}}$	I	MSPI0 serial peripheral chip select input signal	√	√	√	√	√	√	√			
	MSPI0CSS0	O	MSPI0 serial peripheral chip select output signal	√	√	√	√	√	√	√	√	√	√
	MSPI0CSS1	O		√	√	√	√	√	√	√	√		√
	MSPI0CSS2	O		√	√	√	√	√	√	√	√	√	√
	MSPI0CSS3	O		√	√	√	√	√	√	√	√	√	√
	MSPI0CSS4	O		√	√	√	√	√	√	√	√	√	√
	MSPI0CSS5	O		√	√	√	√	√	√	√	√	√	√
	MSPI0CSS6	O		√	√	√	√	√	√	√	√	√	√
	MSPI0CSS7	O		√	√	√	√	√	√	√	√	√	√
	MSPI0DCS	I	MSPI0 data consistency check signal	√	√	√	√	√	√	√	√	√	√
	MSPI0_SCKP	IO	MSPI0 serial clock differential input/ output	√	√	√	√	√	√				
	MSPI0_SCKN	IO		√	√	√	√	√	√				
	MSPI0_SOP	O	MSPI0 transmit data differential output	√	√	√	√	√	√				
	MSPI0_SON	O		√	√	√	√	√	√				
	MSPI0_SIP	I	MSPI0 receive data differential input	√	√	√	√	√	√				
	MSPI0_SIN	I		√	√	√	√	√	√				
	MSPI1SC	IO	MSPI1 serial clock input/output	√	√	√	√	√	√	√	√	√	√

Table 2.1 Pin Function Name Definition (11/35)

Category	Function name	I/O	Explanation	RH850/ U2A-EVA (BGA516)	RH850/ U2A16 (BGA516)	RH850/ U2A16 (BGA373)	RH850/ U2A16 (BGA292)	RH850/ U2A8 (BGA373)	RH850/ U2A8 (BGA292)	RH850/ U2A6 (BGA292)	RH850/ U2A6 (QFP176)	RH850/ U2A6 (BGA156)	RH850/ U2A6 (QFP144)
MSPI	MSPI1SI	I	MSPI1 receive data input	√	√	√	√	√	√	√	√	√	√
	MSPI1SO	O	MSPI1 transmit data output	√	√	√	√	√	√	√	√	√	√
	$\overline{\text{MSPI1SSI}}$	I	MSPI1 serial peripheral chip select input signal	√	√	√	√	√	√	√	√	√	√
	MSPI1CSS0	O	MSPI1 serial peripheral chip select output signal	√	√	√	√	√	√	√	√	√	√
	MSPI1CSS1	O		√	√	√	√	√	√	√	√	√	√
	MSPI1CSS2	O		√	√	√	√	√	√	√	√		√
	MSPI1CSS3	O		√	√	√	√	√	√	√	√	√	√
	MSPI1CSS4	O		√	√	√	√	√	√	√	√	√	√
	MSPI1CSS5	O		√	√	√	√	√	√	√	√	√	√
	MSPI1CSS6	O		√	√	√	√	√	√	√	√	√	√
	MSPI1CSS7	O		√	√	√	√	√	√	√	√	√	√
	MSPI1DCS	I	MSPI1 data consistency check signal	√	√	√	√	√	√	√	√	√	√
	MSPI1_SCKP	IO	MSPI1 serial clock differential input/ output	√	√	√	√	√	√	√			
	MSPI1_SCKN	IO		√	√	√	√	√	√	√			
	MSPI1_SOP	O	MSPI1 transmit data differential output	√	√	√	√	√	√	√			
	MSPI1_SON	O		√	√	√	√	√	√	√			
	MSPI1_SIP	I	MSPI1 receive data differential input	√	√	√	√	√	√	√			
	MSPI1_SIN	I		√	√	√	√	√	√	√			
	MSPI2SC	IO	MSPI2 serial clock input/output	√	√	√	√	√	√	√	√	√	√
	MSPI2SI	I	MSPI2 receive data input	√	√	√	√	√	√	√	√	√	√
	MSPI2SO	O	MSPI2 transmit data output	√	√	√	√	√	√	√	√	√	√
	$\overline{\text{MSPI2SSI}}$	I	MSPI2 serial peripheral chip select input signal	√	√	√	√	√	√	√	√		√
	MSPI2CSS0	O	MSPI2 serial peripheral chip select output signal	√	√	√	√	√	√	√	√	√	√
	MSPI2CSS1	O		√	√	√	√	√	√	√	√		√
	MSPI2CSS2	O		√	√	√	√	√	√	√	√		√
	MSPI2CSS3	O		√	√	√	√	√	√	√	√	√	
	MSPI2CSS4	O	MSPI2 serial peripheral chip select output signal	√	√	√	√	√	√	√	√		√
	MSPI2CSS5	O		√	√	√	√	√	√	√	√		√
	MSPI2CSS6	O		√	√	√	√	√	√	√	√		√
	MSPI2CSS7	O		√	√	√	√	√	√	√	√	√	√
	MSPI2DCS	I	MSPI2 data consistency check signal	√	√	√	√	√	√	√	√	√	√
	MSPI3SC	IO	MSPI3 serial clock input/output	√	√	√	√	√	√	√	√	√	√
	MSPI3SI	I	MSPI3 receive data input	√	√	√	√	√	√	√	√	√	√
	MSPI3SO	O	MSPI3 transmit data output	√	√	√	√	√	√	√	√	√	√

Table 2.1 Pin Function Name Definition (12/35)

Category	Function name	I/O	Explanation	RH850/ U2A-EVA (BGA516)	RH850/ U2A16 (BGA516)	RH850/ U2A16 (BGA373)	RH850/ U2A16 (BGA292)	RH850/ U2A8 (BGA373)	RH850/ U2A8 (BGA292)	RH850/ U2A6 (BGA292)	RH850/ U2A6 (QFP176)	RH850/ U2A6 (BGA156)	RH850/ U2A6 (QFP144)
MSPI	$\overline{\text{MSPI3SSI}}$	I	MSPI3 serial peripheral chip select input signal	√	√	√	√	√	√	√			
	MSPI3CSS0	O	MSPI3 serial peripheral chip select output signal	√	√	√	√	√	√	√	√		√
	MSPI3CSS1	O		√	√	√	√	√	√	√	√		√
	MSPI3CSS2	O		√	√	√	√	√	√	√	√	√	√
	MSPI3CSS3	O		√	√	√	√	√	√	√	√		
	MSPI3CSS4	O		√	√	√	√	√	√	√			
	MSPI3CSS5	O		√	√	√	√	√	√	√			
	MSPI3CSS6	O		√	√	√	√	√	√	√			
	MSPI3CSS7	O		√	√	√	√	√	√	√			
	MSPI3DCS	I	MSPI3 data consistency check signal	√	√	√	√	√	√	√	√	√	√
	MSPI4SC	IO	MSPI4 serial clock input/output	√	√	√	√	√	√	√	√	√	
	MSPI4SI	I	MSPI4 receive data input	√	√	√	√	√	√	√	√	√	
	MSPI4SO	O	MSPI4 transmit data output	√	√	√	√	√	√	√	√	√	
	$\overline{\text{MSPI4SSI}}$	I	MSPI4 serial peripheral chip select input signal	√	√	√	√	√	√	√			
	MSPI4CSS0	O	MSPI4 serial peripheral chip select output signal	√	√	√	√	√	√	√			
	MSPI4CSS1	O		√	√	√	√	√	√	√	√	√	
	MSPI4CSS2	O		√	√	√	√	√	√	√	√	√	
	MSPI4CSS3	O		√	√	√	√	√	√	√	√	√	
	MSPI4CSS4	O		√	√	√	√	√	√	√	√	√	
	MSPI4CSS5	O		√	√	√	√	√	√	√	√	√	
	MSPI4CSS6	O		√	√	√	√	√	√	√	√	√	
	MSPI4CSS7	O		√	√	√	√	√	√	√	√		
	MSPI4DCS	I	MSPI4 data consistency check signal	√	√	√	√	√	√	√	√	√	
	MSPI5SC	IO	MSPI5 serial clock input/output	√	√	√	√	√	√	√	√	√	
	MSPI5SI	I	MSPI5 receive data input	√	√	√	√	√	√	√	√	√	
	MSPI5SO	O	MSPI5 transmit data output	√	√	√	√	√	√	√	√	√	
	$\overline{\text{MSPI5SSI}}$	I	MSPI5 serial peripheral chip select input signal	√	√	√	√	√	√	√	√	√	
	MSPI5CSS0	O	MSPI5 serial peripheral chip select output signal	√	√	√	√	√	√	√	√	√	
	MSPI5CSS1	O	MSPI5 slave select signal output	√	√	√	√	√	√	√	√	√	
	MSPI5CSS2	O		√	√	√	√	√	√	√	√	√	
	MSPI5CSS3	O		√	√	√	√	√	√	√	√		
	MSPI5DCS	I	MSPI5 data consistency check signal	√	√	√	√	√	√	√	√	√	
	MSPI6SC	IO	MSPI6 serial clock input/output	√	√	√		√					

Table 2.1 Pin Function Name Definition (13/35)

Category	Function name	I/O	Explanation	RH850/ U2A-EVA (BGA516)	RH850/ U2A16 (BGA516)	RH850/ U2A16 (BGA373)	RH850/ U2A16 (BGA292)	RH850/ U2A8 (BGA373)	RH850/ U2A8 (BGA292)	RH850/ U2A6 (BGA292)	RH850/ U2A6 (QFP176)	RH850/ U2A6 (BGA156)	RH850/ U2A6 (QFP144)
MSPI	MSPI6SI	I	MSPI6 receive data input	√	√	√		√					
	MSPI6SO	O	MSPI6 transmit data output	√	√	√		√					
	$\overline{\text{MSPI6SSI}}$	I	MSPI6 serial peripheral chip select input signal	√	√	√		√					
	MSPI6CSS0	O	MSPI6 serial peripheral chip select output signal	√	√	√		√					
	MSPI6CSS1	O		√	√	√		√					
	MSPI6CSS2	O		√	√	√		√					
	MSPI6CSS3	O		√	√	√		√					
	MSPI6DCS	I	MSPI6 data consistency check signal	√	√	√		√					
	MSPI7SC	IO	MSPI7 serial clock input/output	√	√	√		√					
	MSPI7SI	I	MSPI7 receive data input	√	√	√		√					
	MSPI7SO	O	MSPI7 transmit data output	√	√	√		√					
	$\overline{\text{MSPI7SSI}}$	I	MSPI7 serial peripheral chip select input signal	√	√	√		√					
	MSPI7CSS0	O	MSPI7 serial peripheral chip select output signal	√	√	√		√					
	MSPI7CSS1	O		√	√	√		√					
	MSPI7CSS2	O		√	√	√		√					
	MSPI7CSS3	O		√	√	√		√					
	MSPI7DCS	I	MSPI7 data consistency check signal	√	√	√		√					
	MSPI8SC	IO	MSPI8 serial clock input/output	√	√	√		√					
	MSPI8SI	I	MSPI8 receive data input	√	√	√		√					
	MSPI8SO	O	MSPI8 transmit data output	√	√	√		√					
	$\overline{\text{MSPI8SSI}}$	I	MSPI8 serial peripheral chip select input signal	√	√	√		√					
	MSPI8CSS0	O	MSPI8 serial peripheral chip select output signal	√	√	√		√					
	MSPI8CSS1	O		√	√	√		√					
	MSPI8CSS2	O		√	√	√		√					
	MSPI8CSS3	O		√	√	√		√					
	MSPI8DCS	I	MSPI8 data consistency check signal	√	√	√		√					
	MSPI9SC	IO	MSPI9 serial clock input/output	√	√								
	MSPI9SI	I	MSPI9 receive data input	√	√								
	MSPI9SO	O	MSPI9 transmit data output	√	√								
	$\overline{\text{MSPI9SSI}}$	I	MSPI9 serial peripheral chip select input signal	√	√								

Table 2.1 Pin Function Name Definition (14/35)

Category	Function name	I/O	Explanation	RH850/ U2A-EVA (BGA516)	RH850/ U2A16 (BGA516)	RH850/ U2A16 (BGA373)	RH850/ U2A16 (BGA292)	RH850/ U2A8 (BGA373)	RH850/ U2A8 (BGA292)	RH850/ U2A6 (BGA292)	RH850/ U2A6 (QFP176)	RH850/ U2A6 (BGA156)	RH850/ U2A6 (QFP144)
MSPI	MSPI9CSS0	O	MSPI9 serial peripheral chip select output signal	√	√								
	MSPI9CSS1	O		√	√								
	MSPI9CSS2	O		√	√								
	MSPI9CSS3	O		√	√								
	MSPI9DCS	I	MSPI9 data consistency check signal	√	√								
SCI3	SCI30RXD	I	SCI30 data input signal	√	√	√	√	√	√				
	SCI30TXD	O	SCI30 data output signal	√	√	√	√	√	√				
	SCI30SCK	IO	SCI30 serial clock input/output	√	√	√	√	√	√				
	SCI31RXD	I	SCI31 data input signal	√	√	√	√	√	√				
	SCI31TXD	O	SCI31 data output signal	√	√	√	√	√	√				
	SCI31SCK	IO	SCI31 serial clock input/output	√	√	√	√	√	√				
	SCI32RXD	I	SCI32 data input signal	√	√	√	√	√	√				
	SCI32TXD	O	SCI32 data output signal	√	√	√	√	√	√				
	SCI32SCK	IO	SCI32 serial clock input/output	√	√	√	√	√	√				
RLIN3	RLIN30RX	I	RLIN30 receive data input	√	√	√	√	√	√	√	√	√	√
	RLIN30TX	O	RLIN30 transmit data output	√	√	√	√	√	√	√	√	√	√
	RLIN31RX	I	RLIN31 receive data input	√	√	√	√	√	√	√	√		
	RLIN31TX	O	RLIN31 transmit data output	√	√	√	√	√	√	√	√		
	RLIN32RX	I	RLIN32 receive data input	√	√	√	√	√	√	√	√		√
	RLIN32TX	O	RLIN32 transmit data output	√	√	√	√	√	√	√	√		√
	RLIN33RX	I	RLIN33 receive data input	√	√	√	√	√	√	√	√	√	√
	RLIN33TX	O	RLIN33 transmit data output	√	√	√	√	√	√	√	√	√	√
	RLIN34RX	I	RLIN34 receive data input	√	√	√	√	√	√	√	√	√	√
	RLIN34TX	O	RLIN34 transmit data output	√	√	√	√	√	√	√	√	√	√
	RLIN35RX	I	RLIN35 receive data input	√	√	√	√	√	√	√	√	√	√
	RLIN35TX	O	RLIN35 transmit data output	√	√	√	√	√	√	√	√	√	√
	RLIN36RX	I	RLIN36 receive data input	√	√	√	√	√	√	√	√		
	RLIN36TX	O	RLIN36 transmit data output	√	√	√	√	√	√	√	√		
	RLIN37RX	I	RLIN37 receive data input	√	√	√	√	√	√	√	√		√

Table 2.1 Pin Function Name Definition (15/35)

Category	Function name	I/O	Explanation	RH850/ U2A-EVA (BGA516)	RH850/ U2A16 (BGA516)	RH850/ U2A16 (BGA373)	RH850/ U2A16 (BGA292)	RH850/ U2A8 (BGA373)	RH850/ U2A8 (BGA292)	RH850/ U2A6 (BGA292)	RH850/ U2A6 (QFP176)	RH850/ U2A6 (BGA156)	RH850/ U2A6 (QFP144)
RLIN3	RLIN37TX	O	RLIN37 transmit data output	√	√	√	√	√	√	√	√		√
	RLIN38RX	I	RLIN38 receive data input	√	√	√	√	√	√	√	√	√	√
	RLIN38TX	O	RLIN38 transmit data output	√	√	√	√	√	√	√	√	√	√
	RLIN39RX	I	RLIN39 receive data input	√	√	√	√	√	√	√	√	√	√
	RLIN39TX	O	RLIN39 transmit data output	√	√	√	√	√	√	√	√	√	√
	RLIN310RX	I	RLIN310 receive data input	√	√	√	√	√	√	√	√	√	√
	RLIN310TX	O	RLIN310 transmit data output	√	√	√	√	√	√	√	√	√	√
	RLIN311RX	I	RLIN311 receive data input	√	√	√	√	√	√	√	√	√	√
	RLIN311TX	O	RLIN311 transmit data output	√	√	√	√	√	√	√	√	√	√
	RLIN312RX	I	RLIN312 receive data input	√	√	√		√					
	RLIN312TX	O	RLIN312 transmit data output	√	√	√		√					
	RLIN313RX	I	RLIN313 receive data input	√	√	√		√					
	RLIN313TX	O	RLIN313 transmit data output	√	√	√		√					
	RLIN314RX	I	RLIN314 receive data input	√	√	√		√					
	RLIN314TX	O	RLIN314 transmit data output	√	√	√		√					
	RLIN315RX	I	RLIN315 receive data input	√	√	√		√					
	RLIN315TX	O	RLIN315 transmit data output	√	√	√		√					
	RLIN316RX	I	RLIN316 receive data input	√	√	√		√					
	RLIN316TX	O	RLIN316 transmit data output	√	√	√		√					
	RLIN317RX	I	RLIN317 receive data input	√	√	√		√					
	RLIN317TX	O	RLIN317 transmit data output	√	√	√		√					
	RLIN318RX	I	RLIN318 receive data input	√	√	√		√					
	RLIN318TX	O	RLIN318 transmit data output	√	√	√		√					
	RLIN319RX	I	RLIN319 receive data input	√	√	√		√					
	RLIN319TX	O	RLIN319 transmit data output	√	√	√		√					
	RLIN320RX	I	RLIN320 receive data input	√	√	√		√					
	RLIN320TX	O	RLIN320 transmit data output	√	√	√		√					
	RLIN321RX	I	RLIN321 receive data input	√	√	√		√					

Table 2.1 Pin Function Name Definition (16/35)

Category	Function name	I/O	Explanation	RH850/ U2A-EVA (BGA516)	RH850/ U2A16 (BGA516)	RH850/ U2A16 (BGA373)	RH850/ U2A16 (BGA292)	RH850/ U2A8 (BGA373)	RH850/ U2A8 (BGA292)	RH850/ U2A6 (BGA292)	RH850/ U2A6 (QFP176)	RH850/ U2A6 (BGA156)	RH850/ U2A6 (QFP144)
RLIN3	RLIN321TX	O	RLIN321 transmit data output	√	√	√		√					
	RLIN322RX	I	RLIN322 receive data input	√	√	√		√					
	RLIN322TX	O	RLIN322 transmit data output	√	√	√		√					
	RLIN323RX	I	RLIN323 receive data input	√	√	√		√					
	RLIN323TX	O	RLIN323 transmit data output	√	√	√		√					
RIIC	RIIC0SCL	IO	RIIC0 serial clock	√	√	√	√	√	√	√	√	√	√
	RIIC0SDA	IO	RIIC0 serial data	√	√	√	√	√	√	√	√	√	√
	RIIC1SCL	IO	RIIC1 serial clock	√	√	√	√	√	√	√	√	√	
	RIIC1SDA	IO	RIIC1 serial data	√	√	√	√	√	√	√	√	√	
RS-CANFD	CAN0RX	I	CAN0 receive data input	√	√	√	√	√	√	√	√	√	√
	CAN0TX	O	CAN0 transmit data output	√	√	√	√	√	√	√	√	√	√
	CAN1RX	I	CAN1 receive data input	√	√	√	√	√	√	√	√	√	√
	CAN1TX	O	CAN1 transmit data output	√	√	√	√	√	√	√	√	√	√
	CAN2RX	I	CAN2 receive data input	√	√	√	√	√	√	√			√
	CAN2TX	O	CAN2 transmit data output	√	√	√	√	√	√	√			√
	CAN3RX	I	CAN3 receive data input	√	√	√	√	√	√	√	√		
	CAN3TX	O	CAN3 transmit data output	√	√	√	√	√	√	√	√		
	CAN4RX	I	CAN4 receive data input	√	√	√	√	√	√	√	√	√	√
	CAN4TX	O	CAN4 transmit data output	√	√	√	√	√	√	√	√	√	√
	CAN5RX	I	CAN5 receive data input	√	√	√	√	√	√	√	√		
	CAN5TX	O	CAN5 transmit data output	√	√	√	√	√	√	√	√		
	CAN6RX	I	CAN6 receive data input	√	√	√	√	√	√	√	√	√	√
	CAN6TX	O	CAN6 transmit data output	√	√	√	√	√	√	√	√	√	√
	CAN7RX	I	CAN7 receive data input	√	√	√	√	√	√	√	√		√
	CAN7TX	O	CAN7 transmit data output	√	√	√	√	√	√	√	√		√
	CAN8RX	I	CAN8 receive data input	√	√	√	√	√	√	√	√	√	√
	CAN8TX	O	CAN8 transmit data output	√	√	√	√	√	√	√	√	√	√
	CAN9RX	I	CAN9 receive data input	√	√	√	√	√	√	√	√	√	
	CAN9TX	O	CAN9 transmit data output	√	√	√	√	√	√	√	√	√	
	CAN10RX	I	CAN10 receive data input	√	√	√	√	√	√	√	√	√	

Table 2.1 Pin Function Name Definition (17/35)

Category	Function name	I/O	Explanation	RH850/ U2A-EVA (BGA516)	RH850/ U2A16 (BGA516)	RH850/ U2A16 (BGA373)	RH850/ U2A16 (BGA292)	RH850/ U2A8 (BGA373)	RH850/ U2A8 (BGA292)	RH850/ U2A6 (BGA292)	RH850/ U2A6 (QFP176)	RH850/ U2A6 (BGA156)	RH850/ U2A6 (QFP144)
RS-CANFD	CAN10TX	O	CAN10 transmit data output	√	√	√	√	√	√	√	√	√	
	CAN11RX	I	CAN11 receive data input	√	√	√	√	√	√	√	√	√	
	CAN11TX	O	CAN11 transmit data output	√	√	√	√	√	√	√	√	√	
	CAN12RX	I	CAN12 receive data input	√	√	√	√	√	√				
	CAN12TX	O	CAN12 transmit data output	√	√	√	√	√	√				
	CAN13RX	I	CAN13 receive data input	√	√	√	√	√	√				
	CAN13TX	O	CAN13 transmit data output	√	√	√	√	√	√				
	CAN14RX	I	CAN14 receive data input	√	√	√	√	√	√				
	CAN14TX	O	CAN14 transmit data output	√	√	√	√	√	√				
	CAN15RX	I	CAN15 receive data input	√	√	√	√	√	√				
	CAN15TX	O	CAN15 transmit data output	√	√	√	√	√	√				
FLXA	FLXA0RXDA	I	FLXA0 channel A receive data input	√	√	√	√	√	√	√	√	√	√
	FLXA0TXDA	O	FLXA0 channel A transmit data output	√	√	√	√	√	√	√	√	√	√
	FLXA0TXENA	O	FLXA0 channel A transmit enable	√	√	√	√	√	√	√	√	√	√
	FLXA0RXDB	I	FLXA0 channel B receive data input	√	√	√	√	√	√	√	√	√	√
	FLXA0TXDB	O	FLXA0 channel B transmit data output	√	√	√	√	√	√	√	√	√	√
	FLXA0TXENB	O	FLXA0 channel B transmit enable	√	√	√	√	√	√	√	√	√	√
	FLXA0STPWT	I	FLXA0 stop watch trigger input	√	√	√	√	√	√	√	√	√	√
	FLXA1RXDA	I	FLXA1 channel A receive data input	√	√	√	√	√	√				
	FLXA1TXDA	O	FLXA1 channel A transmit data output	√	√	√	√	√	√				
	FLXA1TXENA	O	FLXA1 channel A transmit enable	√	√	√	√	√	√				
	FLXA1RXDB	I	FLXA1 channel B receive data input	√	√	√	√	√	√				
	FLXA1TXDB	O	FLXA1 channel B transmit data output	√	√	√	√	√	√				
	FLXA1TXENB	O	FLXA1 channel B transmit enable	√	√	√	√	√	√				
	FLXA1STPWT	I	FLXA1 stop watch trigger input	√	√	√	√	√	√				

Table 2.1 Pin Function Name Definition (18/35)

Category	Function name	I/O	Explanation	RH850/ U2A-EVA (BGA516)	RH850/ U2A16 (BGA516)	RH850/ U2A16 (BGA373)	RH850/ U2A16 (BGA292)	RH850/ U2A8 (BGA373)	RH850/ U2A8 (BGA292)	RH850/ U2A6 (BGA292)	RH850/ U2A6 (QFP176)	RH850/ U2A6 (BGA156)	RH850/ U2A6 (QFP144)
ETNB	ETNB0TXCLK	I	MII transmit clock	√	√	√	√	√	√	√	√		√
	ETNB0RXCLK	I	MII receive clock	√	√	√	√	√	√	√	√		√
	ETNB0TXEN	O	MII/RMII transmit data enable	√	√	√	√	√	√	√	√		√
	ETNB0TXD0	O	MII/RMII transmit data	√	√	√	√	√	√	√	√		√
	ETNB0TXD1	O		√	√	√	√	√	√	√	√		√
	ETNB0TXD2	O		√	√	√	√	√	√	√	√		√
	ETNB0TXD3	O		√	√	√	√	√	√	√	√		√
	ETNB0TXER	O	MII transmit data error	√	√	√	√	√	√	√	√		√
	ETNB0RXDV	I	MII receive data valid	√	√	√	√	√	√	√	√		√
	ETNB0RXD0	I	MII/RMII receive data	√	√	√	√	√	√	√	√		√
	ETNB0RXD1	I		√	√	√	√	√	√	√	√		√
	ETNB0RXD2	I		√	√	√	√	√	√	√	√		√
	ETNB0RXD3	I		√	√	√	√	√	√	√	√		√
	ETNB0RXER	I	MII/RMII receive data error	√	√	√	√	√	√	√	√		√
	ETNB0REFCLK	I	RMII reference clock	√	√	√	√	√	√	√	√		√
	ETNB0CRS_DV	I	RMII receive data valid	√	√	√	√	√	√	√	√		√
	ETNB0MDC	O	PHY management clock	√	√	√	√	√	√	√	√		√
	ETNB0MDIO	IO	PHY management transfer data	√	√	√	√	√	√	√	√		√
	ETNB0LINKSTA	I	PHY link status	√	√	√	√	√	√	√	√		√
	ETNB0WOL	O	Wake-On-LAN (Magic Packet detection)	√	√	√	√	√	√	√	√		√
	TX_DATAN	O	SGMII transmit serial data differential output	√	√	√	√	√	√				
	TX_DATAP	O		√	√	√	√	√	√				
	RX_CLKN	I	SGMII receive ddr clock differential input	√									
	RX_CLKP	I		√									
	RX_DATAN	I	SGMII receive serial data differential input	√	√	√	√	√	√				
	RX_DATAP	I		√	√	√	√	√	√				
	ETNB1REFCLK	I	SGMII reference clock	√	√	√	√	√	√				
	ETNB1TXCLK	I	MII transmit clock	√	√								
	ETNB1RXCLK	I	MII receive clock	√	√								
	ETNB1TXEN	O	MII transmit data enable	√	√								
	ETNB1TXD0	O	MII transmit data	√	√								
	ETNB1TXD1	O		√	√								
	ETNB1TXD2	O		√	√								
	ETNB1TXD3	O		√	√								
	ETNB1TXER	O	MII transmit data error	√	√								
	ETNB1RXDV	I	MII receive data valid	√	√								

Table 2.1 Pin Function Name Definition (19/35)

Category	Function name	I/O	Explanation	RH850/ U2A-EVA (BGA516)	RH850/ U2A16 (BGA516)	RH850/ U2A16 (BGA373)	RH850/ U2A16 (BGA292)	RH850/ U2A8 (BGA373)	RH850/ U2A8 (BGA292)	RH850/ U2A6 (BGA292)	RH850/ U2A6 (QFP176)	RH850/ U2A6 (BGA156)	RH850/ U2A6 (QFP144)
ETNB	ETNB1RXD0	I	MII receive data	√	√								
	ETNB1RXD1	I		√	√								
	ETNB1RXD2	I		√	√								
	ETNB1RXD3	I		√	√								
	ETNB1RXER	I	MII receive data error	√	√								
	ETNB1MDC	O	PHY management clock	√	√	√	√	√	√				
	ETNB1MDIO	IO	PHY management transfer data	√	√	√	√	√	√				
	ETNB1LINKSTA	I	PHY link status signal	√	√								
	ETNB1PHYINT	I	PHY interrupt information	√	√	√	√	√	√				
	ETNB1WOL	O	Wake-On-LAN signal (Magic Packet detection)	√	√	√	√	√	√				
RSENT	RSENT0RX	I	RSENT0 receive data input	√	√	√	√	√	√	√	√	√	√
	RSENT0SPCO	O	RSENT0 SPC extension output	√	√	√	√	√	√	√	√	√	√
	RSENT1RX	I	RSENT1 receive data input	√	√	√	√	√	√	√	√	√	√
	RSENT1SPCO	O	RSENT1 SPC extension output	√	√	√	√	√	√	√	√	√	√
	RSENT2RX	I	RSENT2 receive data input	√	√	√	√	√	√	√	√	√	√
	RSENT2SPCO	O	RSENT2 SPC extension output	√	√	√	√	√	√	√	√	√	√
	RSENT3RX	I	RSENT3 receive data input	√	√	√	√	√	√	√	√	√	√
	RSENT3SPCO	O	RSENT3 SPC extension output	√	√	√	√	√	√	√	√	√	√
	RSENT4RX	I	RSENT4 receive data input	√	√	√	√	√	√	√	√	√	√
	RSENT4SPCO	O	RSENT4 SPC extension output	√	√	√	√	√	√	√	√	√	√
	RSENT5RX	I	RSENT5 receive data input	√	√	√	√	√	√	√	√	√	√
	RSENT5SPCO	O	RSENT5 SPC extension output	√	√	√	√	√	√	√	√	√	√
	RSENT6RX	I	RSENT6 receive data input	√	√	√	√	√	√	√	√	√	
	RSENT6SPCO	O	RSENT6 SPC extension output	√	√	√	√	√	√	√	√	√	
	RSENT7RX	I	RSENT7 receive data input	√	√	√	√	√	√	√	√	√	
	RSENT7SPCO	O	RSENT7 SPC extension output	√	√	√	√	√	√	√	√	√	

Table 2.1 Pin Function Name Definition (20/35)

Category	Function name	I/O	Explanation	RH850/ U2A-EVA (BGA516)	RH850/ U2A16 (BGA516)	RH850/ U2A16 (BGA373)	RH850/ U2A16 (BGA292)	RH850/ U2A8 (BGA373)	RH850/ U2A8 (BGA292)	RH850/ U2A6 (BGA292)	RH850/ U2A6 (QFP176)	RH850/ U2A6 (BGA156)	RH850/ U2A6 (QFP144)
PSI5	PSI50RX	I	PSI50 receive data input	√	√	√	√	√	√	√	√	√	√
	PSI50TX	O	PSI50 transmit data output	√	√	√	√	√	√	√	√	√	√
	PSI51RX	I	PSI51 receive data input	√	√	√	√	√	√	√	√	√	
	PSI51TX	O	PSI51 transmit data output	√	√	√	√	√	√	√	√	√	
	PSI52RX	I	PSI52 receive data input	√	√	√	√	√	√	√	√	√	√
	PSI52TX	O	PSI52 transmit data output	√	√	√	√	√	√	√	√	√	√
	PSI53RX	I	PSI53 receive data input	√	√	√	√	√	√	√	√	√	√
	PSI53TX	O	PSI53 transmit data output	√	√	√	√	√	√	√	√	√	√
	PSI5S0RX	I	UART Rx data	√	√	√	√	√	√	√			
	PSI5S0TX	O	UART Tx data	√	√	√	√	√	√	√			
	PSI5S0CLK	O	UART clock	√	√	√	√	√	√	√			
	PSI5S1RX	I	UART Rx data	√	√	√	√	√	√	√	√	√	√
	PSI5S1TX	O	UART Tx data	√	√	√	√	√	√	√	√	√	√
	PSI5S1CLK	O	UART clock	√	√	√	√	√	√	√	√	√	√
RHSIF	HSIF0_REFCLK	IO	RHSIF0 reference clock input/output	√	√	√	√	√	√				
	HSIF0_RXDN	I	RHSIF0 receive data differential input	√	√	√	√	√	√				
	HSIF0_RXDP	I		√	√	√	√	√	√				
	HSIF0_TXDN	O	RHSIF0 transmit data differential output	√	√	√	√	√	√				
	HSIF0_TXDP	O		√	√	√	√	√	√				
CXP1	CXP10RX	I	CXP10 receive data input	√	√	√	√	√	√				
	CXP10TX	O	CXP10 transmit data output	√	√	√	√	√	√				
	CXP11RX	I	CXP11 receive data input	√	√	√	√	√	√				
	CXP11TX	O	CXP11 transmit data output	√	√	√	√	√	√				
	CXP12RX	I	CXP12 receive data input	√	√	√	√	√	√				
	CXP12TX	O	CXP12 transmit data output	√	√	√	√	√	√				
	CXP13RX	I	CXP13 receive data input	√	√	√	√	√	√				
	CXP13TX	O	CXP13 transmit data output	√	√	√	√	√	√				
OSTM	OSTM8O	O	OSTM8 timer output	√	√	√	√	√	√	√	√	√	√
	OSTM9O	O	OSTM9 timer output	√	√	√	√	√	√	√	√	√	√

Table 2.1 Pin Function Name Definition (21/35)

Category	Function name	I/O	Explanation	RH850/ U2A-EVA (BGA516)	RH850/ U2A16 (BGA516)	RH850/ U2A16 (BGA373)	RH850/ U2A16 (BGA292)	RH850/ U2A8 (BGA373)	RH850/ U2A8 (BGA292)	RH850/ U2A6 (BGA292)	RH850/ U2A6 (QFP176)	RH850/ U2A6 (BGA156)	RH850/ U2A6 (QFP144)
TAUD	TAUD0I0	I	TAUD0 channel input	√	√	√	√	√	√	√	√	√	
	TAUD0I1	I		√	√	√	√	√	√	√	√	√	
	TAUD0I2	I		√	√	√	√	√	√	√	√	√	
	TAUD0I3	I		√	√	√	√	√	√	√	√	√	√
	TAUD0I4	I		√	√	√	√	√	√	√	√	√	√
	TAUD0I5	I		√	√	√	√	√	√	√	√	√	
	TAUD0I6	I		√	√	√	√	√	√	√	√		
	TAUD0I7	I		√	√	√	√	√	√	√	√		√
	TAUD0I8	I		√	√	√	√	√	√	√	√		
	TAUD0I9	I		√	√	√	√	√	√	√	√		
	TAUD0I10	I		√	√	√	√	√	√	√	√	√	√
	TAUD0I11	I		√	√	√	√	√	√	√	√	√	√
	TAUD0I12	I		√	√	√	√	√	√	√	√		
	TAUD0I13	I		√	√	√	√	√	√	√	√		
	TAUD0I14	I		√	√	√	√	√	√	√	√		
	TAUD0I15	I		√	√	√	√	√	√	√	√		√
	TAUD0O0	O	TAUD0 channel output	√	√	√	√	√	√	√	√	√	√
	TAUD0O1	O		√	√	√	√	√	√	√	√		
	TAUD0O2	O		√	√	√	√	√	√	√	√		√
	TAUD0O3	O		√	√	√	√	√	√	√	√		
	TAUD0O4	O		√	√	√	√	√	√	√	√		
	TAUD0O5	O		√	√	√	√	√	√	√	√		
	TAUD0O6	O		√	√	√	√	√	√	√	√		
	TAUD0O7	O		√	√	√	√	√	√	√	√		
	TAUD0O8	O		√	√	√	√	√	√	√	√		
	TAUD0O9	O		√	√	√	√	√	√	√			
	TAUD0O10	O		√	√	√	√	√	√	√			
	TAUD0O11	O		√	√	√	√	√	√	√	√		√
	TAUD0O12	O		√	√	√	√	√	√	√	√		√
	TAUD0O13	O		√	√	√	√	√	√	√	√		√
	TAUD0O14	O		√	√	√	√	√	√	√	√	√	√
	TAUD0O15	O		√	√	√	√	√	√	√			√
	TAUD1I0	I	TAUD1 channel input	√	√	√	√	√	√	√	√		√
	TAUD1I1	I		√	√	√	√	√	√	√	√	√	√
	TAUD1I2	I		√	√	√	√	√	√	√	√	√	√
	TAUD1I3	I		√	√	√	√	√	√	√	√		
	TAUD1I4	I		√	√	√	√	√	√	√	√	√	
	TAUD1I5	I		√	√	√	√	√	√	√	√	√	√
	TAUD1I6	I		√	√	√	√	√	√	√	√	√	√
	TAUD1I7	I		√	√	√	√	√	√	√	√	√	√
	TAUD1I8	I		√	√	√	√	√	√	√	√	√	√
	TAUD1I9	I		√	√	√	√	√	√	√	√	√	√
	TAUD1I10	I		√	√	√	√	√	√	√	√	√	√
	TAUD1I11	I		√	√	√	√	√	√	√	√	√	√

Table 2.1 Pin Function Name Definition (22/35)

Category	Function name	I/O	Explanation	RH850/ U2A-EVA (BGA516)	RH850/ U2A16 (BGA516)	RH850/ U2A16 (BGA373)	RH850/ U2A16 (BGA292)	RH850/ U2A8 (BGA373)	RH850/ U2A8 (BGA292)	RH850/ U2A6 (BGA292)	RH850/ U2A6 (QFP176)	RH850/ U2A6 (BGA156)	RH850/ U2A6 (QFP144)
TAUD	TAUD1I12	I		√	√	√	√	√	√	√	√	√	√
	TAUD1I13	I		√	√	√	√	√	√	√	√	√	√
	TAUD1I14	I		√	√	√	√	√	√	√	√	√	√
	TAUD1I15	I		√	√	√	√	√	√	√	√	√	√
	TAUD1O0	O	TAUD1 channel output	√	√	√	√	√	√	√			
	TAUD1O1	O		√	√	√	√	√	√	√	√		√
	TAUD1O2	O		√	√	√	√	√	√	√	√		√
	TAUD1O3	O		√	√	√	√	√	√	√	√	√	√
	TAUD1O4	O		√	√	√	√	√	√	√	√	√	√
	TAUD1O5	O		√	√	√	√	√	√	√	√		√
	TAUD1O6	O		√	√	√	√	√	√	√	√		√
	TAUD1O7	O		√	√	√	√	√	√	√	√	√	√
	TAUD1O8	O		√	√	√	√	√	√	√	√	√	
	TAUD1O9	O		√	√	√	√	√	√	√	√	√	
	TAUD1O10	O		√	√	√	√	√	√	√	√	√	
	TAUD1O11	O		√	√	√	√	√	√	√			
	TAUD1O12	O	TAUD1 channel output	√	√	√	√	√	√	√			
	TAUD1O13	O		√	√	√	√	√	√	√			
	TAUD1O14	O		√	√	√	√	√	√	√			
	TAUD1O15	O		√	√	√	√	√	√	√			
	TAUD2I0	I	TAUD2 channel input	√	√	√	√	√	√	√	√	√	√
	TAUD2I1	I		√	√	√	√	√	√	√	√	√	√
	TAUD2I2	I		√	√	√	√	√	√	√	√		√
	TAUD2I3	I		√	√	√	√	√	√	√	√	√	√
	TAUD2I4	I		√	√	√	√	√	√	√	√	√	√
	TAUD2I5	I		√	√	√	√	√	√	√	√	√	√
	TAUD2I6	I		√	√	√	√	√	√	√	√	√	√
	TAUD2I7	I		√	√	√	√	√	√	√	√	√	√
	TAUD2I8	I		√	√	√	√	√	√	√	√	√	√
	TAUD2I9	I		√	√	√	√	√	√	√	√		√
	TAUD2I10	I		√	√	√	√	√	√	√	√	√	√
	TAUD2I11	I		√	√	√	√	√	√	√	√	√	√
	TAUD2I12	I		√	√	√	√	√	√	√	√		√
	TAUD2I13	I		√	√	√	√	√	√	√	√	√	√
	TAUD2I14	I		√	√	√	√	√	√	√	√	√	√
	TAUD2I15	I		√	√	√	√	√	√	√	√		

Table 2.1 Pin Function Name Definition (23/35)

Category	Function name	I/O	Explanation	RH850/ U2A-EVA (BGA516)	RH850/ U2A16 (BGA516)	RH850/ U2A16 (BGA373)	RH850/ U2A16 (BGA292)	RH850/ U2A8 (BGA373)	RH850/ U2A8 (BGA292)	RH850/ U2A6 (BGA292)	RH850/ U2A6 (QFP176)	RH850/ U2A6 (BGA156)	RH850/ U2A6 (QFP144)
TAUD	TAUD2O0	O	TAUD2 channel output	√	√	√	√	√	√	√			√
	TAUD2O1	O		√	√	√	√	√	√	√			√
	TAUD2O2	O		√	√	√	√	√	√	√			√
	TAUD2O3	O		√	√	√	√	√	√	√			
	TAUD2O4	O		√	√	√	√	√	√	√			
	TAUD2O5	O		√	√	√	√	√	√	√	√		√
	TAUD2O6	O		√	√	√	√	√	√	√	√	√	√
	TAUD2O7	O		√	√	√	√	√	√	√	√	√	√
	TAUD2O8	O		√	√	√	√	√	√	√	√		√
	TAUD2O9	O		√	√	√	√	√	√	√	√		
	TAUD2O10	O		√	√	√	√	√	√	√			
	TAUD2O11	O		√	√	√	√	√	√	√			
	TAUD2O12	O		√	√	√	√	√	√	√			√
	TAUD2O13	O		√	√	√	√	√	√	√	√		√
	TAUD2O14	O		√	√	√	√	√	√	√	√	√	√
	TAUD2O15	O		√	√	√	√	√	√	√	√	√	
TAUJ	TAUJ0I0	I	TAUJ0 channel input	√	√	√	√	√	√	√			√
	TAUJ0I1	I		√	√	√	√	√	√	√	√		√
	TAUJ0I2	I		√	√	√	√	√	√	√	√	√	√
	TAUJ0I3	I		√	√	√	√	√	√	√	√	√	√
	TAUJ0O0	O	TAUJ0 channel output	√	√	√	√	√	√	√			√
	TAUJ0O1	O		√	√	√	√	√	√	√	√		√
	TAUJ0O2	O		√	√	√	√	√	√	√	√	√	√
	TAUJ0O3	O		√	√	√	√	√	√	√	√	√	√
	TAUJ1I0	I	TAUJ1 channel input	√	√	√	√	√	√	√	√	√	√
	TAUJ1I1	I		√	√	√	√	√	√	√	√	√	√
	TAUJ1I2	I		√	√	√	√	√	√	√	√	√	√
	TAUJ1I3	I		√	√	√	√	√	√	√	√	√	√
	TAUJ1O0	O	TAUJ1 channel output	√	√	√	√	√	√	√	√	√	√
	TAUJ1O1	O		√	√	√	√	√	√	√	√	√	√
	TAUJ1O2	O		√	√	√	√	√	√	√	√	√	√
	TAUJ1O3	O		√	√	√	√	√	√	√	√	√	√
	TAUJ2I0	I	TAUJ2 channel input	√	√	√	√	√	√	√	√	√	√
	TAUJ2I1	I		√	√	√	√	√	√	√	√	√	√
	TAUJ2I2	I		√	√	√	√	√	√	√	√	√	√
	TAUJ2I3	I		√	√	√	√	√	√	√	√		√
	TAUJ2O0	O	TAUJ2 channel output	√	√	√	√	√	√	√	√	√	√
	TAUJ2O1	O		√	√	√	√	√	√	√	√	√	√
	TAUJ2O2	O		√	√	√	√	√	√	√	√	√	√
	TAUJ2O3	O		√	√	√	√	√	√	√	√		√

Table 2.1 Pin Function Name Definition (24/35)

Category	Function name	I/O	Explanation	RH850/ U2A-EVA (BGA516)	RH850/ U2A16 (BGA516)	RH850/ U2A16 (BGA373)	RH850/ U2A16 (BGA292)	RH850/ U2A8 (BGA373)	RH850/ U2A8 (BGA292)	RH850/ U2A6 (BGA292)	RH850/ U2A6 (QFP176)	RH850/ U2A6 (BGA156)	RH850/ U2A6 (QFP144)
TAUJ	TAUJ3I0	I	TAUJ3 channel input	√	√	√	√	√	√	√	√	√	√
	TAUJ3I1	I		√	√	√	√	√	√	√	√	√	√
	TAUJ3I2	I		√	√	√	√	√	√	√	√	√	√
	TAUJ3I3	I		√	√	√	√	√	√	√	√	√	√
	TAUJ3O0	O	TAUJ3 channel output	√	√	√	√	√	√	√	√	√	√
	TAUJ3O1	O		√	√	√	√	√	√	√	√	√	√
	TAUJ3O2	O		√	√	√	√	√	√	√	√	√	√
	TAUJ3O3	O		√	√	√	√	√	√	√	√	√	√
TSG3	TSG30O0	O	TSG30 timer up / down status output	√	√	√	√	√	√	√	√		
	TSG30O1	O		√	√	√	√	√	√	√	√		
	TSG30O2	O		√	√	√	√	√	√	√	√		
	TSG30O3	O		√	√	√	√	√	√	√	√		
	TSG30O4	O		√	√	√	√	√	√	√	√		
	TSG30O5	O		√	√	√	√	√	√	√	√		
	TSG30O6	O		√	√	√	√	√	√	√	√		
	TSG30O7	O		√	√	√	√	√	√	√	√		
	TSG30PTSI0	I	TSG30 hall sensor input	√	√	√	√	√	√	√			
	TSG30PTSI1	I		√	√	√	√	√	√	√			
	TSG30PTSI2	I		√	√	√	√	√	√	√			
	TSG30CLKI	I	TSG30 external clock input enable	√	√	√	√	√	√	√			
	TSG31O0	O	TSG31 timer up / down status output	√	√	√	√	√	√	√	√	√	√
	TSG31O1	O		√	√	√	√	√	√	√	√	√	√
	TSG31O2	O		√	√	√	√	√	√	√	√	√	√
	TSG31O3	O		√	√	√	√	√	√	√	√	√	√
	TSG31O4	O		√	√	√	√	√	√	√	√	√	√
	TSG31O5	O		√	√	√	√	√	√	√	√	√	√
	TSG31O6	O		√	√	√	√	√	√	√	√	√	√
	TSG31O7	O		√	√	√	√	√	√	√	√	√	√
	TSG31PTSI0	I	TSG31 hall sensor input	√	√	√	√	√	√	√	√		√
	TSG31PTSI1	I		√	√	√	√	√	√	√	√		√
	TSG31PTSI2	I		√	√	√	√	√	√	√	√		√
	TSG31CLKI	I	TSG31 external clock input enable	√	√	√	√	√	√	√	√	√	√
TPBA	TPBA0O	O	TPBA0 timer pattern buffer output	√	√	√	√	√	√	√	√	√	√
	TPBA1O	O	TPBA1 timer pattern buffer output	√	√	√	√	√	√	√	√	√	√
GTM	GTM0I0	I	GTM0 timer input signals for TIM0	√	√	√	√	√	√	√	√	√	√
	GTM0I1	I		√	√	√	√	√	√	√	√	√	√
	GTM0I2	I		√	√	√	√	√	√	√	√	√	√
	GTM0I3	I		√	√	√	√	√	√	√	√	√	√
	GTM0I4	I		√	√	√	√	√	√	√	√	√	√
	GTM0I5	I		√	√	√	√	√	√	√	√	√	√
	GTM0I6	I		√	√	√	√	√	√	√	√	√	√
	GTM0I7	I		√	√	√	√	√	√	√	√	√	√

Table 2.1 Pin Function Name Definition (25/35)

Category	Function name	I/O	Explanation	RH850/ U2A-EVA (BGA516)	RH850/ U2A16 (BGA516)	RH850/ U2A16 (BGA373)	RH850/ U2A16 (BGA292)	RH850/ U2A8 (BGA373)	RH850/ U2A8 (BGA292)	RH850/ U2A6 (BGA292)	RH850/ U2A6 (QFP176)	RH850/ U2A6 (BGA156)	RH850/ U2A6 (QFP144)
GTM	GTM1I0	I	GTM0 timer input signals for TIM1	√	√	√	√	√	√	√	√	√	√
	GTM1I1	I		√	√	√	√	√	√	√	√	√	√
	GTM1I2	I		√	√	√	√	√	√	√	√	√	√
	GTM1I3	I		√	√	√	√	√	√	√	√	√	√
	GTM1I4	I		√	√	√	√	√	√	√	√	√	√
	GTM1I5	I		√	√	√	√	√	√	√	√	√	√
	GTM1I6	I		√	√	√	√	√	√	√	√	√	√
	GTM1I7	I		√	√	√	√	√	√	√	√	√	√
	GTM2I0	I	GTM0 timer input signals for TIM2	√	√	√	√	√	√	√	√		√
	GTM2I1	I		√	√	√	√	√	√	√	√	√	√
	GTM2I2	I		√	√	√	√	√	√	√	√	√	√
	GTM2I3	I		√	√	√	√	√	√	√	√		√
	GTM2I4	I		√	√	√	√	√	√	√	√	√	√
	GTM2I5	I		√	√	√	√	√	√	√	√	√	√
	GTM2I6	I		√	√	√	√	√	√	√	√	√	√
	GTM2I7	I		√	√	√	√	√	√	√	√	√	√
	GTM3I0	I	GTM0 timer input signals for TIM3	√	√	√	√	√	√	√			√
	GTM3I1	I		√	√	√	√	√	√	√			√
	GTM3I2	I		√	√	√	√	√	√	√			√
	GTM3I3	I		√	√	√	√	√	√	√			√
	GTM3I4	I		√	√	√	√	√	√	√	√	√	√
	GTM3I5	I		√	√	√	√	√	√	√	√	√	√
	GTM3I6	I		√	√	√	√	√	√	√	√	√	√
	GTM3I7	I		√	√	√	√	√	√	√	√	√	√
	GTMAT0O0	O	GTM0 timer output signals for ATOM0	√	√	√	√	√	√	√	√	√	√
	GTMAT0O1	O		√	√	√	√	√	√	√	√	√	√
	GTMAT0O2	O		√	√	√	√	√	√	√	√	√	√
	GTMAT0O3	O		√	√	√	√	√	√	√	√	√	√
	GTMAT0O4	O		√	√	√	√	√	√	√	√	√	√
	GTMAT0O5	O		√	√	√	√	√	√	√	√	√	√
	GTMAT0O6	O		√	√	√	√	√	√	√	√	√	√
	GTMAT0O7	O		√	√	√	√	√	√	√	√		√
	GTMAT1O0	O	GTM0 timer output signals for ATOM1	√	√	√	√	√	√	√	√	√	√
	GTMAT1O1	O		√	√	√	√	√	√	√	√	√	√
	GTMAT1O2	O		√	√	√	√	√	√	√	√	√	√
	GTMAT1O3	O		√	√	√	√	√	√	√	√	√	√
	GTMAT1O4	O		√	√	√	√	√	√	√	√	√	√
	GTMAT1O5	O		√	√	√	√	√	√	√	√		
	GTMAT1O6	O		√	√	√	√	√	√	√	√		
	GTMAT1O7	O		√	√	√	√	√	√	√	√		

Table 2.1 Pin Function Name Definition (26/35)

Category	Function name	I/O	Explanation	RH850/ U2A-EVA (BGA516)	RH850/ U2A16 (BGA516)	RH850/ U2A16 (BGA373)	RH850/ U2A16 (BGA292)	RH850/ U2A8 (BGA373)	RH850/ U2A8 (BGA292)	RH850/ U2A6 (BGA292)	RH850/ U2A6 (QFP176)	RH850/ U2A6 (BGA156)	RH850/ U2A6 (QFP144)
GTM	GTMAT2O0	O	GTM0 timer output signals for ATOM2	√	√	√	√	√	√	√	√		√
	GTMAT2O1	O		√	√	√	√	√	√	√	√	√	
	GTMAT2O2	O		√	√	√	√	√	√	√	√	√	√
	GTMAT2O3	O		√	√	√	√	√	√	√	√	√	
	GTMAT2O4	O		√	√	√	√	√	√	√	√		
	GTMAT2O5	O		√	√	√	√	√	√	√			√
	GTMAT2O6	O		√	√	√	√	√	√	√			
	GTMAT2O7	O		√	√	√	√	√	√	√			
	GTMAT3O0	O	GTM0 timer output signals for ATOM3	√	√	√	√	√	√	√	√		√
	GTMAT3O1	O		√	√	√	√	√	√	√	√	√	√
	GTMAT3O2	O		√	√	√	√	√	√	√	√	√	√
	GTMAT3O3	O		√	√	√	√	√	√	√	√		√
	GTMAT3O4	O		√	√	√	√	√	√	√	√		√
	GTMAT3O5	O		√	√	√	√	√	√	√	√	√	√
	GTMAT3O6	O		√	√	√	√	√	√	√	√	√	√
	GTMAT3O7	O		√	√	√	√	√	√	√	√	√	√
	GTMAT0O0N	O	GTM0 Inverted timer output signals for ATOM0	√	√	√	√	√	√	√	√	√	√
	GTMAT0O1N	O		√	√	√	√	√	√	√	√	√	√
	GTMAT0O2N	O		√	√	√	√	√	√	√	√	√	√
	GTMAT0O3N	O		√	√	√	√	√	√	√	√	√	√
	GTMAT0O4N	O		√	√	√	√	√	√	√	√	√	√
	GTMAT0O5N	O		√	√	√	√	√	√	√	√	√	√
	GTMAT0O6N	O		√	√	√	√	√	√	√	√	√	√
	GTMAT0O7N	O		√	√	√	√	√	√	√	√	√	√
	GTMAT1O0N	O	GTM0 Inverted timer output signals for ATOM1	√	√	√	√	√	√	√	√	√	√
	GTMAT1O1N	O		√	√	√	√	√	√	√	√	√	√
	GTMAT1O2N	O		√	√	√	√	√	√	√	√	√	√
	GTMAT1O3N	O		√	√	√	√	√	√	√	√	√	√
	GTMAT1O4N	O		√	√	√	√	√	√	√	√	√	√
	GTMAT1O5N	O		√	√	√	√	√	√	√	√	√	√
	GTMAT1O6N	O		√	√	√	√	√	√	√	√	√	√
	GTMAT1O7N	O		√	√	√	√	√	√	√	√	√	√
	GTMAT2O0N	O	GTM0 Inverted timer output signals for ATOM2	√	√	√	√	√	√	√	√	√	
	GTMAT2O1N	O		√	√	√	√	√	√	√	√	√	√
	GTMAT2O2N	O		√	√	√	√	√	√	√	√	√	
	GTMAT2O3N	O		√	√	√	√	√	√	√	√	√	
	GTMAT2O4N	O		√	√	√	√	√	√	√	√		√
	GTMAT2O5N	O		√	√	√	√	√	√	√	√	√	√
	GTMAT2O6N	O		√	√	√	√	√	√	√			
	GTMAT2O7N	O		√	√	√	√	√	√	√	√		√
	GTMAT3O0N	O	GTM0 Inverted timer output signals for ATOM3	√	√	√	√	√	√	√	√	√	√
	GTMAT3O1N	O		√	√	√	√	√	√	√	√	√	√
	GTMAT3O2N	O		√	√	√	√	√	√	√	√		
	GTMAT3O3N	O		√	√	√	√	√	√	√	√	√	
	GTMAT3O4N	O		√	√	√	√	√	√	√	√	√	√

Table 2.1 Pin Function Name Definition (27/35)

Category	Function name	I/O	Explanation	RH850/ U2A-EVA (BGA516)	RH850/ U2A16 (BGA516)	RH850/ U2A16 (BGA373)	RH850/ U2A16 (BGA292)	RH850/ U2A8 (BGA373)	RH850/ U2A8 (BGA292)	RH850/ U2A6 (BGA292)	RH850/ U2A6 (QFP176)	RH850/ U2A6 (BGA156)	RH850/ U2A6 (QFP144)
GTM	GTMAT3O5N	O	GTM0 Inverted timer output signals for ATOM3	√	√	√	√	√	√	√	√		√
	GTMAT3O6N	O		√	√	√	√	√	√	√	√	√	√
	GTMAT3O7N	O		√	√	√	√	√	√	√	√	√	√
	GTMECLK0	O	GTM0 external clock	√	√	√	√	√	√	√	√		
	GTMECLK1	O		√	√	√	√	√	√	√	√		√
	GTMECLK2	O		√	√	√	√	√	√	√	√		
RTCA	RTCA0OUT	O	RTCA0 1-Hz pulse output	√	√	√	√	√	√	√	√	√	√
ENCA	ENCA0E0	I	ENCA0 encoder input	√	√	√	√	√	√	√			
	ENCA0E1	I		√	√	√	√	√	√	√			
	ENCA0EC	I	ENCA0 encoder clear input	√	√	√	√	√	√	√			
	ENCA0TIN0	I	ENCA0 capture trigger input	√	√	√	√	√	√	√			
	ENCA0TIN1	I		√	√	√	√	√	√	√			
	ENCA1E0	I	ENCA1 encoder input	√	√	√	√	√	√	√	√		√
	ENCA1E1	I		√	√	√	√	√	√	√	√		√
	ENCA1EC	I	ENCA1 encoder clear input	√	√	√	√	√	√	√	√		√
	ENCA1TIN0	I	ENCA1 capture trigger input	√	√	√	√	√	√	√	√		√
	ENCA1TIN1	I		√	√	√	√	√	√	√	√		√
PIC	TAPA0UN	O	Motor control output U phase (negative)	√	√	√	√	√	√	√	√		
	TAPA0UP	O	Motor control output U phase (positive)	√	√	√	√	√	√	√	√		
	TAPA0VN	O	Motor control output V phase (negative)	√	√	√	√	√	√	√	√		
	TAPA0VP	O	Motor control output V phase (positive)	√	√	√	√	√	√	√	√		
	TAPA0WN	O	Motor control output W phase (negative)	√	√	√	√	√	√	√	√		
	TAPA0WP	O	Motor control output W phase (positive)	√	√	√	√	√	√	√	√		
	TAPA0ESO	I	TAUD0/TSG30 emergency shut-off	√	√	√	√	√	√	√	√		
	TAPA1ESO	I	TAUD1/TSG31 emergency shut-off	√	√	√	√	√	√	√			
	$\overline{\text{ESO0}}$	I	ATOM emergency shut-off	√	√	√	√	√	√	√	√		
	$\overline{\text{ESO1}}$	I		√	√	√	√	√	√	√	√	√	√
	$\overline{\text{ESO2}}$	I		√	√	√	√	√	√	√	√	√	√
	$\overline{\text{ESO3}}$	I		√	√	√	√	√	√	√	√		
PWM-Diag	PWGC0O	O	PWGC0 output	√	√	√	√	√	√	√	√	√	√
	PWGC1O	O	PWGC1 output	√	√	√	√	√	√	√	√		
	PWGC2O	O	PWGC2 output	√	√	√	√	√	√	√	√		√
	PWGC3O	O	PWGC3 output	√	√	√	√	√	√	√	√		
	PWGC4O	O	PWGC4 output	√	√	√	√	√	√	√	√		
	PWGC5O	O	PWGC5 output	√	√	√	√	√	√	√	√		
	PWGC6O	O	PWGC6 output	√	√	√	√	√	√	√	√		
	PWGC7O	O	PWGC7 output	√	√	√	√	√	√	√	√		
	PWGC8O	O	PWGC8 output	√	√	√	√	√	√	√	√		

Table 2.1 Pin Function Name Definition (28/35)

Category	Function name	I/O	Explanation	RH850/ U2A-EVA (BGA516)	RH850/ U2A16 (BGA516)	RH850/ U2A16 (BGA373)	RH850/ U2A16 (BGA292)	RH850/ U2A8 (BGA373)	RH850/ U2A8 (BGA292)	RH850/ U2A6 (BGA292)	RH850/ U2A6 (QFP176)	RH850/ U2A6 (BGA156)	RH850/ U2A6 (QFP144)
PWM-Diag	PWGC9O	O	PWGC9 output	√	√	√	√	√	√	√			
	PWGC10O	O	PWGC10 output	√	√	√	√	√	√	√			
	PWGC11O	O	PWGC11 output	√	√	√	√	√	√	√	√		√
	PWGC12O	O	PWGC12 output	√	√	√	√	√	√	√	√		√
	PWGC13O	O	PWGC13 output	√	√	√	√	√	√	√	√		√
	PWGC14O	O	PWGC14 output	√	√	√	√	√	√	√	√	√	√
	PWGC15O	O	PWGC15 output	√	√	√	√	√	√	√			√
	PWGC16O	O	PWGC16 output	√	√	√	√	√	√	√			√
	PWGC17O	O	PWGC17 output	√	√	√	√	√	√	√			√
	PWGC18O	O	PWGC18 output	√	√	√	√	√	√	√			√
	PWGC19O	O	PWGC19 output	√	√	√	√	√	√	√	√		√
	PWGC20O	O	PWGC20 output	√	√	√	√	√	√	√	√	√	√
	PWGC21O	O	PWGC21 output	√	√	√	√	√	√	√	√	√	√
	PWGC22O	O	PWGC22 output	√	√	√	√	√	√	√			
	PWGC23O	O	PWGC23 output	√	√	√	√	√	√	√			√
	PWGC24O	O	PWGC24 output	√	√	√	√	√	√	√			
	PWGC25O	O	PWGC25 output	√	√	√	√	√	√	√			
	PWGC26O	O	PWGC26 output	√	√	√	√	√	√	√	√		√
	PWGC27O	O	PWGC27 output	√	√	√	√	√	√	√	√	√	√
	PWGC28O	O	PWGC28 output	√	√	√	√	√	√	√	√	√	√
	PWGC29O	O	PWGC29 output	√	√	√	√	√	√	√	√		√
	PWGC30O	O	PWGC30 output	√	√	√	√	√	√	√	√	√	√
	PWGC31O	O	PWGC31 output	√	√	√	√	√	√	√	√	√	√
	PWGC32O	O	PWGC32 output	√	√	√	√	√	√	√	√		
	PWGC33O	O	PWGC33 output	√	√	√	√	√	√	√	√	√	
	PWGC34O	O	PWGC34 output	√	√	√	√	√	√	√	√	√	√
	PWGC35O	O	PWGC35 output	√	√	√	√	√	√	√	√	√	√
	PWGC36O	O	PWGC36 output	√	√	√	√	√	√	√	√	√	√
	PWGC37O	O	PWGC37 output	√	√	√	√	√	√	√	√	√	√
	PWGC38O	O	PWGC38 output	√	√	√	√	√	√	√	√	√	√
	PWGC39O	O	PWGC39 output	√	√	√	√	√	√	√	√	√	√
	PWGC40O	O	PWGC40 output	√	√	√	√	√	√	√	√	√	√
	PWGC41O	O	PWGC41 output	√	√	√	√	√	√	√	√	√	
	PWGC42O	O	PWGC42 output	√	√	√	√	√	√	√	√	√	
	PWGC43O	O	PWGC43 output	√	√	√	√	√	√	√	√	√	
	PWGC44O	O	PWGC44 output	√	√	√	√	√	√	√	√	√	√
	PWGC45O	O	PWGC45 output	√	√	√	√	√	√	√	√	√	√
	PWGC46O	O	PWGC46 output	√	√	√	√	√	√	√	√	√	
	PWGC47O	O	PWGC47 output	√	√	√	√	√	√	√	√		
	PWGC48O	O	PWGC48 output	√	√	√	√	√	√	√	√		√
	PWGC49O	O	PWGC49 output	√	√	√	√	√	√	√	√	√	√
	PWGC50O	O	PWGC50 output	√	√	√	√	√	√	√	√		√
	PWGC51O	O	PWGC51 output	√	√	√	√	√	√	√	√		√
	PWGC52O	O	PWGC52 output	√	√	√	√	√	√	√	√	√	√
	PWGC53O	O	PWGC53 output	√	√	√	√	√	√	√	√	√	√

Table 2.1 Pin Function Name Definition (29/35)

Category	Function name	I/O	Explanation	RH850/ U2A-EVA (BGA516)	RH850/ U2A16 (BGA516)	RH850/ U2A16 (BGA373)	RH850/ U2A16 (BGA292)	RH850/ U2A8 (BGA373)	RH850/ U2A8 (BGA292)	RH850/ U2A6 (BGA292)	RH850/ U2A6 (QFP176)	RH850/ U2A6 (BGA156)	RH850/ U2A6 (QFP144)
PWM-Diag	PWGC54O	O	PWGC54 output	√	√	√	√	√	√	√	√	√	√
	PWGC55O	O	PWGC55 output	√	√	√	√	√	√	√	√	√	√
	PWGC56O	O	PWGC56 output	√	√	√	√	√	√	√	√	√	√
	PWGC57O	O	PWGC57 output	√	√	√	√	√	√	√	√	√	√
	PWGC58O	O	PWGC58 output	√	√	√	√	√	√	√	√	√	√
	PWGC59O	O	PWGC59 output	√	√	√	√	√	√	√	√	√	√
	PWGC60O	O	PWGC60 output	√	√	√	√	√	√	√	√	√	√
	PWGC61O	O	PWGC61 output	√	√	√	√	√	√	√	√	√	√
	PWGC62O	O	PWGC62 output	√	√	√	√	√	√	√	√	√	√
	PWGC63O	O	PWGC63 output	√	√	√	√	√	√	√	√	√	√
	PWGC64O	O	PWGC64 output	√	√	√	√	√	√	√	√		√
	PWGC65O	O	PWGC65 output	√	√	√	√	√	√	√	√	√	√
	PWGC66O	O	PWGC66 output	√	√	√	√	√	√	√	√	√	√
	PWGC67O	O	PWGC67 output	√	√	√	√	√	√	√	√		√
	PWGC68O	O	PWGC68 output	√	√	√	√	√	√	√	√	√	√
	PWGC69O	O	PWGC69 output	√	√	√	√	√	√	√	√	√	√
	PWGC70O	O	PWGC70 output	√	√	√	√	√	√	√			
	PWGC71O	O	PWGC71 output	√	√	√	√	√	√	√	√		√
	PWGC72O	O	PWGC72 output	√	√	√	√	√	√	√	√		√
	PWGC73O	O	PWGC73 output	√	√	√	√	√	√	√	√	√	√
	PWGC74O	O	PWGC74 output	√	√	√	√	√	√	√	√	√	√
	PWGC75O	O	PWGC75 output	√	√	√	√	√	√	√	√		√
	PWGC76O	O	PWGC76 output	√	√	√	√	√	√	√	√		√
	PWGC77O	O	PWGC77 output	√	√	√	√	√	√	√	√	√	√
	PWGC78O	O	PWGC78 output	√	√	√	√	√	√	√	√	√	√
	PWGC79O	O	PWGC79 output	√	√	√	√	√	√	√	√	√	√
	PWGC80O	O	PWGC80 output	√	√	√	√	√	√	√	√	√	√
	PWGC81O	O	PWGC81 output	√	√	√	√	√	√	√	√		√
	PWGC82O	O	PWGC82 output	√	√	√	√	√	√	√	√	√	√
	PWGC83O	O	PWGC83 output	√	√	√	√	√	√	√	√	√	√
	PWGC84O	O	PWGC84 output	√	√	√	√	√	√	√	√	√	
	PWGC85O	O	PWGC85 output	√	√	√	√	√	√	√	√	√	
	PWGC86O	O	PWGC86 output	√	√	√	√	√	√	√	√	√	
	PWGC87O	O	PWGC87 output	√	√	√	√	√	√	√			
	PWGC88O	O	PWGC88 output	√	√	√	√	√	√	√			
	PWGC89O	O	PWGC89 output	√	√	√	√	√	√	√			
	PWGC90O	O	PWGC90 output	√	√	√	√	√	√	√			
	PWGC91O	O	PWGC91 output	√	√	√	√	√	√	√			
	PWGC92O	O	PWGC92 output	√	√	√	√	√	√	√			
	PWGC93O	O	PWGC93 output	√	√	√	√	√	√	√			
	PWGC94O	O	PWGC94 output	√	√	√	√	√	√	√			
	PWGC95O	O	PWGC95 output	√	√	√	√	√	√	√			

Table 2.1 Pin Function Name Definition (30/35)

Category	Function name	I/O	Explanation	RH850/ U2A-EVA (BGA516)	RH850/ U2A16 (BGA516)	RH850/ U2A16 (BGA373)	RH850/ U2A16 (BGA292)	RH850/ U2A8 (BGA373)	RH850/ U2A8 (BGA292)	RH850/ U2A6 (BGA292)	RH850/ U2A6 (QFP176)	RH850/ U2A6 (BGA156)	RH850/ U2A6 (QFP144)
ADCJ	ADCJ0I0	I	ADCJ0 input channel with high accuracy	√	√	√	√	√	√	√	√	√	√
	ADCJ0I1	I		√	√	√	√	√	√	√	√	√	√
	ADCJ0I2	I		√	√	√	√	√	√	√	√	√	√
	ADCJ0I3	I		√	√	√	√	√	√	√	√	√	√
	ADCJ0I4	I		√	√	√	√	√	√	√	√	√	√
	ADCJ0I5	I		√	√	√	√	√	√	√	√	√	√
	ADCJ0I6	I		√	√	√	√	√	√	√	√	√	√
	ADCJ0I7	I		√	√	√	√	√	√	√	√	√	√
	ADCJ0I8	I		√	√	√	√	√	√	√	√		√
	ADCJ0I9	I		√	√	√	√	√	√	√	√		√
	ADCJ0I10	I	ADCJ0 input channel with high accuracy	√	√	√	√	√	√	√	√		
	ADCJ0I11	I		√	√	√	√	√	√	√	√		
	ADCJ0I12	I		√	√	√	√	√	√	√	√		
	ADCJ0I13	I		√	√	√	√	√	√	√	√		
	ADCJ0I14	I		√	√	√	√	√	√	√			
	ADCJ0I15	I		√	√	√	√	√	√	√			
	ADCJ0I16	I		√	√	√	√	√	√	√			
	ADCJ0I17	I		√	√	√	√	√	√	√			
	ADCJ0I18	I		√	√	√	√	√	√	√			
	ADCJ0I19	I		√	√	√	√	√	√	√			
	ADCJ0I0S	I	ADCJ0 input channel with low accuracy	√	√	√	√	√	√	√	√	√	
	ADCJ0I1S	I		√	√	√	√	√	√	√	√	√	
	ADCJ0I2S	I		√	√	√	√	√	√	√	√	√	
	ADCJ0I3S	I		√	√	√	√	√	√	√	√	√	√
	ADCJ0I4S	I		√	√	√	√	√	√	√	√	√	√
	ADCJ0I5S	I		√	√	√	√	√	√	√	√	√	
	ADCJ0I6S	I		√	√	√	√	√	√	√	√		
	ADCJ0I7S	I		√	√	√	√	√	√	√	√		√
	ADCJ0I8S	I		√	√	√	√	√	√	√	√		
	ADCJ0I9S	I		√	√	√	√	√	√	√	√		
	ADCJ0SEL0	O	ADCJ0 external analog multiplexer (MPX) output	√	√	√	√	√	√	√	√		√
	ADCJ0SEL1	O		√	√	√	√	√	√	√	√		√
	ADCJ0SEL2	O		√	√	√	√	√	√	√	√	√	√
	ADCJ0TRG0	I	ADCJ0 external trigger	√	√	√	√	√	√	√	√	√	√
	ADCJ0TRG1	I		√	√	√	√	√	√	√	√	√	√
	ADCJ0TRG2	I		√	√	√	√	√	√	√	√	√	√
	ADCJ0TRG3	I		√	√	√	√	√	√	√	√		√
	ADCJ0TRG4	I		√	√	√	√	√	√	√	√	√	√
	ADCJ0CNV0	O	ADCJ0 conversion timing monitor	√	√	√	√	√	√	√	√		√
	ADCJ0CNV1	O		√	√	√	√	√	√	√			
	ADCJ0CNV2	O		√	√	√	√	√	√	√			
	ADCJ0CNV3	O		√	√	√	√	√	√	√			
	ADCJ0CNV4	O		√	√	√	√	√	√	√			
	A0VREFH	I	ADCJ0 reference voltage pin for the analog part	√	√	√	√	√	√	√	√	√	√

Table 2.1 Pin Function Name Definition (31/35)

Category	Function name	I/O	Explanation	RH850/ U2A-EVA (BGA516)	RH850/ U2A16 (BGA516)	RH850/ U2A16 (BGA373)	RH850/ U2A16 (BGA292)	RH850/ U2A8 (BGA373)	RH850/ U2A8 (BGA292)	RH850/ U2A6 (BGA292)	RH850/ U2A6 (QFP176)	RH850/ U2A6 (BGA156)	RH850/ U2A6 (QFP144)
ADCJ	ADCJ1I0	I	ADCJ1 input channel with high accuracy	√	√	√	√	√	√	√	√	√	√
	ADCJ1I1	I		√	√	√	√	√	√	√	√	√	√
	ADCJ1I2	I		√	√	√	√	√	√	√	√	√	√
	ADCJ1I3	I		√	√	√	√	√	√	√	√	√	√
	ADCJ1I4	I		√	√	√	√	√	√	√	√	√	√
	ADCJ1I5	I		√	√	√	√	√	√	√	√	√	√
	ADCJ1I6	I		√	√	√	√	√	√	√	√	√	√
	ADCJ1I7	I		√	√	√	√	√	√	√	√	√	√
	ADCJ1I8	I		√	√	√	√	√	√	√	√		√
	ADCJ1I9	I		√	√	√	√	√	√	√	√		√
	ADCJ1I10	I		√	√	√	√	√	√	√	√		
	ADCJ1I11	I	ADCJ1 input channel with high accuracy	√	√	√	√	√	√	√	√		
	ADCJ1I12	I		√	√	√	√	√	√	√	√		
	ADCJ1I13	I		√	√	√	√	√	√	√	√		
	ADCJ1I14	I		√	√	√	√	√	√	√			
	ADCJ1I15	I		√	√	√	√	√	√	√			
	ADCJ1I16	I		√	√	√	√	√	√	√			
	ADCJ1I17	I		√	√	√	√	√	√	√			
	ADCJ1I18	I		√	√	√	√	√	√	√			
	ADCJ1I19	I		√	√	√	√	√	√	√			
	ADCJ1I0S	I	ADCJ1 input channel with low accuracy	√	√	√	√	√	√	√	√	√	√
	ADCJ1I1S	I		√	√	√	√	√	√	√	√		
	ADCJ1I2S	I		√	√	√	√	√	√	√	√		
	ADCJ1I3S	I		√	√	√	√	√	√	√	√	√	√
	ADCJ1I4S	I		√	√	√	√	√	√	√	√	√	√
	ADCJ1I5S	I		√	√	√	√	√	√	√	√		
	ADCJ1I6S	I		√	√	√	√	√	√	√	√		√
	ADCJ1I7S	I		√	√	√	√	√	√	√	√	√	√
	ADCJ1I8S	I		√	√	√	√	√	√	√	√		√
	ADCJ1I9S	I		√	√	√	√	√	√	√	√	√	√
	ADCJ1I10S	I		√	√	√	√	√	√	√	√	√	√
	ADCJ1I11S	I		√	√	√	√	√	√	√	√		
	ADCJ1I12S	I		√	√	√	√	√	√	√	√	√	√
	ADCJ1I13S	I		√	√	√	√	√	√	√	√		√
	ADCJ1SEL0	O	ADCJ1 external analog multiplexer (MPX) output	√	√	√	√	√	√	√	√	√	√
	ADCJ1SEL1	O		√	√	√	√	√	√	√	√	√	√
	ADCJ1SEL2	O		√	√	√	√	√	√	√	√		
	ADCJ1TRG0	I	ADCJ1 external trigger	√	√	√	√	√	√	√	√		√
	ADCJ1TRG1	I		√	√	√	√	√	√	√	√		√
	ADCJ1TRG2	I		√	√	√	√	√	√	√	√		√
	ADCJ1TRG3	I		√	√	√	√	√	√	√	√	√	√
	ADCJ1TRG4	I		√	√	√	√	√	√	√	√	√	√

Table 2.1 Pin Function Name Definition (32/35)

Category	Function name	I/O	Explanation	RH850/ U2A-EVA (BGA516)	RH850/ U2A16 (BGA516)	RH850/ U2A16 (BGA373)	RH850/ U2A16 (BGA292)	RH850/ U2A8 (BGA373)	RH850/ U2A8 (BGA292)	RH850/ U2A6 (BGA292)	RH850/ U2A6 (QFP176)	RH850/ U2A6 (BGA156)	RH850/ U2A6 (QFP144)
ADCJ	ADCJ1CNV0	O	ADCJ1 conversion timing monitor	√	√	√	√	√	√	√			
	ADCJ1CNV1	O		√	√	√	√	√	√	√			
	ADCJ1CNV2	O		√	√	√	√	√	√	√			
	ADCJ1CNV3	O		√	√	√	√	√	√	√			
	ADCJ1CNV4	O		√	√	√	√	√	√	√			
	A1VREFH	I	ADCJ1 reference voltage pin for the analog part	√	√	√	√	√	√	√	√	√	√
	ADCJ2I0	I	ADCJ2 input channel with high accuracy	√	√	√	√	√	√	√	√		
	ADCJ2I1	I		√	√	√	√	√	√	√	√		
	ADCJ2I2	I		√	√	√	√	√	√	√	√		
	ADCJ2I3	I		√	√	√	√	√	√	√	√		
	ADCJ2I4	I		√	√	√	√	√	√	√	√		
	ADCJ2I5	I		√	√	√		√					
	ADCJ2I6	I		√	√	√		√					
	ADCJ2I7	I		√	√	√		√					
	ADCJ2I8	I	ADCJ2 input channel with high accuracy	√	√	√		√					
	ADCJ2I9	I		√	√	√		√					
	ADCJ2I10	I		√	√	√		√					
	ADCJ2I11	I		√	√	√		√					
	ADCJ2I12	I		√	√	√		√					
	ADCJ2I13	I		√	√	√		√					
	ADCJ2I14	I		√	√	√		√					
	ADCJ2I15	I		√	√	√		√					
	ADCJ2I16	I		√	√	√		√					
	ADCJ2I17	I		√	√	√		√					
	ADCJ2I18	I		√	√	√		√					
	ADCJ2I19	I		√	√	√		√					
	ADCJ2I0S	I	ADCJ2 input channel with low accuracy	√	√	√	√	√	√	√	√		√
	ADCJ2I1S	I		√	√	√	√	√	√	√			
	ADCJ2I2S	I		√	√	√	√	√	√	√			
	ADCJ2I3S	I		√	√	√	√	√	√	√			√
	ADCJ2I4S	I		√	√	√	√	√	√	√	√		√
	ADCJ2I5S	I		√	√	√	√	√	√	√	√		√
	ADCJ2I6S	I		√	√	√	√	√	√	√	√		
	ADCJ2I7S	I		√	√	√	√	√	√	√	√		√
	ADCJ2I8S	I		√	√	√	√	√	√	√	√		√
	ADCJ2I9S	I		√	√	√	√	√	√	√	√		
	ADCJ2SEL0	O	ADCJ2 external analog multiplexer (MPX) output	√	√	√	√	√	√	√	√		√
	ADCJ2SEL1	O		√	√	√	√	√	√	√	√		
	ADCJ2SEL2	O		√	√	√	√	√	√	√	√		√
	ADCJ2TRG0	I	ADCJ2 external trigger	√	√	√	√	√	√	√	√		
	ADCJ2TRG1	I		√	√	√	√	√	√	√	√		
	ADCJ2TRG2	I		√	√	√	√	√	√	√	√		
	ADCJ2TRG3	I		√	√	√	√	√	√	√	√		
	ADCJ2TRG4	I		√	√	√	√	√	√	√	√		

Table 2.1 Pin Function Name Definition (33/35)

Category	Function name	I/O	Explanation	RH850/U2A-EVA (BGA516)	RH850/U2A16 (BGA516)	RH850/U2A16 (BGA373)	RH850/U2A16 (BGA292)	RH850/U2A8 (BGA373)	RH850/U2A8 (BGA292)	RH850/U2A6 (BGA292)	RH850/U2A6 (QFP176)	RH850/U2A6 (BGA156)	RH850/U2A6 (QFP144)
ADCJ	ADCJ2CNV0	O	ADCJ2 conversion timing monitor	√	√	√	√	√	√	√	√		
	ADCJ2CNV1	O		√	√	√	√	√	√	√	√		
	ADCJ2CNV2	O		√	√	√	√	√	√	√	√		√
	ADCJ2CNV3	O		√	√	√	√	√	√	√	√		√
	ADCJ2CNV4	O		√	√	√	√	√	√	√	√		√
	A2VREFH	I	ADCJ2 reference voltage pin for the analog part	√	√	√	√	√	√	√	√		√
ECM	$\overline{\text{ERROROUT\_M}}$	O	Error output master signal	√	√	√	√	√	√	√	√	√	√
	$\overline{\text{ERROROUT\_C}}$	O	Error output checker signal	√	√	√	√	√	√	√	√	√	√
	$\overline{\text{ERRORIN0}}$	I	External error input signal	√	√	√	√	√	√	√	√	√	√
	$\overline{\text{ERRORIN1}}$	I		√	√	√	√	√	√	√	√	√	√
	$\overline{\text{ERRORIN2}}$	I		√	√	√	√						
	$\overline{\text{ERRORIN3}}$	I		√	√	√	√						
FLASH	FPDT	O	Transmit data output (2-wire UATR, CSI)	√	√	√	√	√	√	√	√	√	√
	FPDR	I	Receive data input (2-wire UATR, CSI)	√	√	√	√	√	√	√	√	√	√
	FPCK	I	Serial clock input (CSI)	√	√	√	√	√	√	√	√	√	√
Debug	$\overline{\text{TRST}}$	I	Test reset input	√	√	√	√	√	√	√	√	√	√
	TDI	I	Test data input	√	√	√	√	√	√	√	√	√	√
	TDO	O	Test data output	√	√	√	√	√	√	√	√	√	√
	TCK	I	Test clock input	√	√	√	√	√	√	√	√	√	√
	TMS	I	Test mode select input	√	√	√	√	√	√	√	√	√	√
	$\overline{\text{RDY}}$	O	Ready output	√	√	√	√	√	√	√	√	√	√
	$\overline{\text{EVTI}}$	I	Event trigger input	√	√								
	$\overline{\text{EVTO}}$	O	Even trigger output	√	√								
	$\overline{\text{LPDRST}}$	I	Test reset input	√	√	√	√	√	√	√	√	√	√
	LPDCLKO	O	LPD 4 pin clock output	√	√	√	√	√	√	√	√	√	√
	LPDI	I	LPD 4 pin data input	√	√	√	√	√	√	√	√	√	√
	LPDO	O	LPD 4 pin data output	√	√	√	√	√	√	√	√	√	√
	LPDCLKI	I	LPD 4 pin clock input	√	√	√	√	√	√	√	√	√	√
AUDR	$\overline{\text{AUDRST}}$	I	AUDR reset signal	√									
	$\overline{\text{AUDSYNC}}$	I	AUDR synchronous signal	√									
	AUDCK	I	AUDR clock signal	√									
	AUDATA0	IO	AUDR data signal	√									
	AUDATA1	IO		√									
	AUDATA2	IO		√									
	AUDATA3	IO		√									

Table 2.1 Pin Function Name Definition (34/35)

Category	Function name	I/O	Explanation	RH850/ U2A-EVA (BGA516)	RH850/ U2A16 (BGA516)	RH850/ U2A16 (BGA373)	RH850/ U2A16 (BGA292)	RH850/ U2A8 (BGA373)	RH850/ U2A8 (BGA292)	RH850/ U2A6 (BGA292)	RH850/ U2A6 (QFP176)	RH850/ U2A6 (BGA156)	RH850/ U2A6 (QFP144)
Aurora	CICREFP	I	Trace I/F clock pos	√									
	CICREFN	I	Trace I/F clock neg	√									
	TODP0	O	Trace I/F data pos 0	√									
	TODN0	O	Trace I/F data neg 0	√									
	TODP1	O	Trace I/F data pos 1	√									
	TODN1	O	Trace I/F data neg 1	√									
	TODP2	O	Trace I/F data pos 2	√									
	TODN2	O	Trace I/F data neg 2	√									
	TODP3	O	Trace I/F data pos 3	√									
	TODN3	O	Trace I/F data neg 3	√									
	$\overline{\text{MSYN}}$	I	Trace I/F Synchronization request	√									
	$\overline{\text{AURORES1}}$	I	EMUVDD domain reset signal	√									
	$\overline{\text{AURORES2}}$	I	EMUVDD domain core signal isolation	√									
	$\overline{\text{AURORESPD}}$	I	Core domain EMUVDD signal isolation	√									
ERAM	$\overline{\text{ERAMRESPD}}$	I	Core domain ERAMVDD signal isolation	√									
	$\overline{\text{ERAMRES2}}$	I	ERAMVDD domain core signal isolation	√									
Power	SYSVCC	-	Power supply for System Logic, Internal voltage regulator and SVR power	√	√	√	√	√	√	√	√	√	√
	VCC	-	Power supply for FLASH	√	√	√	√	√	√	√	√	√	√
	VDD	-	Power supply terminal for core	√	√	√	√	√	√	√	√	√	√
	VSS	-	Common Ground	√	√	√	√	√	√	√	√	√	√
	SVRAVCC	-	Power supply for SVR	√	√	√	√	√	√	√	√	√	√
	SVRDRVCC	-		√	√	√	√	√	√	√	√	√	√
	SVRAVSS	-	Ground for SVR	√	√	√	√	√	√	√	√	√	√
	SVRDRVSS	-		√	√	√	√	√	√	√	√	√	√
	AWOVCL	-	External buffer capacitance of regulator	√	√	√	√	√	√	√	√	√	√

Table 2.1 Pin Function Name Definition (35/35)

Category	Function name	I/O	Explanation	RH850/ U2A-EVA (BGA516)	RH850/ U2A16 (BGA516)	RH850/ U2A16 (BGA373)	RH850/ U2A16 (BGA292)	RH850/ U2A8 (BGA373)	RH850/ U2A8 (BGA292)	RH850/ U2A6 (BGA292)	RH850/ U2A6 (QFP176)	RH850/ U2A6 (BGA156)	RH850/ U2A6 (QFP144)
Power	E0VCC	-	Power supply for I/O port	√	√	√	√	√	√	√	√	√	√
	E1VCC	-		√	√	√	√	√	√	√	√	√	√
	E2VCC	-		√	√	√	√	√	√	√	√	√	√
	LVDVCC	-	Power supply for LVDS	√	√	√	√	√	√				
	A0VCC	-	Power supply for A/D converters	√	√	√	√	√	√	√			
	A1VCC	-		√	√	√	√	√	√	√			
	A2VCC	-		√	√	√	√	√	√	√			
	A0VSS	-	Ground for A/D converters	√	√	√	√	√	√	√	√	√	√
	A1VSS	-		√	√	√	√	√	√	√	√	√	√
	A2VSS	-		√	√	√	√	√	√	√	√		√
	GETH0PVCC	-	Power supply for Ethernet	√	√	√	√	√	√				
	GETH0RVCC	-		√	√	√	√	√	√				
	GETH0BVCC	-		√	√	√	√	√	√				
	GETH0VCL	-		√	√	√	√	√	√				
	DVCC	-	Power supply for Aurora	√									
	DVDD	-		√									
	EMUVCC	-		√									
	EMUVDD	-		√									
	ERAMVDD	-	Power supply for ERAM	√									
	ERAMVCC	-		√									
ICUMHA	ICUMGPIO0	O	ICUMHA GPIO control	√	√	√	√	√	√	√	√	√	√
	ICUMGPIO1	O		√	√	√	√	√	√	√	√	√	√
	ICUMGPIO2	O		√	√	√	√	√	√	√	√	√	√
	ICUMGPIO3	O		√	√	√	√	√	√	√	√	√	√

Section 3 Electrical Characteristics

The specifications in this section are for devices operating under the conditions shown in **Section 3.2.1.1, Supply Voltage Characteristics**. Where a special condition is required for a given specification, the condition will be indicated. Furthermore, the specifications in this section are not guaranteed unless the conditions listed below are met.

3.1 Absolute Maximum Ratings

Conditions:

- VSS = SVRDRVSS = SVRAVSS = AnVSS
- Reference ground potential: VSS = 0 V.

Table 3.1 Absolute Maximum Ratings (1/2)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Power Voltage	$V_{AMRSYSVCC}$	SYSVCC	–0.5		6.5*10	V
	V_{AMRVCC}	VCC	–0.5		6.5*10	V
	V_{AMRVDD}	VDD	–0.5		1.42*11	V
	$V_{AMRE0VCC}$	E0VCC	–0.5		6.5*10	V
	$V_{AMRE1VCC}$	E1VCC	–0.5		6.5*10	V
	$V_{AMRE2VCC}$	E2VCC	–0.5		6.5*10	V
	$V_{AMRLVDVCC}$	LVDVCC	–0.5		6.5*10	V
	$V_{AMRA0VCC}$	A0VCC	–0.5		6.5*10	V
	$V_{AMRA1VCC}$	A1VCC	–0.5		6.5*10	V
	$V_{AMRA2VCC}$	A2VCC	–0.5		6.5*10	V
	$V_{AMRSVRDRVCC}$	SVRDRVCC	–0.5		6.5*10	V
	$V_{AMRSVRAVCC}$	SVRAVCC	–0.5		6.5*10	V
	$V_{AMRDVCC}$	DVCC	–0.5		4.6*12	V
	$V_{AMRDVDD}$	DVDD	–0.5		1.42*11	V
	$V_{AMREMUVCC}$	EMUVCC	–0.5		4.6*12	V
	$V_{AMREMUVDD}$	EMUVDD	–0.5		1.42*11	V
	$V_{AMRERAMVCC}$	ERAMVCC	–0.5		4.6*12	V
	$V_{AMRERAMVDD}$	ERAMVDD	–0.5		1.42*11	V
	$V_{AMRGETH0RVCC}$	GETH0RVCC	–0.5		6.5*10	V
	$V_{AMRGETH0BVCC}$	GETH0BVCC	–0.5		4.6*12	V
	$V_{AMRGETH0PVCC}$	GETH0PVCC	–0.5		6.5*10	V
Input Voltage	V_{AMRI}	E0VCC pin*1	–0.5		E0VCC + 0.5	V
		E1VCC pin*2	–0.5		E1VCC + 0.5	V
		E2VCC pin*3	–0.5		E2VCC + 0.5	V
		$\overline{\text{RESET}}$, FLMD0, X1, X2 PWRCTL pin	–0.5		SYSVCC + 0.5	V
		CICREFN, CICREFP,	–0.5		DVDD+0.3 *9	V
		$\overline{\text{AURORES1}}$, $\overline{\text{AURORES2}}$	–0.5		EMUVCC + 0.5	V
		$\overline{\text{MSYN}}$, $\overline{\text{AURORESPD}}$, $\overline{\text{EVTI}}$, $\overline{\text{EVTO}}$, AUDR I/F*4, $\overline{\text{VMONOUT}}$	–0.5		E0VCC + 0.5	V

Table 3.1 Absolute Maximum Ratings (2/2)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input Voltage	V_{AMRI}	$\overline{ERAMRESPD}$	–0.5		E1VCC + 0.5	V
		$\overline{ERAMRES2}$	–0.5		ERAMVCC + 0.5	V
		RHSIF, MSPI*5	–0.5		LVDVCC + 0.5	V
		SGMII I/F*6	–0.5		GETH0BVCC + 0.5	V
		P3_8 [For U2A-EVA, U2A16 and U2A8 Only]	–0.5		GETH0RVCC + 0.5	V
Analogue reference voltage	$V_{AMRAVREF}$	A0VREFH	–0.5		A0VCC + 0.5	V
		A1VREFH	–0.5		A1VCC + 0.5	V
		A2VREFH	–0.5		A2VCC + 0.5	V
Analogue input voltage	V_{AMRIAN}	A0VCC pins	–0.5		A0VCC + 0.5	V
		A1VCC pins	–0.5		A1VCC + 0.5	V
		A2VCC pins	–0.5		A2VCC + 0.5	V
VSS differential voltage	$V_{VSSDIFF}$		–0.1		0.1	V
Injection current per digital input	I_{INJ_DIN}	*13	–25		25	mA
Injection current per analog input	I_{INJ_AIN}	*13	–25		25	mA
Total Injection current of the device	$\lvert I_{INJ\_TOT} \rvert$	*13			120	mA
Output low current*7	I_{OL1p}	per pin			10	mA
	I_{OLall}	Sum of all output low currents of all EnVCC/ AnVCC pins			200	mA
Output high current*7	I_{OH1p}	per pin			–10	mA
	I_{OHall}	Sum of all output high currents of all EnVCC/ AnVCC pins			–200	mA
Junction temperature	T_j	U2A16 BGA516 U2A16 BGA373 U2A8 BGA373	–40		150	°C
		Other than above	–40		160	°C
Storage temperature*8	T_{stg}	U2A16 BGA516 U2A16 BGA373 U2A8 BGA373	–55		150	°C
		Other than above	–55		160	°C

Note 1. JP0, P0, P1, P2, P3 (except P3_8 [For U2A-EVA, U2A16 and U2A8 Only]), P4, P5, P6, P8

Note 2. P9, P10, P11, P12, P18, P19, P20, 21, P22, P23

Note 3. P24

Note 4. $\overline{AUDRST}$, $\overline{AUDSYNC}$, AUDCK, AUDATA0-AUDATA3

Note 5. RHSIF: HSIF0_TXDP, HSIF0_TXDN, HSIF0_RXDP, HSIF0_RXDN
MSPI: MSPI0_SOP, MSPI0_SON, MSPI0_SIP, MSPI0_SIN, MSPI0_SCKP, MSPI0_SCKN

Note 6. RX_CLKN, RX_CLKP, RX_DATAN, RX_DATAP, TX_DATAN, TX_DATAP and REFCLK.

Note 7. Given specification includes injected currents.

Note 8. After mounting

Note 9. Do not exceed maximum 1.42 V.

Note 10. Voltage overshoot 5.8 V to 6.5 V is permissible, cumulative time is less than 2 h. Voltage overshoot 5.5 V to 5.8 V is permissible, cumulative time is less than 100 h.

Note 11. Voltage overshoot 1.205 V to 1.42 V is permissible, cumulative time is less than 2 h. Voltage overshoot 1.155 V to 1.205 V is permissible, cumulative time is less than 100 h.

Note 12. Voltage overshoot 3.9 V to 4.6 V is permissible, cumulative time is less than 2 h. Voltage overshoot 3.6 V to 3.9 V is permissible, cumulative time is less than 100 h.

Note 13. Input voltage must be kept within -0.8 V ≤ Vin ≤ 6.5 V. Power supply voltage must be kept within rated values. Injection current must be kept within rated values on all states include ramp-up/down, and power-on/off. Injection current effects power dissipation in the package for thermal characteristics.

CAUTION

- **Even momentarily exceeding the absolute maximum rating for just one item creates a threat of failure in the reliability of the products. That is, the absolute maximum ratings are the levels that raise a threat of physical damage to the products. Be sure to use the products only under conditions that do not exceed the ratings. The quality and normal operation of the product are guaranteed under the standards and conditions given as DC and AC characteristics.**
- **Input voltage, analog reference voltage and analog input voltage must not exceed 6.5 V.**
- **Even in case when input voltage does not meet the specified characteristics, it is accepted if the injected current characteristics specified in Section 3.2.7 are met.**

3.2 General & DC Characteristics

3.2.1 Operational Condition

3.2.1.1 Supply Voltage Characteristics

Conditions:

- Temperature range: Tj (min) to Tj (max)
- VSS = SVRDRVSS = SVRAVSS = AnVSS
- Reference ground potential: VSS = 0 V

Table 3.2 Supply Voltage Characteristics (1/2)*1

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
System control supply voltage*6	V_{SYSVCC}	SVR unused*2	3.0		5.5	V
		SVR used*2	3.0		3.6	V
			4.5		5.5	V
Regulator supply voltage	V_{VCC}	SVR unused	3.0		5.5	V
		SVR used	3.0		3.6	V
			4.5		5.5	V
Core supply voltage	V_{VDD}		1.025	1.09	1.155	V
IO supply voltage	V_{E0VCC}		3.0		5.5	V
	V_{E1VCC}					
	V_{E2VCC}					
RHSIF/MSPI LVDS supply voltage	V_{LVDVCC}		3.0		3.6	V
			4.5		5.5	V
ADC supply voltage	V_{A0VCC}		3.0		5.5	V
	V_{A1VCC}					
	V_{A2VCC}					
ADC reference voltage supply	$V_{A0VREFH}$		3.0		5.5	V
	$V_{A1VREFH}$					
	$V_{A2VREFH}$					
SVR supply voltage	$V_{SVRDRVCC}$	*3	3.0		3.6	V
			4.5		5.5	V
	$V_{SVRAVCC}$		3.0		3.6	V
			4.5		5.5	V
Aurora I/F supply voltage (Analog)	V_{DVCC}		3.0		3.6	V
Aurora I/F supply voltage (Digital)	V_{DVDD}	Aurora used	1.04	1.09	1.14	V
		Aurora unused	1.025	1.09	1.155	V
Aurora control IO supply voltage	V_{EMUVCC}		3.0		3.6	V
Aurora control core supply voltage	V_{EMUVDD}	Aurora used	1.04	1.09	1.14	V
		Aurora unused	1.025	1.09	1.155	V
ERAM IO supply voltage*7	$V_{ERAMVCC}$		3.0		3.6	V
ERAM core supply voltage*7	$V_{ERAMVDD}$	Aurora used	1.04	1.09	1.14	V
		Aurora unused	1.025	1.09	1.155	V

Table 3.2 Supply Voltage Characteristics (2/2)*1

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
SGMII supply voltage*5	$V_{GETH0RVCC}$	SGMII used	3.14	3.3	3.46	V
		SGMII unused	3.0		5.5	V
	$V_{GETH0PVCC}$	SGMII used	3.14	3.3	3.46	V
		SGMII unused	3.0		5.5	V
	$V_{GETH0BVCC}$	SGMII used	3.14	3.3	3.46	V
		SGMII unused		*4		V

Note 1. Use this device with the following conditions.
[For U2A-EVA, U2A16 and U2A8 Only]
SVRDRVCC ≥ SYSVCC = VCC = SVRAVCC
A0VCC ≥ A0VREFH ≥ VCC
A0VCC ≥ A0VREFH ≥ E0VCC = LVDVCC
A1VCC ≥ A1VREFH
A2VCC ≥ A2VREFH
GETH0RVCC = GETH0PVCC = GETH0BVCC, when SGMII use.
[For U2A6 Only]
SVRDRVCC ≥ SYSVCC = VCC = SVRAVCC
A0VCC = A0VREFH ≥ VCC
A0VCC = A0VREFH ≥ E0VCC
A1VCC = A1VREFH
A2VCC = A2VREFH

Note 2. SYSVCC is monitored by POC, see **Section 3.2.13, Voltage Detector (POC, VLVI) Characteristics**.

Note 3. Maximum allowable noise for SVRDRVCC is 500mV peak to peak.

Note 4. Input 3.0V to 3.6V voltage or connect to VSS with 1 kΩ or more pull-down resistance.

Note 5. Maximum allowable noise for SGMII power is 50mV peak to peak.

Note 6. Maximum allowable noise for SYSVCC is 100mV peak to peak.When MainOSC is used as the clock source of SGMII, allowable noise for SYSVCC will be 50mV peak to peak.

Note 7. U2A6 has only ERAM core and its supply voltage is V_{VDD}.

CAUTION

During operations, supply the specified voltages to all power lines. When stopping operation, turn off all of the power supplies.

3.2.1.2 Main Oscillator Characteristics

Conditions:

- Supply voltage range: Refer to **Section 3.2.1.1, Supply Voltage Characteristics**.

Table 3.3 Main Oscillator Characteristics (1/3)

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
MainOSC frequency	f_{MOSC} *1,*2	Crystal/Ceramic		16 – 1%		40 + 1%	MHz
		Crystal*5		20 – 100 ppm		20 + 100 ppm	MHz
MainOSC oscillation operating point	V_{MOSCOP}	Crystal/Ceramic			1.217		V
MainOSC oscillation amplitude	$V_{MOSCAMP}$	Crystal/Ceramic		0.9			V
MainOSC oscillation stabilization time	t_{MSTB}	Crystal/Ceramic				5	ms
MainOSC oscillation amplifier reaction time	$t_{MOSCAMP}$	Crystal/Ceramic				200	µs
Internal Capacitor size selectable by MOSC_CAP_SEL setting (OPBT10 setting)	C_{capsel}	MOSC_CAP_SEL [3:0]	= 0000_B	*4	0 (4.0), 0 (5.6)*3	*4	pF
			= 0001_B	*4	1 (4.9), 1 (6.5)*3	*4	pF
			= 0010_B	*4	2 (6.0), 2 (7.6)*3	*4	pF
			= 0011_B	*4	3 (6.9), 3 (8.5)*3	*4	pF
			= 0100_B	*4	4 (7.7), 4 (9.3)*3	*4	pF
			= 0101_B	*4	5 (8.7), 5 (10.2)*3	*4	pF
			= 0110_B	*4	6 (9.8), 6 (11.3)*3	*4	pF
			= 0111_B	*4	7 (10.6), 7 (12.1)*3	*4	pF
			= 1000_B	*4	8 (11.5), 8 (13.1)*3	*4	pF
			= 1001_B	*4	9 (12.6), 9 (14.1)*3	*4	pF
			= 1010_B	*4	10 (13.5), 10 (15.0)*3	*4	pF
Internal damping resistor size selectable by MOSC_RD_SEL_A and MOSC_RD_SEL_B setting (OPBT10 setting)*2	R_{rdsel}	MOSC_RD_SEL_A [2:0] MOSC_RD_SEL_B [2:0] [U2A-EVA only]	= 000_B	169	338	608	Ω
			= 001_B	718	1435	2440	Ω
			= 010_B	1267	2533	4306	Ω
			= 011_B	1711	3422	5475	Ω
			= 100_B	1711	3422	5475	Ω
			= 101_B	1711	3422	5475	Ω
			= 110_B	1711	3422	5475	Ω
			= 111_B	1711	3422	5475	Ω
	R_{rdsel}	MOSC_RD_SEL_A [2:0] MOSC_RD_SEL_B [2:0] U2A16, U2A8 and U2A6]	= 000_B	238	340	578	Ω
			= 001_B	378	540	1026	Ω
			= 010_B	574	820	1435	Ω
			= 011_B	756	1080	1782	Ω
			= 100_B	959	1370	2124	Ω
			= 101_B	1764	2520	3402	Ω
			= 110_B	1764	2520	3402	Ω
			= 111_B	1764	2520	3402	Ω

Table 3.3 Main Oscillator Characteristics (2/3)

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Trans conductance size (g_m) and Output conductance size (g_{ds}) selectable by MOSC_SHTSTBY_A, MOSC_AMPSEL_A, MOSC_SHTSTBY_B and, MOSC_AMPSEL_B setting (OPBT10 setting)*2	g_m, g_{ds}	{MOSC_SHTSTBY_A, MOSC_AMPSEL_A [2:0]} or {MOSC_SHTSTBY_B, MOSC_AMPSEL_B [2:0]} SYSVCC = 3.0 V to 3.6 V	= 0000_B	1.05, 0.079	2.28, 0.153	3.69, 0.452	mS
			= 0001_B	1.66. 0.108	3.58. 0.204	5.78. 0.521	mS
			= 0010_B	2.25, 0.134	4.85, 0.251	7.80, 0.585	mS
			= 0011_B	2.82, 0.158	6.08, 0.294	9.76, 0.645	mS
			= 0100_B	3.73, 0.196	8.07, 0.362	12.91, 0.739	mS
			= 0101_B	4.76, 0.238	10.32, 0.437	16.49, 0.846	mS
			= 0110_B	5.56, 0.271	12.10, 0.496	19.35, 0.929	mS
			= 0111_B	6.33, 0.302	13.81, 0.553	22.08, 1.007	mS
			= 1000_B	3.94, 0.194	8.45, 0.371	13.52, 0.592	mS
			= 1001_B	4.46, 0.215	9.58, 0.409	15.32, 0.651	mS
			= 1010_B	4.97, 0.236	10.69, 0.446	17.07, 0.708	mS
			= 1011_B	5.46, 0.255	11.76, 0.481	18.78, 0.764	mS
			= 1100_B	6.24, 0.286	13.49, 0.538	21.54, 0.852	mS
			= 1101_B	7.12, 0.321	15.46, 0.603	24.71, 0.953	mS
			= 1110_B	7.82, 0.351	17.04, 0.653	27.24, 1.031	mS
			= 1111_B	8.49, 0.377	18.56, 0.701	29.68, 1.105	mS
Trans conductance size (g_m) and Output conductance size (g_{ds}) selectable by MOSC_SHTSTBY_A, MOSC_AMPSEL_A, MOSC_SHTSTBY_B and MOSC_AMPSEL_B setting (OPBT10 setting)*2	g_m, g_{ds}	{MOSC_SHTSTBY_A, MOSC_AMPSEL_A [2:0]} or {MOSC_SHTSTBY_B, MOSC_AMPSEL_B [2:0]} SYSVCC = 4.5 V to 5.5 V	= 0000_B	1.15, 0.089	2.47, 0.163	4.06, 0.535	mS
			= 0001_B	1.80, 0.119	3.85, 0.211	6.27, 0.592	mS
			= 0010_B	2.44, 0.145	5.19, 0.254	8.41, 0.645	mS
			= 0011_B	3.05, 0.170	6.48, 0.295	10.47, 0.697	mS
			= 0100_B	4.04, 0.209	8.57, 0.358	13.80, 0.781	mS
			= 0101_B	5.17, 0.251	10.96, 0.428	17.58, 0.876	mS
			= 0110_B	6.06, 0.284	12.87, 0.482	20.61, 0.952	mS
			= 0111_B	6.91, 0.314	14.70, 0.535	23.53, 1.023	mS
			= 1000_B	4.28, 0.204	8.98, 0.365	14.44, 0.580	mS
			= 1001_B	4.85, 0.226	10.18, 0.401	16.34, 0.633	mS
			= 1010_B	5.41, 0.246	11.36, 0.435	18.20, 0.684	mS
			= 1011_B	5.95, 0.266	12.50, 0.467	20.01, 0.734	mS
			= 1100_B	6.83, 0.297	14.35, 0.522	22.96, 0.815	mS
			= 1101_B	7.82, 0.333	16.49, 0.581	26.35, 0.903	mS
			= 1110_B	8.61, 0.363	18.20, 0.627	29.08, 0.973	mS
			= 1111_B	9.37, 0.389	19.86, 0.672	31.72, 1.040	mS
X1 clock Input frequency	f_{EX}*1	EXCLK mode		15.8		40.0	MHz
X1 clock Input cycle time	t_{EXCYC}	EXCLK mode		25.0		63.1	ns
X1 High level Input voltage	V_{IH}			0.8 × SYSVCC		SYSVCC + 0.3	V
X1 Low level Input voltage	V_{IL}			–0.3		0.2 × SYSVCC	V
X1 Input leakage current	I_{LIH}	VI = SYSVCC				0.5	µA
	I_{LIL}	VI = 0 V				–0.5	µA
X1 clock Input low level pulse width	t_{EXL}	EXCLK mode	f_{EX} = 16 MHz	26			ns
			f_{EX} = 20 MHz	20			ns
			f_{EX} = 24 MHz	16			ns
			f_{EX} = 40 MHz	10			ns

Table 3.3 Main Oscillator Characteristics (3/3)

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
X1 clock Input high level pulse width	t_{EXH}	EXCLK mode	f_{EX} = 16 MHz	26			ns
			f_{EX} = 20 MHz	20			ns
			f_{EX} = 24 MHz	16			ns
			f_{EX} = 40 MHz	10			ns
X1 clock rise time	t_{EXR}	EXCLK mode	f_{EX} = 16 MHz			4	ns
			f_{EX} = 20 MHz			4	ns
			f_{EX} = 24 MHz			3	ns
			f_{EX} = 40 MHz			2.5	ns
X1 clock fall time	t_{EXF}	EXCLK mode	f_{EX} = 16 MHz			4	ns
			f_{EX} = 20 MHz			4	ns
			f_{EX} = 24 MHz			3	ns
			f_{EX} = 40 MHz			2.5	ns
X1 clock Input total jitter (Dj + 14 * rms Random jitter)	t_{CITJ}	The clock source of SGMII used @ 20MHz				73*6	ps peak to peak
X1 Input capacitance	C_{X1}	Main OSC. EXCLK mode, MOSC_CAP_SEL = 0010				10	pF

Note 1. To reach internal usable clocks only following 4 frequencies are supported: 16MHz, 20MHz, 24MHz and 40MHz. Tolerance of external quartz crystal is assumed as +/–1%.

Note 2. The StartUp is supported without external components under following conditions:
• See RH850/U2A-EVA Group User's Manual: Hardware **Section 51.12.16, OPBT10 — Option Byte 10** for default values of drivability, damping resistance and internal capacitance.
• Specification covers a maximum external stray capacitance of up to 6pF to each pin X1 and X2.
• After StartUp drivability and capacitance will be configured by OPBT10
• A possible exceeding of the recommended maximum drive level for a crystal for all start-up phases has to be agreed with the crystal manufacturers separately.

Note 3. Ccapsel_x1 (Ccapsel_x1 including parasitic capacitance to ground at the X1 side), Ccapsel_x2 (Ccapsel_x2 including parasitic capacitance to ground at the X2 side).

Note 4. The capacitor tolerance is ±15%.

Note 5. The clock source of SGMII used. Ethernet grade crystal is mandatory. Example: CX3225GA(KYOCERA)

Note 6. 12 kHz to 20 MHz rms jitter = 3 ps.

CAUTION

Oscillation stabilization times differ according to matching with the resonator. Secure an oscillation stabilization time determined through evaluation of matching.

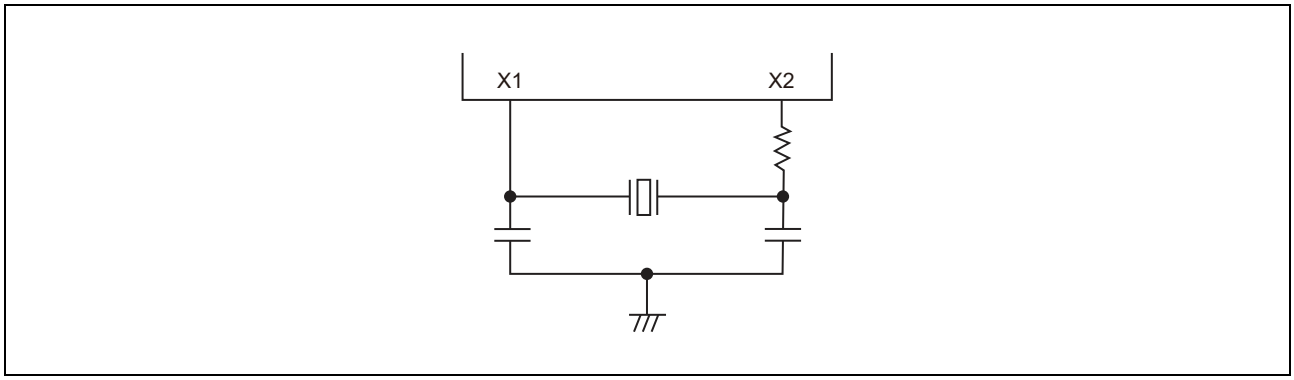


Figure 3.1 Oscillator Circuit Diagram (Crystal with External Components)

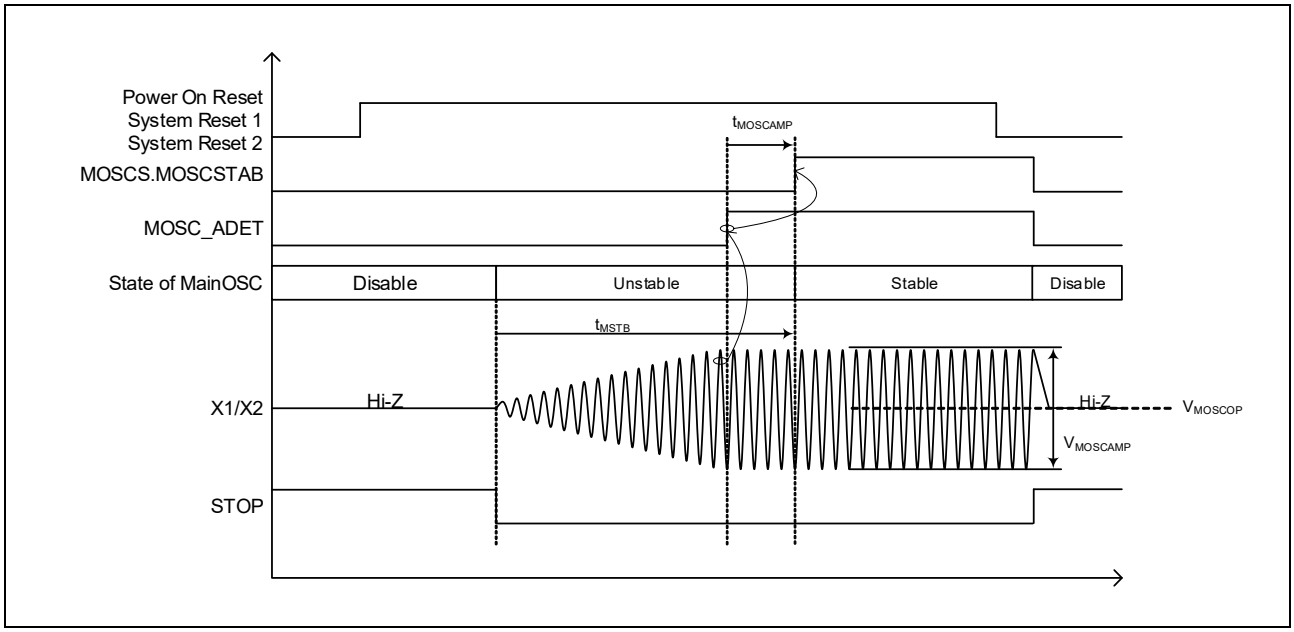


Figure 3.2 Main OSC Stabilization

3.2.1.3 Internal Oscillator Characteristics

Conditions:

- See **Section 3.2.1.1, Supply Voltage Characteristics**.

Table 3.4 Internal Oscillator Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
LS IntOSC frequency	f_{RL}		216	240	264	kHz
HS IntOSC frequency	f_{RH}		190	200	210	MHz
HV IntOSC frequency	f_{RHV}		8	16	24	MHz

3.2.1.4 PLL Characteristics

Conditions:

- See **Section 3.2.1.1, Supply Voltage Characteristics**.

Table 3.5 PLL Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
PLL output long term jitter*1	t_{PLLLTJ}	Term = 1 µs	–500		500	ps
		Term = 10 µs	–1		1	ns
		Term = 20 µs	–2		2	ns
PLL lock time*2	t_{PLLLCT}				112	µs

Note 1. This characteristic is not tested in production.
Note 2. Lock time is time until being set “1” in PLLS.PLLCLKSTAB bit after PLLE.PLLENTRG bit is written “1”.

Table 3.6 RHSIF PLL Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
PLL lock time	$t_{RHPLLLCT}$				50	µs

3.2.1.5 Regulator Characteristics

Conditions:

- See **Section 3.2.1.1, Supply Voltage Characteristics**.

Table 3.7 Regulator Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Output voltage	V_{AWOVCL}	AWOVCL pin	1.025	1.09	1.155	V
	$V_{GETH0VCL}$	GETH0VCL pin	1.025	1.09	1.155	V
Capacitance	C_{AWOVCL}	AWOVCL pin*1	0.140	0.2	0.286	µF
	$C_{GETH0VCL}$	GETH0VCL pin	0.154	0.22	0.286	µF
Equivalent series resistance for load capacitance	R_{VRAWO}	for C_{AWOVCL}			40*2	mΩ
	$R_{VRGETH0}$	for $C_{GETH0VCL}$			40*2	mΩ
Inrush current during power-on	$I_{RUSYSVCC}$	SYSVCC*3			350*2*4	mA
	$I_{RUGETH0PVCC}$	GETH0PVCC			100*2	mA

Note 1. The capacitors has to be mounted with one of the following connections:
- Distribute evenly the total capacitance for the device to all AWOVCL pins.
- Concentrate the total capacitance for the device to one AWOVCL pin.
In this case, the capacitor has to be connected to F23(BGA516), A22(BGA373), A18(BGA292), 126(QFP176), A13(BGA156) and 103(QFP144).
And other AWOVCL pins which capacitor not connected has to be left open.

Note 2. This is reference value.

Note 3. When returning from DeepSTOP.

Note 4. The time of current flow is less than 2.5 µs.

Table 3.8 Switching Voltage Regulator Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Output voltage	VDD		1.025	1.09	1.155	V
Switching frequency	f_{SVRSW}	FSWMODE[1:0] = 00_B	368	434	500	kHz
		FSWMODE[1:0] = 01_B	736	868	1000	kHz
SVR load transient response		Less than ΔI (max)	–33.5*1		33.5*1	mV
SVR efficiency		FSWMODE[1:0] = 00_B		80*1		%
		FSWMODE[1:0] = 01_B		70*1		%
Capacitance	$C_{SVRDRVCC}$	SVRDRVCC pin	9	14		µF
	$C_{SVRAVCC}$	SVRAVCC pin	0.7	1	1.3	µF
	C_{VDD0}	VDD pin. Close to LX		*2		µF
Equivalent series resistance for load capacitance	$R_{VRSVRDRVCC}$	for $C_{SVRDRVCC}$ (@0.1MHz to 5MHz)			10	mΩ
	$R_{VRSVRAVCC}$	for $C_{SVRAVCC}$ (@0.1MHz to 5MHz)			10	mΩ
	R_{VRVDD}	for C_{VDD0} (@0.1MHz to 5MHz)			10	mΩ
Inductance	LX	Close to external MOSFETs		*2		µH
DC resistance for inductance	R_{LX}	for LX			*2	mΩ
Inrush current during power-on	SVRDRVCC	include external circuit			4000*1	mA
Operating current variation*2*4*5	ΔI	I_{ISOVDD_R}, U2A16			440	mA/ 100 µs
		I_{ISOVDD_R}, U2A8			220	
		I_{ISOVDD_R}, U2A6			220	
Ramp-up time with soft start	t_{RUT}				3.6	ms

Note 1. This is reference value.
Note 2. Contact our sale office for the method of setting parameters.
Note 3. The total capacitance for the device has to be distributed around thermal ball.
Note 4. Operating current variation filtered by simple moving average of 20 µs window can be ignored.
Note 5. Operating current variation with smaller than 1 mA/µs slope is not necessary to be counted as "ΔI".

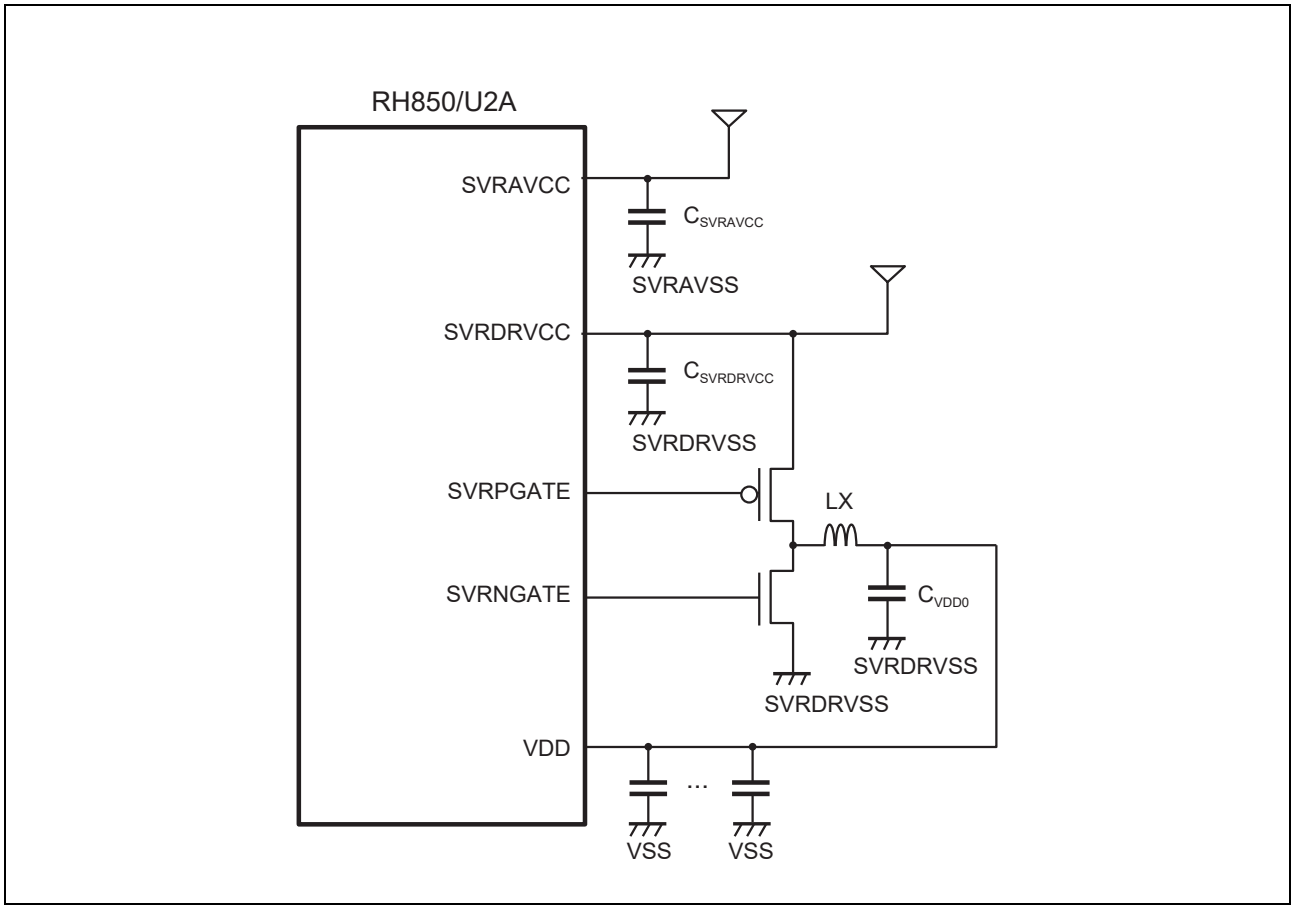


Figure 3.3 External Components of Switching Voltage Regulator

3.2.2 Input Voltage Characteristics

Conditions:

- See **Section 3.2.1.1, Supply Voltage Characteristics**.

Table 3.9 Input Voltage Characteristics

Item	Symbol	Condition*1	MIN.	TYP.	MAX.	Unit
High level input voltage	V_{IH1}	SHMT1, IOVCC = 3.0 to 5.5 V	0.65 × IOVCC		IOVCC + 0.3	V
	V_{IH2}	SHMT2, IOVCC = 3.0 to 5.5 V	0.75 × IOVCC		IOVCC + 0.3	V
	V_{IH3}	SHMT4, IOVCC = 3.0 to 5.5 V	0.80 × IOVCC		IOVCC + 0.3	V
	V_{IH4}	TTL, IOVCC = 3.0 to 5.5 V	2.2		IOVCC + 0.3	V
Low level input voltage	V_{IL1}	SHMT1, IOVCC = 3.0 to 5.5 V	–0.3		0.35 × IOVCC	V
	V_{IL2}	SHMT2, IOVCC = 3.0 to 5.5 V	–0.3		0.25 × IOVCC	V
	V_{IL3}	SHMT4, IOVCC = 3.0 to 5.5 V	–0.3		0.50 × IOVCC	V
	V_{IL4}	TTL, IOVCC = 3.0 to 5.5 V	–0.3		0.8	V
Input hysteresis for Schmitt*3	V_{HS1}	SHMT1, IOVCC = 4.5 to 5.5 V	0.4			V
		SHMT1, IOVCC = 3.0 to 4.5 V	0.3			V
	V_{HS2}	SHMT2, IOVCC = 3.0 to 5.5 V	0.2 × IOVCC			V
	V_{HS3}	SHMT4, IOVCC = 3.0 to 5.5 V	0.1			V

Note 1. "IOVCC" means power supply voltage for I/O ports. See the appendix "*E02_01_List_of_Pin_Assignment.xlsx*" for the power supply of each pin.

Note 2. For X1 pin, see **Section 3.2.1.2, Main Oscillator Characteristics**.

Note 3. The configured drive strength of the output terminals in a power group might affect the hysteresis characteristics of the input terminals in the same power group. See Appendix file "*E02_01_List_of_Pin_Assignment.xlsx*" for the assignment of the power group.

3.2.3 Input Leakage Current

Conditions:

- See **Section 3.2.1.1, Supply Voltage Characteristics**.

Table 3.10 Input Leakage Current

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Input leakage current	I_{LIH1}	Vin = 0 to EnVCC • Pn_m (Except P2_0, P2_5, P2_10 to P2_15, P4_5 to P4_10, P22_0 and P22_4)	Tj ≤ 105°C			0.5	µA
			105°C < Tj ≤ 150°C			1.0	µA
			150°C < Tj			2.0	µA
	I_{LIH2}	Vin = 0 to EnVCC • P2_0, P2_5, P2_10 to P2_15, P4_5 to P4_10, P22_0 and P22_4	Tj ≤ 105°C			0.5	µA
			105°C < Tj			2.0	µA
	I_{LIH3}	Vin = 0 to AnVCC • APn_m	Tj ≤ 150°C			0.5	µA
			150°C < Tj			1.0	µA
	I_{LIL1}	Vin = 0 to EnVCC • Pn_m (Except P2_0, P2_5, P2_10 to P2_15, P4_5 to P4_10, P22_0 and P22_4)	Tj ≤ 105°C			–0.5	µA
			105°C < Tj ≤ 150°C			–1.0	µA
			150°C < Tj			–2.0	µA
	I_{LIL2}	Vin = 0 to EnVCC • P2_0, P2_5, P2_10 to P2_15, P4_5 to P4_10, P22_0 and P22_4	Tj ≤ 105°C			–0.5	µA
			105°C < Tj			–2.0	µA
	I_{LIL3}	Vin = 0 to AnVCC • APn_m	Tj ≤ 150°C			–0.5	µA
			150°C < Tj			–1.0	µA

3.2.4 Pull-up/Pull-down Characteristics

Conditions:

- See **Section 3.2.1.1, Supply Voltage Characteristics**.

Table 3.11 Pull-up/Pull-down Characteristics

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Input pull-up current source	I_{PU1}		IOVCC*1 = 3.0 to 5.5V, Vin = 0V	30		350	µA
Input pull-down current source	I_{PD1}	Other than the below	IOVCC*1 = 3.0 to 5.5V, Vin = IOVCC*1	30		350	µA
	I_{PD2}	$\overline{\text{RESET}}$, $\overline{\text{AURORES1}}$, $\overline{\text{AURORES2}}$, $\overline{\text{AURORESPD}}$, $\overline{\text{ERAMRES2}}$, $\overline{\text{ERAMRESPD}}$	IOVCC*1 = 3.0 to 5.5V, Vin = IOVCC*1			110	µA

Note 1. "IOVCC" means power supply voltage for I/O ports. See the appendix "*E02_01_List_of_Pin_Assignment.xlsx*" for the power supply of each pin.

3.2.5 Output Voltage Characteristics

Conditions:

- See **Section 3.2.1.1, Supply Voltage Characteristics**.

Table 3.12 Output Voltage Characteristics[*1]

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Output resistance	R_{O11}	Drive strength = 1	IOVCC – V_{OH} = 0.4 V, V_{OL} = 0.4 V	6		40	Ω
	R_{O12}	Drive strength = 2	IOVCC – V_{OH} = 0.4 V, V_{OL} = 0.4 V	11		72	Ω
	R_{O13}	Drive strength = 3	IOVCC – V_{OH} = 0.4 V, V_{OL} = 0.4 V	18		100	Ω
	R_{O14}	Drive strength = 4	IOVCC – V_{OH} = 0.4 V, V_{OL} = 0.4 V	32		200	Ω
	R_{O15}	Drive strength = 5	IOVCC – V_{OH} = 0.4 V, V_{OL} = 0.4 V	61		400	Ω
High level output voltage	V_{OH1}	Drive strength = 1 IOVCC = 3.0 to 5.5 V	I_{OH} = –4 mA / pin (4 output pins)[*2]	IOVCC–0.8			V
			I_{OH}= –2 mA / pin (4 output pins)[*2]	IOVCC–0.5			V
	V_{OH2}	Drive strength = 2 IOVCC = 3.0 to 3.6 V	I_{OH} = –4 mA / pin (8 output pins)[*2]	IOVCC–0.8			V
			I_{OH}= –2 mA / pin (8 output pins)[*2]	IOVCC–0.5			V
		Drive strength = 2 IOVCC = 3.6 to 5.5 V	I_{OH} = –4 mA / pin (2 output pins)[*2]	IOVCC–0.8			V
			I_{OH}= –2 mA / pin (2 output pins)[*2]	IOVCC–0.5			V
	V_{OH3}	Drive strength = 3 IOVCC = 3.0 to 5.5 V	I_{OH} = –4 mA / pin (8 output pins)[*2]	IOVCC–0.8			V
			I_{OH} = –2 mA / pin (8 output pins)[*2]	IOVCC–0.5			V
	V_{OH4}	Drive strength = 4 IOVCC = 3.0 to 5.5 V	I_{OH} = –2 mA / pin (16 output pins)[*2]	IOVCC–0.7			V
			I_{OH} = –1 mA / pin (16 output pins)[*2]	IOVCC–0.5			V
	V_{OH5}	Drive strength = 5 IOVCC = 3.0 to 5.5 V	I_{OH} = –1 mA / pin (16 output pins)[*2]	IOVCC–0.7			V
			I_{OH} = –500 µA / pin (16 output pins)[*2]	IOVCC–0.5			V
Low level output voltage	V_{OL1}	Drive strength = 1 IOVCC = 3.0 to 5.5 V	I_{OL} = 4 mA / pin (4 output pins)[*2]			0.8	V
			I_{OL} = 2 mA / pin (4 output pins)[*2]			0.5	V
	V_{OL2}	Drive strength = 2 IOVCC = 3.0 to 3.6 V	I_{OL} = 4 mA / pin (8 output pins)[*2]			0.8	V
			I_{OL} = 2 mA / pin (8 output pins)[*2]			0.5	V
		Drive strength = 2 IOVCC = 3.0 to 5.5 V	I_{OL} = 4 mA / pin (2 output pins)[*2]			0.8	V
			I_{OL} = 2 mA / pin (2 output pins)[*2]			0.5	V
	V_{OL3}	Drive strength = 3 IOVCC = 3.0 to 5.5 V	I_{OL} = 4 mA / pin (8 output pins)[*2]			0.7	V
			I_{OL} = 2 mA / pin (8 output pins)[*2]			0.5	V
	V_{OL4}	Drive strength = 4 IOVCC = 3.0 to 5.5 V	I_{OL} = 2 mA / pin (16 output pins)[*2]			0.7	V
			I_{OL} = 1 mA / pin (16 output pins)[*2]			0.5	V
	V_{OL5}	Drive strength = 5 IOVCC = 3.0 to 5.5 V	I_{OL} = 1 mA / pin (16 output pins)[*2]			0.7	V
			I_{OL} = 500 µA / pin (16 output pins)[*2]			0.5	V

Note 1. "IOVCC" means power supply voltage for I/O ports. See the appendix "*E02_01_List_of_Pin_Assignment.xlsx*" for the power supply of each pin.

Note 2. The number of pin indicates simultaneous ON in one power. The influence of the noise emission should be considered when switching the output level.

3.2.6 Output Current

Conditions:

- See **Section 3.2.1.1, Supply Voltage Characteristics**.

Table 3.13 Output Current Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High level output current	$\|I_{OH}\|$	per pin			8	mA
	$\Sigma\|I_{OH}\|$ EnVCC	Each EnVCC			60	mA
	$\Sigma\|I_{OH}\|$ AnVCC	Each AnVCC			16	mA
Low level output current	I_{OL}	per pin			8	mA
	ΣI_{OL} EnVCC	Each EnVCC			60	mA
	ΣI_{OL} AnVCC	Each AnVCC			16	mA

3.2.7 Injection Current Characteristics

Conditions:

- See **Section 3.2.1.1, Supply Voltage Characteristics**.

Table 3.14 Injection Current Operating Conditions

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
DC injection current (per pin)	I_{INJ_DIN}	Digital pin *1	–2		3	mA
	I_{INJ_AIN}	Analogue pin	–3		3	mA
DC injection current (each power supply)	I_{INJ_E0VCC}	E0VCC			50	mA
	I_{INJ_E1VCC}	E1VCC			50	mA
	I_{INJ_E2VCC}	E2VCC			30	mA
	I_{INJ_A0VCC}	A0VCC			20	mA
	I_{INJ_A1VCC}	A1VCC			20	mA
	I_{INJ_A2VCC}	A2VCC			20	mA
DC injection current (total)	I_{INJ_TOTAL}				80	mA

Note 1. Injection current to the logic pin multiplied with LVDS function is prohibited when LVDS function is used. When LVDS function is not used, Injection current to the logic pin multiplied with LVDS function causes at maximum additional 1 µA leakage current at the P/N combinational pin. For example, injection current to HSIF0_TXDP causes at maximum additional 1 µA leakage current at HSIF0_TXDN.

NOTE

- Injection current to P3_8 pin is prohibited when SGMII function is used.
- Input voltage must be kept within –0.8V ≤ Vin ≤ 6.0V, if injection current is kept within rated value.
- Power supply voltage must be kept within operating conditions.
- Injection current effects power dissipation in the package for thermal characteristics.

3.2.8 LVDS Characteristics

3.2.8.1 LVDS Driver Characteristics

Conditions:

- See **Section 3.2.1.1, Supply Voltage Characteristics**.

Table 3.15 LVDS Driver Characteristics (based on IEEE 1596.3-1996)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Output low-level voltage	V_{LVDSOL}		1000			mV
Output high-level voltage	V_{LVDSOH}				1400	mV
Output differential voltage	V_{LVDSOD}		150		250	mV
Offset voltage	V_{LVDSOS}		1.125	1.2	1.275	V
Output impedance	R_{LVDSOI}		40		300	Ω

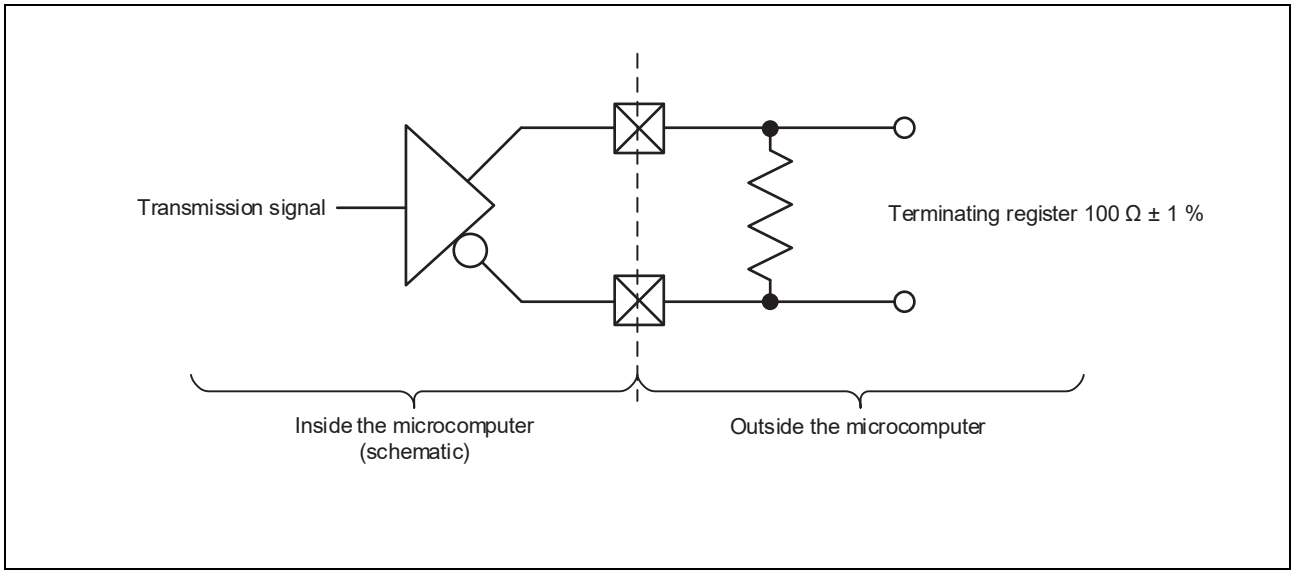


Figure 3.4 LVDS Driver Measurement Conditions

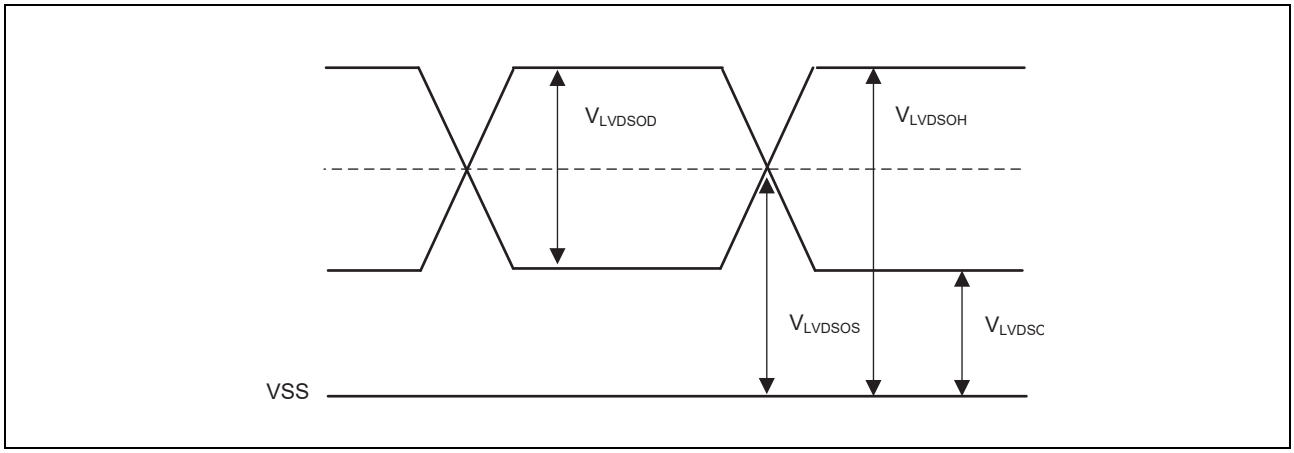


Figure 3.5 Meaning of LVDS Driver Symbols

3.2.8.2 LVDS Receiver Characteristics

Conditions:

- See **Section 3.2.1.1, Supply Voltage Characteristics**.

Table 3.16 LVDS Receiver Characteristics (based on IEEE 1596.3-1996)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Differential Input threshold voltage	$V_{LVDSIDTH}$		–100		100	mV
Input voltage range	V_{LVDI}		0.825		1.575	V

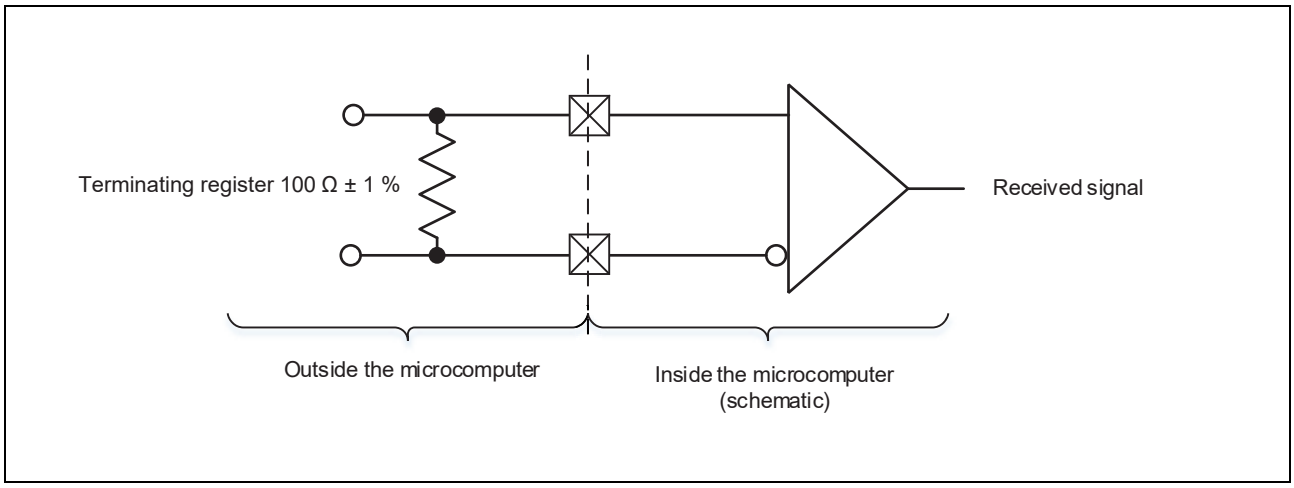


Figure 3.6 LVDS Receiver Measurement Conditions

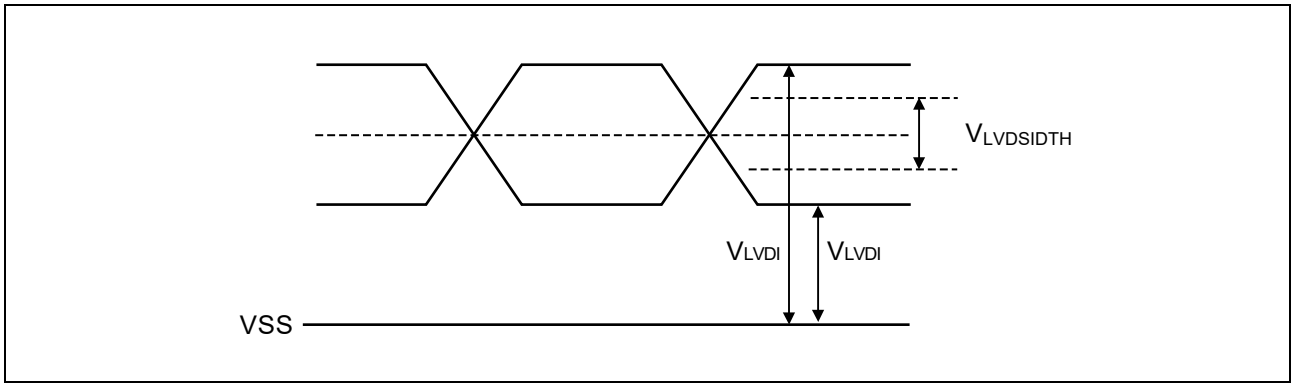


Figure 3.7 Meaning of LVDS Receiver Symbols

3.2.9 SGMII Characteristics

Conditions:

- See **Section 3.2.1.1, Supply Voltage Characteristics**.

Table 3.17 SGMII REFCK Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High level input voltage	V_{IH}		2.0		GETH0RVCC + 0.3	V
Low level input voltage	V_{IL}		–0.3		0.8	V

Table 3.18 SGMII Tx Buffer Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Output voltage high	V_{OH}				1525	mV
Output voltage low	V_{OL}		875			mV
Output Differential Voltage	$\|V_{OD}\|$		150		400	mV
Output Offset Voltage	V_{OS}		1075		1325	mV
Change in V_{OD} between “0” and “1”	$\Delta\|V_{OD}\|$				25	mV
Change in V_{OS} between “0” and “1”	ΔV_{OS}				25	mV
Output current on Short to GND	I_{sa}, I_{sb}				40	mA
Output current when a, b are shorted	I_{sab}				12	mA

Note 1. For details of the symbols, refer to the IEEE1596.3-1996 standard.
Note 2. All parameters measured at Rload = 100 Ω ±1 % load

Table 3.19 SGMII Rx Buffer Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input Voltage range a or b	V_I		675		1725	mV
Input differential threshold	V_{idth}		–50		50	mV
Receiver differential input impedance	R_{in}		80		120	Ω

Note 1. For details of the symbols, refer to the IEEE1596.3-1996 standard.

3.2.10 Aurora Interface Clock Characteristics

Conditions:

- See **Section 3.2.1.1, Supply Voltage Characteristics**.

Table 3.20 Aurora Interface Clock Characteristics (CICREFP, CICREFN)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Differential input voltage	$V_{DIFFCIC}$ *1		200		1600	mV
External AC coupling capacitor	C_{ACC}		75	100	200	nF
Differential input resistance	$Z_{DIFFCIC}$		70	100	130	Ω

Note 1. Peak to peak differential input voltage.

Table 3.21 Aurora Interface Characteristics (TODP0-3/TODN0-3)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Differential output voltage	$V_{DIFFTOD}$ *1		800		1600	mV
Differential output resistance	$Z_{DIFFTOD}$		70		130	Ω

Note 1. Peak to peak differential input voltage.

3.2.11 IO Capacitances

Conditions:

- See **Section 3.2.1.1, Supply Voltage Characteristics**.

Table 3.22 IO Capacitances *1, *2

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f = 1 MHz 0 V for non measurement pins			10	pF
Input/output capacitance	C_{IO}				10	pF
Output capacitance	C_O				10	pF

Note 1. This capacity is the capacity value per BGA_Ball (QFP_Pin) 1 terminal.

Note 2. For analog input pins (ADCJnIm and ADCJnImS), refer to **Section 3.4, A/D Converter Characteristics**.

3.2.12 Supply Current Characteristics

3.2.12.1 General Definition

Power consumption except for the current of I/O buffer (I_{EnVCC}) is specified below.

The parameter I_{EnVCC} depends on customer's application and thus need to be defined by customer in order to determine the total power dissipation of a device.

3.2.12.2 Power Supply Currents

Conditions:

- See **Section 3.2.1.1, Supply Voltage Characteristics**.

Table 3.23 Current consumption for RH850/U2A-EVA*2, *3

Item	Symbol	Power supply	CPU frequency	MIN.	TYP.*1	MAX.	Unit
RUN mode current	I_{SYSVCC_R}	SYSVCC	400 MHz		6	34	mA
			320 MHz		6	34	mA
			240 MHz		6	34	mA
	I_{VCC_R}	VCC*5	400 MHz		22	45	mA
			320 MHz		22	45	mA
			240 MHz		22	45	mA
	I_{ISOVDD_R}	ISOVDD	400 MHz		480	1870	mA
			320 MHz		405	1694	mA
			240 MHz		330	1518	mA
STOP mode current*6	I_{SYSVCC_S}	SYSVCC			3	20	mA
	I_{VCC_S}	VCC			0.005	1	mA
	I_{ISOVDD_S}	ISOVDD			385	1300	mA
DeepSTOP mode current*6	I_{SYSVCC_DS}	SYSVCC			0.52	12	mA
	I_{VCC_DS}	VCC			2	400	µA
	I_{ISOVDD_DS}	ISOVDD			14*4	900*4	mA
Cyclic RUN mode current*6	I_{SYSVCC_CR}	SYSVCC	100 MHz		4	32	mA
	I_{VCC_CR}	VCC	100 MHz		0.008	1.2	mA
	I_{ISOVDD_CR}	ISOVDD	100 MHz		405	1350	mA
Cyclic STOP mode current*6	I_{SYSVCC_CS}	SYSVCC			3	20	mA
	I_{VCC_CS}	VCC			0.005	1	mA
	I_{ISOVDD_CS}	ISOVDD			385	1300	mA

Note 1. The condition of “TYP.” shows the specification with the following conditions. Also, the value is just for reference only.
- Tj = 25°C
- SYSVCC = VCC = EnVCC = LVDVCC = AnVCC = AnVREFH = SVRDRVCC = SVRAVCC = 5.0 V
- GETH0PVCC = GETH0BVCC = GETH0RVCC = 3.3 V
- ISOVDD = 1.09 V

Note 2. The above value does not include the current of SVR converter.

Note 3. The above value does not include the current of I/O buffer.

Note 4. Indicated leak current will be applied if the power continues supplying to ISOVDD during DeepSTOP mode.

Note 5. Additional current (max.60 mA for Code Flash per unit, max.35 mA for Data Flash per unit) will be applied when data writing/erasing to Code or Data Flash is processing.

Note 6. MainOSC and all peripherals are stopped.

Table 3.24 Current consumption for RH850/U2A-EVA (specific power supply)

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
EMUVCC	I_{EMUVCC}					20	mA
DVCC	I_{DVCC}					20	mA
ERAMVCC	$I_{ERAMVCC}$					5	mA
EMUVDD	I_{EMUVDD}					20	mA
DVDD	I_{DVDD}					350	mA
ERAMVDD	$I_{ERAMVDD}$					250	mA

Table 3.25 Current consumption for RH850/U2A16[*2, *3]

Item	Symbol	Power supply	CPU frequency	MIN.	TYP.[*1]	MAX.	Unit
RUN mode current	I_{SYSVCC_R}	SYSVCC	400 MHz		6	34	mA
			320 MHz		6	34	mA
			240 MHz		6	34	mA
	I_{VCC_R}	VCC[*5]	400 MHz		11	35	mA
			320 MHz		11	35	mA
			240 MHz		11	35	mA
	I_{ISOVDD_R}	ISOVDD	400 MHz		420	1650	mA
			320 MHz		355	1483	mA
			240 MHz		290	1316	mA
STOP mode current[*6]	I_{SYSVCC_S}	SYSVCC			3	20	mA
	I_{VCC_S}	VCC			0.005	1	mA
	I_{ISOVDD_S}	ISOVDD			335	1130	mA
DeepSTOP mode current[*6]	I_{SYSVCC_DS}	SYSVCC			0.52	12	mA
	I_{VCC_DS}	VCC			2	400	µA
	I_{ISOVDD_DS}	ISOVDD			12[*4]	730[*4]	mA
Cyclic RUN mode current[*6]	I_{SYSVCC_CR}	SYSVCC	100 MHz		4	32	mA
	I_{VCC_CR}	VCC	100 MHz		0.008	1.2	mA
	I_{ISOVDD_CR}	ISOVDD	100 MHz		350	1180	mA
Cyclic STOP mode current[*6]	I_{SYSVCC_CS}	SYSVCC			3	20	mA
	I_{VCC_CS}	VCC			0.005	1	mA
	I_{ISOVDD_CS}	ISOVDD			335	1130	mA

Note 1. The condition of “TYP.” shows the specification with the following conditions. Also, the value is just for reference only.
- Tj = 25°C
- SYSVCC = VCC = EnVCC = LVDVCC = AnVCC = AnVREFH = SVRDRVCC = SVRAVCC = 5.0 V
- GETH0PVCC = GETH0BVCC = GETH0RVCC = 3.3 V
- ISOVDD = 1.09 V

Note 2. The above value does not include the current of SVR converter.

Note 3. The above value does not include the current of I/O buffer.

Note 4. Indicated leak current will be applied if the power continues supplying to ISOVDD during DeepSTOP mode.

Note 5. Additional current (max.60 mA for Code Flash per unit, max.35 mA for Data Flash per unit) will be applied when data writing/erasing to Code or Data Flash is processing.

Note 6. MainOSC is stopped.

Table 3.26 Current consumption for RH850/U2A8[*2, *3]

Item	Symbol	Power supply	CPU frequency	MIN.	TYP.[*1]	MAX.	Unit
RUN mode current	I_{SYSVCC_R}	SYSVCC	400 MHz		6	30	mA
			320 MHz		6	30	mA
			240 MHz		6	30	mA
	I_{VCC_R}	VCC[*5]	400 MHz		9	28	mA
			320 MHz		9	28	mA
			240 MHz		9	28	mA
	I_{ISOVDD_R}	ISOVDD	400 MHz		245	870	mA
			320 MHz		210	780	mA
			240 MHz		175	690	mA
STOP mode current[*6]	I_{SYSVCC_S}	SYSVCC			3	16	mA
	I_{VCC_S}	VCC			0.005	0.6	mA
	I_{ISOVDD_S}	ISOVDD			170	580	mA
DeepSTOP mode current[*6]	I_{SYSVCC_DS}	SYSVCC			0.46	8	mA
	I_{VCC_DS}	VCC			2	320	µA
	I_{ISOVDD_DS}	ISOVDD			5[*4]	385[*4]	mA
Cyclic RUN mode current[*6]	I_{SYSVCC_CR}	SYSVCC	100 MHz		4	28	mA
	I_{VCC_CR}	VCC	100 MHz		0.008	0.8	mA
	I_{ISOVDD_CR}	ISOVDD	100 MHz		180	620	mA
Cyclic STOP mode current[*6]	I_{SYSVCC_CS}	SYSVCC			3	16	mA
	I_{VCC_CS}	VCC			0.005	0.6	mA
	I_{ISOVDD_CS}	ISOVDD			170	580	mA

Note 1. The condition of “TYP.” shows the specification with the following conditions. Also, the value is just for reference only.
- Tj = 25°C
- SYSVCC = VCC = EnVCC = LVDVCC = AnVCC = AnVREFH = SVRDRVCC = SVRAVCC = 5.0 V
- GETH0PVCC = GETH0BVCC = GETH0RVCC = 3.3 V
- ISOVDD = 1.09 V

Note 2. The above value does not include the current of SVR converter.

Note 3. The above value does not include the current of I/O buffer.

Note 4. Indicated leak current will be applied if the power continues supplying to ISOVDD during DeepSTOP mode.

Note 5. Additional current (max.60 mA for Code Flash per unit, max.35 mA for Data Flash per unit) will be applied when data writing/erasing to Code or Data Flash is processing.

Note 6. MainOSC is stopped.

Table 3.27 Current consumption for RH850/U2A6[*2, *3]

Item	Symbol	Power supply	CPU frequency	MIN.	TYP.[*1]	MAX.	Unit
RUN mode current	I_{SYSVCC_R}	SYSVCC	400 MHz		6	30	mA
			320 MHz		6	30	mA
			240 MHz		6	30	mA
	I_{VCC_R}	VCC[*5]	400 MHz		9	28	mA
			320 MHz		9	28	mA
			240 MHz		9	28	mA
	I_{ISOVDD_R}	ISOVDD	400 MHz		240	840	mA
			320 MHz		207	755	mA
			240 MHz		173	670	mA
STOP mode current[*6]	I_{SYSVCC_S}	SYSVCC			3	16	mA
	I_{VCC_S}	VCC			0.005	0.6	mA
	I_{ISOVDD_S}	ISOVDD			168	570	mA
DeepSTOP mode current[*6]	I_{SYSVCC_DS}	SYSVCC			0.46	8	mA
	I_{VCC_DS}	VCC			2	320	µA
	I_{ISOVDD_DS}	ISOVDD			4[*4]	375[*4]	mA
Cyclic RUN mode current[*6]	I_{SYSVCC_CR}	SYSVCC	100 MHz		4	28	mA
	I_{VCC_CR}	VCC	100 MHz		0.008	0.8	mA
	I_{ISOVDD_CR}	ISOVDD	100 MHz		178	610	mA
Cyclic STOP mode current[*6]	I_{SYSVCC_CS}	SYSVCC			3	16	mA
	I_{VCC_CS}	VCC			0.005	0.6	mA
	I_{ISOVDD_CS}	ISOVDD			168	570	mA

Note 1. The condition of “TYP.” shows the specification with the following conditions. Also, the value is just for reference only.
- Tj = 25°C
- SYSVCC = VCC = EnVCC = AnVCC = AnVREFH = SVRDRVCC = SVRAVCC = 5.0 V
- ISOVDD = 1.09 V

Note 2. The above value does not include the current of SVR converter.

Note 3. The above value does not include the current of I/O buffer.

Note 4. Indicated leak current will be applied if the power continues supplying to ISOVDD during DeepSTOP mode.

Note 5. Additional current (max.60 mA for Code Flash per unit, max.35 mA for Data Flash per unit) will be applied when data writing/erasing to Code or Data Flash is processing.

Note 6. MainOSC is stopped.

3.2.12.3 Power Supply Currents for specific features

Conditions:

- See **Section 3.2.1.1, Supply Voltage Characteristics**.

Table 3.28 Current consumption for specific features*1

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
SVR converter	I_{SVR}	Current of SYSVCC			4	mA
	I_{SVRA}	Current of SVRAVCC			12	mA
LVDS for RHSIF/MSPI	I_{LVDS}	Current of LVDVCC			16	mA
Gigabit Ethernet	I_{GBETH}	Current of GETH0BVCC, GETH0RVCC and GETH0PVCC			90	mA
ADCJ0	I_{ADC0}*2	Current of A0VCC 4ch T&H function is used			5.7	mA
	$I_{ADC0REF}$*2	Current of A0VREFH			0.2	mA
ADCJ1	I_{ADC1}*2	Current of A1VCC 4ch T&H function is used			5.7	mA
	$I_{ADC1REF}$*2	Current of A1VREFH			0.2	mA
ADCJ2	I_{ADC2}*2	Current of A2VCC			2.9	mA
	$I_{ADC2REF}$*2	Current of A2VREFH			0.2	mA

Note 1. This table shows additional current when the specific function indicated above is used.

Note 2. For QFP package and BGA156 package, the current of AnVREFH (IADCnREF) is total of AnVREFH current (IADCnREF) and AnVCC current (IADCn).

3.2.13 Voltage Detector (POC, VLVI) Characteristics

Conditions:

- See **Section 3.2.1.1, Supply Voltage Characteristics**.

Table 3.29 Voltage Detector (POC, VLVI) Characteristics*1

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Detection voltage (SYSVCC)	V_{POC}		2.5	2.63	2.75	V
	V_{VLVI}		1.9	2.0	2.1	V
Response time	t_{DPOC1}	Rise			1.2	ms
	t_{DPOC2}	Fall			10	µs
SYSVCC minimum pulse width	t_{WPOC}		0.2			ms
SYSVCC voltage ramp	t_{SYSVS}		0.002		550	ms/V

Note 1. POC monitors SYSVCC supply voltage.

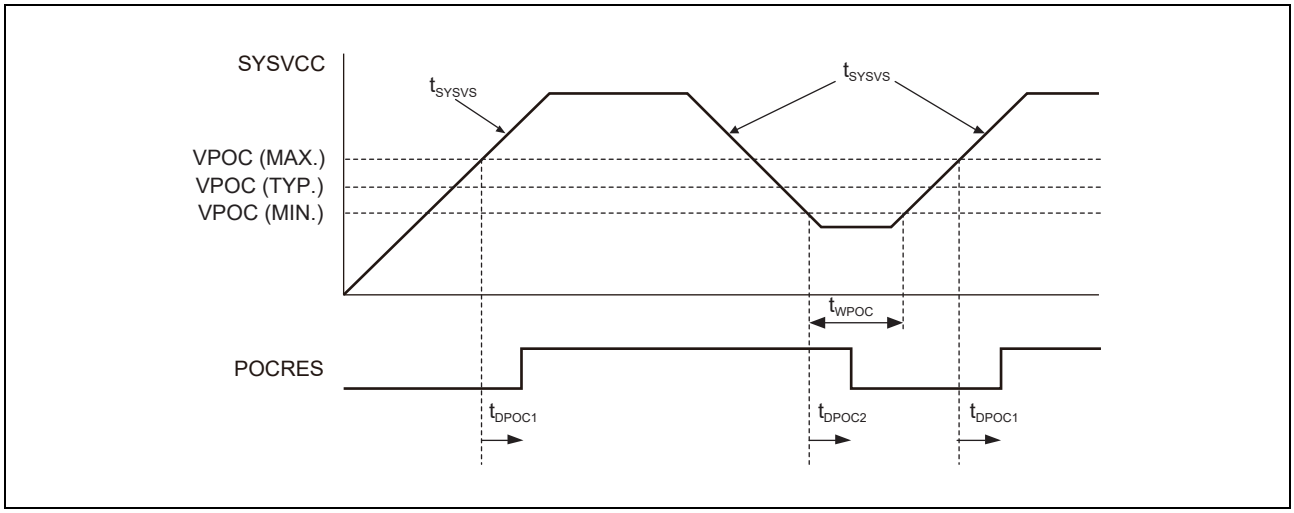


Figure 3.8 POC Characteristics

3.2.14 VMON Characteristics

Conditions:

- See **Section 3.2.1.1, Supply Voltage Characteristics**.

Table 3.30 VMON Characteristics*1

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
VDD primary high detection level	V_{VDDMAH}	AWOVDD	1.155	1.17	1.205	V
	V_{VDDMIH}	ISOVDD	1.155	1.17	1.205	V
VDD primary low detection level	V_{VDDMAL}	AWOVDD	0.975	1.01	1.025	V
	V_{VDDMIL}	ISOVDD Enable assist by Delay Monitor (DMON)	0.985	1.01	1.025	V
VCC primary high detection level	V_{VCCMH}		5.5	5.64	5.8	V
VCC primary low detection level	V_{VCCML}		2.8	2.9	3	V
E0VCC primary high detection level	V_{EVCCMH}		5.5	5.64	5.8	V
E0VCC primary low detection level	V_{EVCCML}		2.8	2.9	3	V
$\overline{\text{VMONOUT}}$ delay time	t_{DVMON}				10+Filter time*1	µs
VMON minimum pulse width	t_{WVMON}		0.2			ms
Voltage ramp	t_{VS}		0.002		550	ms/V

Note 1. See RH850/U2A-EVA Group User's Manual: Hardware **Section 11.3.6, Registers** for details specification of filter time.

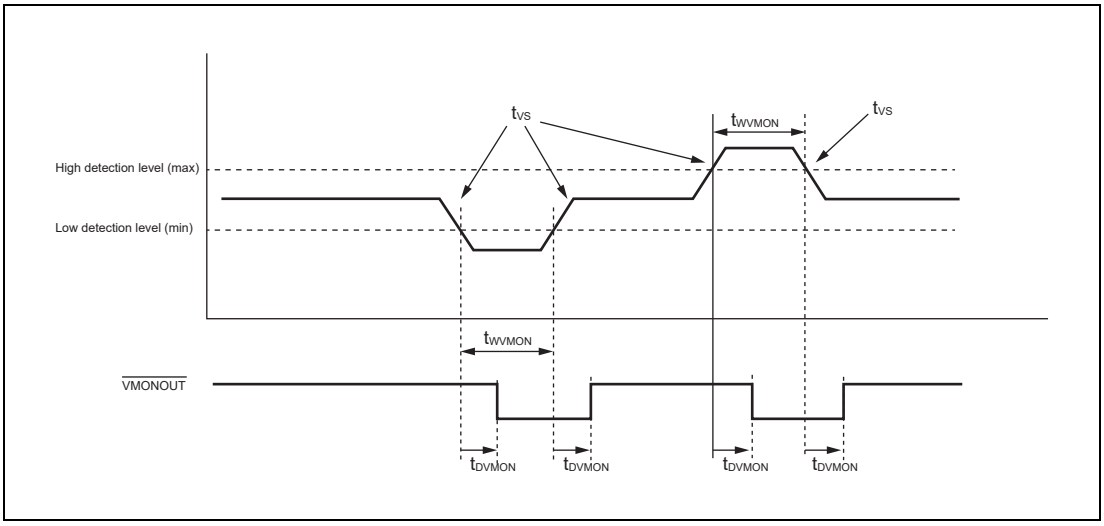


Figure 3.9 VMON Characteristics

3.3 AC Characteristics

3.3.1 AC Characteristic Measurement Condition

3.3.1.1 General Conditions

Below conditions are valid for all subsequent timing specifications if not noted otherwise:

- See **Section 3.2.1.1, Supply Voltage Characteristics**.
- Drive strength = 3
- CL = 30 pF
- All bits of PINVn/JPINV0 are set as 0.
- All bits of PODCn/JPODC0 are set as 0 except for specification on RIIC timing.

NOTE

Even though AC characteristics correspond to the nominal frequency, a main oscillator tolerance of up to 1000 ppm is considered with regard to timing characteristics for communication modules.

3.3.1.2 Input Measurement Points

If not stated otherwise, the below given AC timing specification is based on the measurements points as follows:

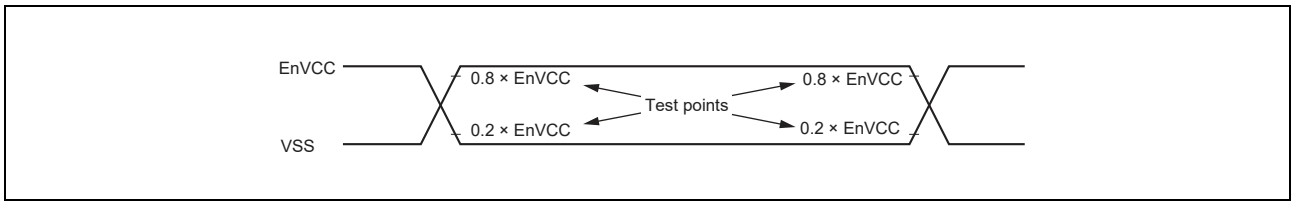


Figure 3.10 AC Input Measurement Points

3.3.1.3 Output Measurement Points

If not stated otherwise, the below given AC timing specification is based on the measurements points as follows:

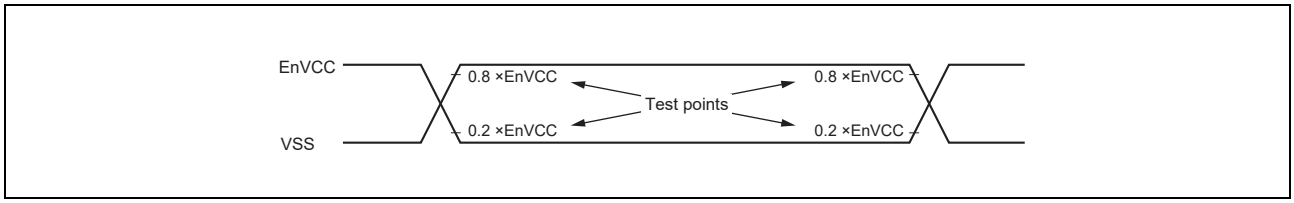


Figure 3.11 AC Output Measurement Points

3.3.1.4 Load conditions

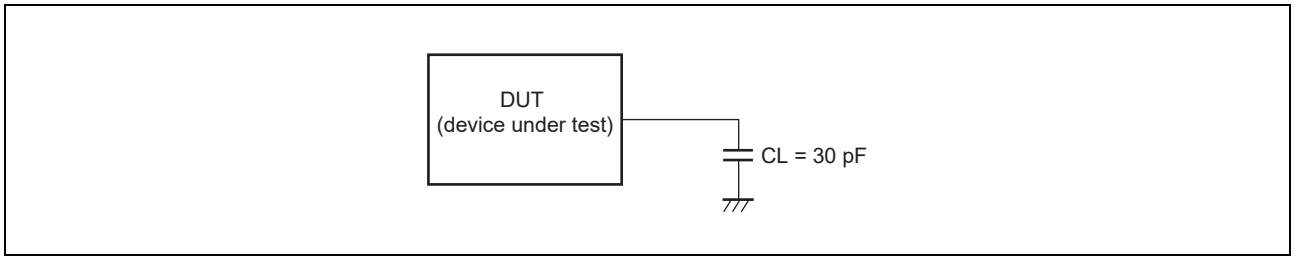


Figure 3.12 AC Load Conditions

3.3.2 Power On/Off Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.31 Power On/Off Timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Reset hold time at power-on	t_{RESH1}*6	Power-up*1 SVR is used	1.3 + t_{RUT}			ms
		Power-up*1 SVR is not used	1.3			ms
Power hold time at reset assertion*5	t_{PWH}	Power-down*2 (ETNB1 (SGMII) used)	64			µs
		Power-down*2 (ETNB1 (SGMII) not used)	10.5			µs
Operation mode low level hold time at power-on	t_{MDL1}*6	SVR is used	0.1 + t_{RUT}			ms
		SVR is not used	0.1			ms
Operating mode setup time at power-on	t_{MDS1}		1			ms
Operating mode setup time at reset assert	t_{MDS2}		1			ms
Operating mode hold time at reset negate	t_{MDH1}		1			ms
Operating mode hold time at power-off	t_{MDH2}		0			µs
$\overline{\text{TRST}}$ setup time at reset	t_{TRMDS}		2			µs
$\overline{\text{TRST}}$ hold time at reset negate*4	t_{TRMDH}		30			ms
$\overline{\text{TRST}}$ hold time at power-on	t_{TRSTH1}*6	SVR is used	1.29 + t_{RUT}			ms
		SVR is not used	1.29			ms
$\overline{\text{TRST}}$ hold time at power-off	t_{TRSTH3}	Time since SYSVCC and VDD were power-off.			10	µs
Oscillator stabilization time	t_{OSC}				5.5	ms
PLL lock in time	t_{PLLL}	*3			1	ms
EMUVDD hold time at power-on	$t_{EMUVDDH1}$		0			ms
EMUVDD setup time at power-off	$t_{EMUVDDS1}$		0			ms

Note 1. t_{RESH1} is the reset time required for the supply of internal clock signals to become stable after power supplies are turned on. There are no restrictions on the rising order of each power supply.

Note 2. t_{PWH} is the time from assertion of the reset signal until any of the power voltages have dropped below the lower-limit voltages.
There are no restrictions on the falling order of each power supply.

Note 3. t_{PLLL} is the time required for PLL to lock in after MOSC oscillation has become stable.

Note 4. Access by the Nexus, LPD and BSCAN during t_{TRMDH} duration is prohibited (both of High and low condition of $\overline{\text{TRST}}$).

Note 5. The device can withstand up to 1000 uncontrolled power down cycles without impact on lifetime.
Uncontrolled means not according to power down timing requirements.

Note 6. Objection of power supplies for t_{RESH1}, t_{TRSTH1} and t_{MDL1} is changed by power configuration.
When SVR is used:All power supplies except for ISOVDD
When SVR is not used: All power supplies

CAUTION

The states of I/O pins are not reset during the noise cancellation interval of the reset signal following its assertion while power is being turned off. During that time, do not allow any input of mid-range potential to the pin or contention of output data.

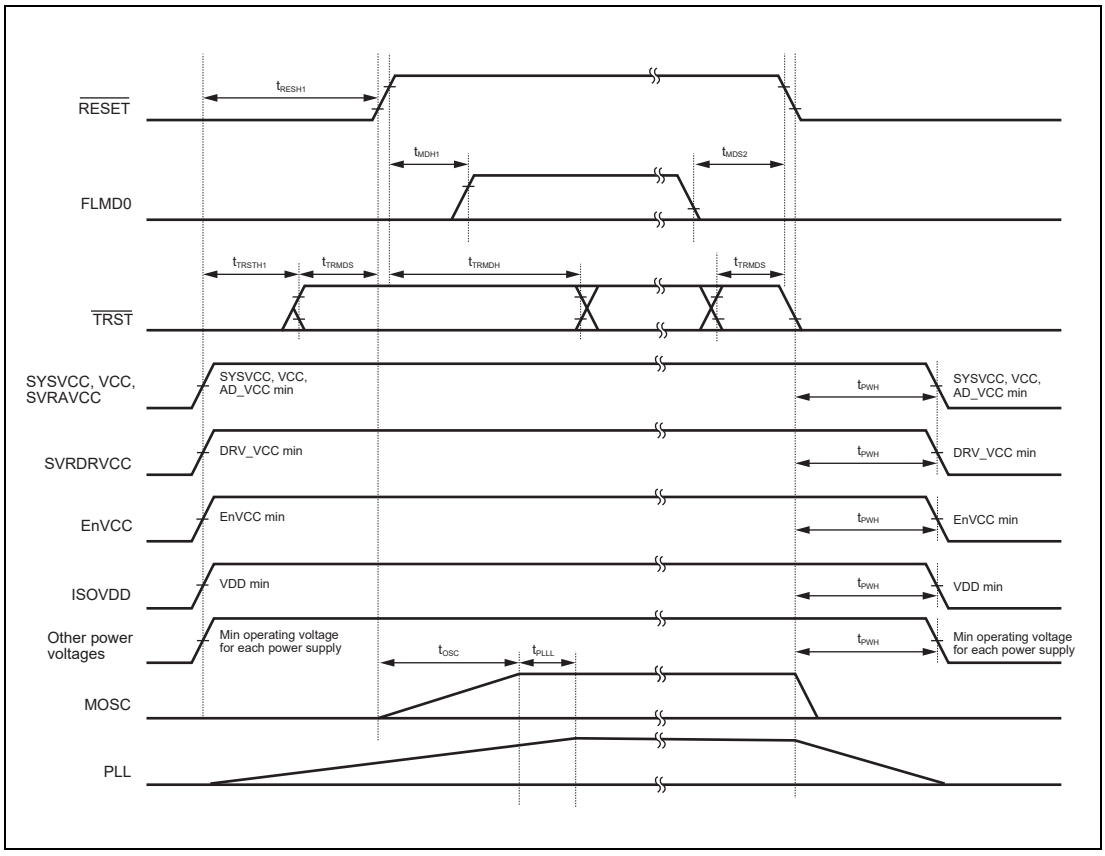


Figure 3.13 Power On/Off Timings (Normal operating mode and User boot mode 0)

NOTE

DVCC, DVDD, ERAMVCC, ERAMVDD and EMUVDD are not included in the other power voltages.
For power on/off timing about those power sources, see **Figure 3.18, EMUVCC, EMUVDD Power On / Off Timings** and **Section 3.3.30, Debug Resource (Aurora, ERAM) Specific Reset Timing**.

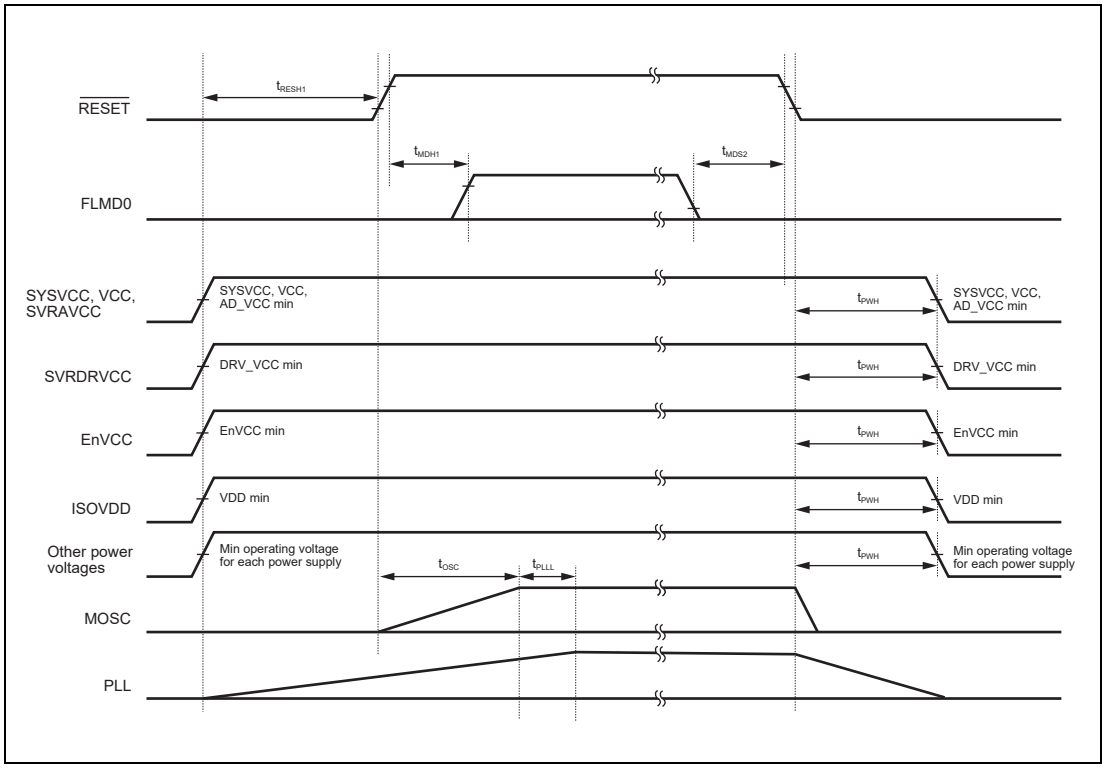


Figure 3.14 Power On/Off Timings (Serial programming mode 0)

NOTE

DVCC, DVDD, ERAMVCC, ERAMVDD and EMUVDD are not included in the other power voltages.

For power on/off timing about those power sources, see **Figure 3.18, EMUVCC, EMUVDD Power On / Off Timings** and **Section 3.3.30, Debug Resource (Aurora, ERAM) Specific Reset Timing**.

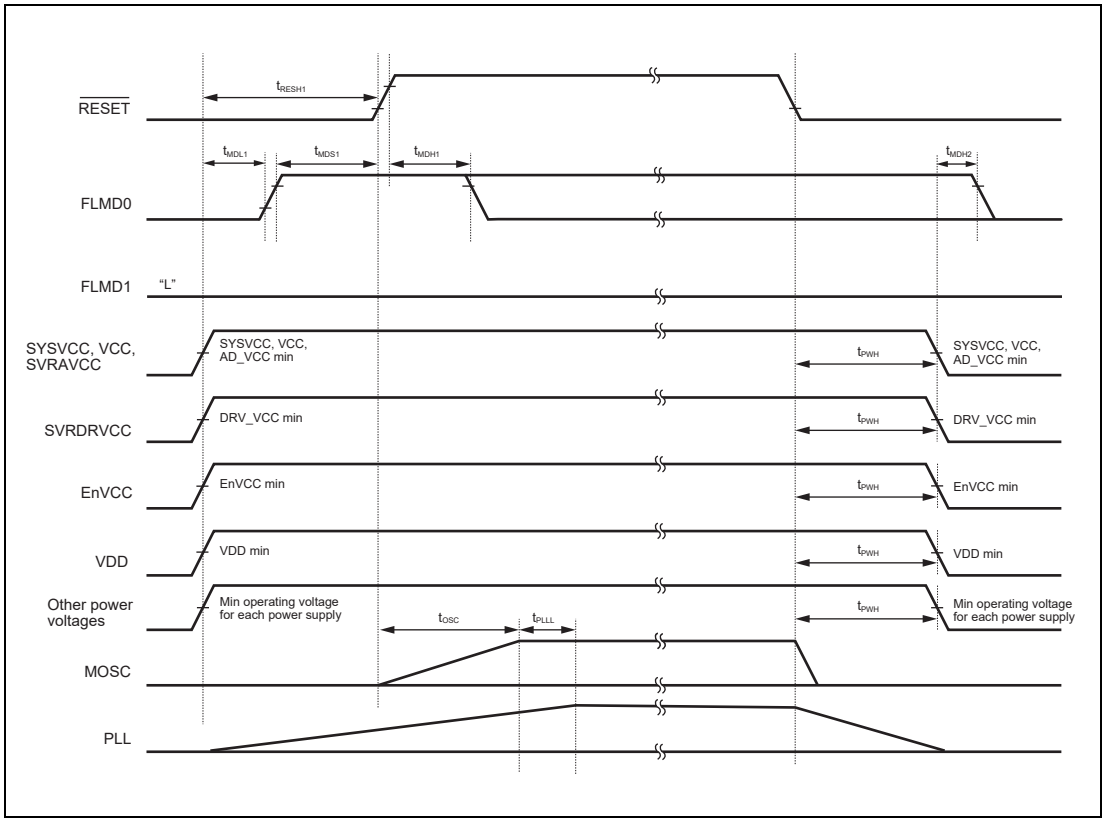


Figure 3.15 Power On/Off Timings (Serial programming mode 1)

NOTE

DVCC, DVDD, ERAMVCC, ERAMVDD and EMUVDD are not included in the other power voltages.
For power on/off timing about those power sources, see **Figure 3.18, EMUVCC, EMUVDD Power On / Off Timings** and **Section 3.3.30, Debug Resource (Aurora, ERAM) Specific Reset Timing**.

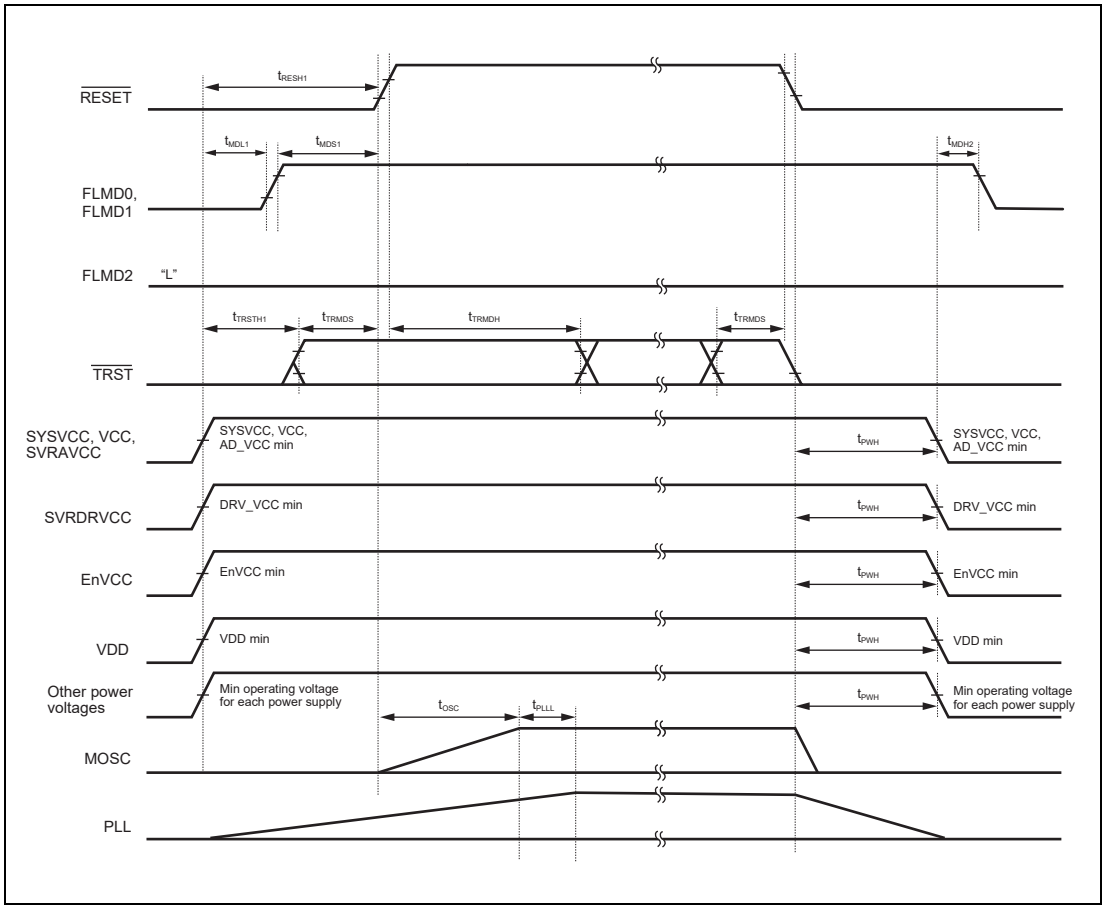


Figure 3.16 Power On/Off Timings (User boot mode 1)

NOTE

DVCC, DVDD, ERAMVCC, ERAMVDD and EMUVDD are not included in the other power voltages.

For power on/off timing about those power sources, see **Figure 3.18, EMUVCC, EMUVDD Power On / Off Timings** and **Section 3.3.30, Debug Resource (Aurora, ERAM) Specific Reset Timing**.

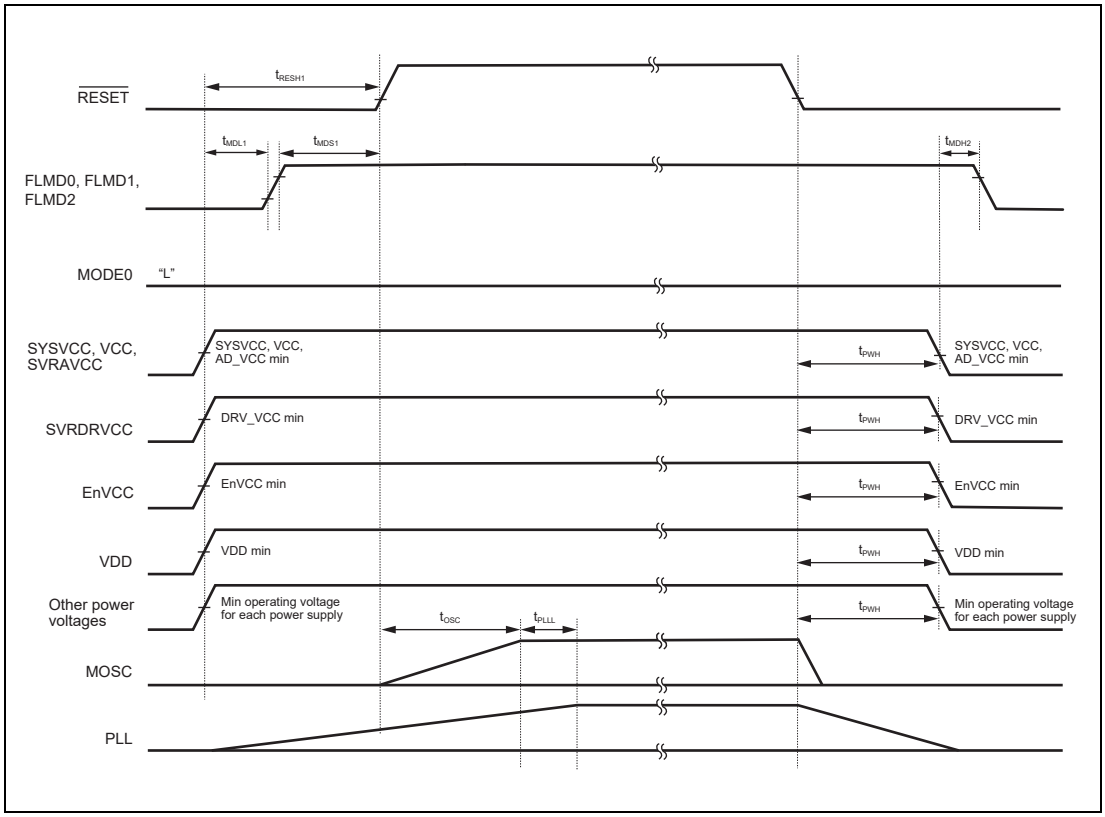


Figure 3.17 Power On/Off Timings (Boundary scan mode)

NOTE

DVCC, DVDD, ERAMVCC, ERAMVDD and EMUVDD are not included in the other power voltages.

For power on/off timing about those power sources, see **Figure 3.18, EMUVCC, EMUVDD Power On / Off Timings** and **Section 3.3.30, Debug Resource (Aurora, ERAM) Specific Reset Timing**.

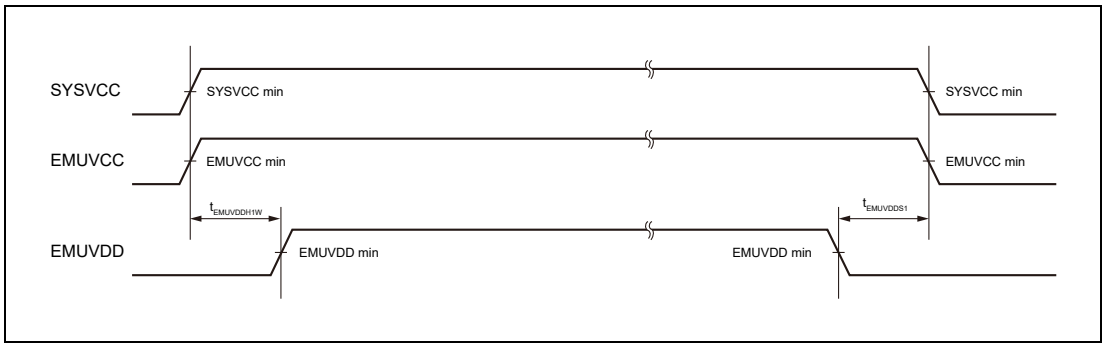


Figure 3.18 EMUVCC, EMUVDD Power On / Off Timings

3.3.2.1 Power Up Sequencing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**

Table 3.32 Power Up Sequencing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Runtime from release of $\overline{\text{RESET}}$ to start of instruction fetch					$1.5 + t_{BIST}$*1	ms

Note 1. t_{BIST} means BIST run time. Refer to **Table 44.490, BIST scenario selection at the next System Reset 2** on RH850/U2A-EVA Group User's Manual: Hardware **Section 44.6.2.41, BSEQ0SEL — BIST Scenario Select Register** for details. Note that the given BIST run time is the typical value and the tolerance of the corresponding clock needs to be taken into account for the maximum value.

3.3.3 Standby Transition/Return Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**

Table 3.33 DeepSTOP Transition/Return Timing In case of VDD External Supply

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Wake-up trigger to PWRCTL delay time	$t_{DPWRCTL}$				100	µs
VDD hold time	t_{HDD}		0			µs
VDD power-on start time	t_{PDD}		0			µs

3.3.4 Clock Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.34 Clock Output Timing*1

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock output period time	t_{CLKOUT}		41.6			ns
Clock output high level width	t_{WCOH}		t_{CLKOUT} / 2 – 10			ns
Clock output low level width	t_{WCOL}		t_{CLKOUT} / 2 – 10			ns

Note 1. There is a function to output the internal clock via EXTCLKnO pin.

NOTE

For base clock, refer to related RH850/U2A-EVA Group User's Manual: Hardware **Section 13, Clock Controller**.

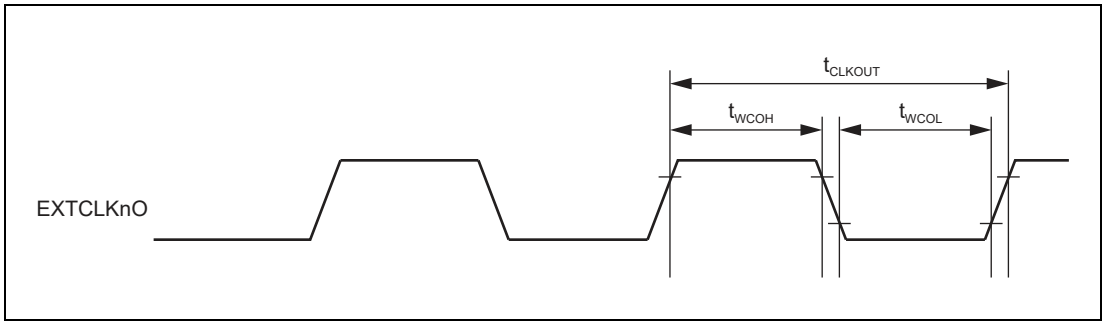


Figure 3.19 Clock Output Timing

3.3.5 Output Slew Rate

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.35 Output Slew Rate

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Output rise and fall time	t_{KRP11}/t_{KFP11}	Drive strength = 1 20% to 80%	CL = 100 pF			6.7	ns
	t_{KRP12}/t_{KFP12}	Drive strength = 2 20% to 80%	CL = 30 pF			4.0	ns
			CL = 50 pF			6.7	ns
			CL = 100 pF			13.4	ns
	t_{KRP13}/t_{KFP13}	Drive strength = 3 20% to 80%	CL = 30p F			6.7	ns
			CL = 50 pF			11.1	ns
			CL = 100 pF			21.0	ns
	t_{KRP14}/t_{KFP14}	Drive strength = 4 20% to 80%	CL = 30 pF			13.5	ns
			CL = 50 pF			22.5	ns
			CL = 100 pF			45.0	ns
	t_{KRP15}/t_{KFP15}	Drive strength = 5 20% to 80%	CL = 30 pF			27.0	ns
			CL = 50 pF			45.0	ns
			CL = 100 pF			90.0	ns

3.3.6 Control Signal Timing

3.3.6.1 $\overline{\text{RESET}}$ Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.36 $\overline{\text{RESET}}$ Timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
$\overline{\text{RESET}}$ input low level width	t_{WRSL}*1		800			µs
$\overline{\text{RESET}}$ pulse rejection width*2	t_{WRRJ}		400		2400	ns

Note 1. t_{WRSL} is the minimum required time to complete the reset state generated by an external reset signal. When an external reset signal is input that is shorter than this time, the reset state will continue even after the external reset release. This microcontroller is completely reset after completion of the reset state. An external reset request is accepted with a reset input width of more than the maximum time of t_{WRRJ}. When the reset pulse width is less than the minimum value of the reset noise rejection width, the reset request is not accepted. When the reset signal is input during DeepSTOP mode, the reset state will continue during the wait time set by PWRGD_CNT even when the external reset signal is released.

Note 2. Input pulses between min. and max. value result in an undefined signal condition (i.e. pulses might be filtered out or not). This characteristic is not tested in production.

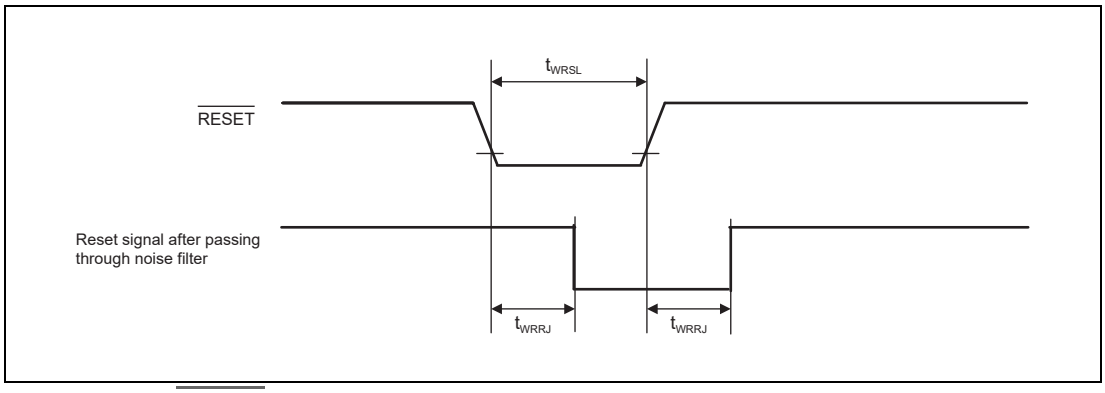


Figure 3.20 $\overline{\text{RESET}}$ Timing

3.3.6.2 Interrupt, Wake-up and Error Input Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.37 Interrupt Timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
NMI input high level width	t_{WNIH}	*3	600			ns
		*4	20			µs
NMI input low level width	t_{WNIL}	*3	600			ns
		*4	20			µs
NMI pulse rejection width*2	t_{WNIRJ}		100		600	ns
INTPn input high level width	t_{WITH}	*3	600			ns
		*4	20			µs
INTPn input low level width	t_{WITL}	*3	600			ns
		*4	20			µs
INTPn pulse rejection width*2	t_{WIRJ}		100		600	ns
RLIN3nRX wake-up input high level width	t_{WRLINH}		(S + 1) x 1/fs*1			ns
RLIN3nRX wake-up input low level width	t_{WRLINL}		(S + 1) x 1/fs*1			ns
RLIN3nRX wake-up pulse rejection width*2	$t_{WRLINRJ}$		(S – 1) x 1/fs*1		(S + 1) x 1/fs*1	ns
CANnRX wake-up input high level width	t_{WCANH}		(S + 1) x 1/fs*1			ns
CANnRX wake-up input low level width	t_{WCANL}		(S + 1) x 1/fs*1			ns
CANnRX wake-up pulse rejection width*2	t_{WCANRJ}		(S – 1) x 1/fs*1		(S + 1) x 1/fs*1	ns
FLXnRXDA wake-up input high level width	t_{WFLXH}		(S + 1) x 1/fs*1			ns
FLXnRXDA wake-up input low level width	t_{WFLXL}		(S + 1) x 1/fs*1			ns
FLXnRXDA wake-up pulse rejection width*2	t_{WFLXRJ}		(S – 1) x 1/fs*1		(S + 1) x 1/fs*1	ns
$\overline{\text{ERRORINn}}$ wake-up input high level width	t_{WERRH}		(S + 1) x 1/fs*1			ns
$\overline{\text{ERRORINn}}$ wake-up input low level width	t_{WERRL}		(S + 1) x 1/fs*1			ns
$\overline{\text{ERRORINn}}$ wake-up pulse rejection width*2	t_{WERRRJ}		(S – 1) x 1/fs*1		(S + 1) x 1/fs*1	ns

Note 1. S: Number of sampling times
fs: The value given by following formula

$$fs = \frac{f_{DNFCK}}{PRS}$$

f_{DNFCK}: frequency of CLK_LSB
PRS: 1, 2, 4, 8, … , 128

Note 2. Input pulses between min. and max. value result in an undefined signal condition (i.e. pulses might be filtered out or not). This characteristic is not tested in production.

Note 3. Edge Detection or Level Detection (CLKA_LPS is operated by CLK_HSIOSC/20)

Note 4. Level Detection (CLKA_LPS is operated by CLK_LSIOSC)

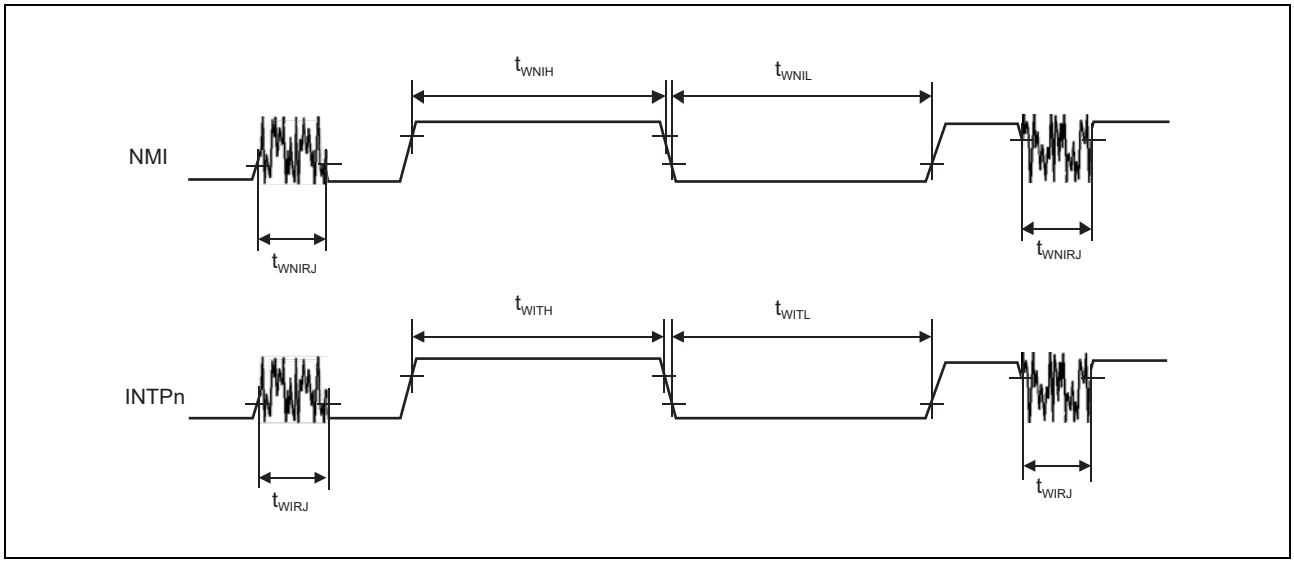


Figure 3.21 Interrupt, wake-up and error input timing

3.3.6.3 Mode Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.38 Mode Timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
FLMD0, FLMD1, FLMD2, MODE0 input high level width	t_{WMDH}		600			ns
FLMD0, FLMD1, FLMD2, MODE0 input low level width	t_{WMDL}		600			ns
FLMD0, FLMD1, FLMD2, MODE0 pulse rejection width*1	t_{WMDRJ}		100		600	ns

Note 1. Input pulses between min. and max. value result in an undefined signal condition (i.e. pulses might be filtered out or not). This characteristic is not tested in production.

NOTE

Switching of FLMD0 after rising edge of $\overline{\text{RESET}}$ is prohibited except for serial programming mode.

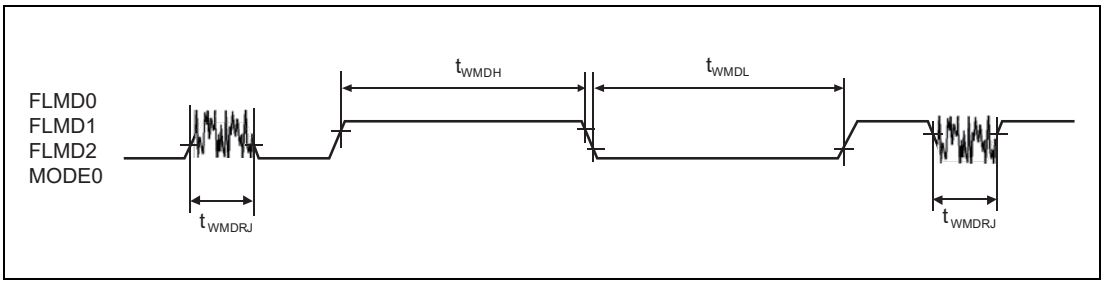


Figure 3.22 Mode Timing

3.3.6.4 ADTRG Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.39 ADCJnTRGm Timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
ADCJnTRGm input high level width	t_{WADH}		(S + 1) x 1/fs*1			ns
ADCJnTRGm input low level width	t_{WADL}		(S + 1) x 1/fs*1			ns
ADCJnTRGm pulse rejection width*2	t_{WADRJ}		(S – 1) x 1/fs*1		(S + 1) x 1/fs*1	ns

Note 1. S: Number of sampling times
fs: The value given by the following formula

$$fs = \frac{f_{DNFCK}}{PRS}$$

f_{DNFCK}: frequency of CLK_ADC, CLKA_ADC
PRS: 1, 2, 4, 8, … , 128

Note 2. Input pulses between min. and max. value result in an undefined signal condition (i.e. pulses might be filtered out or not). This characteristic is not tested in production.

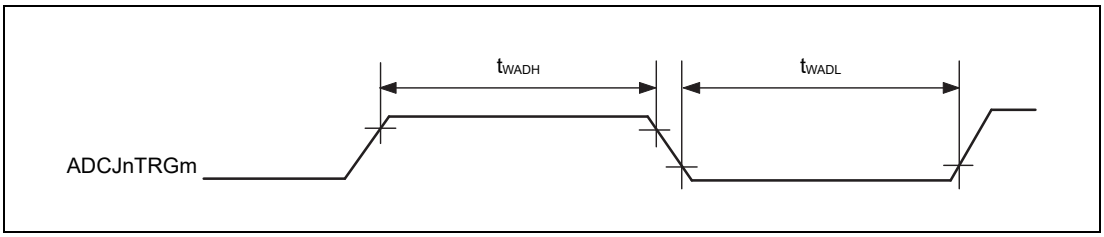


Figure 3.23 ADCJnTRGm Timing

3.3.6.5 Communication Signal Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.40 Control Signal

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
SENTnRX input high level width	$t_{WSENTIH}$	Analog filter	600			ns
		Digital filter	(S + 1) x 1/fs*1			ns
SENTnRX input low level width	$t_{WSENTIL}$	Analog filter	600			ns
		Digital filter	(S + 1) x 1/fs*1			ns
SENTnRX pulse rejection width	$t_{WSENTIRJ}$	Analog filter	100		600	ns
		Digital filter	(S – 1) x 1/fs*1		(S + 1) x 1/fs*1	ns
PSI5nRX input high level width*2	$t_{WPSI5IH}$	Analog filter	600			ns
		Digital filter	(S + 1) x 1/fs*1			ns
PSI5nRX input low level width	$t_{WPSI5IL}$	Analog filter	600			ns
		Digital filter	(S + 1) x 1/fs*1			ns
PSI5nRX pulse rejection width*2	$t_{WPSI5IRJ}$	Analog filter	100		600	ns
		Digital filter	(S – 1) x 1/fs*1		(S + 1) x 1/fs*1	ns

Note 1. S: Number of sampling times
fs: The value given by the following formula

$$fs = \frac{f_{DNFCK}}{PRS}$$

f_{DNFCK}: frequency of CLK_HSB
PRS: 1, 2, 4, 8, … , 128

Note 2. Input pulses between min. and max. value result in an undefined signal condition (i.e. pulses might be filtered out or not). This characteristic is not tested in production.

3.3.7 Low Power Sampler (DPIN input) Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- Drive strength = 4 (SELDP2-0)

Table 3.41 Low Power Sampler Timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
DPINn input delay time	t_{DSDDI}				150	ns

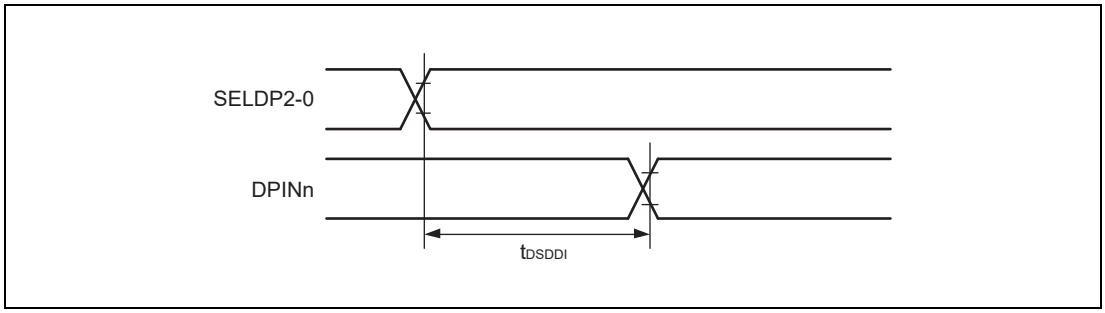


Figure 3.24 Low Power Sampler Timing

3.3.8 SFMA Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- Drive strength = 2
- Buffer type = Sch1

Table 3.42 SFMA Timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
SFMA0CLK clock cycle	$t_{SFMAcyc}$		25			ns
SFMA0CLK high pulse width	t_{SFMAWH}		0.4 × $t_{SFMA0cyc}$		0.6 × $t_{SFMA0cyc}$	ns
SFMA0CLK low pulse width	t_{SFMAWL}		0.4 × $t_{SFMA0cyc}$		0.6 × $t_{SFMA0cyc}$	ns
Data input setup time	$t_{SFMADIS}$		9.0			ns
Data input hold time	t_{SFMDIH}		0.0			ns
SFMA0SSL setup time	t_{SFMASS}		1 × $t_{SFMA0cyc}$ – 12.5		8 × $t_{SFMA0cyc}$	ns
SFMA0SSL hold time	t_{SFMASH}		1.5 × $t_{SFMA0cyc}$		8.5 × $t_{SFMA0cyc}$ + 12.5	ns
Continuous transfer delay time	$t_{SFMACTD}$		1 × $t_{SFMA0cyc}$		8 × $t_{SFMA0cyc}$	ns
Data output delay time	$t_{SFMADOD}$				6.6	ns
Data output hold time	$t_{SFMADOH}$		–4.6			ns
Data output buffer on time	$t_{SFMADBON}$				6.6	ns
Data output buffer off time	$t_{SFMADBOFF}$		–7.0		3.0	ns

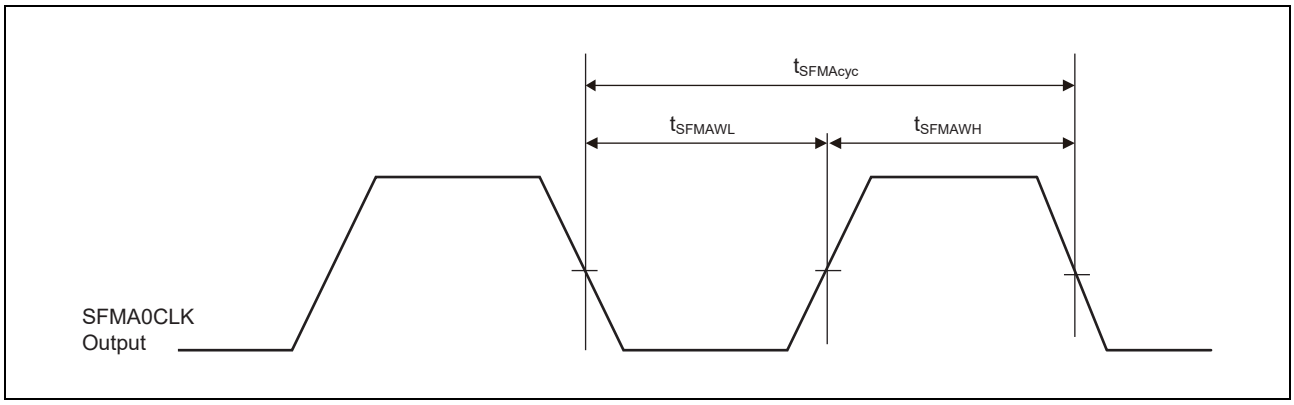


Figure 3.25 SFMA Clock Output Timing

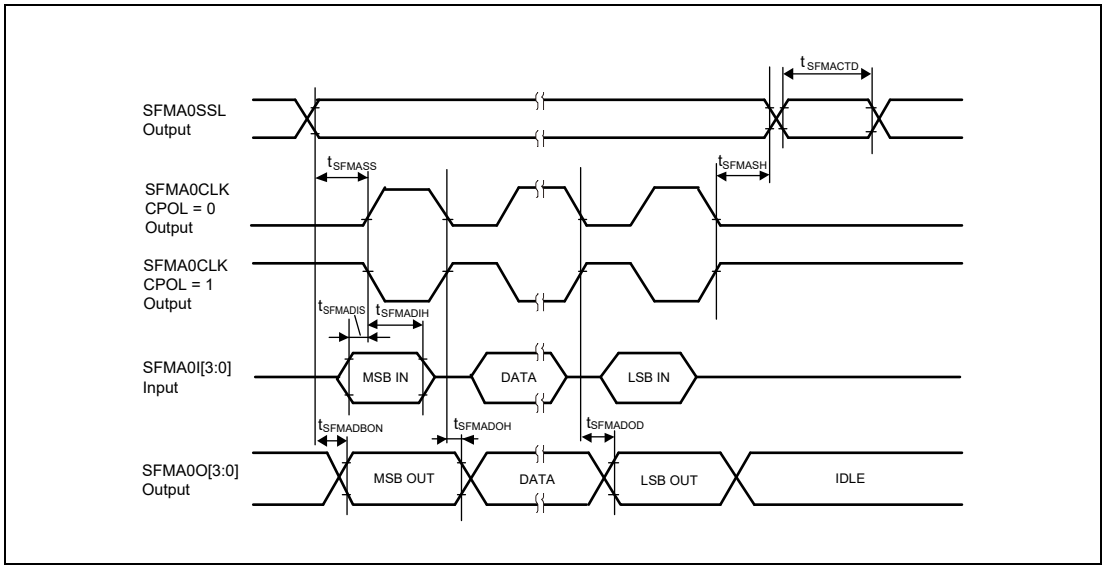


Figure 3.26 SFMA Transmission and Reception Timing (CPHAT = 0, CPHAR = 0)

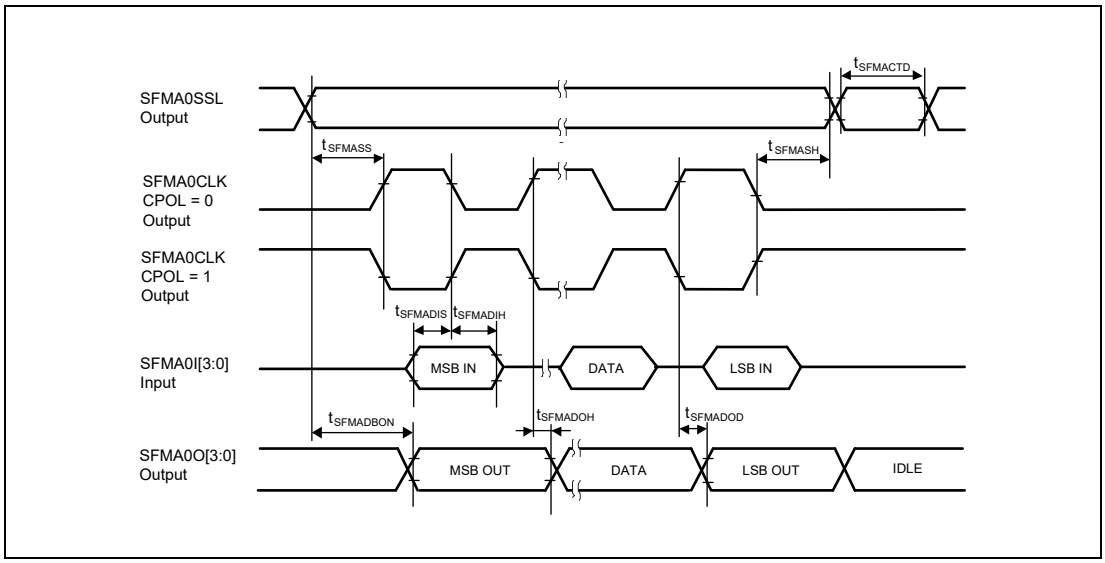


Figure 3.27 SFMA Transmission and Reception Timing (CPHAT = 1, CPHAR = 1)

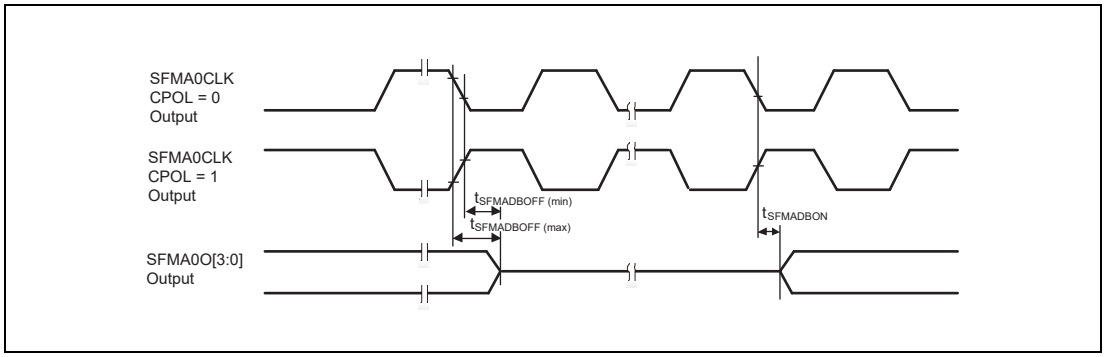


Figure 3.28 SFMA Timing Switching the Buffers on and off (CPHAT = 0, CPHAR = 0)

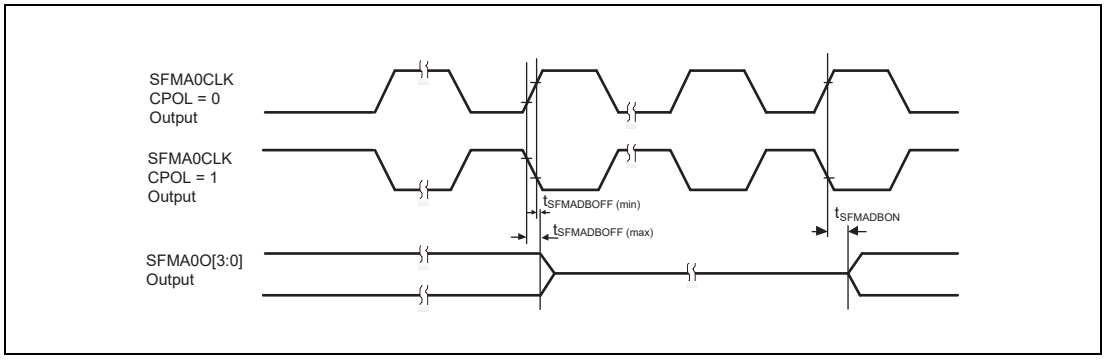


Figure 3.29 SFMA Timing for Switching the Buffers on and off (CPHAT = 1, CPHAR = 1)

3.3.9 MMCA Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- Drive strength = 2
- Buffer type = Sch1

Table 3.43 MMCA Timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
MMCA0CLK clock cycle	$t_{MMCA0CYC}$		25			ns
MMCA0CLK high time	$t_{MMCA0WH}$		6.5			ns
MMCA0CLK low time	$t_{MMCA0WL}$		6.5			ns
MMCA0CMD output data delay time	$t_{MMCA0CMDD}$		– 6.5		6.5	ns
Data output delay time	$t_{MMCA0DADD}$		– 6.5		6.5	ns
MMCA0CMD input data setup time	$t_{MMCA0CMS}$		7.5			ns
MMCA0CMD input data hold time	$t_{MMCA0CMH}$		2.5			ns
Data input setup time	$t_{MMCA0DAS}$		7.5			ns
Data input hold time	$t_{MMCA0DAH}$		2.5			ns

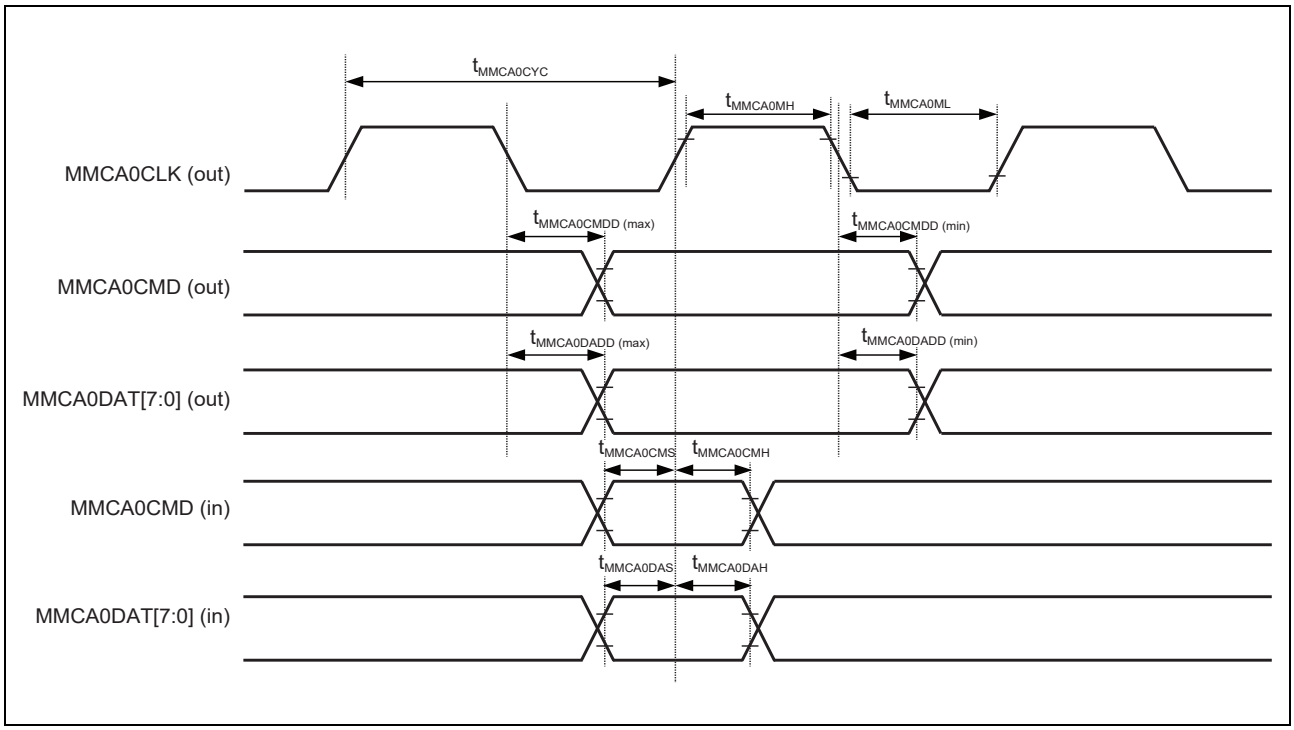


Figure 3.30 MMCA Timing

3.3.10 MSPI Timing

3.3.10.1 MSPI Communication Speed Overview

Table 3.44 MSPI Communication Speed Overview (1/3)

MSPIn pin name		Port	Max. Frequency
MSPI0	SC	P4_6	10 MHz
	SO	P4_5	10 MHz
	SI	P4_7	10 MHz
	SC	P6_8	10 MHz
	SO	P6_9	10 MHz
	SI	P6_7	10 MHz
	SC	P2_12	20 MHz
	SO	P2_13	20 MHz
	SI	P2_11	20 MHz
	SCKN / SCKP	P2_14, P2_15	40 MHz
	SON / SOP	P2_12, P2_13	40 MHz
	SIN / SIP	P2_10, P2_11	40 MHz
MSPI1	SC	P2_2	10 MHz
	SO	P5_2	10 MHz
	SI	P2_1	10 MHz
	SC	P6_8	10 MHz
	SO	P6_7	10 MHz
	SI	P6_9	10 MHz
	SC	P10_3	20 MHz
	SO	P10_2	20 MHz
	SI	P10_4	20 MHz
	SCKN / SCKP	P4_10, P4_9	40 MHz
	SON / SOP	P4_8, P4_7	40 MHz
	SIN / SIP	P4_6, P4_5	40 MHz
MSPI2	SC	P4_7	10 MHz
	SO	P4_6	10 MHz
	SI	P4_10	10 MHz
	SC	P10_11	10 MHz
	SO	P10_10	10 MHz
	SI	P10_12	10 MHz
	SC	P2_0	20 MHz (The selection of "Drive strength = 1" is available at equal or less than 10 MHz.)
	SO	P2_5	20 MHz (The selection of "Drive strength = 1" is available at equal or less than 10 MHz.)
	SI	P2_3	20 MHz

Table 3.44 MSPI Communication Speed Overview (2/3)

MSPIn pin name		Port	Max. Frequency
MSPI3	SC	P22_4	10 MHz (The selection of "Drive strength = 1" is available)
	SO	P22_0	10 MHz (The selection of "Drive strength = 1" is available)
	SI	P22_1	10 MHz
	SC	P24_10	10 MHz
	SO	P24_13	10 MHz
	SI	P24_12	10 MHz
	SC	P5_2	20 MHz
	SO	P5_4	20 MHz
	SI	P5_3	20 MHz
MSPI4	SC	P23_0	10 MHz
	SO	P23_2	10 MHz
	SI	P23_1	10 MHz
	SC	P21_0	20 MHz
	SO	P21_2	20 MHz
	SI	P21_1	20 MHz
MSPI5	SC	P12_0	10 MHz
	SO	P12_2	10 MHz
	SI	P12_1	10 MHz
	SC	P24_4	20 MHz
	SO	P24_6	20 MHz
	SI	P24_5	20 MHz
MSPI6	SC	P9_0	10 MHz
	SO	P9_2	10 MHz
	SI	P9_1	10 MHz
	SC	P11_0	10 MHz
	SO	P11_2	10 MHz
	SI	P11_1	10 MHz
MSPI7	SC	P11_8	10 MHz
	SO	P11_10	10 MHz
	SI	P11_9	10 MHz
	SC	P19_0	10 MHz
	SO	P19_2	10 MHz
	SI	P19_1	10 MHz
MSPI8	SC	P0_0	10 MHz
	SO	P0_2	10 MHz
	SI	P0_1	10 MHz
	SC	P18_1	10 MHz
	SO	P18_3	10 MHz
	SI	P18_2	10 MHz

Table 3.44 MSPI Communication Speed Overview (3/3)

MSPIn pin name		Port	Max. Frequency
MSPI9	SC	P1_0	10 MHz
	SO	P1_2	10 MHz
	SI	P1_1	10 MHz
	SC	P18_8	10 MHz
	SO	P18_10	10 MHz
	SI	P18_9	10 MHz

3.3.10.2 MSPI Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- Buffer type = Sch1

Table 3.45 MSPI Timing (Master mode : Communication Speed 10MHz)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
MSPI operation clock cycle	$T_{MSPInCLK}$		12.5			ns
MSPInSCK cycle*1*5	T_{SCKCYC}		100			ns
MSPInSCK Low/High width*1	T_{SCKWID}	CL = 30 pF Drive strength = 3	0.5 × T_{SCKCYC} – 9			ns
		CL = 50 pF Drive strength = 3	0.5 × T_{SCKCYC} – 12			ns
		CL = 100 pF Drive strength = 3	0.5 × T_{SCKCYC} – 23			ns
		CL = 30 pF Drive strength = 4	0.5 × T_{SCKCYC} – 15.5			ns
		CL = 50 pF Drive strength = 2	0.5 × T_{SCKCYC} – 10			ns
		CL = 100 pF Drive strength = 1*4	0.5 × T_{SCKCYC} – 10			ns
Chip select signal setup time*2*6	T_{MCSSU}	$T_{MSPInCLK}$ = 12.5 ns	MSPInSEUPm [11:0] x $T_{MSPInCLK}$ - 15			ns
Chip select signal hold time*3	T_{MCSHO}	$T_{MSPInCLK}$ = 12.5 ns	MSPInHOLDm [11:0] x $T_{MSPInCLK}$ - 5			ns
Receive data setup time (MSPInSAMP =0)	T_{MSISU1}		20			ns
Receive data setup time (MSPInSAMP =1)	T_{MSISU2}		20			ns
Receive data hold time (MSPInSAMP =0)	T_{MSIHO}		0			ns
Receive data hold time (MSPInSAMP =1)	T_{MSIHO}		0			ns
Transmit data delay time	T_{MSODL}				7	ns
Transmit data hold time	T_{MSOHL}		(T_{SCKCYC} / 2) – 5			ns

Note 1. This item is programmable, the value can be set by MSPInPRCSm[1:0] and MSPInCDIVm[4:0].
Note 2. This item is programmable, the value can be set by MSPInSEUPm[11:0] and it must be set to 002_H or above.
Note 3. This item is programmable, the value can be set by MSPInHOLDm.
Note 4. The selection of "Drive strength = 1" is available on P2_0 and P22_4 only.
Note 5. Use by “PCLK/2 ≥ MSPInSCK”.
Note 6. When using the MSPI at master mode with the setting MSPInCFGm1.MSPInCPHAm = 0, set the period from CS active to the first edge of SCK to 1/2 or more of the communication rate by MSPInSEUPm.

Table 3.46 MSPI Timing (Master mode : Communication Speed 20MHz)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
MSPI operation clock cycle	$T_{MSPInCLK}$		12.5			ns
MSPInSCK cycle*1*4	T_{SCKCYC}		50			ns
MSPInSCK Low/High width*1	T_{SCKWID}	CL = 15pF@50Ω Drive strength = 3	0.5 × T_{SCKCYC} – 6			ns
Chip select signal setup time*2*5	T_{MCSSU}	$T_{MSPInCLK}$ = 12.5 ns	MSPInSEUPm [11:0] x $T_{MSPInCLK}$ – 15			ns
Chip select signal hold time*3	T_{MCSHO}	$T_{MSPInCLK}$ = 12.5 ns	MSPInHOLDm [11:0] x $T_{MSPInCLK}$ – 5			ns
Receive data setup time (MSPInSAMP = 1)	T_{MSISU2}		20			ns
Receive data hold time (MSPInSAMP = 1)	T_{MSIHO}		0			ns
Transmit data delay time	T_{MSODL}				7	ns
Transmit data hold time	T_{MSOHL}		(T_{SCKCYC}/2) – 5			ns

Note 1. This item is programmable, the value can be set by MSPInPRCSm[1:0] and MSPInCDIVm[4:0].
Note 2. This item is programmable, the value can be set by MSPInSEUPm[11:0] and it must be set to 002_H or above.
Note 3. This item is programmable, the value can be set by MSPInHOLDm.
Note 4. Use by “PCLK/2 ≥ MSPInSCK”.
Note 5. When using the MSPI at master mode with the setting MSPInCFGm1.MSPInCPHAm = 0, set the period from CS active to the first edge of SCK to 1/2 or more of the communication rate by MSPInSEUPm.

Table 3.47 MSPI Timing (Master mode : Communication Speed 40MHz)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
MSPI operation clock cycle	$T_{MSPInCLK}$		12.5			ns
MSPInSCK cycle*1*4	T_{SCKCYC}		25			ns
MSPInSCK Low/High width*1	T_{SCKWID}	CL = 15pF@LVDS	0.5 × T_{SCKCYC} – 2.5			ns
Chip select signal setup time*2*5	T_{MCSSU}	$T_{MSPInCLK}$ = 12.5 ns	MSPInSEUPm [11:0] x $T_{MSPInCLK}$ – 15			ns
Chip select signal hold time*3	T_{MCSHO}	$T_{MSPInCLK}$ = 12.5 ns	MSPInHOLDm [11:0] x $T_{MSPInCLK}$ – 5			ns
Receive data setup time (MSPInSAMP = 1)	T_{MSISU2}		7			ns
Receive data hold time (MSPInSAMP = 1)	T_{MSIHO}		0			ns
Transmit data delay time	T_{MSODL}				5	ns
Transmit data hold time	T_{MSOHL}		(T_{SCKCYC}/2) – 5			ns

Note 1. This item is programmable, the value can be set by MSPInPRCSm[1:0] and MSPInCDIVm[4:0].
Note 2. This item is programmable, the value can be set by MSPInSEUPm[11:0] and it must be set to 002_H or above.
Note 3. This item is programmable, the value can be set by MSPInHOLDm.
Note 4. Use by “PCLK/2 ≥ MSPInSCK”.
Note 5. When using the MSPI at master mode with the setting MSPInCFGm1.MSPInCPHAm = 0, set the period from CS active to the first edge of SCK to 1/2 or more of the communication rate by MSPInSEUPm.

Table 3.48 MSPI Timing (Slave mode : Communication Speed 10MHz)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
MSPI operation clock cycle	$T_{MSPInCLK}$		12.5			ns
MSPInSCK cycle	T_{SCKCYC}		100			ns
MSPInSCK Low/High width	T_{SCKWID}		$0.5 \times T_{SCKCYC} - 23$			ns
Chip select signal setup time (MSPInCSIE = 1)	T_{SCSSU}		15			ns
Chip select signal hold time (MSPInCSIE = 1)	T_{SCSHO}		10			ns
Receive data setup time	T_{SSISU}		6			ns
Receive data hold time	T_{SSIHO}		5			ns
Transmit data delay time 1	T_{SSODL1}				54	ns
Transmit data delay time 2 (MSPInCSIE = 1)	T_{SSODL2}				40	ns
Transmit data hold time	T_{SSOHL}		$(T_{SCKCYC}/2) - 5$			ns
Transmit data release time (MSPInCSIE = 1)	T_{SSOREL}				40	ns

Table 3.49 MSPI Timing (Slave mode : Communication Speed 20MHz)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
MSPI operation clock cycle	$T_{MSPInCLK}$		12.5			ns
MSPInSCK cycle	T_{SCKCYC}		50			ns
MSPInSCK Low/High width	T_{SCKWID}		$0.5 \times T_{SCKCYC} - 6$			ns
Chip select signal setup time (MSPInCSIE = 1)	T_{SCSSU}		15			ns
Chip select signal hold time (MSPInCSIE = 1)	T_{SCSHO}		10			ns
Receive data setup time	T_{SSISU}		6			ns
Receive data hold time	T_{SSIHO}		5			ns
Transmit data delay time 1	T_{SSODL1}				24	ns
Transmit data delay time 2 (MSPInCSIE = 1)	T_{SSODL2}				40	ns
Transmit data hold time	T_{SSOHL}		$(T_{SCKCYC}/2) - 5$			ns
Transmit data release time (MSPInCSIE = 1)	T_{SSOREL}				40	ns

Table 3.50 MSPI Timing (Slave mode: Communication Speed 40MHz)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
MSPI operation clock cycle	$T_{MSPInCLK}$		12.5			ns
MSPInSCK cycle	T_{SCKCYC}		25			ns
MSPInSCK Low/High width	T_{SCKWID}		0.5 × T_{SCKCYC} – 2.5			ns
Chip select signal setup time (MSPInCSIE = 1)	T_{SCSSU}		15			ns
Chip select signal hold time (MSPInCSIE = 1)	T_{SCSHO}		10			ns
Receive data setup time	T_{SSISU}		6			ns
Receive data hold time	T_{SSIHO}		5			ns
Transmit data delay time 1	T_{SSODL1}				12	ns
Transmit data hold time	T_{SSOHL}		(T_{SCKCYC}/2) – 5			ns

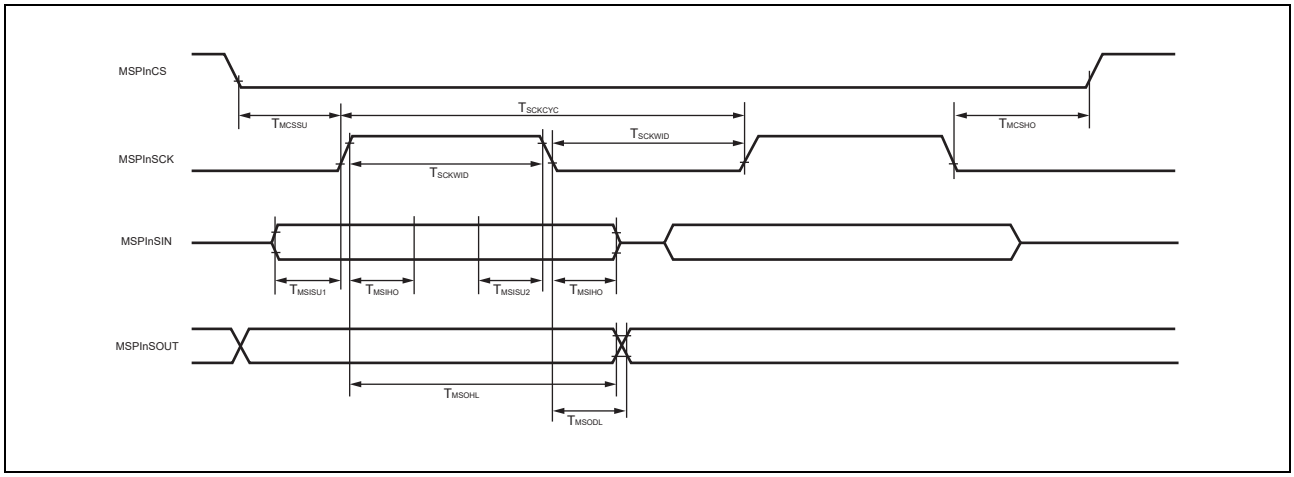


Figure 3.31 MSPIn Timing (Master Mode, MSPInCPHAm = 0)

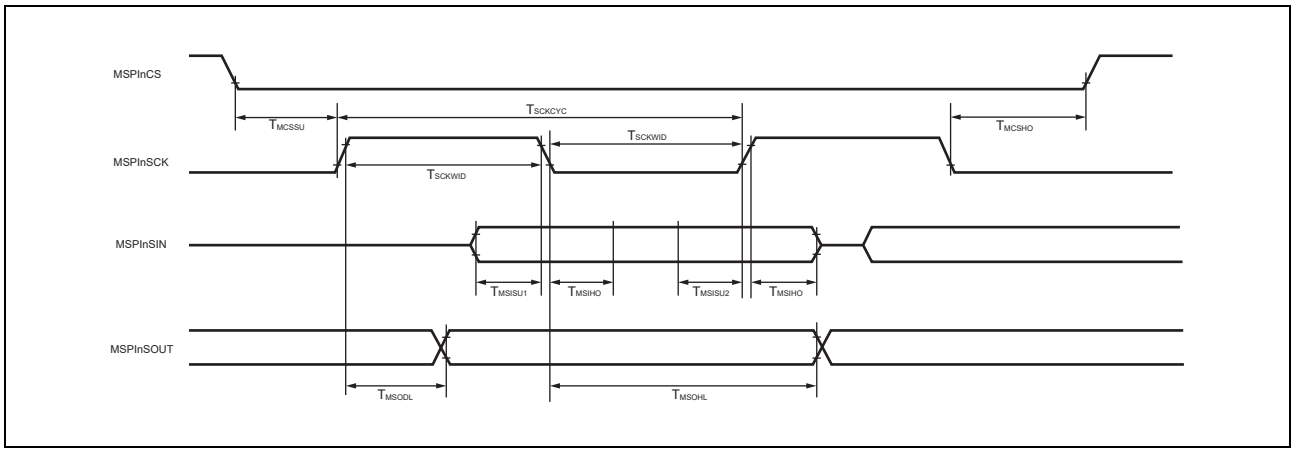


Figure 3.32 MSPIn Timing (Master Mode, MSPInCPHAm = 1)

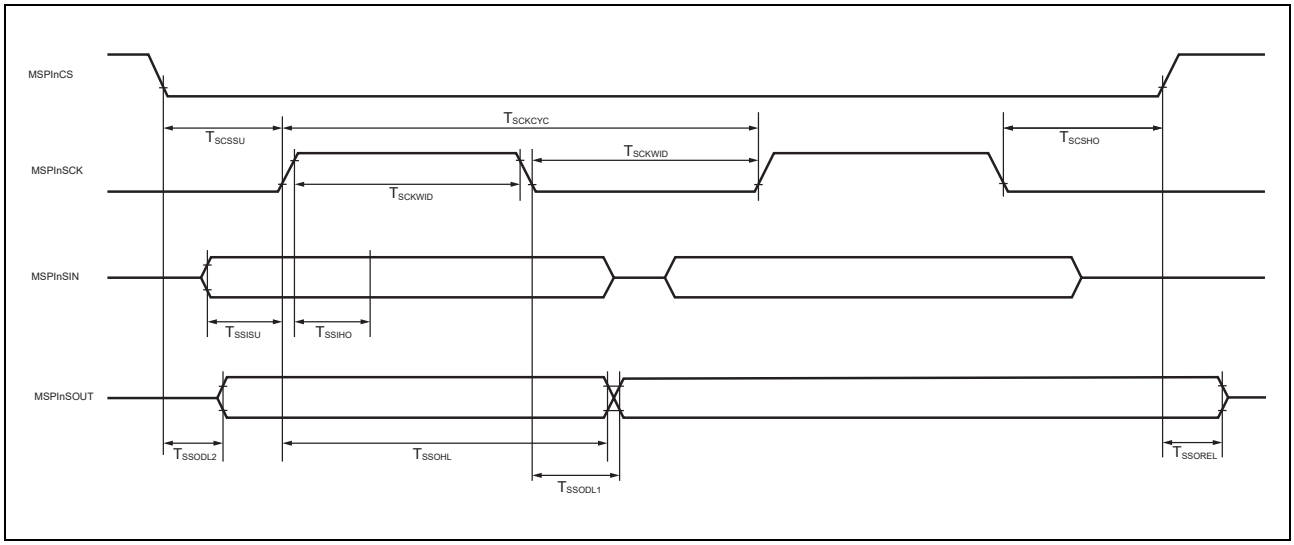


Figure 3.33 MSPIn Timing (Slave Mode, MSPInCPHA0 = 0)

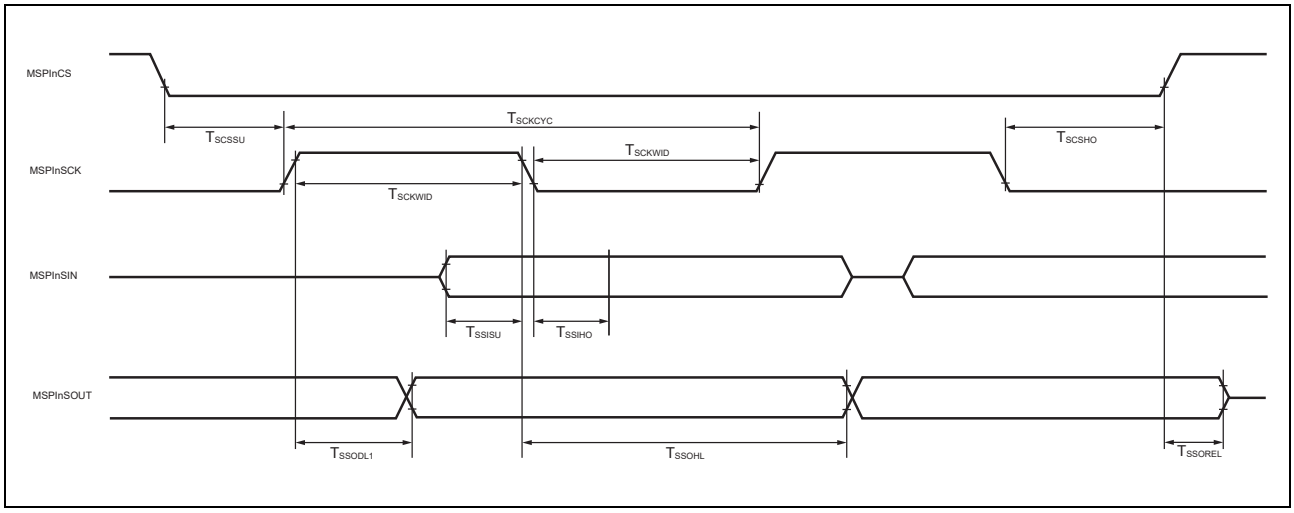


Figure 3.34 MSPIn Timing (Slave Mode, MSPInCPHA0 = 1)

3.3.11 SCI3 Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- Buffer type = Sch1

Table 3.51 SCI3 Timing (Master Mode, Asynchronous)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Transfer rate	r_{SCI3AS}				10	Mbps

Table 3.52 SCI3 Timing (Master Mode, Synchronous)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Output cycle time	$t_{SCI3Scyc}$		200			ns
Output clock pulse width	t_{SCI3SW}		0.4 × $t_{SCI3Scyc}$		0.6 × $t_{SCI3Scyc}$	ns
Transmit data delay time	$t_{SCI3TXD}$		–40		40	ns
Receive data setup time	$t_{SCI3RXS}$		4 × t_{PCLK}			ns
Receive data hold time	$t_{SCI3RXH}$		4 × t_{PCLK}			ns

Note: t_{PCLK} is the period of PCLK (CLK_HSB).

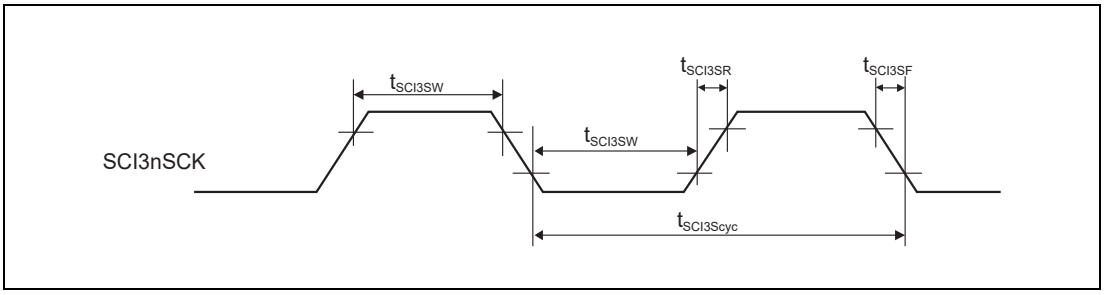


Figure 3.35 SCI Clock Input/Output Timing

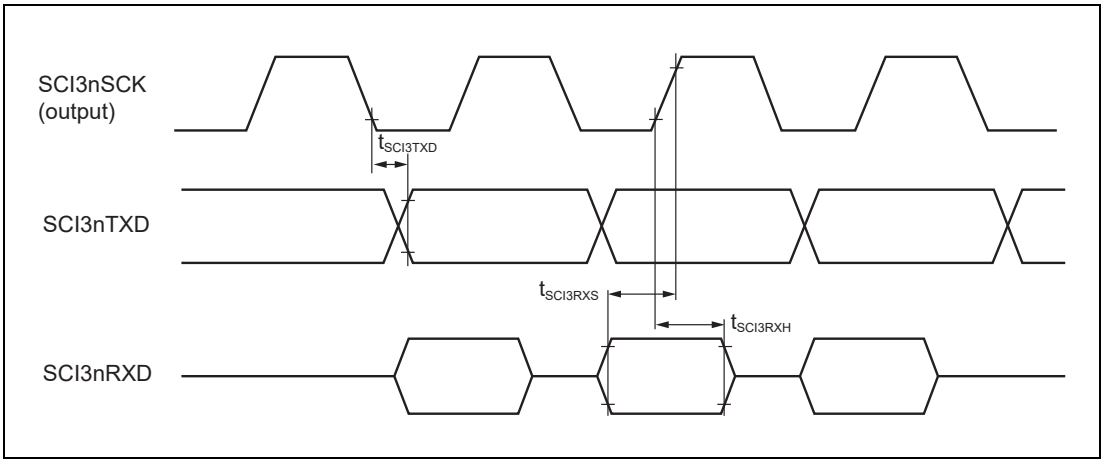


Figure 3.36 SCI3 Input/Output Timing, Clock Synchronous Mode (in Master Mode)

Table 3.53 SCI3 Timing (Slave Mode)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input cycle time	$t_{SCI3Scyc}$		200			ns
Input clock pulse width	t_{SCI3SW}		0.4 × $t_{SCI3Scyc}$		0.6 × $t_{SCI3Scyc}$	ns
Transmit data delay time*1	$t_{SCI3TXD}$		2 × t_{PCLK}		50 + 4 × t_{PCLK}	ns
Input clock rising time	t_{SCI3SR}				20	ns
Input clock falling time	t_{SCI3SF}				20	ns
Receive data setup time	$t_{SCI3RXS}$		4 × t_{PCLK}			ns
Receive data hold time	$t_{SCI3RXH}$		4 × t_{PCLK}			ns

Note 1. This does not apply to transmission of Data 0 (the first bit) which is transferred not in continuous transfer mode. Transmission of Data 0 (the first bit) which is transferred not in continuous transfer mode starts when TDRE becomes 0.

Note: t_{PCLK} is the period of PCLK (CLK_HSB).

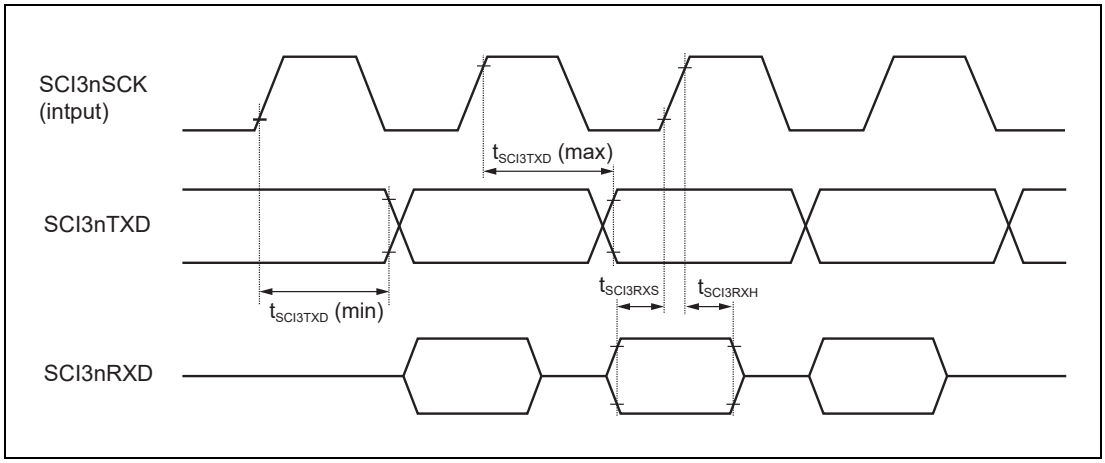


Figure 3.37 SCI3 Input/Output Timing, Clock Synchronous Mode (in Slave Mode)

3.3.12 RLIN3 Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- Drive strength = 4
- Buffer type = Sch1

Table 3.54 RLIN3 Timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
RLIN3 transfer rate	r_{RLin}	LIN mode			20	kbps
	r_{RLine}	LIN extended baud rate*1			115.2	kbps
	r_{RLurt}	UART mode			8	Mbps

Note 1. The LIN extended baud rate is not part of the LIN standard specification.

3.3.13 RIIC Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- Buffer type = Sch1

Table 3.55 RIIC Timing (Normal Mode)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
RIICnSCL clock period	f_{CLK}				100	kHz
Bus free time (between stop/start condition)	t_{BUF}		4.7			µs
Hold time[*1]	t_{HD}: STA		4.0			µs
RIICnSCL clock low level width	t_{LOW}		4.7			µs
RIICnSCL clock high level time	t_{HIGH}		4.0			µs
Setup time for start/restart condition	t_{SU}: STA		4.7			µs
Data hold time	t_{HD}: DAT	CBUS compatible master	5.0			µs
		I^2C mode	0[*2]		[*3]	µs
Data setup time	t_{SU}: DAT		250			ns
Stop condition setup time	t_{SU}: STO		4.0			µs

Note 1. At the start condition, the first clock pulse is generated after the hold time.

Note 2. The system requires a minimum of 300 ns hold time internally for the RIICnSDA signal (at VIH min. of RIICnSCL signal). In order to occupy the undefined area at the falling edge of RIICnSCL.

Note 3. If the system does not extend the RIICnSCL signal low hold time (t_{Low}), only the maximum data hold time (t_{HD}: DAT) needs to be satisfied.

Table 3.56 RIIC Timing (Fast Mode)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
RIICnSCL clock period	f_{CLK}				400	kHz
Bus free time (between stop/start condition)	t_{BUF}		1.3			µs
Hold time[*1]	t_{HD}: STA		0.6			µs
RIICnSCL clock low level width	t_{LOW}		1.3			µs
RIICnSCL clock high level time	t_{HIGH}		0.6			µs
Setup time for start/restart condition	t_{SU}: STA		0.6			µs
Data hold time	t_{HD}: DAT	I^2C mode	0[*2]		[*5]	µs
Data setup time	t_{SU}: DAT		100[*3]			ns
Stop condition setup time	t_{SU}: STO		0.6			µs
Pulse width with spike suppressed by input filter	t_{SP}		0		[*4]	ns

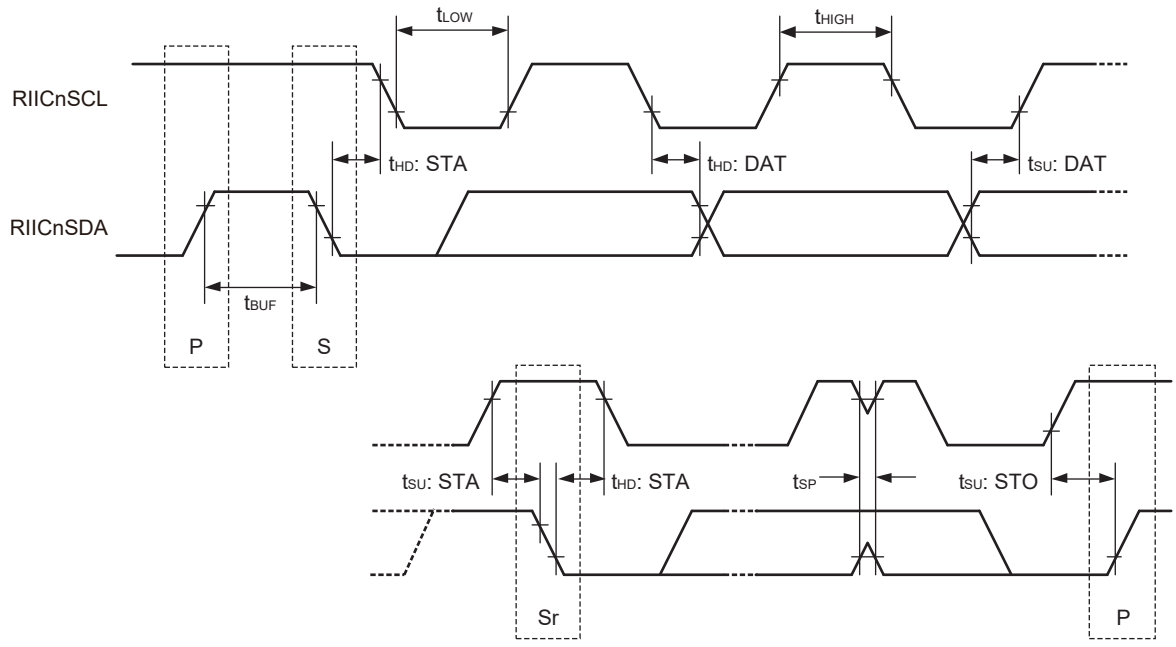
Note 1. At the start condition, the first clock pulse is generated after the hold time.

Note 2. The system requires a minimum of 300 ns hold time internally for the RIICnSDA signal (at VIH min. of RIICnSCL signal). In order to occupy the undefined area at the falling edge of RIICnSCL.

Note 3. The fast mode I^2C bus can be used in normal mode I^2C bus system. In this case, set the fast mode I^2C bus so that it meets the following conditions.
- If the system does not extend the RIICnSCL signal's low state hold time: t_{SU}: DAT ≥ 250 ns
- If the system extends the RIICnSCL signal's low state hold time:
Transmit the following data bit to the RIICnSDA line prior to releasing the RIICnSCL line (1250 ns: Normal mode I^2C bus specification).

Note 4. The filtered width is specified by the frequency of IICΦ and the value of RIICnMR3.NF[1:0].

Note 5. If the system does not extend the RIICnSCL signal low hold time (t_{Low}), only the maximum data hold time (t_{HD}: DAT) needs to be satisfied.



Note
P: Stop condition S: Start condition Sr: Restart condition

Figure 3.38 RIIC Timing

3.3.14 RS-CANFD Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- Buffer type = Sch1

Table 3.57 RS-CANFD Timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Transfer rate	r_{CN1}	Classical CAN mode			1	Mbps
	r_{CN2}	CAN FD mode (nominal bit rate)			1	Mbps
	r_{CN3}	CAN FD mode (data bit rate)			8	Mbps
Internal delay time	t_{DCIN}	$t_{INPUT} + t_{OUTPUT}$			50	ns

Note 1. For the configuration of the transfer speed, see RH850/U2A-EVA Group User's Manual: Hardware **Section 23.5.1.3, Baud Rate.**

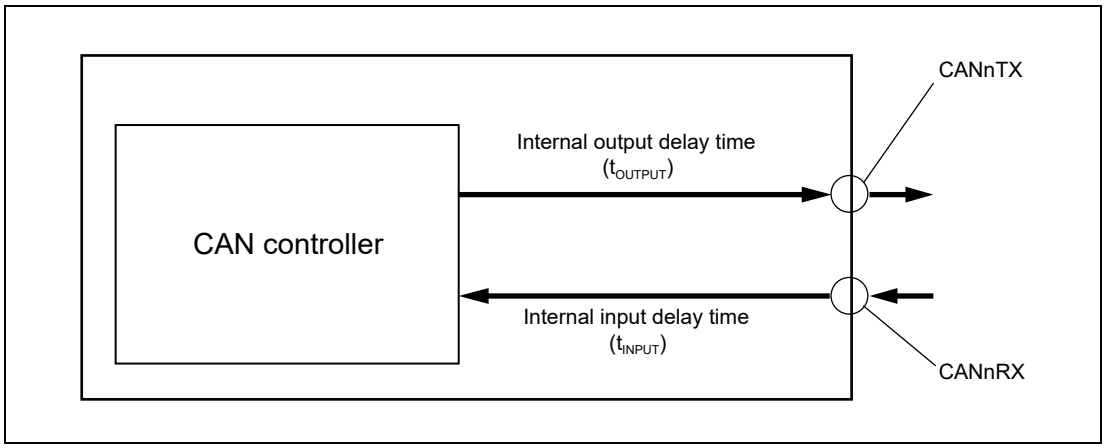


Figure 3.39 RS-CANFD Timing

3.3.15 FlexRay Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- CL =25 pF
- Buffer type = Sch1

Table 3.58 FlexRay Timing*1

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Transfer rate	r_{FLXA}				10	Mbps

Note 1. Base of this specification is “FlexRay Electrical Physical Layer Specification V3.0.1, Oct-2010”

3.3.16 RSENT Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- Drive strength = 4
- Buffer type = Sch1

Table 3.59 RSENT Timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Tick Time			1		90	µs

3.3.17 Renesas High-speed Serial I/F Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- HSIF0_REFCLK: CL = 15 pF
- Buffer type = Sch1
- E0VCC = 5.0 ± 0.5 V or 3.3V ± 0.3 V

Table 3.60 External Reference Clock Input/Output Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
External Reference Clock Input frequency	f_{REFCKI}		10		20	MHz
External Reference Clock Input duty cycle	DCREFCKI		35		65	%
External Reference Clock output frequency	f_{REFCKO}		10		20	MHz
External Reference Clock output duty cycle	DCREFCKO		35		65	%

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- HSIF0_REFCLK: CL = 15 pF
- E0VCC = 5.0 ± 0.5 V or 3.3V ± 0.3 V
- HSIF0_TXDP, HSIF0_TXDN: CL = 5.0 pF

Table 3.61 RHSIF Transmit Data Timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Transmit data cycle	f_{TX}	Slow mode			5	M Baud
		Fast mode			320	M Baud
Transmit data delay time (HSIF0_REFCLK input)	$t_{REFITXDD}$	Slow mode	0		60	ns
		Fast mode*1				ns
Transmit data delay time (HSIF0_REFCLK output)	$t_{REFOTXDD}$	Slow mode RHSIFnREFCLK 20MHz	–20		20	ns
		Slow mode RHSIFnREFCLK 10MHz	15		85	ns
		Fast mode*1				ns

Note 1. Asynchronous

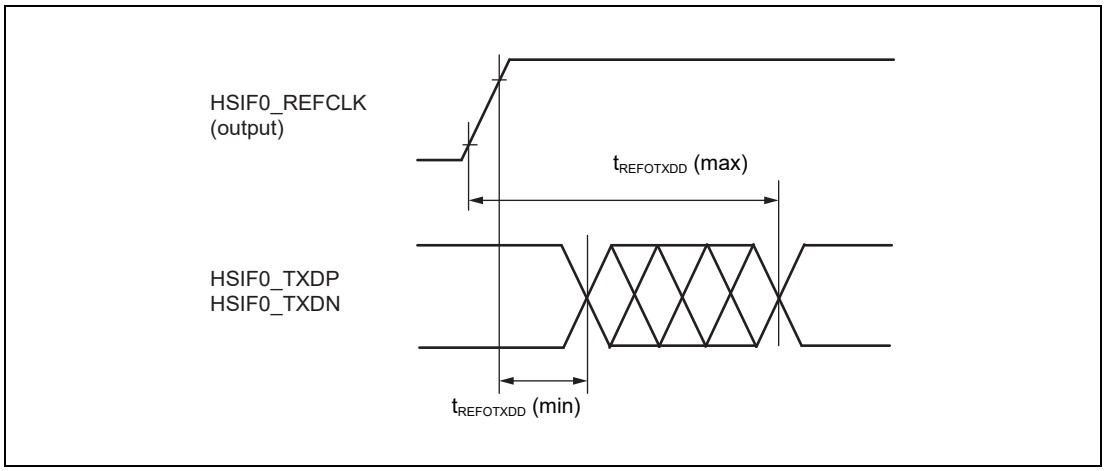


Figure 3.40 RHSIF Transmit Data Timing (HSIF0_REFCLK: output)

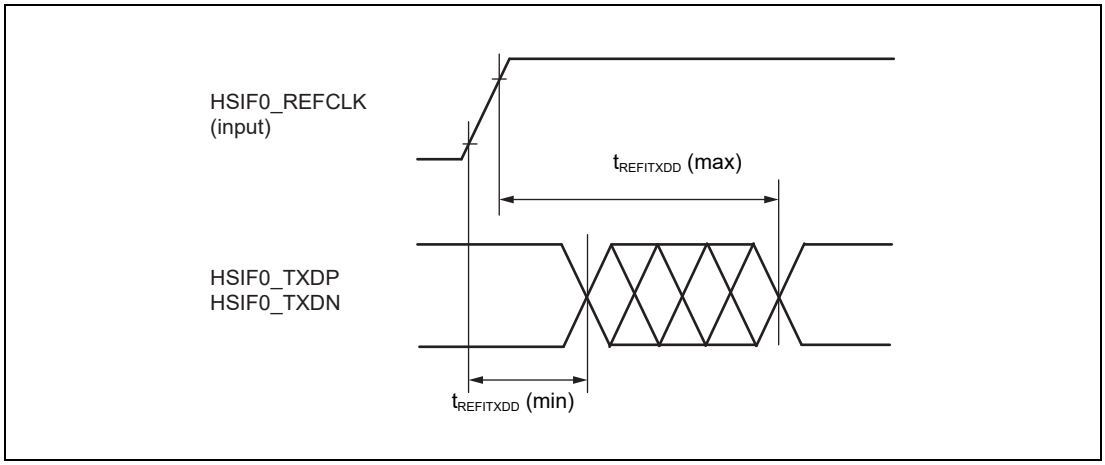


Figure 3.41 RHSIF Transmit Data Timing (HSIF0_REFCLK: input)

Table 3.62 RHSIF Receipt Data Timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Receipt data cycle	f_{RX}	Slow mode			5	M Baud
		Fast mode			320	M Baud

3.3.18 CXPI Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- Drive strength = 4
- Buffer type = Sch1

Table 3.63 CXPI Timing (CXPI-PWM Mode, Master node)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
CXPI transfer rate	r_{CXPI}				20	kbps
CXPI cycle time	Tbit		50			µs
Required loop back delay time (from CXP1nTX to CXP1nRX)	t_{pwm_loop}				0.05 × Tbit	µs

Table 3.64 CXPI Timing (CXPI-PWM Mode, Slave node)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
CXPI transfer rate	r_{CXPI}				20	kbps
CXPI cycle time	Tbit		50			µs
CXP1nTX output delay time (from CXP1nRX)	$t_{tx\_0\_pd}$		4 × t_{PCLK} *1		511 × t_{PCLK} + 4 × t_{PCLK} + 0.1 *1,*2	µs
Required loop back delay time (from CXP1nTX to CXP1nRX)	t_{pwm_loop}				0.05 × Tbit	µs

Note 1. t_{PCLK} is period of CLK_HSB

Note 2. "511 × t_{PCLK}" means maximum surge noise filter time. For details, see RH850/U2A-EVA Group User's Manual: Hardware **Section 30.4.1.6, CXP1nFIL — CXPI Input Filter Setting Register**

Table 3.65 CXPI Timing (CXPI-NRZ Mode, Master or Slave node)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
CXPI transfer rate	r_{CXPI}				20	kbps
CXPI cycle time	Tbit		50			µs
Required loop back delay time (from CXP1nTX to CXP1nRX)	t_{nrz_loop}		1 × Tbit		4 × Tbit	µs

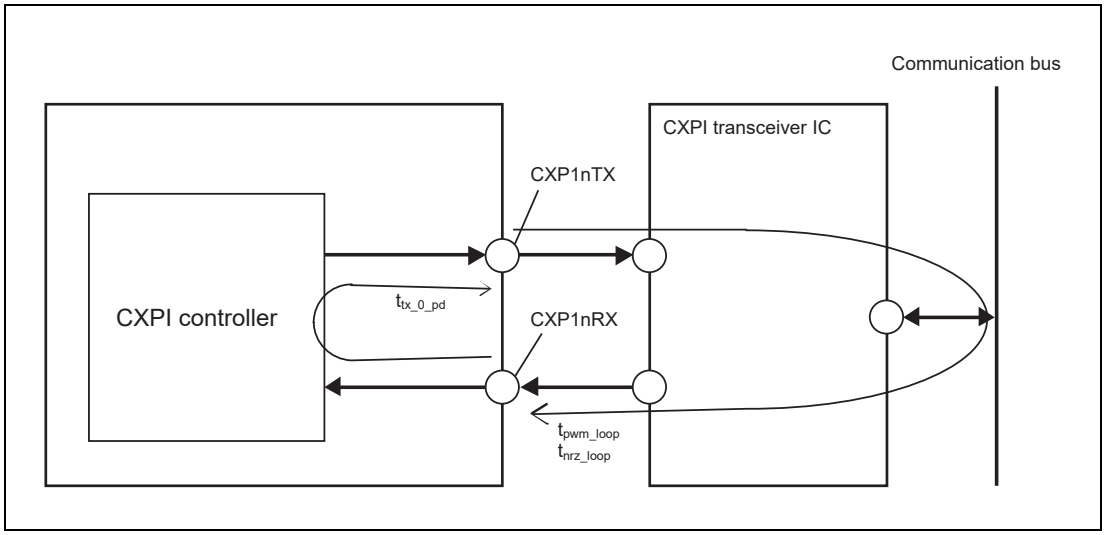


Figure 3.42 CXPI Block Diagram and Timing Path

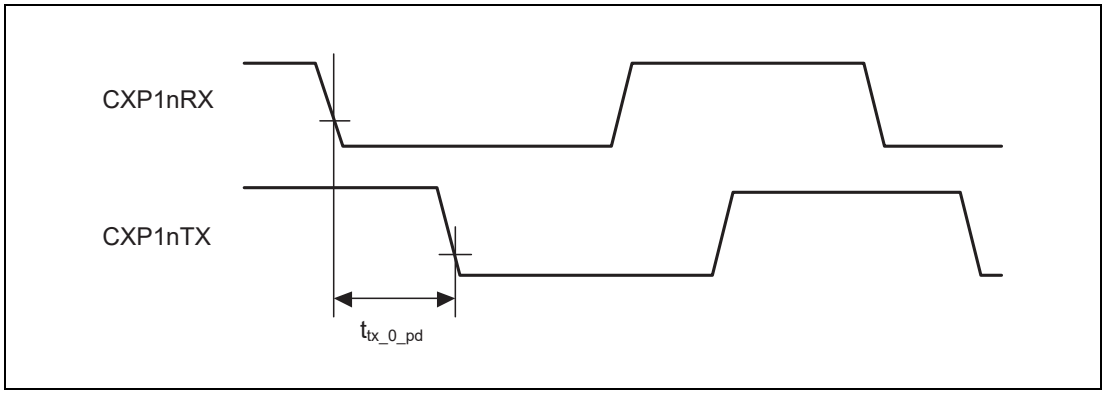


Figure 3.43 $t_{tx\_0\_pd}$ Waveform in CXPI PWM Mode

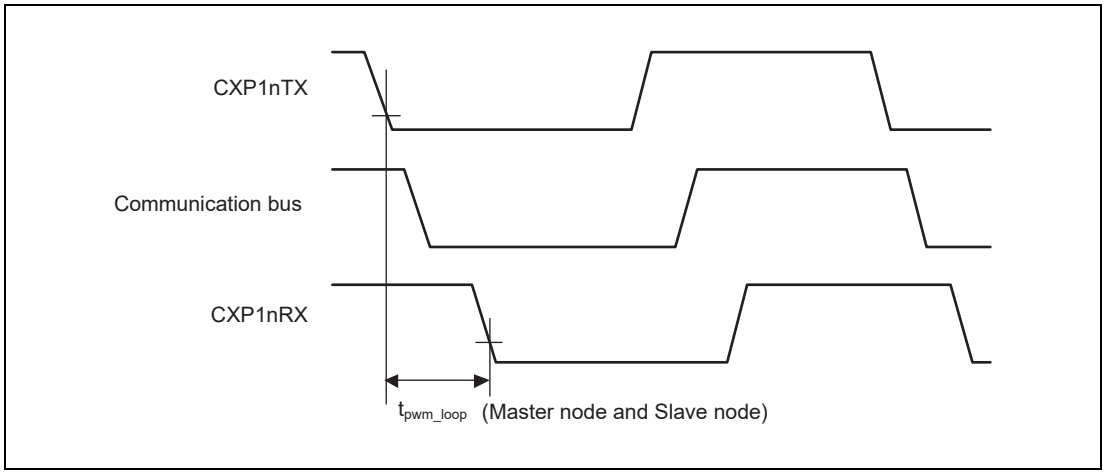


Figure 3.44 t_{pwm_loop} Waveform in CXPI PWM Mode

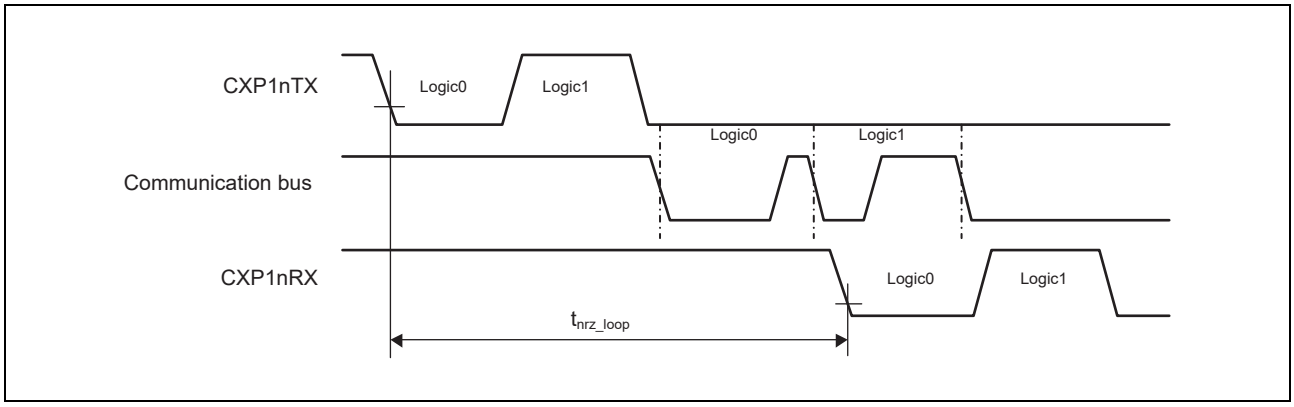


Figure 3.45 t_{nrz_loop} Waveform in CXPI NRZ Mode

3.3.19 Ethernet Timing

3.3.19.1 MII Characteristics

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- CL = 15 pF
- Buffer type = TTL

Table 3.66 Ethernet Timing – 10 Mbit/s MII Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
ETNBnTXCLK width	t_{MTC}		400 – 100 ppm	400	400 + 100 ppm	ns
ETNBnTXCLK high width	t_{MTCH}	*1	140	200	260	ns
ETNBnTXCLK low width	t_{MTCL}	*1	140	200	260	ns
ETNBnTXD [3:0] delay time	t_{MTXD}		0		25	ns
ETNBnTXEN delay time	t_{MTXE}		0		25	ns
ETNBnRXCLK width	t_{MRC}		400 – 100 ppm	400	400 + 100 ppm	ns
ETNBnRXCLK high width	t_{MRCH}	*1	140	200	260	ns
ETNBnRXCLK low width	t_{MRCL}	*1	140	200	260	ns
ETNBnRXD [3:0] setup time	t_{MRXDS}		10			ns
ETNBnRXD [3:0] hold time	t_{MRXDH}		10			ns
ETNBnRXDV, ETNBnRXER setup time	t_{MRDES}		10			ns
ETNBnRXDV, ETNBnRXER hold time	t_{MRDEH}		10			ns
ETNBnWOL delay time	t_{MWOL}		1		30	ns

Note 1. The duty cycle of ETNBnTXCLK and ETNBnRXCLK shall be between 35 to 65% (IEEE802.3).

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- Cload = 15 pF
- Drive strength = 2
- Buffer type = TTL

Table 3.67 Ethernet Timing – 100 Mbit/s MII Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
ETNBnTXCLK width	t_{MTC}		40 – 100 ppm	40	40 + 100 ppm	ns
ETNBnTXCLK high width	t_{MTCH}	*1	14	20	26	ns
ETNBnTXCLK low width	t_{MTCL}	*1	14	20	26	ns
ETNBnTXD [3:0] delay time	t_{MTXD}		0		25	ns
ETNBnTXEN delay time	t_{MTXE}		0		25	ns
ETNBnRXCLK width	t_{MRC}		40 – 100 ppm	40	40 + 100 ppm	ns
ETNBnRXCLK high width	t_{MRCH}	*1	14	20	26	ns
ETNBnRXCLK low width	t_{MRCL}	*1	14	20	26	ns
ETNBnRXD [3:0] setup time	t_{MRXDS}		10			ns
ETNBnRXD [3:0] hold time	t_{MRXDH}		10			ns
ETNBnRXDV, ETNBnRXER setup time	t_{MRDES}		10			ns
ETNBnRXDV, ETNBnRXER hold time	t_{MRDEH}		10			ns
ETNBnWOL delay time	t_{MWOL}		1		30	ns

Note 1. The duty cycle of ETNBnTXCLK and ETNBnRXCLK shall be between 35 to 65% (IEEE802.3).

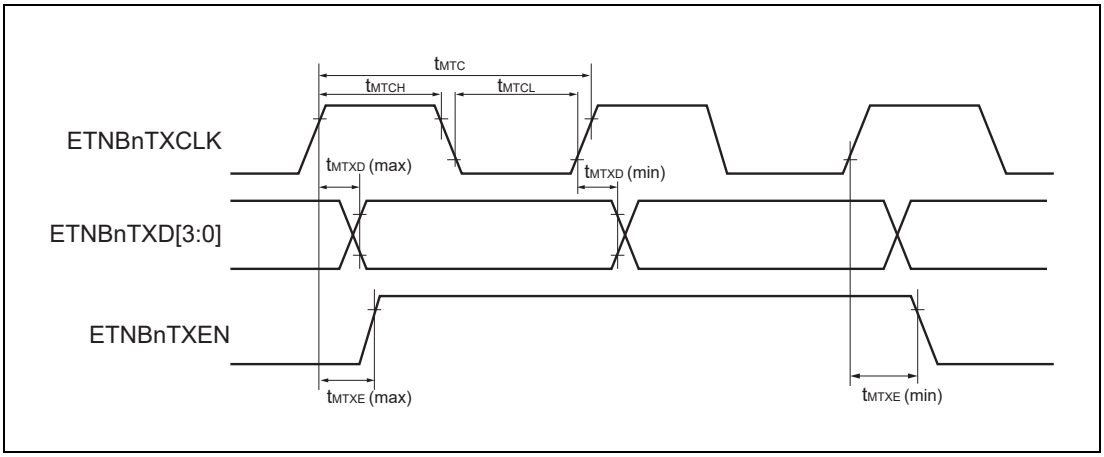


Figure 3.46 Ethernet Timing – MII Transmitter

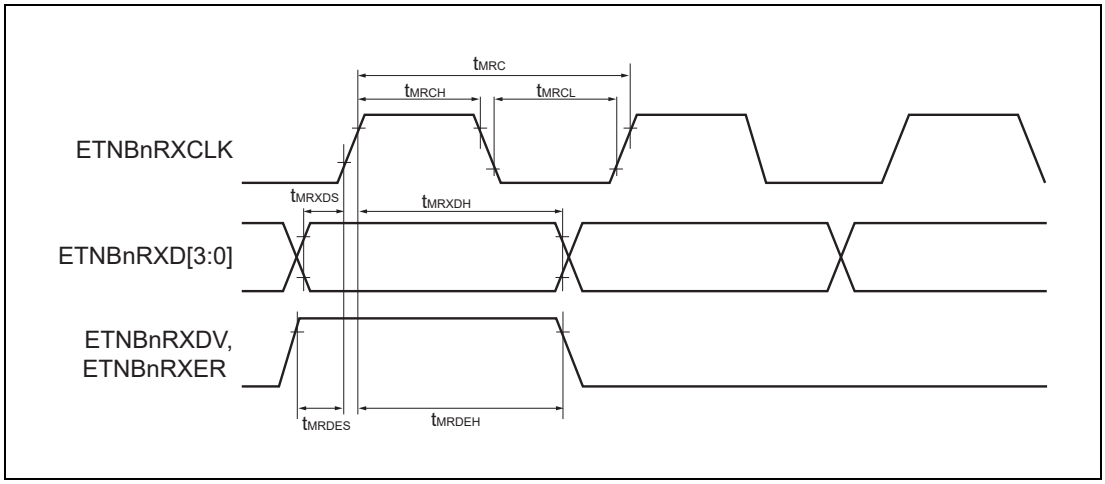


Figure 3.47 Ether net Timing – MII Receiver

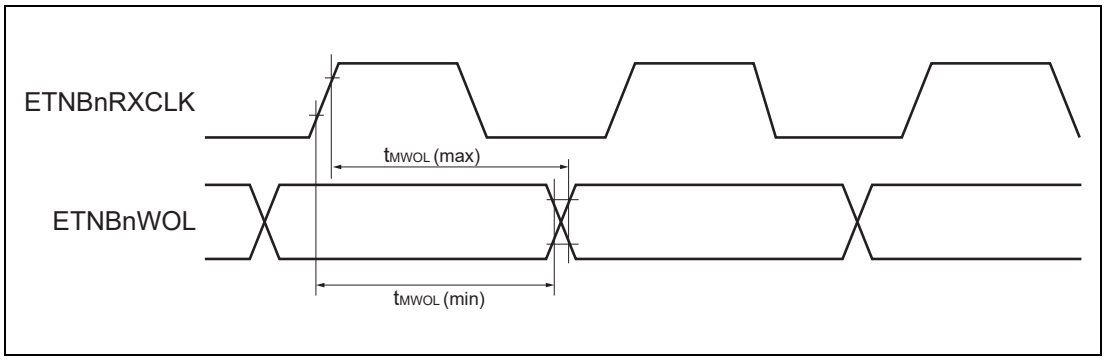


Figure 3.48 Ethernet Timing – MII WOL

3.3.19.2 RMII Characteristics

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- CL = 15 pF
- Drive strength = 2
- Buffer type = TTL

Table 3.68 Ethernet Timing – RMII Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
ETNB0REF50CK width	t_{RMC}		20 – 50 ppm	20	20 + 50 ppm	ns
ETNB0REF50CK high width	t_{RMCH}	*1	7		13	ns
ETNB0REF50CK low width	t_{RMCL}	*1	7		13	ns
ETNB0RXD [1:0], ETNB0CRS _DV and ETNB0RXER setup time	t_{RMS}		4			ns
ETNB0RXD [1:0], ETNB0CRS_DV and ETNB0RXER hold time	t_{RMH}		2			ns
ETNB0TXD [1:0], ETNB0TXEN output delay time	t_{RMD}		2		16	ns
ETNB0WOL delay time	t_{RMWOL}		1		30	ns

Note 1. The duty cycle of ETNB0REF50CK shall be between 35 to 65% (RMII™ specification).

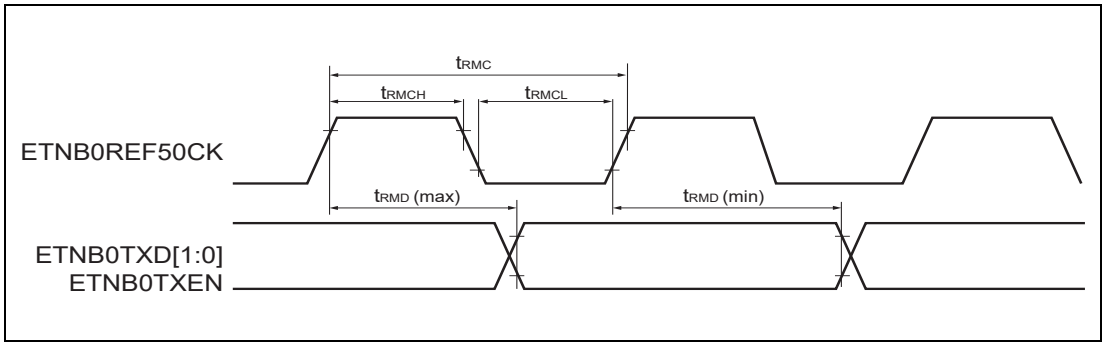


Figure 3.49 Ethernet Timing – RMII Transmitter

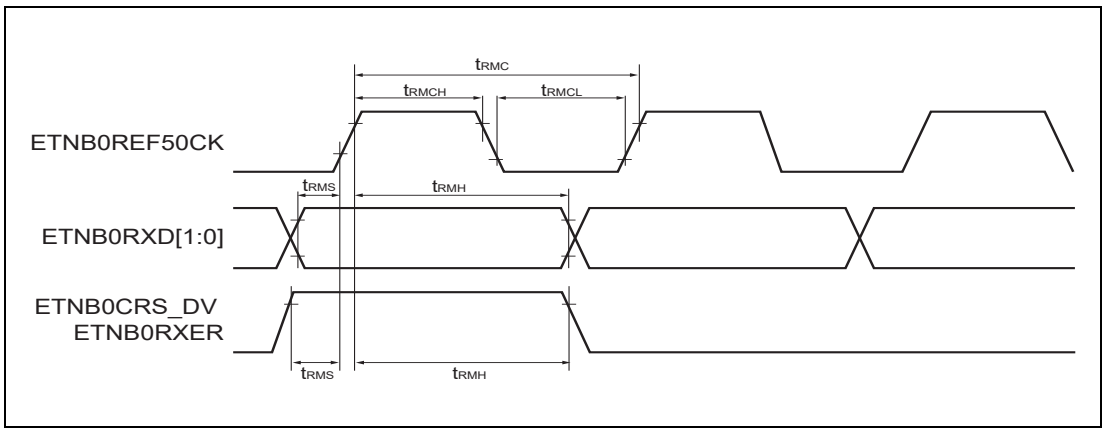


Figure 3.50 Ethernet Timing – RMII Receiver

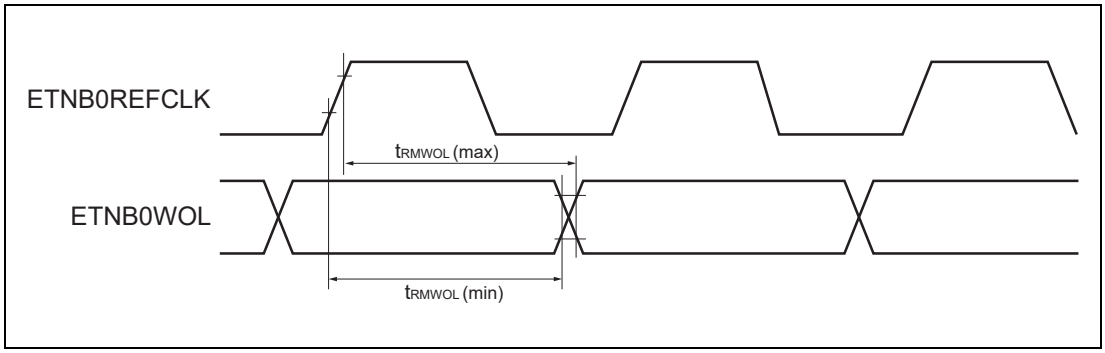


Figure 3.51 Ethernet Timing – RMII WOL

3.3.19.3 SGMII Characteristics

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.69 Ethernet Timing – SGMII REFCK Characteristics

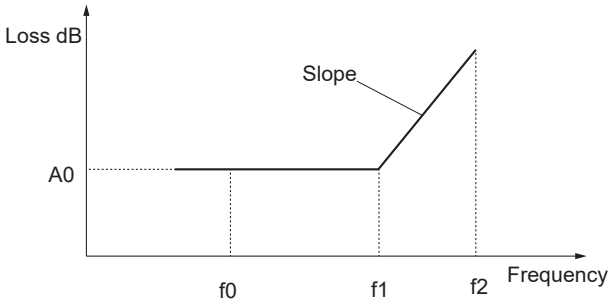
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock input frequency	t_{CIF}		40 – 100ppm		40 + 100 ppm	ns
Clock input duty cycle	t_{CIDC}		45		55	%
Clock input rising/falling time (20%-80%)	t_{CIRFT}				3	ns
Clock Input Total jitter (Dj+ 14* rms Random jitter)	t_{CITJ}				73*1	ps peak to peak

Note 1. 12 kHz to 20 MHz rms jittrer = 3 ps.

Table 3.70 Ethernet Timing – SGMII Tx buffer Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Signaling speed	t_{SS}		1.25 – 100 ppm		1.25 + 100 ppm	GBd
Total output jitter (Dj+14*rms random jitter)	t_{TOJ}				300	ps peak to peak
VOD rise/fall time (20% - 80%)	t_{VRFT}		60		250	ps
Differential output return loss (min)	DORL				*1	dB

Note 1. See the **Figure 3.52, Differential output return loss** for details of differential output return loss.



Parameter value		Unit
A0	-8	dB
f0	50	MHz
f1	0.625	GHz
f2	1.25	GHz
Slope	10	dB/dec

Figure 3.52 Differential output return loss

Table 3.71 Ethernet Timing – SGMII Rx buffer Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Signaling speed	t_{SS}		1.25 – 100 ppm		1.25 + 100 ppm	GBd
Total input jitter tolerance*2 (Dj+14*rms random jitter)	t_{TIJT}				400	ps peak to peak
setup/hold time*1, *3	t_{SHT}		120			ps

Note 1. Measured at 50% of the transition

Note 2. Only supported by RH850/U2A

Note 3. Only supported by RH850/U2A-EVA

Table 3.72 Ethernet Timing – Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
SGMII power stabilization time	t_{SPST}				1.2	ms

3.3.19.4 Management Interface

Timing of management interface (ETNBnMDC and ETNBnMDIO) depends on software. It is necessary to adjust wait time according to AC specification of PHY.

3.3.20 PSI5 Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- Drive strength = 4

Table 3.73 PSI5 Timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Bit time		125 kbps (Low speed)	7.6	8.0	8.4	µs
		189 kbps (High speed)	5.0	5.3	5.6	µs
		250 kbps (PAS compatibility)	3.8	4.0	4.2	µs
Gap time		125 kbps (Low speed)	8.4			µs
		189 kbps (High speed)	5.6			µs
		250 kbps (PAS compatibility)	2.0			µs

3.3.21 PSI5-S Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.74 PSI5-S Timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
PSI5-S transfer rate	r_{PSI5S1}	PSI5-S mode			5.33	Mbps
	r_{PSI5S2}	UART mode			5.33	Mbps
Output clock cycle	$t_{PSIScyc}$	PSI5-S mode	37.5			ns
Output clock pulse width	$t_{PSISCKW}$	PSI5-S mode	0.3 x $t_{PSIScyc}$		0.5 x $t_{PSIScyc}$	ns

3.3.22 Timer Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.75 Timer Input Timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
TAUDnIm input high level width	t_{WTDIH}		(S + 1) x 1/fs*1			ns
TAUDnIm input low level width	t_{WTDIL}		(S + 1) x 1/fs*1			ns
TAUDnIm pulse rejection width*2	t_{WTDRJ}		(S – 1) x 1/fs*1		(S + 1) x 1/fs*1	ns
TAUJnIm input high level width	t_{WTJIH}	Analog noise filter	600*3			ns
		Digital noise filter	(S + 1) x 1/fs*1			ns
TAUJnIm input low level width	t_{WTJIL}	Analog noise filter	600*3			ns
		Digital noise filter	(S + 1) x 1/fs*1			ns
TAUJnIm pulse rejection width*2	t_{WTJRJ}	Analog noise filter	100		600*3	ns
		Digital noise filter	(S – 1) x 1/fs*1		(S + 1) x 1/fs*1	ns
TAPAnESO input high level width*4	t_{WTPIH}	Analog noise filter	600			ns
		Digital noise filter	(S + 1) x 1/fs*1			ns
TAPAnESO input low level width*4	t_{WTPIL}	Analog noise filter	600			ns
		Digital noise filter	(S + 1) x 1/fs*1			ns
TAPAnESO pulse rejection width*2, *4	t_{WTPRJ}	Analog noise filter	100		600	ns
		Digital noise filter	(S – 1) x 1/fs*1		(S + 1) x 1/fs*1	ns
ENCAnTINm input high level width	t_{WENIH}		(S + 1) x 1/fs*1			ns
ENCAnTINm input low level width	t_{WENIL}		(S + 1) x 1/fs*1			ns
ENCAnTINm pulse rejection width*2	t_{WENRJ}		(S – 1) x 1/fs*1		(S + 1) x 1/fs*1	ns
TSG3nPTSIm/ENCAnEx, TSG3nCLKI high level width	t_{WTGIH}		(S + 1) x 1/fs*1			ns
TSG3nPTSIm/ENCAnEx, TSG3nCLKI low level width	t_{WTGIL}		(S + 1) x 1/fs*1			ns
TSG3nPTSIm/ENCAnEx, TSG3nCLKI pulse rejection width*2	t_{WTGRJ}		(S – 1) x 1/fs*1		(S + 1) x 1/fs*1	ns

Note 1. S: Number of sampling times
fs: The value given by the following formula

$$fs = \frac{f_{DNFCK}}{PRS}$$

f_{DNFCK}: frequency of CLKA_TAUJ (for TAUJ2 and TAUJ3), CLK_HSB (others)
PRS: 1, 2, 4, 8, … , 128

Note 2. Input pulse shorter than the given min. value will be filtered out. Input pulses between min. and max. value result in an undefined signal condition (i.e. pulses might be filtered or not.
This characteristic is not tested in production.

Note 3. When CLK_LSIOSC is selected by CLKA_TAUJ register, at least one clock period of CLK_LSIOSC (4.6 µs) is required for activation of input signal for that domain. Any input pulses with less than 4.6 µs width may be rejected.

Note 4. By-pass of filter is possible. For details, see RH850/U2A-EVA Group User's Manual: Hardware **Section 2.7.2.10, ANF/DNF Type F1**.

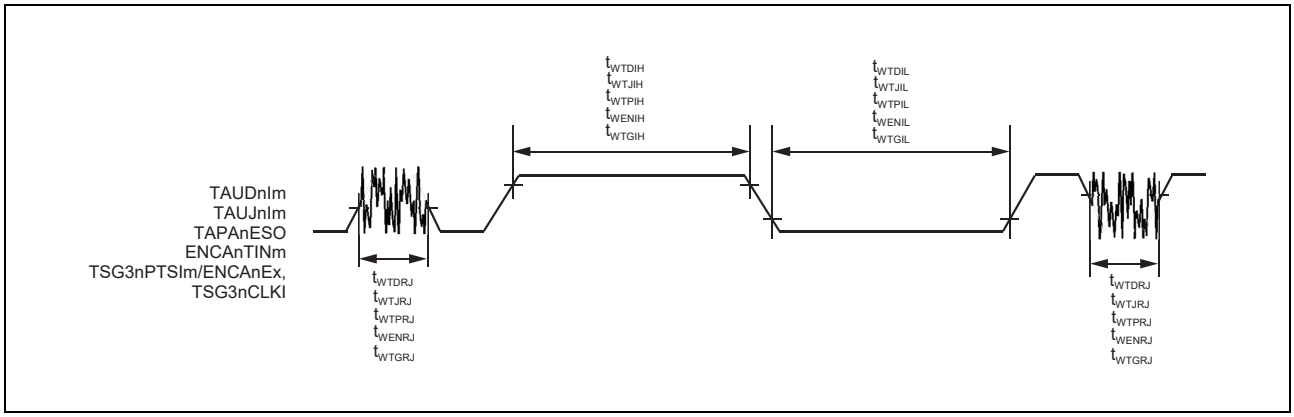


Figure 3.53 Timer Input Timing

3.3.23 GTM Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.76 GTM Timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
GTM input high level width	t_{WGTIH}		4 × Tsamp*1			ns
GTM input low level width	t_{WGTIL}		4 × Tsamp*1			ns
GTM output cycle time	t_{CYGTO}		4 × Tsamp*1			ns
GTMECLKn output cycle	$t_{CYGTECLK}$		8 × Tsamp*1			ns
GTMECLKn output high level width	t_{WGTOH}		4 × Tsamp*1 – 10			ns
GTMECLKn output low level width	t_{WGTOL}		4 × Tsamp*1 – 10			ns

Note 1. Tsamp = $1/f_{CLK\_UHSB}$

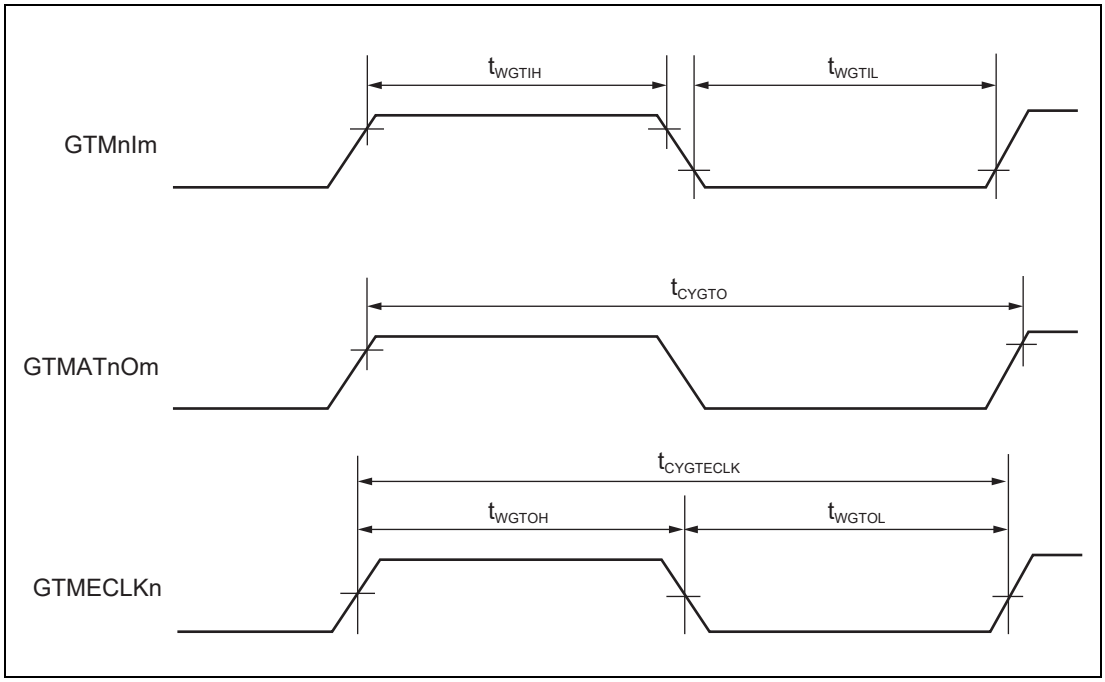


Figure 3.54 GTM Timing

3.3.24 Emergency shut-Off (ESO) Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.77 ESO Timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
GTMATnOx Hi-z delay time	t_{DESO}				50	ns

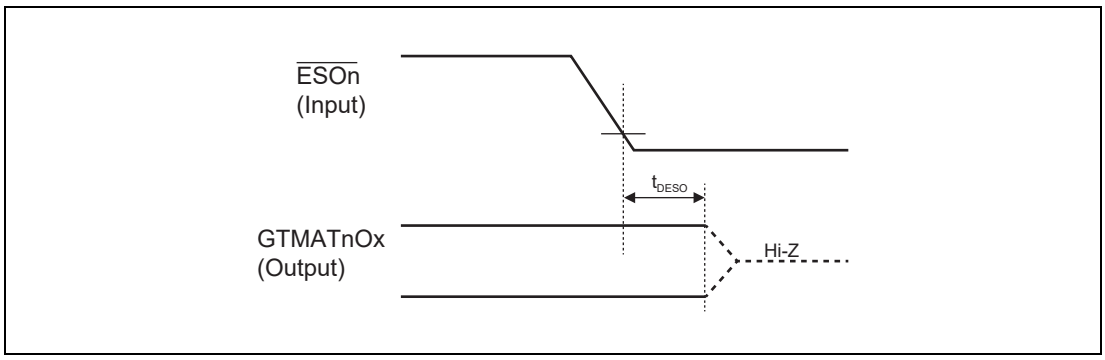


Figure 3.55 ESO Timing

3.3.25 Debug Reset Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.78 Debug Reset Timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
$\overline{\text{TRST}}$ input low level width	t_{WTRL}		600			ns
$\overline{\text{TRST}}$ pulse rejection*1	t_{WTRRJ}		100		600	ns
$\overline{\text{AURORES1}}$, $\overline{\text{AURORES2}}$, $\overline{\text{AURORESPD}}$ input low level width	t_{WARSL}		600			ns
$\overline{\text{AURORES1}}$, $\overline{\text{AURORES2}}$, $\overline{\text{AURORESPD}}$ pulse rejection width*1	t_{WARRJ}		100		600	ns
$\overline{\text{ERAMRESPD}}$, $\overline{\text{ERAMRES2}}$ input low level width	t_{WERSL}		600			ns
$\overline{\text{ERAMRESPD}}$, $\overline{\text{ERAMRES2}}$ pulse rejection width*1	t_{WERRJ}		100		600	ns

Note 1. Input pulses shorter than the given min. value will be filtered out (resulting in no interrupt detected). Input pulses between min. and max. value result in an undefined interrupt signal condition (i.e. pulses might be filtered out or not).

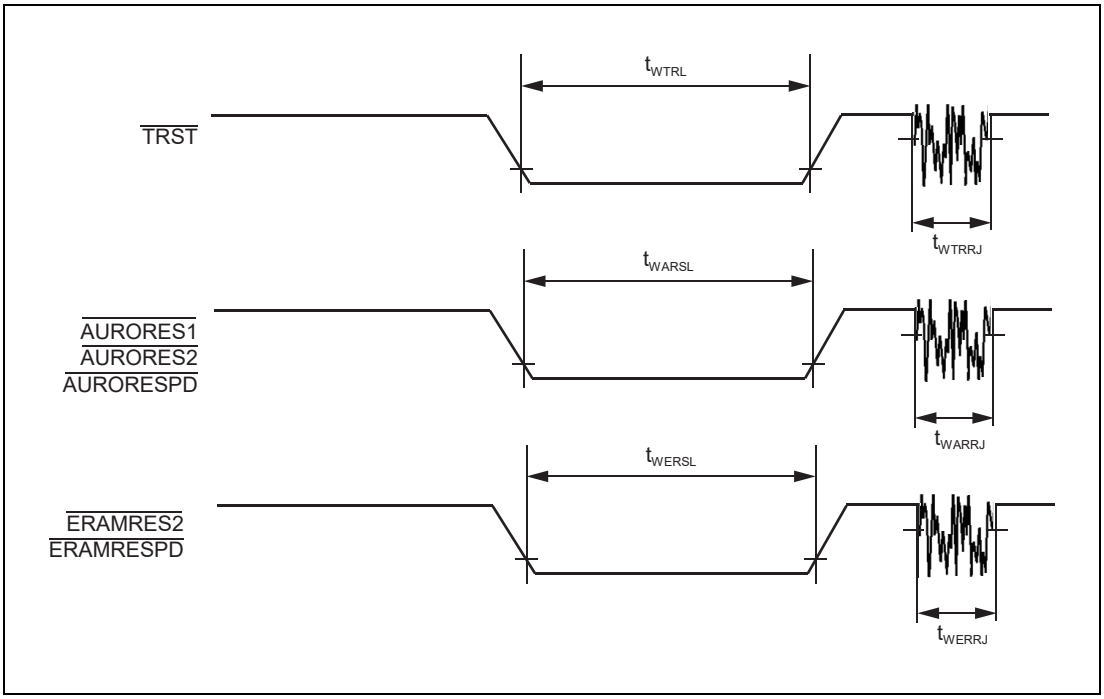


Figure 3.56 Debug Reset Timing

3.3.26 Nexus Interface Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- Buffer type = TTL

Table 3.79 Nexus Interface Timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
TCK Cycle width	t_{TCKW}		50			ns
TCK high level width	t_{TCKWH}		21			ns
TCK low level width	t_{TCKWL}		21			ns
TMS/TDI setup time	t_{TISU}		6			ns
TMS/TDI hold time	t_{TIH}		6			ns
TDO output delay time	t_{TDOD}				17	ns
$\overline{RDY}$ delay time	t_{RDYD}				17	ns
TCK/$\overline{TRST}$/TMS/TDI input rising time	t_{TIR}				4	ns
TCK/$\overline{TRST}$/TMS/TDI input falling time	t_{TIF}				4	ns

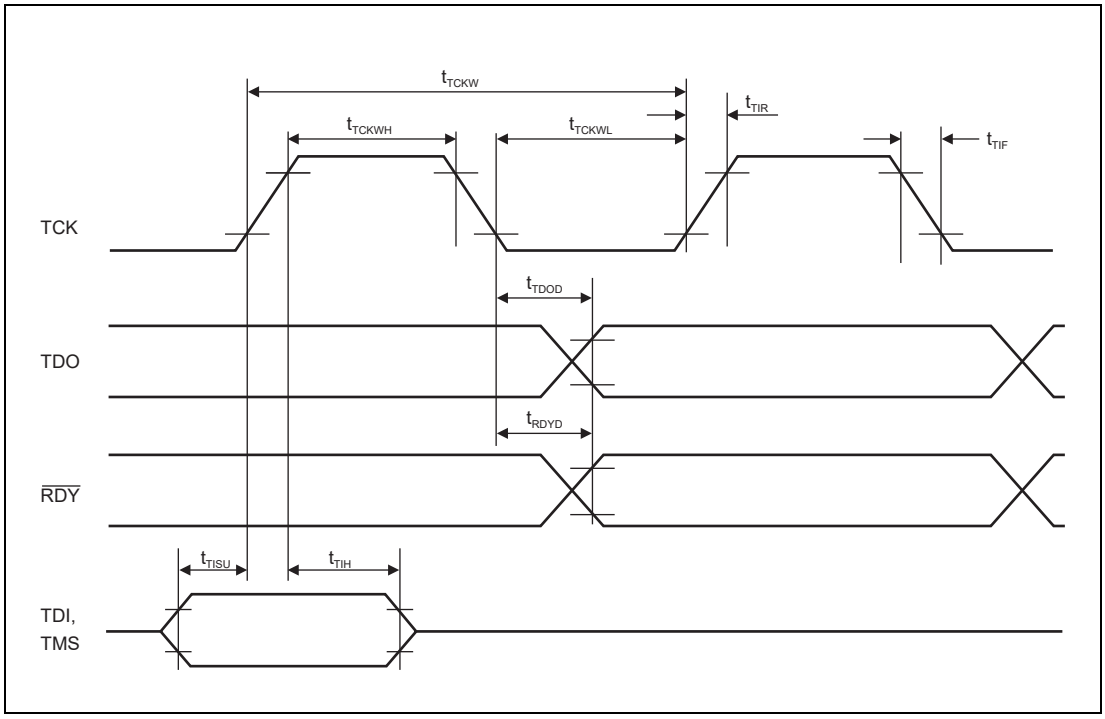


Figure 3.57 Nexus Interface Timing

3.3.27 LPD (4pin) Interface Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.80 LPD (4pin) Interface Timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
LPDCLK cycle time	$t_{LPDCKCYC}$		25			ns
LPDCLK high/low level width	t_{LPDCKW}		4.5			ns
LPDCLK input rising/falling time	$t_{LPDCKRF}$				8	ns
LPDI setup time	t_{LPDSU}		3			ns
LPDI hold time	t_{LPDH}		3			ns
LPDCLKO cycle time	$t_{LPDCKOCYC}$		25			ns
LPDCLKO high/low level width	$t_{LPDCKOW}$		t_{LPDCKW} - 2			ns
LPDCLK to LPDCLKO delay time	$t_{LPDCKOD}$				44	ns
LPDO output delay	t_{LPDOD}		0		18	ns

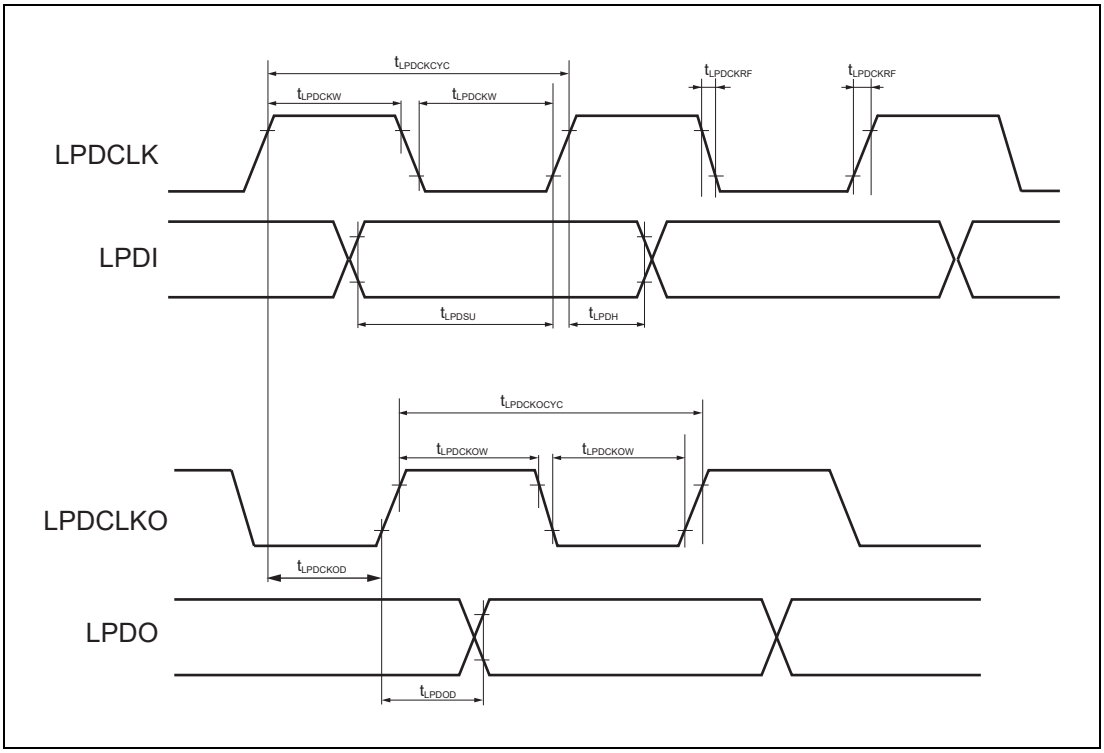


Figure 3.58 LPD (4pin) Interface Timing

3.3.28 AUDR Interface Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- CL = 10 pF
- Drive strength = 2
- Buffer type = SHMT1 ($\overline{\text{AUDRST}}$), TTL (Others)

Table 3.81 AUDR Interface Timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
AUDCK cycle time	$t_{AUCKcyc}$		20			ns
AUDCK high level width	t_{AUCKH}		0.4 x $t_{AUCKcyc}$			ns
AUDCK low level width	t_{AUCKL}		0.4 x $t_{AUCKcyc}$			ns
$\overline{\text{AUDRST}}$ setup time	t_{AURSTS}		12			ns
$\overline{\text{AUDRST}}$ pulse width	t_{AURSTW}		5 x $t_{AUCKcyc}$			ns
$\overline{\text{AUDSYNC}}$ setup time	t_{AUSYS}		10			ns
$\overline{\text{AUDSYNC}}$ hold time	t_{AUSYH}		5			ns
AUDATA input setup time	t_{AUDTS}		8			ns
AUDATA input hold time	t_{AUDTH}		5			ns
AUDATA output delay	t_{AUDTD}				$t_{AUCKcyc}$ – 3.4	ns

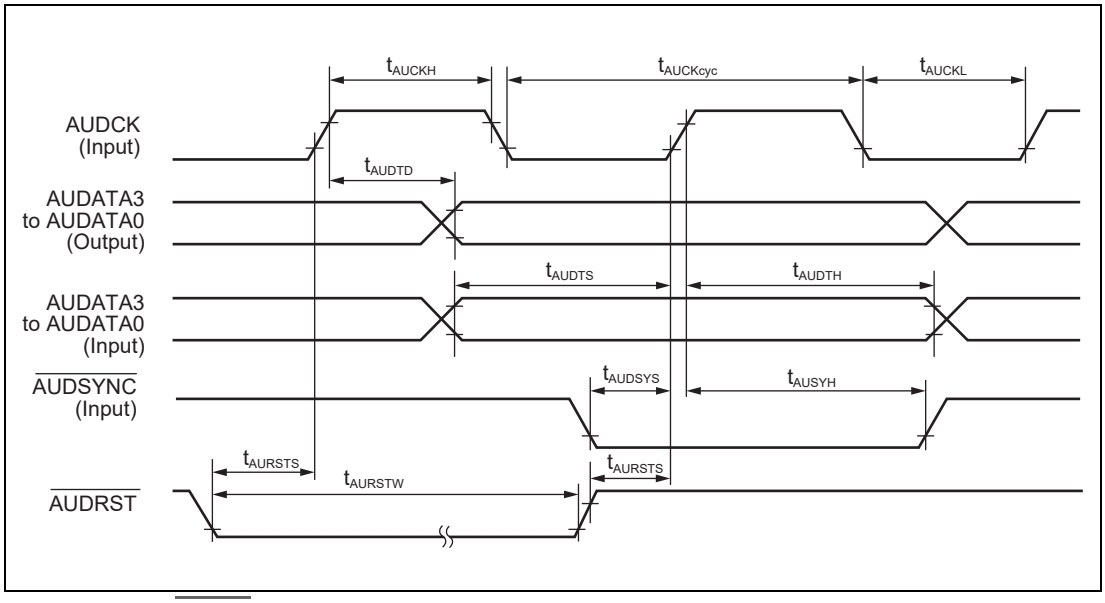


Figure 3.59 $\overline{\text{AUDR}}$ Interface Timing

3.3.29 Aurora Interface Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

3.3.29.1 Aurora Interface — 1.25 Gbps baud rate

Table 3.82 Aurora Interface Operating Condition – 1.25Gbps baud rate

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Rise/Fall Time	t_{AITRF}	*1	60			ps
Deterministic jitter	t_{AIDJ}				0.17	UI
Total jitter	t_{AITJ}				0.35	UI
Output skew	t_{AIOS}	*2			25	ps
Multiple output skew	t_{AIMOS}	*3			1000	ps
Unit interval	t_{AIUI}		800 - 100 ppm		800 +100 ppm	ps

Note 1. At driver output.
Note 2. Skew at transmitter output between the differential pair.
Note 3. Skew at transmitter output between lanes of a multi-lane channel.

3.3.29.2 Aurora Interface — 2.5 Gbps baud rate

Table 3.83 Aurora Interface Operating Condition – 2.5Gbps baud rate

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Rise/Fall Time	t_{AITRF}	*1	40			ps
Deterministic jitter	t_{AIDJ}				0.17	UI
Total jitter	t_{AITJ}				0.35	UI
Output skew	t_{AIOS}	*2			20	ps
Multiple output skew	t_{AIMOS}	*3			1000	ps
Unit interval	t_{AIUI}		400 - 100 ppm		400 + 100 ppm	ps

Note 1. At driver output.
Note 2. Skew at transmitter output between the differential pair.
Note 3. Skew at transmitter output between lanes of a multi-lane channel.

3.3.29.3 Aurora Interface — 3.125 Gbps baud rate

Table 3.84 Aurora Interface Operating Condition – 3.125Gbps baud rate

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Rise / Fall Time	t_{AITRF}	*1	30			ps
Deterministic jitter	t_{AIDJ}				0.17	UI
Total jitter	t_{AITJ}				0.35	UI
Output skew	t_{AIOS}	*2			15	ps
Multiple output skew	t_{AIMOS}	*3			1000	ps
Unit interval	t_{AIUI}		320 -100 ppm		320 + 100 ppm	ps

Note 1. At driver output.
Note 2. Skew at transmitter output between the differential pair.
Note 3. Skew at transmitter output between lanes of a multi-lane channel.

3.3.29.4 Aurora Interface — 5 Gbps baud rate

Table 3.85 Aurora Interface Operating Condition – 5Gbps baud rate

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Rise/Fall Time	t_{AITRF}	*1	30			ps
Deterministic jitter	t_{AIDJ}				0.25	UI
Total jitter	t_{AITJ}				0.35	UI
Output skew	t_{AIOS}	*2			15	ps
Multiple output skew	t_{AIMOS}	*3			1000	ps
Unit interval	t_{AIUI}		200 - 100 ppm		200 + 100 ppm	ps

Note 1. At driver output.
Note 2. Skew at transmitter output between the differential pair.
Note 3. Skew at transmitter output between lanes of a multi-lane channel.

3.3.29.5 Aurora Interface — 6.25 Gbps baud rate

Table 3.86 Aurora Interface Operating Condition – 6.25Gbps baud rate

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Rise / Fall Time	t_{AITRF}	*1	30			ps
Deterministic jitter	t_{AIDJ}				0.25	UI
Total jitter	t_{AITJ}				0.35	UI
Output skew	t_{AIOS}	*2			15	ps
Multiple output skew	t_{AIMOS}	*3			1000	ps
Unit interval	t_{AIUI}		160 - 100 ppm		160 +100 ppm	ps

Note 1. At driver output.
Note 2. Skew at transmitter output between the differential pair.
Note 3. Skew at transmitter output between lanes of a multi-lane channel.

3.3.29.6 Aurora Interface — Transmitter clock Timing

Table 3.87 Aurora Interface Transmitter clock timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Reference clock frequency	f_{AICLK}	1.25 Gbps baud rate		62.5		MHz
		2.5 Gbps baud rate		125		MHz
		3.125 Gbps baud rate		156.25		MHz
		5 Gbps baud rate		125		MHz
		6.25 Gbps baud rate		156.25		MHz
Reference clock rise time	t_{AICTR}			200	400	ps
Reference clock fall time	t_{AICTF}			200	400	ps
Reference clock duty cycle			45		55	%
Reference clock total jitter	t_{AICTJ}	*1			40*2	ps
Stability	$t_{AICSTAB}$				50	ppm

Note 1. Peak to peak.

Note 2. Phase noise of CICREF[P/N] should be below the line of **Figure 3.60**.

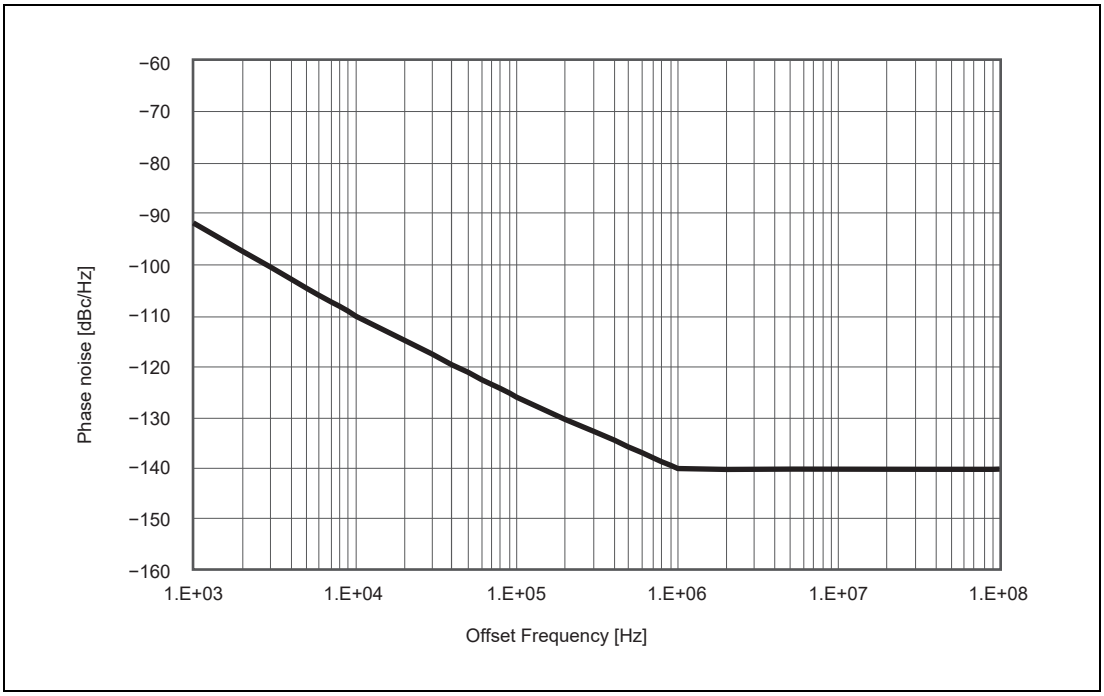


Figure 3.60 Phase noise of CICREF[P/N]

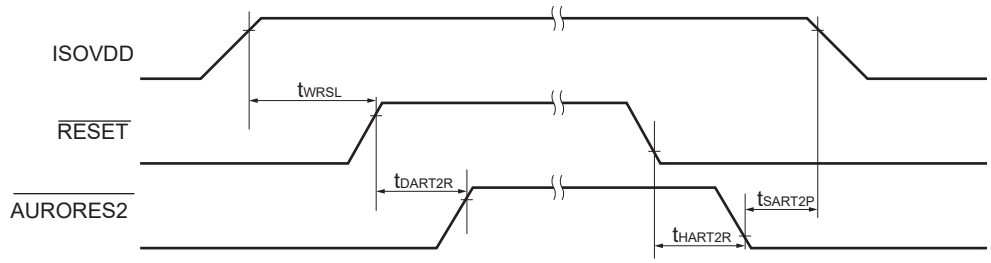
3.3.30 Debug Resource (Aurora, ERAM) Specific Reset Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

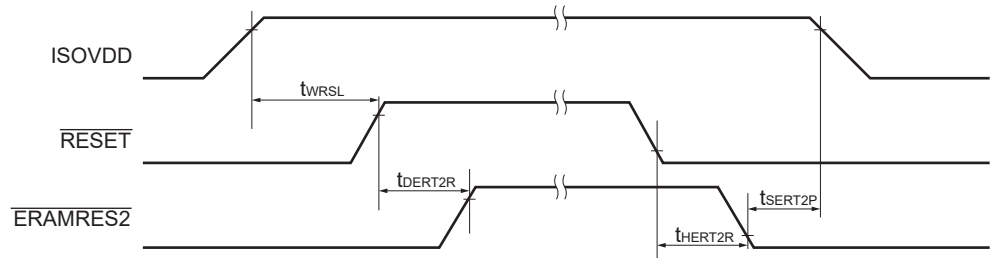
Table 3.88 Debug Resource (Aurora, ERAM) Specific Reset Timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
$\overline{\text{AURORES2}}$ release timing delay	t_{DART2R}		0		400	ns
$\overline{\text{AURORES2}}$ inactive hold time	t_{HART2R}		2.4			µs
$\overline{\text{AURORES2}}$ setup time	t_{SART2P}		2.4			µs
$\overline{\text{ERAMRES2}}$ release timing delay	t_{DERT2R}		0		400	ns
$\overline{\text{ERAMRES2}}$ inactive hold time	t_{HERT2R}		2.4			µs
$\overline{\text{ERAMRES2}}$ assert setup time	t_{SERT2P}		2.4			µs
$\overline{\text{AURORES1}}$, $\overline{\text{AURORESPD}}$ release timing delay	$t_{DART2AVD}$		2.4			µs
$\overline{\text{AURORES1}}$, $\overline{\text{AURORESPD}}$ inactive hold time	$t_{SART2AVD}$		2.4			µs
$\overline{\text{ERAMRESPD}}$ release timing delay	$t_{DERT2EVD}$		2.4			µs
$\overline{\text{ERAMRESPD}}$ inactive hold time	$t_{SERT2EVD}$		2.4			µs



Note: About the parameter t_{WRSL}, refer to "$\overline{\text{RESET}}$ input level width" in **Section 3.3.6.1, RESET Timing**

Figure 3.61 $\overline{\text{AURORES2}}$ AC Timing



Note: About the parameter t_{WRSL}, refer to "$\overline{\text{RESET}}$ input low level width" in **Section 3.3.6.1, RESET Timing**

Figure 3.62 $\overline{\text{ERAMRES2}}$ AC Timing

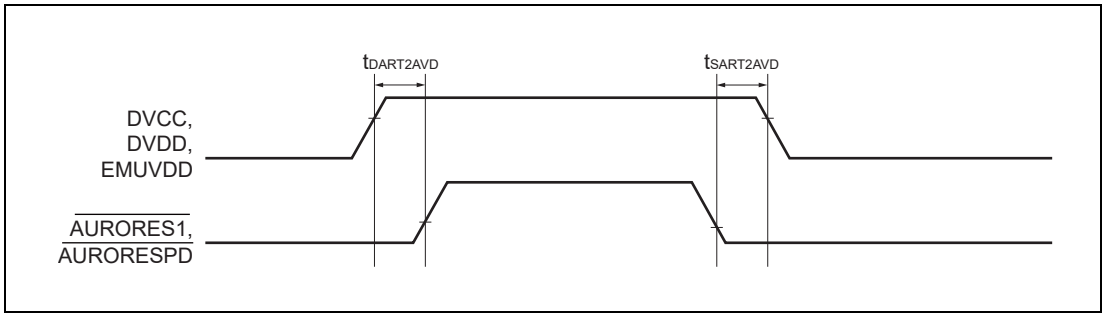


Figure 3.63 $\overline{\text{AURORES1}}$ and $\overline{\text{AURORESPD}}$ AC Timing

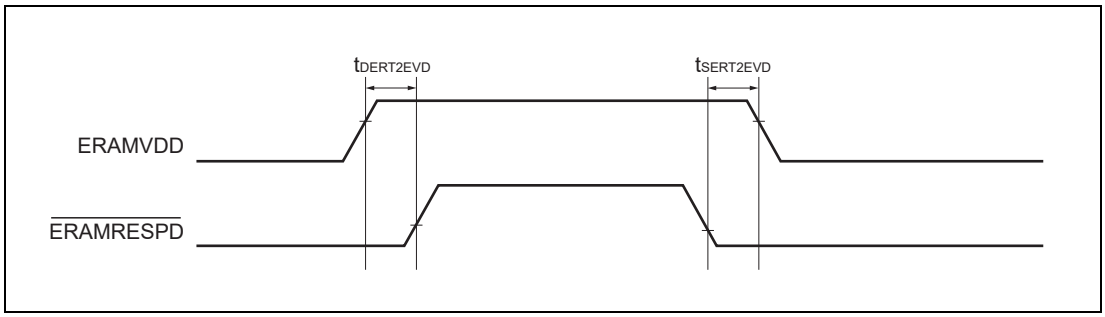


Figure 3.64 $\overline{\text{ERAMRESPD}}$ AC Timing

3.3.31 Debug Event Interface Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.89 Debug Event Interface Timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
$\overline{\text{EVTI}}$ input high level width	t_{WEVIH}	*1	2 ×t_{MCKW} *3			ns
		*2	2 ×t_{TCKW}			ns
$\overline{\text{EVTI}}$ input low level width	t_{WEVIL}	*1	2 ×t_{MCKW} *3			ns
		*2	2 ×t_{TCKW}			ns
$\overline{\text{EVTO}}$ output high level width	t_{WEVOH}		t_{MCKW} *3			ns
$\overline{\text{EVTO}}$ output low level width	t_{WEVOL}		t_{MCKW} *3			ns
$\overline{\text{MSYN}}$ input high level width	t_{WMSNH}		2 ×t_{MCKW} *3			ns
$\overline{\text{MSYN}}$ input low level width	t_{WMSNL}		2 ×t_{MCKW} *3			ns

Note 1. When used as event trigger.

Note 2. When used as break input.

Note 3. t_{MCKW} is the cycle of the clock (MCKO) obtained by dividing the CPU clock (CLK_CPU) and the value must be divided by 16 (default). For details, refer to the *RH850/U2A-EVA Group User's Manual: Emulation*.

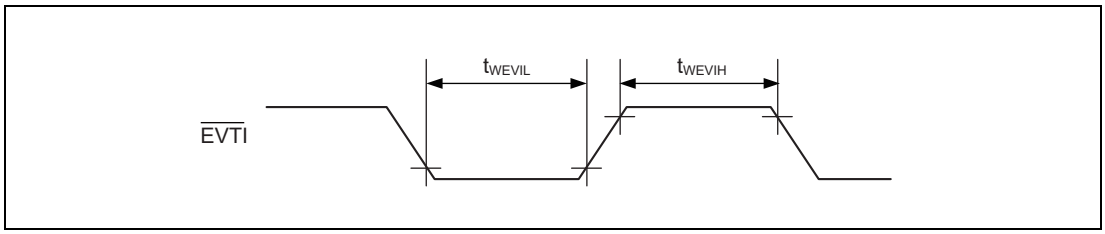


Figure 3.65 $\overline{\text{EVTI}}$ Timing

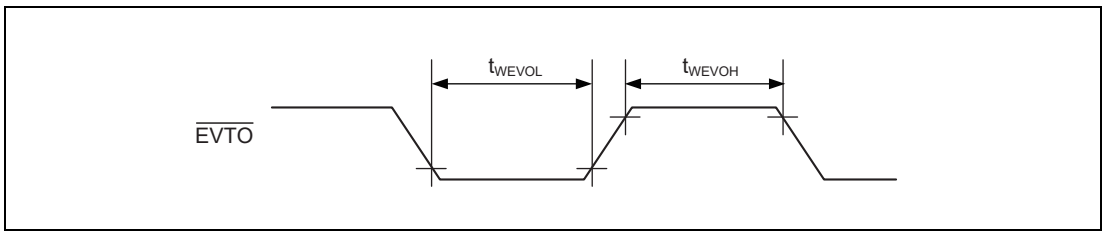


Figure 3.66 $\overline{\text{EVTO}}$ Timing

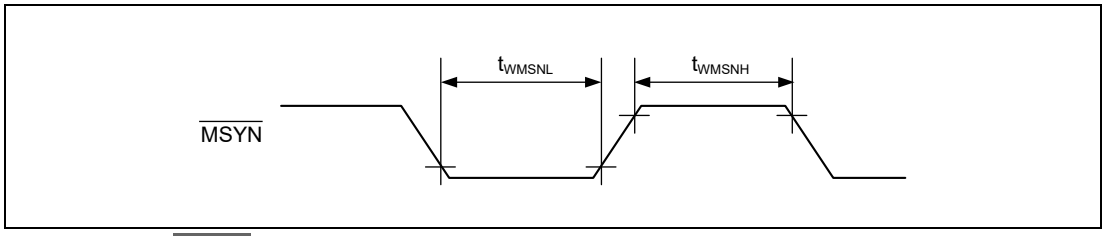


Figure 3.67 $\overline{\text{MSYN}}$ Timing

3.3.32 Debug Interface Mode Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.90 Debug Interface Mode Timing

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
TCK (JP0_2) input timing before $\overline{\text{TRST}}$	$t_{DBGIFSWCK}$		$10\times t_{LPDCKW}$ $10\times t_{TCKW}$			ns
TDI (JP0_0) setup time	$t_{DBGIFSWS}$		$10\times t_{LPDCKW}$ $10\times t_{TCKW}$			ns
TDI (JP0_0) hold time	$t_{DBGIFSWH}$		2			µs

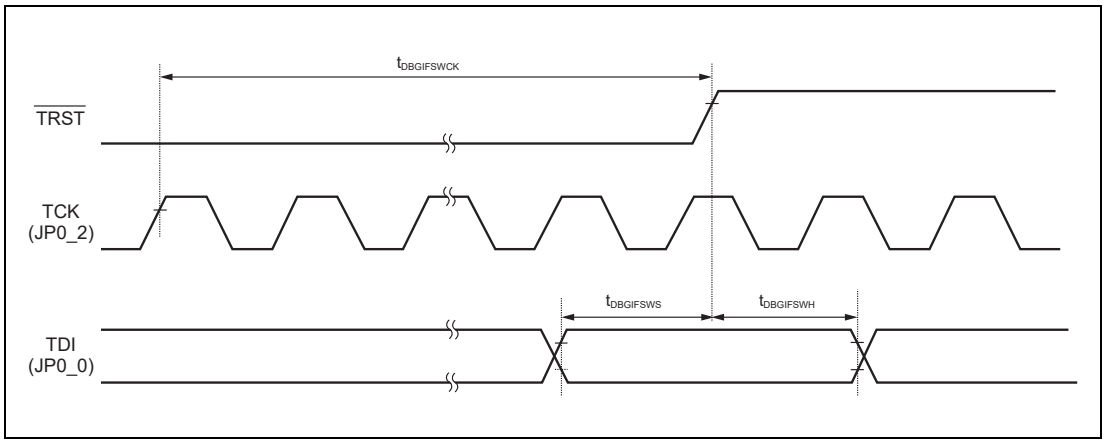


Figure 3.68 Debug Interface Mode Timing

3.3.33 Debug Wake-up Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.91 Debug wake-up timing

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
INTDCUTDI setup time	t_{IDCUS}		1			ms
INTDCUTDI hold time	t_{IDCUH}		3			ms

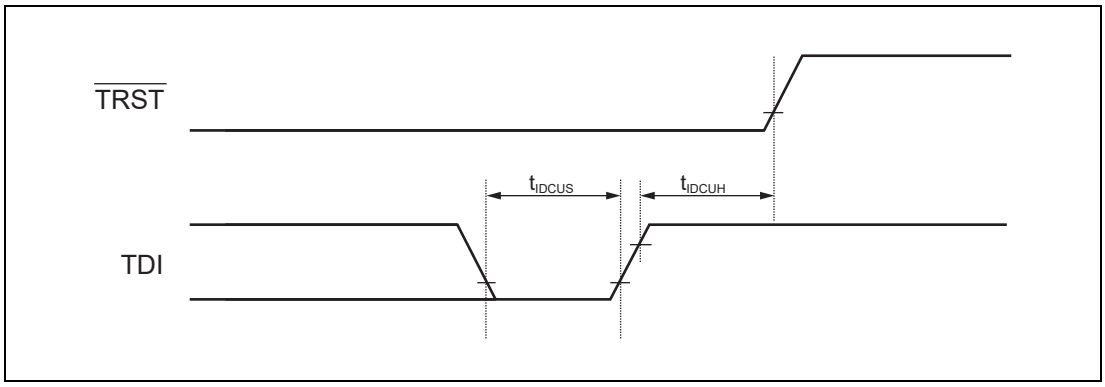


Figure 3.69 Debug wake-up timing

3.3.34 Flash Programming

3.3.34.1 Flash Programming Characteristics

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.92 Flash Programming transfer rate

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Flash Programming transfer rate	r_{FP}	2-wired UART mode			2.5	Mbps
FPCK cycle time	t_{KCYSF}	3-wired Clock Sync mode	100*1			ns
FPCK high level width	t_{KWHSF}	3-wired Clock Sync mode	$t_{KCYSF}/2 - 10$			ns
FPCK low level width	t_{KWLSF}	3-wired Clock Sync mode	$t_{KCYSF}/2 - 10$			ns
FPDR setup time	t_{SSISF}	3-wired Clock Sync mode	$2 \times t_{FPcyc}$*2			ns
FPDR hold time	t_{HSISF}	3-wired Clock Sync mode	$2 \times t_{FPcyc}$*2			ns
FPDT output delay	t_{DSOSF}	3-wired Clock Sync mode	$2 \times t_{FPcyc}$*2		$3 \times t_{FPcyc}$*2 + 32	ns
FPDT hold time	t_{HSOSF}	3-wired clock sync mode	$2 \times t_{FPcyc}$*2			ns

Note 1. Input the external clock data is more than or equal to 8 clocks of CLK_HSB.
Note 2. t_{FPcyc} is a period of CLK_HSB.

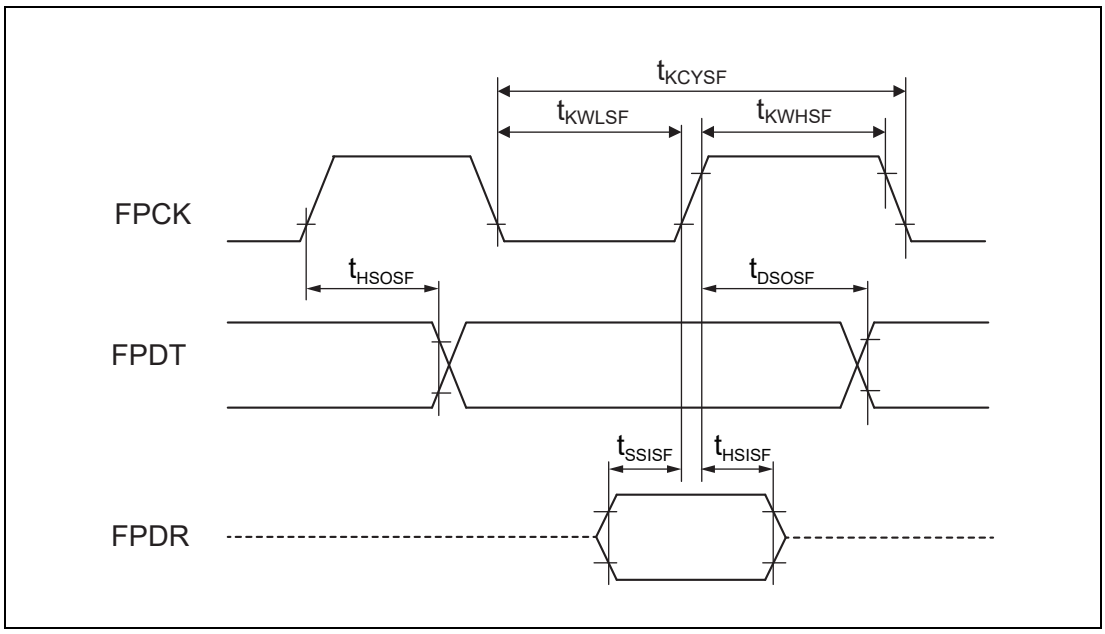


Figure 3.70 Flash Programming transfer rate

3.3.34.2 Serial Programming Setup Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.93 Serial Programming Setup Timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
FLMD0 pulse input start time	t_{MD0IS}		2			ms
FLMD0 pulse input end time	t_{MD0IE}				100	ms
FLMD0 low/high level width	t_{MD0PWL}/ t_{MD0PWH}		4			µs
FLMD0 rise time	t_{MD0R}				20	ns
FLMD0 fall time	t_{MD0F}				20	ns

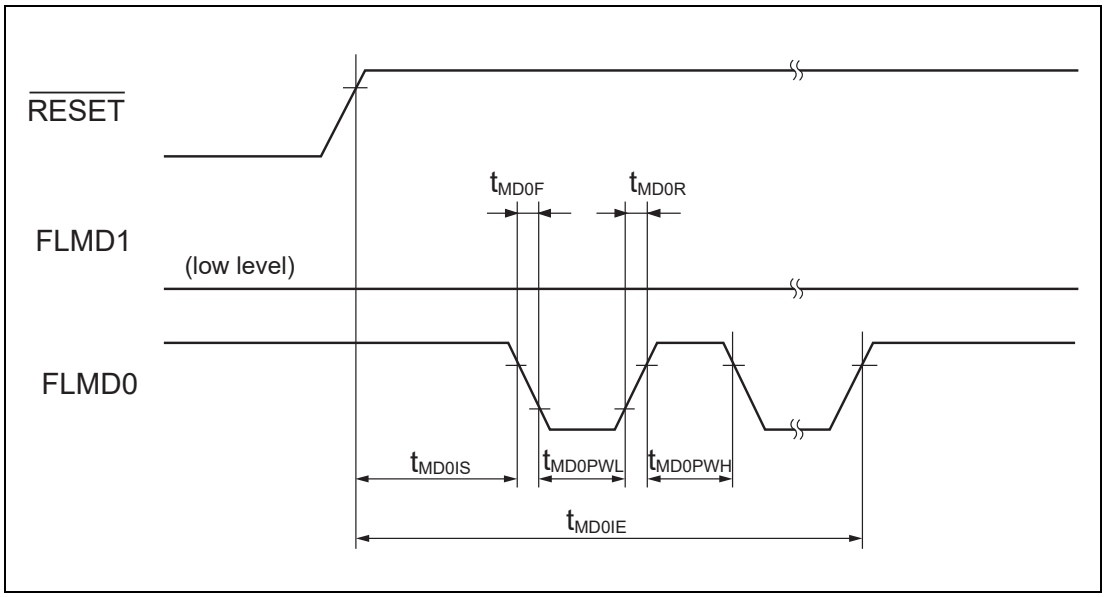


Figure 3.71 Flash Programming transfer rate

NOTE

For FLMD0 pulses, see RH850/U2A-EVA Group User's Manual: Hardware **Section 51.7.3, Selection of Flash Programming Interface**.

3.4 A/D Converter Characteristics

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.94 ADC Characteristics (1/2)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Resolution	RESn		12		12	bit
Analog supply voltages	AnVCC		3.0		5.5	V
Reference voltages	AnVREFH		AnVCC–1.0 (Do not set to below 3.0 V) [For U2A-EVA, U2A16 and U2A8 Only]		AnVCC	V
			AnVCC [For U2A6 Only]			
Analog input voltage	V_{IAN}	ADCJnIm (T&H not used)	AnVSS		AnVREFH	V
		ADCJnIm (T&H used)	0.2		AnVREFH -0.2	V
		ADCJ0ImS (A0VREFH ≥ E2VCC)	A0VSS		E2VCC	V
		ADCJ1ImS (A1VREFH ≥ E1VCC)	A1VSS		E1VCC	V
		ADCJ2ImS (A2VREFH ≥ E0VCC)	A2VSS		E0VCC	V
Operation frequency	f_{ADCLK}	CLKA_ADC	10*3		40	MHz
		CLK_ADC	20		40	MHz
Conversion time	t_{CONV}	t_{SPL} + t_{SAR}*4	1.0			µs
Sampling time	t_{SPL}*4		0.45			µs
T&H sampling time	t_{THSMP}	In self-diagnosis	0.45			µs
		First conversion (including after self-diagnosis)	10			µs
		Other than above	0.45			µs
T&H hold time	t_{THHOLD}				10	µs
Slope of analog input voltage	t_{VSIAN}	T&H used	–5		5	kV/s
Total error	TOE	ADCJnIm (T&H not used)	–4.0		4.0	LSB
		ADCJnIm (T&H used), 3.0 V ≤ AnVREFH < 4.5 V	–8.0		8.0	LSB
		ADCJnIm (T&H used), 4.5 V ≤ AnVREFH < 5.5 V	–6.0		6.0	LSB
		ADCJnImS	–8.0		8.0	LSB
Integral non-linearity error*1	INL	ADCJnIm (T&H not used)	–2.0		2.0	LSB
		ADCJnIm (T&H used)	–3.0		3.0	LSB
		ADCJnImS	–6.0		6.0	LSB
Differential non-linearity error*1	DNL	ADCJnIm (T&H not used)	–1.0		2.0	LSB
		ADCJnIm (T&H used)	–1.0		2.0	LSB
		ADCJnImS	–1.0		4.0	LSB
Offset error*1 (Zero scale error)	OSE	ADCJnIm (T&H not used)	–3.5		3.5	LSB
		ADCJnIm (T&H used), 3.0 V ≤ AnVREFH < 4.5 V	–7.5		7.5	LSB
		ADCJnIm (T&H used), 4.5 V ≤ AnVREFH < 5.5 V	–5.5		5.5	LSB
		ADCJnImS	–7.5		7.5	LSB

Table 3.94 ADC Characteristics (2/2)

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Full-scale error*1	FSE	ADCJnIm (T&H not used)		–3.5		3.5	LSB
		ADCJnIm (T&H used), 3.0 V ≤ AnVREFH < 4.5 V		–7.5		7.5	LSB
		ADCJnIm (T&H used), 4.5 V ≤ AnVREFH < 5.5 V		–5.5		5.5	LSB
		ADCJnImS		–7.5		7.5	LSB
Pin self diagnosis		for AnVCC/2		–60.0		60.0	LSB
		Other than above		–40.0		40.0	LSB
AD core self-diagnosis Function				–8.0		8.0	LSB
Secondary power supply voltage monitor absolute error*2		for E0VCC, VCC		–16		16	LSB
		for AWOVDD, ISOVDD		–10		10	LSB
Pull-up resistor for wiring break detection	R_{PU}	ADCJnIm pins	VIAN = AnVSS	10		34	kΩ
			VIAN = AnVCC/2	5		22	kΩ
			VIAN = AnVCC	3		16	kΩ
		ADCJnImS pins	VIAN = AnVSS	10		34	kΩ
			VIAN = EnVCC/2	5		22	kΩ
			VIAN = EnVCC	3		16	kΩ
Pull-down resistor for wiring break detection	R_{PD}	ADCJnIm pins	VIAN = AnVSS	1.5		10	kΩ
			VIAN = AnVCC/2	5		19	kΩ
			VIAN = AnVCC	10		34	kΩ
		ADCJnImS pins	VIAN = AnVSS	1.5		10	kΩ
			VIAN = EnVCC/2	5		19	kΩ
			VIAN = EnVCC	10		34	kΩ

Note 1. Quantization error is not included.

Note 2. Error of only voltage monitor.

Note 3. Include oscillation accuracy of HS IntOSC.

Note 4. For details of t_{SPL} and t_{SAR}, see RH850/U2A-EVA Group User's Manual: Hardware **Section 43.4.24, Analog Input Sampling and Scan Group Processing Time**.

CAUTION

An analog input pin can also be used as a digital general-purpose input or output pin.

Changes in a digital input or output at the analog input pin during an AD conversion may reduce the precision of conversion.

The coupling noise from the changes in digital inputs or outputs of pins near the analog input pin during an AD conversion may also reduce the precision of conversion.

The power supply noise from the changes in digital outputs of pins of the same power supply as the analog input or the ADC that are performing AD conversion may also reduce the precision of conversion.

3.4.1 Sampling Errors in the External Circuit of the A/D Converter

Sampling error is error to which “Errors (Sampling error 1) which depend on input leakage current of analog pin” and “Errors (Sampling error 2) which depend on conversion cycles with charge sharing” were added.

$$Sampling\ error\ =\ Sampling\ error\ 1\ +\ Sampling\ error\ 2$$

The external circuits of the A/D pins which become the factor of sampling error (sampling error 1 and sampling error 2) are shown below.

(a) Errors (Sampling error 1) which depend on input leakage current of analog pin

The error depends on the input leakage current (ILeak) of analog pin and external resistance (Re), and occurs.

The error which depends on the input leakage current is given by the formula of the following.

$$Sampling\ error\ 1\ (LSB)\ =\ Re \times ILeak \times \frac{4096}{V_{avrefh}}$$

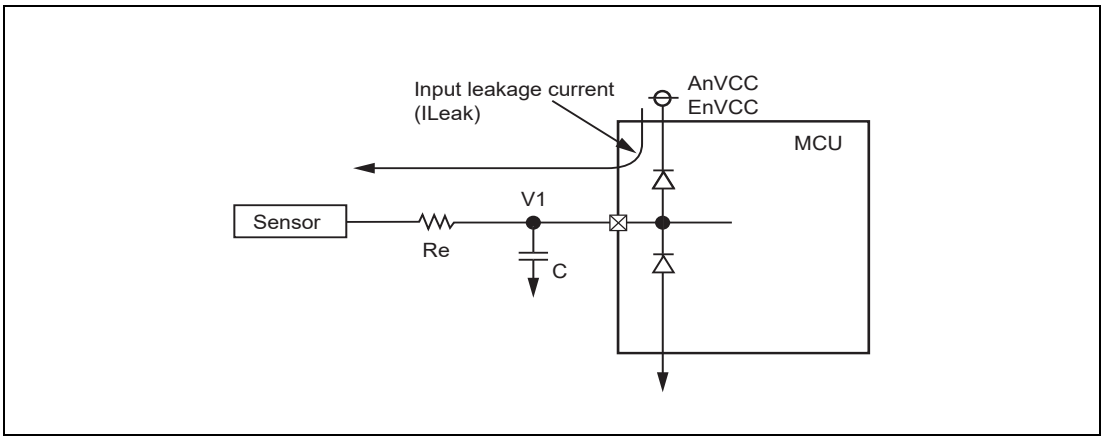


Figure 3.72 Errors (Sampling error 1) which Depend on Input Leakage Current of Analog Pin

(b) Errors (Sampling error 2) which depend on conversion cycles with charge sharing

A formula for errors in sampled values due to the external circuit of the A/D converter is given below. These errors will depend on the input circuit and conversion cycle. The formula given below for the errors is simplified for the calculation of sampling error based on internal stray capacitance, amplifier offset, resistance of the signal source, and conversion cycle. This formula can also be used to calculate the effects of the signal source resistance and conversion cycle on these errors.

The formula gives the error of analog input 2 as shown in the figure below when A/D conversion is performed in the order of analog input 1 then 2.

$$Sampling\ error\ 2\ (LSB) = \left[\left(\frac{|V2 - V1| \times CIN1}{Ce + CIN1} + \frac{|V_{vfaerr}| \times CIN2}{Ce + CIN2}\right) \times \frac{1}{1 - e^{(-T1)/(Re \times Ce)}} + \left(\frac{1}{T1} \times C1 \times V3 \times Re\right)\right] \times \frac{4096}{V_{avrefh}}$$

Table 3.95 Definition of the symbols for the Sampling Error Formula

Item	Symbol	Condition	Reference	Unit
Common capacitance of the final stage of channel multiplexer	CIN1	ADCJ0Im	1.5	pF
		ADCJ0ImS	5.2	pF
		ADCJ1Im	1.5	pF
		ADCJ1ImS	6.6	pF
		ADCJ2Im	1.5	pF
		ADCJ2ImS	5.2	pF
Common capacitance of the final stage of the amplifier and T&H control circuit	CIN2	ADCJ0Im, ADCJ0ImS	9.1	pF
		ADCJ1Im, ADCJ1ImS	9.1	pF
		ADCJ2Im, ADCJ2ImS	8.0	pF
External capacitor on analog input pin	Ce		Depends on customer's environment	µF
Signal source impedance	Re			kΩ
Conversions cycle of analog Input pins	T1			ms
AnVREFH voltage	Vavrefh			V
Potential difference between V1 and V2	V2-V1			V
Offset voltage of the amplifier and T&H control circuit	Vvfaerr		50	mV
Parasitic capacitance in the channel multiplexer	C1	ADCJnIm	2	pF
		ADCJnImS	4	
|AnVCC voltage / 2.5 - measured pin voltage (V2)|	V3		Depends on customer's environment	V

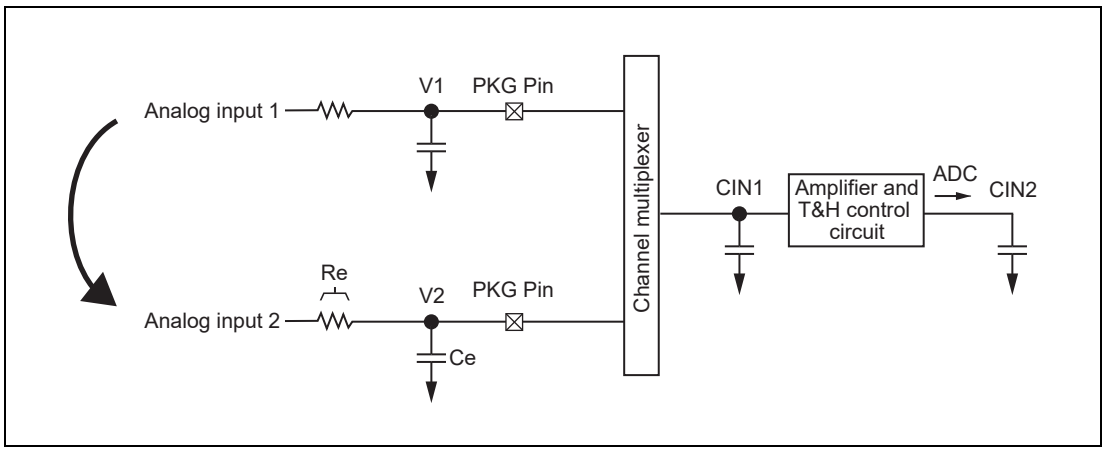


Figure 3.73 Schematic for Sampling Error 2 Formula

Values for conversion error calculated by using this formula do not include error (absolute error, etc.) specified in the A/D converter characteristics.

This formula is a desktop formula and is theoretical. When the signal source has an extremely high resistance or when the conversion cycle is too short, calculated and measured values may differ. Actual error depends on the external capacitor, external resistor, capacitance and resistance of board wiring, so evaluate and verify the error on the user board is no greater than the value produced by this formula (Condition of this formula is "Re < 1.5 MΩ and T1 ≥ 10 µs", or "1.5 MΩ ≤ Re ≤ 2 MΩ and T1 ≥ 512 µs").

3.5 Code Flash Characteristics

The code flash memory is shipped in the erased state. If the code flash memory is read where it has not been written after erasure (no write condition), an ECC error is generated, resulting in the occurrence of an exception.

Table 3.96 Code Flash Basic Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Operation frequency	f_{CLKFC} *1		8		40	MHz
Number of rewrites*2	CWRT	Data retention of 20 years*3	1000			times

Note 1. f_{CLKFC} is the frequency of CLK_LSB.

Note 2. The number of rewrites is the number of erasures for each block. When the number of rewrites is “n”, the device can be erased “n” times for each block. For example, when a block of 64 KB is erased after 512 bytes of writing have been performed for different addresses 128 times, the number of rewrites is counted as 1. However, multiple writing to the same address is not possible with 1 erasure (overwriting prohibited).

Note 3. Retention period under average Ta = 85°C. This is the period starting on completion of a successful erasure of the code flash memory.

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- Only the processing time of the hardware. The overhead required by the software is not included.

Table 3.97 Code Flash Programming Characteristics

Item	Symbol	Block size	Condition	8MHz ≤ f_{CLKFC} < 20 MHz			20MHz ≤ f_{CLKFC} < 40 MHz			f_{CLKFC} = 40 MHz			Unit
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Programming time		512 B	CWRT < 100 times		0.31	2.0		0.25	1.8		0.24	1.7	ms
			CWRT ≥ 100 times		0.39	2.4		0.3	2.2		0.29	2.1	ms
		8 KB	CWRT < 100 times		5.0	17		4.0	15		3.8	14	ms
			CWRT ≥ 100 times		6.0	20		4.8	18		4.6	17	ms
		1 MB	CWRT < 100 times		0.64	2.2		0.5	1.9		0.47	1.8	s
			CWRT ≥ 100 times		0.77	2.7		0.6	2.3		0.57	2.2	s
Erasure time*1		16 KB	CWRT < 100 times		26	108		24	98		24	96	ms
			CWRT ≥ 100 times		32	130		29	118		29	116	ms
		64 KB	CWRT < 100 times		88	374		81	340		78	330	ms
			CWRT ≥ 100 times		106	449		98	408		94	396	ms
		1 MB	CWRT < 100 times		1.4	6.0		1.3	5.4		1.25	5.3	s
			CWRT ≥ 100 times		1.7	7.2		1.6	6.5		1.5	6.4	s

Note 1. When erase counter function is used, add the erase counter update time. For details, see **Table 3.101** and **Table 3.102**.

Table 3.98 Code Flash Programming/Erasure suspend latency Characteristics

Item	Symbol	Block size	Condition	8MHz ≤ f_{CLKFC} < 20 MHz			20MHz ≤ f_{CLKFC} < 40 MHz			f_{CLKFC} = 40 MHz			Unit
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Programming Suspend Latency	tSPD					160			120			120	µs
Erasure Suspend Latency	tSESD1		Priority on suspension The 1st suspend for the same erasing pulse			150			120			120	µs
	tSESD2		Priority on suspension The 2nd suspend for the same erasing pulse			1.7			1.7			1.7	ms
	tSEED		Priority on erasure			1.7			1.7			1.7	ms

Table 3.99 Code Flash Programming/Erasure resume latency Characteristics

Item	Symbol	Block size	Condition	8MHz ≤ f_{CLKFC} < 20 MHz			20MHz ≤ f_{CLKFC} < 40 MHz			f_{CLKFC} = 40 MHz			Unit
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Programming Resume Latency	tRPT					80			50			50	µs
Erasure Resume Latency	tREST1		Priority on suspension Resume after the 1st suspend for the same erasing pulse			1.7			1.7			1.7	ms
	tREST2		Priority on suspension Resume after the 2nd suspend for the same erasing pulse			110			80			80	µs
	tREET		Priority on erasure			110			80			80	µs

Table 3.100 Code Flash Forced Stop command latency

Item	Symbol	Block size	Condition	8MHz ≤ f_{CLKFC} < 20 MHz			20MHz ≤ f_{CLKFC} < 40 MHz			f_{CLKFC} = 40 MHz			Unit
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Forced Stop command Latency	tFD					28			20			20	µs

Table 3.101 Erase Counter update time Characteristics [For U2A-EVA]

Item	Symbol	Block size	Condition	8MHz ≤ f_{CLKFC} < 20 MHz			20MHz ≤ f_{CLKFC} < 40 MHz			f_{CLKFC} = 40 MHz			Unit
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Erase Counter update time					31.64	448.72		29.1	430.08		28.75	422.88	ms

Table 3.102 Erase Counter update time Characteristics [For U2A16/U2A8/U2A6]

Item	Symbol	Block size	Condition	8MHz ≤ f_{CLKFC} < 20 MHz			20MHz ≤ f_{CLKFC} < 40 MHz			f_{CLKFC} = 40 MHz			Unit
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Erase Counter update time					16.64	193.72		15.0	181.08		14.65	176.88	ms

3.6 Data Flash Characteristics

The data flash memory is shipped in the erased state. If the data flash memory is read where it has not been written after erasure (no write condition), an ECC error is generated, resulting in the occurrence of an exception.

Table 3.103 Data Flash Basic Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Operation frequency	f_{CLKFD} *1		8		40	MHz
Number of rewrites*2	DWRT	Data retention 20 years*3	125k			Times
		Data retention 3 years*3	250k			Times

Note 1. f_{CLKFD} is the frequency of CLK_LSB.

Note 2. The number of rewrites is the number of erasures for each block. When the number of rewrites is “n”, the device can be erased “n” times for each block. For example, when a block of 4096 bytes is erased after 4 bytes of writing have been performed for different addresses 1024 times, the number of rewrites is counted as 1. However, multiple writing to the same address is not possible with 1 erasure (overwriting prohibited).

Note 3. Retention period under average Ta = 85°C. This is the period starting on completion of a successful erasure of the data flash memory.

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- Only the processing time of the hardware. The overhead required by the software is not included.

Table 3.104 Data Flash Programming Characteristics

Item	Symbol	Block size	Condition	8MHz ≤ f_{CLKFD} < 20 MHz			20MHz ≤ f_{CLKFD} < 40 MHz			f_{CLKFD} = 40 MHz			Unit
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Programming time		4 B			0.12	0.82		0.09	0.70		0.08	0.66	ms
		8 B			0.13	0.88		0.09	0.73		0.08	0.67	ms
		16 B			0.14	0.97		0.09	0.76		0.08	0.70	ms
		32 B			0.14	0.97		0.09	0.76		0.08	0.70	ms
		64 B			0.14	0.97		0.10	0.76		0.09	0.70	ms
		128 B			0.17	1.20		0.13	0.95		0.11	0.89	ms
		2 KB			2.72	9.64		2.08	7.56		1.76	6.92	ms
		128 KB			0.174	0.62		0.13	0.48		0.11	0.44	s
Property Programming time		32 B			0.41	2.64		0.29	2.18		0.25	2.03	ms
Switch Programming time		32 B			0.26	1.79		0.18	1.46		0.16	1.36	ms
TAG Update time					0.30	1.70		0.21	1.43		0.18	1.34	ms
Erasure time		2 KB *1			11.1	105		9.9	95		9.6	92	ms
		4 KB			19.2	179		17	160		16.4	155	ms
		128 KB			0.62	5.73		0.55	5.12		0.53	4.96	s
Blank check command time		4 B				5.5			2.3			1.3	µs
		4 KB				1.8			0.8			0.5	ms
Property Erasure time		2 KB			11.1	105		9.9	95		9.6	92	ms
Switch Erasure time		2 KB			11.4	106.7		10.1	96.4		9.8	93.4	ms
TAG Erasure time		2 KB			11.4	106.7		10.1	96.4		9.8	93.4	ms

Note 1. Extended Data Area Only

Table 3.105 Data Flash Programming/Erasure suspend latency Characteristics

Item	Symbol	Block size	Condition	8MHz ≤ f_{CLKFD} < 20 MHz			20MHz ≤ f_{CLKFD} < 40 MHz			f_{CLKFD} = 40 MHz			Unit
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Programming Suspend Latency*1	tSPD					160			120			120	µs
Erasure Suspend Latency*1	tSESD1		Priority on suspension The 1st suspend for the same erasing pulse			150			120			120	µs
	tSESD2		Priority on suspension The 2nd suspend for the same erasing pulse			300			300			300	µs
	tSEED		Priority on erasure			300			300			300	µs

Note 1. Data Area and Extended Data Area Only

Table 3.106 Data Flash Programming/Erasure resume latency Characteristics

Item	Symbol	Block size	Condition	8MHz ≤ f_{CLKFD} < 20 MHz			20MHz ≤ f_{CLKFD} < 40 MHz			f_{CLKFD} = 40 MHz			Unit
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Programming Resume Latency*1	tRPT					80			50			50	µs
Erasure Resume Latency*1	tREST1		Priority on suspension Resume after the 1st suspend for the same erasing pulse			300			300			300	µs
	tREST2		Priority on suspension Resume after the 2nd suspend for the same erasing pulse			100			70			70	µs
	tREET		Priority on erasure			100			70			70	µs

Note 1. Data Area and Extended Data Area Only

Table 3.107 Forced Stop command latency

Item	Symbol	Block size	Condition	8MHz ≤ f_{CLKFD} < 20 MHz			20MHz ≤ f_{CLKFD} < 40 MHz			f_{CLKFD} = 40 MHz			Unit
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Forced Stop command Latency	tFD					28			20			20	µs

3.7 Temperature Sensor Characteristics

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.108 Temperature Sensor Characteristics*1*2*3

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Temperature accuracy	A_{CCTS1}	– 40 °C ≤ Tj ≤ + 140 °C	–4		4	°C
	A_{CCTS2}	Tj > 140 °C	–2		2	°C
Temperature update period	t_{TSUP}		10			ms
Operation stabilization waiting time	t_{TSSB}				200	µs

Note 1. The temperature borders need to be set keeping the temperature range (Tj(min) to Tj(max)) including the temperature sensor accuracy.

Note 2. It does not include accuracy of measuring equipment.

Note 3. Temperature sensor cannot detect local heat generation inside the chip.

3.8 Thermal Characteristics

3.8.1 Thermal Characteristics Parameter

Table 3.109 Thermal Characteristics*1

Parameter	Estimated value										Unit	Remark
	U2A-EVA	U2A16			U2A8		U2A6					
	BGA516	BGA516	BGA373	BGA292	BGA373	BGA292	BGA292	QFP176	BGA156	QFP144		
θja	10.8	13.4	13.7	13.9	15.9	16.3	17.9	12.4	18.7	12.6	°C/W	JESD51-9 compliant (4 layers)
θjb	6.0	8.8	8.5	8.0	10.6	10.3	12.1	6.0	10.9	5.0	°C/W	JESD51-9 compliant (4 layers)
θjc	3.7	5.7	5.8	5.9	7.8	8.2	9.3	11.9	11.4	11.6	°C/W	JESD51-9 compliant (4 layers)
θjcbot	3.4	5.3	5.4	5.3	7.2	7.3	8.7	1.1	8.3	0.7	°C/W	JESD51-9 compliant (4 layers)
Ψjb	5.7	8.4	8.1	7.7	10.2	10.0	11.8	5.8	10.6	4.9	°C/W	JESD51-9 compliant (4 layers)
Ψjmb*2	3.1	4.8	4.6	4.9	6.3	6.5	7.9	0.9	7.8	0.6	°C/W	JESD51-9 compliant (4 layers)
Ψjt	0.2	0.2	0.2	0.2	0.2	0.2	0.3	0.3	0.3	0.3	°C/W	JESD51-9 compliant (4 layers)
4Lθja	12.7	15.8	16.1	16.7	18.5	19.3	21.0	14.3	23.1	15.1	°C/W	L board (4 layers)
4Lθjb	7.3	10.5	10.0	9.6	12.3	12.0	14.0	8.0	12.7	6.9	°C/W	L board (4 layers)
4LΨjb	6.7	9.9	9.4	9.1	11.7	11.5	13.4	7.9	12.3	6.7	°C/W	L board (4 layers)
4LΨjmb*2	3.1	4.7	4.4	4.8	6.0	6.3	7.7	0.9	8.0	0.5	°C/W	L board (4 layers)
4LΨjt	0.2	0.2	0.2	0.2	0.3	0.3	0.3	0.3	0.4	0.3	°C/W	L board (4 layers)
4LTb_inc	6.2	5.9	6.9	7.6	6.9	7.9	7.8	6.4	10.9	8.3	°C/W	L board (4 layers)

Note 1. The thermal characterization parameters depends on the usage environment.

Note 2. Ψjmb shows thermal characterization parameter from junction to board surface (center of the PKG on layer-1; Tmb).

Ψjmb = (Tj-Tmb)/Pd (Pd: power consumption of the chip)

3.8.2 Assumed Board

Table 3.110 JESD51-9 Compliant Board (4 layers)

	Board Size (mm)		
	X	Y	Area (mm^2)
Board Size	101.5	114.5	11621.75
Remaining copper rate		Conductor thickness	
50 – 95 – 95 – 50%		70 – 35 – 35 – 70 µm	

Table 3.111 L board (4 layers)

	Board Size (mm)		
	X	Y	Area (mm^2)
Board Size	90	160	14400
Remaining copper rate		Conductor thickness	
30 – 80 – 80 – 30%		35 – 35 – 35 – 35 µm	

3.9 BSCAN Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- Buffer type = TTL

Table 3.112 BSCAN Timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
TCK cycle width	t_{DCKW}		100			ns
TDI setup time	t_{SDI}		12			ns
TDI hold time	t_{HDI}		3			ns
TMS setup time	t_{SMS}		12			ns
TMS hold time	t_{HMS}		3			ns
TDO delay time	t_{DDO}		0		30	ns

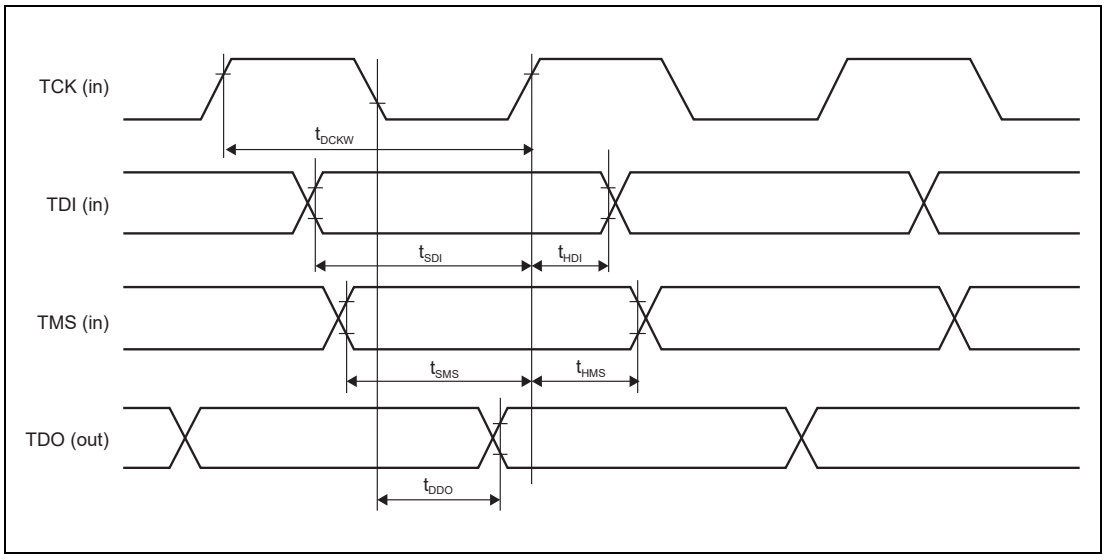


Figure 3.74 BSCAN Timing

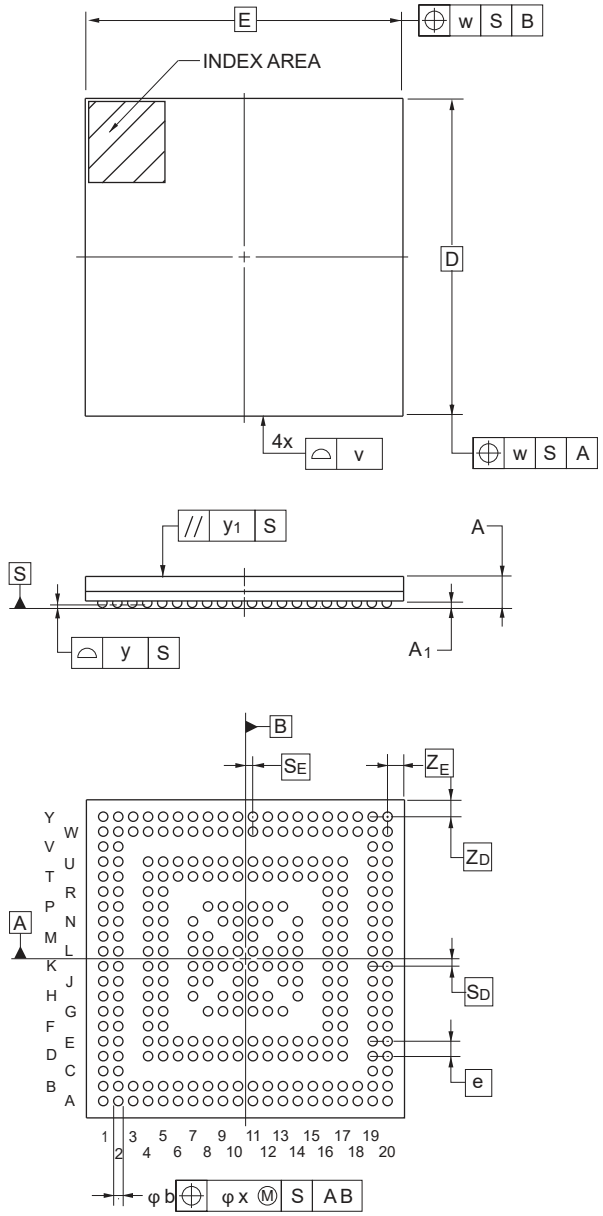
Section 4 Package

4.1 Package Outline

4.1.1 FPBGA (292pin) Package Drawing

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-FBGA292-17x17-0.80	PRBG0292GC-A	T292F1-80-GNP	0.9

Unit: mm



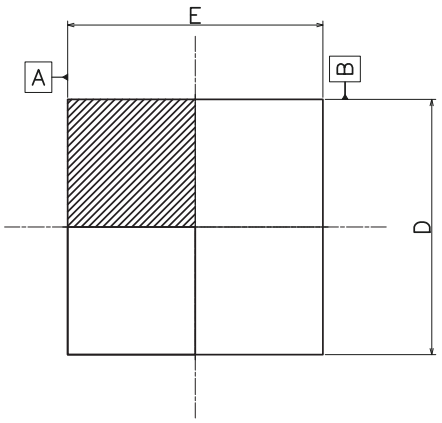
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	17.00	—
E	—	17.00	—
A	—	—	1.90
A_1	0.30	0.35	0.40
e	—	0.80	—
b	0.50	0.55	0.60
x	—	—	0.12
y	—	—	0.10
y_1	—	—	0.20
Z_D	—	0.90	—
Z_E	—	0.90	—
v	—	—	0.15
w	—	—	0.20
S_D	—	0.40	—
S_E	—	0.40	—

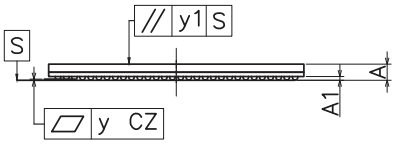
Note: INDEX AREA is on the corner near a ball A1 (Top View side).

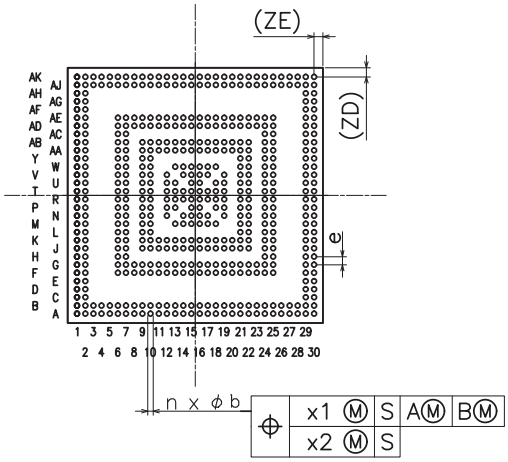
Figure 4.1 FPBGA (292pin) outline

4.1.2 FPBGA (516pin (RENESAS Code = PRBG0516GC-A)) Package Drawing

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-FBGA516-25x25-0.80	PRBG0516GC-A	2.00







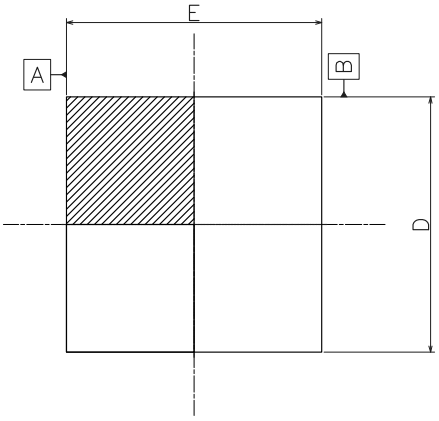
Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	24.90	25.00	25.10
E	24.90	25.00	25.10
A	—	—	2.00
A_1	0.29	0.34	0.39
e	—	0.80	—
b	0.50	0.55	0.60
x_1	—	—	0.20
x_2	—	—	0.08
y	—	—	0.15
y_1	—	—	0.20
n	—	516	—
Z_D	—	0.90	—
Z_E	—	0.90	—

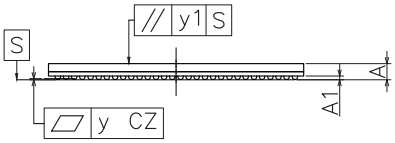
Note: INDEX AREA is on the corner near a ball A1 (Top View side).

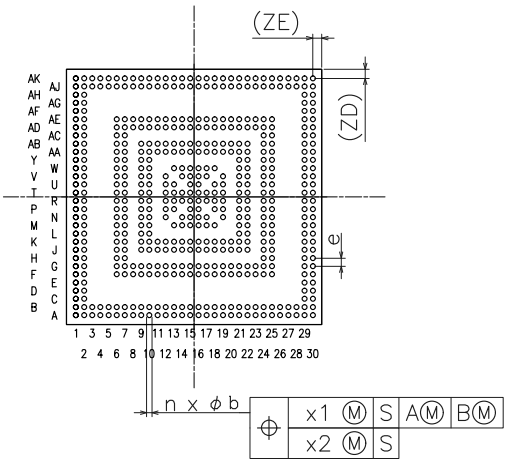
Figure 4.2 FPBGA (516pin (RENESAS Code = PRBG0516GC-A)) outline

4.1.3 FPBGA (516pin (RENESAS Code = PRBG0516GD-A)) Package Drawing

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-FBGA516-25x25-0.80	PRBG0516GD-A	2.20







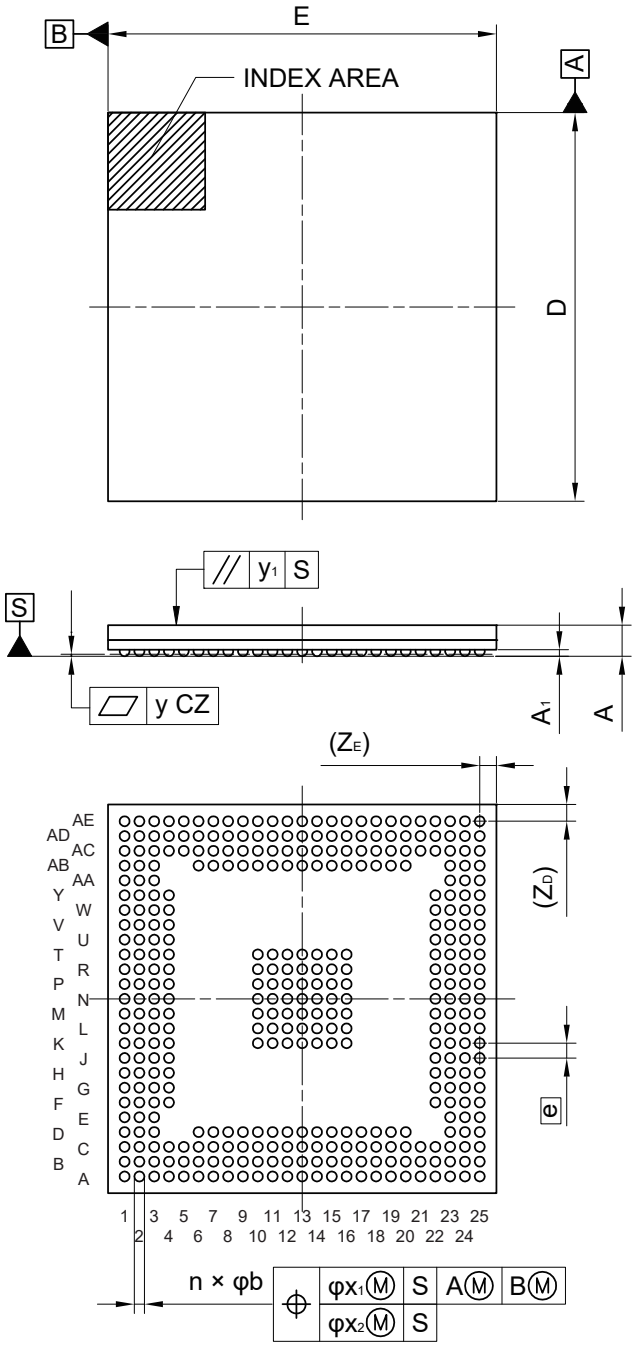
Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	24.90	25.00	25.10
E	24.90	25.00	25.10
A	—	—	2.00
A_1	0.29	0.34	0.39
e	—	0.80	—
b	0.50	0.55	0.60
x_1	—	—	0.20
x_2	—	—	0.08
y	—	—	0.15
y_1	—	—	0.20
n	—	516	—
Z_D	—	0.90	—
Z_E	—	0.90	—

Note: INDEX AREA is on the corner near a ball A1 (Top View side).

Figure 4.3 FPBGA (516pin (RENESAS Code = PRBG0516GD-A)) outline

4.1.4 FPBGA (373pin) Package Drawing

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-FBGA373-21x21-0.80	PRBG0373GB-A	1.4



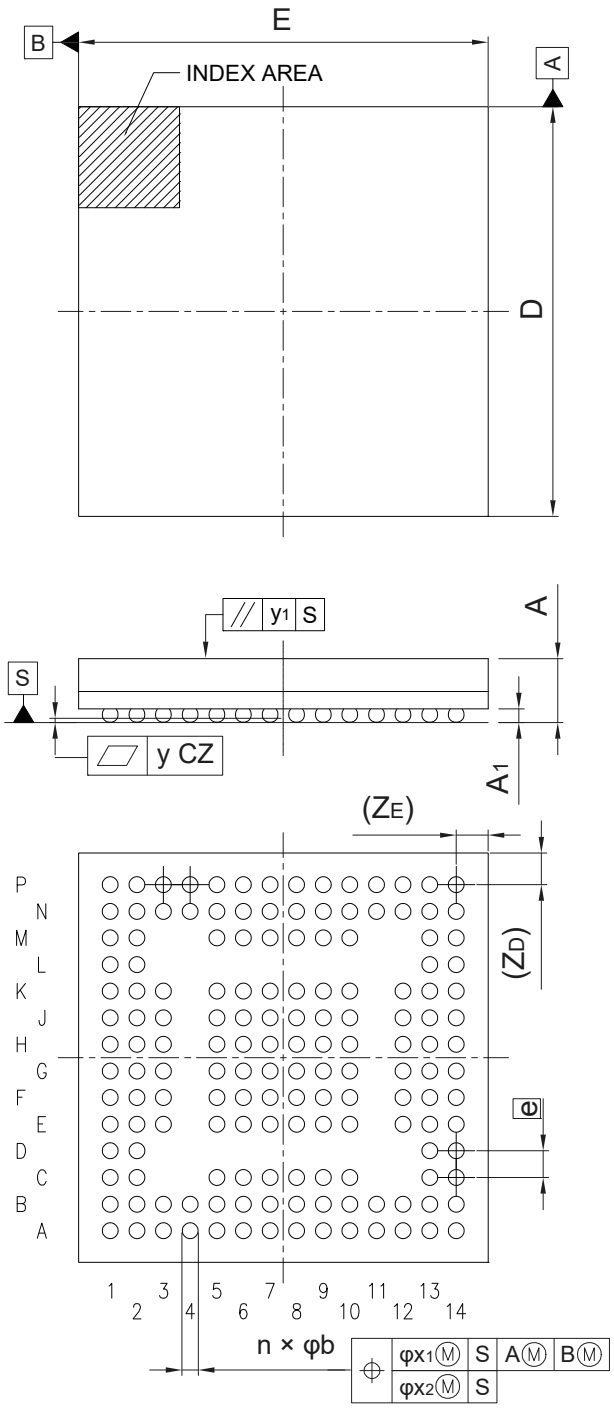
Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	20.90	21.00	21.10
E	20.90	21.00	21.10
A	—	—	2.00
A_1	0.30	0.35	0.40
e	—	0.80	—
b	0.49	0.54	0.59
x_1	—	—	0.20
x_2	—	—	0.08
y	—	—	0.10
y_1	—	—	0.20
Z_D	—	0.90	—
Z_E	—	0.90	—
n	—	373	—

Note: INDEX AREA is on the corner near a ball A1 (Top View side).

Figure 4.4 FPBGA (373pin) outline

4.1.5 LFPBGA (156pin) Package Drawing

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-LFBGA156-10x10-0.65	PLBG0156JC-A	0.30



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	9.92	10.00	10.08
E	9.92	10.00	10.08
A	—	—	1.70
A_1	0.21	0.26	0.31
e	—	0.65	—
b	0.40	0.45	0.50
x_1	—	—	0.15
x_2	—	—	0.08
y	—	—	0.10
y_1	—	—	0.20
n	—	156	—
Z_D	—	0.775	—
Z_E	—	0.775	—

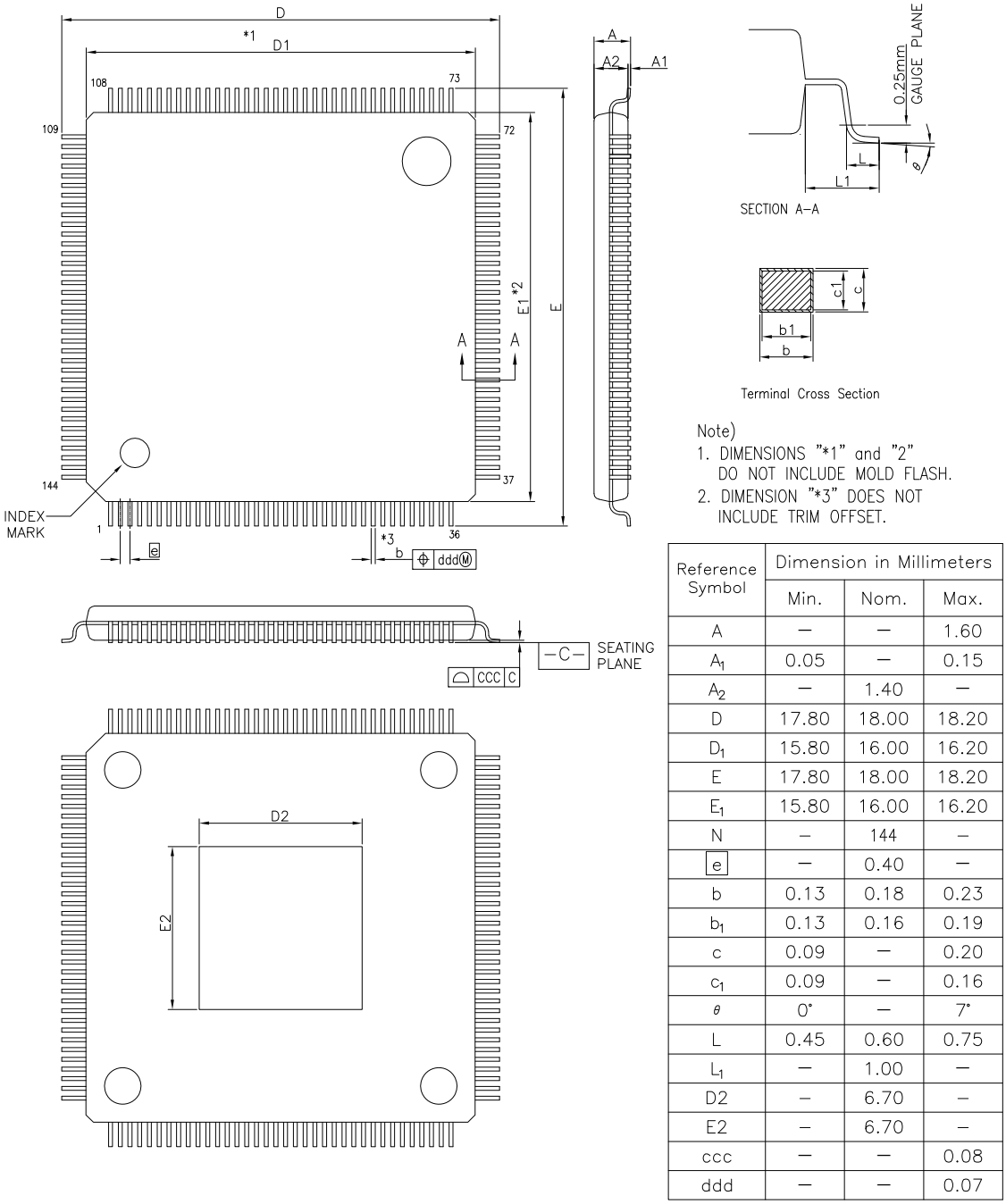
Note: INDEX AREA is on the corner near a ball A1 (Top View side).

Figure 4.5 LFPBGA (156pin) outline

4.1.6 HLQFP (144pin) Package Drawing

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HLFQFP144-16x16-0.40	PLQP0144LC-B	0.90

UNIT:MM



Note)
1. DIMENSIONS "*1" and "2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

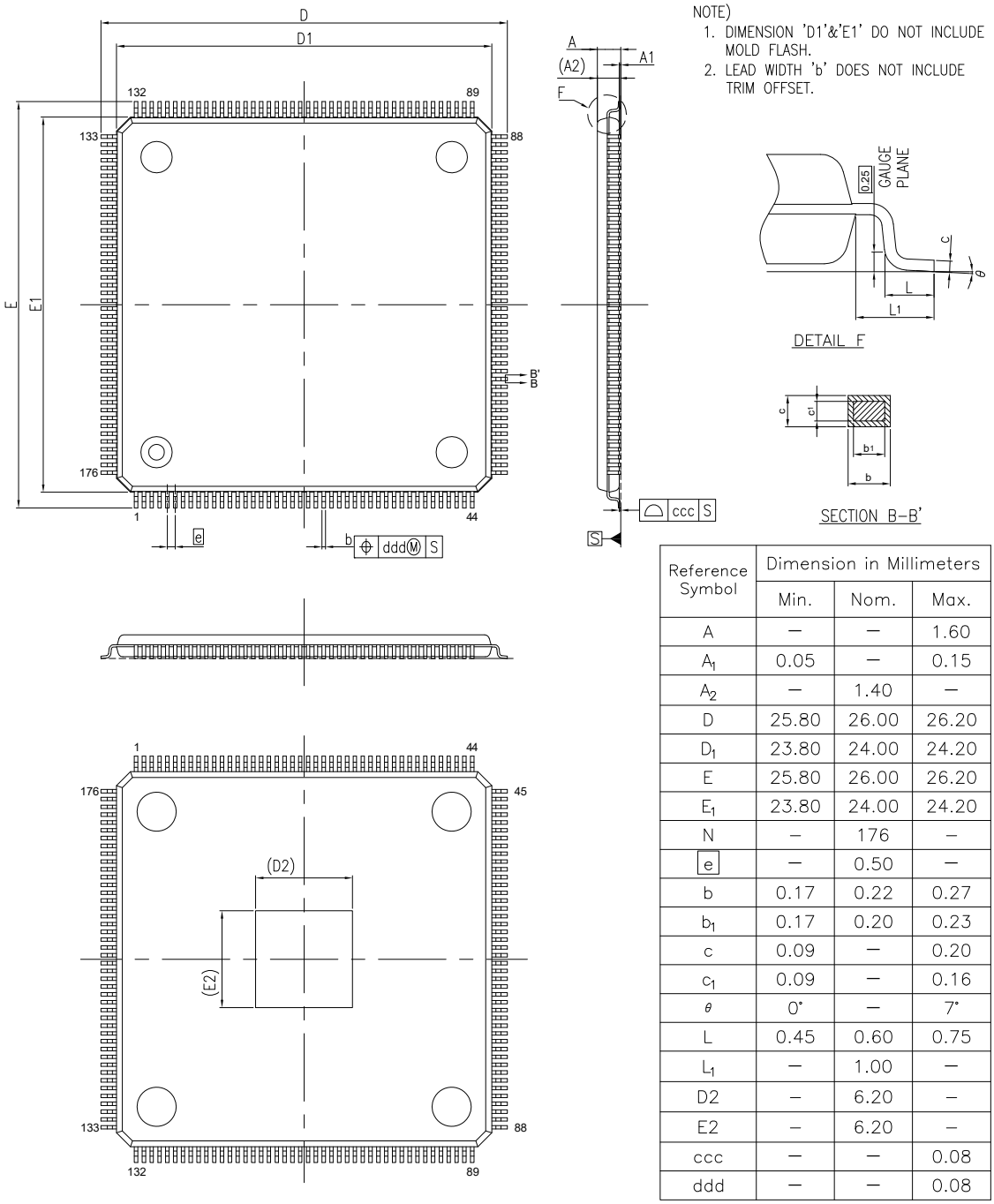
Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	–	–	1.60
A_1	0.05	–	0.15
A_2	–	1.40	–
D	17.80	18.00	18.20
D_1	15.80	16.00	16.20
E	17.80	18.00	18.20
E_1	15.80	16.00	16.20
N	–	144	–
e	–	0.40	–
b	0.13	0.18	0.23
b_1	0.13	0.16	0.19
c	0.09	–	0.20
c_1	0.09	–	0.16
θ	0°	–	7°
L	0.45	0.60	0.75
L_1	–	1.00	–
D2	–	6.70	–
E2	–	6.70	–
ccc	–	–	0.08
ddd	–	–	0.07

Figure 4.6 HLQFP (144pin) outline

4.1.7 HLQFP (176pin) Package Drawing

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HLFQFP176-24x24-0.50	PLQP0176KH-B	1.97

UNIT: MM



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	–	–	1.60
A_1	0.05	–	0.15
A_2	–	1.40	–
D	25.80	26.00	26.20
D_1	23.80	24.00	24.20
E	25.80	26.00	26.20
E_1	23.80	24.00	24.20
N	–	176	–
e	–	0.50	–
b	0.17	0.22	0.27
b_1	0.17	0.20	0.23
c	0.09	–	0.20
c_1	0.09	–	0.16
θ	0°	–	7°
L	0.45	0.60	0.75
L_1	–	1.00	–
D2	–	6.20	–
E2	–	6.20	–
ccc	–	–	0.08
ddd	–	–	0.08

Figure 4.7 HLQFP (176pin) outline

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	2025.06.16	-	First Edition

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to power supply or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.
5. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
6. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
7. Power ON/OFF sequence
   In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

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