Product Introduction

Concept

The market of instrument clusters on automotive requires various kinds of unit, such as from traditional instrument clusters to graphical instrument clusters.

The RH850/D1x series microcontroller focuses on instrument clusters for automotive.

The RH850/D1x series can cover wide range of instrument clusters.

Major differences in the series are functionality of graphics.

Then, it is possible to choose products in RH850/D1x series by graphics functionality of instrument clusters.

In addition, other functionality, such as standard peripherals and instrument cluster specific peripherals, has very high compatibility.

Therefore, RH850/D1x series makes easy to develop platform by reducing software development costs.

In addition, there are several features, such as internal Video RAM, for reduce BOM costs.

Function Overview

- JCP-2016 BL products (1/2)

Product Features			D1S1
Memory	Code Flash		1 MB
	Local RAM (LRAM)		128 KB
	Retention RAM (RRAM)		16 KB
	Data Flash		32 KB
	Video RAM (VRAM) with Video RAM wrapper		—
External memory interfaces	Serial Flash Memory I/F (SFMA)	Bus width	—
		Mode	
		Max. clock	
CPU	CPU System		G3M
	CPU frequency		120 MHz
	Floating Point Unit (FPU)		Provided
	Memory Protection Unit (MPU)		Provided
	Memory caches	Instruction cache	8 KB/4-way associative
		Non-CPU system memories	—
DMA			16 channels
Operating clock	Main Oscillator (MainOSC)		8 to 16 MHz
	Low Speed Internal Oscillator (LS IntOSC)		typ. 240 kHz
	High Speed Internal Oscillator (HS IntOSC)		typ. 8 MHz
	Sub Oscillator (SubOSC)		typ. 32.768 kHz
	Spread-spectrum PLL0		max. 480 MHz
	PLL1		fixed to 480 MHz
I/O port			92
A/D Converter (ADCE)			16 channels, 12 bit resolution
Timer	Timer Array Unit B (TAUB)		3 units (16 bit resolution, 16 channels/unit)
	Timer Array Unit J (TAUJ)		1 unit (32 bit resolution, 4 channels/unit)
	Operating System Timer (OSTM)		2 units (32 bit resolution, 1 channel/unit)
	Alway-On-Area Timer (AWOT)		1 unit (32 bit resolution, 1 channel/unit)
	Real-Time Clock (RTCA)		Provided
	Window Watchdog Timer A (WDTA)		2 units
	PWM Generators with Diagnostic		1 unit (12 bit resolution, 24 PWM generators, 12 with diagnostic capability)
Communication interfaces	Clocked Serial Interface G (CSIG)		4 channels
	Clocked Serial Interface H (CSIH)		2 channels
	CAN Interface (RS-CAN)		3 channels (total 192 message buffers)*1
	CAN Interface (RS-CANFD)		3 channels (total 192 message buffers)*1
	LIN/UART Interface (RLIN3)		4 channels
	I^2C Interface (RIIC)		3 channels
External interrupts	Maskable		11
	Non-maskable (NMI)		1
Audio	Sound Generator (SG)		1 unit
	PCM-PWM Converter (PCMP)		1 unit
	Serial Sound Interface (SSIF)		2 units (1 channel/unit)

- JCP-2016 BL products (2/2)

Product Features			D1S1
Video and Graphics	Video Output	Channels	—
		I/F	—
		RLE decoding	—
		Sprite layer	—
		Timing Controller (TCON)	—
Other functions	LCD Bus I/F (LCBI)		8 bit output, max. 10 MHz*4
	Clock Monitors (CLMA)		for MainOSC, LS IntOSC, HS IntOSC, PLL0, PLL1
	Data CRC (DCRA)		Provided
	Power-On-Clear (POC)		Provided
	Intelligent Stepper Motor Driver (ISM), incl. zero point detection for each channel		1 unit, 4 channels
	Error Correction Coding (ECC)		for Code Flash, Data Flash, Local RAM, Retention RAM, RS-CAN RAM, Caches tag/data RAMs
	Intelligent Cryptographic Unit (ICU-S2)		Provided
	On-Chip debug (OCD)		Provided
	Boundary Scan		Provided
Voltage supply*2	Internal logic	AWO*3	3.3 V, 5 V via on-chip voltage regulator
		ISO*3	3.3 V, 5 V via on-chip voltage regulator
	I/O buffers	GPIO*3	3.3 V, 5 V
	A/D Converter supplies		nominal 3.3 V, 5 V
Package	Type		QFP
	Pins		144
	pin/ball pitch		0.5 mm

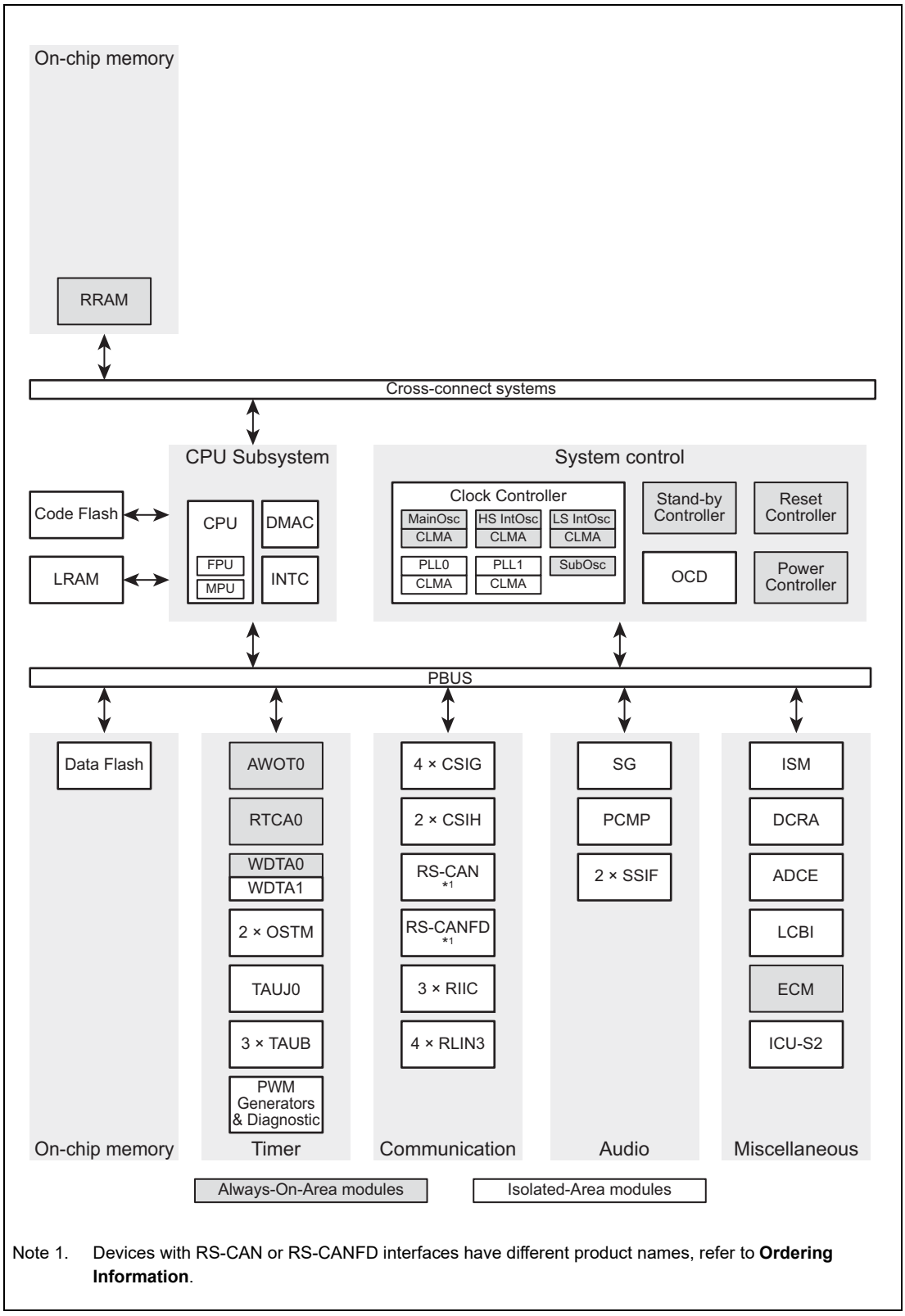
Note 1. Devices with RS-CAN or RS-CANFD interfaces have different product names, refer to **Ordering Information**.

Note 2. The supply voltages are given as nominal values. Refer to data sheet **Section 1.5.7, Supply Voltage** for detail specification of electrical values.

Note 3. AWO: Always-On-Area
ISO: Isolated-Area
GPIO: General purpose I/O port

Note 4. The LCBI module of this device does not support the TFT mode.

Block Diagram



Note 1. Devices with RS-CAN or RS-CANFD interfaces have different product names, refer to **Ordering Information**.

D1S1 Block Diagram

Ordering Information

Series Name	Part Number	Renesas Order Code	Remarks
D1S1	R7F701417		D1S1 with RS-CAN I/F
	R7F701437		D1S1 with RS-CANFD I/F

Pin Map

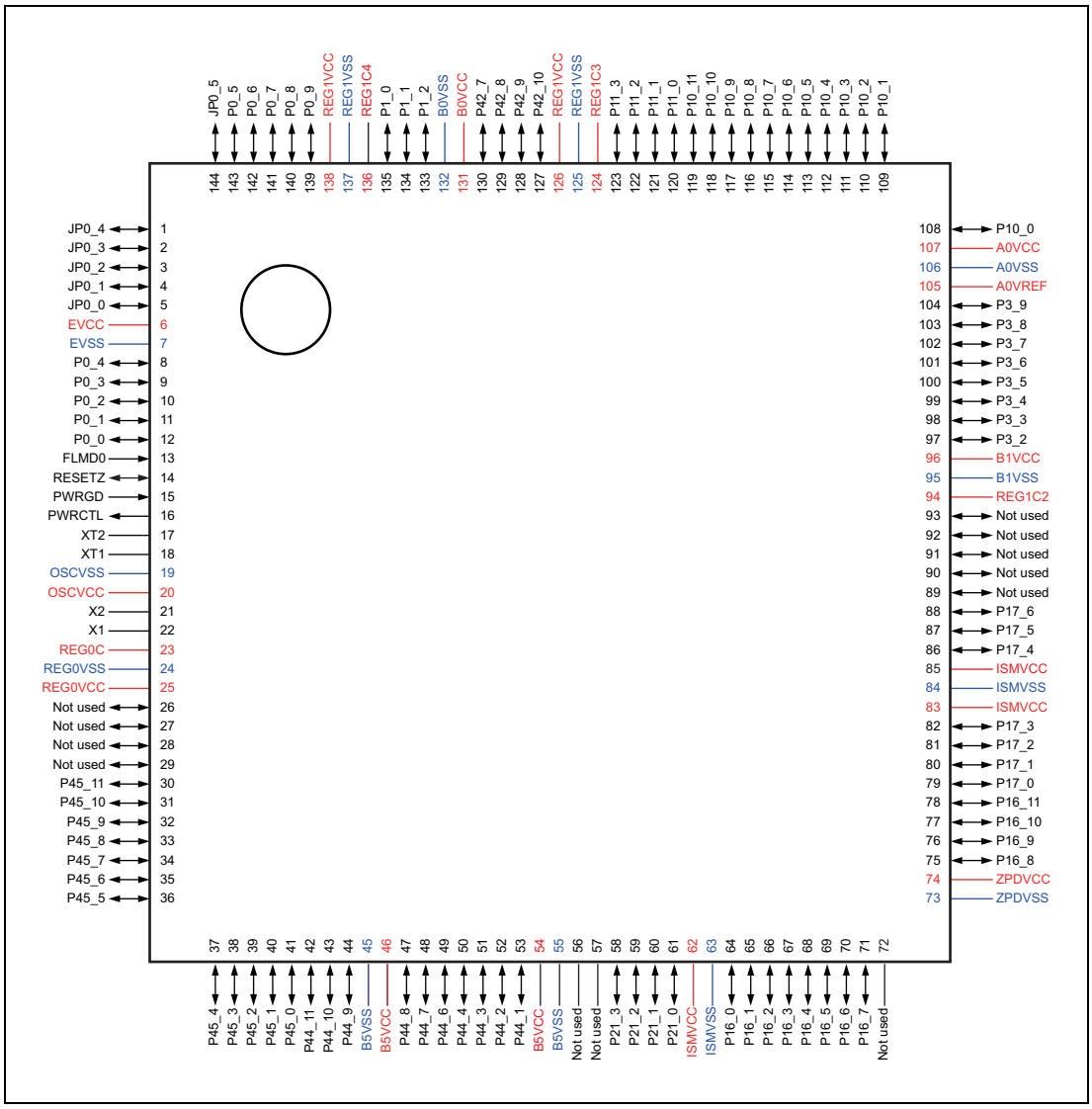


Figure A.1 D1S1(R7F701417) (Top View)

Product Lineup

The RH850/D1x device family comprises several family members. An overview with the pin and package information is given in the following table:

	Family Member	Package
RH850/D1S1	R7F701417	QFP144
	R7F701437	

Terms for Temperature

This specification describes a class of powerful devices that self-heating depend on the usage and thereby needed current consumption. Therefore this specification is based on two data for temperature:

- T_j: TJ or alternative T_j

is the chip junction temperature in [°C].

- Ta: TA or alternative Ta

is the ambient temperature (according to JEDEC standard JESD51-2A) in [°C] For details about the coherence between T_j and Ta see **Section 2.1, Junction-to-Ambient Resistance**.

Section 1 Electrical Specifications

1.1 Pin Groups

1.1.1 Power Supply Pins

Information about the power supply pin naming and the power supply schemes, i.e. the power supply pins and the modules they supply are provided in the "*User's Manual*" in section "*Power Supply*".

In this section the detailed distribution of dedicated power supply pins for certain I/O modules is provided. This covers different power supply pins that are indicated by different supply pin naming or different prefix. It covers also the supply of I/O modules that are supplied by several power supply pins that differ only for the suffix.

Pins having different suffix but same naming with same prefix are connected among each other but may have slightly different characteristic to parts of the I/O module. This is especially valid for devices with BGA packages, where the bonding between the die and the balls does not differ for the suffix. Nevertheless the electrical specification for each I/O pin does refer to a special power supply pin pair indicated by the complete naming including the suffix.

CAUTION

As not denoted otherwise this document neglects suffixes for power supply pins with same functions that can be treat as equal.

This document provides in the following sections;

- **Section 1.4, Absolute Maximum Ratings**
- **Section 1.5, General Operating Conditions**
- **Section 1.6, General IO Characteristic**

the voltage ranges of the power supply pins and port pins.

There the alias XyVCCn is often used to keep the operating condition description generic. Depending on the pin group supply the alias has to be replaced by the port buffer power.

1.1.2 Port Pins

A port buffer consists out of an output and input buffer with special features. Below abbreviation is used for the following port buffer tables.

1.1.2.1 Output Table Abbreviations

(1) Buffer Power Supply

Describes to which power supply pin pair the pin is connected.

(2) IOHold

The availability of this function to each pin is marked with “x” in the associated column. For pins without this functionality the field is empty. In IOHOLD mode the I/O buffer maintains the level and drive strength it was in before entering this mode.

(3) Output

There exist different output buffer types.

- GP: General purpose output buffer.
  - Used for all general purpose I/O functions.
  - Provides frequency control option.
- HD: High drivability output buffer.
  - With high drive capability that is mainly used to drive stepper motors.
- AN: Analog output buffer.
  - Output buffer used w/ analog input buffer for A/D Converter.

The characteristic of each type is described in **Section 1.6, General IO Characteristic**.

The availability of the buffers to each pin is marked with “x” in the associated column. For pins without this functionality the field is empty.

In case the buffer is in addition initial activated by RESET an “R” or “L” is used instead of the “x”.

The “L” is used if the output direction of an output buffer is initial active low “R” is used instead of the “x”.

(4) Open Drain

The availability of the open drain emulation to each pin is marked with “x” in the associated column. For pins without this functionality the field is empty.

In case the open drain emulation is in addition initial activated by RESET an “R” is used instead of the “x”.

1.1.2.2 Input Table Abbreviations

(1) TriState

While this feature is active the input and output buffers are disabled (all PODCn_m = 1, PIBCn_m = 0). The ports enter high impedance status (HiZ). Thus these ports can be left unconnected, if they are not used.

A “R” in this column indicates that the output and input/output port is initial disabled by RESET and enters high impedance status (HiZ).

A “x” indicates that the feature is programmable during operation.

(2) Input

The characteristic of each type is described in **Section 1.6, General IO Characteristic** and can be selected by port control registers.

- CMOS1
- (LV)TTL
- Schmitt1
- Schmitt2
- Schmitt4

Not all input characteristics are available for each input port.

The availability of the input characteristic to each pin is marked with “x” in the associated column. For pins without this functionality the field is empty.

In case the input characteristic is in addition initial activated by RESET an “R”

is used instead of the “x”.

(3) Resistor

For input pins an internal pull-up (PU) and pull-down (PD) resistor can be selected. The availability is marked with “x” and “R” in the same meaning as above.

(4) Reset State

The output level status in case of active MCU reset.

“Z” means high impedance (output not driven).

“L” means low level (actively driven output).

(5) Drive Control

For output pins the drivability can be selected by PDSCn registers (=0 low speed, =1 high speed). In case the output drivability can be selected for a port it is indicated by “x” marking.

1.1.3 Pin Information for D1S1

Table 1.1 Pin Information for D1S1

Pin	Buffer Power Supply	Output				Open Drain	Tri State	Input					Resistor			Reset State	Drive Control
		GP (Slow)	GP (fast)	HD	AN			CMOS1	Schmitt1	Schmitt2	Schmitt4	TTL	PU	PD	IO-Hold		
RESETZ	EV_{CC}	×				×				×						L	
FLMD0	EV_{CC}								×				×	R		Z	
PWRCTL	EV_{CC}	×														L	
PWRGD	EV_{CC}								x							Z	
JP0_0	EV_{CC}	×				×	×		R		×	×	×	×		Z	
JP0_1	EV_{CC}	×				×	×				×		×	×		L	× *2
JP0_2	EV_{CC}	×				×	×		R		×	×	×	×		Z	
JP0_3	EV_{CC}	×				×	×				R	×	×	×		Z	
JP0_4	EV_{CC}	×				×	×				R	×	×	R		Z	
JP0_5	EV_{CC}	×				×	×				×		×	×		Z	× *2
P0	EV_{CC}	×	×			×	×		R		×	×	×	×	×	Z	×
P1	$B0V_{CC}$	×	×			×	×	×	R		×		×	×	×	Z	×
P3	$B1V_{CC}$	×	×			×	×	×	R		×		×	×	×	Z	×
P10	$A0V_{CC}$	×			×	×	×	×						×		Z	
P11	$A0V_{CC}$	×			×	×	×	×						×		Z	
P16	$ISMV_{CC}$	×		×		×	×	×	R		×				×	L	×
P17[3:0]	$ISMV_{CC}$	×		×		×	×	×	R		×				×	L	×
P17[6:4]	$ISMV_{CC}$	×	×			×	×	×	R		×		×	×	×	Z	×
P21	$B5V_{CC}$	×	×			×	×	×	R		×		×	×		Z	×
P42	$B0V_{CC}$	×	×			×	×	×	R		×		×	×	×	Z	×
P44	$B5V_{CC}$	×	×			×	×	×	R		×		×	×	×	Z	×
P45	$B5V_{CC}$	×	×			×	×	×	R		×		×	×	×	Z	×

Note 1. P16/P17[3:0] are driven by HD capability at Reset State.

Note 2. JP0_1/JP0_5 has JPDSC. However, AC/DC spec cover slow mode only.

1.2 Classification of Testing

Besides testing the specified parameters directly or indirectly at mass production state there is also the method of special product characterization and design simulation. Such parameters are marked in the classification tag column “CT” of each electrical parameter table with the associated classification tag.

Table 1.2 Parameter Classifications

Classification Tag		
Abbr	**Tag Name**	**Tag Description**
PC	Product Characterization	Those parameters are achieved by device characterization by measuring a statistically relevant sample size across process variations.
DS	Design Simulation	Those parameters are derived from simulations.

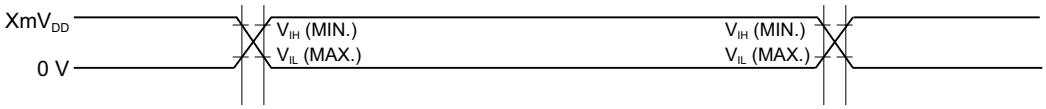
1.3 General Measurement Conditions

As not otherwise denoted the general measurement condition for testing are

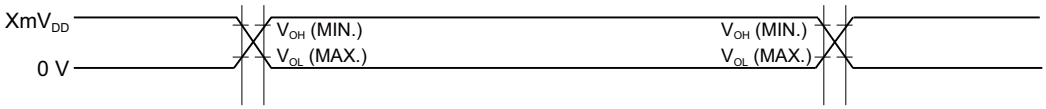
Condition: T_J = –40 to +T_{Jmax}
VSS = OSCVSS = REGnVSS = EVSS = BnVSS = ISMVSS = ZPDVSS = A0VSS = = 0 V

1.3.1 AC Characteristic Measurement Condition

(1) AC Test Input Measurement Points



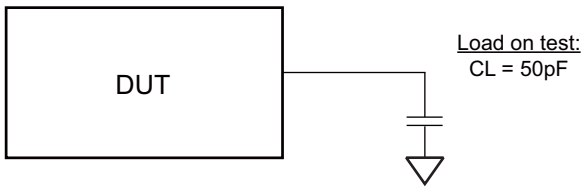
(2) AC Test Output Measurement Points



CAUTIONS

1. If not other denoted output timings are not valid for open drain setting.
2. If not other denoted input timings are valid for CMOS1 level.
   - Using the Schmitt 1/2/4 input characteristics results in a different delay time. If Schmitt 1/2/4 is used, the difference of the propagation delay timing to CMOS1 has to be added. For port input propagation delay timing please refer to Port Input Characteristics.

(3) Load Conditions



NOTES

1. As not otherwise denoted the standard load condition for testing is
   - 1 nF for Intelligent stepper motor driver (HD type)
   - 50 pF for all lower speed port buffer (GP type in slow mode)
   - 30 pF for video and SFMA I/O ports. (GP type in fast mode)
2. For critical AC timing specifications (mostly of interfaces with crucial round- trip delay calculations), please refer to the individual sections and check under which test conditions the individual AC specifications are valid.

1.4 Absolute Maximum Ratings

1.4.1 Definition of Absolute Maximum Ratings

Absolute maximum ratings are values of voltage, current, temperature, power dissipation etc., which must not be exceeded at any time, otherwise deterioration or destruction of the device may take place. Maximum values and limits given in this document should be taken into consideration anytime when using the device.

(1) Maximum Temperature Ratings

Specifies the absolute maximum limitation of operating and storage temperature.

NOTE

The device's function is not guaranteed outside of the specified maximum temperature ratings.

(2) Maximum Voltage Ratings

Specifies the absolute maximum limitation of supply and input voltages.

NOTE

The device's function is not guaranteed outside of the specified operating range and below the specified maximum voltage ratings.

(3) Maximum Current Ratings

Specifies the absolute maximum limitation of input and output currents.

1.4.2 Thermal Characteristics

Table 1.3 Thermal Characteristics

Parameter	Symbol	Condition	T_{Jmin}	TYP.	T_{Jmax}	Unit
Storage temperature	T_{STGB}	D1S1	–55		150	°C
Operating temperature	T_{OPR}	D1S1	–40		150	°C

1.4.3 Supply Voltages

Condition: T_j = –40 to +T_{Jmax}
REG0VSS = OSCVSS = EVSS = REG1VSS = BnVSS = ISMVSS = ZPDVSS = A0VSS = 0 V

Table 1.4 VCC / VDD Data

Parameter	Symbol*1,*2	Condition	Ratings	Unit
Always-On-Area	REG0VCC		–0.5 to 6.5	V
	OSCVCC		–0.5 to 6.5	V
	EVCC		–0.5 to 6.5	V
System	REG1VCC		–0.5 to 6.5 V	V
Internal voltage regulator Ports	REG0C, REG1C*3		–0.5 to 1.8	V
	B0VCC		–0.5 to 6.5	V
	B1VCC		–0.5 to 6.5	V
	B5VCC		–0.5 to 6.5	V
Stepper Motor Controller, Zero point detection circuit	ISMVCC		–0.5 to 6.5	V
	ZPDVCC		–0.5 to 6.5	V
A/D Converter	A0VCC	A0VCC>=ISOVDD	–0.5 to 6.5	V
	A0VREF	A0VREF<= A0VCC	–0.5 to 6.5	V

Note 1. As long as not otherwise noted this specification does not differ between pins with different suffix for the symbol.
Note 2. The symbol reflects all supplies within D1x. Therefore not each symbol is available for each product.
Note 3. These pins are for special use only and should not be used for other connections than specified. Pins are operated with the internal generated core voltage.

Table 1.5 VSS Data

Parameter	Symbol*1,*2	Condition	Ratings	Unit
Always-On-Area	REG0VSS	reference ground potential	0	V
	OSCVSS		–0.5 to 0.5	V
	EVSS		–0.5 to 0.5	V
System	REG1VSS		–0.5 to 0.5	V
Ports	B0VSS		–0.5 to 0.5	V
	B1VSS		–0.5 to 0.5	V
	B5VSS		–0.5 to 0.5	V
Stepper Motor Controller, Zero point detection circuit	ISMVSS		–0.5 to 0.5	V
	ZPDVSS		–0.5 to 0.5	V
A/D Converter	A0VSS		–0.5 to 0.5	V

Note 1. As long as not otherwise noted this specification does not differ between pins with different suffix for the symbol.
Note 2. The symbol reflects all supplies within D1x. Therefore not each symbol is available for each product.

1.4.4 Port Voltage

Condition: T_j = –40 to $+T_{Jmax}$

Table 1.6 Port Input Voltage

Parameter		Symbol[*1,*2]	Condition	Ratings	Unit
Input voltage	Pins supplied by EVCC	V_{I0}	V_{I0} < EVCC + 0.5 V	–0.5 to 6.5	V
	Pins supplied by BnVCC	V_{I1}	V_{I1} < BnVCC + 0.5 V	–0.5 to 6.5	V
	Pins supplied by ISMVCC	V_{I6}	V_{I6} < ISMVCC + 0.5 V	–0.5 to 6.5	V
	Pins supplied by A0VCC	V_{I7}	V_{I7} < A0VCC + 0.5 V	–0.5 to 6.5	V

Note 1. The characteristics of the alternative-function pins are the same as those of the port pins unless otherwise specified.

Note 2. The symbol reflects all supplies within D1x. Therefore not each symbol is available for each product.

1.4.5 Port Currents

The port currents describe the allowed currents that can be sourced from / sunken into a port pin respectively a port pin supply group.

Condition: T_j = –40 to +T_{Jmax}
REG0VSS = OSCVSS = EVSS = REG1VSS = BnVSS = ISMVSS = ZPDVSS = A0VSS = 0 V

CAUTION

The currents in the customer's application must not exceed the absolute maximum current ratings as specified in **Table 1.7, Low Level Output Current** and **Table 1.8, High Level Output Current** below.

For the calculation of the total power dissipation of a device (Ptot) also the power consumption of the IO pins (PIO) has to be considered. PIO is dependent on the customer's application. Therefore, it has to be taken care that with the resulting PIO the Ptot does not exceed the given limits of T_{Jmax}.

Table 1.7 Low Level Output Current

Parameter	Symbol[*1]	Condition	Average	MAX.	Unit
Pins supplied by EVSS	IOL0	1pin	—	10	mA
		Sum of all absolute IOL0 of pins supplied by same supply pin pair	—	60	mA
Pins supplied by B0VSS	IOL1	1pin	—	10	mA
		Sum of all absolute IOL1 of pins supplied by same supply pin pair	—	60	mA
Pins supplied by B1VSS	IOL2	1pin	—	10	mA
		Sum of all absolute IOL2 of pins supplied by same supply pin pair	—	60	mA
Pins supplied by B5VSS	IOL6	1pin	—	10	mA
		Sum of all absolute IOL6 of pins supplied by same supply pin pair	—	60	mA
Pins supplied by ISMVSS (PDSCn = 0)	IOL11	1 pin	—	10	mA
		Sum of all absolute IOL11 of pins supplied by same supply pins	—	60	mA
Pins supplied by ISMVSS (PDSCn = 1)	IOL11	1 pin (T_j = –40°C)	52	60	mA
		1 pin (T_j = 25°C)	39	45	mA
		1 pin (T_j = 125°C)	32	40	mA
		1 pin (T_j = 150°C)	30	38	mA
		Sum of all absolute IOL11 of pins supplied by all supply pins (T_j = –40°C)	441		mA
		Sum of all absolute IOL11 of pins supplied by all supply pins (T_j = 25°C)	351		mA
		Sum of all absolute IOL11 of pins supplied by all supply pins (T_j = 125°C)	288		mA
		Sum of all absolute IOL11 of pins supplied by all supply pins (T_j = 150°C)	270		mA
Pins supplied by A0VSS	IOL12	1 pin	—	10	mA
		Sum of all absolute IOL12 of pins supplied by same supply pin pair	—	60	mA

Note 1. The characteristics of the alternative-function pins are the same as those of the port pins unless otherwise specified.

Table 1.8 High Level Output Current

Parameter	Symbol*1	Condition	Average	Peak	Unit
Pins supplied by EVCC	IOH0	1 pin	—	–10	mA
		Sum of all absolute IOH0 of pins supplied by same supply pin pair	—	–60	mA
Pins supplied by B0VCC	IOH1	1 pin	—	–10	mA
		Sum of all absolute IOH1 of pins supplied by same supply pin pair	—	–60	mA
Pins supplied by B1VCC	IOH2	1 pin	—	–10	mA
		Sum of all absolute IOH2 of pins supplied by same supply pin pair	—	–60	mA
Pins supplied by B5VCC	IOH6	1 pin	—	–10	mA
		Sum of all absolute IOH6 of pins supplied by same supply pin pair	—	–60	mA
Pins supplied by ISMVCC (PDSCn = 0)	IOH11	1 pin	—	–10	mA
		Sum of all absolute IOH11 of pins supplied by same supply pins	—	–60	mA
Pins supplied by ISMVCC (PDSCn = 1)	IOH11	1 pin (T_j = –40°C)	–52	–60	mA
		1 pin (T_j = 25°C)	–39	–45	mA
		1 pin (T_j = 125°C)	–32	–40	mA
		1 pin (T_j = 150°C)	–30	–38	mA
		Sum of all absolute IOH11 of pins supplied by all supply pins (T_j = –40°C)	–441		mA
		Sum of all absolute IOH11 of pins supplied by all supply pins (T_j = 25°C)	–351		mA
		Sum of all absolute IOH11 of pins supplied by all supply pins (T_j = 125°C)	–288		mA
		Sum of all absolute IOH11 of pins supplied by all supply pins (T_j = 150°C)	–270		mA
Pins supplied by A0VCC	IOH12	1 pin	—	–10	mA
		Sum of all absolute IOH12 of pins supplied by same supply pin pair	—	–60	mA

Note 1. The characteristics of the alternative-function pins are the same as those of the port pins unless otherwise specified.

1.5 General Operating Conditions

1.5.1 Requirements for External Power Supply Connections

The customer has to ensure a low resistive connection of all XyVSS pins on the PCB. This specification denotes ground supply pins as:

- VSS = OSCVSS = REGnVSS = EVSS = BnVSS = ISMVSS = ZPDVSS = A0VSS = 0 V

The customer has to ensure a low resistive connection of all same XyVCC pins on the PCB. This specification denotes power supply pins as:

- REGnVCC, REG0C, OSCVCC, EVCC, BnVCC, ISMVCC, A0VCC, A0VREF, ZPDVCC

1.5.2 Power Area Definition:

- AWO = Powered
  - REG0VCC = Powered
  - EVCC = Powered
- ISO = powered
  - REG1VCC = Powered

NOTE

"Powered" means to supply a voltage according to supply voltage range specified in **Section 1.5.7, Supply Voltage**.

1.5.3 Power-Up/-Down Ramp

For a proper start-up (power-up) and switch-off (power-down) of the device it is mandatory that the customer applies an ext. system supply voltage (XyVCC), with a ramp that is equal or slower than specified below.

- XyVCC means each power domain

Table 1.9 Power-up Restrictions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
REG0VCC/EVCC ramp-up time	T_{pupr0}	0 V to 3.1 V	0.00		500	V/ms
REG1VCC ramp-up time		0 V to 3.1 V	0.00		400	V/ms
POC0RESET release to PWRCTL assert					100	µs
OSCVCC ramp-up after or equal REG0VCC	T_{puosc}	0 V to 3.0 V	0.0			µs
A0VCC/A0VREF ramp-up before REG1VCC	T_{pud1}	0 V to 3.0 V	0.0			µs
REG1VCC ramp-up after PWRCTL	T_{pud3}	0 V to 3.0 V	0.0			µs
A0VCC/BnVCC/ISMVCC/ZPDVCC ramp-up after REG0VCC	T_{pudio}	0 V to 3.0 V	0.0			µs
PWRGD ramp-up after REG1VCC	T_{pgdu}	Low to High	0.0			µs
Power-up delay	T_{pudly}	POC0RES			0.8 (HS IntOSC)	ms
		except POC0RES			0.5 (HS IntOSC)	ms
					1.2 (LS IntOSC)	ms
PWRGD pulse width	T_{wpg}		10.0			µs
PWRCTL assert from wake-up trigger receive	T_{pctl}		10.0		100	µs

Table 1.10 Power-down Restrictions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
REG0VCC/EVCC shutdown time	T_{pdpr0}	3.0 V to 0 V	0.00		500	V/ms
REG1VCC shutdown time		3.0 V to 0 V	0.00		400	V/ms
OSCVCC shutdown before REG0VCC	T_{pdosc}	3.0 V to 0 V	0.0			µs
A0VCC/A0VREF shutdown from PWRCTL	T_{pdd1}	3.0 V to 0 V	0.0			µs
REG1VCC shutdown after PWRCTL	T_{pdd3}	3.0 V to 0 V	0.0			µs
A0VCC/BnVCC/ISMVCC/ZPDVCC shutdown before REG0VCC	T_{pddio}	3.0 V to 0 V	–10.0			ms

When PWRGD become to fail (low), then internal reset asserted. But, REG1VCC need to keep >2.7v during following period.

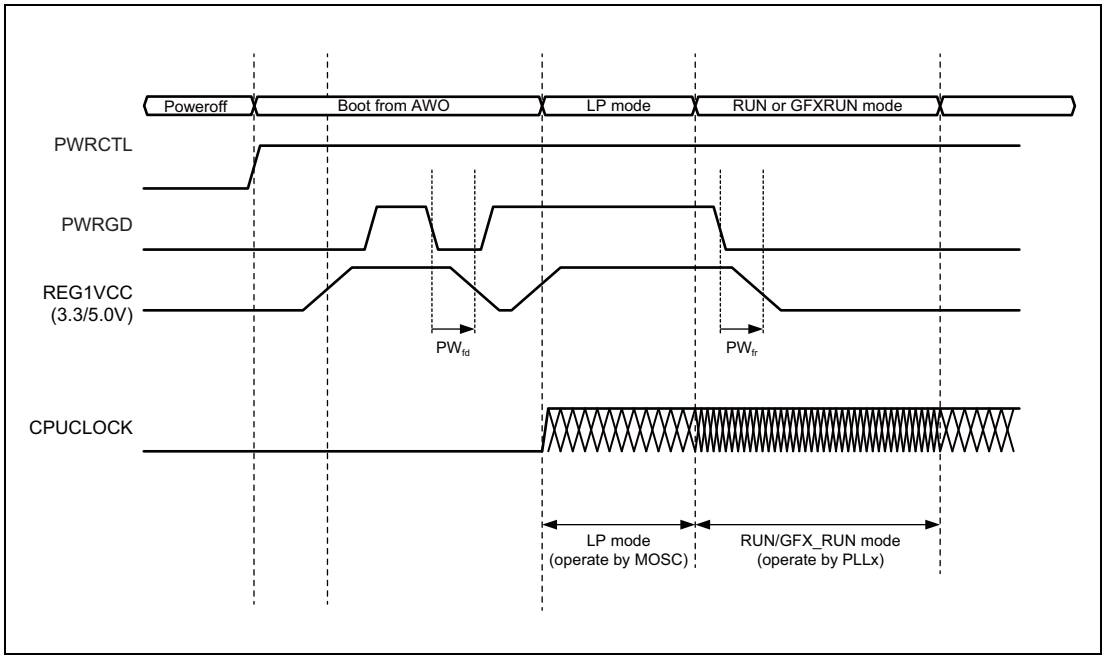


Figure 1.1 PWRGD/REG1VCC Failure

Table 1.11 Power Supply Failure

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
PWRGD shutdown to REG1VCC fail	PW_{fr}	LP/RUN mode	0			µs
	PW_{fd}	Except LP/ RUN mode	0			µs

Note: PWRGD shutdown to REG1VCC fail is not relevant in case MCU successfully entered the deep-stop mode. For this case please refer to **Figure 1.4**.

Table 1.12 Power Supply Ripple Specs

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Ripple of all supply	R_{rpl}		–10		10	%
Maximum rating of all slope	R_{slp}				100	V/s

1.5.4 Power-Up/Down Sequences of External Supply Voltages

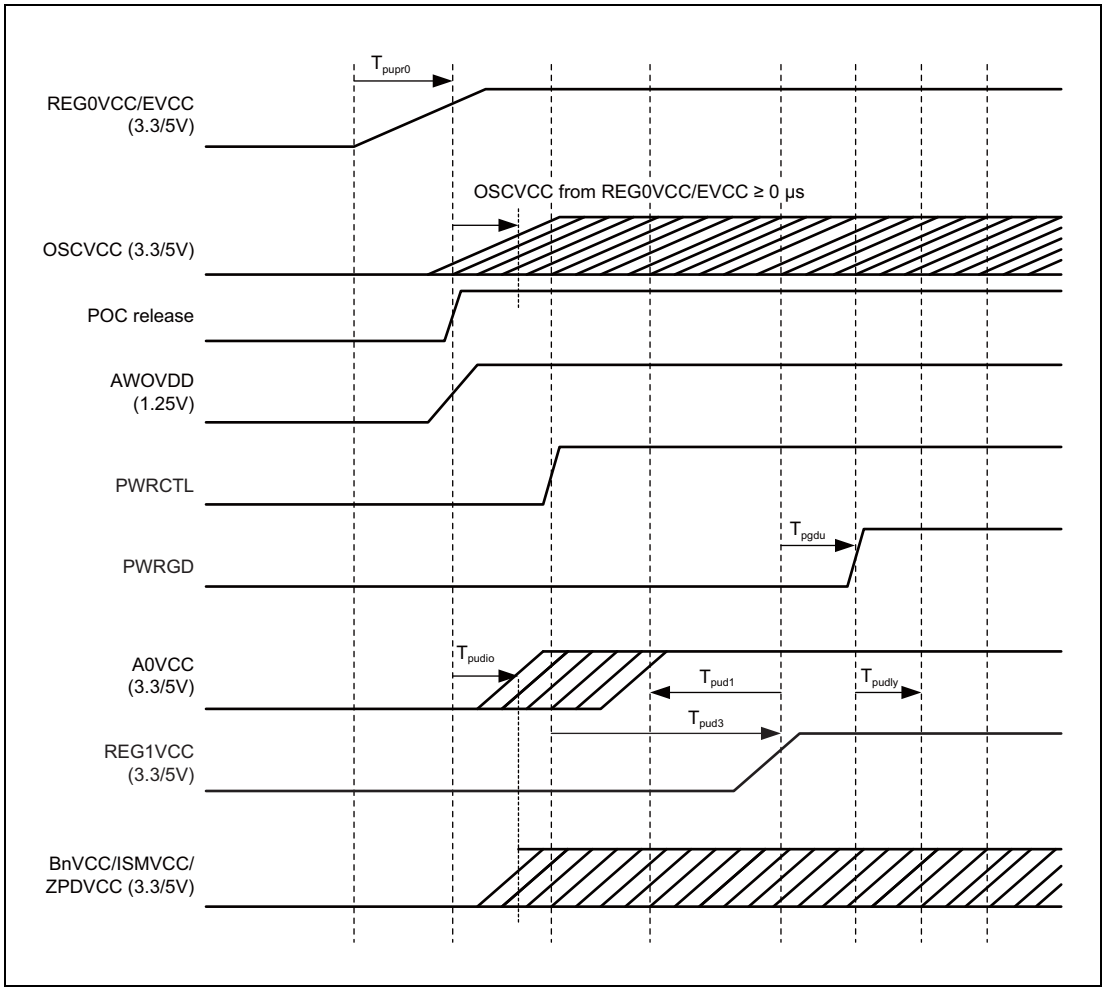


Figure 1.2 Power-up Sequence

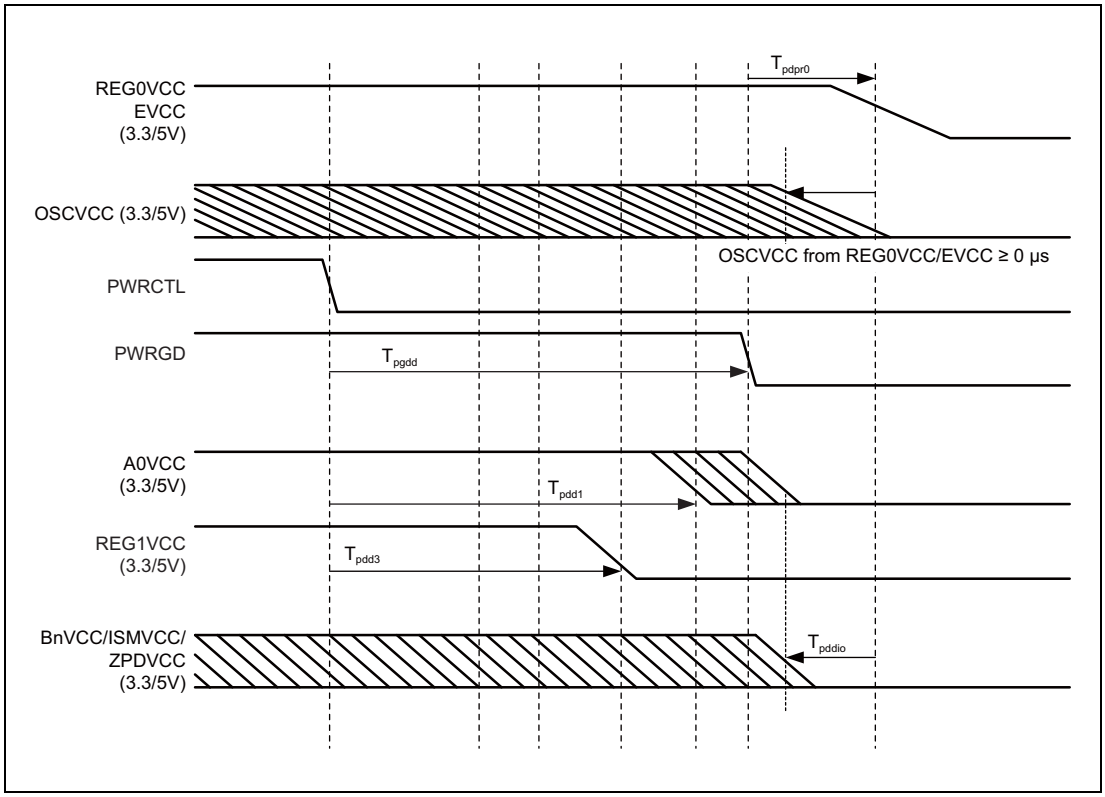


Figure 1.3 Power-down Sequence

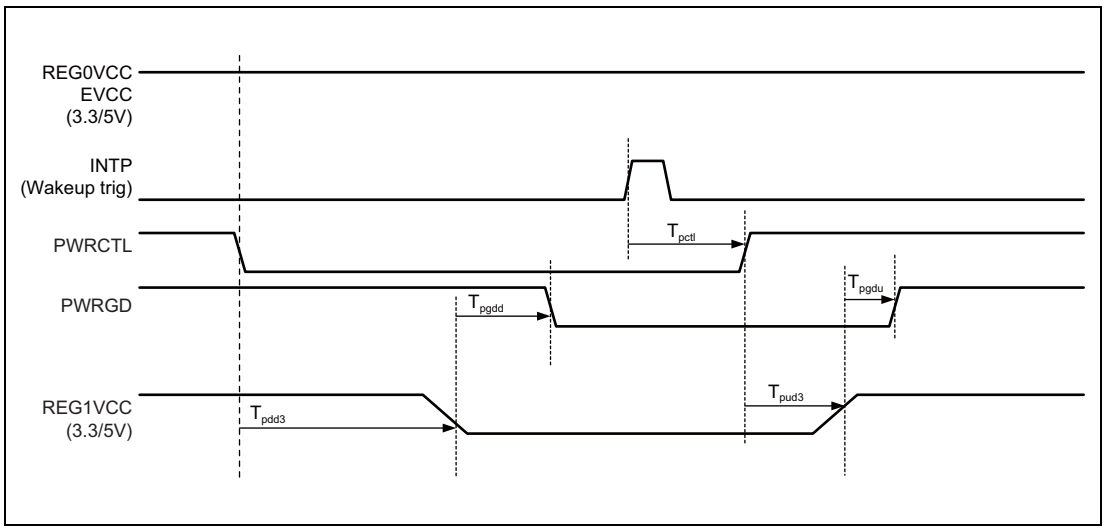


Figure 1.4 DeepSTOP Enter/Exit Sequence

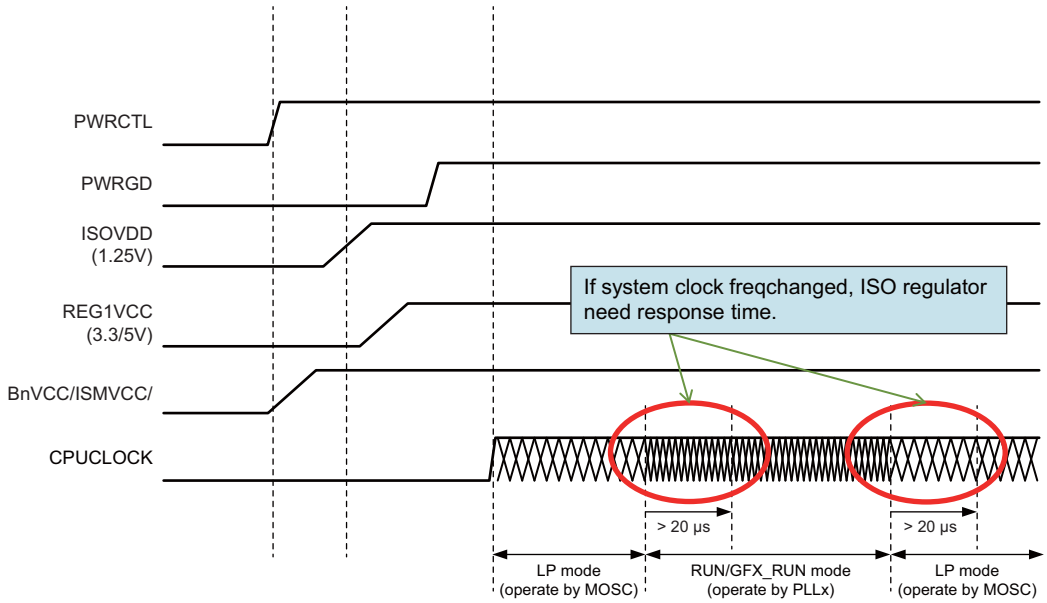
NOTE

- When REG0VCC is supplied, it is possible to supply REG1VCC, regardless of the PWRCTL signal state.
- In case of successful DeepSTOP entry (when MCU has set PWRCTL = L), there is no restriction for PWRGD shutdown timing. Because of that a value for the parameter T_{pgdd} is not specified.

Please refer to the **Section 1.13.2, Stand-by Current Consumption** and consider the leakage currents of active domain for this case.

1.5.5 Clock Source Change Behavior

D1x must keep the blank time when PLL on/off switching (more than 20 µs).



Note: Changing of one or all of this clock tree registers below must not be done again within a period of 20 µs after last change.

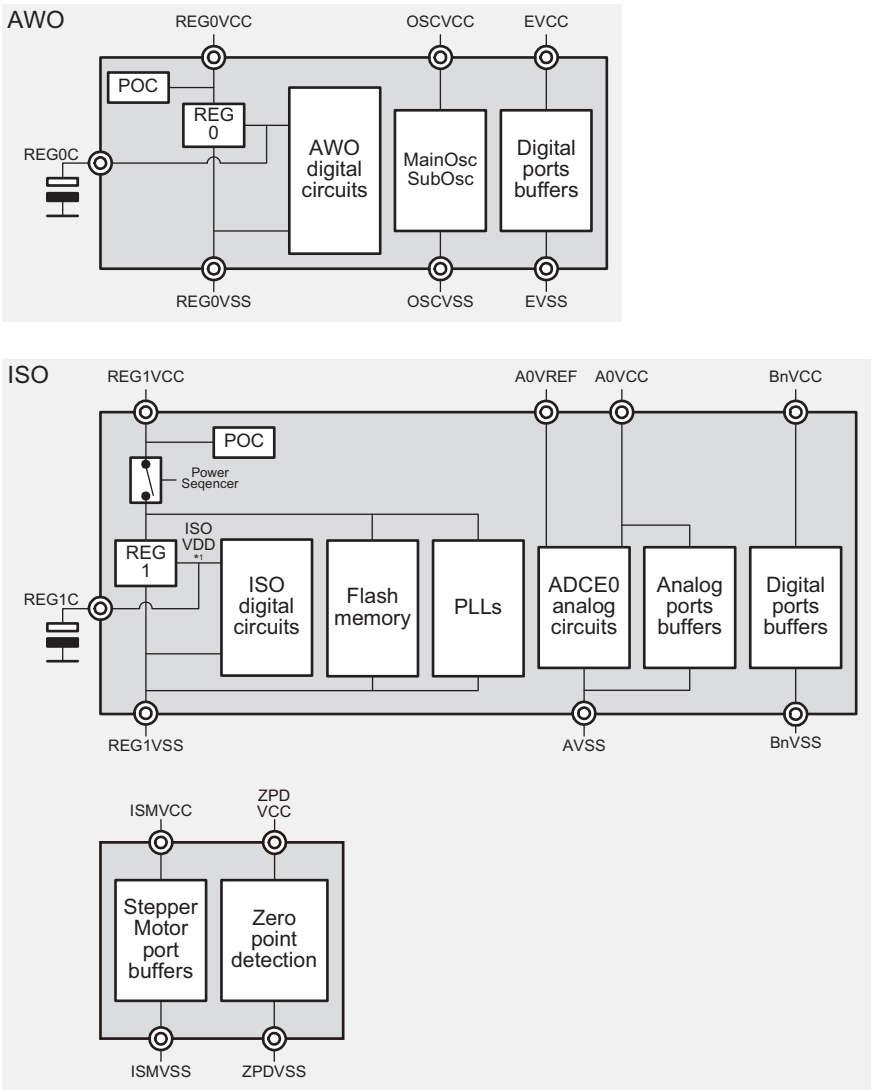
a) stop mask change of CKSC_IPLL0S_CTL
b) stop mask change of CKSC_IPLL1S_CTL
c) clock selector change of CKSC_ICPUCLKS_CTL
d) clock divider change of CKSC_ICPUCLKD_CTL
e) stop mask change of CKSC_ISDRBS_CTL
f) PLL0 dis-/enable trigger of PLL0E
g) PLL1 dis-/enable trigger of PLL1E

Figure 1.5 Power-down Sequence

1.5.6 Core Voltage Supplies

The core voltage supply has to be provided to the AWO and to the ISO area separately.

AWO area and ISO are utilizing one on-chip regulator each. (AWO:REG0VCC, ISO:REG1VCC).



Note 1. ISOVDD is also input to the A/D Converter channel 20 for supply voltage monitoring purposes.

Figure 1.6 Voltage Supply

1.5.7 Supply Voltage

Condition: T_j = –40 to $+T_{Jmax}$

Table 1.13 VCC Data

Parameter	PO[*1]	Symbol[*2]	Condition	MIN.	TYP.	MAX.	Unit
System	No	REG0VCC[*3]		2.7		5.5	V
	Yes	REG1VCC		2.7		5.5	V
	Yes	OSCVCC		2.7		5.5	V
Ports	No	EVCC[*7]		2.7		5.5	V
	Yes	BnVCC		2.7		5.5	V
	Yes	ISMVCC		2.7		5.5	V
A/D Converter[*5]	Yes	A0VCC[*6]		2.7		5.5	V
	Yes	A0VREF[*6]		2.7		5.5	V
ZPD Comparator[*5]	Yes	ZPDVCC[*6]		2.7[*4]		5.5	V

Note 1. PO = Power Off possibility: Under certain conditions some power supply pins are allowed to be unprovided in low power operating modes. This column informs about the principle allowance (Yes/No). However the details of supply voltage dependencies have to be obtained.

Note 2. As long as not other noted this specification does not differ between pins with different suffix for the symbol.

Note 3. Full device operation is only available, when the supply voltage is above the POC0 threshold voltage. The device may stop operation due to a $\overline{\text{RESET}}$ condition generated by the POC0, if the supply voltage drops below the POC0 threshold voltage.

Note 4. ZPD operation only 4.5 to 5.5 V

Note 5. 2.7 to 3.0 V range only specified DC characteristics.

Note 6. D1x should be keep this relation: A0VCC ≥ ISOVDD (ISOVDD is generated by REG1VCC (Except D1M2(H)), A0VREF ≤ A0VCC

Note 7. EVCC should be kept same voltage level with REG0VCC.

1.5.8 Overload Condition (Injected Current)

The overload condition describes the behaviour in case of current injection to the port pins.

Condition: T_j = –40°C to +T_{Jmax}, XyVCC = 3.0 to 5.5 V

Table 1.14 Overload Current

Parameter		Symbol	Condition	Ratings*1	Unit
Overload Current*2 V_{IN} > VCC V_{IN} < VSS	Pins supplied by EVCC	I_{INJPM} I_{INJNM}	1 pin	±2	mA
			Sum of all absolute I_{INJPM} + I_{INJNM} of pins supplied as a group*3	|50|	mA
	Pins supplied by B0VCC		1 pin	±2	mA
			Sum of all absolute I_{INJPM} + I_{INJNM} of pins supplied as a group*3	|50|	mA
	Pin supplied by B1VCC		1 pin	±2	mA
			Sum of all absolute I_{INJPM} +I_{INJNM} of pins supplied as a group*3	|50|	mA
	Pin supplied by B5VCC		1 pin	±2	mA
			Sum of all absolute I_{INJPM} + I_{INJNM} of pins supplied as a group*3	|50|	mA
	Pin supplied by ISMVCC		1 pin	±2	mA
			Sum of all absolute I_{INJPM} + I_{INJNM} of pins supplied as a group*3	|50|	mA
	Pin supplied by A0VCC		1 pin	±3	mA
			Sum of all absolute I_{INJPM} + I_{INJNM} of pins supplied as a group*3	|10|	mA

Note 1. The total current may be limited further by the total power dissipation.

Note 2. Be sure not to exceed the absolute maximum ratings (Max. value) of each supply voltage.

Note 3. The total overload current must be within the output current.

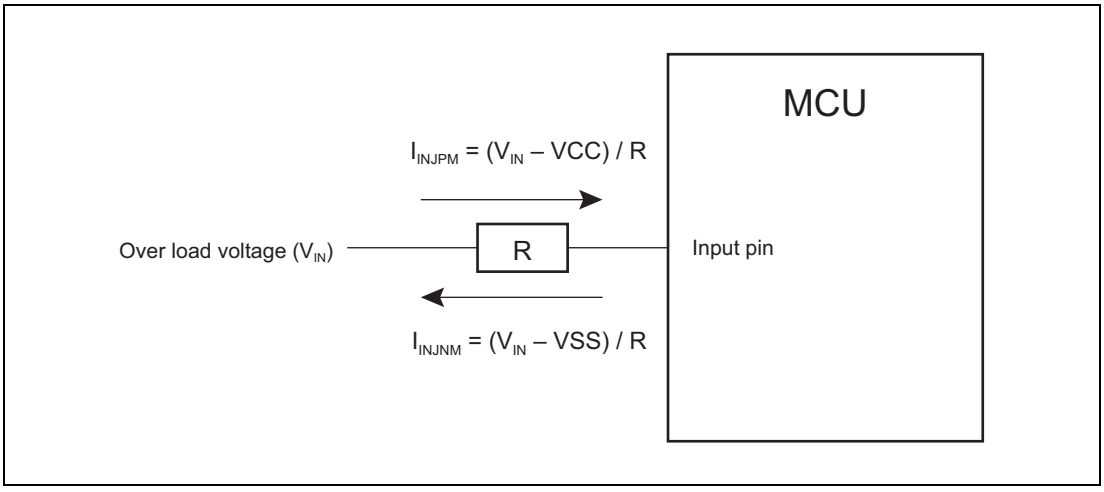


Figure 1.7 Definition of I_{INJPM} and I_{INJNM}

1.5.9 Operating Conditions

1.5.9.1 CPU Clock

Table 1.15 CPU Clock Frequency

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
D1S1	*1				120	MHz

Note 1. The center frequency is mentioned. SSCG margin needs to be added.

1.5.9.2 Module Clock

(1) APB Modules Clock

All modules (macros) that are connected though APB peripheral bus, and D1x has 3 type APB bus clocks.

(a) C_ISO_PCLK

Basically D1x uses synchronous APB bus clock with CPU clock

Table 1.16 C_ISO_PCLK Modules Clock Frequency

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
D1S1	f_{max},APB*1				60	MHz

Note 1. The center frequency is mentioned. SSCG margin needs to be added.

(b) CLKJIT

Communication macro uses fixed frequency CLKJIT clock. It asynchronous with CPU clock and use SSC (Spread Spectrum Clocking).

Table 1.17 CLKJIT Modules Clock Frequency

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
D1x:	f_{max},JIT*1				80	MHz

Note 1. The center frequency is mentioned. SSCG margin needs to be added.

(c) CLKFIX

Audio and timer macro uses fixed frequency CLKFIX clock. It asynchronous with CPU clock and use non-SSC (Spread Spectrum Clocking).

Table 1.18 CLKFIX Modules Clock Frequency

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
D1x:	f_{max},FIX				80	MHz

(2) XC bus Modules Clock

Table 1.19 XC Modules Clock Frequency

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
D1S1	f_{max},XC bus*1				60	MHz

Note 1. The center frequency is mentioned. SSCG margin needs to be added.

1.5.10 Oscillator Characteristics

1.5.10.1 Main Oscillator

A ceramic or crystal resonator can be connected to the main clock input pins as shown in **Figure 1.8, Recommended Main Oscillator Circuit**.

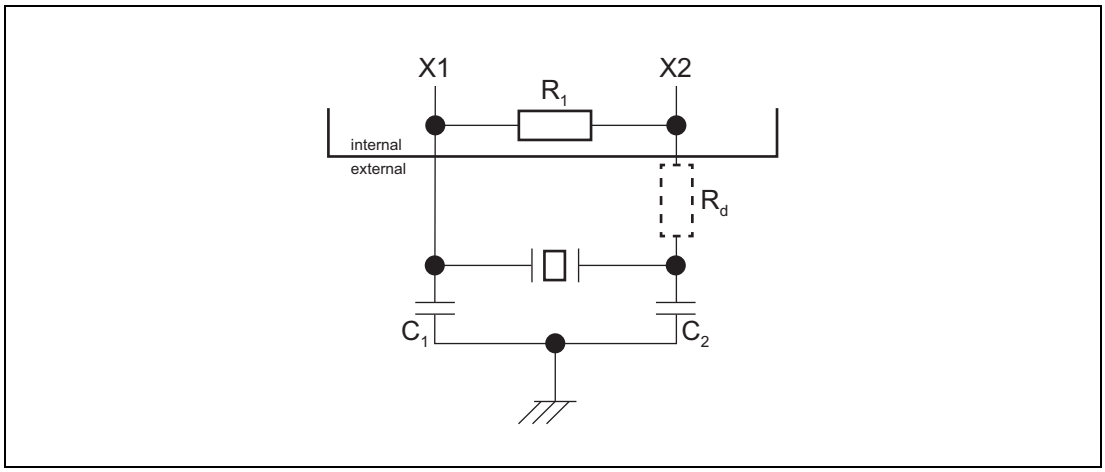


Figure 1.8 Recommended Main Oscillator Circuit

CAUTION

Values of C1, C2 and Rd depend on the used ceramic or crystal resonator and must be specified in cooperation with ceramic or crystal resonator manufacturer.

(1) Main Oscillator Characteristics

Condition: T_j = –40°C to +T_{Jmax}
OSCVCC = 3.0 to 5.5 V
Typ condition indicate following condition
- T_j = 25°C

Table 1.20 Main Oscillator Characteristics

Parameter	CT	Symbol	Condition	MIN.	TYP.	MAX.	Unit
X1, X2 Oscillator Frequency		f_{OSC}		7.2		16	MHz
Oscillator stabilization time	DS	T_{OST}*1				6.0	ms

Note 1. T_{OST} depends on the external crystal. Shorter timing might be found by evaluation.
Note 2. OSCVCC set to 5.5 V for MAX. value.
Note 3. OSCVCC set to 3.6 V for MAX. value.
Note 4. OSCVCC operation at 3.3 V is prohibited at AMPSEL=11_B.

1.5.10.2 Sub Oscillator

A crystal resonator can be connected to the sub clock input pins as shown in **Figure 1.9, Recommended Sub Oscillator Circuit**.

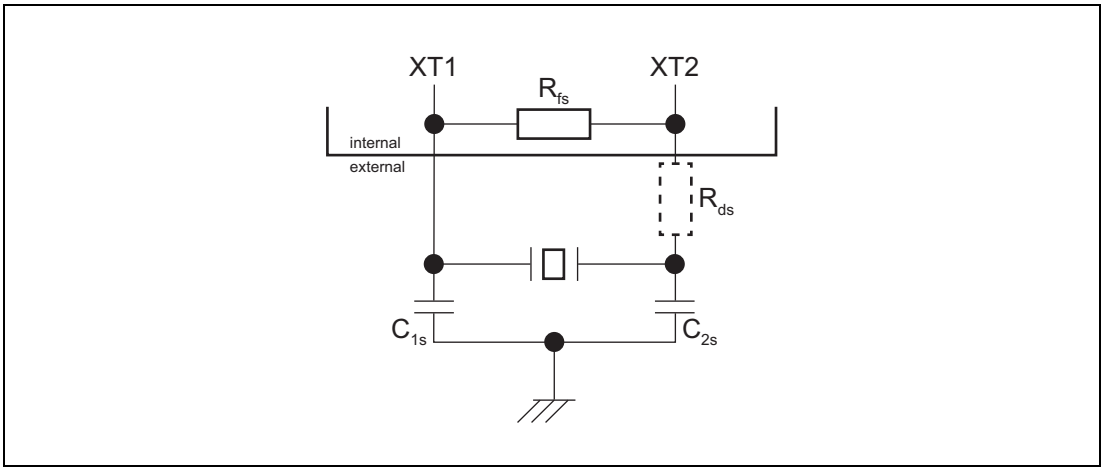


Figure 1.9 Recommended Sub Oscillator Circuit

CAUTION

Values of C_{1s}, C_{2s} and R_{ds} depend on the used crystal and must be specified in cooperation with crystal manufacturer.

(1) Sub Oscillator Characteristics

Condition: T_j = –40°C to +T_{Jmax}

Table 1.21 Sub Oscillator Characteristics

Parameter	CT	Symbol	Condition	MIN.	TYP.	MAX.	Unit
XT1,XT2 Oscillator Frequency		f_{SOSC}		32	32.768	35	kHz
Sub oscillator stabilization time		T_{SOST}*1				2.0	s
Current	PC	I_{DDSOSC}			2		µA

Note 1. T_{SOST} depends on the external crystal. Shorter timing might be found by evaluation.

1.5.10.3 Internal Oscillator Characteristics

Condition: T_j = –40°C to +T_{Jmax}

Table 1.22 Internal Oscillator (240 kHz) Characteristics

Parameter	CT	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Output Frequency		f_{240}		220	240	260	kHz
Oscillation Stabilization Time	DS*1	$T_{240STAB}$				60	µs
Current	PC	$I_{DDLOSCL}$	REG0VCC = 5.0 V		5		µA

Note 1. Not tested in production. Specified by design.

Table 1.23 Internal Oscillator (8 MHz) Characteristics

Parameter	CT	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Output Frequency		f_8		7.200	8.00	8.800	MHz
Oscillation Stabilization Time	DS*1	T_{8STAB}				15	µs
Current	PC	$I_{DDLOSCH}$	REG0VCC = 5.0 V		30		µA

Note 1. Not tested in production. Specified by design.

1.5.10.4 PLL Characteristics

Table 1.24 PLL0 Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
PLL input frequency	f_{PLLkIN}		7.2		16	MHz
PLL output frequency	$f_{PLLkCLK}$				508	MHz
PLL output period jitter		w/o SSCG	–100.0		100.0	ps
PLL output phase jitter		w/o SSCG	–1.5		1.5	ns
PLL lock up time		w/ SSCG			800.0	µs
PLL modulation frequency		w/ SSCG	20.0		100.0	kHz
PLL frequency dithering range		Center spread	±0.82	±2	±5.9	%
		Down spread	0.82	5.0	11.80	%

Table 1.25 PLL1 Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
PLL input frequency	f_{PLLkIN}		7.2		16	MHz
PLL output frequency	$f_{PLLkCLK}$				480.0	MHz
PLL output period jitter			–100.0		100.0	ps
Long term jitter		Term = 1 µs	–500		500	ps
		Term = 20 µs	–2.0		2.0	ns
PLL lock up time					100.0	µs

Table 1.26 PLL0 SSCG Dithering Range for Each Settings

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Frequency dithering range	f_{dit}	Dithered frequency mode (down spread only)	SELMPERCENT = 000	0.82	1.0	1.18	%
			SELMPERCENT = 001	1.64	2.0	2.36	
			SELMPERCENT = 010	2.46	3.0	3.54	
			SELMPERCENT = 011	3.28	4.0	4.72	
			SELMPERCENT = 100	4.10	5.0	5.90	
			SELMPERCENT = 101	4.92	6.0	7.08	
			SELMPERCENT = 110	6.56	8.0	9.44	
			SELMPERCENT = 111	8.20	10.0	11.80	
		Dithered frequency mode (center spread)	SELMPERCENT = 000	Invalid			
			SELMPERCENT = 001	±0.82	±1.0	±1.18	
			SELMPERCENT = 010	Invalid			
			SELMPERCENT = 011	±1.64	±2.0	±2.36	
			SELMPERCENT = 100	Invalid			
			SELMPERCENT = 101	±2.46	±3.0	±3.54	
			SELMPERCENT = 110	±.3.28	±4.0	±4.72	
			SELMPERCENT = 111	±4.10	±5.0	±5.90	

1.5.11 Voltage Regulator Conditions

Condition: T_j = –40°C to +T_{Jmax}
REGnVCC = 2.7 to 5.5 V

Table 1.27 Voltage Regulator

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Output voltage stabilization time	t_{REG}				1	ms
Output voltage level	TV_{tole}		1.2	1.25	1.3	V
Capacitance to REGnC (n=0,1)	C_{REG}			0.1		µF
PSRR	C_{PSRR}				–10	db
Output tolerance of REG1VCC			–4		4	%
Equivalent series resistance for load capacitance	RVRAWO	for AWO area			50*1	mΩ
	RVRISO	for ISO area			50*1	mΩ

Note 1. All values are defined by device characterization, not tested in production.

1.6 General IO Characteristic

1.6.1 Output Port Characteristics

1.6.1.1 GP Port Buffer

(1) Frequency Control of GP Port Buffers

The maximum frequency of the GP port buffer can be controlled via register setting in the port control in two steps; fast mode and slow mode.

Effectively the frequency control option limits the slew rate, what results in a (limited) max. frequency of the buffer.

Condition: Buffer power supply: XyVCC = 2.7 to 5.5V

Table 1.28 GP Output Buffer Characteristic

Parameter[*1]	CT	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Output voltage high level		CMOS V_{OHa1}	slow mode: I_{oh} ≤ –1mA, 16pin simultaneous operation slow mode: I_{oh} ≤ –2mA, 2pin simultaneous operation	XyVCC –0.5		XyVCC	V
		CMOS V_{OHa2}	fast mode: I_{oh} ≤ –5mA, 5pin simultaneous operation	XyVCC –0.5		XyVCC	
Output voltage low level		CMOS V_{OLa1}	slow mode: I_{oh} ≤ –1mA, 16pin simultaneous operation slow mode : I_{oh} ≤ –2mA, 2pin simultaneous operation	XyVSS		XyVSS +0.4	V
		CMOS V_{OLa2}	fast mode: I_{ol} <= 5mA, 5pin simultaneous operation	XyVSS		XyVSS +0.4	
cross current in port buffer during output level switching[*2]		I_{Cross}				0	mA
current limit during output level switching	DS	IODL	frequency control: slow mode XyVCC = 3.0 to 5.5 V			2	mA
			frequency control: fast mode XyVCC = 3.0 to 5.5 V			5	mA
Output frequency[*3]	DS[*4]	f_{max}	frequency control: fast mode C_L = 50 pF; XyVCC = 3.0 to 5.5 V	20			MHz
			frequency control: fast mode C_L = 30 pF; XyVCC = 3.0 to 5.5 V	50			MHz
			frequency control: slow mode C_L = 50 pF; XyVCC = 3.0 to 5.5 V	8			MHz
			frequency control: slow mode C_L = 30 pF; XyVCC = 3.0 to 5.5 V	10			MHz
			frequency control: fast mode C_L = 300 pF; XyVCC = 3.0 to 5.5 V	100			kHz

Note 1. The characteristics of the alternative-function pins are the same as those of the port pins unless otherwise specified.

Note 2. The cross current caused by the frequency control (slew rate limitation) must not cause a cross current during buffer level switching.

Note 3. Measurement according to **Section 1.3.1, AC Characteristic Measurement Condition**

Note 4. Not tested in production. Specified by design.

1.6.1.2 AN Port Buffer

Condition: Buffer power supply (XyVCC): A0VCC = 2.7 to 5.5 V

Table 1.29 AN Output Buffer Characteristic

Parameter*1	CT	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Output voltage high		V_{OHg2}	$I_{OHg2} \leq -1$ mA*2, 16pin simultaneous operation	XyVCC –0.5		XyVCC	V
Output voltage low		V_{OLg2}	$I_{OLg2} \leq 1$mA*2, 16pin simultaneous operation			XyVSS +0.4	V
Output propagation delay time		t_{pdo}	C_{load} = 50 pF			22	ns
			C_{load} = 30 pF			13	ns
Output rise/fall time		t_{rfo}	C_{load} = 50 pF			33	ns
			C_{load} = 30 pF			22	ns
Maximum output frequency*3	DS	f_{maxo}	C_{load} = 50 pF	8			MHz
			C_{load} = 30 pF	10			MHz

Note 1. The characteristics of the alternative-function pins are the same as those of the port pins unless otherwise specified

Note 2. A port output current might affect the A/D Converter accuracy on neighbor pins. For details see **Section 1.8.1, Analog/Digital Converter (ADCE)**.

Note 3. Measurement according to **Section 1.3.1, AC Characteristic Measurement Condition**.

1.6.1.3 HD Port Buffer

The stepper motor driver (SMD) is a bi-directional I/O buffer with the same buffer like the GP buffers but with a high current output buffer and an additional zero point detection path.

A output frequency up to 32 kHz is possible if the SMDIO is used with the GP Output path (Selection0).

Stepper Motor Driver mode (Selection1) the buffer have to provide the full drivability of the specified current output in the ISMVCC = 4.75 V to 5.25 V supply range. Outside this supply range no current is specified for this mode. Refer to **Figure 1.10, Output Current Diagram of SMDIO Buffer (valid only at Ta = –40°C)**."

NOTE

Selection 0/1 is the Stepper Motor Driver output buffers selection and corresponds to the register PDSC[17:16].PDSCn_m = 0/1 setting.

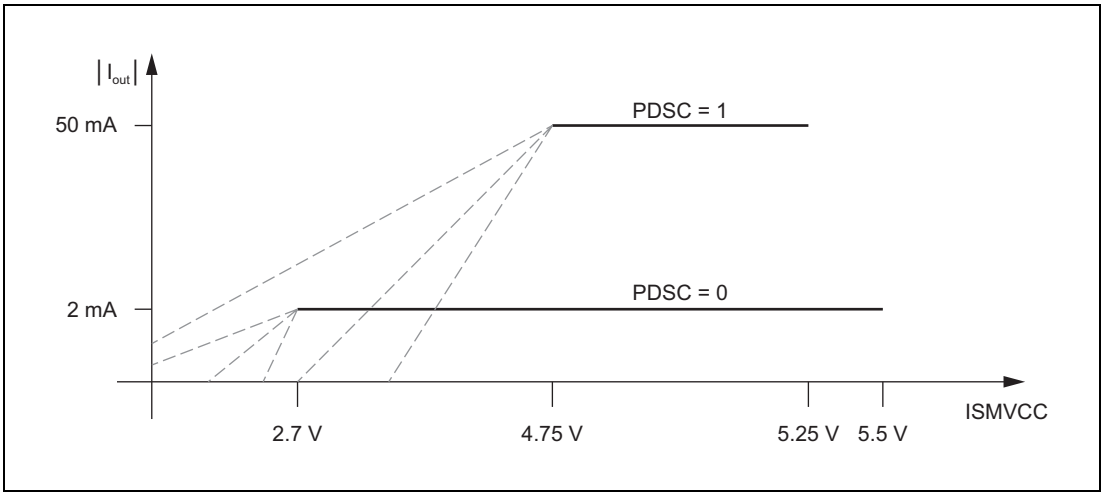


Figure 1.10 Output Current Diagram of SMDIO Buffer (valid only at Ta = –40°C)

The output voltage and current of the SMDIO buffer are shown in the below **Figure 1.11, Output Voltage and Current of the SMD Function**. The cross current through the buffer is visible. It is caused by the two output transistors that are kept open simultaneously for a specific time while the output level is switched. Opening both transistors is necessary in order to control the slew rate. It is also necessary since the inductance of the stepper motor induces a reverse current that would be discharged through the protection diodes, if the transistor is not open.

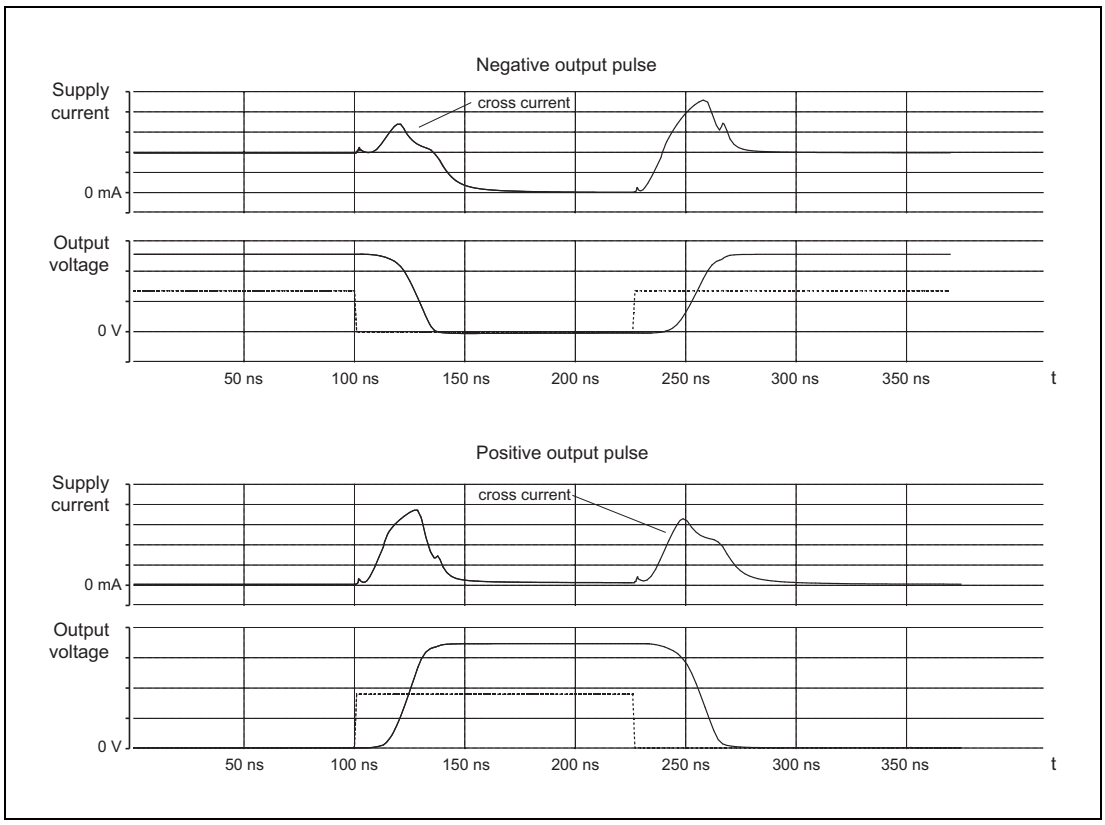


Figure 1.11 Output Voltage and Current of the SMD Function

CAUTION

- Buffer power supply (XyVCC):
  - Selection0: ISMVCCn = 2.7 to 5.5 V
  - Selection1: ISMVCCn = 4.75 to 5.25 V

NOTE

Selection 0/1 is the Stepper Motor Driver output buffers selection and corresponds to register setting in port control macro.

Table 1.30 HD Output Buffer Characteristic

Parameter*1	CT	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Output voltage high		V_{OHd2}	(Selection0)	I_{OHd2} ≤ –2 mA	XyVCC –0.5		XyVCC	V
		V_{OHd3}	(Selection1) XyVCC = 4.75 to 5.25 V	I_{OHd3} = –52 mA T_J = –40°C	XyVCC –0.48		XyVCC	V
				I_{OHd3} = –45 mA T_J = –40°C	XyVCC –0.5			
		V_{OHd4}		I_{OHd4} = –39 mA T_J = 25°C				
		V_{OHd5}		I_{OHd5} =-32 mA T_J = 125°C				
		V_{OHd6}		I_{OHd6} = –30 mA T_J = 150°C				
Output voltage low		V_{OLd2}	(Selection0)	I_{OLd2} ≤ 2 mA	XyVSS		XyVSS +0.5	V
		V_{OLd3}	(Selection1) XyVCC = 4.75 to 5.25 V	I_{Old3} = 52 mA T_J = –40°C	XyVSS		XyVSS +0.52	V
				I_{Old3} = 45 mA T_J = –40°C			XyVSS +0.5	
		V_{OLd4}		I_{Old4} = 39 mA T_J = 25°C				
		V_{OLd5}		I_{Old5} = 32 mA T_J = 125°C				
		V_{OLd6}		I_{Old6} = 30 mA T_J = 150°C				
Output voltage deviation*2	DS*3	VDEV*4	(Selection1)				50	mV
Output slew rate*6	DS*3	t_{RFd}		10% - 90%	12		70	ns
Peak cross current*7	DS*3	I_{CROSS}*4					50	mA
Output pulse width*8	DS*3	t_{MO}d			125			ns
Output pulse length deviation*8	DS*3	t_{SMDEV}*4			–10	5	45	ns
Output resistance		R_{OSM}	(Selection1) XyVCC = 4.75 to 5.25 V	T_J = –40°C	5		11.6	Ω
				T_J = 25°C			15.4	Ω
				T_J = 125°C			18.8	Ω
				T_J = 150°C			21	Ω
Output frequency	DS*3	f_{OSMDIO}	(Selection0)	I_O = 3mA C_{load} = 50 pF		32		kHz
	DS*3	f_{OSMDIO}	(Selection1)	C_{load} = 50 pF		128		kHz

Note 1. The characteristics of the alternative-function pins are the same as those of the port pins unless otherwise specified.

Note 2. Output voltage deviation defines the difference of the outputs levels of the same stepper motor. VDEV = max (| VOHx – VOHy | , | VOLx – VOLy |) @ IOHx = IOHy, IOLx = IOLy. x and y denote any combination of two pins of a four pin group that is used for one stepper motor. The output voltage deviation is not tested, but specified by design.

Note 3. Not tested in production. Specified by design.

Note 4. The slew rate control generates a cross current in the output stage to control the energy of the external inductive load. The output voltage deviation is not tested, but specified by design.

Note 5. The slew rate control generates a cross current in the output stage to control the energy of the external inductive load. The cross current flows only during the output transition time t_{RF}. It flows in addition to the output current. The cross current is not tested, but derived from simulation.

Note 6. The output buffer cannot generate high or low pulses shorter than this time, because of its slew rate control system. This value is not tested, but derived from simulation.

Note 7. The slew rate control function causes a deviation of output pulse time compared to the ideal selected output

pulse setting. This value is not tested, but derived from simulation.

Note 8. Measurement according to **Section 1.3.1, AC Characteristic Measurement Condition**.

1.6.2 Port Input Characteristics

1.6.2.1 CMOS1

Condition: Buffer power supply: XyVCC

Table 1.31 CMOS1 Input Characteristic

Parameter*1	CT	Symbol	Condition*2	MIN.	TYP.	MAX.	Unit
Input voltage high		V_{IHa1}	CMOS XyVCC = 2.7 to 5.5 V	0.65 × XyVCC		XyVCC +0.3	V
Input voltage low		V_{ILa1}	CMOS XyVCC = 2.7 to 5.5 V	–0.3		0.35 × XyVCC	V
Input propagation delay time	DS	$t_{pdi,c1}$	XyVCC = 2.7 to 5.5 V C_{load} = 0.4 pF			3.0	ns

Note 1. The characteristics of the alternative-function pins are the same as those of the port pins unless otherwise specified.

Note 2. The alias XyVCC in the condition is used instead of the operating voltage range for the related port group. By no means it extends the operating range of the related supply voltage. The exceeding condition will be meaningless.

1.6.2.2 Schmitt1

Condition: Buffer power supply: XyVCC
For different input timing of Schmitt trigger buffer see **Section 1.3.1, AC Characteristic Measurement Condition**.

Table 1.32 Schmitt1 Input Characteristic

Parameter*1	CT	Symbol	Condition*2		MIN.	TYP.	MAX.	Unit
Input voltage high		V_{IHa2}	Schmitt1 XyVCC = 2.7 to 5.5 V	for FLMD0	0.68 × XyVCC		XyVCC +0.3	
				except FLMD0	0.7 × XyVCC			
Input voltage low		V_{ILa2}	Schmitt1 XyVCC = 2.7 to 5.5 V		–0.3		0.3 × XyVCC	
Input hysteresis		V_{Ha1}	Schmitt1		0.3			V
Input propagation delay time	DS	$t_{pdi,s1}$	XyVCC = 2.7 to 5.5 V C_{load} = 0.4 pF				5.0	ns

Note 1. The characteristics of the alternative-function pins are the same as those of the port pins unless otherwise specified.

Note 2. The alias XyVCC in the condition is used instead of the operating voltage range for the related port group. By no means it extends the operating range of the related supply voltage. The exceeding condition will be meaningless.

1.6.2.3 Schmitt2

Condition: Buffer power supply: XyVCC
For different input timing of Schmitt trigger buffer see **Section 1.3.1, AC Characteristic Measurement Condition**.

Table 1.33 Schmitt2 Input Characteristic

Parameter*1	CT	Symbol	Condition*2	MIN.	TYP.	MAX.	Unit
Input voltage high		V_{IHa}	Schmitt2 XyVCC = 2.7 to 5.5 V	0.75 × XyVCC		XyVCC +0.3	V
Input voltage low		V_{ILa}	Schmitt2 XyVCC = 2.7 to 5.5 V	–0.3		0.25 × XyVCC	V
Input hysteresis		V_{Ha2}	Schmitt2	0.2 × VCC			V
Input propagation delay time	DS	$t_{pdi,s2}$	XyVCC = 2.7 to 5.5 V C_{load} = 0.4 pF			5.0	ns

Note 1. The characteristics of the alternative-function pins are the same as those of the port pins unless otherwise specified.

Note 2. The alias XyVCC in the condition is used instead of the operating voltage range for the related port group. By no means it extends the operating range of the related supply voltage. The exceeding condition will be meaningless.

NOTE

The Schmitt2 input characteristic is to be used for the $\overline{\text{RESET}}$ input of the device.

1.6.2.4 Schmitt4

Condition: Buffer power supply: XyVCC
For different input timing of Schmitt trigger buffer see **Section 1.3.1, AC Characteristic Measurement Condition**.

Table 1.34 Schmitt4 Input Characteristic

Parameter*1	CT	Symbol	Condition*2	MIN.	TYP.	MAX.	Unit
Input voltage high		V_{IHa4}	Schmitt4 XyVCC = 2.7 to 5.5 V	0.80 × XyVCC		XyVCC +0.3	V
Input voltage low		V_{ILa4}	Schmitt4 XyVCC = 2.7 to 5.5 V	–0.3		0.50 × XyVCC	V
Input hysteresis		V_{Ha4}	Schmitt4	0.1			V
Input propagation delay time	DS	$t_{pdi,s4}$	XyVCC = 2.7 to 5.5 V C_{load}=0.4 pF			5.0	ns

Note 1. The characteristics of the alternative-function pins are the same as those of the port pins unless otherwise specified.

Note 2. The alias XyVCC in the condition is used instead of the operating voltage range for the related port group. By no means it extends the operating range of the related supply voltage. The exceeding condition will be meaningless.

1.6.2.5 (LV)TTL

Condition: Buffer power supply: XyVCC

Table 1.35 (LV)TTL Input Characteristic

Parameter*1	CT	Symbol	Condition*2	MIN.	TYP.	MAX.	Unit
Input voltage high		V_{IHLTa1}	LVTTL XyVCC = 3.0 to 3.6 V	2.0		XyVCC +0.3	V
Input voltage high		V_{IHTa1}	TTL XyVCC = 3.6 to 5.5 V	2.2		XyVCC +0.3	V
Input voltage low		V_{ILLTa1}	LVTTL XyVCC = 3.0 to 3.6 V	–0.3		0.8	V
Input voltage low		V_{ILTa1}	TTL XyVCC = 3.6 to 5.5 V	–0.3		0.8	V
Input propagation delay time	DS	$t_{pdi\text{-}c1}$	XyVCC = 3.0 to 5.5 V			4.0	ns

Note 1. The characteristics of the alternative-function pins are the same as those of the port pins unless otherwise specified.

Note 2. The alias XyVCC in the condition is used instead of the operating voltage range for the related port group. By no means it extends the operating range of the related supply voltage. The exceeding condition will be meaningless.

1.6.2.6 Pull-Up and Pull-Down Resistors

Table 1.36 Pull-up and Pull-down Resistor Characteristic

Parameter*1	CT	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Pull-Up resistor		R_{PU}		20	40	120	kΩ
Pull-Down resistor		R_{PD}		20	40	120	kΩ
Pull-Up resistor		R_{PU}	only FLMD0	4		44	kΩ
Pull-Down resistor		R_{PD}	only FLMD0	4		50	kΩ

Note 1. The characteristics of the alternative-function pins are the same as those of the port pins unless otherwise specified.

1.6.3 IO Input Leakage Current

Condition: T_j = –40°C to T_{Jmax}
Buffer power supply: XyVCC.
Typ condition indicate following condition
- Each VCC set to 5.0V
- T_j = 25°C
- Device: maximum condition

Table 1.37 Input leakage Current for Each Power Domain

Parameter*1	Domain	Symbol	Condition	MIN.	TYP.	MAX.	Unit
input leakage current (high level)	EVCC B0VCC B1VCC B5VCC A0VCC	$I_{inLeakH}$	1 pin supplied by XyVCC XyVSS ≤ Vi ≤ XyVCC	–0.5	–0.1		µA
input leakage current (low level)		$I_{inLeakL}$	1 pin supplied by XyVCC XyVSS ≤ Vi ≤ XyVCC		0.1	+0.5	µA
input leakage current (high level)	ISMVCC	$I_{inLeakH}$	1 pin supplied by XyVCC XyVSS ≤ Vi ≤ XyVCC	–0.6	–0.1		µA
input leakage current (low level)		$I_{inLeakL}$	1 pin supplied by XyVCC XyVSS ≤ Vi ≤ XyVCC		0.1	+0.5	µA

Note 1. The characteristics of the alternative-function pins are the same as those of the port pins unless otherwise specified.

1.6.4 I/O Capacitance

Table 1.38 IO Buffer Capacitance

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
All	CIO	f = 1 MHz			8.0	pF

Table 1.39 Input Buffer Capacitance

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input buffer capacitance	CI	f = 1 MHz			8.0	pF

1.7 General Module Operating Conditions

1.7.1 $\overline{\text{RESET}}$

Condition: AWO = powered
EVCC = 2.7 to 5.5 V, CL = Max.100 pF
Measurement according to **Section 1.3.1, AC Characteristic Measurement Condition**

Table 1.40 Reset AC Characteristic

Parameter	CT	Symbol	Condition	MIN.	TYP.	MAX.	Unit
$\overline{\text{RESET}}$ low-level width*1		t_{WRSL} (in RUN/HALT mode)		10			µs
		t_{WRSL} (in deepstop mode)		25			µs
$\overline{\text{RESET}}$ pulse rejection*2	DS	t_{WRRJ}		100			ns

Note 1. This signal low time is needed to ensure that the internal $\overline{\text{RESET}}$ is activated.

Note 2. The $\overline{\text{RESET}}$ input incorporates an analog filter. Pulses shorter than this minimum will be ignored. Not tested in production.

NOTE

Reset pulses shorter than the given value may not be recognized by the device, they do not cause undefined states of the device.

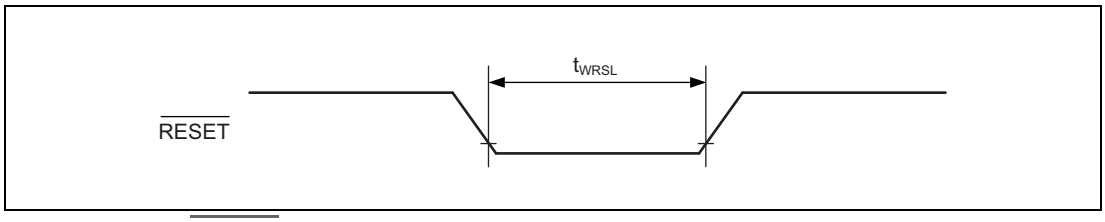


Figure 1.12 $\overline{\text{RESET}}$ Timing

1.7.2 Interrupt Timing

Condition: AWO = powered, ISO = powered
EVCC = 2.7 to 5.5V, BnVCC = 2.7 to 5.5V
Measurement according to **Section 1.3.1, AC Characteristic Measurement Condition**. The input timings are valid if the digital filter is bypassed.

Table 1.41 Interrupt AC Characteristics

Parameter	CT	Symbol	Condition	MIN.	TYP.	MAX.	Unit
NMI high-level width*1		t_{NIH}		10			µs
NMI low-level width*1		t_{NIL}		10			µs
NMI pulse rejection*2	DS*3	t_{NIRJ}		50			ns
I_{NTPn}*4 high-level width*1		t_{ITH}*5		24			µs
I_{NTPn}*4 low-level width*1		t_{ITL}*5		24			µs
I_{NTPn}*4 pulse rejection*2	DS*3	t_{ITRJ}		50			ns

Note 1. Pulses longer than this value will pass the input filter.
Note 2. Pulses shorter than this value do not pass the input filters.
Note 3. Characteristic is not tested in production.
Note 4. n = 10...0.
Note 5. 24 µs is for when high speed internal oscillator is configured to stop in DEEPSTOP (ROSCSTPM.ROSCSTPMSK = 0_B). Other case is 10 µs.

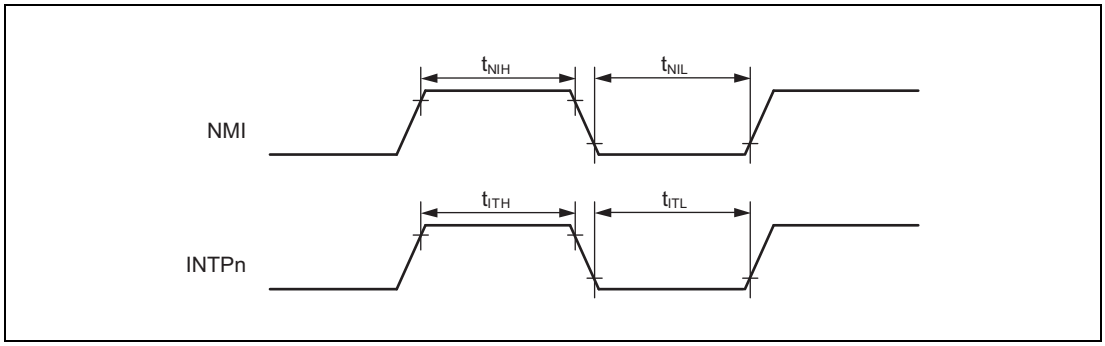


Figure 1.13 Interrupt Timing

NOTE

Interrupt timing is generated by analog delay elements. Delay characteristics have a wide range in production.

1.7.3 System Pins Timing

The below specification is valid for all system pins:

- FLMD0, FLMD1, MODE0, MODE1, PWRGD, JP0_4.

Instead of using the names of the system pins the term SYSPIN is used.

These system pins SYSPIN incorporate an analog noise filter within the input signal path:

Condition: AWO = powered,
EVCC = 2.7 to 5.5 V
Measurement according to **Section 1.3.1, AC Characteristic Measurement Condition**. The input timings are valid if the digital filter is bypassed.

Table 1.42 System Pins AC Characteristics

Parameter	CT	Symbol	Condition	MIN.	TYP.	MAX.	Unit
SYSPIN high-level width*1		t_{SPH}		10			µs
		t_{SPHGD}	PWRGD	10			µs
SYSPIN low-level width*1		t_{SPL}		10			ns
		t_{SPLGD}	PWRGD	10			µs
SYSPIN pulse rejection*2	DS*3	t_{SPRJ}		50			ns

Note 1. Pulses longer than this value will pass the input filter.
Note 2. Pulses shorter than this value do not pass the input filters.
Note 3. Characteristic is not tested in production.

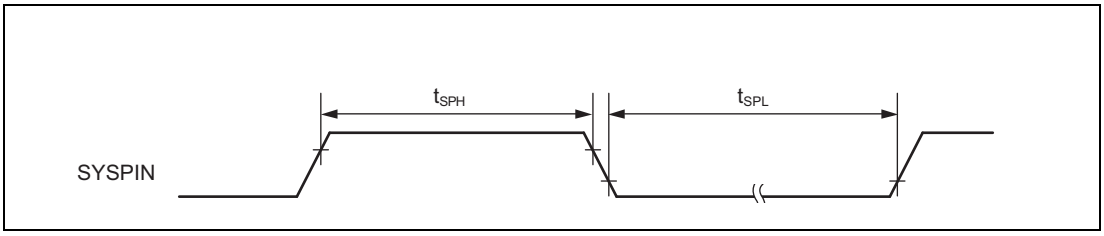


Figure 1.14 System Pins Timing

NOTE

System Pins timing is generated by analog delay elements. Delay characteristics have a wide range in production. System pins need hold time of 1 µs from FLMD0 determined.

1.7.4 Clock-Output Function

Condition: AWO = powered
EVCC = 2.7 to 5.5 V
Measurement according to **Section 1.3.1, AC Characteristic Measurement Condition**. The input timings are valid if the digital filter is bypassed.

Table 1.43 Clock Output Mode via GPIO Buffer

Parameter	CT	Symbol	Pin mode	Condition	MIN.	TYP.	MAX.	Unit
Clock output period time (CSCXFOUT)		t_{clkout}			50			ns
CSCXFOUT high/low-level width		t_{FPH}/t_{FPL}	CSCXFOUTP (FOUT)	N = 1 or even value, drive strength = fast	t_{clkout} × 0.4			ns
				N = odd value (N ≥ 3), drive strength = fast	t_{clkout} × ((N – 1) / 2N) – 10			ns
				N = 1 or even value, drive strength = slow	t_{clkout} × 0.5 – 25			ns
				N = odd value (N ≥ 3), drive strength = slow	t_{clkout} × ((N – 1) / 2N) – 25			ns

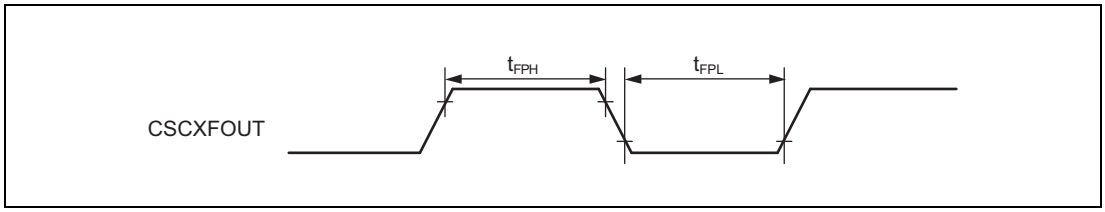


Figure 1.15 Clock Output Function Timing (CSCXFOUT)

1.7.5 ECM ERROUT

Table 1.44 ECM ERROUT AC Characteristic

Parameter	CT	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High/low pulse width		t_{ECMHNB} / t_{ECMLNB}		2 × t_{SYNC}*1 + 5			ns

Note 1. t_{SYNC} is TAUB or OSTM operation clock cycle.

1.7.6 General Digital Noise Filter (DNF) Specification

(1) Minimum Pulse Rejection Width

Minimum pulse rejection width means that this is the minimum pulse width that will definitely be suppressed or in other words, ext. signal pulses with a longer width might pass the filter.

$$t_{wDNF(min)} = (s-1) \times \frac{1}{f_s}$$

(2) Maximum Pulse Rejection Width

Maximum pulse rejection width means that this is the maximum pulse width that can be suppressed or in other words, ext. signal pulses with a longer width will definitely pass the filter.

$$t_{wDNF(max)} = (s) \times \frac{1}{f_s}$$

NOTE

Ext. signal pulses with a width between $t_{wDNF(min)}$ and $t_{wDNF(max)}$ may be suppressed or pass the filter.

(3) Minimum Delay Time

Minimum delay time is the minimum time that ext. signals need to propagate through the DNF, i.e. it is the path delay of the DNF.

$$t_{dDNF(min)} = (s-1) \times \frac{1}{f_s} + 2\left(\frac{1}{f_{DNFATCKI}}\right)$$

(4) Maximum Delay Time

Maximum delay time is the maximum time that ext. signals need to propagate through the DNF, i.e. it is the path delay of the DNF.

$$t_{dDNF(max)} = (s) \times \frac{1}{f_s} + 3\left(\frac{1}{f_{DNFATCKI}}\right)$$

(5) Formula Explanation

s is the number of sampling times (s = 2..5), depending on setting of register bit DNFAnCTL.DNFAnNFSTS;

fs is the sampling clock The sampling clock is derived from the DNF module input clock (DNFATCKI) as follows:

$$f_S = \frac{f_{DNFATCKI}}{PRS}$$

$f_{DNFATCKI}$ is the DNF module clock

PRS is the prescaler (PRS = 1, 2, 4, ..., 128), depending on the setting of register bit DNFAnCTL.DNFAnPRS;

NOTES

1. Please consider the register settings of the DNF while using the above mentioned formulas.
2. There is also a filter bypass available for each DNF. This should be used for high-speed application of the module function.

1.8 Analog Module Operating Conditions

1.8.1 Analog/Digital Converter (ADCE)

Condition: AWO = powered, ISO = powered

Table 1.45 ADC Characteristic

Parameter	CT	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Reference Voltages		A0VREF		2.7		A0VCC	V
Analog input voltage		V_{AIN}		0		A0VREF	V
Resolution				10		12	bit
A/D Converter system frequency	DS	f_{ADCLK}		8		40	MHz
Conversion time		t_{CONV}		1.15			µs
Overall Error*1	PC	TOE	10-bit mode, A0VCC = 4.5 to 5.5 V			±1	LSB
			10-bit mode, A0VCC = 3.6 to 4.5 V			±1.5	LSB
			10-bit mode, A0VCC = 2.7 to 3.6 V			±2	LSB
			12-bit mode, A0VCC = 4.5 to 5.5 V			±4	LSB
			12-bit mode, A0VCC = 3.6 to 4.5 V			±6	LSB
			12-bit mode, A0VCC = 2.7 to 3.6 V			±8	LSB
Conversion result for positive overload condition	PC		A0VREF = A0VCC ≤ AIN	4015 – |TOE| (12-bit mode) 1003 – |TOE| (10-bit mode)		4095 (12-bit mode) 1023 (10-bit mode)	LSB
Analog input pull-down resistance				350	500	650	kΩ
Analog supply current during normal operation	PC	I_{AVCC}				3.0	mA
Analog supply current during power-down	PC	I_{AVCCPD}			1		µA
Analog reference supply current	PC	I_{A0VREF}	During normal operation		500	1000	µA

Note 1. Not include quantization error.

Table 1.46 Self-diagnosis Characteristic

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Accuracy of self-diagnosis	TESH0SN	12-bit mode	Diagnosis voltage = A0VREF	4015 – |TOE|*1,*2		4095*1,*2	LSB
			Diagnosis voltage = 2/3 × A0VREF	2651 – |TOE|*1,*2	2731	2811 + |TOE|*1,*2	LSB
			Diagnosis voltage = 1/2 × A0VREF	1968 – |TOE|*1,*2	2048	2128 + |TOE|*1,*2	LSB
			Diagnosis voltage = 1/3 × A0VREF	1285 – |TOE|*1,*2	1365	1445 + |TOE|*1,*2	LSB
			Diagnosis voltage = A0VSS	0		80 + |TOE|*1,*2	LSB
	TESH0SN	10-bit mode	Diagnosis voltage = A0VREF	1003 – |TOE|*1,*2		1023*1,*2	LSB
			Diagnosis voltage = 2/3 × A0VREF	663 – |TOE|*1,*2	683	703 + |TOE|*1,*2	LSB
			Diagnosis voltage = 1/2 × A0VREF	492 – |TOE|*1,*2	512	532 + |TOE|*1,*2	LSB
			Diagnosis voltage = 1/3 × A0VREF	321 – |TOE|*1,*2	341	361 + |TOE|*1,*2	LSB
			Diagnosis voltage = A0VSS	0		20 + |TOE|*1,*2	LSB
Accuracy degradation of self-diagnosis on current injection	TESH0SND	Positive current injection = 0.1 mA		0		200	LSB
		Negative current injection = –0.1 mA		–100		0	LSB

Note: Not include quantization error

Note 1. For a reliable detection of the ADC faults it is necessary that the conversion voltage doesn't exceed the conversion range.

Note 2. The injected current during ADC self-diagnosis when A0VCC = 5 V has to be limited to 0.1 mA and no injected current is allowed during ADC self-diagnosis when A0VCC = 3.3 V or in 10-bit mode. Accuracy degradation shown in **Table 1.46** is measured on injected ±0.1 mA current to measurement pins.

CAUTION

Please be aware that the accuracy of the A/D Converter input channel is influenced by a exceeding voltage drop to the AVSS and AVCC power supply lines. This exceeding voltage drop is caused by a higher sum of total current that flows at adjacent digital pins with disabled A/D Converter input functionality (depending on number of switching digital output pins, load capacitance, sum of overload current, timing gap between IO output switching and sampling of A/D Converter input channel).

1.8.1.1 Equivalent Circuit of A/D Converter Input Pin

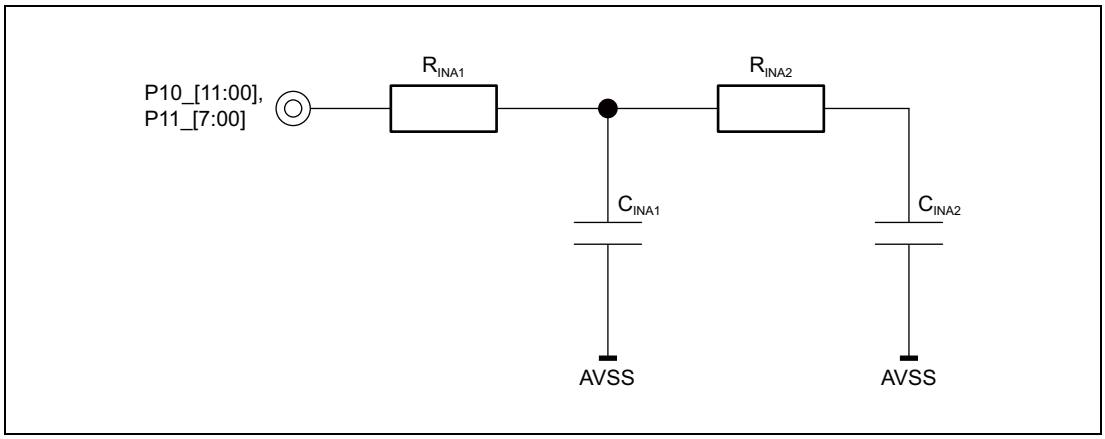


Figure 1.16 Equivalent Circuit of A/D Converter Input Pin - 2nd-order Model

Table 1.47 Analog Input Equivalent Circuit

Parameter	CT	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Analog input equivalent circuit resistance	DS*1	R_{INA1}			2.5		kΩ
		R_{INA2}			1.1		kΩ
Analog input equivalent circuit capacitance	DS*1	C_{INA1}			3.5		pF
		C_{INA2}			0.5		pF

Note 1. Not tested in production. Specified by design.

1.8.1.2 External Circuit on ADC Inputs

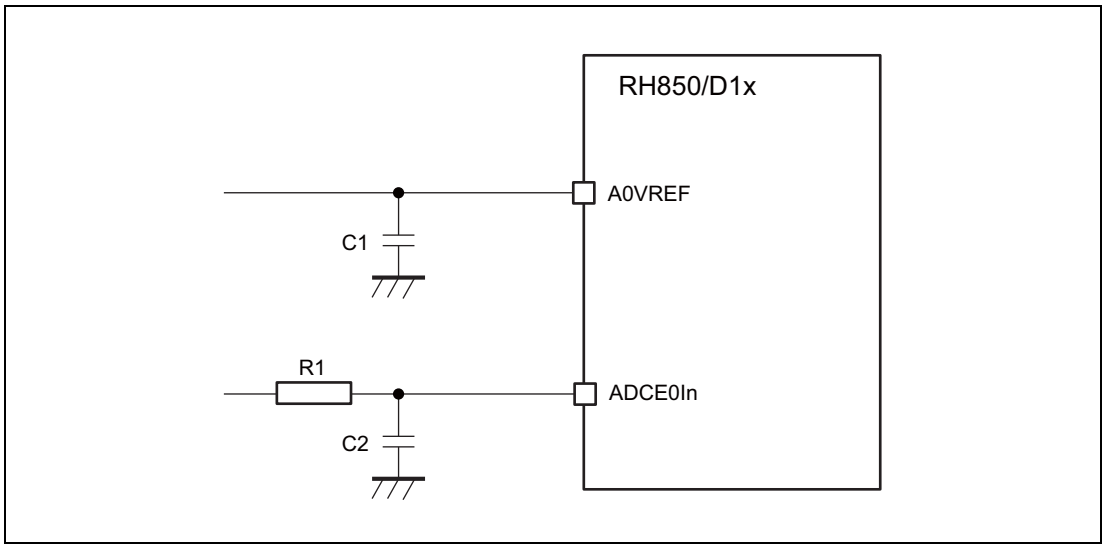


Figure 1.17 External Circuit on ADC Inputs

The external circuit on ADC input depends the input condition of user (filter condition). The characteristic of ADC is improved while R is small and C is large (about 0.1 µF). If R is large, ADC conversion error is occurred by dropping the voltage inputted ADCE0Im terminal. If C is small ADC input terminal cannot endure noise.

Component	Value
R1	10 kΩ
C1	100 nF
C2	10 nF

As guide line for the calculation of the external capacitor the formula based on the internal equivalent capacitance and the ADC resolution of the corresponding AD-converter channel can be used:

$C_{external} = C_{IN} \times 2$ ADC resolution

$C_{external}$: External capacitor

C_{IN}: Equivalent input capacitance (≈ CINA1 + CINA2)

1.8.1.3 A/D Converter Trigger Timing

Condition: The input incorporates a digital noise filter (DNF) in the input signal path. The filter function can be bypassed. If not bypassed the DNF filters all pulses that are shorter than the given high- and low-level width. Longer pulses are passed.

Table 1.48 ADCE0TRGn AC Characteristic

Parameter	CT	Symbol	Condition	MIN.	TYP.	MAX.	Unit
ADCE0TRGn input high-level width	DS	t_{WADTH}	filtered (DNF)*1	t_{dDNF}(max) + 2 × t_{SYNC} + 5*2			ns
			filter-bypassed*3	2 × t_{SYNC} + 5			ns
ADCE0TRGn input low-level width		t_{WADTL}	filtered (DNF)	t_{dDNF}(max) + 2 × t_{SYNC} + 5*2			ns
			filter-bypassed	2 × t_{SYNC} + 5			ns
ADCE0TRGn input pulse rejection		t_{ADTRJ}	filtered (DNF)	t_{dDNF}(min) + t_{SYNC} + 5			ns
			filter-bypassed	t_{SYNC} + 5			ns

Note 1. Please consider the following SFR bit of the filter control module for selecting the filtered input signal: FCLA0CTLn.FCLA0BYPSn = 0

Note 2. 2 × t_{SYNC} is the delay time due to the synchronization of the input signal of the A/D Converter Trigger with the module clock of the A/D Converter module (t_{SYNC} = one module clock cycle).Note: Please consider the correct module clock of the A/D Converter

Note 3. Please consider the following SFR bit of the filter control module for selecting the filter-bypassed input signal: FCLA0CTLn.FCLA0BYPSn = 1

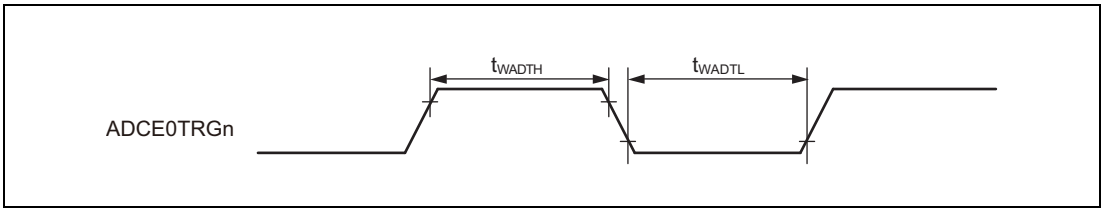


Figure 1.18 ADCE0TRGn Input Timing

1.8.1.4 How to Read A/D Converter Characteristics Table

This section describes the meanings of the terms peculiar to the A/D converter.

(1) Resolution

The minimum analog input voltage that can be identified, i.e. the ratio of the analog input voltage to 1 digital output is called 1 LSB (Least Significant Bit). The ratio of 1 LSB to the full scale is expressed as %FSR (Full Scale Range). %FSR is the ratio, in percentage, of the range in which an analog input voltage can be converted, and is expressed as follows regardless of the resolution.

1%FSR = (Maximum value of analog input voltage that can be converted - Minimum value of analog input voltage that can be converted) /100

= (AVrefp – AVrefm) /100

At a resolution of 10 bits the relation between 1 LSB and %FSR is as follows:

1 LSB = $1 / 2^{10}$

= 1 / 1,024

= 0.098 %FSR

At a resolution of 12 bits the relation between 1 LSB and %FSR is as follows:

1 LSB = $1 / 2^{12}$

= 1 / 4,096

= 0.024 %FSR

The accuracy is determined by the total error, regardless of the resolution.

(2) Total Error

This is the maximum value of the difference between the actually measured value and the theoretical value.

It is the total of the zero-scale error, full-scale error, linearity error, and a combination of these errors.

The total error shown in the characteristics table does not include the quantization error.

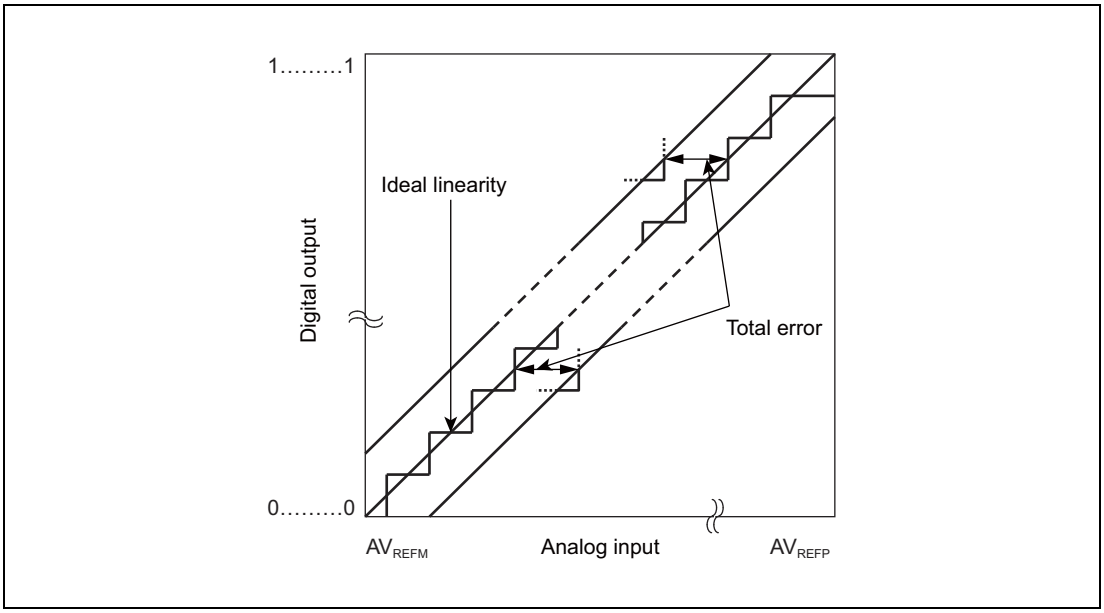


Figure 1.19 Total Error

(3) Quantization Error

This is the error of ±1/2 LSB that always occurs when an analog value is converted into a digital value. Because the A/D converter converts an analog input voltage in a range of ±1/2 LSB into the same digital code, the quantization error is unavoidable.

Note that this error is not included in the total error, zero-scale error, full-scale error, integral linearity error, and differential linearity error in the characteristics table.

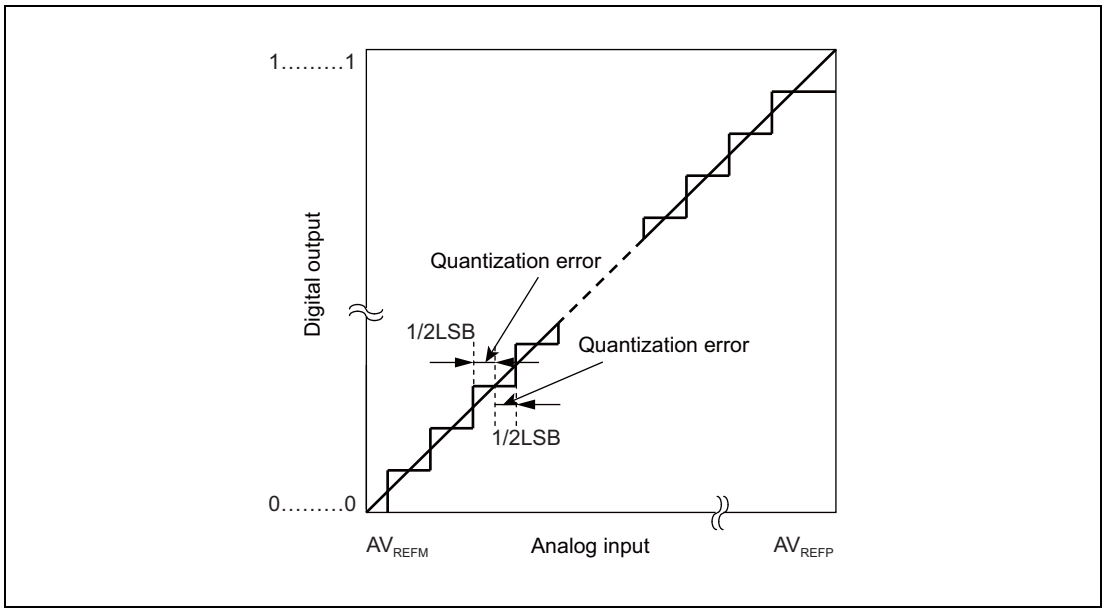
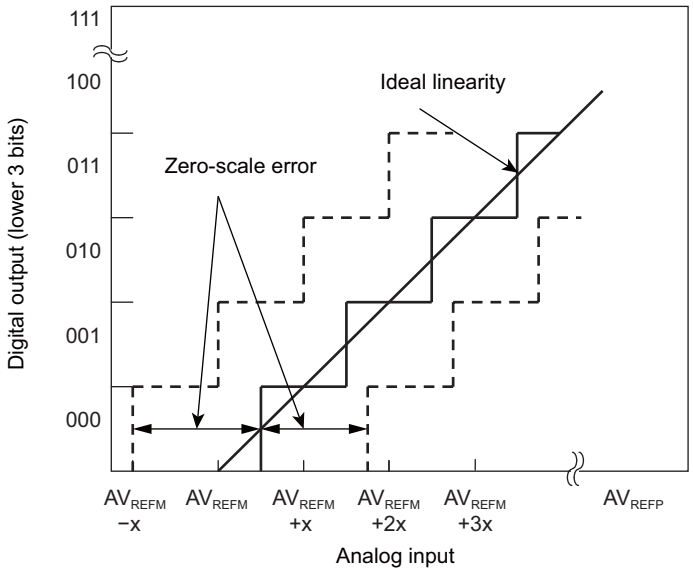


Figure 1.20 Quantization Error

(4) Zero-scale Error

This is the difference between the actually measured value of the analog input voltage and the theoretical value (1/2 LSB) when the digital output changes from 0…000 to 0…001.

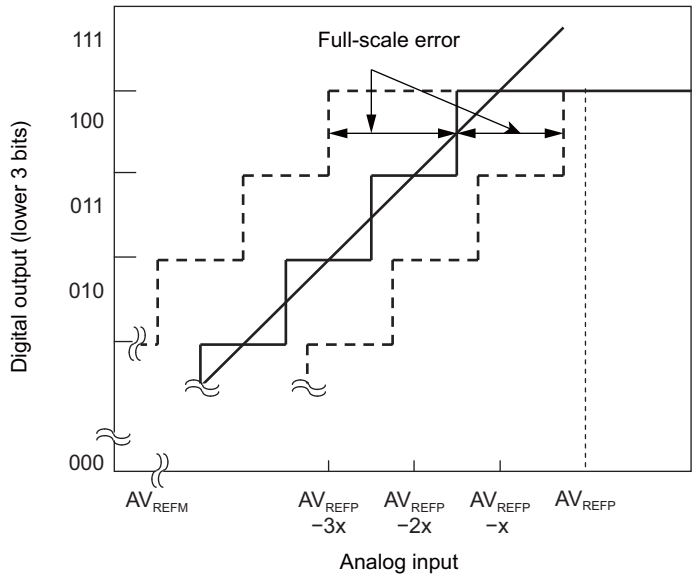


Note: x: voltage equivalent to 1 LSB
$x = (AV_{refp} - AV_{refm}) \times 1\ LSB$

Figure 1.21 Zero-scale Error

(5) Full-scale Error

This is the difference between the actually measured value of the analog input voltage and the theoretical value (full scale – 3/2 LSB) when the digital output changes from 1…110 to 1…111.



Note: x: voltage equivalent to 1 LSB
$x = (AV_{refp} - AV_{refm}) \times 1\ LSB$

Figure 1.22 Zero-scale Error

(6) Differential Linearity Error

Ideally, the width at which a specific code is output is 1 LSB. The differential linearity error is the difference between the actually measured value of the width at which a specific code is output and the ideal value.

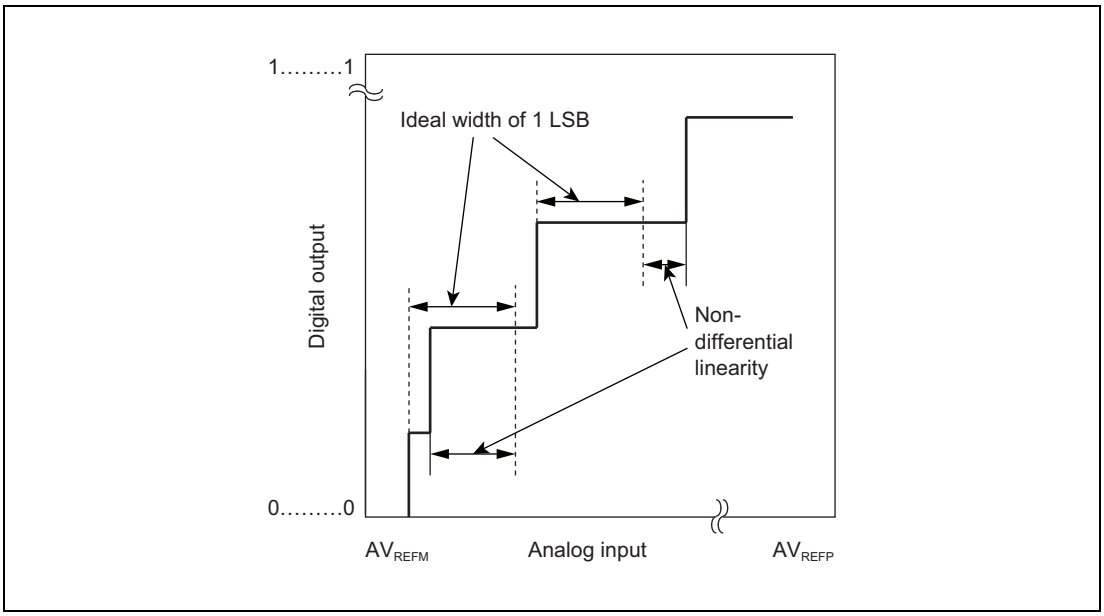


Figure 1.23 Differential Linearity Error

(7) Integral Linearity Error

This indicates the degree to which the conversion characteristic shifts from the ideal linearity, and indicates the maximum value of the difference between the actually measured value and the ideal linearity where the zero-scale error and full-scale error are 0.

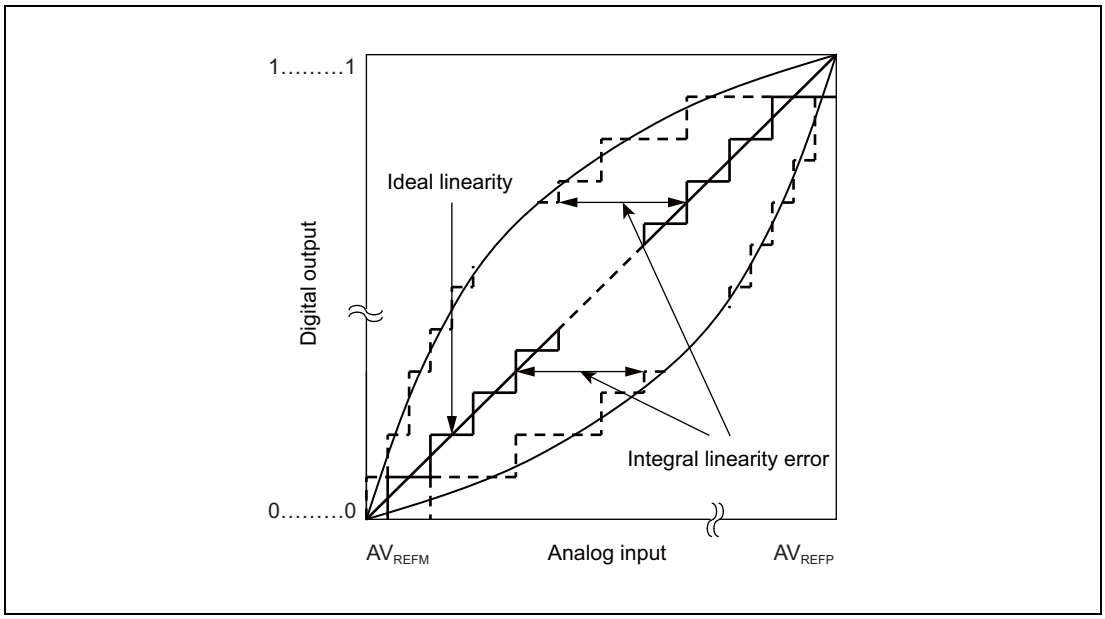


Figure 1.24 Integral Linearity Error

(8) Conversion Time

This is the time from when an analog voltage is input until digital output is produced.

The conversion time in the characteristics table includes sampling time.

(9) Sampling Time

This is the time during which the analog switch is on to input the analog voltage to the sample & hold circuit.

(10) A/D Start Time

This is the time from the A/D conversion trigger to the start of A/D conversion.

1.8.2 POC Characteristic

1.8.2.1 POC Characteristic on AWO

Condition: AWO = powered
REG0VCC = 2.7 to 5.5 V

CAUTIONS

1. The POC ensures that the devices stops operation ($\overline{\text{RESET}}$ condition) when the device is outside the operation voltage range, under the condition that the supply voltage slope on REG0VCC is ≤500V/ms.
2. Full device operation is only available, when the supply voltage is above the maximum threshold voltage. The device may stop operation due to reset condition generated by POC, if the supply voltage drops below the given max threshold voltage.

Table 1.49 POC Characteristic on AWO

Parameter	CT	Symbol	Condition	MIN.	TYP.	MAX.	Unit
POC detection threshold voltage		V_{POC0}	Power-on(Rise)	2.8	2.95	3.1	V
			Power-down(Fall)	2.8	2.9	3.0	V
POC threshold voltage hysteresis	DS*1	V_{POC0H}			2		mV
Response time at power up	DS*1	ts_{POC0R}	At power on(Rise) $V_{POC0ramp}$ = 0.00 to 0.5V/ms			2	ms
			At power on(Rise) $V_{POC0ramp}$ = 0.5 to 500V/ms			6.3	ms
			At power on(Rise) $V_{POC0ramp}$ = 0.00 to 20V/ms			2	ms
			At power on(Rise) $V_{POC0ramp}$ = 20 to 500V/ms			5	ms
Response time at power-down		ts_{POC0F}	$V_{POC0ramp}$ = 0.00 to 500V/ms			5	µs
POC0 supply voltage ramp*2	DS*1	$V_{POC0ramp}$		0.00		500	V/ms
POC minimum pulse width	DS*1	t_{POC0W}		0.2			ms
POC noise rejection width	DS*1	t_{POC0RJ}				30	ns

Note 1. Not tested in production. Specified by design.

Note 2. Up to the specified maximum POC0 supply voltage down ramp the POC0 ensures that the devices stops operation and enters a defined state (i.e. $\overline{\text{RESET}}$ condition).

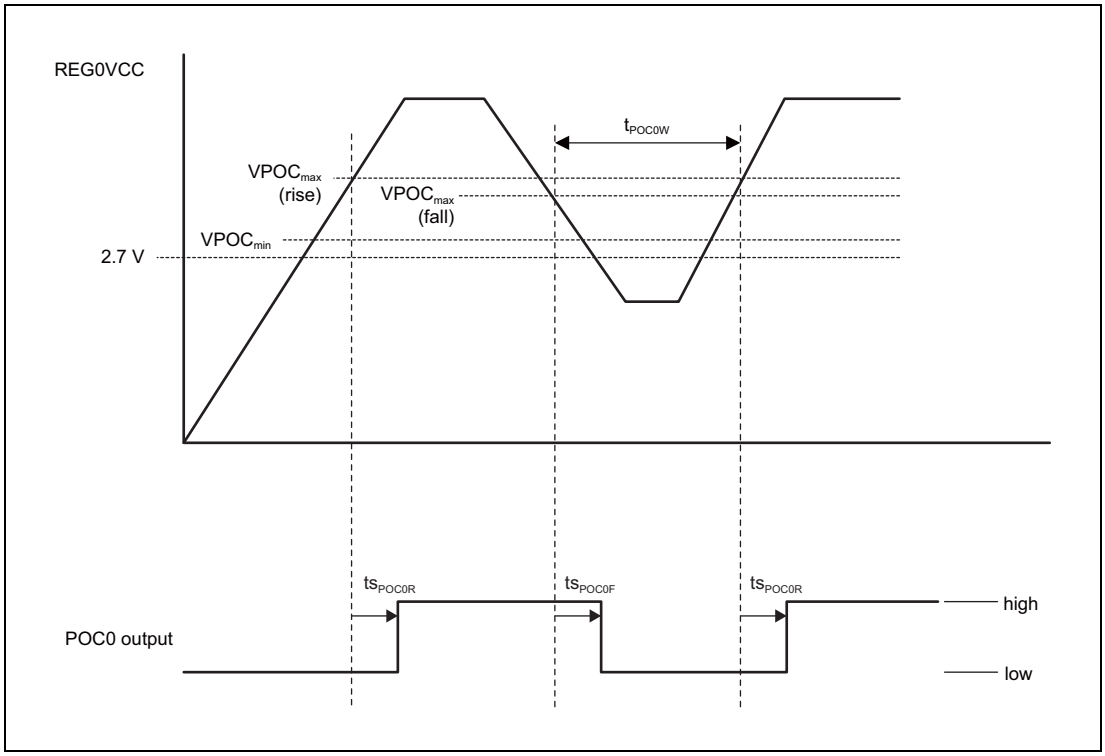


Figure 1.25 POC0 Timing

1.8.2.2 POC Characteristic on ISO

Condition: AWO = powered, ISO = powered
REG1VCC = 2.7 to 5.5 V

CAUTION

The POC ensures that the ISO stops operation when the device is outside the operation voltage range, under the condition that the supply voltage slope on REG1VCC is ≤400V/ms.

Table 1.50 POC Characteristic on ISO

Parameter	CT	Symbol	Condition	MIN.	TYP.	MAX.	Unit
POC detection threshold voltage		V_{POC1}	Power-on(Rise)	2.8	2.95	3.1	V
			Power-down(Fall)	2.8	2.9	3.0	V
POC threshold voltage hysteresis	DS*1	V_{POC1H}			2		mV
Response time at power up	DS*1	ts_{POC1R}	At power on(Rise) $V_{POC1ramp}$ = 0.00 to 0.5V/ms			2	ms
			At power on(Rise) $V_{POC1ramp}$ = 0.5 to 400V/ms			6.3	ms
			At power on(Rise) $V_{POC1ramp}$ = 0.00 to 20V/ms			2	ms
			At power on(Rise) $V_{POC1ramp}$ = 20 to 400V/ms			5	ms
Response time at power-down		ts_{POC1F}	$V_{POC1ramp}$ = 0.00 to 400V/ms			5	µs
POC1 supply voltage ramp*2	DS*1	$V_{POC1ramp}$		0.00		400	V/ms
POC minimum pulse width	DS*1	t_{POC1W}		0.2			ms
POC noise rejection width	DS*1	t_{POC1RJ}				30	ns

Note 1. Not tested in production. Specified by design.

Note 2. Up to the specified maximum POC1 supply voltage down ramp the POC1 ensures that the devices stops operation and enters a defined state (i.e. $\overline{\text{RESET}}$ condition).

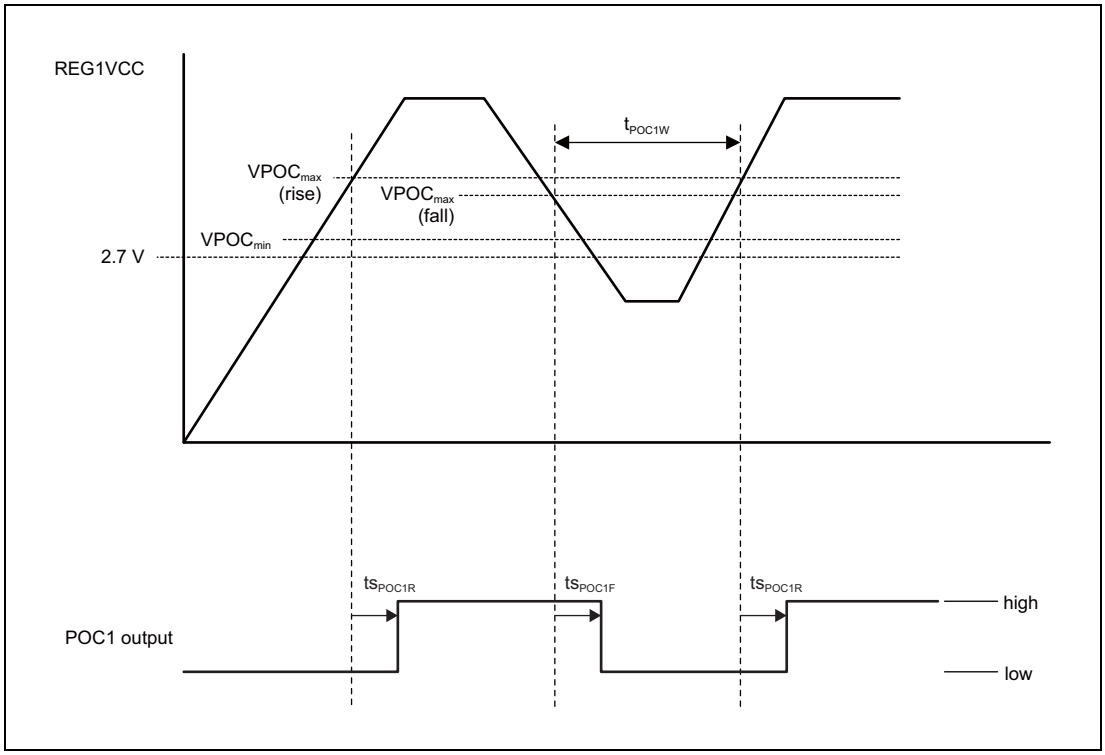


Figure 1.26 POC1 Timing

1.8.3 Zero Point Detection (ZPD)

The ZPD input path is an analog connection from the pad of a stepper motor driver (SMD) buffer to the ZPD module by-passing the digital input path of the general purpose input function of the SMD buffer.

Condition: AWO = powered, ISO = powered
ZPDVCC =4.5 to 5.5 V

Table 1.51 DC Characteristics Stepper Motor Driver Zero Point Detection

Parameter	CT	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Accuracy of ZPD comparator		Vth, ZPD	Internal reference, V_{ZPD} ≤ 350 mV	–20		20	mV
		Vth, ZPD	Internal reference, V_{ZPD} ≥ 450 mV	–30		30	mV
Input pulse width*1	DS*2	t_{PW}		2			µs
Comparator output delay		t_{ZPDD}				1	µs
Dynamic current of ZPDVCC		I_{ZPDVCC}				2.0	mA

Note 1. The input pulse should have a minimum pulse width (TPW) to be detected properly. Shorter pulses may be ignored.

Note 2. Not tested in production. Specified by design.

NOTES

1. Four independent stepper motor channels (consisting of four SMD pins) can be measured by the ZPD.
2. For each stepper motor channel, 4 different inputs (SMD pins) can be selected for the ZPD.
3. Each stepper motor channel can be compared to 1 out of 3 reference voltages. Two of the reference voltages are generated based on Internal BGR.
4. Each reference voltage(V_{ZPD}) is as follows.
   - Selection by ISMnGZPDCTL.ISMnGGRV1[3:0]
     - 100, 150, 215, 230, 235, 245, 250, 350, 450, 480, 500, 550, 650, 750, and 850 mV
   - Selection by ISMnGZPDCTL.ISMnGGRV2[3:0]
     - 150, 215, 225, 235, 245, 350, 450, 470, 480, 490, 500, 550, 650, 750, and 850 mV
5. The measurement itself is done by analogue comparators of the ZPD.
6. Each stepper motor channel has its own comparator.
7. For the timing of the ZPD function refer to **Figure 1.27, Timing of ZPD Function**.

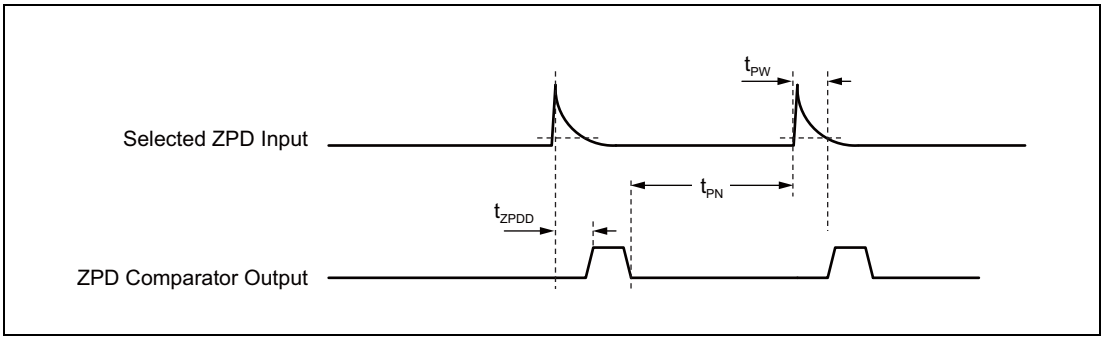


Figure 1.27 Timing of ZPD Function

1.8.4 Temperature Sensor

Condition: AWO = powered, ISO = powered
REG1VCC = 3.0 to 5.5 V

Table 1.52 Temperature Sensor Specification

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Temperature detect Accuracy		Tj = –40 to 25°C	–10.0		10	°C
		Tj = 25 to 150°C	–5		5	°C
Stability time of output voltage			6.0			µs
Return time from Standby state					200.0	µs
Operation current					200.0	µA
Standby current					25.0	µA

1.9 Timer Module Operating Condition

1.9.1 Timer TAUB/TAUJ Timing

Table 1.53 Timer TAUB/TAUJ AC Specification*1

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
TAUx high/low-level width	t_{TAUHNB} / t_{TAULNB}	filtered (DNF)	$t_{dDNF(max)}$ + 2 × t_{SYNC} + 5*2,*3			ns
		filter-bypassed	2 × t_{SYNC} + 5			ns
TAUx pulse rejection	t_{TAURJ}	filtered (DNF)	$t_{dDNF(min)}$ + t_{SYNC} + 5*2			ns
		filter-bypassed	t_{SYNC} + 5			ns

Note 1. The external input incorporates a digital noise filter (DNF). Using a filter control macro this DNF can be placed into the input signal path. The filter control macro can also be used to bypass the DNF.

Note 2. Please refer to **Section 1.7.6, General Digital Noise Filter (DNF) Specification**.

Note 3. 2 × t_{SYNC} is the delay time due to the synchronization of the input signal of the Timer TAUx with the macro clock of the Timer TAUx (t_{SYNC} = one macro clock cycle)

1.10 Serial Interface Module Operating Condition

1.10.1 LIN / UART Interface

Table 1.54 LIN / UART AC Specification

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Transfer rate UART	t_{UARTR}		0.3		1000.0	Kbps
Transfer rate LIN	t_{LIN}		1		115.2	Kbps
UART/LIN RX pulse rejection	t_{UARTRJ}		$t_{PCLK} \times 2^{PRS}$			ns

Note: PRS is the RLIN3/UART clock prescaler division value, set in the macro register. Please refer the prescaler function in Users Manual.

1.10.2 Synchronous Interface CSIG

1.10.2.1 Master Mode

Table 1.55 Master Mode AC Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
PCLK frequency	t_{KCYf}				80	MHz
PCLK cycle time	t_{KCY}		12.5			ns
Clock output cycle time	t_{KCYM}		100.0			ns
Clock output high level width	t_{KWHM}		0.5 × t_{KCYM} – 10.0			ns
Clock output low level width	t_{KWLM}		0.5 × t_{KCYM} – 10.0			ns
Data input setup time	t_{SSIM}	filtered (DNF)	29 + $t_{dDNFSI(max)}$			ns
		filter-bypassed	29			ns
Data input hold time	t_{HSIM}	filtered (DNF)	0 – $t_{dDNF(max)}$			ns
		filter-bypassed	0			ns
Data output delay max time	t_{DSOM}				5.0	ns
Data output delay min time	t_{HSOM}		–20			ns
Ready / Busy input signal (CSIGnRY) setup time	t_{SRYI}	filtered (DNF)	2 × t_{KCY} + $t_{dDNF(max)}$ + 16.6			ns
		filter-bypassed	2 × t_{KCY} + 16.6			ns
Ready / Busy input signal (CSIGnRY) high level width	t_{WRYI}	filtered (DNF)	t_{KCY} + $t_{dDNFRY(max)}$ – 5			ns
		filter-bypassed	t_{KCY} – 5			ns

(1) [CSIGnSC / CSIGnSO] Output Pins and [CSIGnSI] Input Pin in Master Mode

Note: Setting: CSIGnCTL1.CSIGnCKR = 0 (consider CSIGnCFG0.CSIGnDAP bit)

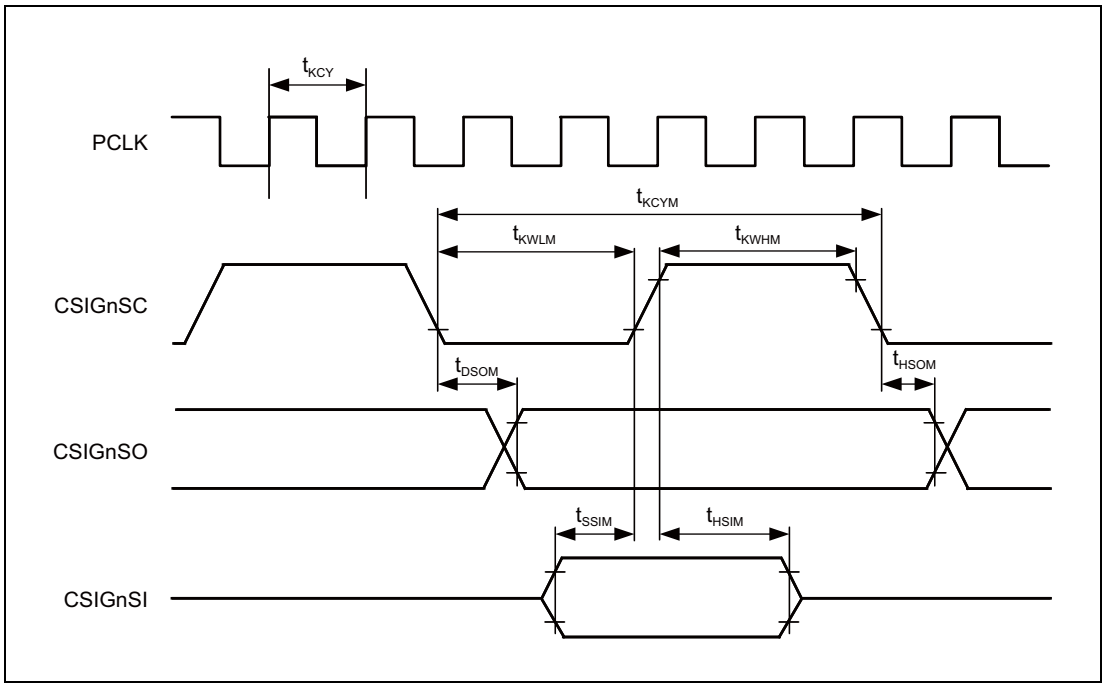


Figure 1.28 CSIGn Master Mode Timing (a)

(2) [CSIGnSC / CSIGnSO] Output Pins and [CSIGnSI] Input Pin in Master Mode

Note: Setting: CSIGnCTL1.CSIGnCKR = 1 (consider CSIGnCFG0.CSIGnDAP bit)

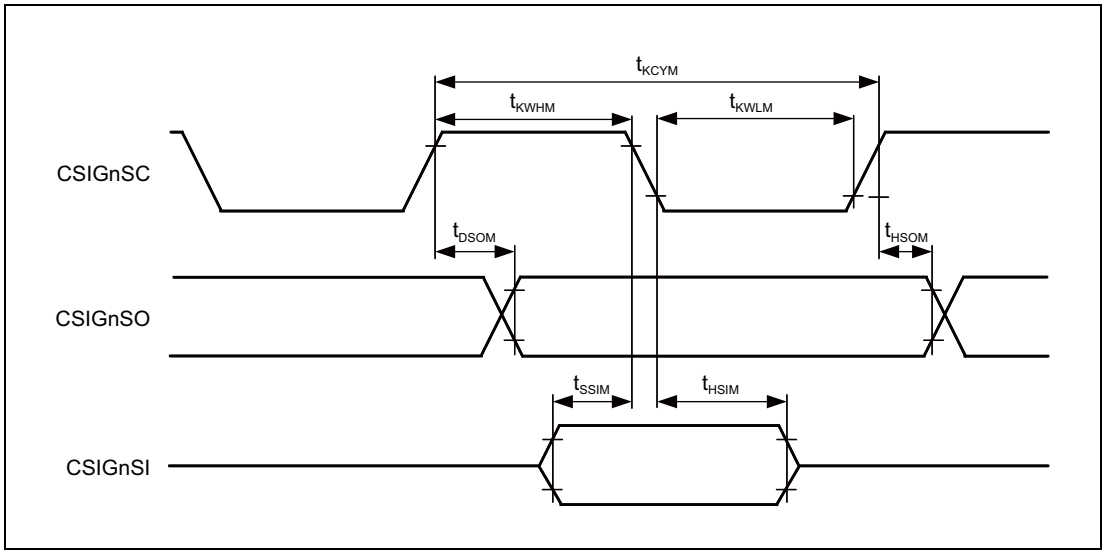


Figure 1.29 CSIGn Master Mode Timing (b): Inverted Clock2

(3) [CSIGnSC] Output Pin and [CSIGnRY] Input Pin in Master Mode

Note: Settings: CSIGnCTL1.CSIGnSIT=0, CSIGnCTL1.CSIGnHSE=1, CSIGnCTL1.CSIGnCKR = 0 (consider CSIGnCFG0.CSIGnDAP bit)

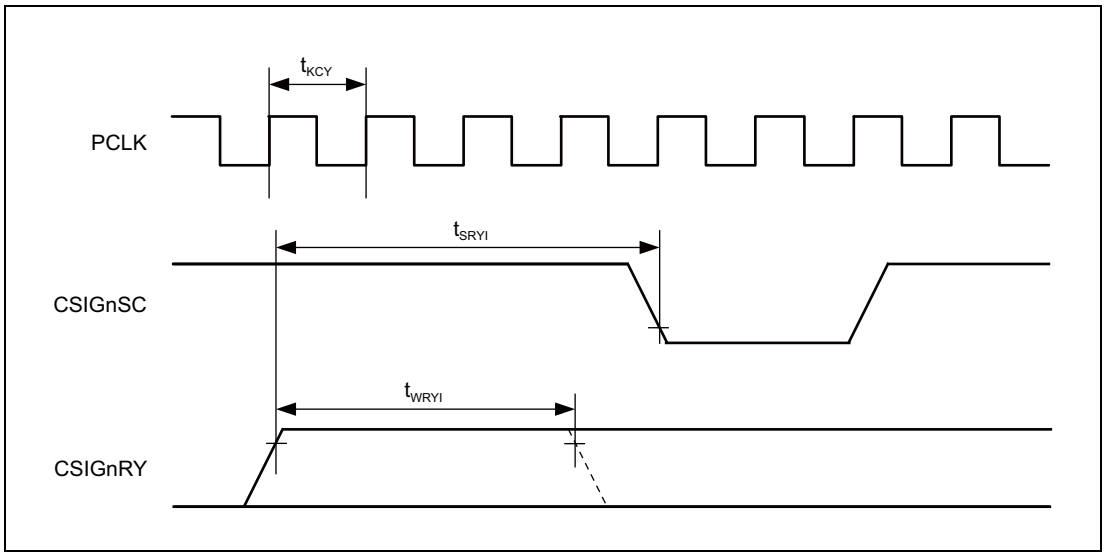


Figure 1.30 CSIGn Master Mode Timing (c): Ready / Busy Input Signal (CSIGnRY)

(4) [CSIGnSC] Output Pin and [CSIGnRY] Input Pin in Master Mode

Note: Settings: CSIGnCTL1.CSIGnSIT=0, CSIGnCTL1.CSIGnHSE=1, CSIGnCTL1.CSIGnCKR = 0 (consider CSIGnCFG0.CSIGnDAP bit)

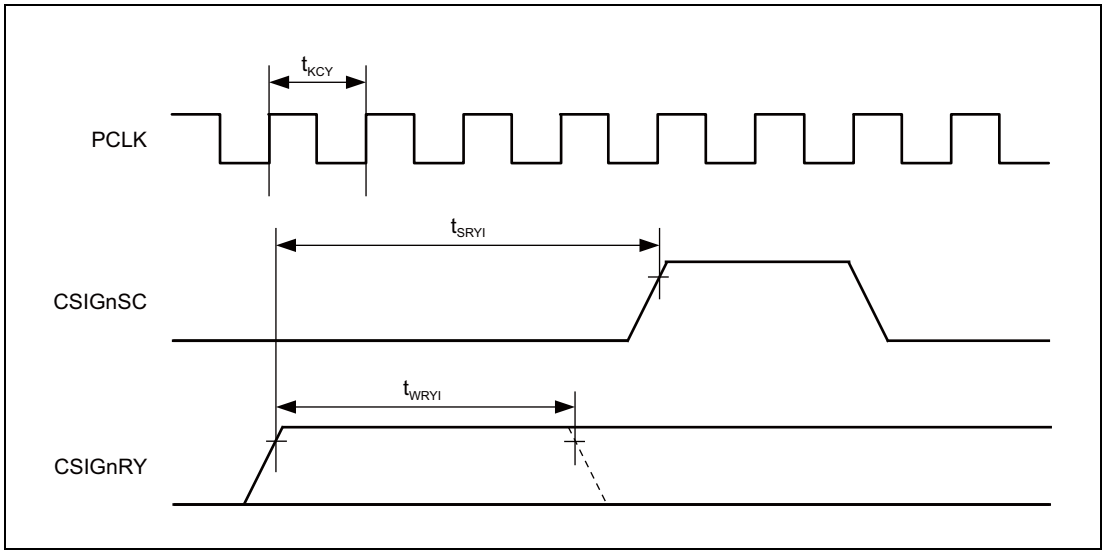


Figure 1.31 CSIGn Master Mode Timing (d): Ready / Busy Input Signal (CSIGnRY) - Inv.Clock

(5) [CSIGnSC / CSIGnDCS] Input Pins in Master Mode

Note: Settings: CSIGnCTL1.CSIGnDCS = 1, CSIGnCTL1.CSIGnCKR = 0 (consider CSIGnCFG0.CSIGnDAP bit)

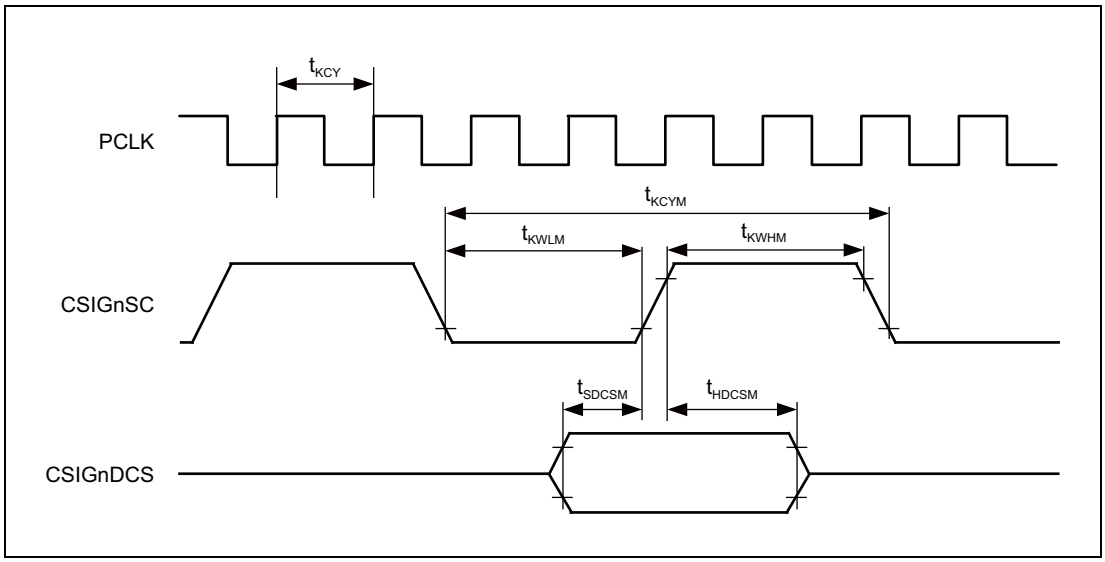


Figure 1.32 CSIGn Master Mode Timing (e): Data Consistency Check (CSIGnDCS)

(6) [CSIGnSC / CSIGnDCS] Input Pins in Master Mode

Note: Settings: CSIGnCTL1.CSIGnDCS=1, CSIGnCTL1.CSIGnCKR=0 (consider CSIGnCFG0.CSIGnDAP bit)

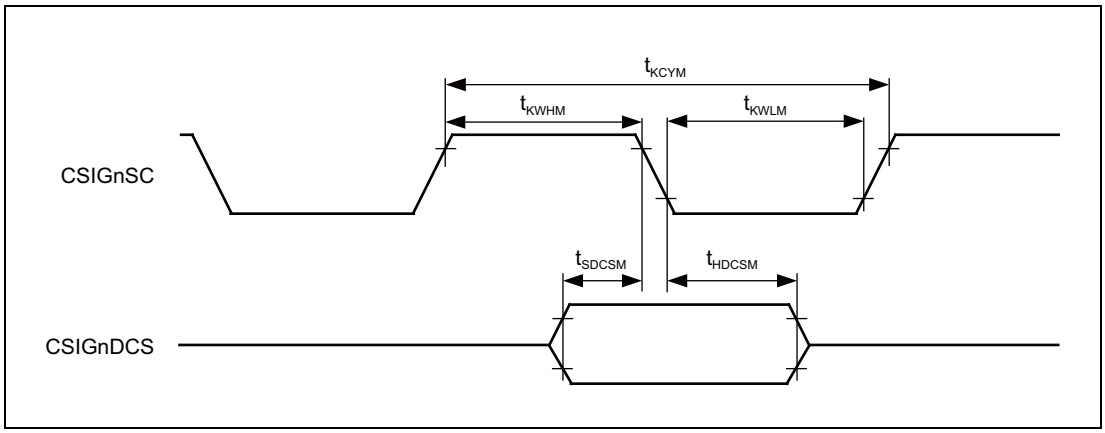


Figure 1.33 CSIGn Master Mode Timing (f): Data Consistency Check (CSIGnDCS) - Inverted Clock

1.10.2.2 Slave Mode

Table 1.56 Slave Mode AC Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
PCLK frequency	t_{KCYf}				80	MHz
PCLK cycle time	t_{KCY}		12.5			ns
Clock input cycle time	t_{KCYM}	filtered (DNF)	$8 \times t_{dDNFSCI(max)}$			ns
		filter-bypassed	75			ns
Clock input high level width	t_{KWHS}	filtered (DNF)	$4 \times t_{dDNFSCI(max)} - 5$			ns
		filter-bypassed	32.5			ns
Clock input low level width	t_{KWLS}	filtered (DNF)	$4 \times t_{dDNFSCI(max)} - 5$			ns
		filter-bypassed	32.5			ns
Data input setup time	t_{SSIS}	filtered (DNF)	$7 + t_{dDNFSCI(min)} - t_{dDNFSI(max)}$			ns
		filter-bypassed	7.5			ns
Data input hold time	t_{HSIS}	filtered (DNF)	$7 + t_{KCY} + t_{dDNFSCI(max)} - t_{dDNFSI(min)}$			ns
		filter-bypassed	$7.5 + t_{KCY}$			ns
Data output delay time	t_{DSOS}	filtered (DNF)			$35 + t_{dDNFSCI(max)}$	ns
		filter-bypassed			35	
Slave select control input signal setup time	t_{SSSIS}	filtered (DNF)	$0.5 \times t_{KCYS} + t_{dDNFSCI(min)} - t_{dDNFSI(max)} - 7$			ns
		filter-bypassed	$0.5 \times t_{KCYS} - 5$			ns
Slave select control input signal hold time	t_{HSSIS}	filtered (DNF)	$7 + t_{KCY} + t_{dDNFSCI(max)} - t_{dDNFSI(min)}$			ns
		filter-bypassed	$7.5 + t_{CKYS} - 5$			ns
Ready / Busy output signal (CSIG0RY) output delay time	t_{DRYO}	filtered (DNF)			$35 + t_{KCY} + t_{dDNFSCI(max)}$	ns
		filter-bypassed			$35 + t_{KCY}$	ns

(1) [CSIGnSO] Output Pin and [CSIGnSC / CSIGnSI] Input Pins in Slave Mode

Note: Setting: CSIGnCTL1.CSIGnCKR = 0 (consider CSIGnCFG0.CSIGnDAP bit)

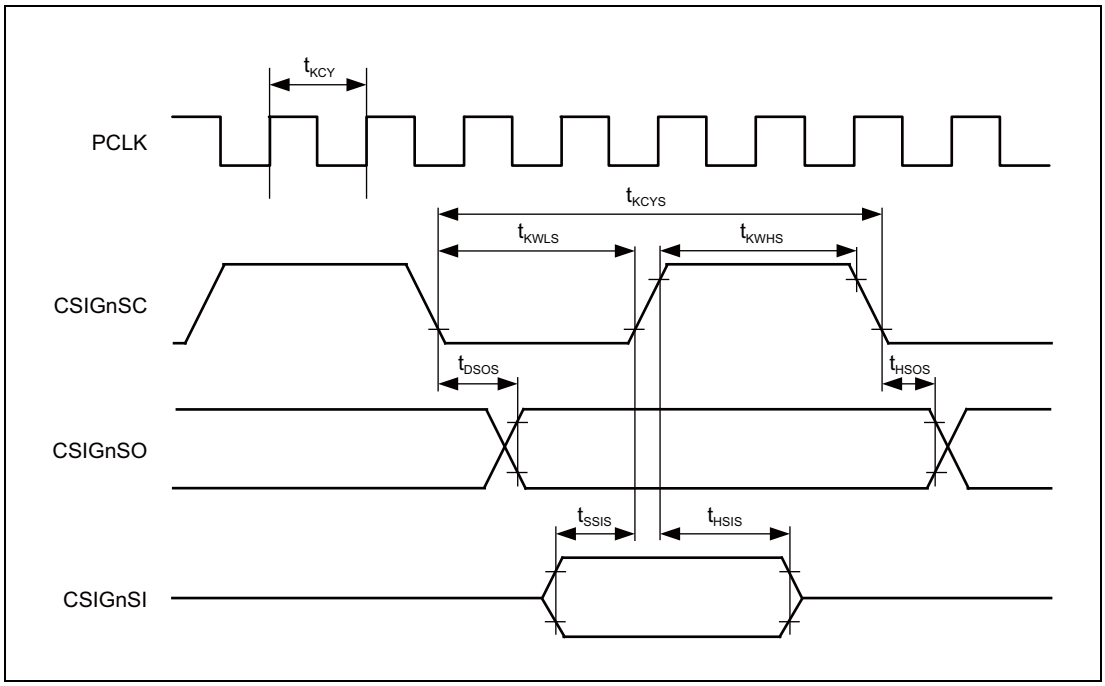


Figure 1.34 CSIGn Slave Mode Timing (a)

(2) [CSIGnSO] Output Pin and [CSIGnSC / CSIGnSI] Input Pins in Slave Mode

Note: Setting: CSIGnCTL1.CSIGnCKR = 0 (consider CSIGnCFG0.CSIGnDAP bit)

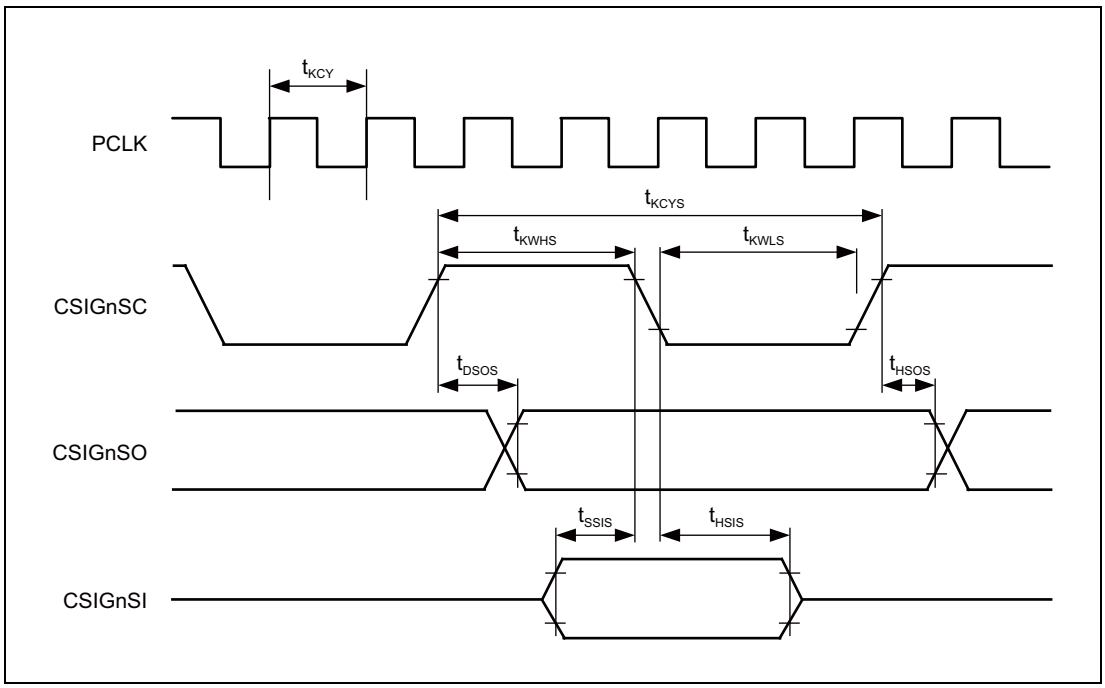


Figure 1.35 CSIGn Slave Mode Timing (b) - Inverted Clock

(3) [CSIGnSC / CSIGnSI] Input Pins in Slave Mode

Note: Settings: CSIGnCTL1.CSIGnSSE = 1, CSIGnCTL1.CSIGnCKR=0 (consider CSIGnCFG0.CSIGnDAP bit)

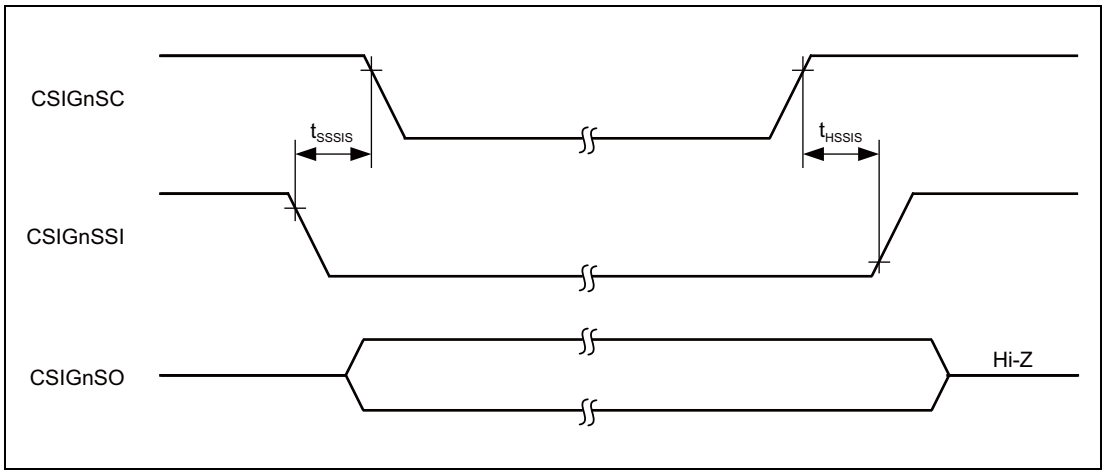


Figure 1.36 CSIGn Slave Mode Timing (c): Slave Select Ctrl Input (CSIGnSSI)

(4) [CSIGnSC / CSIGnSSI] Input Pins in Slave Mode

Note: Settings: CSIGnCTL1.CSIGnSSE = 1, CSIGnCTL1.CSIGnCKR = 1 (consider CSIGnCFG0.CSIGnDAP bit)

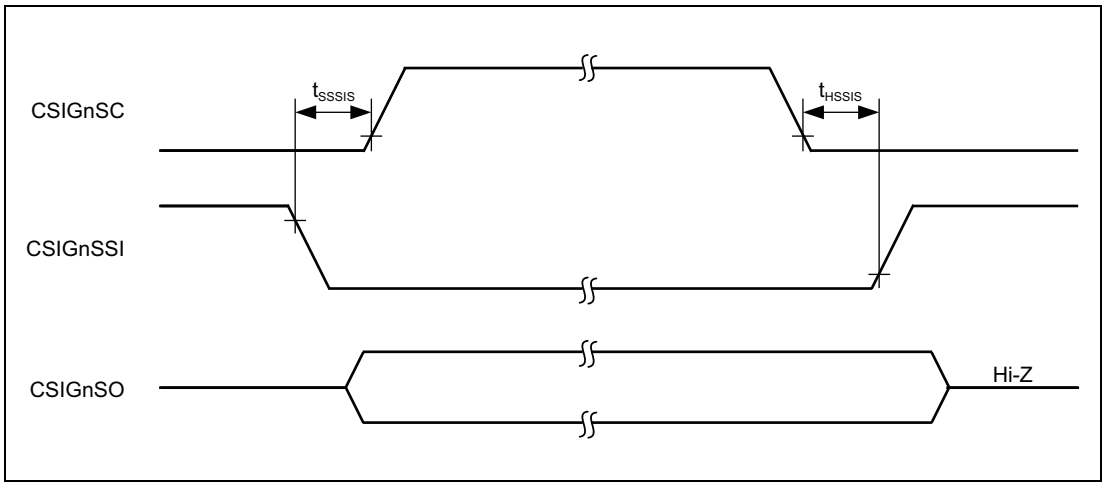


Figure 1.37 CSIGn Slave Mode Timing (d): Slave Select Ctrl Input (CSIGnSSI) - Inverted Clock

(5) [CSIG0SC] Input Pin and [CSIG0RY] Output Pin in Slave Mode

Note: Settings: CSIG0CFG0.CSIG0CKP = 0, CSIGnCTL1.CSIGnCKR = 0 (consider CSIGnCFG0.CSIGnDAP bit)

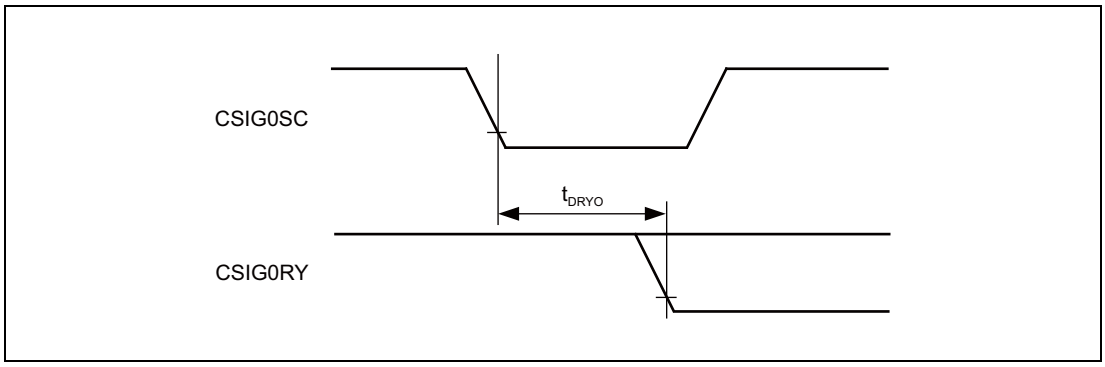


Figure 1.38 CSIGn Slave Mode Timing (e): Ready / Busy Output Signal (CSIGnRY)

(6) [CSIG0SC] Input Pin and [CSIG0RY] Output Pin in Slave Mode

Note: Settings: CSIG0CFG0.CSIG0CKP = 0, CSIGnCTL1.CSIGnCKR = 1 (consider CSIGnCFG0.CSIGnDAP bit)

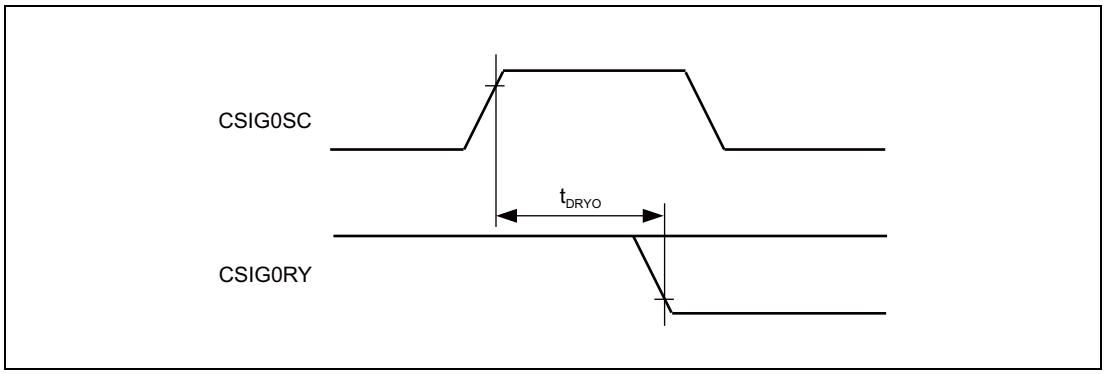


Figure 1.39 CSIGn Slave Mode Timing (f): Ready / Busy Output Signal (CSIGnRY) - Inverted Clock

(7) [CSIGnSO] Output Pin and [CSIGnSC / CSIGnSI] Input Pins in Slave Mode

Note: Settings: CSIG0CFG0.CSIG0CKP = 1, CSIGnCTL1.CSIGnCKR = 0 (consider CSIGnCFG0.CSIGnDAP bit)

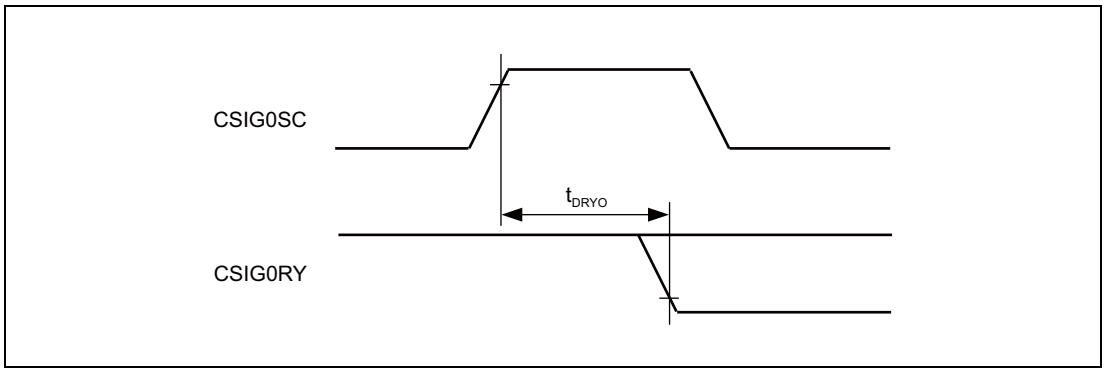


Figure 1.40 CSIGn Slave Mode Timing (g): Ready / Busy Output Signal (CSIGnRY)

(8) [CSIG0SC] Output Pin and [CSIGnSC / CSIGnSI] Input Pins in Slave Mode

Note: Settings: CSIG0CFG0.CSIG0CKP = 1, CSIGnCTL1.CSIGnCKR = 1 (consider CSIGnCFG0.CSIGnDAP bit)

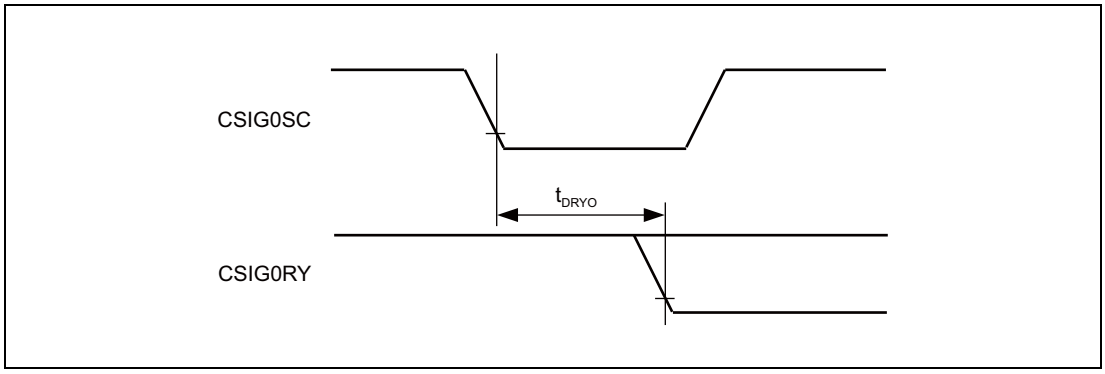


Figure 1.41 CSIGn Slave Mode Timing (h): Ready / Busy Output Signal (CSIGnRY) - Inverted Clock

(9) [CSIGnSC, CSIGnDCS] Input Pins in Slave Mode

Note: Settings: CSIGnCTL1.CSIGnDCS = 1, CSIGnCTL1.CSIGnCKR = 0 (consider CSIGnCFG0.CSIGnDAP bit)

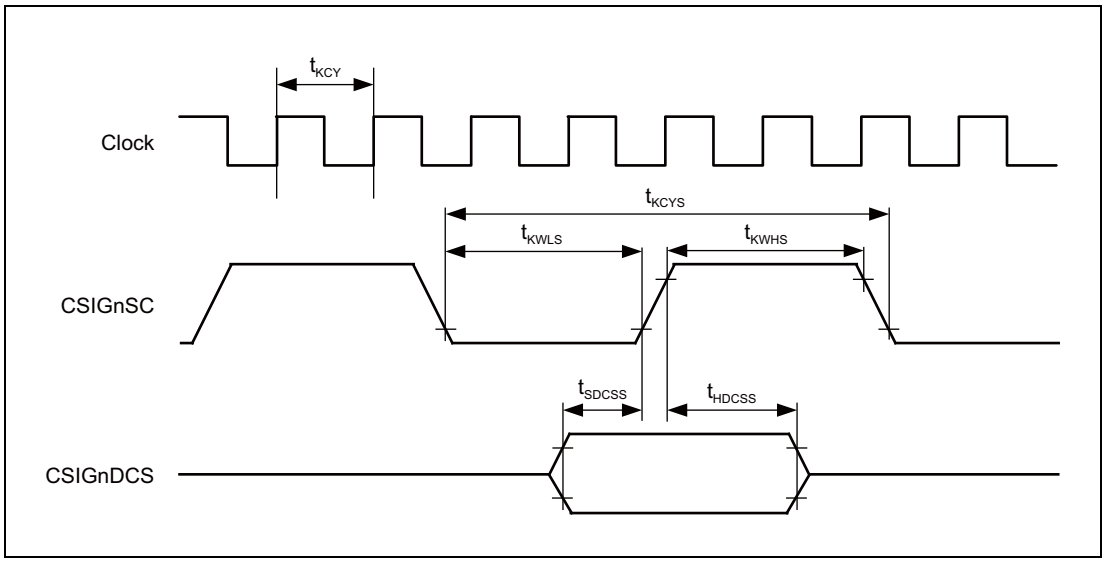


Figure 1.42 CSIGn Slave Mode Timing (h): Data Consistency Check (CSIGnDCS).CSIGnDAP bit)

(10) [CSIGnSC, CSIGnDCS] Input Pins in Slave Mode

Note: Settings: CSIGnCTL1.CSIGnDCS = 1, CSIGnCTL1.CSIGnCKR = 0 (consider CSIGnCFG0.CSIGnDAP bit)

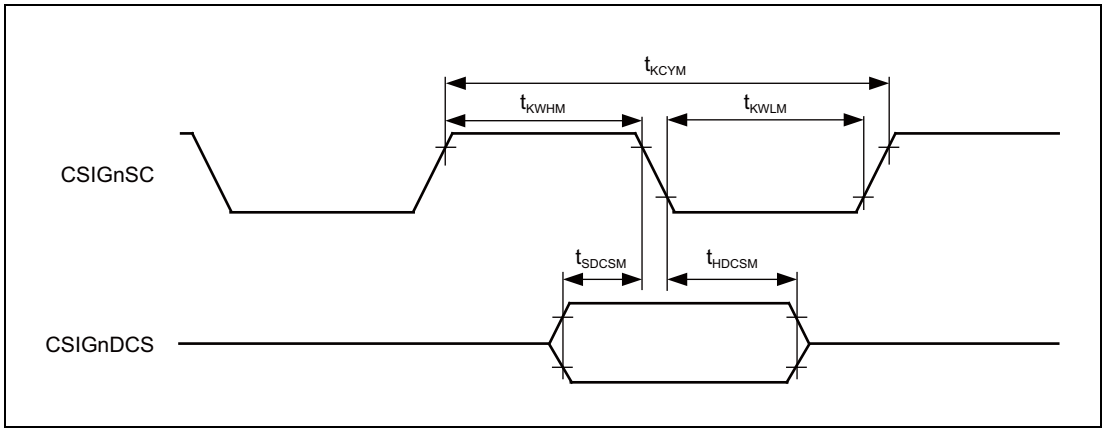
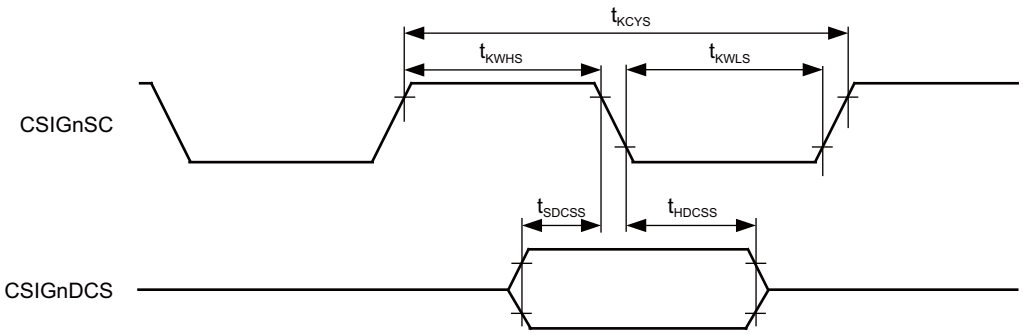
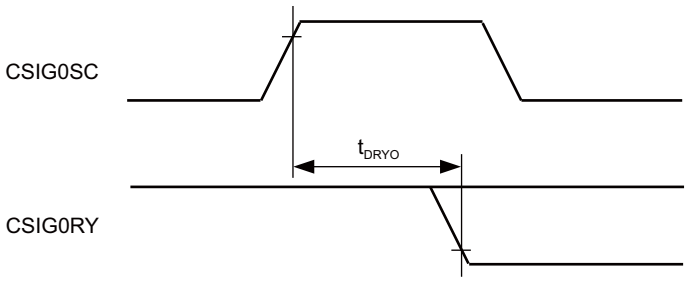


Figure 1.43 CSIGn Slave Mode Timing (i): Data Consistency Check (CSIGnDCS).CSIGnDAP bit) - Inverted Clock



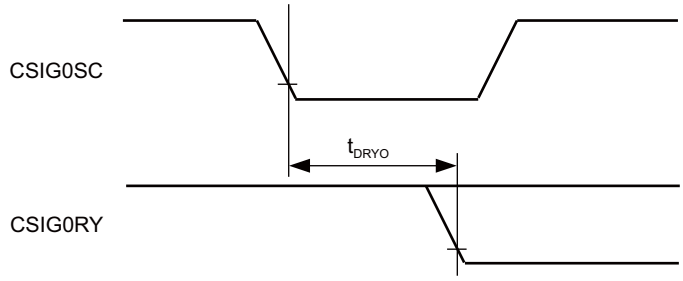
Note: Settings: CSIGnCTL1.CSIGnDCS = 1, CSIGnCTL1.CSIGnCKR = 1
(consider CSIGnCFG0.CSIGnDAP bit)

Figure 1.44 Slave Mode Wave Form6



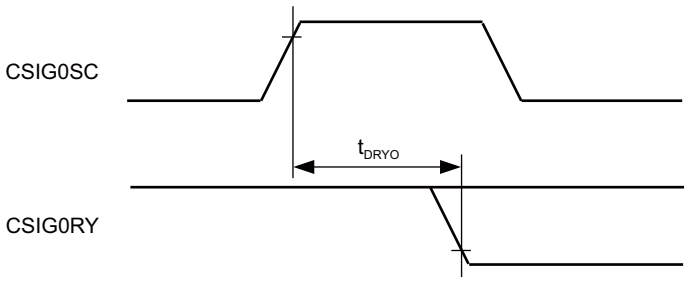
Note: Settings: CSIG0CFG0.CSIG0CKP = 0, CSIGnCTL1.CSIGnCKR = 1
(consider CSIGnCFG0.CSIGnDAP bit)

Figure 1.45 Slave Mode Wave Form7



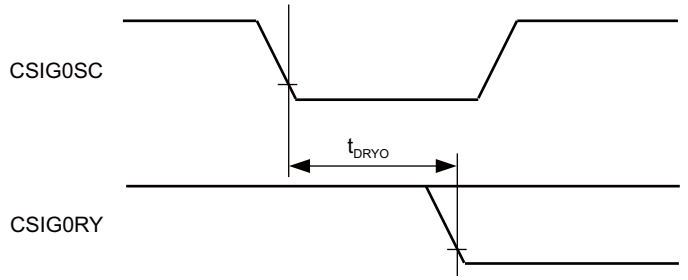
Note: Settings: CSIG0CFG0.CSIG0CKP = 0, CSIGnCTL1.CSIGnCKR = 0
(consider CSIGnCFG0.CSIGnDAP bit)

Figure 1.46 Slave Mode Wave Form8



Note: Settings: CSIG0CFG0.CSIG0CKP = 1, CSIGnCTL1.CSIGnCKR = 0
(consider CSIGnCFG0.CSIGnDAP bit)

Figure 1.47 Slave Mode Wave Form9



Note: Settings: CSIG0CFG0.CSIG0CKP = 1, CSIGnCTL1.CSIGnCKR = 1
(consider CSIGnCFG0.CSIGnDAP bit)

Figure 1.48 Slave Mode Wave Form10

1.10.3 Synchronous Interface CSIH

1.10.3.1 Master Mode

Table 1.57 Master Mode AC Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
PCLK frequency	t_{KCYf}				80	MHz
PCLK cycle time	t_{KCY}		12.5			ns
Clock output cycle time	t_{KCYM}		50.0			ns
Clock output high level width	t_{KWHM}		$0.5 \times t_{KCYM} - 10.0$			ns
Clock output low level width	t_{KWLM}		$0.5 \times t_{KCYM} - 10.0$			ns
Data input setup time	t_{SSIM}	filtered (DNF)	$17 + t_{dDNFSI(max)}$			ns
		filter-bypassed	17			ns
Data input hold time	t_{HSIM}	filtered (DNF)	$0 - t_{dDNF(max)}$			ns
		filter-bypassed	0			ns
Data output delay max time	t_{DSOM}				5.0	ns
Data output delay min time	t_{HSOM}		–10			ns
Ready / Busy input signal (CSIHnRY) setup time	t_{SRYI}	filtered (DNF)	$2 \times t_{KCY} + t_{dDNF(max)} + 16.6$			ns
		filter-bypassed	$2 \times t_{KCY} + 16.6$			ns
Ready / Busy input signal (CSIHnRY) high level width	t_{WRYI}	filtered (DNF)	$t_{KCY} + t_{dDNFRY(max)} - 5$			ns
		filter-bypassed	$t_{KCY} - 5$			ns
CSS signal (CSIHnCSS) inactive width	t_{WSCSB}		$CSIDLE \times t_{KCY} - 5$			ns
CSS signal (CSIHnCSS) setup time	t_{SSCSB0}	CSIHnDAP=0	$CSSETUP \times t_{KCY} - 24$			ns
		CSIHnDAP=1	$(CSSETUP + 0.5) \times t_{KCY} - 24$			ns
CSS signal (CSIHnCSS) hold time	t_{HSCSB0}	CSIHnSIT=0	$CSHOLD \times t_{KCY} - 3$			ns
		CSIHnSIT=1	$(CSHOLD + 0.5) \times t_{KCY} - 3$			ns

Remark: CSIDLE: setting value of CSIHnCFGx.CSIHnIDx0-2
CSSETUP: setting value of CSIHnCFGx.CSIHnSPx3-0
CSHOLD: setting value of CSIHnCFG0-7.CSIHnHDx3-0

Timing waveforms are same as master mode of CSIH (except CSS).

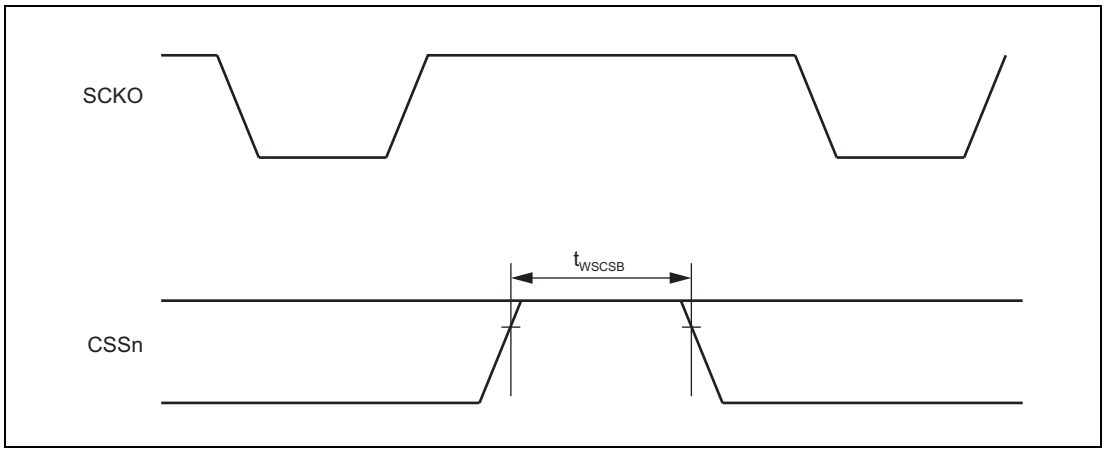
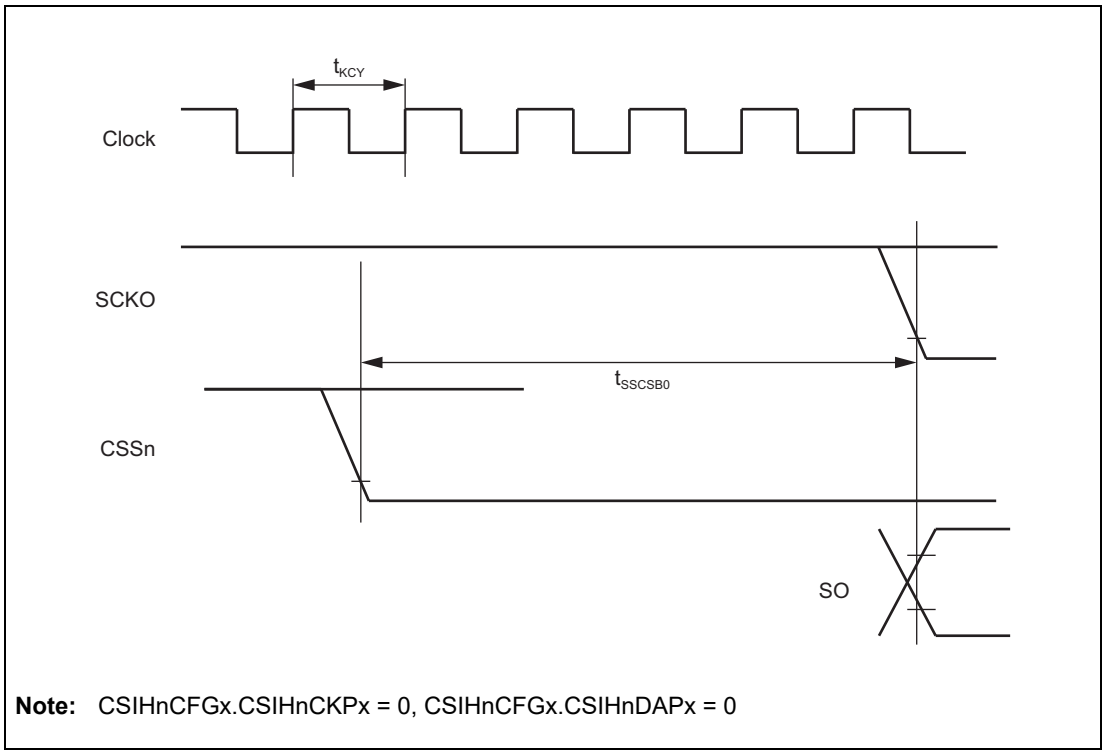
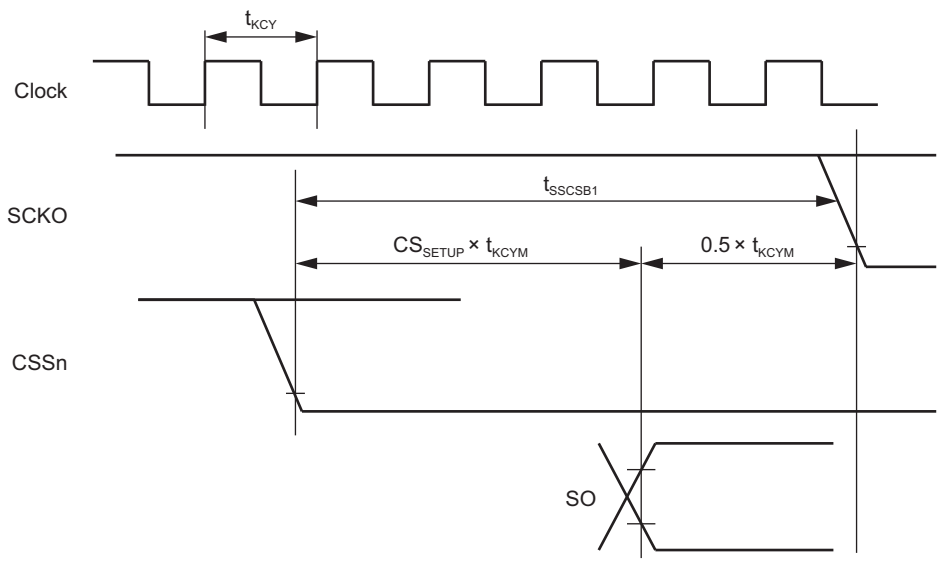


Figure 1.49 CSIH Master Mode Wave Form1



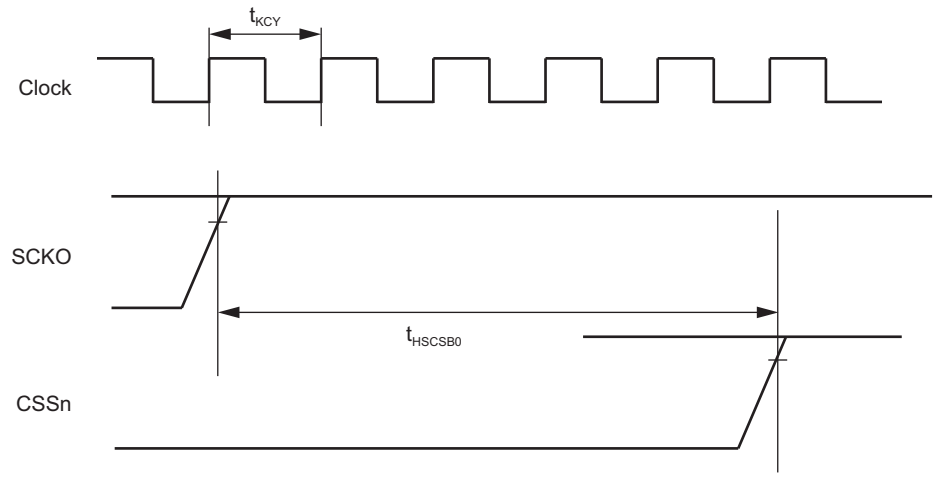
Note: CSIHnCFGx.CSIHnCKPx = 0, CSIHnCFGx.CSIHnDAPx = 0

Figure 1.50 CSIH Master Mode Wave Form2



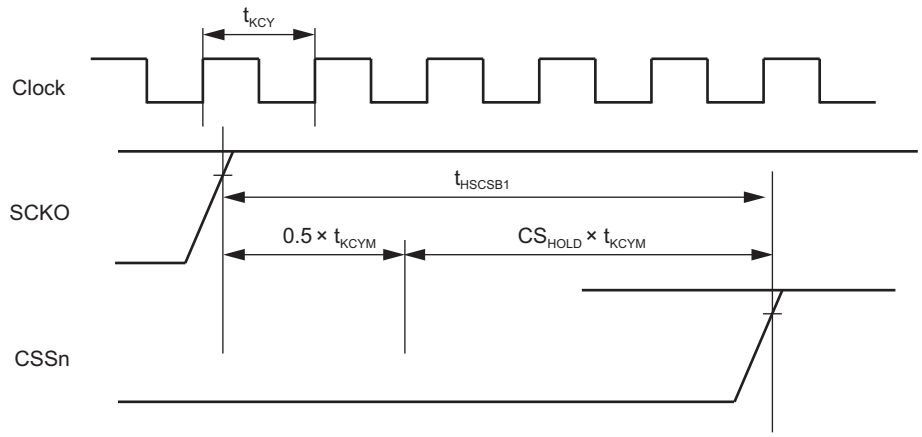
Note: CSIHnCFGx.CSIHnCKPx = 0, CSIHnCFGx.CSIHnDAPx = 1

Figure 1.51 CSIH Master Mode Wave Form3



Note: CSIH0CTL1.CSIH0SIT = 0, CSIHnCFGx.CSIHnCKPx = 0, CSIHnCFGx.CSIHnDAPx = 0

Figure 1.52 CSIH Master Mode Wave Form4



Note: CSIH0CTL1.CSIH0SIT = 1, CSIHnCFGx.CSIHnCKPx = 0, CSIHnCFGx.CSIHnDAPx = 0

Figure 1.53 CSIH Master Mode Wave Form5

1.10.3.2 Slave Mode

Table 1.58 Slave Mode AC Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
PCLK frequency	t_{KCYf}				80	MHz
PCLK cycle time	t_{KCY}		12.5			ns
Clock input cycle time	t_{KCYM}	filtered (DNF)	$6 \times t_{dDNFSCI(max)}$			ns
		filter-bypassed	75			ns
Clock input high level width	t_{KWHS}	filtered (DNF)	$3 \times t_{dDNFSCI(max)} - 5$			ns
		filter-bypassed	35			ns
Clock input low level width	t_{KWLS}	filtered (DNF)	$3 \times t_{dDNFSCI(max)} - 5$			ns
		filter-bypassed	35			ns
Data input setup time	t_{SSIS}	filtered (DNF)	$7 + t_{dDNFSCI(min)} - t_{dDNFSI(max)}$			ns
		filter-bypassed	7.5			ns
Data input hold time	t_{HSIS}	filtered (DNF)	$7 + t_{KCY} + t_{dDNFSCI(max)} - t_{dDNFSI(min)}$			ns
		filter-bypassed	$7.5 + t_{KCY}$			ns
Data output delay time	t_{DSOS}	filtered (DNF)			$32.5 + t_{dDNFSCI(max)}$	ns
		filter-bypassed			32.5	
Slave select control input signal setup time	t_{SSSIS}	filtered (DNF)	$0.5 \times t_{KCYS} + t_{dDNFSCI(min)} - t_{dDNFSI(max)} - 7$			ns
		filter-bypassed	0.5 x tKCYS – 5			ns
Slave select control input signal hold time	t_{HSSIS}	filtered (DNF)	$7 + t_{KCY} + t_{dDNFSCI(max)} - t_{dDNFSI(min)}$			ns
		filter-bypassed	$7.5 + t_{CKYS} - 5$			ns
Ready / Busy output signal (CSIH0RY) output delay time	t_{DRYO}	filtered (DNF)			$32.5 + t_{KCY} + t_{dDNFSCI(max)}$	ns
		filter-bypassed			$32.5 + t_{KCY}$	ns

Timing waveforms are same as slave mode of CSIG.

1.10.4 FLSCI3

Table 1.59 FLSCI3 AC Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Transfer rate	t_{FLSCI3}				2000.0	Kbps

1.10.5 I²C Bus Interface

Condition: AWO = powered, ISO = powered
BnVDD = 3.0 to 5.5 V, RVCC=3.0 to 3.6 V
Measurement according to **Section 1.3.1, AC Characteristic Measurement Condition**.
The input timings are valid if the digital filter is bypassed.
The current I²C implementation complies with the I²C bus format (*Philips 1995 update Ver.2.1, Rev. June 5, 1996*). High speed (HS) mode is not supported.

Table 1.60 I²C AC Characteristics

Parameter	CT	Symbol	Normal Mode		Fast-speed Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCLn clock frequency	DS	f_{CLK}	0	100	0	400	kHz
Bus-free time (between stop/start conditions)		t_{BUF}	4.7	—	1.3	—	µs
Hold time[*1]		$t_{HD:STA}$	4.0	—	0.6	—	µs
SCLn clock low-level width		t_{LOW}	4.7	—	1.3	—	µs
SCLn clock high-level width		t_{HIGH}	4.0	—	0.6	—	µs
Setup time for start/restart conditions		$t_{SU:STA}$	4.7	—	0.6	—	µs
Data hold time CBUS compatible master		$t_{HD:DAT}$	5.0	—	-	—	µs
Data hold time I²C mode			0[*2]	3.45[*3]	0[*2]	0.9[*3]	µs
Data setup time		$t_{SU:DAT}$	250		100[*4]		ns
STOP condition setup time		$t_{SU:STO}$	4.0		0.6		µs
Noise suppression[*5]		t_{SP}				t_{IICLK}[*6]	ns
Capacitive load of each bus line		C_b		400		400	pF

Note 1. At the start condition, the first clock pulse is generated after the hold time

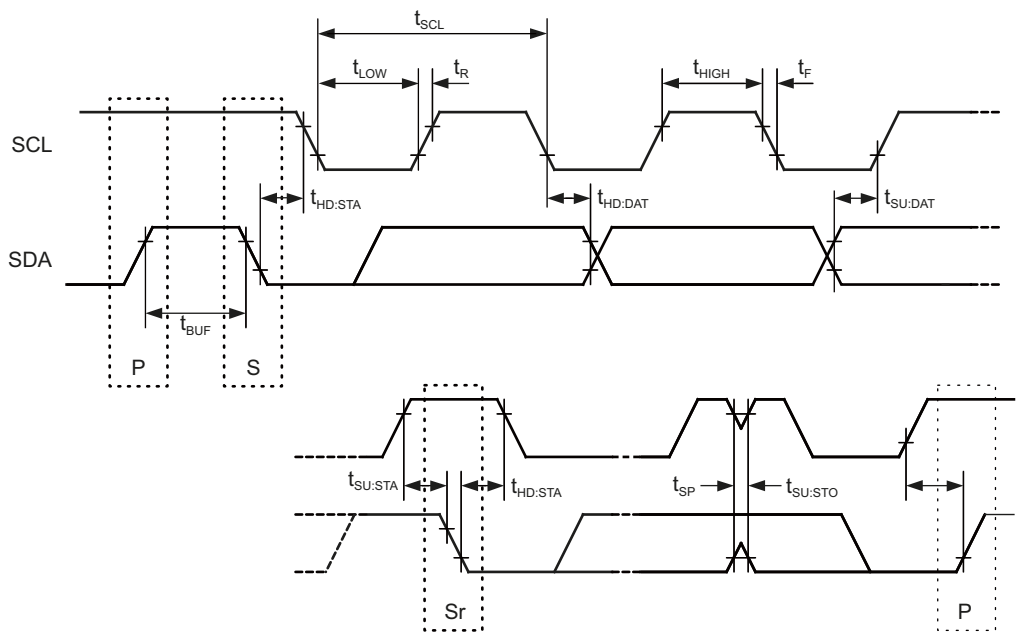
Note 2. The system requires a minimum of 300ns hold time internally for the SDA signal (at VIHmin of SCLn signal) in order to occupy the undefined area at the falling edge of SCLn.

Note 3. If the system does not extend the SCL0 signal low hold time (tlow), only the maximum data hold time ($t_{HD:DAT)}$ needs to be satisfied.

Note 4. The fast-speed-mode IIC bus can be used in a normal-mode IIC bus system.
In this case, set the fast-speed-mode IIC bus so that it meets the following conditions:
- If the system does not extend the SCL0n signal's low state hold time: $t_{SU:DAT} \geq 250$ ns
- If the system extends the SCL0n signal's low state hold time:
Transmit the following data bit to the SDA0 line prior to releasing the SCL0 line
($t_{Rmax.} + t_{SU:DAT} = 1000 + 250 = 1250$ ns: Normal mode IIC bus specification).

Note 5. Noise suppression is only available in Fast-speed mode.

Note 6. t_{IICLK} is the period of the IICLK supplied by the clock controller.



Note 1. P: Stop condition
S: Start condition
Sr: Restart condition

Note 2. Rise and Fall time depend on the actual load of the signal and the selected output current limit. For a capacitive load the time can be roughly calculated from:
(t_R = VOH / IOH × CL),
(t_F = VOH / IOL × CL)

Figure 1.54 I^2C Timing Waveform

1.10.6 SSIF (Serial Sound Interface)

Table 1.61 Audio Clock Input Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
External ACK inputs	t_{ACKI}	DNF used	100		1000	ns
		DNF not used	20		1000	ns
External ACK outputs	t_{ACKO}		41.667		531.25	ns

Table 1.62 IIS Master Mode Interface Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
SCK output cycle time	t_o	DNF used	200		64000	ns
		DNF not used	80		64000	ns
SCK high width	t_{HC}		0.45 × t_o		0.55 × t_o	ns
SCK low width	t_{LC}		0.45 × t_o		0.55 × t_o	ns
SCK outputs rise time	t_{RC}				30	ns
SDO/WS outputs delay time	t_{DTR}		–5		30	ns
SDI input setup time	t_{SR}	filtered (DNF)	25 + $t_{DNFSDI(max)}$			ns
		filter-bypassed	25			ns
SDI input hold time	t_{HTR}	filtered (DNF)	25 + $t_{DNFSDI(max)}$			ns
		filter-bypassed	25			ns

Table 1.63 IIS Slave Mode Interface Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
SCK input cycle time	t_i	DNF used	200		64000	ns
		DNF not used	80		64000	ns
SCK high width	t_{HC}		0.45 × t_i		0.55 × t_i	ns
SCK low width	t_{LC}		0.45 × t_i		0.55 × t_i	ns
SCK inputs rise time	t_{RC}				30	ns
SDO outputs delay time	t_{DTR}		–5		30	ns
SDI/WS input setup time	t_{SR}	filtered (DNF)	25 + $t_{DNFSDI(max)}$			ns
		filter-bypassed	25			ns
SDI/WS input hold time	t_{HTR}	filtered (DNF)	25 + $t_{DNFSDI(max)}$			ns
		filter-bypassed	25			ns

1.10.7 PCM-PWM Converter (PCMP)

Table 1.64 PCM-PWM Converter Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Output frequency of High-speed PWM	f_{PWMOP}		10		60	kHz
Output period time	f_{PWMOP}		16.67			µs
Output time difference for each PWM outputs	t_{ANOD}, t_{BNOD}		–10.0		10.0	ns

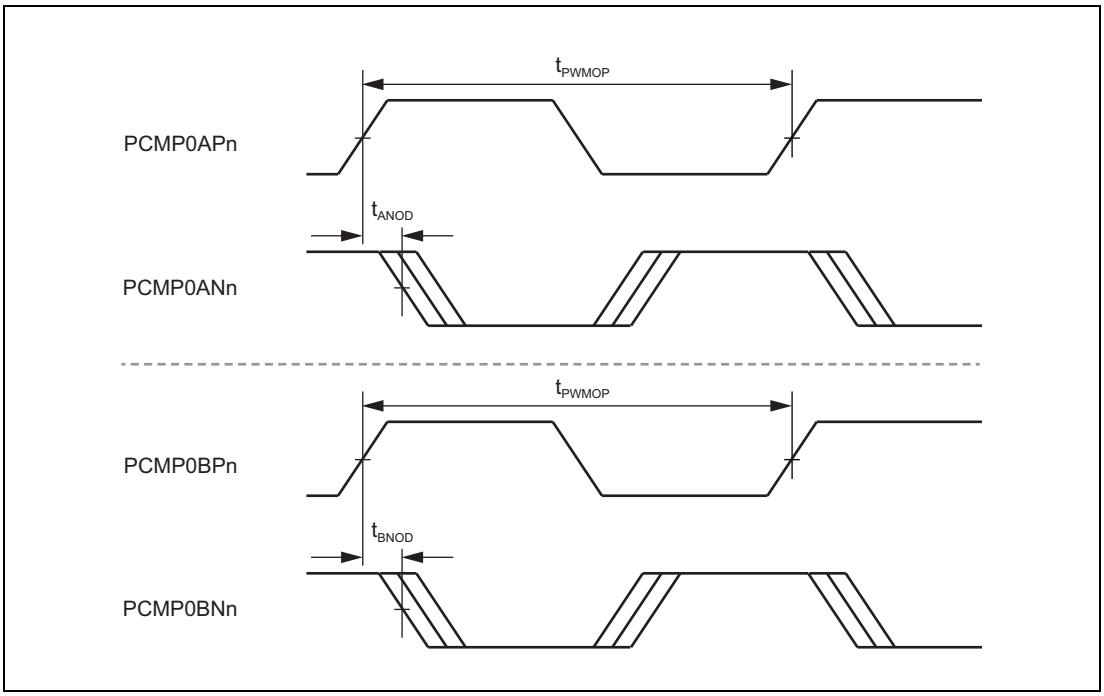


Figure 1.55 PCM-PWM Timing Waveform

1.10.8 RS-CAN Interface

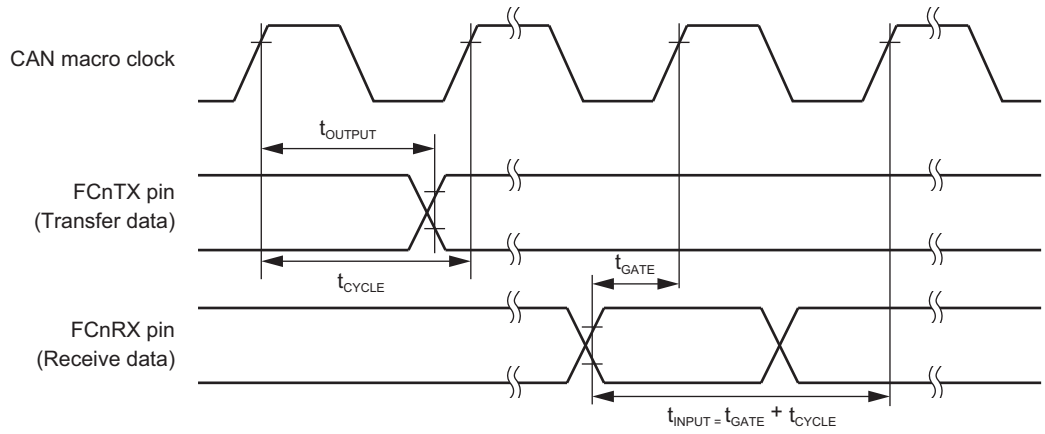
Condition: AWO = powered, ISO = powered
EVDD = 3.0 to 5.5 V
Measurement according to **Section 1.3.1, AC Characteristic Measurement Condition**.
The input timings are valid if the digital filter is bypassed.

Table 1.65 CAN AC Characteristics

Parameter	CT	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Transfer rate	DS	t_{FCNn}	Regular CAN			1000	Kbps
Internal delay time		t_{INTDEL}	Regular CAN			37.5	ns
CAN Node Delay time		t_{NODE}	t_{CYCLE} = 62.5 ns, regular CAN			100	ns

NOTE

The CAN module of this device is conform to ISO 11898-1. Additionally it is tested according to CAN Conformance Specification (i.e. ISO16845).



Note: CAN node delay time (t_{NODE})
= INPUT delay time (t_{INPUT}) + Output delay time (t_{OUTPUT})
Internal delay time (t_{INTDEL})
= Internal gate delay time (t_{GATE}) + Output delay time (t_{OUTPUT})

Figure 1.56 CAN Interface Waveform

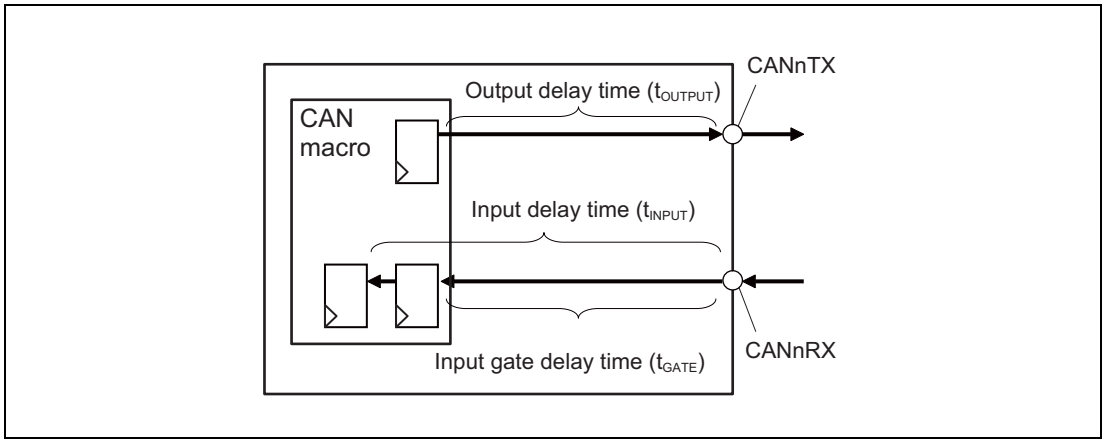


Figure 1.57 CAN Delay Time Definition

1.10.9 CAN-FD Interface

Table 1.66 CAN-FD AC Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Transfer rate	DS	t_{FCNn}			8000	Kbps
CAN-FD Node Delay time		t_{NODE}			50	ns

Note: CAN node delay time (t_{NODE})
= INPUT delay time (t_{INPUT}) + Output delay time (t_{OUTPUT})

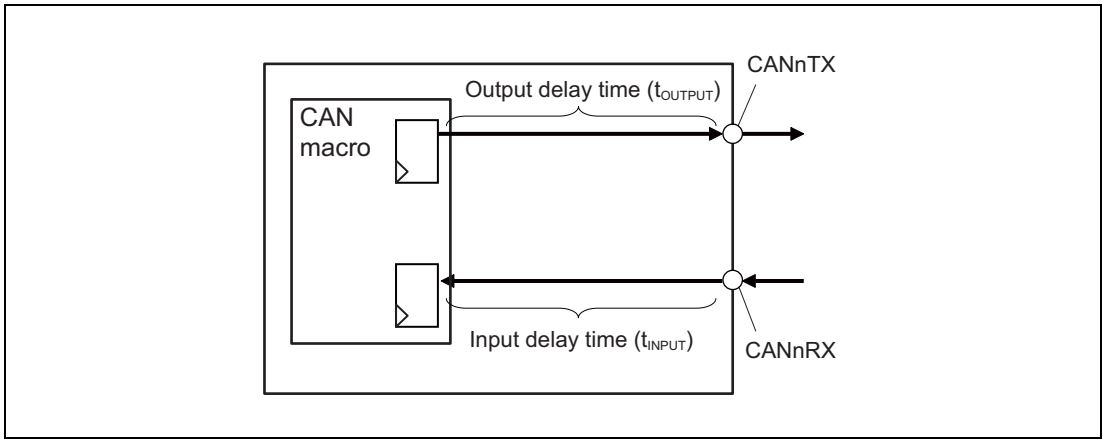


Figure 1.58 CAN-FD Delay Time Definition

1.11 Graphic Module Operating Conditions

1.11.1 LCD Bus Interface (LCBI)

Table 1.67 RAM Operation Mode AC Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Cycle time (transfer period)	t_{CYCr}*1	slow mode	CYC_{slow} × T – 5			ns
		fast mode	CYC_{fast} × T – 5			ns
Address setup time (WRITE mode: A0 falling to CSZ&WRZ falling) (READ mode: A0 falling to CSZ&RDZ falling)	t_{ASr}	slow mode	(TIAD + TIDW + 2) × T			ns
		fast mode	0			ns
Address hold time (WRITE mode: WRZ rising to A0&CSZ rising) (READ mode: RDZ rising to A0&CSZ rising)	t_{AHr}	slow mode	(TIDZ + 1) × T – 10			ns
		fast mode				
WRITE strobe LOW pulse width	t_{WRZLr}	slow mode	(TIWR + 1) × T – 10			ns
		fast mode				
WRITE strobe HIGH pulse width	t_{WRZHr}	slow mode	(TIAD + TIDW + TIDZ + 3) × T – 10			ns
		fast mode	(TIDZ + 1) × T – 10			ns
READ strobe LOW pulse width	t_{RDZLr}	slow mode	((TIRD + 1) × T – 10			ns
		fast mode				
READ strobe HIGH pulse width	t_{RDZHr}	slow mode	(TIAD + TIDW + TIDZ + 3) × T – 10			ns
		fast mode	(TIDZ + 1) × T – 10			ns
Data output setup time (WRITE mode) D[7:0] to CSZ&WRZ falling	t_{DOSr}	slow mode			(TIDW + 1) × T	ns
		fast mode			0	ns
Data output hold time (WRITE mode) WRZ rising to D[7:0]	t_{DOHr}	slow mode	(TIDZ + 1) × T – 10			ns
		fast mode				
Data input setup time (READ mode) D[7:0] to CSZ&RDZ rising	t_{DISr}	slow mode	50.0			ns
		fast mode				
Data input hold time (READ mode) D[1:0] from CSZ&RDZ rising	t_{DIHr}	slow mode	1 × T			ns
		fast mode	1 × T			
Output disable Time (WRITE mode to READ mode) D[7:0] Hi-Z to RDZ falling	t_{ODr}	slow mode	(TIAD + TIDW + 2) × T			ns
		fast mode	0.0			ns

Note 1. The parameters CYCslow respectively CYCfast, as well as the parameter T are set as described in *the UM Section 36.3.1.2, Transfer Speed*.
Where the transfer period CYCr (depending on slow or fast mode named CYCslow or CYCfast) corresponds to the settings of the LCBInBCYC register.
Likewise the time for one step of a transfer period T corresponds to the settings of the LCBInCKSEL register, means the PCLK divider setting.

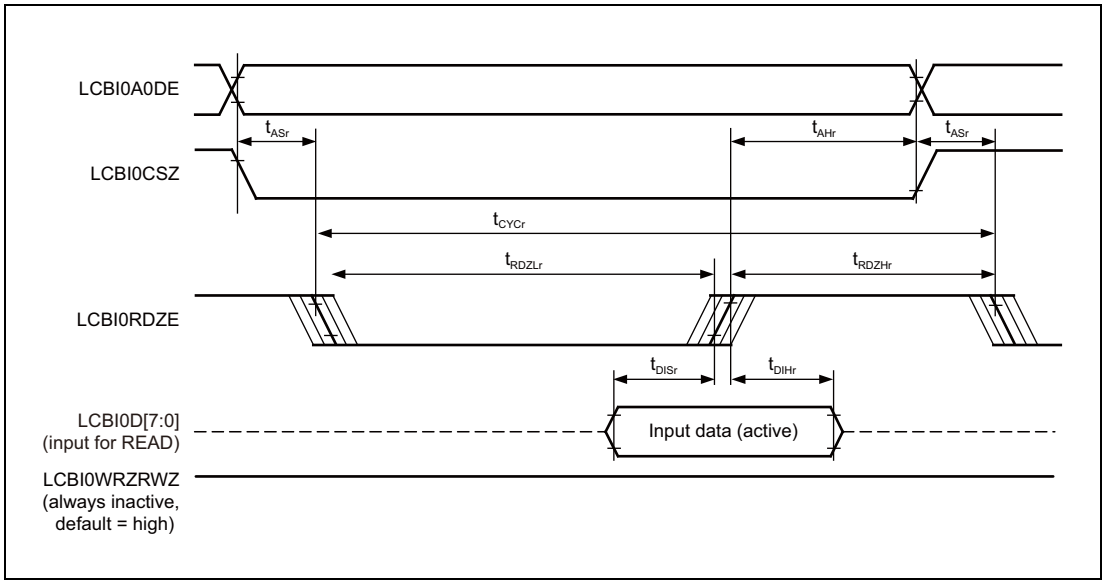


Figure 1.59 LCD Bus Interface RAM Operation Mode (READ)

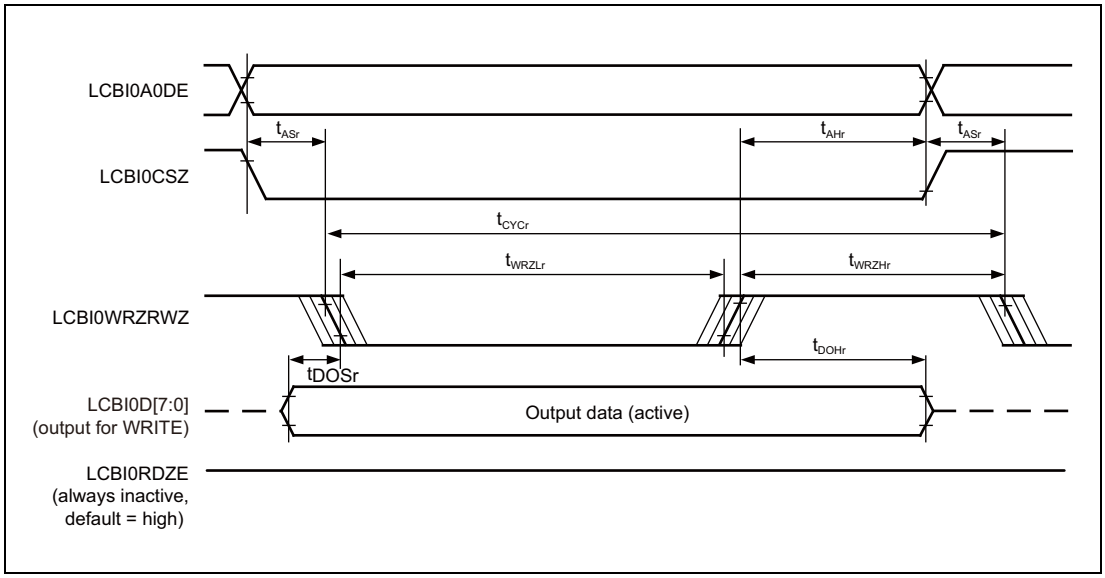


Figure 1.60 LCD Bus Interface RAM Operation Mode (WRITE)

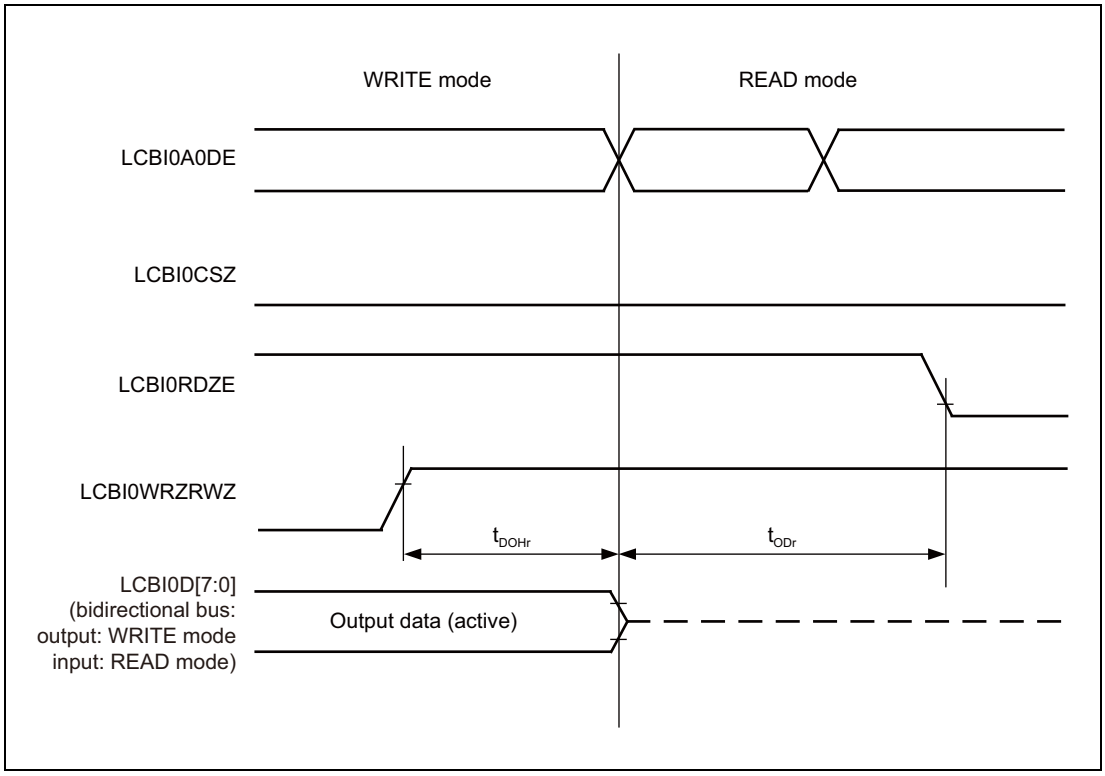


Figure 1.61 LCD Bus Interface RAM Operation Mode (WRITE/READ switch)

Table 1.68 E-type Operation Mode AC Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Cycle time (transfer period)	t_{CYCe}	slow mode	CYC_{slow} × T – 5			ns
		fast mode	CYC_{fast} × T – 5			ns
Address setup time (A0 falling to CSZ&E falling)	t_{ASe}	slow mode	(TMAD + TMDW + 2) × T			ns
		fast mode	0			ns
Address hold time (WRZ rising to A0&CSZ rising)	t_{AHe}	slow mode	(TMDZ + 1) × T – 10			ns
		fast mode				
Enable control signal LOW pulse width	t_{ENRLe}/ t_{ENWLe}	slow mode	(TMED + 1) × T – 10			ns
		fast mode				
Enable control signal HIGH pulse width	t_{ENRHe}/ t_{ENWHe}	slow mode	(TMAD + TMDW + TMDZ + 3) × T – 10			ns
		fast mode	(TMDZ + 1) × T – 10			ns
Data output setup time (WRITE mode) D[7:0]&WRZ to E falling	t_{DOSe}	slow mode			(TMDW + 1) × T	ns
		fast mode			0	ns
Data output hold time (WRITE mode) E rising to D[7:0]	t_{DOHe}	slow mode	(TMDZ + 1) × T – 10			ns
		fast mode				
Data input setup time (READ mode) D[7:0] to CSZ&E rising	t_{DISe}	slow mode	50.0			ns
		fast mode				
Data input hold time (READ mode) D[1:0] from CSZ&E rising	t_{DIHe}	slow mode	1 × T			ns
		fast mode	1 × T			ns
Output disable Time (WRITE mode to READ mode) D[7:0] Hi-Z to E falling	t_{ODe}	slow mode	(TMAD + TMDW + 2) × T			ns
		fast mode	0.0			ns

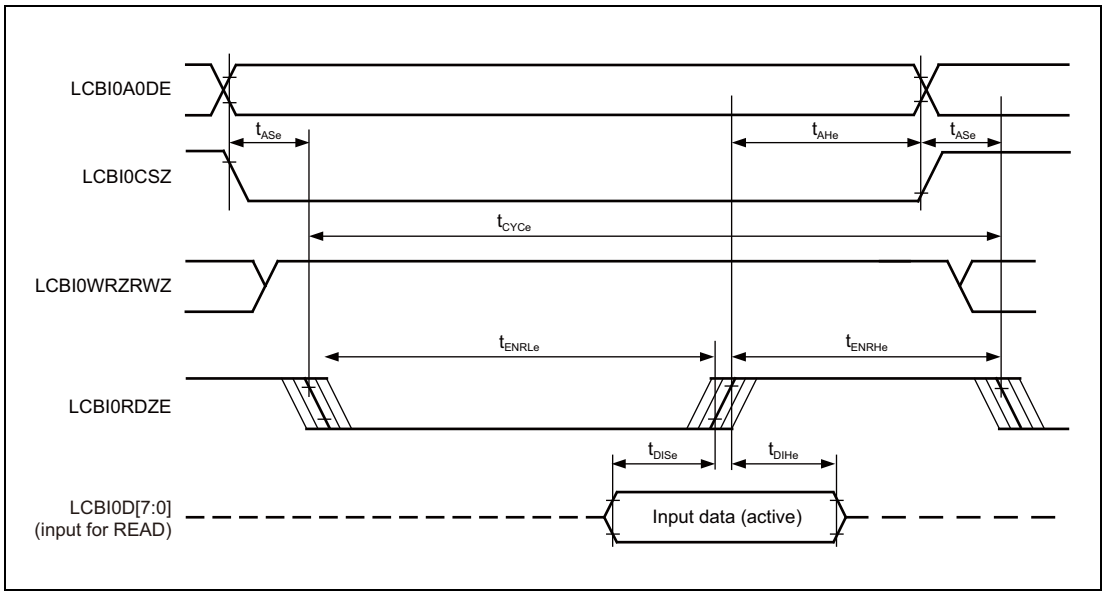


Figure 1.62 LCD Bus Interface E-type Operation Mode (READ)

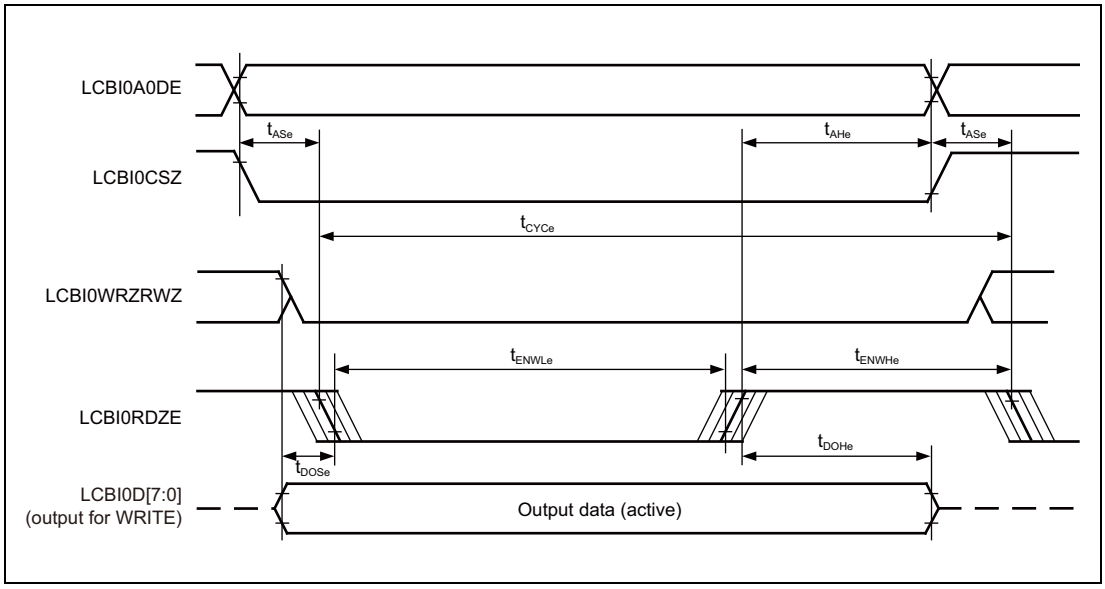


Figure 1.63 LCD Bus Interface E-type Operation Mode (WRITE)

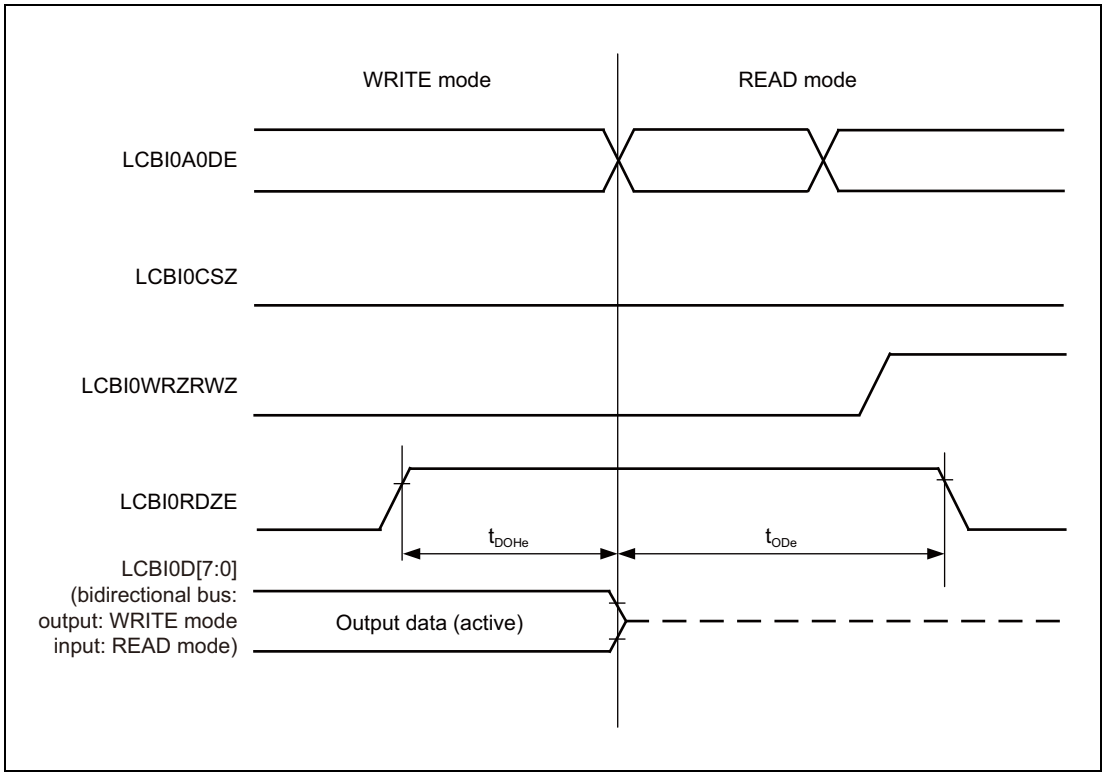


Figure 1.64 LCD Bus Interface E-type Operation Mode (WRITE/READ switch)

1.12 Flash Characteristics

1.12.1 Code Flash

The code flash memory is shipped in the erase state. If the code flash memory is read where it has not been written after erasure (no write condition), an ECC error is generated, resulting in the occurrence of an exception.

Condition: T_j = –40°C to $+T_{Jmax}$
AWO = powered, ISO = powered

Table 1.69 Basic Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Operation frequency	f_{PCLK}		4		60	MHz
Operation voltage (actual supply voltage is equal to REG1VCC)	V_{dd}		2.7		5.5	V
Number of rewrites	CWRT	Data retention of 20 years	1000.0			times
Programming temperature (Ta)	TPRG		–40.0		105.0	°C

Note: Retention period under average Ta = 85°C. This is the period starting on completion of a successful erasure of the code flash memory.

Table 1.70 Timing Characteristics

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Programming time		f_{PCLK} ≥ 20 MHz P/E < 100 times	256 B		2	6	ms
			8 KB		50	90	ms
			32 KB		200	360	ms
			128 KB		800	1440	ms
		f_{PCLK} ≥ 20 MHz P/E ≥ 100 times	256 B		2.4	7.2	ms
			8 KB		60	108	ms
			32 KB		240	432	ms
			128 KB		960	1728	ms
Erase Time		f_{PCLK} ≥ 20 MHz P/E < 100 times	8 KB		50	120	ms
			32 KB		200	480	ms
			128 KB		800	1750	ms
		f_{PCLK} ≥ 20 MHz P/E ≥ 100 times	8 KB		60	144	ms
			32 KB		240	576	ms
			128 KB		960	2100	ms

1.12.2 Data Flash

The data flash memory is shipped in the erased state. If the data flash memory is read where it has not been written after erasure (no write condition), an ECC error is generated, resulting in the occurrence of an exception.

Condition: T_j = –40°C to $+T_{Jmax}$
AWO = powered, ISO = powered

Table 1.71 Basic Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Operation frequency	f_{PCLK}		4		60	MHz
Operation voltage (actual supply voltage is equal to REG1VCC)	V_{dd}		2.7		5.5	V
Number of rewrites	CWRT	Data retention of 20 years	125 k			times
		Data retention of 3 years	250 k			times
Programming temperature (Ta)	TPRG		–40.0		105.0	°C

Note: Retention period under average Ta = 85°C. This is the period starting on completion of a successful erasure of the code flash memory.

Table 1.72 Timing Characteristics

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Programming time		f_{PCLK} ≥ 20 MHz	4 B		0.3	1.7	ms
			64 B		4.8	13	ms
Erase Time		f_{PCLK} ≥ 20 MHz	64 B		3	10	ms
			32 KB		1.6	5.2	s
Blank check time		f_{PCLK} ≥ 20 MHz	4 B			30	µs
			64 B			100	µs

1.13 Power Supply Current

1.13.1 Operation Current Consumption

Condition: T_j = –40°C to + T_{Jmax}
Vss = OSCVss = REGnVss = EVss = BnVss = ISMVss = ZPDVss = A0Vss = 0V
Clock setting:
CPU: 120 MHz, AXI: 60 MHz, APB: 60 MHz
IO current: The input/output current is mainly part of the special application use case and not covered in this “Power supply current”. Excluded from this are some currents that need to be considered separately.
Please apply both dynamic and static current for total current of each domain.
AWO = powered, ISO = powered

Table 1.73 Dynamic Current

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Operation Current of $REG0V_{CC}$	$I_{OREG0VCC}$	REG0VCC = 3.0 to 5.5 V			2	mA
Operation Current of $REG1V_{CC}$	$I_{OREG1VCC}$	REG1VCC = 3.0 to 5.5 V			70	mA

Remark: OSCVCC current depend on frequency and external logics for Main oscillator. Detail specs please refer to **Section 1.5.10.1, Main Oscillator**.

Table 1.74 Static Current

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Static Current of $REG0V_{CC}$	$I_{SREG0VCC}$	REG0VCC = 3.0 to 5.5 V			3	mA
Static Current of $REG1V_{CC}$	$I_{SREG1VCC}$	REG1VCC = 3.0 to 5.5 V			75	mA

1.13.2 Stand-by Current Consumption

Condition: T_j = –40°C to 85°C
Vss = OSCVss = REGnVss = EVss = BnVss = ISMVss = ZPDVss = A0Vss = 0 V
Clock setting:
f_{RL}: On
IO current: The input/output current is mainly part of the special application use case and not covered in this “Power supply current”. Excluded from this are some currents that need to be considered separately.
AWO = powered, ISO = Off.
Typ condition indicate following condition
- Each VCC set to 5.0 V
- T_j = 25°C
- Device = center condition

Table 1.75 Stand-by Current

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Operation Current of $OSCV_{CC}$	I_{OSCVCC}	f_{XT}: On, f_X: Off			4	µA
		f_{XT}: On, f_X: Off, Each VCC set to 5.0 V, T_j = 25°C			2	µA
		f_{XT}: Off, f_X: On[*1] Each VCC set to 5.0 V, T_j = 25°C			340	µA
		f_{XT}: Off, f_X: Off Possible to turn off			1	µA
Leakage Current of $REG1V_{CC}$	$I_{REG1VCC}$	Possible to turn off		2	3	µA
Leakage Current of $A0V_{REF}$	I_{A0VREF}	Possible to turn off < $A0V_{CC}$		0.1	1	µA
Operation Current of EV_{CC}	I_{EVCC}	T_j = 85°C		1	20	µA
		Each VCC set to 5.0 V, T_j = 25°C			1	µA
Leakage Current of ZPDVCC	I_{ZPDVCC}	Possible to turn off		0.1	2	µA

Note 1. Main oscillator current depend on frequency (AMPSEL setting) and external logics. Detail specs please refer to **Section 1.5.10.1, Main Oscillator**.

Section 2 Package

2.1 Junction-to-Ambient Resistance

The simplest method to determine the actual chip temperature is to use the single resistance metric of θja. The following equation may be used:

$$Tj = Ta + (Ptot \times \theta ja)$$

- Tj: is the chip junction temperature in [°C]
- Ta: is the ambient temperature (according to JEDEC standard JESD51-2A) in [°C]
- Ptot: is the total power consumption (refer to section DC characteristic) in [W]
- θja is the thermal resistance between junction and ambient in [°C/W]

This simple metric considers the test board properties in a natural convection environment. The thermal resistance is derived from a defined test fixture (JEDEC) or simulation of such test fixture using a 3D simulation with a detailed model. Since real application is usually quite different from this environment, the error in determining the maximum Tj can be quite big. The amount of deviation depends entirely on the application and can easily reach >30%.

A sufficient margin to Tjmax must be applied, considering the simulation error.

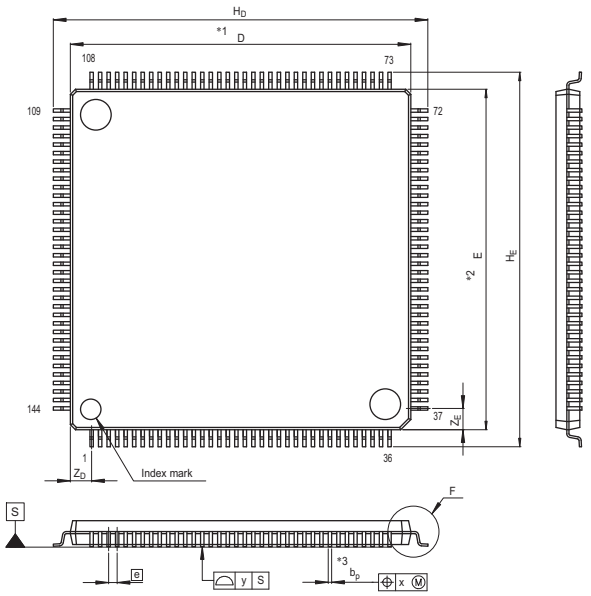
Table 2.1 Thermal resistance – Junction-to-ambient resistance

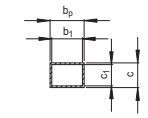
Device	Symbol	Condition	Package	Value	Unit
D1S1 (R7F701417)	θja	JEDEC	QFP144	37.9	°C/W

2.2 Device Packages

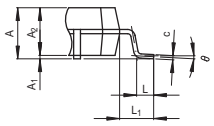
2.2.1 D1S1 Device (R7F701417)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP144-20x20-0.50	PLQP0144KA-A	144P6Q-A / FP-144L / FP-144LV	1.2g





Terminal cross section



Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.9	20.0	20.1
E	19.9	20.0	20.1
A_2	—	1.4	—
H_D	21.8	22.0	22.2
H_E	21.8	22.0	22.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure 2.1 144-pin Plastic QFP, 0.5 mm Pin-pitch

REVISION HISTORY	RH850/D1L/D1M Datasheet

Rev.	Date	Description	
		Page	Summary
1.00	Jan 07, 2019	—	First Edition issued

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