RC38312/RC38112

FemtoClock®3 Radio Synchronizer and Multi-Frequency Clock Synthesizer

Description

The RC38312/RC38112 is an ultra-low phase noise radio synchronizer, multi-frequency clock synthesizer, and digitally controlled oscillator (DCO). This flexible, low-power device outputs clocks with ultra-low in-band phase noise and spurious for 4G and 5G RF transceivers and with jitter below 25fs-rms for 112Gbps and 224Gbps SerDes.

Applications

- 5G radio units (RU)
- 5G distribution units (DU), switches, and routers
- Reference clock for 112Gbps and 224Gbps SerDes
- High-performance DCO for Precision Time Protocol (PTP) based clocks

Features

- Ultra-low phase noise synthesizer with jitter below 25fs RMS, 12kHz to 20MHz with 4MHz HPF
- Three independent low-phase noise sync domains
- Four independent low-phase noise frequency domains
- Support for JESD204B/C
- Time sync block with time to digital converter (TDC), time of day (TOD) counter, and PTP clocks
- 12 clock outputs with independent integer dividers
  - 8: LVDS, HCSL (AC-LVPECL) or CML
  - 4: LVDS, HCSL (AC-LVPECL) or LVCMOS
- Output frequency range:
  - CML: DC to 2.5GHz
  - LVDS or HCSL: DC to 1GHz
  - LVCMOS: DC to 250MHz
- Four differential or single-ended clock inputs
- Operates from a 1.8V supply.
- Clock inputs tolerate 1.8V input when the device is powered off, sinking less than 1mA
- CLKIN input frequency range: DC to 1GHz
- Time Sync TDC supports 1PPS and PP2S inputs
- DPLLs comply with ITU-T G.8262 and G.8262.1
- DPLL input-to-output phase variation ≤ 100ps
- DCO frequency resolution < 10^{-13}
- Package: 9 × 9 mm, 100-BGA

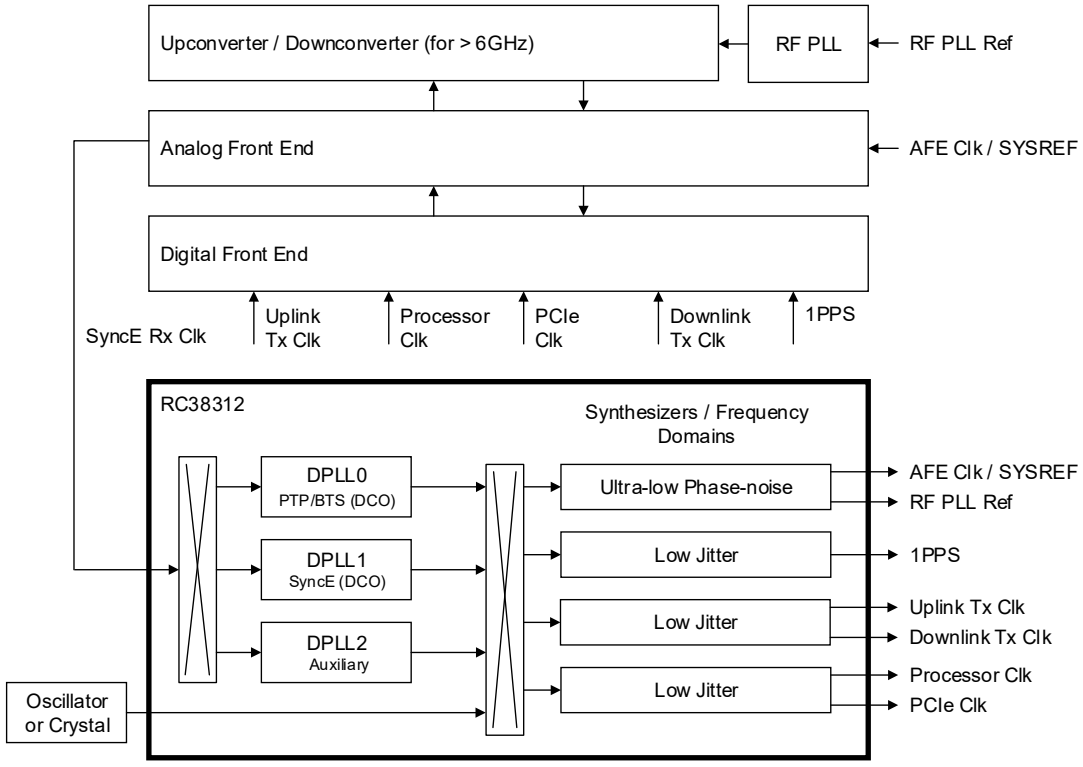


Figure 1. Typical 5G Radio Unit Use Case

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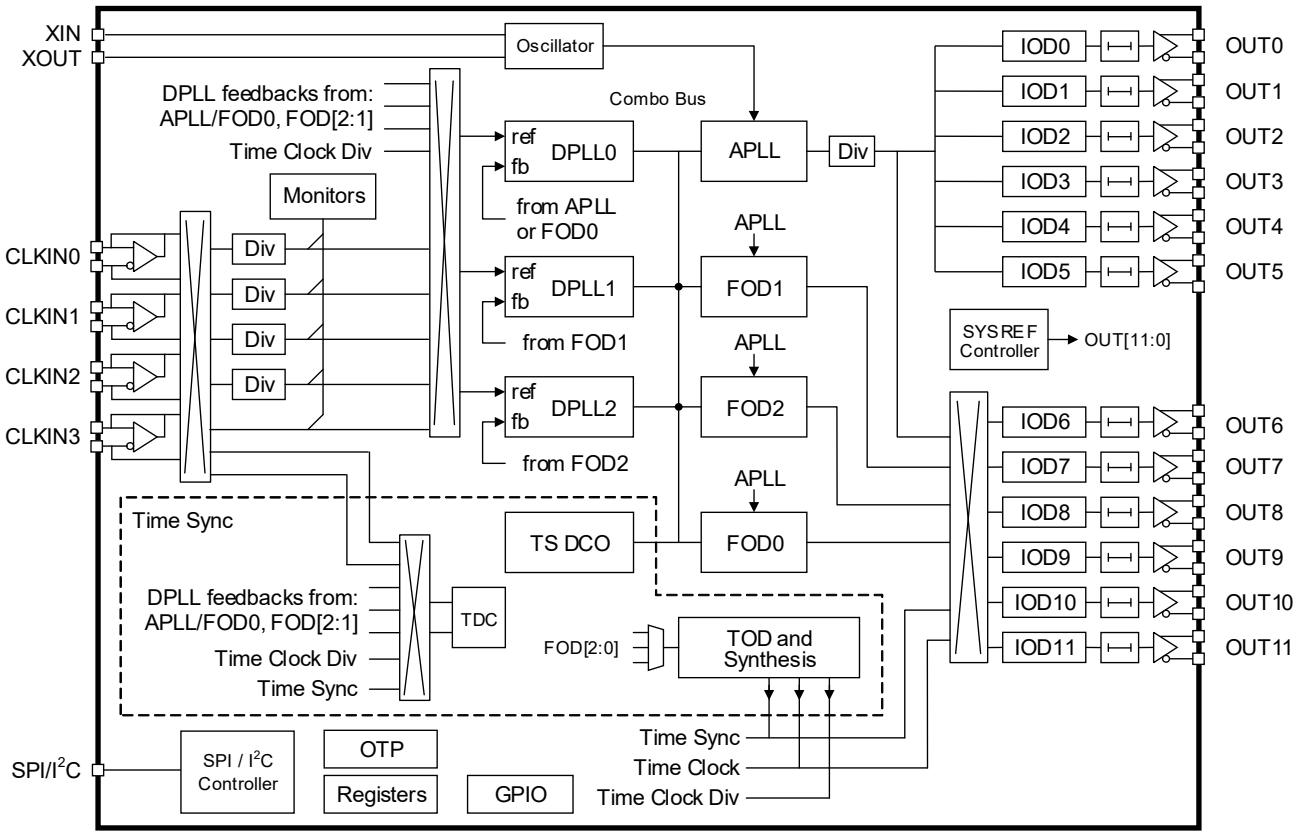


Figure 2. RC38312 Block Diagram

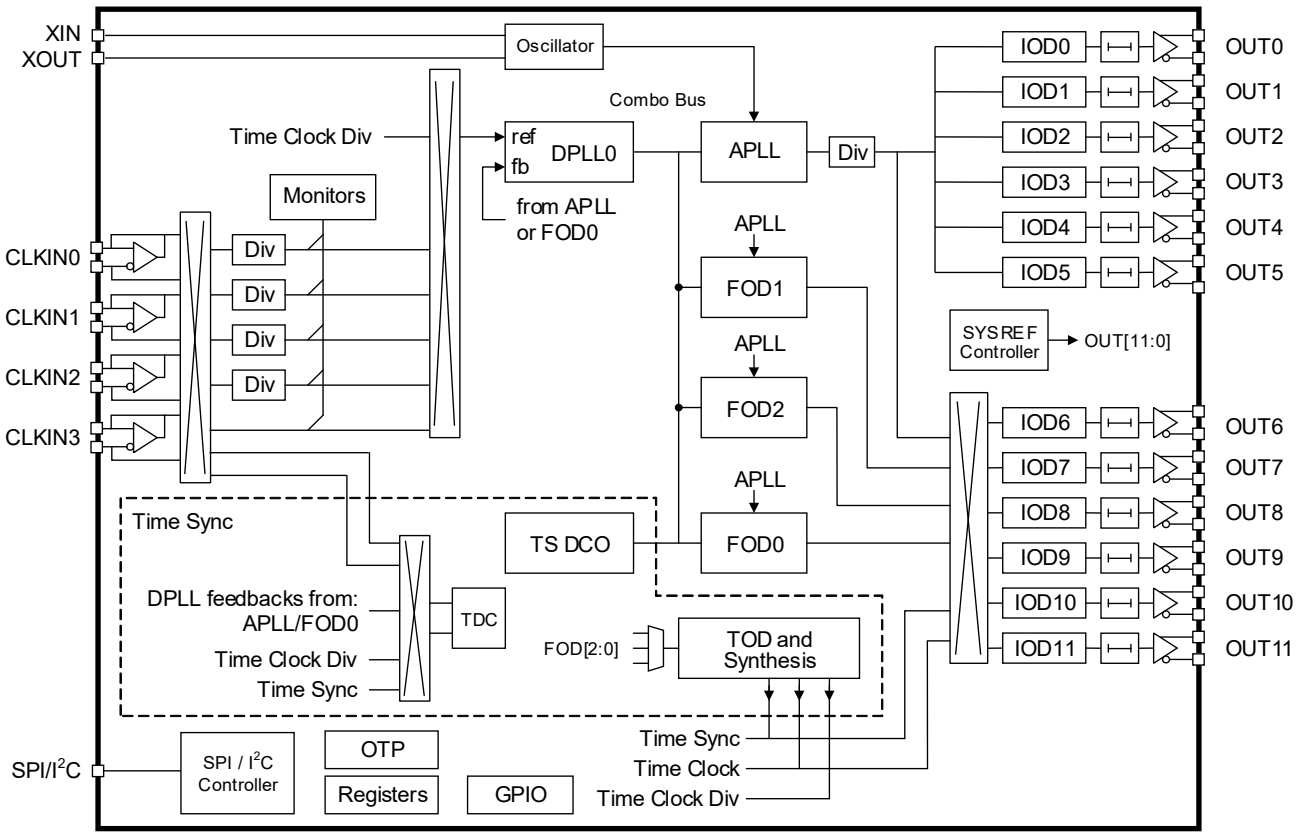


Figure 3. RC38112 Block Diagram

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1. Pin Information

1.1 Pin Assignments

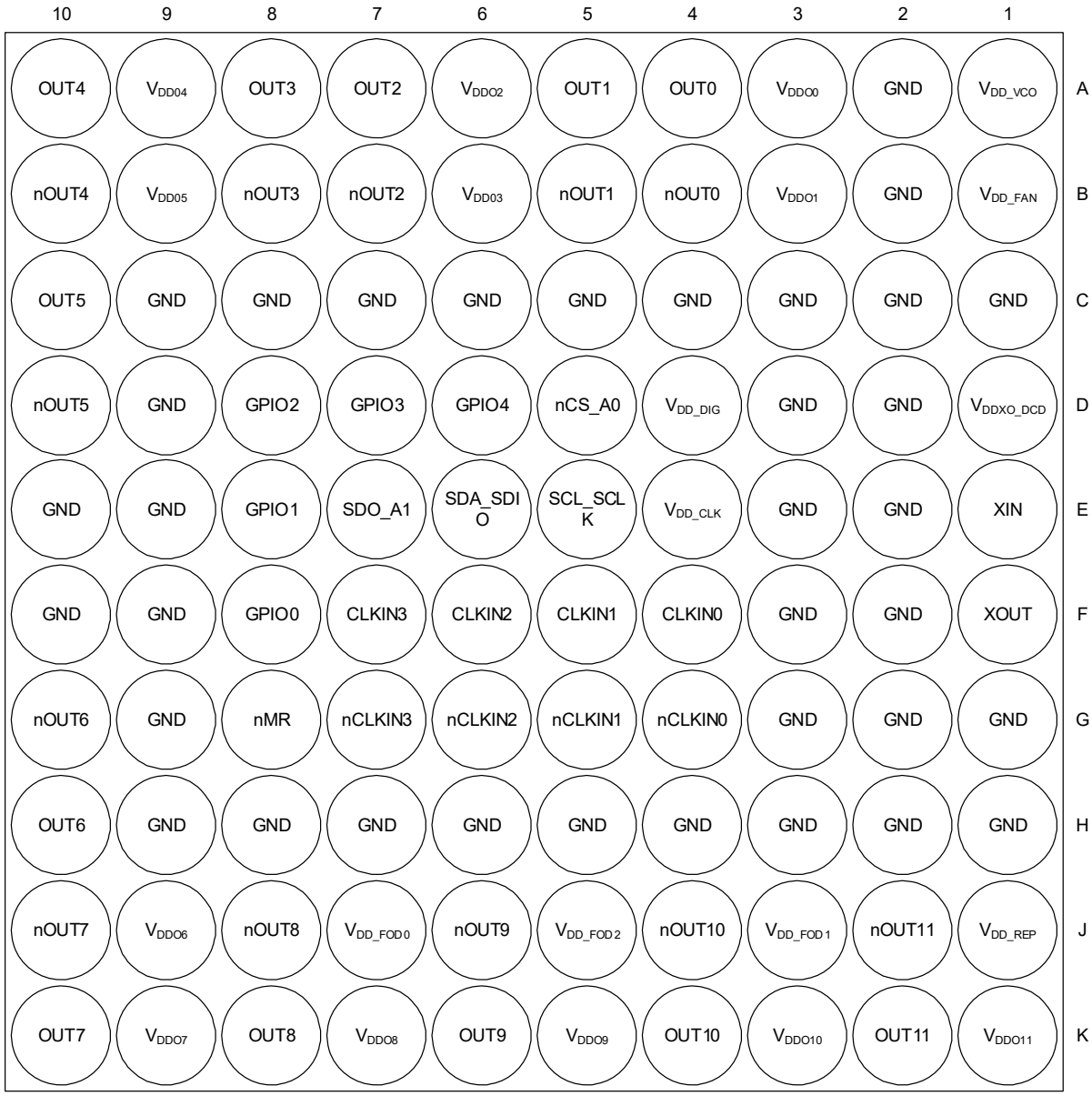


Figure 4. Pin Assignments – Bottom View

1.2 Pin Descriptions

Table 1. Pin Descriptions

Pin Number	Pin Name	Type		Description
A1	V_{DD_VCO}	Power	-	Power supply for the VCO. 1.8V is supported.
A2	GND	Power	-	Ground reference rail.
A3	V_{DDO0}	Power	-	Power supply for OUT0/nOUT0 and IOD0. 1.8V is supported. This pin can be tied to ground to minimize power consumption if the corresponding output is unused. This pin must not be allowed to float.
A4	OUT0	O	-	Clock output, differential pair. LVDS, HCSL, or CML. OUTx indicates the positive pin of a differential pair.

Table 1. Pin Descriptions (Cont.)

Pin Number	Pin Name	Type		Description
A5	OUT1	O	-	Clock output, differential pair. LVDS, HCSL, or CML. OUTx indicates the positive pin of a differential pair.
A6	V_{DDO2}	Power	-	Power supply for OUT2/nOUT2 and IOD2. 1.8V is supported. This pin can be tied to ground to minimize power consumption if the corresponding output is unused. This pin must not be allowed to float.
A7	OUT2	O	-	Clock output, differential pair. LVDS, HCSL, or CML. OUTx indicates the positive pin of a differential pair.
A8	OUT3	O	-	Clock output, differential pair. LVDS, HCSL, or CML. OUTx indicates the positive pin of a differential pair.
A9	V_{DDO4}	Power	-	Power supply for OUT4/nOUT4 and IOD4. 1.8V is supported. This pin can be tied to ground to minimize power consumption if the corresponding output is unused. This pin must not be allowed to float.
A10	OUT4	O	-	Clock output, differential pair. LVDS, HCSL, or CML. OUTx indicates the positive pin of a differential pair.
B1	V_{DD_FAN}	Power	-	Power supply for internal buffering to FODs and IODs. 1.8V is supported.
B2	GND	Power	-	Ground reference rail.
B3	V_{DDO1}	Power	-	Power supply for OUT1/nOUT1 and IOD1. 1.8V is supported. This pin can be tied to ground to minimize power consumption if the corresponding output is unused. This pin must not be allowed to float.
B4	nOUT0	O	-	Clock output, differential pair. LVDS, HCSL, or CML. nOUTx indicates the negative pin of a differential pair.
B5	nOUT1	O	-	Clock output, differential pair. LVDS, HCSL, or CML. nOUTx indicates the negative pin of a differential pair.
B6	V_{DDO3}	Power	-	Power supply for OUT3/nOUT3 and IOD3. 1.8V is supported. This pin can be tied to ground to minimize power consumption if the corresponding output is unused. This pin must not be allowed to float.
B7	nOUT2	O	-	Clock output, differential pair. LVDS, HCSL, or CML. nOUTx indicates the negative pin of a differential pair.
B8	nOUT3	O	-	Clock output, differential pair. LVDS, HCSL, or CML. nOUTx indicates the negative pin of a differential pair.
B9	V_{DDO5}	Power	-	Power supply for OUT5/nOUT5 and IOD5. 1.8V is supported. This pin can be tied to ground to minimize power consumption if the corresponding output is unused. This pin must not be allowed to float.
B10	nOUT4	O	-	Clock output, differential pair. LVDS, HCSL, or CML. nOUTx indicates the negative pin of a differential pair.
C1	GND	Power	-	Ground reference rail.
C2	GND	Power	-	Ground reference rail.
C3	GND	Power	-	Ground reference rail.
C4	GND	Power	-	Ground reference rail.
C5	GND	Power	-	Ground reference rail.
C6	GND	Power	-	Ground reference rail.
C7	GND	Power	-	Ground reference rail.
C8	GND	Power	-	Ground reference rail.
C9	GND	Power	-	Ground reference rail.
C10	OUT5	O	-	Clock output, differential pair. LVDS, HCSL, or CML. OUTx indicates the positive pin of a differential pair.
D1	V_{DDXO_DCD}	Power	-	Power supply for XIN, XOUT and the DCD block. 1.8V is supported.
D2	GND	Power	-	Ground reference rail.

Table 1. Pin Descriptions (Cont.)

Pin Number	Pin Name	Type		Description
D3	GND	Power	-	Ground reference rail.
D4	V_{DD_DIG}	Power	-	Power supply for digital core, serial port, digital in FODs, and digital in the APLL. 1.8V, 2.5V, and 3.3V are supported.
D5	nCS_A0	I	Pull-up	I^2C mode: address bit 0. SPI mode: active low chip select. GPIO DC electrical characteristics apply to this pin.
D6	GPIO4	I/O	Pull-up	General purpose input/output. The VDD_FOD0 pin must be powered to ensure proper operation.
D7	GPIO3	I/O	Pull-up	General purpose input/output. The VDD_FOD0 pin must be powered to ensure proper operation.
D8	GPIO2	I/O	Pull-up	General purpose input/output. The VDD_FOD0 pin must be powered to ensure proper operation.
D9	GND	Power	-	Ground reference rail.
D10	nOUT5	O	-	Clock output, differential pair. LVDS, HCSL, or CML. nOUTx indicates the negative pin of a differential pair.
E1	XIN	I	-	Crystal oscillator/xCXO input.
E2	GND	Power	-	Ground reference rail.
E3	GND	Power	-	Ground reference rail.
E4	V_{DD_CLK}	Power	-	Power supply for CLKINx buffers, dividers, muxes, and the TDC. 1.8V is supported.
E5	SCL_SCLK	I/O	Pull-up	I^2C mode: I^2C interface bi-directional clock. SPI mode: serial clock. GPIO DC electrical characteristics apply to this pin.
E6	SDA_SDIO	I/O	Pull-up	I^2C mode: I^2C interface bi-directional serial data. SPI 3-wire mode: bi-directional serial data. SPI 4-wire mode: input serial data. GPIO DC electrical characteristics apply to this pin.
E7	SDO_A1	I/O	Pull-up	I^2C mode: address bit 1. SPI 3-wire mode: unused. SPI 4-wire mode: output serial data. GPIO DC electrical characteristics apply to this pin.
E8	GPIO1	I/O	Pull-up	General purpose input/output. The VDD_FOD0 pin must be powered to ensure proper operation.
E9	GND	Power	-	Ground reference rail.
E10	GND	Power	-	Ground reference rail.
F1	XOUT	O	-	Crystal oscillator output.
F2	GND	Power	-	Ground reference rail.
F3	GND	Power	-	Ground reference rail.
F4	CLKIN0	I	Pull-down	Clock reference input, differential pair/single ended. CLKINx indicates the positive pin of a differential pair.
F5	CLKIN1	I	Pull-down	Clock reference input, differential pair/single ended. CLKINx indicates the positive pin of a differential pair.
F6	CLKIN2	I	Pull-down	Clock reference input, differential pair/single ended. CLKINx indicates the positive pin of a differential pair.
F7	CLKIN3	I	Pull-down	Clock reference input, differential pair/single ended. CLKINx indicates the positive pin of a differential pair.
F8	GPIO0	I/O	Pull-up	General purpose input/output. The VDD_FOD0 pin must be powered to ensure proper operation.
F9	GND	Power	-	Ground reference rail.
F10	GND	Power	-	Ground reference rail.
G1	GND	Power	-	Ground reference rail.
G2	GND	Power	-	Ground reference rail.

Table 1. Pin Descriptions (Cont.)

Pin Number	Pin Name	Type		Description
G3	GND	Power	-	Ground reference rail.
G4	nCLKIN0	I	Pull-up	Clock reference input, differential pair/single-ended. nCLKINx indicates the negative pin of a differential pair.
G5	nCLKIN1	I	Pull-up	Clock reference input, differential pair/single-ended. nCLKINx indicates the negative pin of a differential pair.
G6	nCLKIN2	I	Pull-up	Clock reference input, differential pair/single-ended. nCLKINx indicates the negative pin of a differential pair.
G7	nCLKIN3	I	Pull-up	Clock reference input, differential pair/single-ended. nCLKINx indicates the negative pin of a differential pair.
G8	nMR	I	Pull-up	Active low controller (master) reset. The V_{DD_FOD0} pin must be powered to ensure proper operation. GPIO DC electrical characteristics apply to this pin.
G9	GND	Power	-	Ground reference rail.
G10	nOUT6	O	-	Clock output, differential pair. LVDS, HCSL, or CML. nOUTx indicates the negative pin of a differential pair.
H1	GND	Power	-	Ground reference rail.
H2	GND	Power	-	Ground reference rail.
H3	GND	Power	-	Ground reference rail.
H4	GND	Power	-	Ground reference rail.
H5	GND	Power	-	Ground reference rail.
H6	GND	Power	-	Ground reference rail.
H7	GND	Power	-	Ground reference rail.
H8	GND	Power	-	Ground reference rail.
H9	GND	Power	-	Ground reference rail.
H10	OUT6	O	-	Clock output, differential pair. LVDS, HCSL, or CML. OUTx indicates the positive pin of a differential pair.
J1	V_{DD_REP}	Power	-	Power supply for all FOD digital. 1.8V is supported.
J2	nOUT11	O	-	Clock output, differential pair/single ended. LVDS, HCSL or LVCMOS. nOUTx indicates the negative pin of a differential pair.
J3	V_{DD_FOD1}	Power	-	Power supply for FOD1. 1.8V is supported.
J4	nOUT10	O	-	Clock output, differential pair/single ended. LVDS, HCSL or LVCMOS. nOUTx indicates the negative pin of a differential pair.
J5	V_{DD_FOD2}	Power	-	Power supply for FOD2. 1.8V is supported.
J6	nOUT9	O	-	Clock output, differential pair/single ended. LVDS, HCSL or LVCMOS. nOUTx indicates the negative pin of a differential pair.
J7	V_{DD_FOD0}	Power	-	Power supply for FOD0, nMR, and GPIO[4:0]. 1.8V is supported.
J8	nOUT8	O	-	Clock output, differential pair/single ended. LVDS, HCSL or LVCMOS. nOUTx indicates the negative pin of a differential pair.
J9	V_{DDO6}	Power	-	Power supply for OUT6/nOUT6 and IOD6. 1.8V is supported. This pin can be tied to ground to minimize power consumption if the corresponding output is unused. This pin must not be allowed to float.
J10	nOUT7	O	-	Clock output, differential pair. LVDS, HCSL, or CML. nOUTx indicates the negative pin of a differential pair.
K1	V_{DDO11}	Power	-	Power supply for OUT11/nOUT11 and IOD11. 1.8V is supported. This pin can be tied to ground to minimize power consumption if the corresponding output is unused. This pin must not be allowed to float.
K2	OUT11	O	-	Clock output, differential pair/single ended. LVDS, HCSL or LVCMOS. OUTx indicates the positive pin of a differential pair.

Table 1. Pin Descriptions (Cont.)

Pin Number	Pin Name	Type		Description
K3	V_{DDO10}	Power	-	Power supply for OUT10/nOUT10 and IOD10. 1.8V is supported. This pin can be tied to ground to minimize power consumption if the corresponding output is unused. This pin must not be allowed to float.
K4	OUT10	O	-	Clock output, differential pair/single ended. LVDS, HCSL or LVCMOS. OUTx indicates the positive pin of a differential pair.
K5	V_{DDO9}	Power	-	Power supply for OUT9/nOUT9 and IOD9. 1.8V is supported. This pin can be tied to ground to minimize power consumption if the corresponding output is unused. This pin must not be allowed to float.
K6	OUT9	O	-	Clock output, differential pair/single ended. LVDS, HCSL or LVCMOS. OUTx indicates the positive pin of a differential pair.
K7	V_{DDO8}	Power	-	Power supply for OUT8/nOUT8 and IOD8. 1.8V is supported. This pin can be tied to ground to minimize power consumption if the corresponding output is unused. This pin must not be allowed to float.
K8	OUT8	O	-	Clock output, differential pair/single ended. LVDS, HCSL or LVCMOS. OUTx indicates the positive pin of a differential pair.
K9	V_{DDO7}	Power	-	Power supply for OUT7/nOUT7 and IOD7. 1.8V is supported. This pin can be tied to ground to minimize power consumption if the corresponding output is unused. This pin must not be allowed to float.
K10	OUT7	O	-	Clock output, differential pair. LVDS, HCSL, or CML. OUTx indicates the positive pin of a differential pair.

1.3 Input Characteristics

Table 2. Input Characteristics

Symbol	Parameter		Condition	Minimum	Typical	Maximum	Unit
C_{IN}	Input capacitance	CLKIN/nCLKIN, nMR, nCS_A0, SDO_A1, GPIOn, SCL_SCLK, SDA_SDIO	-	-	4	-	pF
R_{PULLUP}	Input pull-up resistor	nMR, nCLKIN, nCS_A0, SDO_A1, GPIOn	-	-	53	-	kΩ
$R_{PULLDOWN}$	Input pull-down resistor	CLKIN, nCS_A0, SDO_A1, GPIOn	-	-	53	-	kΩ

2. Specifications

2.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Condition	Minimum	Maximum	Unit
V_{DD18}	Supply Voltage with Respect to Ground	V_{DD_CLK}, V_{DDXO_DCD}, V_{DD_VCO}, V_{DD_FAN}, V_{DD_REP}, V_{DD_FOD0}, V_{DD_FOD1}, V_{DD_FOD2}, V_{DDOx}	-0.5	1.89	V
V_{DD33}	Supply Voltage with Respect to Ground	V_{DD_DIG}	-0.5	3.63	V
V_{IN}	Input Voltage	XIN [1]	-0.5	1.32	V
		GPIOx used as inputs, nMR [2]	-0.5	V_{DDx} + 0.3	
		CLKINx	-0.5	V_{DD_CLK} + 0.3	
		nCS_A0, SDO_A1, SCL_SCLK, SDA_SDIO	-0.5	V_{DD_DIG} + 0.3	
I_{IN}	Input Current	GPIOx used as inputs, nMR	-	±25	mA
		CLKINx	-	±50	
		nCS_A0, SDO_A1, SCL_SCLK, SDA_SDIO	-	±25	
I_{OUT}	Output Current - Continuous	OUTx, nOUTx	-	30	mA
		LOCK, SDO_A1, SCL_SCLK, SDA_SDIO	-	25	
		GPIOx used as outputs	-	25	
	Output Current - Surge	OUTx, nOUTx	-	30	mA
		LOCK, SDO_A1, SCL_SCLK, SDA_SDIO	-	25	
		GPIOx used as outputs	-	25	
T_{JMAX}	Maximum Junction Temperature	-	-	150	°C
T_S	Storage Temperature	Storage Temperature	-65	150	°C
-	Human Body Model (Tested per JESD22-A114 (JS-001) Classification)	-	-	2000	V
-	Charged Device Model (Tested per JESD22-C101 Classification)	-	-	500	V

1. This limit only applies when XIN is overdriven by an external oscillator. No limit is implied when connected directly to a crystal.
2. V_{DDx} refers to the supply powering the GPIO. For V_{DD} pin mapping, see GPIO V_{DD} Pin Assignments.

2.2 Recommended Operating Conditions

Table 4. Recommended Operating Conditions [1][2]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
T_J	Maximum Junction Temperature	-	-	-	125	°C
T_A	Ambient Operating Temperature	-	-40	-	85	°C
V_{DDx}	Supply Voltage with Respect to Ground	V_{DDx} pins with 1.8V supply	1.71	1.8	1.89	V
		V_{DDx} pins with 2.5V supply	2.375	2.5	2.625	V
		V_{DDx} pins with 3.3V supply	3.135	3.3	3.465	V
t_{PU}	Power up time for all V_{DD} to reach minimum specified voltage	Power ramps must be monotonic	-	-	20	ms

1. All electrical characteristics are specified over Recommended Operating Conditions unless noted otherwise.
2. All conditions in this table must be met to guarantee device functionality and performance.

2.3 Thermal Specifications

Table 5. Thermal Specifications

Package	Symbol	Condition	Typical Value	Unit
BJG100	Θ_{JC}	Junction to case	12.5	°C/W
	Θ_{JB}	Junction to base	7.7	
	Θ_{JA0}	Junction to air, still air	23	
	Θ_{JA1}	Junction to air, 1 m/s air flow	21	
	Θ_{JA3}	Junction to air, 2 m/s air flow	19	
	Θ_{JA5}	Junction to air, 3 m/s air flow	18	

2.4 APLL Phase Jitter

Table 6. APLL Phase Jitter [1][2][3][4]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
$t_{JIT}(\Phi)$	Random Phase Jitter (12kHz to 20MHz), OUT[11:0] differential, APLL steered by DPLL0, BW = 25Hz,[5] CLKIN = 25MHz, XIN = 68MHz, VCO = 9.8304GHz	245.76MHz	-	69	85	fs RMS
		491.52MHz	-	48	56	
$t_{JIT}(\Phi)$	Random Phase Jitter (12kHz to 20MHz), OUT[11:0] differential, APLL steered by DPLL0, BW = 25Hz,[5] CLKIN = 25MHz, XIN = 68.8MHz, VCO = 9.375GHz	156.25MHz	-	62	73	fs RMS
		312.5MHz	-	58	67	
$t_{JIT}(\Phi)$	Random Phase Jitter (12kHz to 20MHz) with 4MHz high-pass-filter, OUT[11:0] differential, APLL steered by DPLL0, BW = 25Hz,[5] CLKIN = 25MHz, XIN = 54MHz, VCO = 9.375GHz	312.5MHz	-	25	-	fs RMS
$t_{JIT}(\Phi)$	Random Phase Jitter (12kHz to 20MHz) with 4MHz high-pass-filter, OUT[11:0] differential, APLL configured as a synthesizer, XIN = 54MHz, VCO = 9.375GHz	312.5MHz	-	25	-	fs RMS

1. The device will meet specifications after thermal equilibrium has been reached.

2. Characterized using a Rohde and Schwarz SMA100 overdriving the crystal interface.
3. Measured after the APLL has locked and settled.
4. All outputs enabled and generating clocks with the same frequency sourced from the APLL via integer output dividers.
5. Measured after the DPLL has locked and settled using a jitter free and wander-free reference.

2.5 FOD Phase Jitter

Table 7. FOD Phase Jitter [1][2][3][4]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
$t_{JIT}(\Phi)$	Random Phase Jitter (12kHz to 20MHz), OUT[11:6] differential, APLL steered by DPLL0, BW = 25Hz,[5] CLKIN = 25MHz, XIN = 68MHz, FOD configured as a synthesizer/DCO, VCO = 9.763GHz or VCO = 10.224GHz[6]	155.52MHz	-	107	127	fs RMS
		161,132,812.5MHz	-	119	140	
		156.25MHz	-	104	127	
		312.5MHz	-	88	112	
		625MHz	-	88	101	

1. The device will meet specifications after thermal equilibrium has been reached.
2. Characterized using a Rohde and Schwarz SMA100 overdriving the crystal interface.
3. Measured after the APLL has locked and settled.
4. All OUT[11:6] enabled and generating the same frequency sourced from the same FOD, other OUT[x] disabled.
5. Measured after the DPLL has locked and settled using a jitter free and wander-free reference.
6. See Table 12 for VCO frequencies supported by each part number.

2.6 TOD and Synthesis Phase Jitter

Table 8. TOD and Synthesis Phase Jitter [1][2][3][4][5]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
$t_{JIT}(\Phi)$	Random Phase Jitter (12kHz to 20MHz), OUT[11:8] differential, FOD0 configured as a synthesizer/DCO, FOD0 = 500MHz	125MHz	-	1.2	2.1	ps RMS
		250MHz	-	0.8	1.3	

1. The device will meet specifications after thermal equilibrium has been reached.
2. Characterized using a Rohde and Schwarz SMA100 overdriving the XTAL interface.
3. Measured after the APLL has locked and settled.
4. All OUT[11:8] enabled and generating the same frequency, other OUT[x] disabled.
5. Measured after the DPLL has locked and settled using a jitter free and wander-free reference.

2.7 APLL Phase Noise

Table 9. APLL Phase Noise [1][2][3][4]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
$\Phi_{SSB}(10)$	Single Sideband Phase Noise, OUT[7:0] differential, Carrier 245.76MHz; APLL steered by DPLL0, BW = 25Hz,[5] CLKIN = 25MHz from Rb timebase, XIN = 73MHz, VCO = 9.8304GHz	10Hz Offset	-	-72	-	dBc/Hz
$\Phi_{SSB}(100)$		100Hz Offset	-	-104	-	
$\Phi_{SSB}(1k)$		1kHz Offset	-	-123	-	
$\Phi_{SSB}(10k)$		10kHz Offset	-	-138	-	
$\Phi_{SSB}(100k)$		100kHz Offset	-	-145	-	
$\Phi_{SSB}(800k)$		800kHz Offset	-	-150	-	
$\Phi_{SSB}(1M)$		1MHz Offset	-	-148	-	
$\Phi_{SSB}(1.72M)$		1.72MHz Offset	-	-155	-	
$\Phi_{SSB}(10M)$		10MHz Offset	-	-164	-	
$\Phi_{SSB}(30M)$		30MHz Offset	-	-165	-	

Table 9. APLL Phase Noise [1][2][3][4] (Cont.)

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
$\Phi_{SSB}(10)$	Single Sideband Phase Noise, OUT[7:0] differential, Carrier 491.52MHz; APLL steered by DPLL0, BW = 25Hz,[5] CLKIN = 25MHz from Rb timebase, XIN = 73MHz, VCO = 9.8304GHz	10Hz Offset	-	-69	-	dBc/Hz
$\Phi_{SSB}(100)$		100Hz Offset	-	-98	-	
$\Phi_{SSB}(1k)$		1kHz Offset	-	-117	-	
$\Phi_{SSB}(10k)$		10kHz Offset	-	-132	-	
$\Phi_{SSB}(100k)$		100kHz Offset	-	-139	-	
$\Phi_{SSB}(800k)$		800kHz Offset	-	-144	-	
$\Phi_{SSB}(1M)$		1MHz Offset	-	-142	-	
$\Phi_{SSB}(1.72M)$		1.72MHz Offset	-	-150	-	
$\Phi_{SSB}(10M)$		10MHz Offset	-	-161	-	
$\Phi_{SSB}(30M)$		30MHz Offset	-	-161	-	

1. The device will meet specifications after thermal equilibrium has been reached.
2. Characterized using a Rohde and Schwarz SMA100 overdriving the crystal interface.
3. Measured after the DPLL and APLL have locked and settled.
4. All OUT[7:0] enabled and generating the same frequency.
5. Measured after the DPLL has locked and settled using a jitter free and wander-free reference.

2.8 Peak APLL Spurious Power

Table 10. Peak APLL Spurious Power [1][2][3][4][5][6]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
Φ_{SPUR}	Peak Spurious Power 100Hz to 100MHz, OUT[7:0] differential, APLL steered by DPLL0, DPLL BW = 25Hz, CLKIN = 25MHz, XIN = 73MHz, VCO = 9.8304GHz	Carrier 245.76MHz	-	-92	-	dBc
		Carrier 491.52MHz;	-	-86	-	

1. The device will meet specifications after thermal equilibrium has been reached.
2. Characterized using a Rohde and Schwarz SMA100 overdriving the crystal interface.
3. Measured after the APLL has locked and settled.
4. Measured after the DPLL has locked and settled using a jitter free and wander-free reference.
5. All OUT[7:0] enabled and generating the same frequency.
6. All FODs and OUT[8:11] disabled.

2.9 Power Supply Noise Rejection

Table 11. Power Supply Noise Rejection [1]

Symbol	Parameter	Condition [2][3][4]	Minimum	Typical	Maximum	Unit
PSNR	Power Supply Rejection Ratio V_{DDx} = 1.8V	f_{NOISE} = 10kHz	-	-81	-	dBc
		f_{NOISE} = 25kHz	-	-83	-	
		f_{NOISE} = 50kHz	-	-80	-	
		f_{NOISE} = 100kHz	-	-80	-	
		f_{NOISE} = 500kHz	-	-62	-	
		f_{NOISE} = 1MHz	-	-64	-	

1. The device will meet specifications after thermal equilibrium has been reached.
2. 100mV peak-to-peak sine wave applied to any VDDO, excluding VDDO of the output being measured and excluding VDD_VCO.
3. Relative to 156.25MHz carrier frequency.
4. Measured on any differential output.

2.10 Crystal Oscillator Input and APLL AC/DC Electrical Characteristics

Table 12. Crystal Oscillator Input and Analog PLL AC/DC Characteristics

Symbol	Parameter	Condition		Minimum	Typical	Maximum	Unit
-	Mode of oscillation	-			Fundamental		-
f_{IN}	Input Frequency	Using a crystal		25	-	80	MHz
		Over-driving XIN input		25	-	100	
V_{BIAS}	Bias point for XIN	Over-driving XIN input		-	0.6	-	V
V_{IVS}	Input voltage swing for XIN	Over-driving XIN input		-	-	1.2	V
C_T	Internal crystal oscillator tuning capacitance[1]	xo_fixedcap_on = 0x0	xobuf_digicap_x1 = 0x0 xobuf_digcap_x2 = 0x0	6.2	-	-	pF
			xobuf_digicap_x1 = 0xF xobuf_digcap_x2 = 0xF	-	-	10.2	
		xo_fixedcap_on = 0x1	xobuf_digicap_x1 = 0x0 xobuf_digcap_x2 = 0x0	9.2	-	-	
			xobuf_digicap_x1 = 0xF xobuf_digcap_x2 = 0xF	-	-	13.2	
f_{VCO}	Analog PLL VCO Operating Frequency	RC38312x1xx, RC38112x1xx		9.8	-	10.35	GHz
		RC38312x2xx, RC38112x2xx		9.3	-	9.85	GHz
F_{TOL}	Frequency Tolerance [2][3][4][5]	-40°C to 85°C		-450	-	450	PPM

1. For applications where the XIN input is overdriven, xo_buf_digicap_x1, xo_buf_digicap_x2, and xo_fixedcap_on should all be set to 0x0 for best phase noise performance.
2. F_{TOL} refers to the frequency accuracy of the APLL frequency reference, either a crystal connected between XIN and XOUT, or an oscillator connected to XIN and overdriving the crystal interface. The APLL can reliably lock to a reference that meets the F_{TOL} limits.
3. Inclusive of initial tolerance at 25°C, temperature stability, and aging.
4. The APLL frequency steering range ($\pm F_{STEER}$) available for a DPLL or DCO to digitally steer the APLL is determined by the following expression: $F_{STEER} = |F_{TOL}| - |F_{ACC}|$; where F_{ACC} is the frequency accuracy of the APLL frequency reference. For example, if the frequency accuracy of the APLL frequency reference is ±100PPM. then the APLL frequency steering range will be ±350PPM.
5. The frequency accuracy of the APLL frequency reference should be chosen to meet the free-running frequency requirements of the application, and to allow sufficient frequency steering range for a DPLL or DCO to lock the APLL to its reference and to track reference noise. For more information, see APLL Frequency Reference.

2.11 Recommended Crystal Characteristics

Table 13. Recommended Crystal Characteristics

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
ESR	Equivalent Series Resistance	8pF ≤ C_L ≤ 10pF	-	-	50	Ω
C_O	Shunt Capacitance	-	-	-	4	pF
C_L	Load Capacitance	-	-	-	10	pF
Drive	Drive Level [1]	C_L = 8pF	-	160	-	µW
		C_L = 10pF	-	225	-	
F_{TOL}	Frequency Tolerance	-	See F_{TOL} in Table 12 and APLL Frequency Reference			-

1. Refers to power in the crystal (equivalent series resistance).

2.12 Clock Input (CLKIN/nCLKIN) AC/DC Characteristics

Table 14. Clock Input (CLKIN/nCLKIN) AC/DC Characteristics

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{IPP}	Differential input peak-to-peak voltage [1]	-	0.15	-	1.20	V
V_{CMR}	Differential input common mode voltage [2]	PMOS buffer (HCSL) input	$V_{I(PP)}$ / 2	0.35	V_{DD_CLK} - 1.2	V
		NMOS buffer (LVDS) input	0.7	-	V_{DD_CLK} - $V_{I(PP)}$	
F_{IN}	Input frequency	Differential input	-	-	1000	MHz
		Single-ended input	-	-	250	
F_{PD}	DPLL phase detector frequency [3]	-	0.001	-	33	MHz
I_{IH}	Differential input high current, CLKIN	V_{IN} = $V_{DD_CLK\ (max)}$	-	-	150	µA
	Differential input high current, nCLKIN		-	-	5	
I_{IL}	Differential input low current, CLKIN	V_{IN} = 0V	-5	-	-	µA
	Differential input low current, nCLKIN		-150	-	-	
V_{IH}	Input high voltage	V_{DD_CLK} = $V_{DD_CLK\ (max)}$	0.65 × V_{DD_CLK}	-	V_{DD_CLK} + 0.3	V
V_{IL}	Input low voltage	V_{DD_CLK} = $V_{DD_CLK\ (max)}$	-0.3	-	0.35 x V_{DD_CLK}	V
I_{IH}	Input high current	V_{IN} = $V_{DD_CLK\ (max)}$	-	-	50	µA
I_{IL}	Input low current	V_{IN} = 0V	-50	-	-	µA

1. Single-ended value.
2. Common mode is defined as the cross-point.
3. Internal input dividers may be used to reduce the CLKIN/nCLKIN frequency to be within the valid range.

2.13 Output Frequencies and Start-Up Time

Table 15. Output Frequencies and Start-Up Time

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
f_{OUT}	Output Frequency	OUT[7:0]: CML	DC	-	2500	MHz
		OUT[11:0]: LVDS, HCSL	DC	-	1000	
		OUT[11:8]: LVCMOS	DC	-	250	
Δf_{OUT}	Output frequency tuning resolution	Fractional Output Divider	-	-	0.1	PPT
$t_{Start-up}$	Start-up time [1][2]	Synthesizer mode	-	28	31	ms

1. Measured from when all power supplies have reached > 90% of nominal voltage to the first stable clock edge on the output. A stable clock is defined as one generated from a locked PLL (as appropriate for the configuration listed) with no further perturbations in frequency expected. Includes time needed to load a configuration from internal OTP.
2. Start-up time will depend on the actual configuration used. For more information, please contact Renesas Technical Support.

2.14 Phase and Frequency Uncertainty

Table 16. Phase and Frequency Uncertainty [1][2]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
Δt_{HS}	Output phase change using hitless reference switching	-	-	-	210	ps
Δf_{HO}	Initial frequency offset entering holdover	Using holdover filter with 1mHz bandwidth and allowing settling time of 1 hour	-	-	0.2	PPB
Δt_{HO}	Initial phase shift entering holdover	Using LOS monitor to disqualify	-	-	17	ps

1. The device will meet specifications after thermal equilibrium has been reached.
2. Measured after the DPLL has locked and settled using a jitter free and wander-free reference.

2.15 Output-to-Output Skew and Input-to-Output Delay

Table 17. Output-to-Output Skew and Input-to-Output Delay [1][2]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
t_{SK}	Output-to-output skew differential outputs [3][4]	Any two outputs from the same APLL or FOD source	-	25	50	ps
	Output-to-output skew LVCMOS outputs [3][4]	Any two outputs from the same APLL or FOD source	-	43	86	
t_{SK_SR}	Output-to-output skew between SYSREF and Device Clock incident edge	Differential outputs. Zero phase compensation.	-	24	50	ps
Δt_{SK}	Output-to-output skew temperature variation [4]	Single device, at a fixed voltage, over temperature	-	0.02	0.10	ps/°C
	Output-to-output skew variation [3]	Single device, over process, temperature and voltage	-	0.08	0.80	
t_{PD}	Input-to-output delay differential inputs and differential outputs [5][6]	DC-coupled input, any CLKINx to any OUTx via any DPLLx	0.67	1.13	1.65	ns
		AC-coupled input, any CLKINx to any OUTx via any DPLLx	0.75	1.24	1.69	
Δt_{PD}	Input-to-output delay variation [5][6]	DC-coupled input, fixed voltage, over temperature	-	0.5	0.8	ps/°C
		AC-coupled input, fixed voltage, over temperature	-	1.0	1.4	

1. The device will meet specifications after thermal equilibrium has been reached.
2. Measured across the full operating temperature range.
3. Defined as the time between the rising edges of two outputs of the same frequency, configuration, loading, and supply voltage.
4. This parameter is defined in accordance with JEDEC Standard 65.
5. Input-to-output delay is defined as the time between the rising edge of a reference clock at CLKINx and the associated rising edge of an output clock at OUTx that is locked to the reference by the DPLL. The reference clock and the output clock must have the same frequency and the reference input dividers must be bypassed.
6. Measured after the DPLL has locked and settled using a jitter free and wander-free reference to the DPLL.

2.16 LVCMOS Output AC/DC Characteristics

Table 18. LVCMOS Output AC/DC Characteristics [1]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{OH}	Output high voltage [2]	I_{OH} = -2mA	V_{DDO} - 0.45	-	-	V
V_{OL}	Output low voltage [2]	I_{OL} = 2mA	-	-	0.45	V
V_{OH}	Output high voltage [2]	I_{OH} = -100µA	V_{DDO} - 0.2	-	-	V
V_{OL}	Output low voltage [2]	I_{OL} = 100µA	-	-	0.2	V
I_{OZ}	Output leakage current	Outputs tri-stated	-5	-	5	µA
Z_{OUTDC}	DC output impedance	At 25°C, out_cmos_same_phase = 0	-	24	-	Ω
		At 25°C, out_cmos_same_phase = 1	-	34	-	
t_R/t_F	Rise/Fall time, 20% to 80%	-	140	214	295	ps
t_{DC}	Output duty cycle	From APLL, even IOD divide	47	50	55	%
		From APLL, odd IOD divide ≥ 3	49	52	55	
		From FOD, even IOD divide	47	50	51	
		From FOD, odd IOD divide ≥ 3	50	50	51	
		From FOD with IOD divide = 1	46	49	52	

1. Measured with outputs terminated with 50Ω to $V_{DDO}/2$.
2. These values are compliant with JESD8-7A.

2.17 LVDS Output AC/DC Characteristics

Table 19. LVDS Output AC/DC Characteristics [1]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{OD}	Output voltage swing [2][3]	out_boost = 0x0	266	373	440	mV
		out_boost = 0x1	336	448	521	
		out_boost = 0x2				
		out_boost = 0x3	392	501	586	
V_{OS}	Offset voltage [3]	out_boost = 0x0	1188	1227	1306	mV
		out_boost = 0x1	1084	1163	1241	
		out_boost = 0x2				
		out_boost = 0x3	1005	1114	1185	
ΔV_{OS}	Change in VOS between complimentary output states [3]	out_boost = 0x0	-	3	33	mV
		out_boost = 0x1	-	4	39	
		out_boost = 0x2				
		out_boost = 0x3	-	3	46	
t_R/t_F	Rise/Fall time, 20% to 80%	out_boost = 0x0	65	179	415	ps
		out_boost = 0x1	73	177	404	
		out_boost = 0x2				
		out_boost = 0x3	76	176	385	
t_{DC}	Output duty cycle	From APLL, even IOD divide	46	50	52	%
		From APLL, odd IOD divide ≥ 3	48	50	50	
		From APLL with IOD divide = 1	43	48	51	
		From FOD, even IOD divide	49	50	51	
		From FOD, odd IOD divide ≥ 3	50	50	51	
		From FOD with IOD divide = 1	46	49	52	

1. Terminated with 100Ω across OUTx and nOUTx, out_pull_down = 0x0, out_pull_up = 0x0.
2. Single-ended measurement.
3. Tested at 10MHz.

2.18 HCSL Output AC/DC Characteristics

Table 20. HCSL Output AC/DC Characteristics [1]

Symbol	Parameter	Condition		Minimum	Typical	Maximum	Unit
V_{OVS}	Output voltage swing [2][3][4]	out_boost = 0x0	-	673	801	960	mV
		out_boost = 0x1	-	745	930	1125	
		out_boost = 0x2	-				
		out_boost = 0x3	-	850	995	1211	
V_{CM}	Common mode [3]	out_boost = Any	-	387	414	441	mV
t_R/t_F	Rise/Fall time, 20% to 80%	out_boost = Any	From APLL, FOD[0]	100	172	268	ps
			From FOD[2:1]	140	235	365	
t_{DC}	Output duty cycle	From APLL, even IOD divide	-	47	49	51	%
		From APLL, odd IOD divide ≥ 3	-	48	49	51	
		From APLL with IOD divide = 1	-	44	47	51	
		From FOD, even IOD divide	-	49	50	51	
		From FOD, odd IOD divide ≥ 3	-	49	50	51	
		From FOD with IOD divide = 1	-	47	50	52	

1. Terminated with 50Ω to ground on each of OUTx and nOUTx, out_pull_down = 0x0, out_pull_up = 0x0.
2. Single-ended measurement.
3. Output frequency = 10MHz.
4. At 312.5MHz, when outboost = 0x3: V_{OVS} Minimum = 0.8V and Maximum = 1.2V.

2.19 CML Output AC/DC Characteristics

Table 21. CML Output AC/DC Characteristics [1]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{OH}	Output high voltage	-	-	1800	-	mV
V_{OVS}	Output voltage swing [2][3]	out_boost = 0x0	676	766	831	mV
		out_boost = 0x1	790	901	993	
		out_boost = 0x2				
		out_boost = 0x3	860	983	1093	
t_R/t_F	Rise/Fall time, 20% to 80%	out_boost = Any	171	249	320	ps
t_{DC}	Output duty cycle	From APLL, even IOD divide	48	50	51	%
		From APLL, odd IOD divide ≥ 3	49	50	51	
		From APLL with IOD divide = 1	44	47	50	
		From FOD, even IOD divide	46	49	52	
		From FOD, odd IOD divide ≥ 3	49	50	51	
		From FOD with IOD divide = 1	47	49	51	

1. Terminated with 50Ω to V_{DDOx} on each of OUTx and nOUTx, out_pull_down = 0x0, out_pull_up = 0x0.
2. Single-ended measurement.
3. Output frequency = 10MHz.

2.20 Power Supply Current

Table 22. Power Supply Current [1]

Symbol	Parameter	Condition		Typical	Maximum	Unit
I_{DD_CLK}	Supply current for V_{DD_CLK}	All CLKIN[3:0] enabled, single ended and supplied to a DPLL, Time Sync TDC enabled, Ref4 supplied to the TDCAPLL		28	55	mA
		All CLKIN[3:0] enabled, differential and supplied to a DPLL		29	32	
I_{DDXO_DCD}	Supply current for V_{DDXO_DCD}	V_{DDXO_DCD} = 1.89V		49	54	mA
I_{DD_VCO}	Supply current for V_{DD_VCO}	V_{DD_VCO} = 1.89V		162	171	mA
I_{DD_DIG}	Supply current for V_{DD_DIG}	V_{DD_DIG} = 1.89V or 3.465V, All FODs off $I_{DD_FODDIGBASE}$		40	46	mA
		V_{DD_DIG} = 1.89V or 3.465V Current adder for one FOD at 120MHz $I_{DD_PERFODDIG}$		7	11	
		V_{DD_DIG} = 1.89V or 3.465V Current adder for one FOD at 793MHz $I_{DD_FODDIGPERMHZ}$		9	15	
I_{DD_FODx}	Supply current for V_{DDOx_FODx}[2]	V_{DDOx_FODx} = 1.89V Current with the FOD off $I_{DD_FODBASE}$		3	5	mA
		V_{DDOx_FODx} = 1.89V Current adder for one FOD at 120MHz I_{DD_PERFOD}		42	47	
		V_{DDOx_FODx} = 1.89V Current adder for one FOD at 793MHz IFODDIG793		51	57	
I_{DD_REP}	Supply current for V_{DD_REP}	V_{DD_REP} = 1.89V		8	9	mA
I_{DD_FAN}	Supply current for V_{DD_FAN}	V_{DD_FAN} = 1.89V		122	156	mA
I_{DDOx} [3]	Supply current for V_{DDOx}	HCSL mode, 245.76MHz	out_boost = 0x0	24	29	mA
			out_boost = 0x1	27	32	
			out_boost = 0x2			
			out_boost = 0x3	28	34	
I_{DDOx} [3]	Supply current for V_{DDOx}	LVDS mode, 245.76MHz	out_boost = 0x0	14	18	mA
			out_boost = 0x1			
			out_boost = 0x2			
			out_boost = 0x3			
I_{DDOx} [3]	Supply current for V_{DDOx}	CML mode, 245.76MHz	out_boost = 0x0	2	11	mA
			out_boost = 0x1			
			out_boost = 0x2			
			out_boost = 0x3			
I_{DDOx} [3]	Supply current for V_{DDOx}	LVCMOS mode	out_cmos_same_phase = 0x0	3	29	mA
			out_cmos_same_phase = 0x1	3	36	
I_{DDOx} [3]	Supply current for V_{DDOx}	Output disabled		2	5	mA

1. Internal dynamic switching current at maximum f_{OUT} is included, unless otherwise noted.
2. For I_{DD_FOD0} this value does not include supply currents for GPIO outputs.
3. Measured with outputs unloaded.

2.21 GPIO, Serial Port, and nMR DC Electrical Characteristics

Table 23. GPIO, Serial Port, and nMR DC Electrical Characteristics [1][2][3][4]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{IH}	Input high voltage	-	0.6 x V_{DDx}	-	V_{DDx} + 0.3	V
V_{IL}	Input low voltage	-	-0.3	-	0.4 x V_{DDx}	V
V_{OH}	Output high voltage	I_{OH} = -2mA	V_{DDx} - 0.45	-	V_{DDx} + 0.3	V
V_{OL}	Output low voltage	I_{OL} = 2mA	-	-	0.45	V
V_{OH}	Output high voltage	I_{OH} = -100µA	V_{DDx} - 0.2	-	V_{DDx} + 0.3	V
V_{OL}	Output low voltage	I_{OL} = 100µA	-	-	0.2	V

1. Applies to GPIO[4:0], SCL_SCLK, SDA_SDIO, SDO_A1, nCS_A0, and nMR.
2. Input specifications refer to pins acting as inputs, output specifications refer to pins acting as outputs.
3. V_{DDx} refers to V_{DD_DIG} for SCL_SCLK, SDA_SDIO, SDO_A1, and nCS_A0; and it refers to V_{DD_FOD0} for GPIO[4:0] and nMR (see Pin Assignments).
4. Values are compliant with JESD8-7A.

2.22 CMOS GPIO, Serial Port, and nMR Common Electrical Characteristics

Table 24. CMOS GPIO, Serial Port, and nMR Common Electrical Characteristics [1][2][3]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
I_{IL}	Input leakage current	Does not include input pull-up/pull-down resistor current. V_{IL} = 0V, V_{IH} = V_{DDx}	-50	-	50	µA
R_P	Pull-up/pull-down resistor	If enabled	-	53	-	kΩ

1. Applies to GPIO[4:0], SCL_SCLK, SDA_SDIO, SDO_A1, nCS_A0, and nMR.
2. Input specifications refer to pins acting as inputs, output specifications refer to pins acting as outputs.
3. V_{DDx} refers to V_{DD_DIG} for SCL_SCLK, SDA_SDIO, SDO_A1, and nCS_A0; and it refers to V_{DD_FOD0} for GPIO[4:0] and nMR (see Pin Assignments).

2.23 I²C Bus Target Timing Diagram

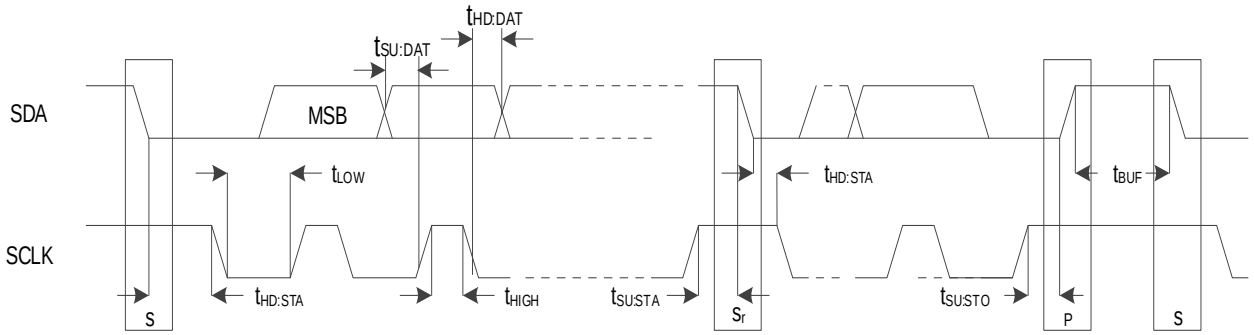


Figure 5. I²C Bus Target Timing Diagram

2.24 I²C Bus Target Timing

Table 25. I²C Bus Target Timing

Symbol	Parameter	Condition	Minimum	Maximum	Unit
f_{SCL}	SCL clock frequency	-	10	1000	kHz
$t_{HD:STA}$	Hold time after (REPEATED) START Condition	-	0.26	-	µs
t_{LOW}	Clock low period	-	0.5	-	µs
t_{HIGH}	Clock high period	-	0.26	-	µs
$t_{SU:STA}$	REPEATED START Condition setup time	-	0.26	-	µs
$t_{HD:DAT}$	Data hold time	-	0	-	ns
$t_{SU:DAT}$	Data setup time	-	50	-	ns
$t_{SU:STO}$	STOP condition setup time	-	0.26	-	µs
t_{BUF}	Bus free time between STOP and START Condition	-	0.5	-	µs
t_{SPIKE}	Noise spike suppression time [1]	i2c_spike_fltr = 0x3	-	50	ns

1. Device rejects noise spikes of a duration up to the maximum specified value.

2.25 I²C Bus AC/DC Electrical Characteristics

Table 26. I²C Bus AC/DC Electrical Characteristics [1]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{IH}	High-level input voltage for SCL_SCLK and SDA_SDIO	-	0.6 x V_{DD_DIG}	-	-	V
V_{IL}	Low-level input voltage for SCL_SCLK and SDA_SDIO	-	-	-	0.4 x V_{DD_DIG}	V
V_{HYS}	Hysteresis of Schmitt trigger inputs	-	0.05 x V_{DDD_DIG}	-	-	V
V_{OL}	Low-level output voltage for SDA_SDIO	I_{OL} = 4mA	-	-	0.4	V
I_{IN}	Input leakage current per pin	-	[2]	-	[2]	µA

1. VOH is governed by the V_{PUP}, the voltage rail to which the pull-up resistors are connected.
2. See Table 24.

2.26 SPI Target Timing Diagrams

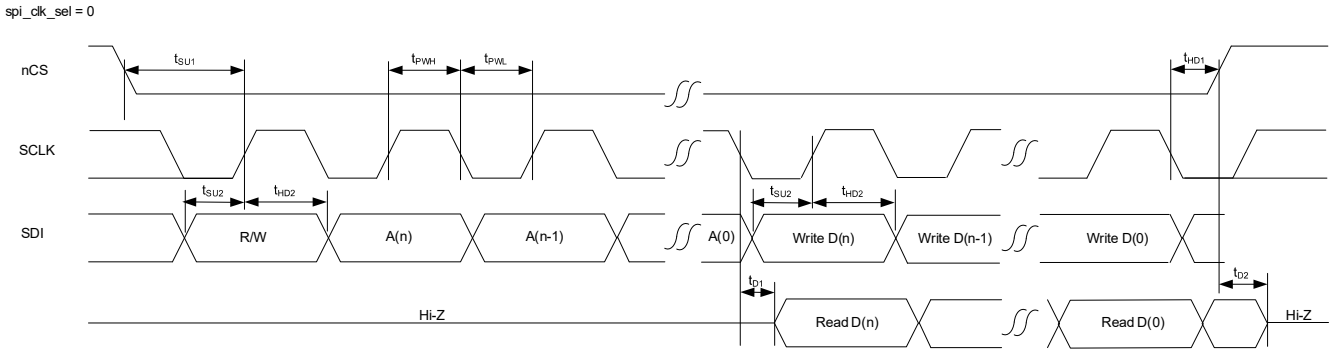


Figure 6. SPI Timing Diagram (SPI_CLK_SEL = 0)

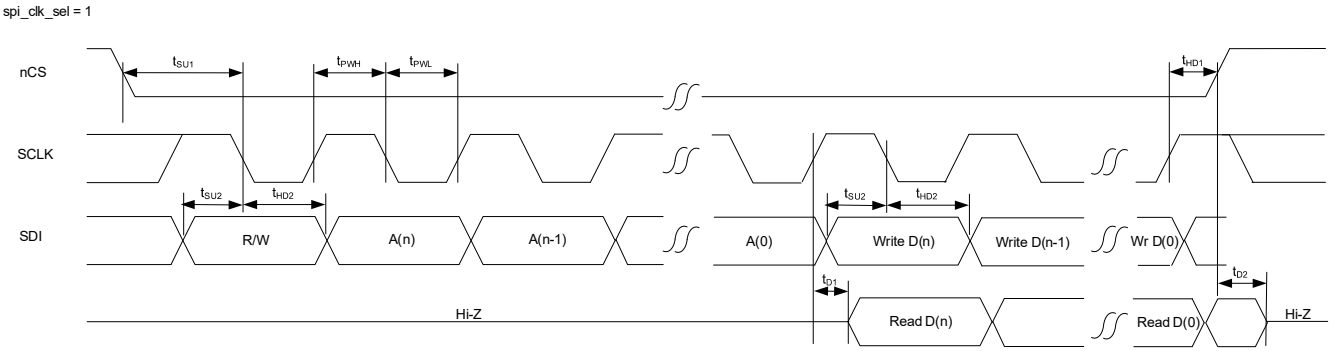


Figure 7. SPI Timing Diagram (SPI_CLK_SEL = 1)

2.27 SPI Target Timing

Table 27. SPI Target Timing

Symbol	Parameter	Minimum	Typical	Maximum	Unit
f_{MAX}	Maximum operating frequency	0.1	-	20	MHz
t_{PWH}	SCLK pulse width high	14	-	-	ns
t_{PWL}	SCLK pulse width low	14	-	-	ns
t_{SU1}	nCS setup time to SCLK rising or falling edge	10	-	-	ns
t_{HD1}	nCS hold time from SCLK rising or falling edge	2	-	-	ns
t_{SU2}	SDIO setup time to SCLK rising or falling edge	4	-	-	ns
t_{HD2}	SDIO hold time from SCLK rising or falling edge	3	-	-	ns
t_{D1}	Read data valid time from SCLK rising or falling edge	4.7	-	7.4	ns
t_{D2}	SDIO read data Hi-Z time from CS high [1]	-	-	14.5	ns

1. This is the time until the device releases the signal. Rise time to any specific voltage is dependent on pull-up resistor strength and PCB trace loading.

3. Functional Description

3.1 Overview

The RC38312/RC38112 is an ultra-low phase noise radio synchronizer, multi-frequency clock synthesizer, and digitally controlled oscillator (DCO). This flexible, low-power device outputs clocks with ultra-low, in-band phase noise and spurious for 4G and 5G RF transceivers and with jitter below 25fs-rms for 112Gbps and 224Gbps SerDes.

The RC38312/RC38112 has four differential clock inputs and 12 differential clock outputs. The RC38312 provides three digital PLLs (DPLL), and the RC38112 provides one DPLL. Both devices provide an ultra-low phase noise analog PLL (APLL) based clock synthesizer, and three low phase noise fractional output divider (FOD) based clock synthesizers. For device block diagrams, see Figure 2 and Figure 3.

The differential clock inputs can each be configured as two single-ended inputs. The clock inputs can operate at frequencies up to 1GHz for differential and 250MHz for single-ended.

Eight of the differential outputs can be configured as LVDS, HCSL (AC-LVPECL) or CML outputs. Four of the differential outputs can be configured as LVDS or HCSL (AC-LVPECL) outputs, or they can each be configured as two LVCMOS outputs. The LVDS and HCSL (AC-LVPECL) outputs can operate at frequencies up to 1GHz, the CML outputs can operate at frequencies up to 2.5GHz, and the LVCMOS outputs can operate at frequencies up to 250MHz.

3.2 APLL Frequency Reference

The RC38312/RC38112 requires an APLL frequency reference. The frequency reference must support the phase noise, frequency accuracy, and frequency stability requirements of the intended application.

The frequency reference can be implemented using an external crystal resonator connected between the XIN and XOUT pins and the device oscillator circuitry. Alternatively, an external oscillator can be connected to the XIN pin to overdrive the internal oscillator circuitry.

If a crystal resonator is used for the frequency reference, the resonant frequency must be from 25MHz to 80MHz. If an external oscillator is used, it must provide a low-phase noise clock with frequency from 25MHz to 100MHz. For frequency reference requirements, see Table 12 and Table 13.

For all applications, the phase noise of the frequency reference, after filtering by the APLL, is the minimum phase noise that will appear on all clocks output by the device.

For DPLL applications, the accuracy of the frequency reference determines the frequency accuracy of the reference monitors and free-running clocks. The stability of the frequency reference determines the holdover stability of the DPLL and it affects the lowest filtering bandwidth the DPLL can support.

For DCO applications, the accuracy of the frequency reference determines the frequency accuracy of the free-running clocks. The stability of the frequency reference determines the stability of the DCO clocks when a source of synchronization is not available, and it affects the lowest filtering bandwidth that a filtering algorithm can support.

The accuracy of the frequency reference should be chosen to meet the free-running frequency accuracy requirements of the application (see Table 28 for examples) and to allow sufficient APLL frequency steering range for a DPLL or DCO to lock the APLL to its reference and to track reference noise.

The available APLL frequency steering range ($\pm F_{STEER}$) is determined by the following expression: $F_{STEER} = |F_{TOL}| - |F_{ACC}|$; where F_{ACC} is the accuracy of the frequency reference. See Table 12 for the value of F_{TOL} and for additional details.

Table 28. Recommended Free-Running Frequency Accuracy by Application

Application	Recommended Free-Running Frequency Accuracy (PPM)
PCIe Free-running clock synthesizer	±100
Most Ethernet types Jitter attenuator or free-running clock synthesizer	±100
800GBASE-xR8, 10GBASE-T Jitter attenuator or free-running clock synthesizer	±50
100GBASE-ZR, 10GBASE-W Jitter attenuator or free-running clock synthesizer	±20
ITU-T G.8262, G.8262.1 SEC, EEC, OEC, eSEC, eEEC, eOEC	±4.6
ITU-T G.8273.2, G.8273.3 T-BC, T-TSC, T-BC-A, T-TSC-A, T-BC-P, T-TSC-P	±4.6

3.3 Analog PLL

The internal APLL has a bandwidth of approximately 1MHz, it locks to the frequency reference and synthesizes an ultra-low phase noise clock of virtually any frequency from 9.70GHz to 10.40GHz, or from 9.30GHz to 10.0GHz, depending on the version of the device. The APLL inherits the frequency accuracy of the frequency reference and this determines the free-run frequency accuracy of the device.

The APLL can be assigned as the primary synthesizer for DPLL0 and its FFO can be steered by DPLL0. When DPLL0 is locked to a reference, the APLL output clock and its derivatives have the same long-term frequency accuracy as the reference.

The APLL output clock is pre-divided by 2, 3, 5, or 7 and is available to the integer output dividers (IOD). The pre-divided APLL clock is available directly to IOD[5:0]; it is also available via cross-connect to IOD[11:6]. The undivided APLL clock is supplied to FOD[3:0].

3.4 Integer Output Dividers

Each IOD divides its input clock by a programmable 23-bit integer value.

3.5 Fractional Output Dividers

The FODs divide the APLL clock to synthesize low phase noise clocks with programmable frequencies. The FODs are capable of integer division, rational division (that is, M/N), and fractional division with 1 part per trillion frequency resolution. The FOD output clocks are available via cross-connect to IOD[11:6].

When configured for fractional division, the FODs can operate as DCOs, and they can cancel digital frequency adjustments made to the APLL via the Combo Bus so that their output frequencies are virtually unaffected by digital steering of the APLL. The frequency steering range of the FODs is ±244PPM.

3.6 Divider Synchronization

For each DPLL, the feedback divider is synchronized with the IODs selected to divide the output of its synthesizer. The rising edges of clocks from these dividers will be aligned for every Nth rising edge of the synthesizer clock, where N is the lowest common multiple of the accumulated divide ratios along the paths from the synthesizer to the divider outputs.

Consider the following example: DPLL0 uses the APLL as its synthesizer. The DPLL is locked to a 1kHz input reference and the APLL is operating at 10GHz. The pre-divider supplies a 5GHz clock to IOD1, IOD2, and the DPLL feedback divider. IOD1 uses a divide ratio of 40 to produce a 125MHz clock, IOD2 uses a divide ratio of 625,000 to produce an 8kHz clock, and the DPLL feedback divider uses a divide ratio of 5,000,000 to produce 1kHz at the DPLL phase detector. In this example, the lowest common multiple of the divisors along the three

paths is 10,000,000. Therefore, the outputs of IOD1 and IOD2 will be aligned with the input reference once for every 10,000,000 edges of the 10GHz clock. In other words, the 1kHz reference, the 8kHz and the 125MHz clocks will be aligned for every edge of the 1kHz input reference (excluding the effects of reference noise and DPLL filtering).

3.7 Digital PLLs

Up to five of the clock inputs can be selected as inputs for the reference monitors and the DPLL reference selection multiplexer. The DPLLs can lock to reference frequencies from 1kHz to 33MHz; clock inputs with frequencies above 33MHz must be divided using the internal reference dividers. Each DPLL steers its respective synthesizer (APLL or FOD) using digital frequency control words via the Combo Bus. The DPLLs support loop filter settings from 1mHz to 1kHz.

In DCO mode, the DPLLs do not lock to an input reference and its frequency is steered by external software instead.

The DPLLs operate in five states: Free-run, Acquire, Normal, Holdover, and Hitless Switch.

3.7.1 DPLL Free-Run State

In the Free-run state, a DPLL does not generate frequency control words and its respective synthesizer operates based on the frequency reference, and, if so configured, on information from other channels via the Combo Bus.

3.7.2 DPLL Acquire State

In the Acquire state, a DPLL tracks the selected qualified reference with the acquisition bandwidth and damping factor settings until the DPLL declares lock. The acquisition bandwidth and damping factor can be configured to accelerate the locking process. When a DPLL achieves lock it automatically transitions to the Normal state.

3.7.3 DPLL Normal State

In the Normal state, a DPLL tracks the selected reference with the normal locking bandwidth and damping factor settings. The normal bandwidth and damping factor can be configured to meet the filtering requirements of the intended application. In the Normal state, the long-term FFO of the DPLL synthesizer output clocks is the same as the long-term FFO of the reference and no cycle slips will occur.

3.7.4 DPLL Holdover State

In the Holdover state, a DPLL outputs digital frequency control words based on data acquired while in the Normal state so that its synthesizer outputs accurate frequencies when a reference is not provided to the DPLL. While a DPLL is in the Holdover state, its synthesizer operates based on the frequency reference, the DPLL holdover data, and, if so configured, on information from other channels via the Combo Bus.

3.7.5 DPLL Hitless Switch State

In the Hitless Switch state, the DPLL enters Holdover and measures the phase offset between the selected reference and the DPLL feedback clock. The measured phase offset is stored by the DPLL and is used to minimize the phase transient at the output of the DPLL when it locks to the new reference.

3.8 DPLL External Feedback

In some applications it is useful to use an external feedback path from the synthesizer to the DPLL. The DPLL reference selection multiplexer can select one of the external references for use as the feedback clock for the DPLL. When external feedback is used, the feedback clock must have the same frequency as the selected DPLL reference.

3.9 DPLL Reference Switching

The active reference for a DPLL is determined by forced selection or by automatic selection based on user-programmed priorities, locking allowances, reference monitors, revertive and non-revertive settings, and GPIO LOS inputs.

A DPLL will act to close phase differences between the selected reference and the feedback clock. A step change in the phase difference can occur when a new reference is selected while the DPLL is in the Acquire state or the Normal state, or when the DPLL exits the Holdover state and enters the Acquire state. The resulting phase transient is filtered by the DPLL loop filter and the phase slope limiter, and there will not be any instantaneous phase steps or glitches on the device outputs.

3.9.1 Hitless Reference Switching

Hitless reference switching causes a DPLL to ignore the phase difference between the newly selected reference and the DPLL feedback clock; the DPLL will track the FFO of the newly selected reference.

When hitless reference switching is enabled – and a DPLL is in the Acquire state or the Normal state, and the selected reference is changed – the DPLL enters the Holdover state and measures the phase offset between the newly selected reference and the DPLL feedback clock. The measured phase offset is stored and is subtracted from later phase offsets measured by the DPLL phase detector. The DPLL then enters the Acquire state.

When the DPLL is in the Holdover state due to a reference failure or any other reason, hitless reference switching can be used when entering the Acquire state.

3.9.2 Aligned Reference Switching

Hitless reference switching does not allow a deterministic phase relationship to exist between the DPLL reference and its output clocks. When a deterministic phase relationship is needed, hitless reference switching should not be enabled so that the DPLL can align its output clocks with the DPLL reference.

3.10 Clock Output Enable

The RC38312/RC38112 enables and disables clock outputs synchronously to ensure there are no runt pulses during clock output enable and disable operations.

Clock output enables can be controlled by software using the global_oe and out_driver_en register fields. Alternatively, GPIOs can be assigned the clock output enable function using the oe_source_sel and gpio_func register fields. For more information, see the *RC38312, RC38112, RC38208, RC38108 Programming Guide*.

When a GPIO is assigned an output enable function it should be configured with gpio_resync = 0x0 and gpio_deglitch_bypass = 0x1; this disables GPIO resynchronization and bypasses the GPIO deglitcher ensuring lowest latency. When so configured, the maximum time delay from the time the voltage level on a GPIO input changes state until the clock output is enabled or disabled is 13ns plus 4 periods of the output clock.

3.11 Reference Monitors

The references can be continually monitored for loss of signal and for frequency offset per user programmed thresholds.

3.12 SYSREF

The RC38312/RC38112 includes a SYSREF controller that can output SYSREF signals on any of OUT[11:0].

The SYSREF controller can be configured to generate a continuous stream of SYSREF pulses triggered by a signal on a level-sensitive GPIO, active high or active low. Continuous SYSREF generation can also be controlled by a register bit.

The SYSREF controller can be configured to generate a programmable number, from 1 to 255, of SYSREF pulses triggered by a signal on an edge-sensitive GPIO. The GPIO can be programmed to be rising or falling edge sensitive. A programmable number of SYSREF pulses can also be triggered by writing a register bit.

A single RC38312/RC38112 device can control several other connected RC38312/RC38112 devices so that they all generate simultaneous and aligned SYSREF signals. The controlling device can be triggered as described above.

3.13 Time Sync

The RC38312/RC38112 includes a Time Sync block that enables external software to monitor and control phase and time alignment of the device with external signals and devices.

The time of day (TOD) and Synthesis block synthesizes a time clock with a frequency from 10MHz to 250MHz. The block includes a 60-bit addressable TOD accumulator that counts time clock pulses and generates sync pulses with a frequency from 0.5Hz to 8kHz. The phase of the time sync pulses can be controlled by external software without disturbing the time clock. Any one of the FODs can be used to control the frequency of time clock. The time clock and time sync signals are available on any of OUT[11:8].

A time-to-digital converter (TDC) is provided to make precision phase and time comparisons between external signals, between internal signals, or between internal and external signals with frequencies between one-time-event and 33MHz. Internal signals available to the TDC are the time clock, time sync, and the DPLL feedback clocks. The precision of the TDC is better than 100ps.

3.14 Status and Control

All control and status registers are accessed through a 1MHz I^2C or 20MHz SPI Target microprocessor interface. The device can automatically load a configuration from internal one time programmable (OTP) memory. Alternatively, the I^2C controller interface can automatically load a configuration from an external EEPROM after reset.

For more information about the device's registers, contact Renesas Technical Support.

4. Applications Information

4.1 Power Considerations

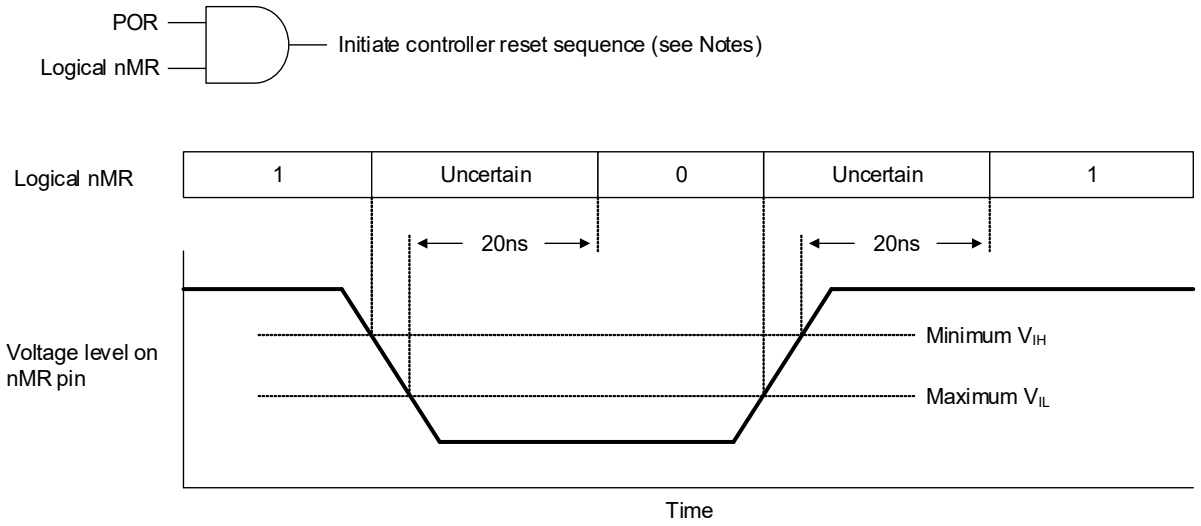
There are no power supply sequencing requirements when nMR is asserted (externally driven low); however, if nMR is left floating and if V_{DDOx} or V_{DD_CLK} reach 90% of V_{DD} nominal after V_{DD_DIG}, then a soft reset or a controller reset must be initiated to ensure the output dividers are synchronized.

For power and current consumption calculations, see the Renesas IC Toolbox (RICBox) software tool.

4.2 Power-On Reset and Reset Controller

Upon power-up, an internal power-on reset (POR) signal is asserted 20ms after the V_{DDXO}, V_{DD_DCD}, and V_{DDD33_DIG} supplies all reach 90% of V_{DD} nominal. The first controller reset sequence is initiated when POR is asserted and the voltage level on the nMR pin is high.

After the first controller reset sequence is initiated, another controller reset sequence can be initiated by taking the voltage level on the nMR pin low and then high while POR remains asserted (see Figure 8). To ensure a controller reset sequence is initiated, the voltage level on the nMR pin must be held low for at least 20ns before transitioning high. To ensure deterministic behavior, voltage level transitions on the nMR pin must be monotonic between minimum V_{IH} and maximum V_{IL} (see Table 23).



Notes:
- Requires 1 from logical nMR for the first controller reset sequence
- Requires 0 to 1 transition from logical nMR after the first controller reset sequence has been initiated

Figure 8. Controller Reset Sequence Initiation

The nMR pin has an internal pull-up that can be left to float, or it can optionally be externally pulled high or low. If nMR is high when the internal POR is asserted, the reset controller will initiate a controller reset sequence. If nMR is low when the internal POR is asserted, the reset controller will not initiate a controller reset sequence until nMR is taken high.

During the controller reset sequence all clock outputs are initially disabled and will be enabled during the reset sequence at a point depending on the out_startup bits. Disabled differential outputs will have OUTx = low and nOUTx = high. Disabled LVCMOS outputs with cmos_same_phase = 1 will have OUTx = low and nOUTx = low. Disabled LVCMOS outputs with cmos_same_phase = 0 will have OUTx = low and nOUTx = high.

The serial ports are accessible when the device_ready_sts register bit is set to 0x1. Any GPIO can be configured to indicate the state of the device_ready_sts register bit by setting the associated gpio_func register field to 0x18. When a reset sequence completes, the rst_done_sts register bit is set to 0x1.

When a configuration is loaded from EEPROM, the voltage level on the nMR pin must be held high from the time a controller reset sequence is initiated until after the EEPROM transactions have completed, as indicated when the device_ready_sts bit is set to 1. Any GPIO can be configured to indicate the state of the device_ready_sts bit.

4.3 Recommendations for Unused Input and Output Pins

4.3.1 CLKIN/nCLKIN Pins

Unused CLKIN/nCLKIN pins should be left to float. Renesas recommends that CLKIN/nCLKIN inputs that are connected but not used, should not be driven with active signals.

4.3.2 LVCMOS Control Pins

LVCMOS control pins have internal pull-up resistors. Additional 1kΩ pull-up resistors can be added but are not required.

4.3.3 LVCMOS Output Pins

Unused LVCMOS outputs must be left to float. Renesas recommends that no trace should be attached. Unused LVCMOS outputs should be configured to a high-impedance state to prevent noise generation.

4.3.4 Differential Output Pins

Unused differential outputs must be left to float. Renesas recommends that no trace should be attached. Both sides of a differential output pair should be either left to float or terminated.

4.4 Overdriving the Crystal Interface

When overdriving the crystal interface, the XOUT pin is left to float and the XIN input is overdriven by an AC coupled LVCMOS driver, or by one side of an AC coupled differential driver. The XIN pin is internally biased to 0.6V. The voltage swing on XIN should be between 0.5V peak-to-peak and 1.2V peak-to-peak, and the slew rate should not be less than 0.6V/ns.

Figure 9 shows a 1.8V or 2.5V LVCMOS driver overdriving the XIN pin. For V_{DD} = 1.8V, considering the output impedance of the driver (R_O), the values of the series resistance (R_S) and R_1 should be chosen so that the voltage swing on XIN will be below 1.2V peak-to-peak. For V_{DD} = 2.5V the sum of the output impedance of the driver (R_O) and the series resistance (R_S) can be made higher than R_1 so that the voltage swing on XIN will be below 1.2V peak-to-peak.

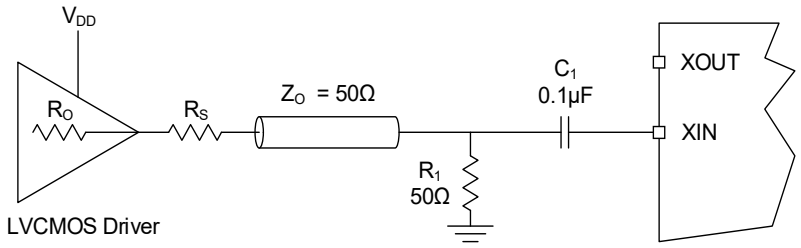


Figure 9. LVCMOS Driver to Crystal Input Interface

Figure 10 shows one side of an LVPECL driver overdriving the XIN pin.

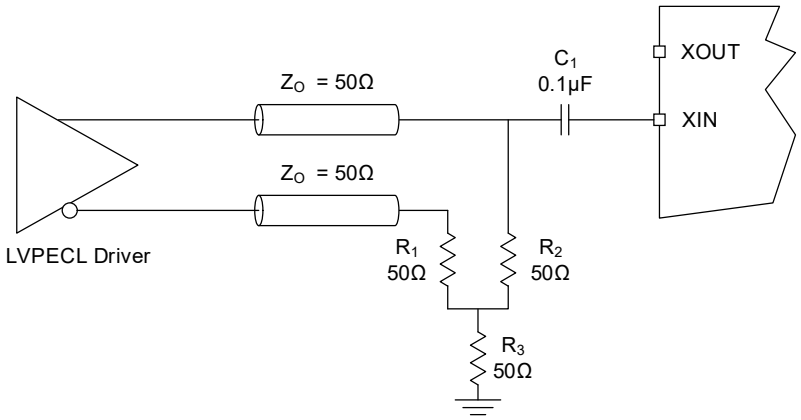


Figure 10. LVPECL Driver to Crystal Input Interface

4.5 Differential Output Termination

The RC38312/RC38112 programmable differential clock outputs support LVDS, HCSL, and CML. Receivers that support LVDS, HCSL, or CML can be direct-coupled with RC38312/RC38112 outputs. Differential receiver types other than LVDS, HCSL, or CML can be AC-coupled.

The RC38312/RC38112 differential clock outputs support selectable internal termination resistors as shown in Figure 11. The value of resistors R_{O1}, R_{O2}, R_{O3}, and R_{O4} is 50Ω.

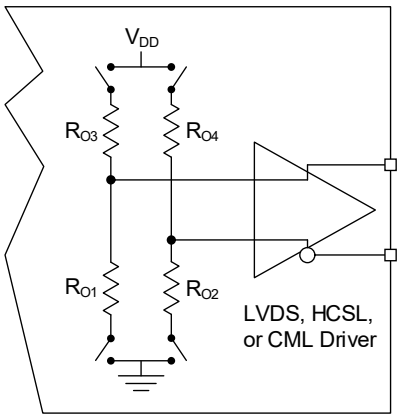


Figure 11. Internal Termination Resistors for Differential Drivers

Note: Some receivers are equipped with internal terminations that can include the following: trace termination, voltage biasing, and AC-coupling. Consult with the receiver specifications to determine if the termination components shown in this section are needed.

4.5.1 Direct-Coupled HCSL Termination

For HCSL receivers, RC38312/RC38112 clock outputs should be configured for HCSL, and the devices should be direct-coupled. The RC38312/RC38112 supports several programmable HCSL voltage swing options.

Figure 12 shows an HCSL driver direct-coupled with an HCSL receiver and configured for internal source termination. The RC38312/RC38112 supports source termination, with an internal 50Ω resistors to ground at the transmitter. Resistor R_1 is optional and is used to improve impedance matching. If R_1 is used, it will reduce the amplitude at the receiver by 50%, this can be mitigated by adjusting the output amplitude of the driver.

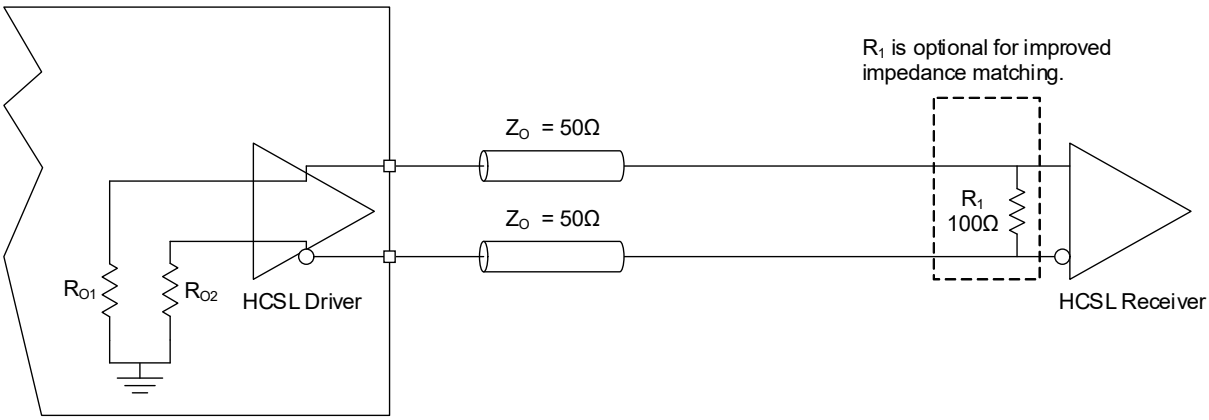


Figure 12. HCSL Source Termination Using Internal Termination

Figure 13 shows an HCSL driver direct-coupled with an HCSL receiver using end termination.

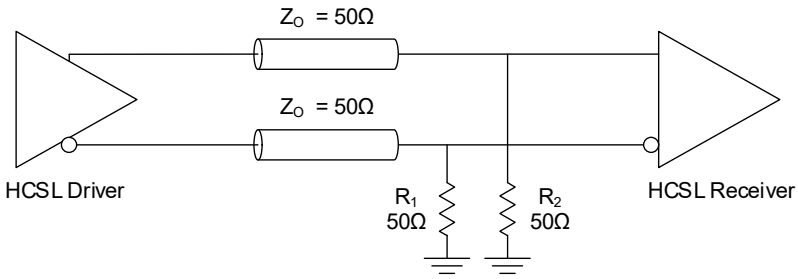


Figure 13. HCSL End Termination

4.5.2 Direct-Coupled LVDS Termination

For LVDS receivers, RC38312/RC38112 clock outputs should be configured for LVDS, and should be direct-coupled. The RC38312/RC38112 supports several programmable LVDS voltage swing and common mode options.

Figure 14 shows an LVDS driver direct-coupled with an LVDS receiver. The recommended value for the termination resistor (R_1) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Z_0) of the transmission line. To avoid transmission-line reflection issues, R_1 should be surface-mounted and placed as close to the receiver as practical.

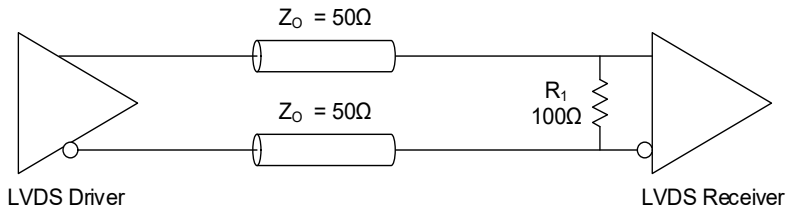


Figure 14. LVDS Termination

4.5.3 Direct-Coupled CML Termination

For CML receivers, RC38312/RC38112 clock outputs should be configured for CML, and should be direct-coupled. The RC38312/RC38112 supports several programmable CML voltage swing options.

Figure 15 shows a CML driver direct-coupled with a CML receiver.

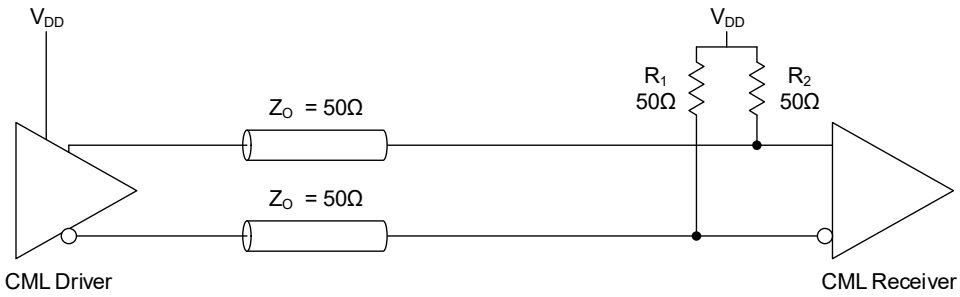


Figure 15. Direct-Coupled CML Termination

4.5.4 AC-Coupled Differential Termination

For AC-coupled differential terminations, the RC38312/RC38112's clock outputs should be configured for HCSL and the HCSL driver should be configured with a voltage swing appropriate for the receiver. The RC38312/RC38112 supports several programmable HCSL voltage swing options.

Figure 16 shows an HCSL driver configured for internal termination and AC-coupled with a differential receiver with external termination resistors and biasing. Resistors R_1, R_2, R_3, and R_4 should be selected to provide the appropriate bias voltage for the receiver. Consult receiver specifications for input swing and bias requirements. An optional resistor (R_5) can be used to improve impedance matching. If R_5 is used, it will reduce the amplitude at the receiver by 50%; this can be mitigated by adjusting the output amplitude of the driver.

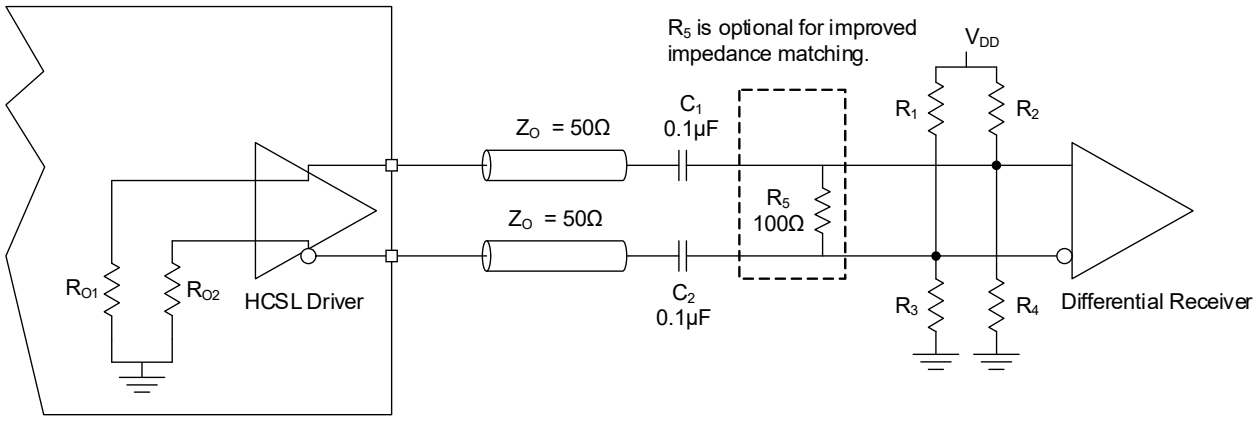


Figure 16. AC-Coupled Differential Termination

For more information on AC-coupling, see Renesas application note AN-953, *Quick Guide - Output Terminations*.

4.5.5 AC-Coupled LVPECL (AC-LVPECL) Termination

AC-coupling should be used for LVPECL receivers.

For AC-coupled LVPECL (AC-LVPECL) terminations, the RC38312/RC38112 clock outputs should be configured for HCSL. The RC38312/RC38112 supports several programmable HCSL voltage swing options and it should be configured as appropriate for the receiver and termination scheme. Consult receiver specifications for input swing and bias requirements.

Figure 17 shows an HCSL driver configured for internal termination driving an AC-LVPECL receiver with internal termination resistors and biasing.

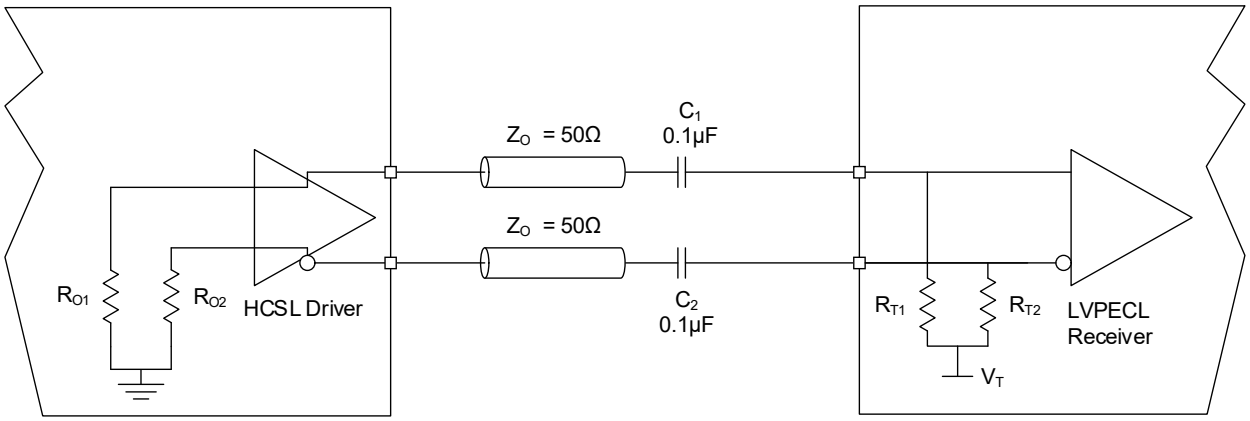


Figure 17. AC-LVPECL Termination for LVPECL Receiver with Internal Termination Resistors and Biasing

For more information on AC-coupling, see Renesas application note AN-953, *Quick Guide - Output Terminations*.

5. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

6. Marking Diagrams



- Lines 1 and 2: part number.
- Line 3:
  - "$" indicates the mark code.
  - "YWW" indicates the last digit of the year and work week the part was assembled.
  - "#" indicates the last three characters of assembly lot.

Figure 18. RC38312A Marking Diagram



- Lines 1 and 2: part number.
- Line 3:
  - "$" indicates the mark code.
  - "YWW" indicates the last digit of the year and work week the part was assembled.
  - "#" indicates the last three characters of assembly lot.

Figure 19. RC38112A Marking Diagram

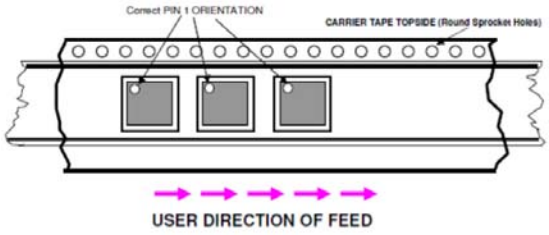
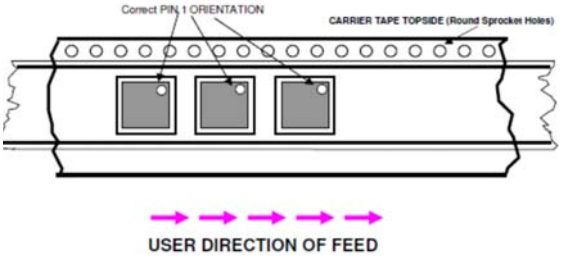
7. Ordering Information

Table 29. Ordering Information

Part Number [1][2]	Package Description	Carrier Type	Temperature Range [3]
RC38312AyxxGBB#HC0	100-BGA, 9 × 9 mm	Tape, Pin 1 orientation: EIA-481-C	-40 to +105°C
RC38312AyxxGBB#KC0	100-BGA, 9 × 9 mm	Tape, Pin 1 orientation: EIA-481-D/E	
RC38312AyxxGBB#BC0	100-BGA, 9 × 9 mm	Tray	
RC38112AyxxGBB#HC0	100-BGA, 9 × 9 mm	Tape, Pin 1 orientation: EIA-481-C	-40 to +105°C
RC38112AyxxGBB#KC0	100-BGA, 9 × 9 mm	Tape, Pin 1 orientation: EIA-481-D/E	
RC38112AyxxGBB#BC0	100-BGA, 9 × 9 mm	Tray	

1. Replace "y" in the part number with "1" for VCO frequency range 9.8GHz to 10.35GHz, or "2" for VCO frequency range 9.3GHz to 9.85GHz.
2. Replace "xx" in the part number with the desired pre-programmed configuration code provided by Renesas in response to a custom configuration request or use "00" for unprogrammed parts.
   Note: An unprogrammed part supports four default configurations: config_0 (SPI 4-wire), config_1 (SPI 3-wire), config_2 (I2C), and config_3 (external EEPROM).
3. Temperature range refers to board temperature.

Table 30. Pin 1 Orientation in Tape and Reel Packaging

Part Number Suffix	Pin 1 Orientation	Illustration
HC0	Quadrant 1 (EIA-481-C)	
KC0	Quadrant 2 (EIA-481-D/E)	

8. Revision History

Revision	Date	Description
1.13	Oct 5, 2026	▪ Changed the minimum value of f_{VCO} (Condition: RC38312x2xx, RC38112x2xx) to 9.3GHz in Crystal Oscillator Input and APLL AC/DC Electrical Characteristics ▪ Changed the second VCO frequency range in footnote 1 to 9.3GHz to 9.85GHz in Ordering Information
1.12	May 11, 2026	▪ Added a caution statement to Absolute Maximum Ratings
1.11	Nov 17, 2025	▪ Clarified the use of nMR in power sequencing in Power Considerations ▪ Added a note to footnote 2 in Table 29
1.10	Sep 2, 2025	▪ Updated Overdriving the Crystal Interface to indicate the slew rate should not be less than 0.6V/ns.; previously, it indicated 0.2V/ns ▪ Updated footnote 3 in Table 24 ▪ Changed use of the terms “master/slave” to “controller/target”
1.09	Aug 18, 2025	▪ Updated footnote 2 in Table 20 and Table 21 to indicate “Single-ended measurement.”
1.08	May 9, 2025	▪ Updated Figure 2 and Figure 3 ▪ Updated Table 3: • Changed V_{DDOx} to V_{DDx} • Changed the maximum value of the fourth condition for V_{IN}
1.07	Mar 25, 2025	▪ Added column numbers to Figure 4 ▪ Changed “device frequency reference” to “APLL frequency reference” in Table 12 and APLL Frequency Reference ▪ Updated t_R/t_F in Table 20
1.06	Jan 7, 2025	▪ Updated the footnotes in Table 19, Table 20, and Table 21
1.05	Dec 13, 2024	▪ Updated Table 6 ▪ Updated Z_{OUTDC} in Table 18 ▪ Updated the minimum value of V_{OVS} in Table 20 ▪ Added Clock Output Enable
1.04	Oct 29, 2024	▪ Updated footnote 1 in Ordering Information.
1.03	Sep 26, 2024	▪ Updated footnote 3 in Table 23 ▪ Added ECAD Design Information ▪ Completed other minor changes

Revision	Date	Description
1.02	Aug 7, 2024	▪ Updated the typical value of I_{DDOx} for CML and output disabled in Table 22
1.01	Jul 16, 2024	▪ Updated the Features list ▪ Updated the following tables: Table 14, Table 22, Table 23, Table 24, Table 26, Table 27, and Table 28
1.00	Jun 28, 2024	Initial release

A. ECAD Design Information

This appendix supports the development of the PCB ECAD model for this device. It is intended to be used by PCB designers.

A.1 Part Number Indexing

Orderable Part Number [1]	Number of Pins	Package Type	Package Code/POD Number
RC38312A1xxGBB#HC0	100	BGA	BJG100
RC38312A1xxGBB#KC0	100	BGA	BJG100
RC38312A1xxGBB#BC0	100	BGA	BJG100
RC38112A1xxGBB#HC0	100	BGA	BJG100
RC38112A1xxGBB#KC0	100	BGA	BJG100
RC38112A1xxGBB#BC0	100	BGA	BJG100
RC38312A2xxGBB#HC0	100	BGA	BJG100
RC38312A2xxGBB#KC0	100	BGA	BJG100
RC38312A2xxGBB#BC0	100	BGA	BJG100
RC38112A2xxGBB#HC0	100	BGA	BJG100
RC38112A2xxGBB#KC0	100	BGA	BJG100
RC38112A2xxGBB#BC0	100	BGA	BJG100

1. Replace “xx” in the part number with the desired pre-programmed configuration code provided by Renesas in response to a custom configuration request or use “00” for unprogrammed parts.

A.2 Symbol Pin Information

A.2.1 100-BGA

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
A1	V_{DD_VCO}	Power	-
A2	GND	Power	-
A3	V_{DDO0}	Power	-
A4	OUT0	Output	-
A5	OUT1	Output	-
A6	V_{DDO2}	Power	-
A7	OUT2	Output	-
A8	OUT3	Output	-
A9	V_{DDO4}	Power	-
A10	OUT4	Output	-
B1	V_{DD_FAN}	Power	-
B2	GND	Power	-
B3	V_{DDO1}	Power	-
B4	nOUT0	Output	-
B5	nOUT1	Output	-
B6	V_{DDO3}	Power	-
B7	nOUT2	Output	-
B8	nOUT3	Output	-
B9	V_{DDO5}	Power	-
B10	nOUT4	Output	-
C1	GND	Power	-
C2	GND	Power	-
C3	GND	Power	-
C4	GND	Power	-
C5	GND	Power	-
C6	GND	Power	-
C7	GND	Power	-
C8	GND	Power	-
C9	GND	Power	-
C10	OUT5	Output	-

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
D1	V_{DDXO_DCD}	Power	-
D2	GND	Power	-
D3	GND	Power	-
D4	V_{DD_DIG}	Power	-
D5	nCS_A0	Input	-
D6	GPIO4	I/O	-
D7	GPIO3	I/O	-
D8	GPIO2	I/O	-
D9	GND	Power	-
D10	nOUT5	Output	-
E1	XIN	Input	-
E2	GND	Power	-
E3	GND	Power	-
E4	V_{DD_CLK}	Power	-
E5	SCL_SCLK	I/O	-
E6	SDA_SDIO	I/O	-
E7	SDO_A1	I/O	-
E8	GPIO1	I/O	-
E9	GND	Power	-
E10	GND	Power	-
F1	XOUT	Output	-
F2	GND	Power	-
F3	GND	Power	-
F4	CLKIN0	Input	-
F5	CLKIN1	Input	-
F6	CLKIN2	Input	-
F7	CLKIN3	Input	-
F8	GPIO0	I/O	-
F9	GND	Power	-
F10	GND	Power	-
G1	GND	Power	-
G2	GND	Power	-
G3	GND	Power	-
G4	nCLKIN0	Input	-
G5	nCLKIN1	Input	-
G6	nCLKIN2	Input	-
G7	nCLKIN3	Input	-
G8	nMR	Input	-
G9	GND	Power	-
G10	nOUT6	Output	-
H1	GND	Power	-
H2	GND	Power	-
H3	GND	Power	-
H4	GND	Power	-
H5	GND	Power	-
H6	GND	Power	-
H7	GND	Power	-
H8	GND	Power	-
H9	GND	Power	-
H10	OUT6	Output	-
J1	V_{DD_REP}	Power	-
J2	nOUT11	Output	-
J3	V_{DD_FOD1}	Power	-
J4	nOUT10	Output	-
J5	V_{DD_FOD2}	Power	-
J6	nOUT9	Output	-

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
J7	V_{DD_FOD0}	Power	-
J8	nOUT8	Output	-
J9	V_{DDO6}	Power	-
J10	nOUT7	Output	-
K1	V_{DDO11}	Power	-
K2	OUT11	Output	-
K3	V_{DDO10}	Power	-
K4	OUT10	Output	-
K5	V_{DDO9}	Power	-
K6	OUT9	Output	-
K7	V_{DDO8}	Power	-
K8	OUT8	Output	-
K9	V_{DDO7}	Power	-
K10	OUT7	Output	-

A.3 Symbol Parameters

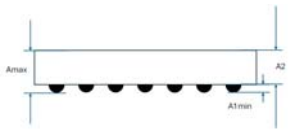
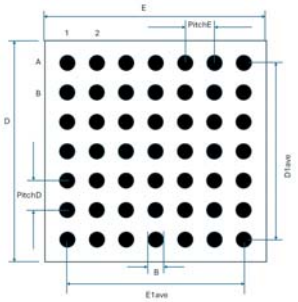
Orderable Part Number [1]	Qualification	Mounting Type	Min Operating Temperature	Max Operating Temperature	Min Input Voltage	Max Input Voltage	RoHS	Output Type	DPLL Channels	Interface	Max Output Frequency	Phase Jitter	XTAL Frequency
RC38312A1xxGBB#HC0	Industrial	SMD	-40 °C	85 °C	1.71 V	3.465 V	Yes	LVCMOS,LVDS,HCSL,CML	3	I2C,SPI	2500 MHz	25 fs	80 MHz
RC38312A1xxGBB#KC0	Industrial	SMD	-40 °C	85 °C	1.71 V	3.465 V	Yes	LVCMOS,LVDS,HCSL,CML	3	I2C,SPI	2500 MHz	25 fs	80 MHz
RC38312A1xxGBB#BC0	Industrial	SMD	-40 °C	85 °C	1.71 V	3.465 V	Yes	LVCMOS,LVDS,HCSL,CML	3	I2C,SPI	2500 MHz	25 fs	80 MHz
RC38112A1xxGBB#HC0	Industrial	SMD	-40 °C	85 °C	1.71 V	3.465 V	Yes	LVCMOS,LVDS,HCSL,CML	1	I2C,SPI	2500 MHz	25 fs	80 MHz
RC38112A1xxGBB#KC0	Industrial	SMD	-40 °C	85 °C	1.71 V	3.465 V	Yes	LVCMOS,LVDS,HCSL,CML	1	I2C,SPI	2500 MHz	25 fs	80 MHz
RC38112A1xxGBB#BC0	Industrial	SMD	-40 °C	85 °C	1.71 V	3.465 V	Yes	LVCMOS,LVDS,HCSL,CML	1	I2C,SPI	2500 MHz	25 fs	80 MHz
RC38312A2xxGBB#HC0	Industrial	SMD	-40 °C	85 °C	1.71 V	3.465 V	Yes	LVCMOS,LVDS,HCSL,CML	3	I2C,SPI	2500 MHz	25 fs	80 MHz
RC38312A2xxGBB#KC0	Industrial	SMD	-40 °C	85 °C	1.71 V	3.465 V	Yes	LVCMOS,LVDS,HCSL,CML	3	I2C,SPI	2500 MHz	25 fs	80 MHz
RC38312A2xxGBB#BC0	Industrial	SMD	-40 °C	85 °C	1.71 V	3.465 V	Yes	LVCMOS,LVDS,HCSL,CML	3	I2C,SPI	2500 MHz	25 fs	80 MHz
RC38112A2xxGBB#HC0	Industrial	SMD	-40 °C	85 °C	1.71 V	3.465 V	Yes	LVCMOS,LVDS,HCSL,CML	1	I2C,SPI	2500 MHz	25 fs	80 MHz
RC38112A2xxGBB#KC0	Industrial	SMD	-40 °C	85 °C	1.71 V	3.465 V	Yes	LVCMOS,LVDS,HCSL,CML	1	I2C,SPI	2500 MHz	25 fs	80 MHz
RC38112A2xxGBB#BC0	Industrial	SMD	-40 °C	85 °C	1.71 V	3.465 V	Yes	LVCMOS,LVDS,HCSL,CML	1	I2C,SPI	2500 MHz	25 fs	80 MHz

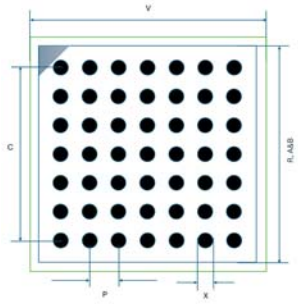
1. Replace “xx” in the part number with the desired pre-programmed configuration code provided by Renesas in response to a custom configuration request or use “00” for unprogrammed parts.

A.4 Footprint Design Information

A.4.1 100-BGA

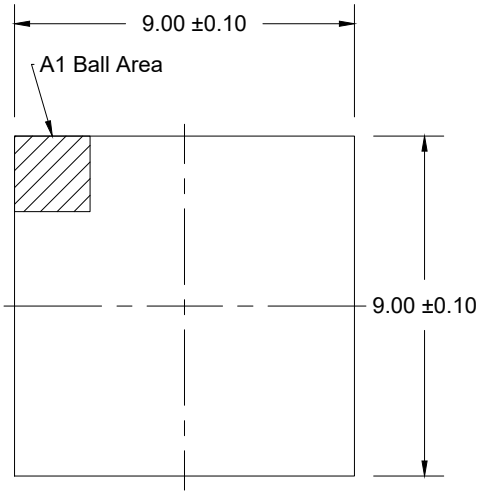
IPC Footprint Type	Package Code/ POD Number	Number of Pins
BGA	BJG100	100

Description	Dimension	Value (mm)	Diagram
Minimum body span (vertical side)	Dmin	8.9	
Maximum body span (vertical side)	Dmax	9.1	
Average length of grid (vertical side)	D1ave	7.2	
Minimum body span (horizontal side)	Emin	8.9	
Maximum body span (horizontal side)	Emax	9.1	
Average length of grid (horizontal side)	E1ave	7.2	
Minimum Standoff Height	A1min	0.30	
Maximum Height	Amax	1.19	
Average ball diameter	Bnom	0.469	
Distance between the center of any two adjacent balls (vertical side)	PitchD	0.8	
Distance between the center of any two adjacent balls (horizontal side)	PitchE	0.8	
P = Plain Grid, S = Staggered Grid	GridType	P	
F = Full Matrix, P = Perimeter, SD = Selectively Depopulated, TE = Thermally Enhanced	MatrixType	F	
Number of balls (vertical side)	Rows	10	
Number of balls (horizontal side)	Columns	10	
Maximum number of ball positions (Rows x Columns)	Nmax	100	
Number of actual balls present	PinCount	100	
Ball positions removed from matrix. Example: C5-H10,B6-B9,A1	DepopulateBalls	-	
Ball positions added back into depopulated matrix. Example: C8,D6-F9	RepopulateBalls	-	

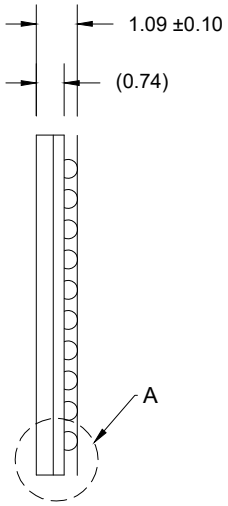
Recommended Land Pattern (NSMD Design)			
Description	**Dimension**	**Value (mm)**	**Diagram**
Diameter of pad. If specified this overrides the calculated value. This can be used to specify a manufacturer's recommended pad size.	X	0.365	
Solder Mask Expansion	S	0.05	

Package Outline Drawing

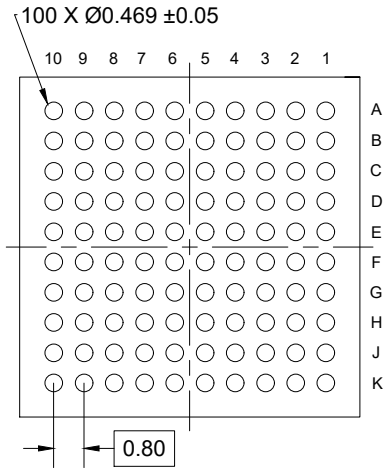
Package Code: BJG100
100-BGA 9.00 x 9.00 x 1.09 mm Body, 0.80 mm Pitch
PSC-4959-01, Revision: 01, Date Created: Mar 14, 2023



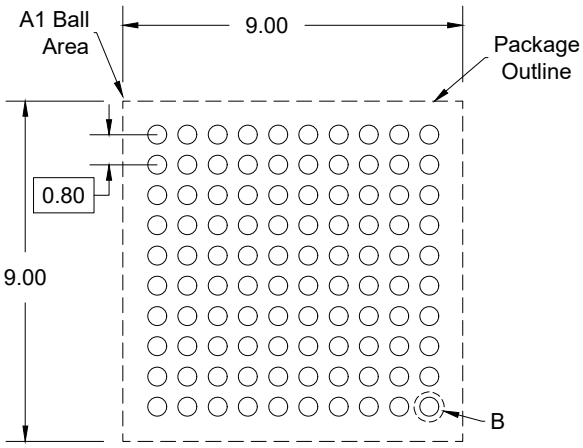
TOP VIEW



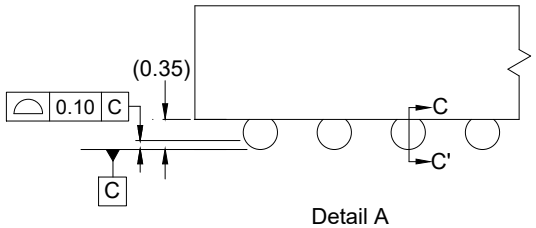
SIDE VIEW



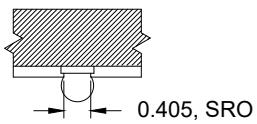
BOTTOM VIEW



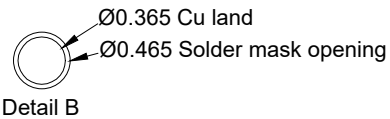
RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)



Detail A
(Rotated 90° CW)



Detail C - C'



Detail B

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.
5. Pre-reflow solderball diameter is Ø0.45 mm.

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