

RBA300N10EANS-3UA02

REXFET-1 N-Channel Power MOSFET

100V - 340A - 1.5mΩ

Description

Renesas TOLL technology features ultra compact, leadless designs for enhanced thermal performance, management, and reliability. Wettable Flank solution supports Better Reliability & Ease of Assembly. Renesas new split gate technology provide suitable for use in low RDS(on) and switching capability for high power & high-frequency application.

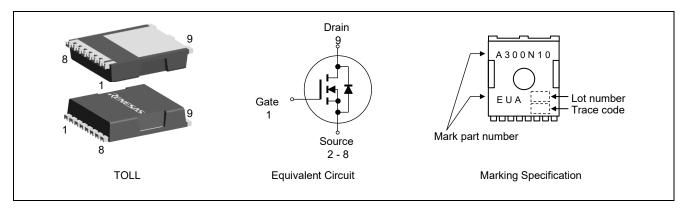
Features

- Standard level gate drive voltage: V_{GS(th)} = 2.0~4.0V
- Super Low on-state resistance: $R_{DS(on)} = 1.5 m\Omega$ Max.
- Low input capacitance
- Low thermal resistance
- AEC-Q101 qualified
- PPAP capable
- · Pb-free lead plating: RoHS compliant
- MSL1 classified according to IPC/JEDEC J-STD-020

Application

• Automotive: Small Traction (2-wheel, 3-wheel vehicle), 48V load, OBC, Charging station, LDC, etc.

Outline



Absolute Maximum Ratings

(Tj=25°C unless otherwise notice.)

Item	Symbol	Ratings	Unit
Drain to Source Voltage	V _{DSS}	100	V
Gate to Source Voltage	V _{GSS}	±20	V
Drain Current (DC)	I _{D(DC)} T _{c=25°C} Notes2,6	±340	A
Drain Current (DC)	ID(DC) Tc=100°C Notes2,6	±272	Α
Drain Current (Chip limitation)	ID(DC) Tc=25°C Notes2,6	±380	Α
Drain Current (pulse)	I _{D(pulse)} Notes1,3,6	±1360	А
Power Dissipation	P _D Notes1,6	468	W
Operating Junction Temperature	Tj	-55 to 175	°C
Storage Temperature	T _{stg}	-55 to 175	°C
Single Avalanche Current	I _{AS} Notes4	64	A
Single Avalanche Energy	Eas Notes4	409	mJ

Thermal Resistance

Item	Symbol	Max.	Unit
Junction to Case Thermal Resistance	R _{th(j-c)} Notes6	0.32	°C/W
Junction to Ambient Thermal Resistance	Rth(j-a) Notes5,6	40	°C/W

Electrical Characteristics

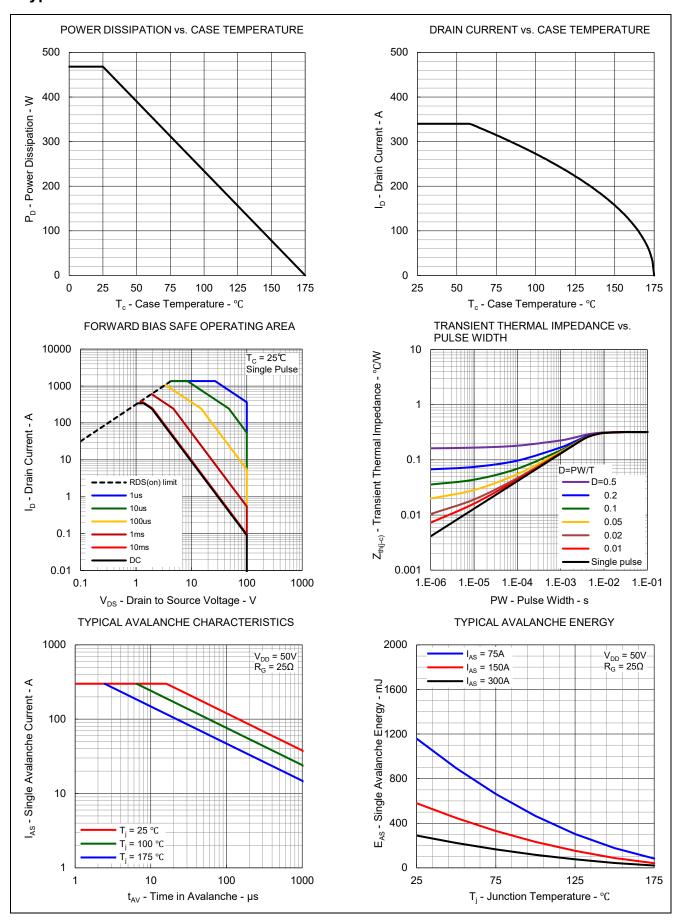
(T_j=25°C unless otherwise notice.)

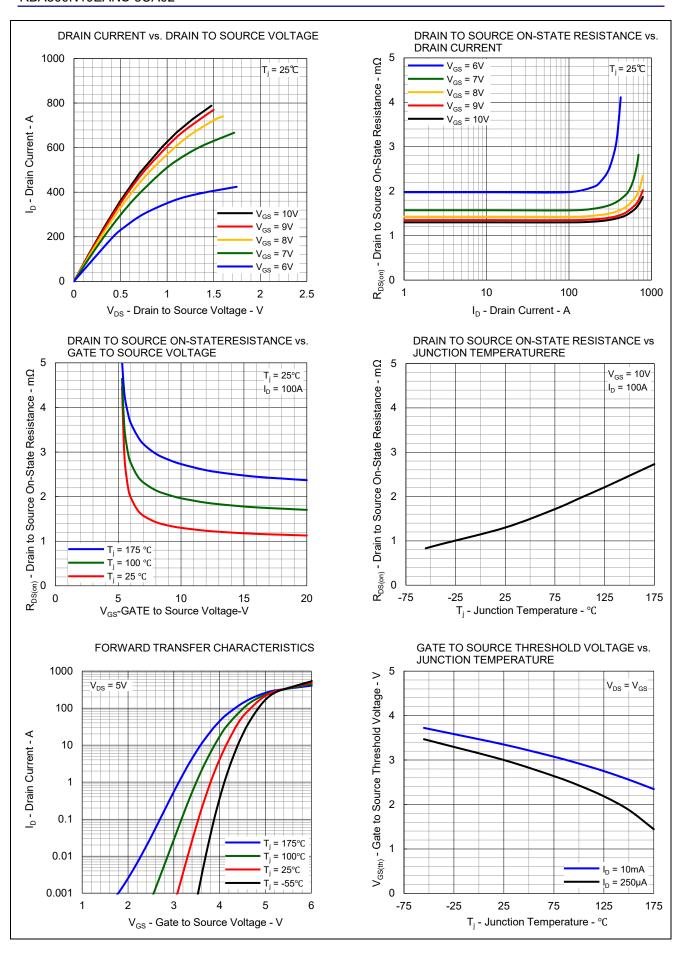
Item	Symbol	Min	Тур	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I _{DSS}	_	_	10	μA	V _{DS} = 100 V, V _{GS} = 0 V
Gate Leakage Current	I _{GSS}	_	_	±100	nA	V_{GS} = \pm 20 V , V_{DS} = 0 V
Gate to Source Threshold Voltage	$V_{GS(th)}$	2.0	_	4.0	V	V_{DS} = V_{GS} , I_D = 250 μ A
Drain to Source On-state Resistance	R _{DS(on)}	_	1.3	1.5	mΩ	V _G S = 10 V, I _D = 100 A
Input Capacitance	C _{iss}	_	13000	_	pF	V _{DS} = 50 V
Output Capacitance	C _{oss}	_	3300	_	pF	V _{GS} = 0 V
Reverse Transfer Capacitance	C _{rss}	_	80	_	pF	f = 100 kHz
Gate resistance	R_g	_	1.8	_	Ω	
Turn-on Delay Time	t _{d(on)}	_	75	_	ns	V _{DD} = 50 V
Rise Time	t _r	_	60	_	ns	I _D = 100 A
Turn-off Delay Time	t _{d(off)}	_	130	_	ns	V _{GS} = 10 V
Fall Time	t _f	_	55	_	ns	$R_G = 5 \Omega$
Total Gate Charge	Q_g	_	170	_	nC	V _{DD} = 50 V
Gate to Source Charge	Q_{gs}	_	75	_	nC	V _G s = 10 V
Gate to Drain Charge	Q_{gd}	_	30	_	nC	I _D = 100 A
Gate plateau voltage	V _{plateau}	_	5.4	_	V	
Output Charge	Q _{oss}	_	280	_	nC	V _{DD} = 50 V, V _{GS} = 0 V
Body Diode Forward Voltage	$V_{F(S-D)}$	_	0.85	1.5	V	I _F = 100 A, V _{GS} = 0 V
Reverse Recovery Time	t _{rr}	_	110	_	ns	I _F = 100 A, V _{GS} = 0 V
Reverse Recovery Charge	Q _{rr}	_	300	_	nC	di/dt = 100 A/μs

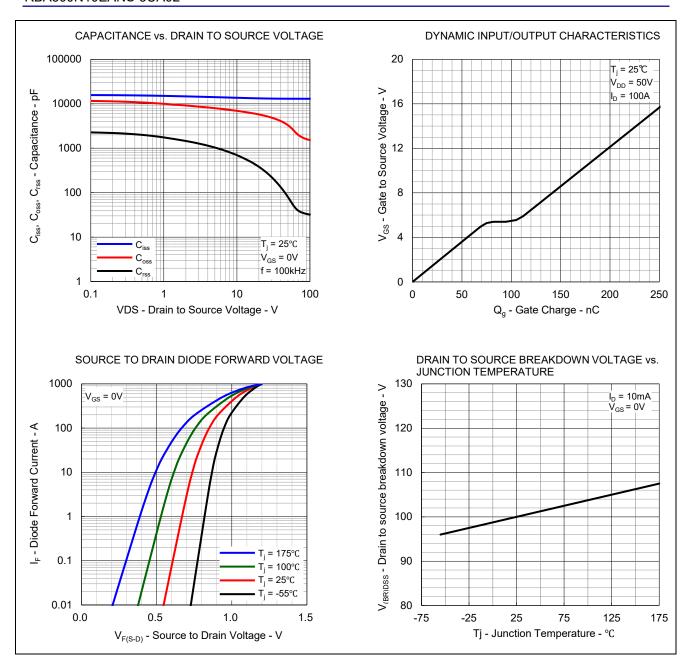
Notes 1. $T_c = 25$ °C

- 2. Value is limited by overall system design including PCB.
- 3. PW \leq 10 μ s
- 4. L = $100 \mu H$, V_{DD} = 50 V , R_G = $25 \ \Omega$
- 5. Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4. (2 oz Cu pad.)
- 6. Defined by design. Not subject to production test.

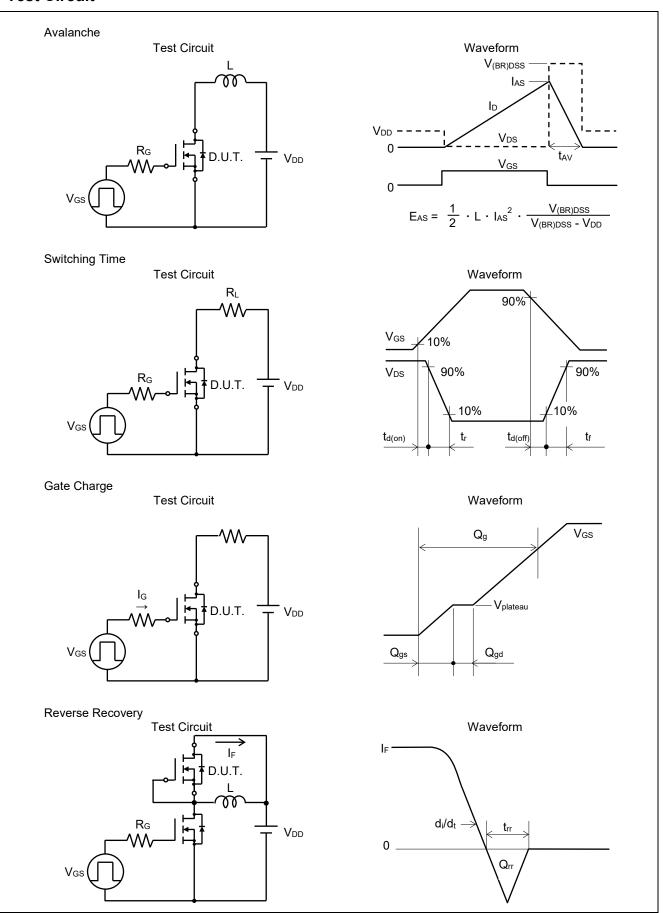
Typical Characteristics



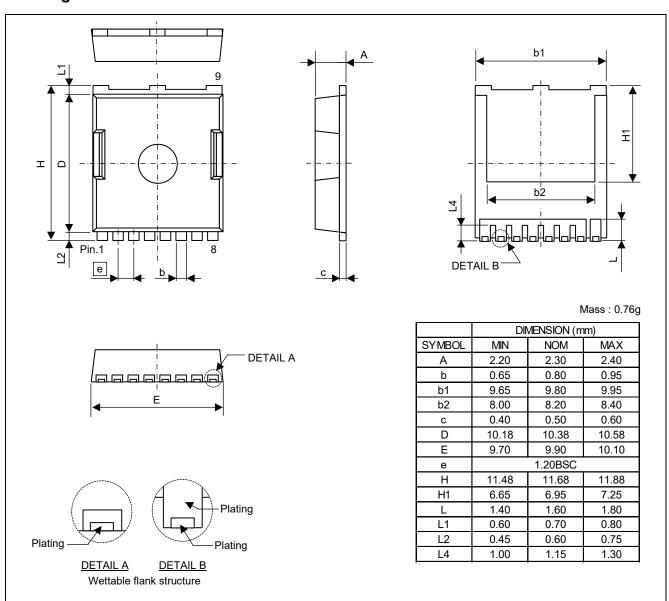




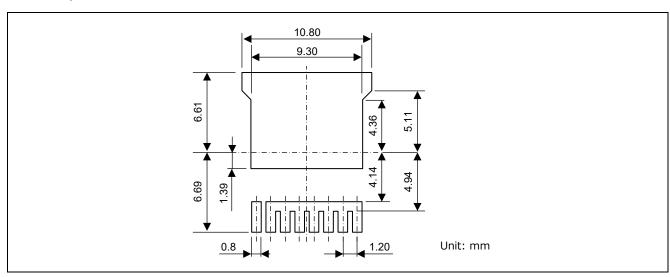
Test Circuit



Package Dimensions



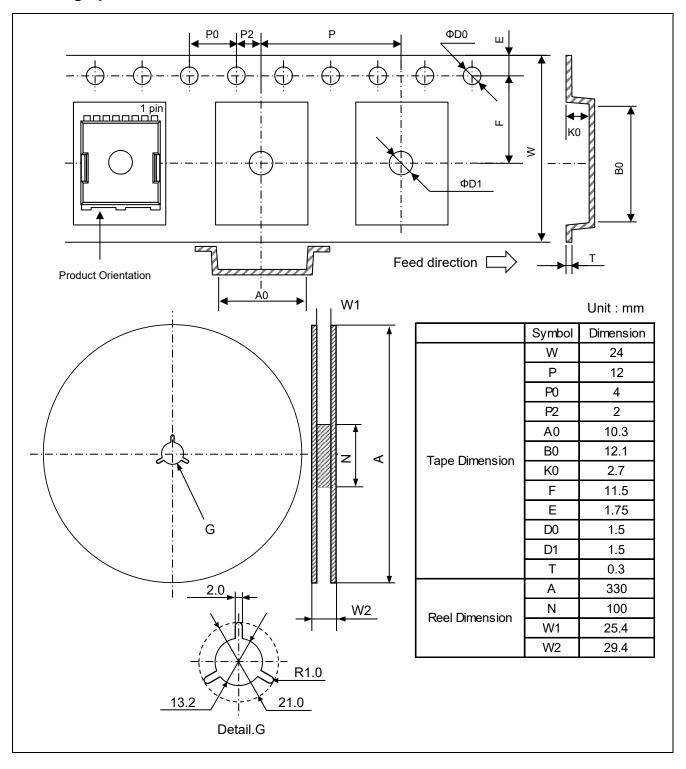
Mount pad



Ordering Information

Part No.	Packing	Quantity	
RBA300N10EANS-3UA02#GB0	Taping	2000pcs/reel	

Packing Specification



Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

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