RAA788000

Rogowski Coil Based Power-Line Current Sensor with Amplifier

The RAA788000 is a low-power, power-line current sensor for contactless AC current measurements in the range of 2A to 5000A. The device consists of an on-chip Rogowski coil, a buffer amplifier, and a signal amplifier.

From an alternating power-line current, the magnetic flux flows through the on-chip coil generating an electromotive force (EMF) that is amplified and filtered by a signal amplifier.

The amplifier output is typically fed into an analog-to-digital converter with a subsequent signal processor that calculates the current magnitude.

The RAA788000 operates from a single 2.7V to 3.6V supply. The device is available in a small 16 Ld TSSOP package and has an operation that is specified for the temperature range from -40°C to +105°C.

The RAA788000 is available in a 16 Ld thin shrink small outline package (TSSOP).

Features

- On-chip coil sensor
- Low noise density: E_n = 50nV/√Hz at 10Hz
- Low supply voltage: V_S = 2.7V to 3.6V
- Temperature range: -40°C to +105°C
- Small 16 Ld TSSOP package

Applications

- Power-line current measurements
- Watt meters

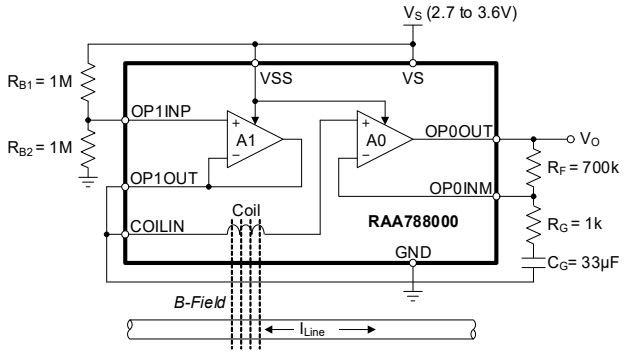


Figure 1. Typical Single-Current Sensor Application

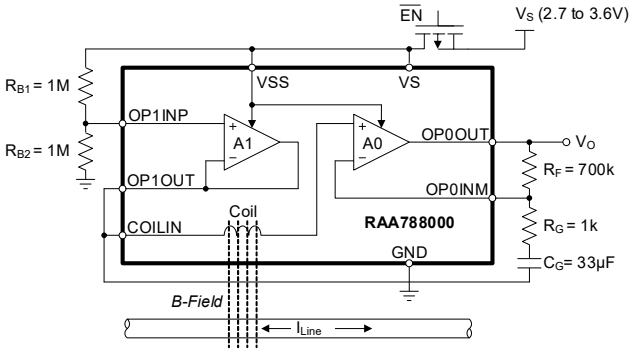


Figure 2. Typical Single-Current Sensor Application with Enable Function

Contents

1. Overview

1.1 Block Diagram

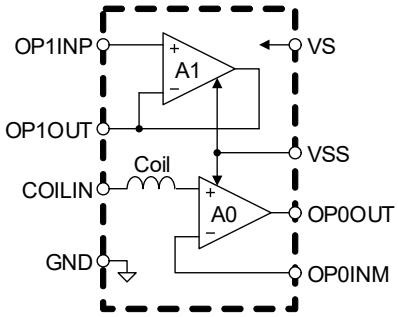
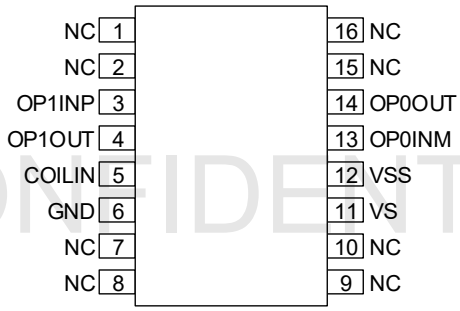


Figure 3. Block Diagram

2. Pin Information

2.1 Pin Assignments



Top View

2.2 Pin Descriptions

Pin Number	Pin Name	Description
1, 2, 7, 8, 9, 10, 15, 16	NC	Not connected internally.
3	OP1INP	Buffer amplifier (A1) non-inverting input.
4	OP1OUT	Buffer amplifier (A1) output.
5	COILIN	Coil bias voltage input.
6	GND	Current sensor IC ground.
11	VS	Current sensor IC positive supply voltage.
12	VSS	Positive supply voltage for both amplifiers. Connect the VSS pin to the VS pin externally.
13	OP0INM	Current sense amplifier (A0) inverting input.
14	OP0OUT	Current sense amplifier (A0) output.

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
Positive Supply Voltage, V_S, V_{SS}	-0.3	+4.6	V
Negative Supply Voltage, GND	-0.3	+0.3	V
Input Voltage, V_I (OP1INP, COILIN, OP0INM)	-0.3	V_S + 0.3	V
Output Voltage, V_O, (OP0OUT, OP1OUT)	-0.3	V_S + 0.3	V
High-Level Output Current, I_{OH}, (OP0OUT, OP1OUT)	-	-0.3	mA
Low-Level Output Current, I_{OL}, (OP0OUT, OP1OUT)	-	+0.3	mA
Human Body Model (Tested per JS-001-2017)	-	2000	V
Charged Device Model (Tested per JS-002-2018)	-	750	V

3.2 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Supply Voltage, V_S	2.7	3.6	V
Ambient Temperature	-40	+105	°C

3.3 Thermal Specifications

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	16 Ld TSSOP Package	θ_{JA}[1]	Junction to air	98	°C/W
		θ_{JC}[2]	Junction to case	30	°C/W

1. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board in free air. See TB379.
2. For θ_{JC}, the case temperature location is taken at the package top center.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature	-	+150	°C
Maximum Storage Temperature Range	-65	+150	°C
Pb-Free Reflow Profile	See TB493.		

3.4 Electrical Specifications

V_S = 3.3V, V_{IN} = V_S/2, T_A = 25°C, unless otherwise specified.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Offset Voltage	VOS_{A0}	T_A = 25°C, V_{IN} = 0.25V	-	-	±3.1	mV
	VOS_{A1}		-	-	±3.1	
Input Offset Voltage Drift[1]	dV_{OS}/dT	V_S = 3.3 to 3.6V, V_{IN} = 0.25V to V_S - 0.6V	-	4	9.8	µV/°C
Input Bias Current	I_B	V_S = 3.6V	-	-	1	nA
Input Voltage Range	V_{IN}	-	0	-	V_S	V
Output Voltage Swing, Low	V_{OL}	V_{IN} = GND, I_{LOAD} = +0.3mA	-	0.01	0.09	V
Output Voltage Swing, High	V_{OH}	V_{IN} = V_S, I_{LOAD} = -0.3mA	V_S - 0.16	V_S - 0.04	-	V
Open-Loop Gain[1]	A_{OL}	-	-	120	-	dB
Gain Bandwidth	GBW	-	-	480	-	kHz
Phase Margin[1]	Φ_M	-	-	57	-	deg
Slew Rate	SR	V_{IN} = GND to V_S	-	0.27	-	V/µs
Input Voltage Noise[1]	E_n	f = 0.1 to 10Hz	-	1.6	-	μV_{P-P}
Input Voltage Noise Density[1]	e_n	f = 1kHz	-	50	-	nV/√Hz
Common-mode Rejection Ratio	CMRR	f = 60Hz	-	101	-	dB
Power Supply Rejection Ratio	PSRR	f = 60Hz	-	86	-	dB
DC Characteristics						
Supply Current	I_{DD}	V_S = V_{SS} = 2.7 to 3.6V	-	0.4	0.5	mA

1. Limits established by characterization and are not production tested.

4. Typical Performance Graphs

V_S = 3.3V, V_{REF} = V_S/2, T_A = 25°C, unless specified otherwise. All trendlines applied are linear equations.

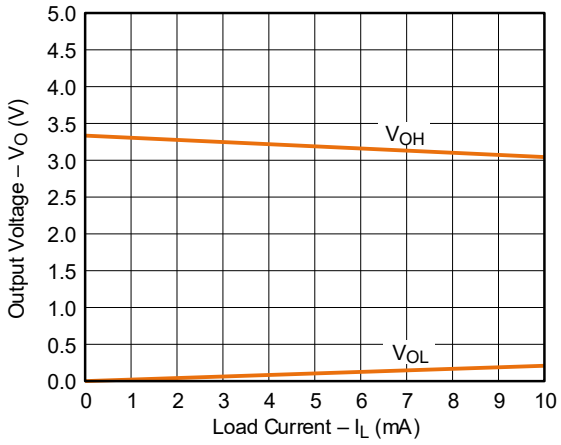


Figure 4. Output Voltage vs Load Current

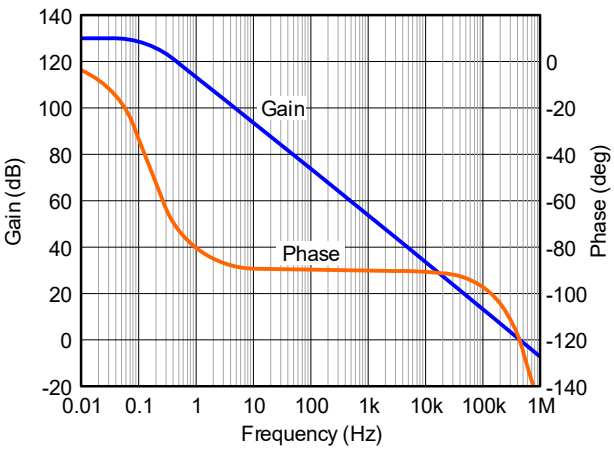


Figure 5. Open-Loop Gain and Phase vs Frequency

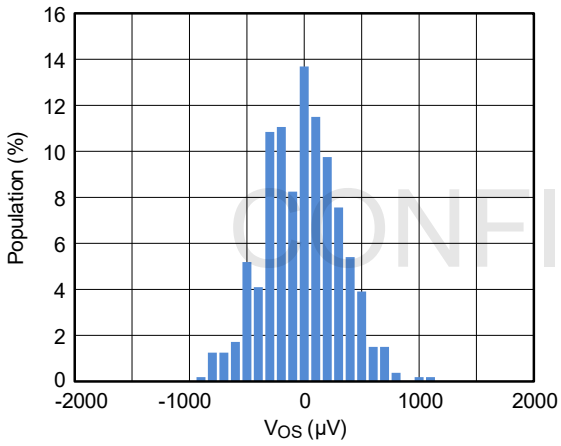


Figure 6. Offset Voltage Histogram

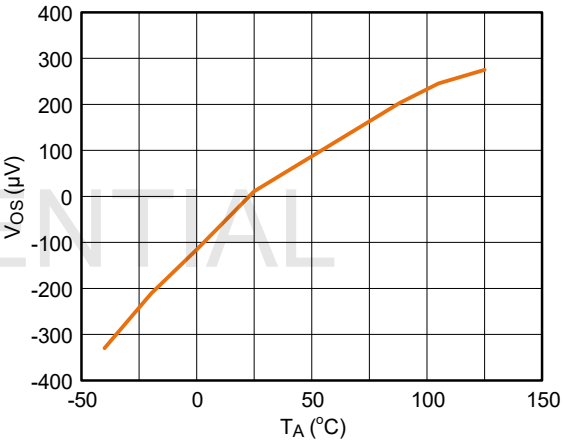


Figure 7. Offset Voltage vs Temperature

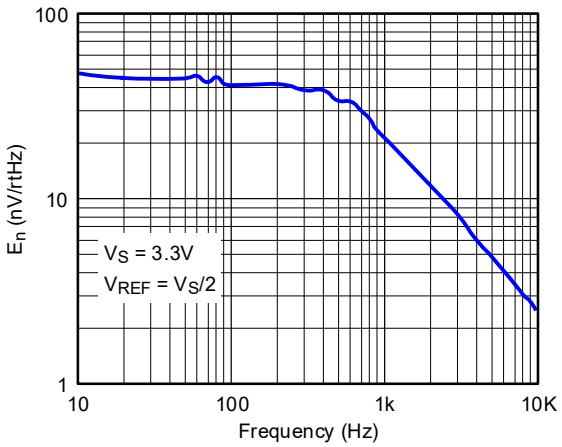


Figure 8. Input Voltage Noise Density vs Frequency

V_S = 3.3V, V_{REF} = 0.25V, G_{SE} = 101, G_{DIFF} = 201, T_A = 25°C, Cable = 2-AWG, Distance from Cable to IC = 4mm, unless specified otherwise. All trendlines applied are linear equations. (*Note*: For opposite topology details, see the *RTKA788000DE0000BU Evaluation Board Manual*.)

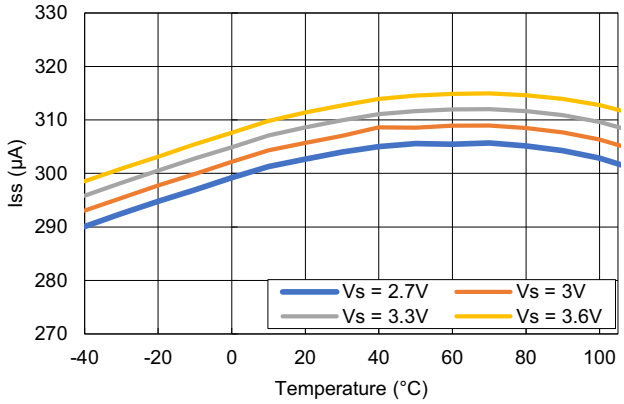


Figure 9. Supply Current vs Ambient Temperature, Topology = Single

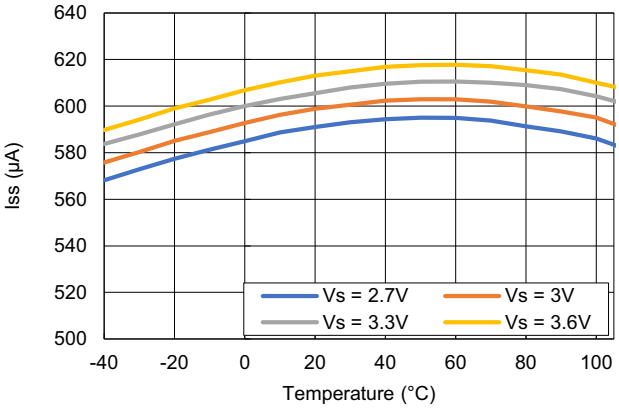


Figure 10. Supply Current vs Ambient Temperature, Topology = Stacked

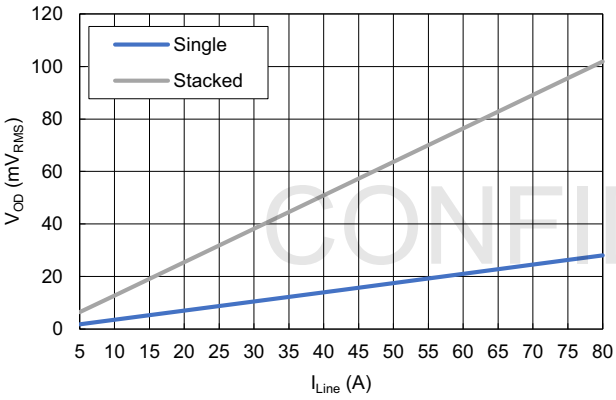


Figure 11. Output Voltage vs Line Current I_{LOAD} = 0A

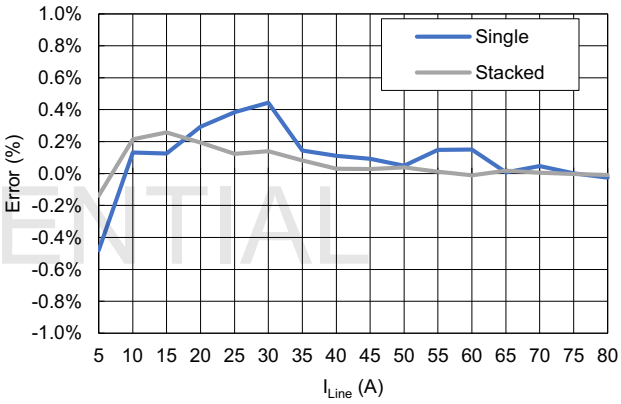


Figure 12. Trendline Error vs Line Current I_{LOAD} = 0A

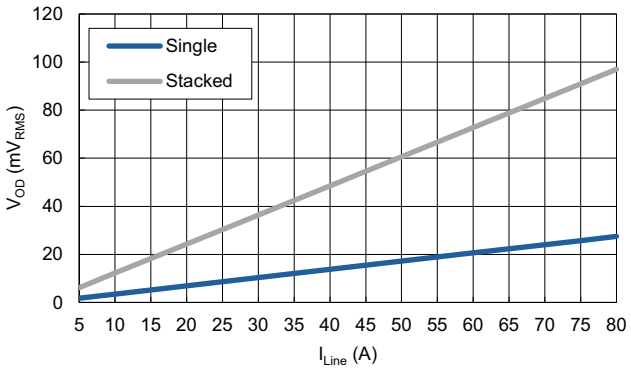


Figure 13. Output Voltage vs Line Current I_{LOAD} = 300µA

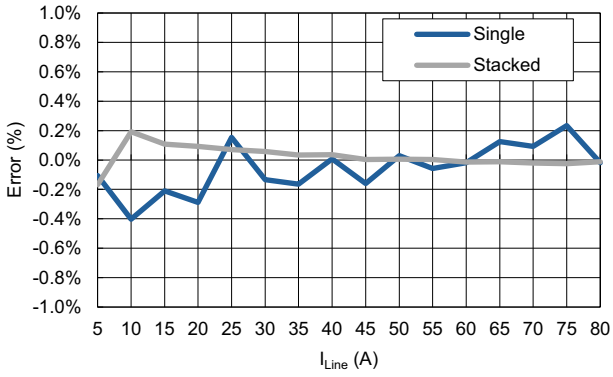


Figure 14. Trendline Error vs Line Current I_{LOAD} = 300µA

V_S = 3.3V, V_{REF} = 0.25V, G_{SE} = 101, G_{DIFF} = 201, T_A = 25°C, Cable = 2-AWG, Distance from Cable to IC = 4mm, unless specified otherwise. All trendlines applied are linear equations. (*Note*: For opposite topology details, see the *RTKA788000DE0000BU Evaluation Board Manual*.) (Cont.)

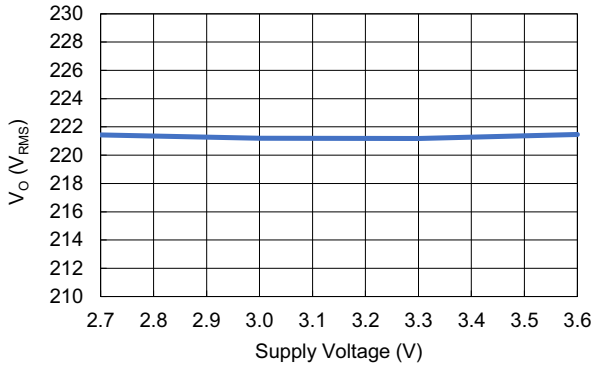


Figure 15. Output Voltage vs Supply Voltage
I_{LINE} = 50A, Topology = Single

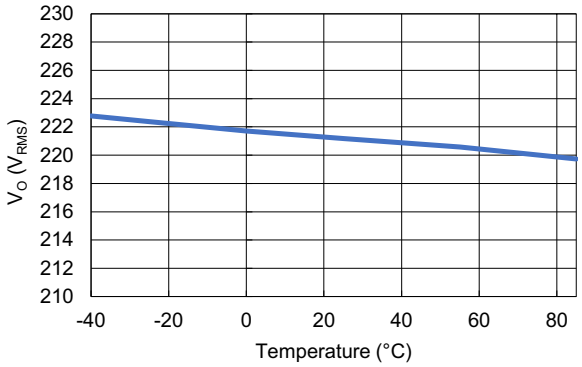


Figure 16. Output Voltage vs Ambient Temperature
I_{LINE} = 50A, Topology = Single

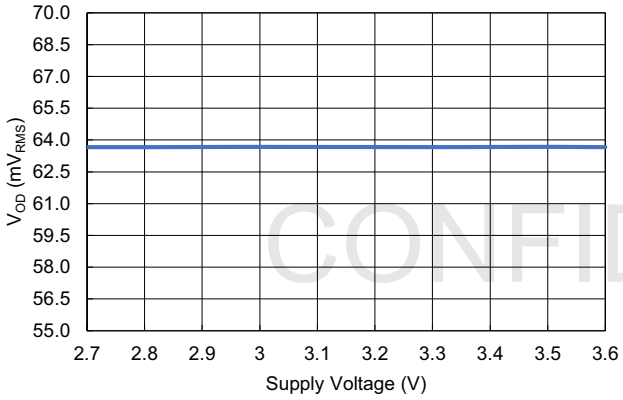


Figure 17. Output Voltage vs Supply Voltage
I_{LINE} = 50A, Topology = Stacked

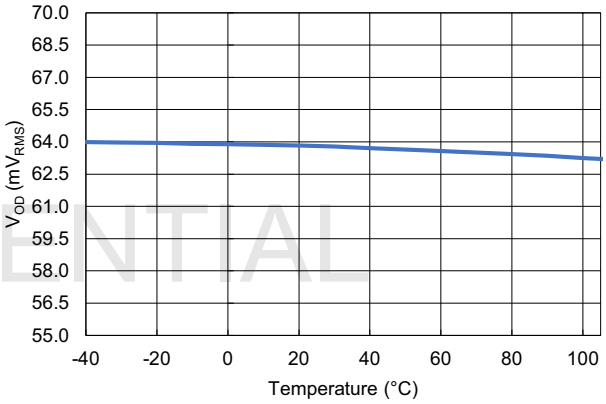


Figure 18. Output Voltage vs Ambient Temperature
I_{LINE} = 50A, Topology = Stacked

5. Device Information

The RAA788000 consists of an on-chip coil for current sensing, a buffer amplifier to bias the coil, and a signal amplifier to boost the electromotive force (EMF) of the coil (Figure 19).

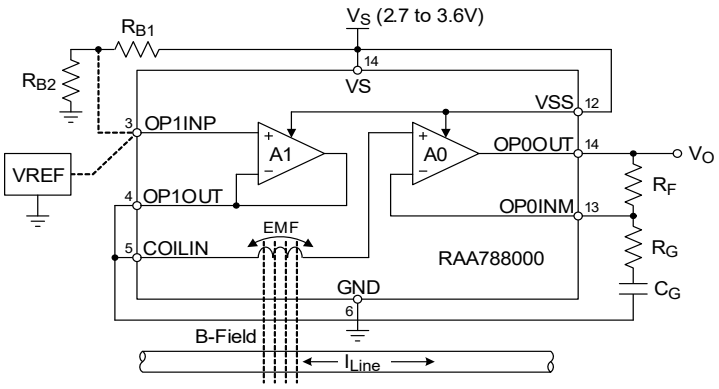


Figure 19. Single-Sensor Connections

5.1 Amplifier: A1

Amplifier, A1, is a unity-gain buffer, whose input (OP1INP) can be connected either to a low-impedance reference voltage source, or to a high-impedance voltage divider that derives the reference voltage from the positive supply, V_S. Its low-impedance output is directly connected to the device coil input, COILIN.

5.2 Amplifier: A0

Amplifier, A0, is a signal amplifier, operating in the non-inverting configuration. The non-inverting input is internally connected to the coil. The gain of this amplifier stage is set using the ratio of feedback resistor to gain resistor: $G = 1 + R_F/R_G$.

5.3 On-Chip Coil

The AC current of an adjacent power line creates a magnetic field that penetrates the on-chip coil. The coil generates a voltage (V_{COIL}) that is amplified by amplifier, A0. In Figure 20, assuming that the distance from the power line is r (m) and the current is I (A), the magnetic field H (A/m) generated by the current in the power line is as shown in Equation 1.

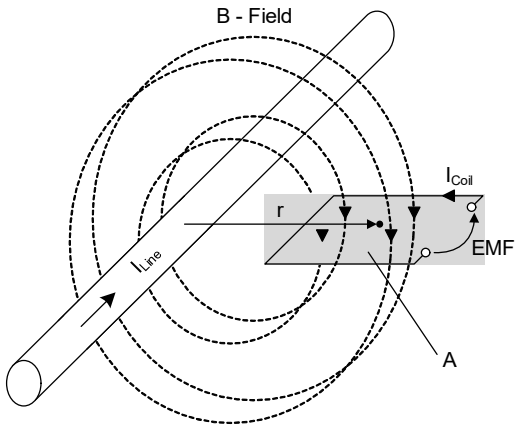


Figure 20. Line Current-to-EMF Conversion

(EQ. 1) $$H = \frac{I}{2\pi \times r}$$

The inductive electromotive force (V) generated by the coil closing the loop of the magnetic flux is in proportion to the change in the magnetic flux Φ (Wb) per unit time as follows.

(EQ. 2) $$V_{coil} = -N\left(\frac{d\phi}{dt}\right) = -N\frac{d}{dt}(BA) = -N\frac{d}{dt}(\mu HA) = -N\frac{d}{dt}\left(\frac{\mu IA}{2\pi r}\right) = -\frac{\mu NA}{2\pi r}\left(\frac{dI}{dt}\right)$$

Assuming the current through the power line

(EQ. 3) $$I = I_{peak} \times \sin(2\pi ft)$$

Then,

(EQ. 4) $$V_{coil} = -\frac{\mu NA}{2\pi r} \times \frac{d}{dt}\left((I_{peak} \times \sin(2\pi ft)\right) = -N \times I_{peak} \times \frac{\mu Af}{r}\cos(2\pi ft)\right)$$

So,

(EQ. 5) $$V_{coil\_peak} = N \times I_{peak} \times \frac{\mu Af}{r}$$

or

(EQ. 6) $$V_{coil\_RMS} = N \times I_{RMS} \times \frac{\mu Af}{r}$$

Here, N is the number of windings in the coil, μ (H/m) is the magnetic permeability, A (m^2) is the area of the coil enclosing the magnetic flux, f is the frequency of the line current, and r is the distance between the conductor and coil center.

6. Application Information

6.1 Sensitivity versus Measurement Topology

Current measurements with the RAA788000 allows for the use of various measurement topologies.

A single-sensor application is usually enough to measure line currents ≥5A. For lower currents however, the use of two sensors is recommended. Combining their individual signal amplifiers to a single differential amplifier stage increases measurement sensitivity by a factor of four (see Amplifier Configurations). Evidently, this requires a differential input signal in the form of coil voltages with equal magnitude but opposite polarity. In other words, there must be a 180° phase shift between the two coil EMFs.

To determine the coil positions that produce this phase shift, as well as those that do not, we apply the right-hand and left-hand rules (Figure 21).

The right-hand rule states: when grabbing a conductor with the right hand, the thumb points into the direction of the current flow, and the conductor enclosing fingers indicate the direction of the magnetic field lines.

For magnetic field lines penetrating a simple loop coil, the left-hand rule applies: when enclosing a magnetic field with the left hand, the thumb points into the direction of the field lines, and the field enclosing fingers indicate the direction of the coil current.

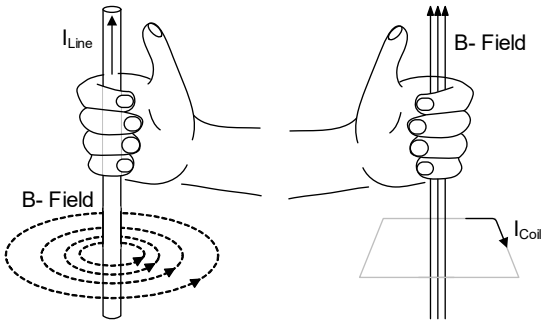


Figure 21. Right-Hand and Left-Hand Rules

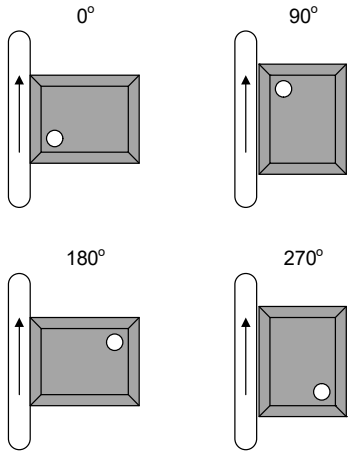


Figure 22. Coil Positions Causing No Phase Shift

Therefore, turning a single-current sensor around its center axis, produces no change in EMF phase as the magnetic field lines always penetrate the coil from the same direction (Figure 22). The same is true for placing two current sensors side-by-side. There is no difference in EMF phase between the two as the magnetic field penetrates both coils from the same direction.

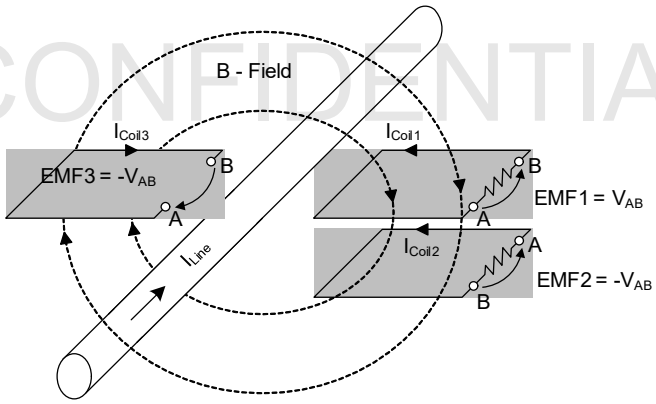


Figure 23. Coil Positions Causing 180° Phase Shift

The only way to cause a 180° phase shift is by placing the 2nd sensor such that the magnetic field lines penetrate its coil from the opposite direction. This is accomplished by either flipping the 2nd coil upside down or placing it at the opposite side of the current carrying conductor (Figure 23). In both cases, the currents in coil 2 and coil 3 change direction, which causes the resulting EMF2 and EMF3 to experience a 180° phase shift in comparison to EMF1. This leads to the stacked and opposite-sensor topologies in Figure 25 and Figure 26.

Therefore, the three measurement topologies feasible with the RAA788000 are the single-sensor, stacked-sensor, and opposite-sensor topologies.

The single-sensor topology (Figure 24) has the lowest sensitivity and is recommended for measuring currents above 5A. Its design is simple and low in cost and has the benefit of being easily adjustable to the center height of large cables.

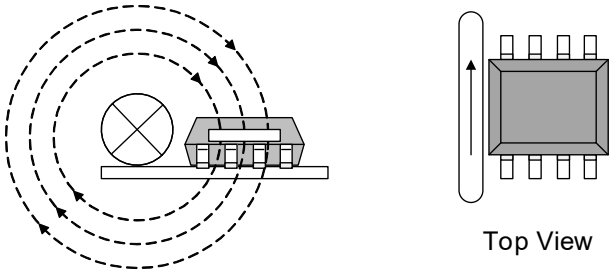


Figure 24. Single Sensor Topology

The stacked-sensor topology (Figure 25) has high sensitivity and great linearity. Here, two sensors are placed on the top and the bottom of the PCB to generate coil voltages of opposite polarity. Their individual output amplifiers are combined to one different signal amplifier. This approach creates twice the coil voltage and twice the signal gain, therefore, four-times the sensitivity of a single sensor. It is the preferred solution for measuring currents down to 2A in large cables, as it can be easily fixed to mid cable height. The increased design complexity makes it slightly costlier.

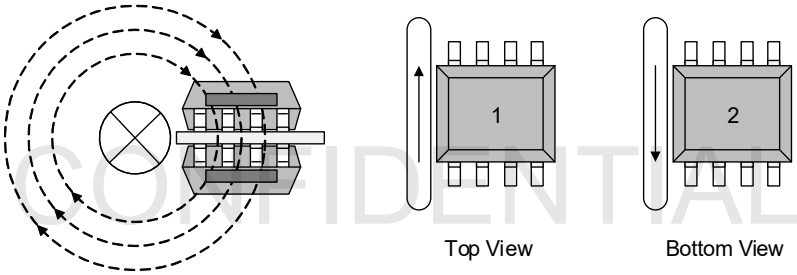


Figure 25. Stacked Sensor Topology

The opposite-sensor topology (Figure 26) is equal in sensitivity, linearity, and current measurement range to the stacked topology. Adjusting the sensors to mid cable height is cumbersome, therefore, this topology is better suited for smaller cable diameters, where both sensors and cable share the same PCB platform.

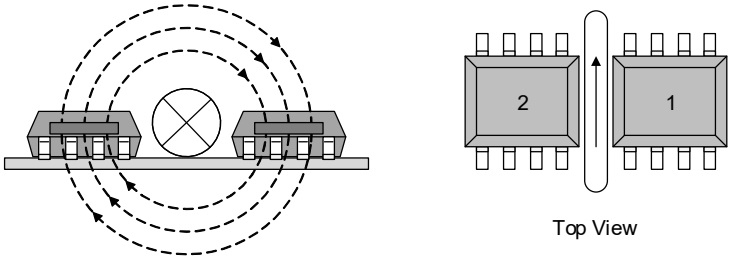


Figure 26. Opposite Sensor Topology

6.2 Amplifier Configurations

The single-sensor topology uses a single non-inverting amplifier whose AC or passband gain is:

(EQ. 7) $G_{PB(SE)} = 1 + R_F / R_G$

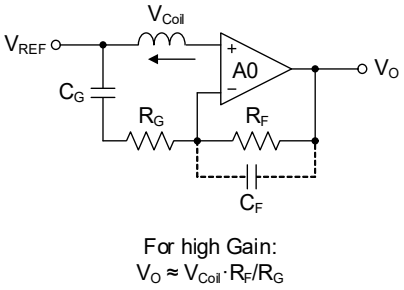


Figure 27. Singe-Ended Amplifier

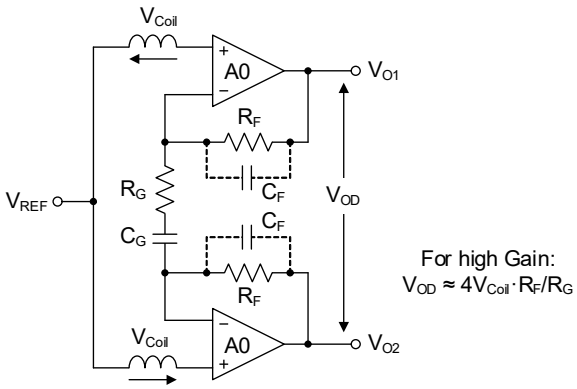


Figure 28. Differential Amplifier

The other two topologies (Stacked, Opposite) use a differential amplifier design with a passband gain of:

(EQ. 8) $G_{PB(DIF)} = 1 + 2R_F/R_G$

Because both, input voltage and passband gain of the differential amplifier are twice that of a single-ended amplifier, the overall sensitivity is four times that of the single amplifier. Therefore, when measuring line currents below 5A, a two-sensor topology is highly recommended.

6.3 Band-Pass Filtering

Both amplifier designs (Figure 27 and Figure 28) use a DC blocking capacitor, C_G, to prevent the input offset voltages from being amplified. Therefore, at DC, both amplifiers operate at unity-gain. C_G in combination with R_G forms a high-pass filter (Figure 29) with a corner frequency of:

(EQ. 9) $f_{c(HP)} = 1/(2\pi R_G C_G)$

Depending on the gain factor, a noise reduction capacitor, C_F, might be added in parallel to R_F. C_F and R_F form a low-pass filter with a corner frequency of:

(EQ. 10) $f_{c(LP)} = 1/(2\pi R_F C_F)$

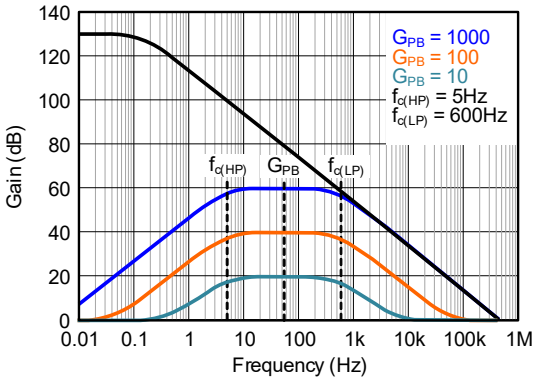


Figure 29. Frequency Responses for Various Gain Settings

To minimize phase errors, set $f_{c(HP)}$ to 1/10th of the lowest signal frequency (50Hz), and $f_{c(LP)}$ to 10-times the highest signal frequency (60Hz). This makes $f_{c(HP)}$ = 5Hz and $f_{c(LP)}$ = 600Hz.

6.4 Suggested Circuit Design Procedure

- For high current measurements in the 10A to 1kA range, use a single sensor. For currents in the 0.1A to 100A range use a dual sensor approach. As previously mentioned, for small cable diameters, Renesas recommends using the opposite-sensor topology, for larger cable diameters, Renesas recommends using the stacked topology.
- Fix the current sensor PCB to the cable using zip-ties (Figure 30). Ensure the sensors are placed as close as possible to the cable.

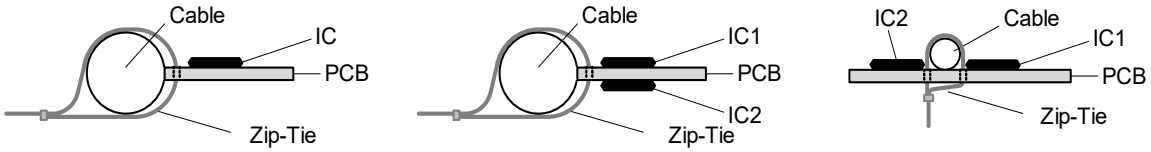


Figure 30. Sensor PCB Fixtures for Single-, Stacked-, and Opposite Sensor Topologies Cables

- For highest noise immunity, run the RAA788000 at 3.6V to get maximum dynamic output swing. To match V_{OD} to the input range of a subsequent ADC, perform any necessary signal attenuation at the ADC input, not at the amplifier output.
- Making $f_{c(HP)} \approx 5Hz$, requires large capacitors. Use R_G = 1kΩ or 10kΩ to limit the capacitor values to C_G = 33µF or 3.3µF, respectively.
- Then calculate R_F using Equation 11:

(EQ. 11) $$R_F = R_G \times \frac{G_{PB(DIF)} - 1}{2}$$

- For low-gain circuits (G_{Diff} = 10), the total output noise can be reduced by up to 60% when making CF:

(EQ. 12) $$C_F = \frac{1}{2\pi \times f_{c(LP)} \times R_F}$$

- For medium-gains (G_{Diff} = 100), noise reduction through C_F can still be 30%. However, the loop gain at 600Hz is reduced, therefore, lowering $f_{c(LP)}$. To maintain $f_{c(LP)}$ at 600Hz, calculates C_F with:

(EQ. 13) $$C_F = \frac{1}{2.25\pi \times f_{c(LP)} \times R_F}$$

- For high-gains (G_{Diff} = 1000), C_F is not required as the low-pass filtering is performed by the open-loop gain of the amplifier.

6.5 Performance Evaluation Circuits

Figure 31 and Figure 32 depict the single and differential amplifier circuits used to evaluate the typical performance curves in this datasheet. A single 3.3V supply powers the circuits. Both amplifiers A_1 and A_0 get positive supply voltage from the VSS pin. Connect the VSS pin to the VS pin for all IC configurations. The 1M bias resistors, R_B, set the reference voltage at the coil inputs to 1.65V. With R_F = 700kΩ, R_G = 1kΩ, and C_G = 33µF, the passband gain is set to G_{SE} = 701V/V for the single amplifier and G_{Diff} = 1401V/V for the differential amplifier. The high-pass corner frequency is set to $f_{c(HP)}$ = 5Hz for both amplifier circuits.

Figure 33 and Figure 34 show application circuits requiring an Enable function. The inverse of the enable signal is applied to the gate of the P-type MOSFET. When EN goes low, the P-type MOSFET turns off, which pulls down the VS and VSS pins of the IC to 0V, disabling the part.

In Figure 35 and Figure 36, the IC supply voltage is provided by the digital output pin of a MCU. The part can be enabled or disabled by toggling the MCU output pin high and low. Use Level shifters in case the logic high of the MCU pin is outside the range of 2.7V to 3.6V.

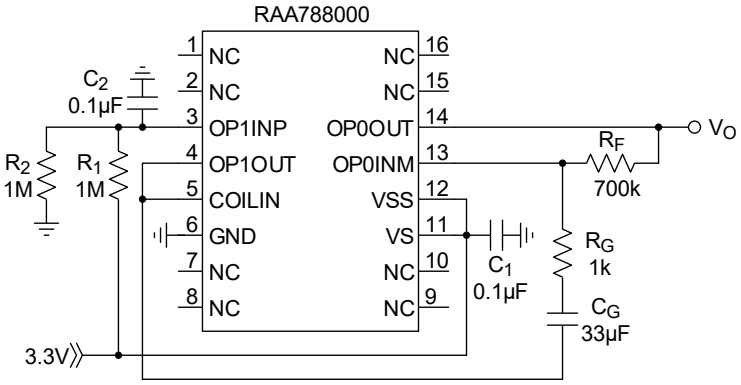


Figure 31. Single-Ended Amplifier Circuit for Performance Evaluation

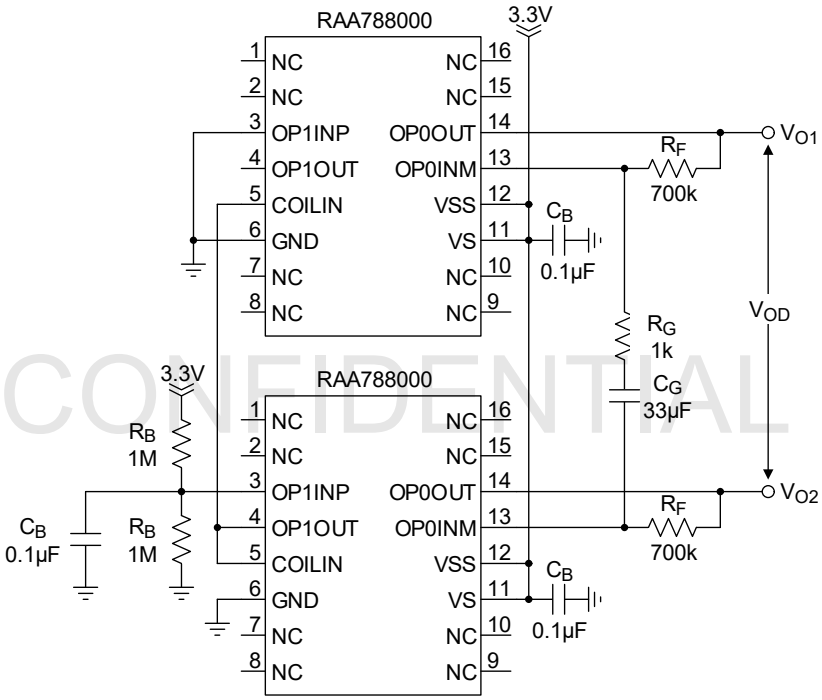


Figure 32. Differential Amplifier Circuit for Performance Evaluation

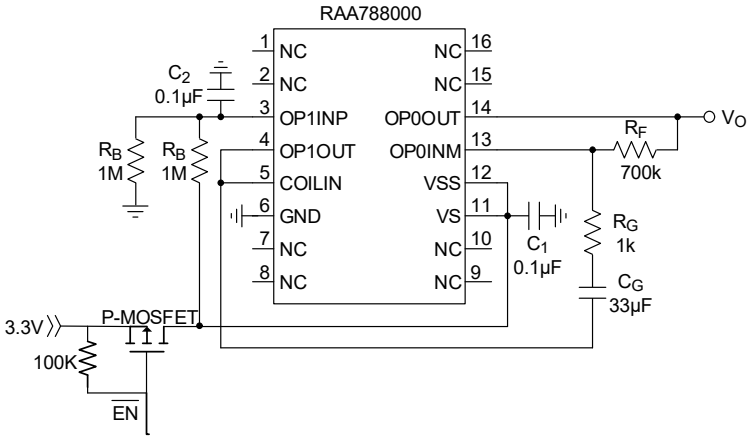


Figure 33. Single-Ended Amplifier Circuit with Enable function for Performance Evaluation

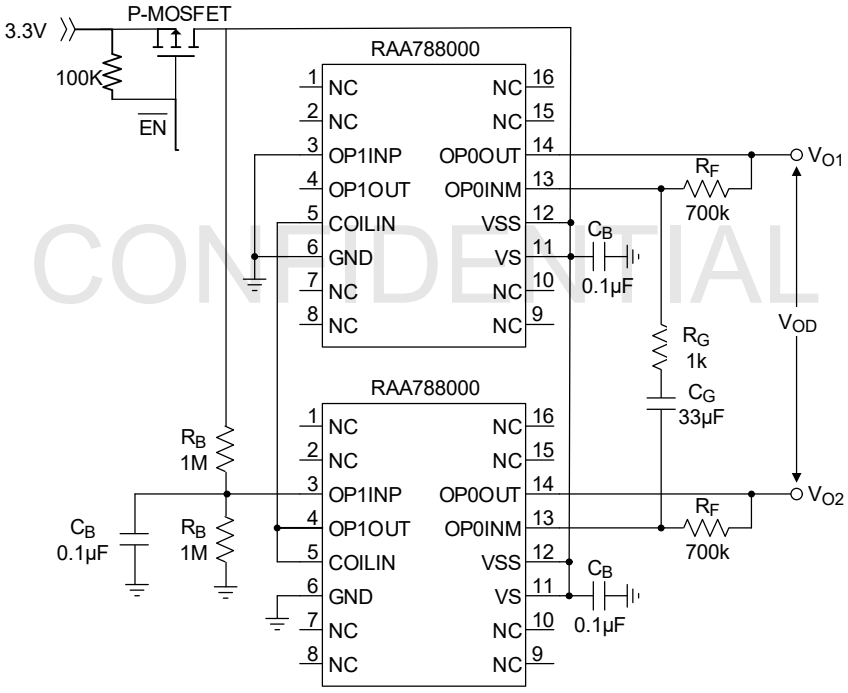


Figure 34. Differential Amplifier Circuit with Enable function for Performance Evaluation

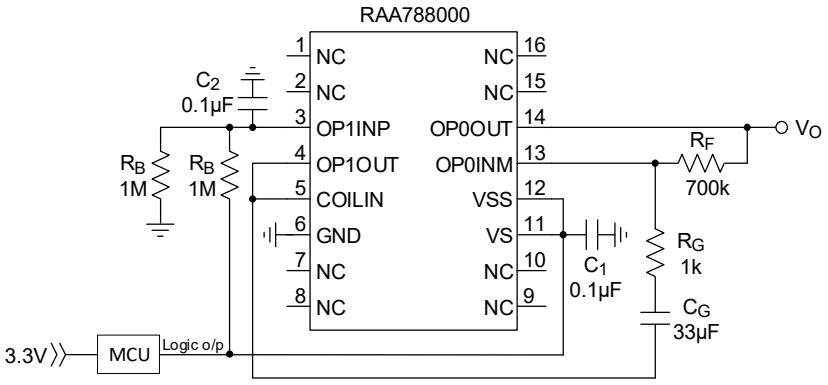


Figure 35. Single-Ended Amplifier Circuit with Enable function using MCU

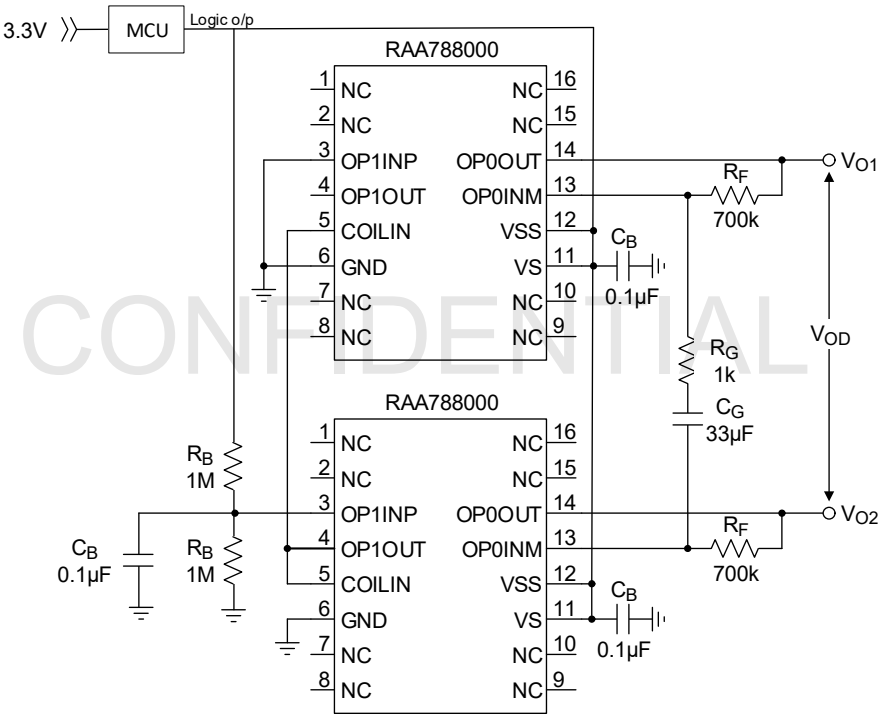
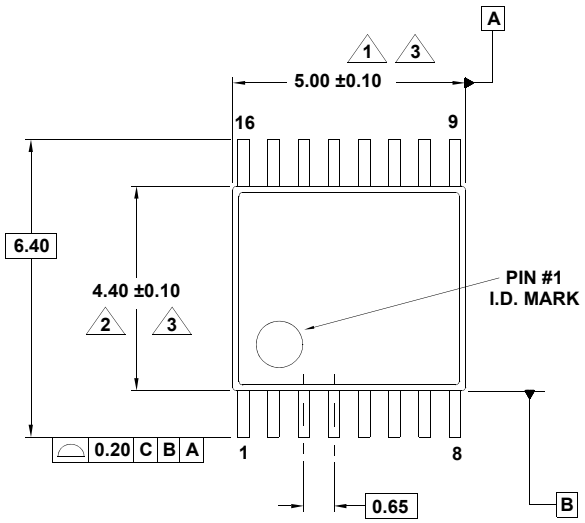


Figure 36. Differential Amplifier Circuit with Enable Function using MCU

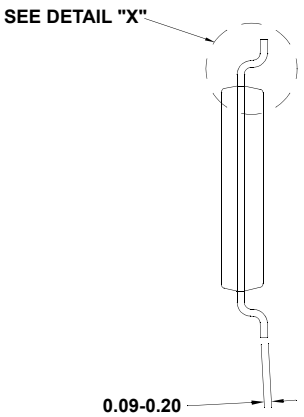
7. Package Outline Drawing

For the most recent package outline drawing, see M16.173.

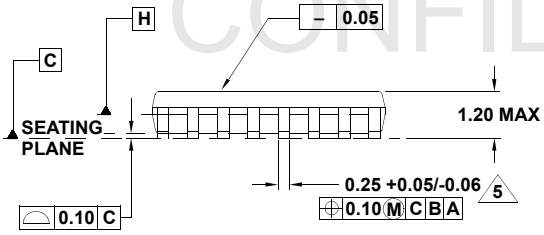
M16.173
16 Lead Thin Shrink Small Outline Package (TSSOP)
Rev 2, 5/10



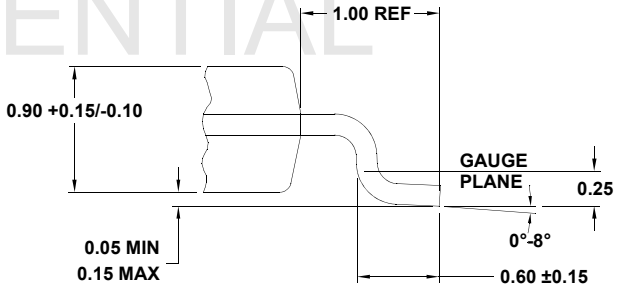
TOP VIEW



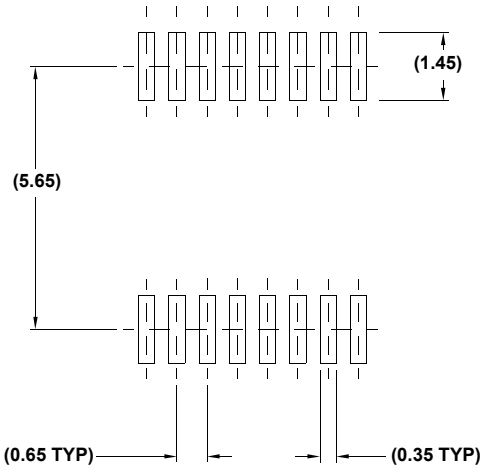
END VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
3. Dimensions are measured at datum plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Dimension does not include dambar protrusion. Allowable protrusion shall be 0.08mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.
6. Dimension in ( ) are for reference only.
7. Conforms to JEDEC MO-153.

8. Ordering Information

Part Number[1][2]	Part Marking	Package Description (RoHS Compliant)	Pkg. Dwg #	Carrier Type[3]	Temp. Range
RAA788000GSP#HA0	788000	16 Ld TSSOP	M16.173	Reel, 2.5k	-40 to +105°C
RTKA788000DE0000BU	Opposite Sensor Topology Evaluation Board				
RTKA788000DE0010BU	Stacked Sensor Topology Evaluation Board				

1. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. For the Moisture Sensitivity Level (MSL), see the RAA788000 product page. For more information about MSL, see TB363.
3. See TB347 for details about reel specifications.

9. Revision History

Revision	Date	Description
1.03	Jun 6, 2024	Updated description on page 1. Updated On-Chip Coil section.
1.02	May 9, 2024	Updated Figures 1 and 2. Updated Figures 9 to 18. Removed Figures 19 and 20. Updated section 5.3 On-Chip Coil. Removed Equation 1 and Figures 22 and 23. Updated Ordering Information.
1.01	Jun 7, 2023	Updated the temperature range throughout document. Updated Pin Assignments and Pin Description for pin 12. Added Figures 2, 36-39. Updated Figures 1, 3, 9, 10, 34, and 35 Moved ESD information to abs max section. Updated Thermal Information table formatting. Updated the following in the Electrical Specifications section: ▪ Updated the Input Offset Voltage maximum specs from ±10mV to 3.1mV. ▪ Changed Low level output voltage parameter name to Output voltage Swing, Low. Same with high level output voltage. ▪ V_{OH} min and typical values changed. ▪ Removed the following specs from the EC table: EN Pin Low Level and High Level Input Voltage. ▪ Supply current test condition changed and data is only for one test condition. Updated the Performance Evaluation Circuits section.
1.00	Oct 14, 2022	Initial release.

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