RAA489255

3-5 Cell Battery Front End

Description

The RAA489255 IC is a 3-5 cell battery monitor with battery health monitoring for packs in the typical configuration with MCU control.

The RAA489255 measures pack voltage, cell voltage, external temperature, and internal temperature per serial instructions from the controller. The RAA489255 has system and internal checks to monitor the health of the part and the state of the system.

The part has an I^2C with CRC interface to reliably communicate to the required MCU.

The device has six open-drain high voltage GPIOs that are capable of driving LEDs or fuse blowing.

The RAA489255 current consumption is low with an average Idle current of 85µA. The low current consumption maximizes the storage and discharge life of a battery.

The RAA489255 is offered in an efficient 32-pin 4mm×4mm QFN package.

Features

- IDLE Mode Supply Current: 85µA
- Low Power Mode Supply Current: 1.9µA
- VPACK Voltages: 6V to 27V
- High Hot Plug Rating: 21V
- CELL Measurement Accuracy: ±12mV
- Open Wire and System Checks
- 6 High Voltage GPIOs

Applications

- Power tools
- Handheld electronics
- Battery health monitor

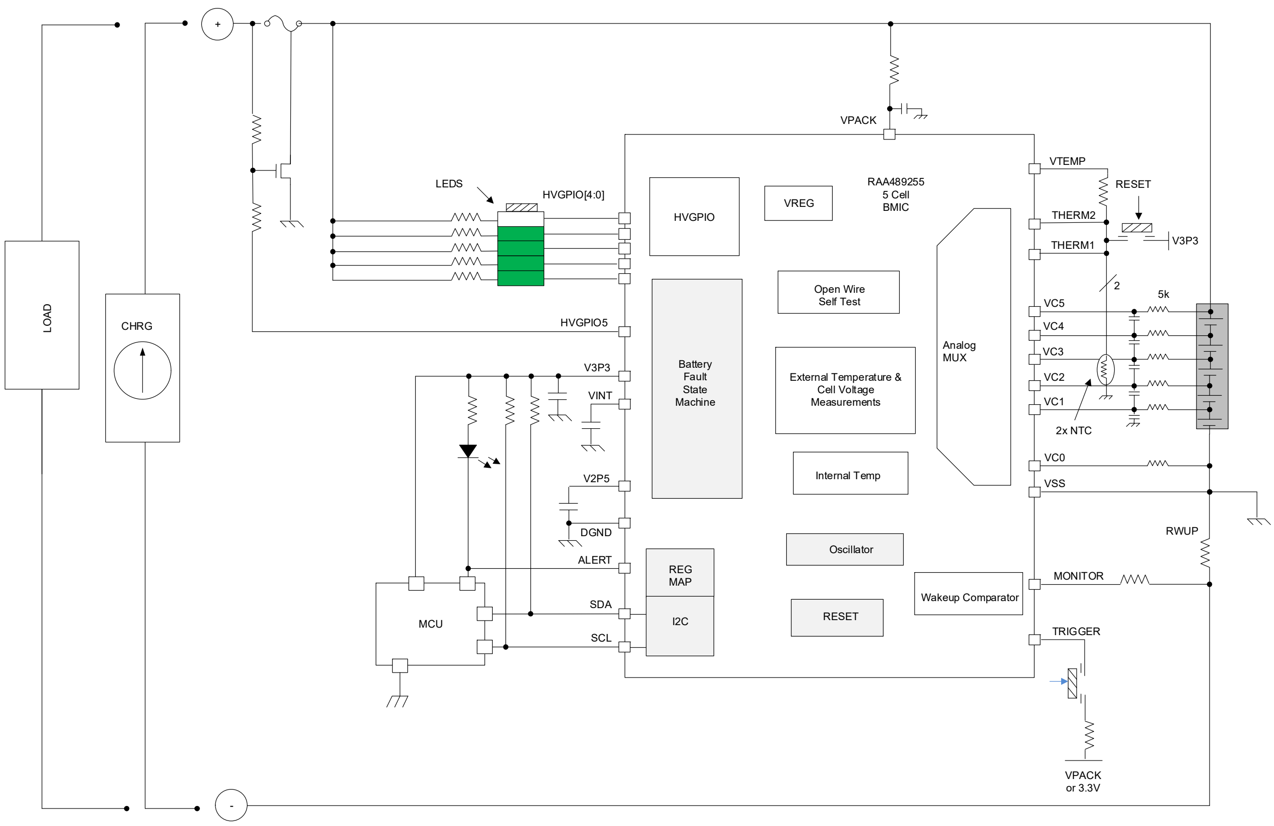

Figure 1. Typical Application

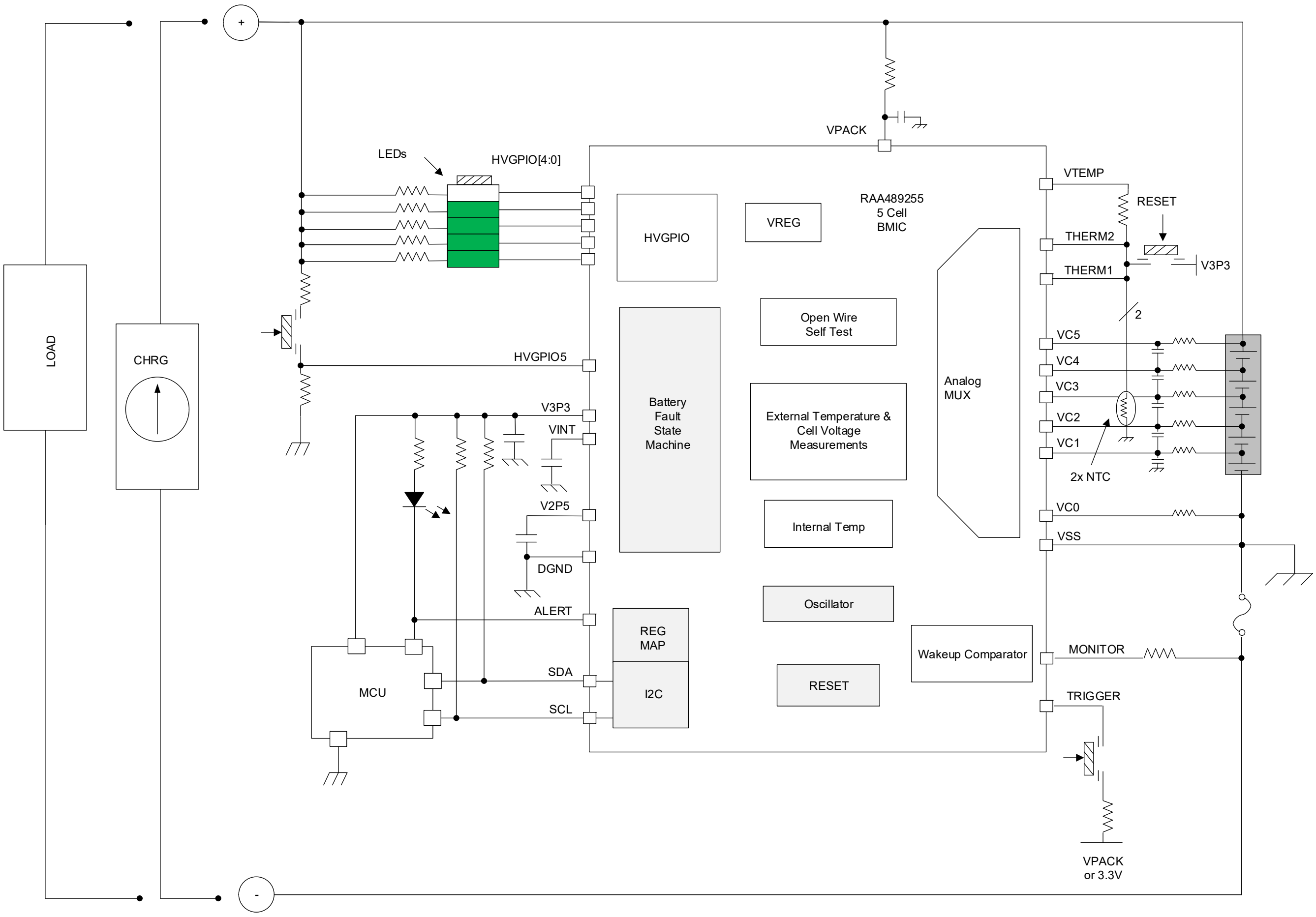

Figure 2. Alternate Application

Contents

1. Overview

1.1 Block Diagram

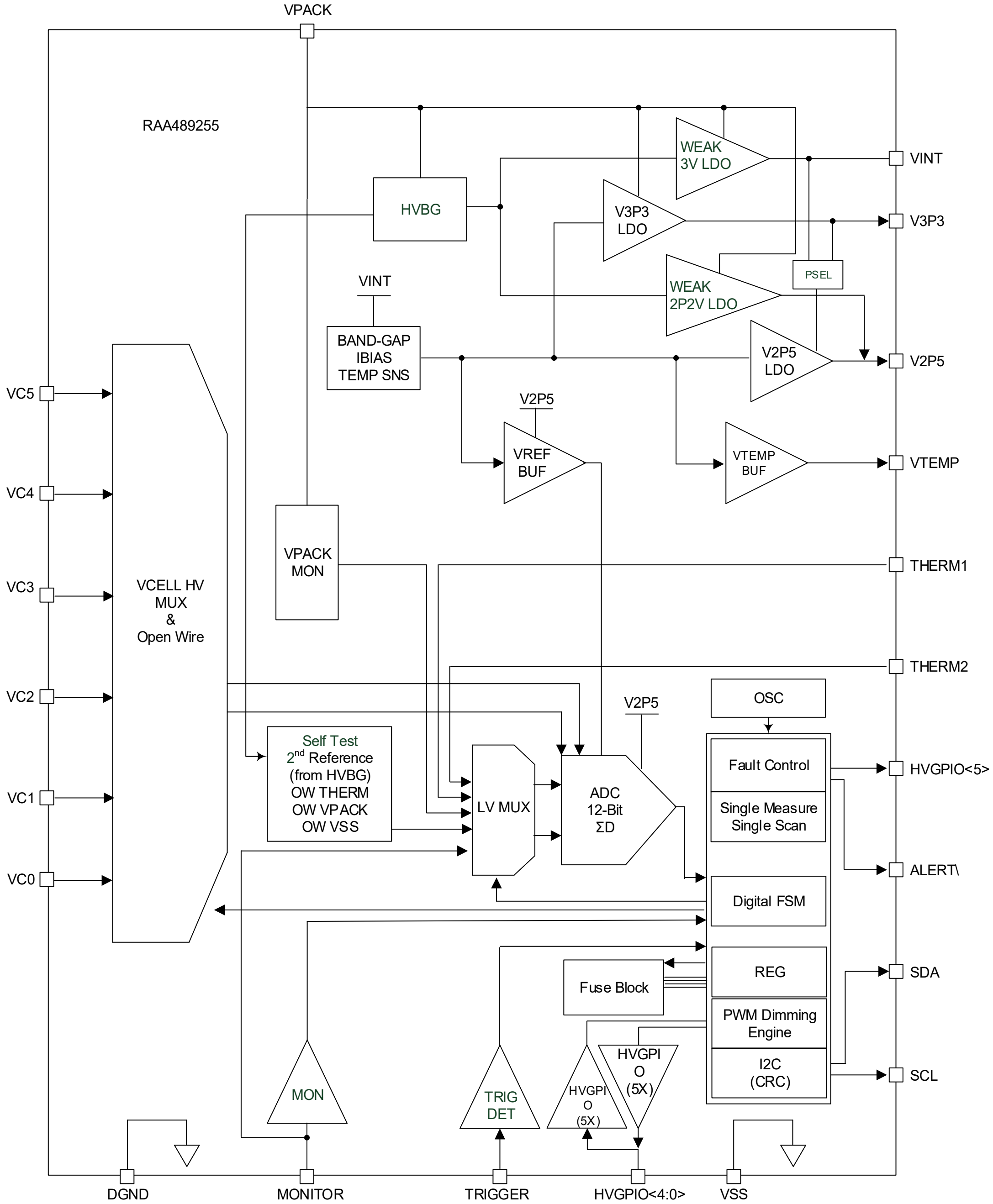

Figure 3. Block Diagram

2. Pin Information

2.1 Pin Assignments

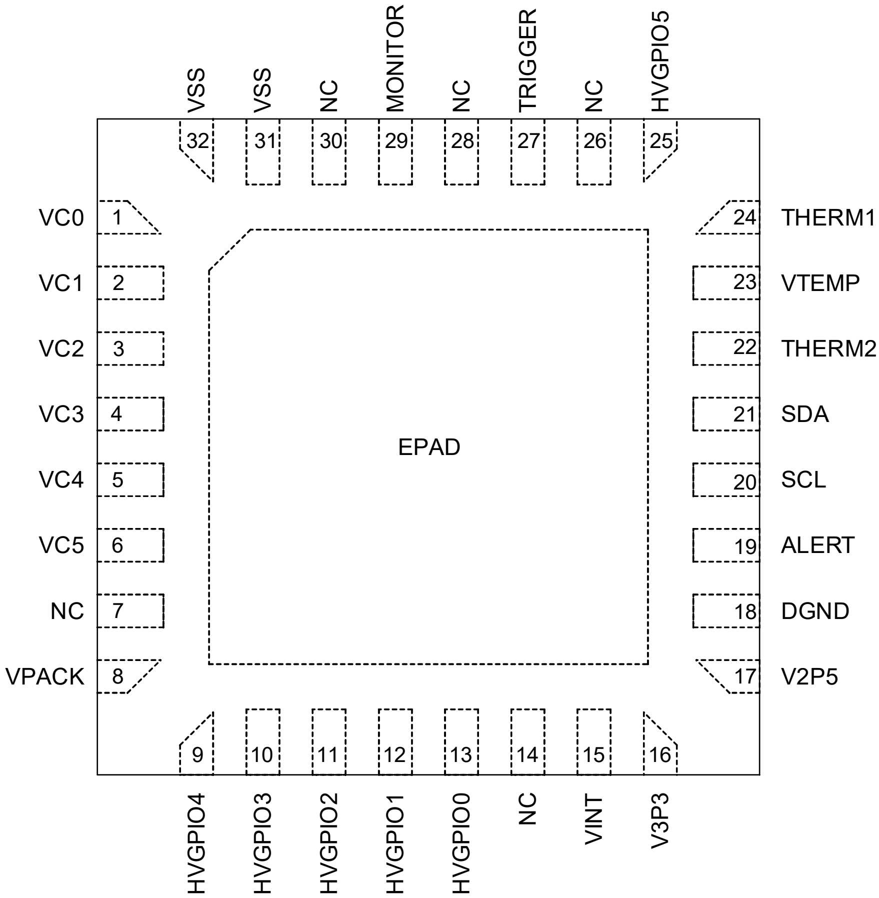

Figure 4. Pin Assignments - Top View

2.2 Pin Descriptions

Pin Number	Pin Name	Description
1	VC0	VC0 Sense Input. Voltage sense line for the negative terminal of CELL 1. This connection should be a separate path to the cell that does not carry load or charge current.
2, 3, 4, 5, 6	VCn (n = 1 to 5)	Battery cell voltage inputs. For applications with a 5-cell battery string, where cell number 1 connects to the lowest voltage and cell number 5 connects to the highest voltage, VCn connects to the positive terminal of cell n. The negative terminal of cell n connects to VC n-1. All connections from cell to pin are made through a low pass filter network (VC5 connects only to the positive terminal of Cell 5).
7, 14, 26, 28, 30	NC	No Connect. Do not connect these pins to bias other system nodes.
8	VPACK	VPACK Pin. Connect this pin to the pack voltage. A voltage at this pin powers the IC. Connect a series 10Ω and a 10µF capacitor from pin to VSS.
9	HVGPIO4	High Voltage GPIO Pins. The open-drain output pins can be used as high voltage general purpose Input / Output pins, or PWM outputs for LED control.
10	HVGPIO3	
11	HVGPIO2	
12	HVGPIO1	
13	HVGPIO0	

Pin Number	Pin Name	Description
15	VINT	3.3V internal supply decoupling pin. Connect a 4.7µF capacitor between this pin and VSS. Do not connect external loads to this pin.
16	V3P3	3.3V supply voltage output. Connect a 4.7µF capacitor between this pin and VSS. External loads may be connected to this node.
17	V2P5	Internal 2.5V supply decoupling pin. Connect a 1µF capacitor between V2P5 and DGND.
19	ALERT	ALERT Pin. The pin is the fault and status indicator for the pack. The Fault and Status bits can change the state of the ALERT pin. The pin is an open-drain NMOS. The pin asserts to the VSS level when a fault or status bit is present provided the signal of the bit is connected to the pin. Otherwise, the pin is in a high impedance state. A pull-up resistor greater than 10kΩ to MCU voltage is typically required.
18	DGND	Digital ground
20	SCL	Serial Clock Pin. This pin is the clock signal for the I2C communication interface. An optional pull-up resistor greater than 4.7kΩ to 3.3V can be attached.
21	SDA	Serial Data Pin. This is an open-drain serial data I/O for the I^2C communication interface.A pull-up resistor greater than 4.7kΩ to 3.3V is required
22	THERM2	Thermistor Pins. Connect a thermistor to each of these pins. Thresholds are compared to the respective measurement of the thermistor. Reset the device by connecting the THERM2 pin to V3P3 pin.
24	THERM1	
23	VTEMP	VTEMP Pin. Connect this pin to the pull-up resistor of the thermistor circuit.
25	HVGPIO5	High Voltage GPIO Pin. The open-drain output pin can be used as high voltage general purpose Input / Output pins and special wakeup function.
27	TRIGGER	TRIGGER. Connect to a switch/button that pulls the pin either to VPACK or VSS. The connection exits the device from Low Power mode.
29	MONITOR	Monitor. Connect to either a small resistor or a metal trace. The pin monitors for charge and discharge current.
31, 32	VSS	Ground. VSS is the negative reference voltage for the chip. In most applications, the pin is connected to GND.
-	EPAD	Electrical Pad. Connect to VSS.

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
VPACK	-0.3	+27	V
Trigger, HVGPIO[0:5]	-0.3	VPACK	V
VPACK - VC5	-27	+27	V
VC5	-0.3	+27	V
VC4	-0.3	+23	V
VC3	-0.3	+17	V
VC2	-0.3	+12	V
VC1	-0.3	+6.5	V
VC0	-0.3	+0.5	V
VCn - VC(n-1) (n = 1 to 5)	-0.3	6.5	V
DGND	-0.3	0.5	V
V3P3	-0.3	6.5	V
V2P5	-0.3	2.9	V
THERM1, VTEMP, THERM2, MONITOR	-0.3	2.9	V
SDA, SCL, ALERT	DGND -0.3	6.5	V
HVGPIO[0:5]	-20	0	mA
ALERT, SDA	-10	0	mA
Maximum Junction Temperature	-	+125	°C
Maximum Storage Temperature Range	-65	+150	°C
Human Body Model (Tested per JS-001-2023)	-	2	kV
Charged Device Model (Tested per JS-002-2022)	-	750	V
Latch-Up (Tested per JESD78E; Class 2, Level A)	-	100	mA

3.2 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Supply Voltage, VPACK	6	21.5	V
Ambient Temperature	-40	+85	°C
VCn - VC(n-1) (n = 1 to 5);	1.5	4.25	V
HVGPIO[0:5]	0	VPACK	V
ALERT, SDA, SCL	0	3.3	V
THERM1, THERM2	0	1.9	V
MONITOR	-0.100	1.9	V
DGND-VSS, VC0-VSS	-0.1	0.1	V

3.3 Thermal Information

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	32 Ld 4x4 QFN Package	θ_{JA}[1]	Junction to ambient	38	°C/W
		θ_{JC}[2]	Junction to case	2.5	°C/W

1. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
2. For θ_{JC}, the case temperature location is the center of the exposed metal pad on the package underside.

3.4 Electrical Specifications

T_A = +25°C, VPACK = 18V; VCn = 3.6V, DGND = VSS = 0V, unless otherwise specified. All voltages are with respect to VSS.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Power Supply						
Power-On Reset Voltage at VPACK	V_{PORf}	Falling edge	2.6	3.3	4.2	V
Power-On Reset Voltage at VPACK	V_{PORr}	Rising edge	-	4.87	-	V
Power-On Reset Voltage Hysteresis	V_{PORhys}			1.5	-	V
Current Consumed by the IC	I_{VPACK}	SCAN Mode (During Scan), VPACK = 21.5V	-	-	700	µA
		IDLE Mode, VPACK = 21.5V	-	-	85	µA
		Low Power Mode, VPACK = 21.5V	-	1.9	-	µA
VCn						
VCn Measurement Error	V_{Cn_ME}	Cells 1 to 5; T= 0°C to 25°C; RS = 1kΩ; VCn = 1.5V to 4.5V; Single Trigger Measurement	-12	±3	12	mV
VCn Leakage Current OFF	V_{Cn_IbOff}	-	-	100	-	nA
VPACK						
VPACK Attenuation	$V_{PACKAttn}$	-	-	18	-	V/V
VPACK Measurement Error	V_{PACK_ME}	7.5V < VPACK < 22.5V	-	±0.5	-	%
VPACK Measurement Error TC	V_{PACKME_TC}	T = -40C to 85C	-	±100	-	ppm/°C
VTEMP						
VTEMP Voltage Accuracy		0mA to 2mA load	2.00	2.06	2.12	V
VTEMP Measurement Error	V_{VTEMP_ME}	-	-	±4.5	-	mV
VTEMP Measurement Error TC	V_{VTEMP_TC}	T = -40C to 85C	-	±100	-	ppm/°C
Settling Time for VTEMP before a THERM1, THERM2 measurement	t_{VTEMP}	V_{TEMP} Turn on to first thermistor measurement	-	20	-	ms
VTEMP Max Threshold	$VTEMP_{max}$	Code > 0x06CC = OWF	-	2.253	-	V
VTEMP Min Threshold	$VTEMP_{min}$	Code < 0x0533 = OWF	-	1.843	-	V
Thermistor						
Thermistor Measurement Error	$THERM_{ME}$	VTHERMx = 1V	-	±4	-	mV

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Thermistor Measurement Error TC	$THERM_{TC}$	T= -40°C to 85°C	-	100	-	ppm/°C
THERM1 & THERM2 Pin Leakage Current		-	-1	-	1	µA
Open Wire Threshold Code	OW_{Vtherm}	Code greater than 0x0FD7 = OWF	-	1.9	-	V
RESET Voltage Threshold (THERM2)	RST_{Vtherm}	Only THERM2; Voltage above V2P5	0.4	-	-	V
RESET time (THERM2)	t_{RESET}	The time the THERM2 pin is above RST_{Vtherm} before the device RESETs	-	500	-	ms
RESET Exit Time (THERM2)	t_{RST_Exit}	The time between the THERM2 pin falling below 2.6V and the state machine transitioning to Power Up State (pin must not read OW)	-	2	-	ms
Power-On Reset Startup Time to Measurement	$t_{StartUp}$	VPACK > V_{POR}, RESET falling edge or soft reset or exiting LP Mode to the first measurement command	-	-	100	ms
Internal Temperature Sensor						
Internal Temperature Sensor Voltage	IT_{25C}	(25C ~0x006D) Char Only	-	0x006D	-	HEX
Internal Temperature Threshold	IOT_{TH}	Analog Comparator	-	100	-	C
VINT, V3P3 & V2P5						
V3P3 Voltage Accuracy	$V3P3_V$	At V3P3 Pin, no external load	3.20	3.33	3.44	V
VINT Pin Voltage	$V3P3_V$	Low Power Mode, no external load	-	3.3	-	V
V2P5 Pin Voltage	$V2P5_V$	Low Power Mode, no external load	-	2.5	-	V
V3P3 & V2P5 Measurement Error	REG_{ME}	-	-	±7.5	-	mV
V3P3 Drive current	I_{3p3v_Idrv}	-	10	20	-	mA
V3P3 & V2P5 Thresholds						
V3P3 Overvoltage Threshold	$dV3P3_{OV}$	Digital Compare, Self Test (0x0BE0)	-	3.553	-	V
V3P3 Undervoltage Threshold	$dV3P3_{UV}$	Digital Compare, Self Test (0x0999)	-	2.97	-	V
V3P3 Power-Good OV Threshold	PG_{V3P3_OV}	Analog Comparator	-	3.82	-	V
V3P3 Power-Good UV Threshold	PG_{V3P3_UV}	Analog Comparator	-	2.55	-	V
V2P5 Overvoltage Threshold	$dV2P5_{OV}$	Digital Compare, Self Test (0x08BD)	-	2.75	-	V
V2P5 Undervoltage Threshold	$dV2P5_{UV}$	Digital Compare, Self Test (0x06CA)	-	2.25	-	V
V2P5 Power Good OV Threshold	PG_{V2P5_OV}	Analog Comparator	-	2.82	-	V
V2P5 Power Good UV Threshold	PG_{V2P5_UV}	Analog Comparator	-	2.2	-	V

T_A = +25°C, VPACK = 18V; VCn = 3.6V, DGND = VSS = 0V, unless otherwise specified. All voltages are with respect to VSS.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Trigger						
Trigger Threshold	V_{TrThr}	Trigger_Pol = 1; Rising Edge Detect Trigger_Pol = 0; Falling Edge Detect	0.9	1.2	1.6	V
Trigger Hysteresis	V_{TrHys}	-	-	100	-	mV
Trigger Pin Internal Pull-Down	T_{RiPD}	To VSS	-	20	-	MΩ
Trigger De-Bounce	t_{Trdb}	Min time the pin exceeds threshold	-	4	-	ms
HVGPIO						
HVGPIO Low Level Output Voltage	$HVGPIO_{VOL}$	I_{sink} = 10mA	-	0.45	0.6	V
HVGPIO Low Level Input Voltage	$HVGPIO_{VIL}$		-	-	0.8	V
HVGPIO Leakage Current	$HVGPIO_{LIH}$	HVGPIO = VPACK	-	-	1	µA
HVGPIO5 Wakeup Threshold	$HVGPIO5_W$	Rising Edge Detect		1.6		V
Open Wire						
Open Wire Current	-	From VC pin to VSS	-	430	-	µA
Open Wire Detection Time	t_{OWON}	Open-wire current source on time	-	8	-	ms
Open Wire ADC Read Time	-	Reference to OW Assertion. Time to first compare	-	4	-	ms
Detection Threshold (VCn)	V_{OWth1}	ADC code 0x0058	-	0.6	-	V
Detection Threshold (VSS and VPACK)	V_{OWth2}	-	-	0.25	-	V
System						
4MHz Oscillator Accuracy	-	-	3.78	-	4.21	%
31.5kHz Oscillator Accuracy	-	-	25.83	-	37.84	%
ALERT Pin						
ALERT Low Level Output Voltage	AT_{VOL}	I_{sink} = 2mA	-	0.22	0.6	V
ALERT Low Level Input Voltage	AT_{VIL}	-	0	-	1.2	V
ALERT Leakage Current	AT_{LIH}	0V to 3.3V	-	<1	-	µA
I^2C Interface Specifications						
SDA and SCL Input Buffer LOW Voltage	V_{IL}	-	-0.3	-	$0.3xV_{3p3}$	V
SDA and SCL Input Buffer HIGH Voltage	V_{IH}	-	$0.7xV_{3p3}$	-	$V_{3p3}+0.3$	V
SDA and SCL Input Buffer Hysteresis	$I2C_{Hysteresis}$	-	-	$0.05xV_{3p3}$	-	V
SDA Output Buffer LOW Voltage	V_{OL}	I_{sink} = 2mA	0	0.23	0.4	V
Pin Leakage Current for SDA and SCL Pins	I_{leak}	-	-1	-	1	µA
SCL Frequency	f_{SCL}	-	-	-	400	kHz
Pulse Width Suppression Time at SDA and SCL Inputs	t_{IN}	Any pulse narrower than the max spec is suppressed	-	-	50	ns

T_A = +25°C, VPACK = 18V; VCn = 3.6V, DGND = VSS = 0V, unless otherwise specified. All voltages are with respect to VSS.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
SCL Falling Edge to SDA Output Data Valid	t_{AA}	SCL falling edge crossing 30% of V_{DD}, until SDA exits the 30% to 70% of V_{DD} window	-	-	900	ns
Time the Bus Must be Free Before the Start of a New Transmission	t_{BUF}	SDA crossing 70% of V_{DD} during a STOP condition, to SDA crossing 70% of V_{DD} during the following START condition	1300	-	-	ns
Clock LOW Time	t_{LOW}	Measured at the 30% of V_{DD} crossing	1300	-	-	ns
Clock HIGH Time	t_{HIGH}	Measured at the 70% of V_{DD} crossing	600	-	-	ns
SDA Low Time Out I2C communication is reset bus released	$t_{TIMEOUT}$	-	25	32	-	ms
8^{th} Bit to ACK Bit Delay (Applies to reading ADC Output Data Only)	$I^2C\_t_{WAIT}$	Time between the rising edge of the clock pulse corresponding to the last bit of any byte, and the falling edge of the clock pulse corresponding to the Acknowledge bit	7	-	-	µs
START Condition Setup Time	$t_{SU:STA}$	SCL rising edge to SDA falling edge. Both crossing 70% of V_{DD}	600	-	-	ns
START Condition Hold Time	$t_{HD:STA}$	From SDA falling edge crossing 30% of V_{DD} to SCL falling edge crossing 70% of V_{DD}	600	-	-	ns
Input Data Setup Time	$t_{SU:DAT}$	From SDA exiting the 30% to 70% of V_{DD} window, to SCL rising edge crossing 30% of V_{DD}	100	-	-	ns
Input Data Hold Time	$t_{HD:DAT}$	From SCL falling edge crossing 30% of V_{DD} to SDA entering the 30% to 70% of V_{DD} window	20	-	900	ns
STOP Condition Setup Time	$t_{SU:STO}$	From SCL rising edge crossing 70% of V_{DD}, to SDA rising edge crossing 30% of V_{DD}	600	17	-	ns
STOP Condition Hold Time	$t_{HD:STO}$	From SDA rising edge to SCL falling edge. Both crossing 70% of V_{DD}	600	45	-	ns
Output Data Hold Time	t_{DH}	From SCL falling edge crossing 30% of V_{DD}, until SDA enters the 30% to 70% of V_{DD} window	0	150	-	ns
SDA and SCL Rise Time	t_R	From 30% to 70% of V_{DD}	20+0.1×C	-	300	ns
SDA and SCL Fall Time	t_F	From 70% to 30% of V_{DD}	20+0.1×C	-	300	ns

4. Typical Performance Curves

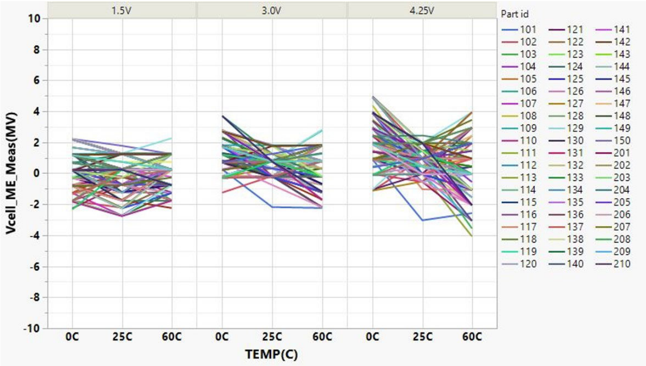


Figure 5. Cell 1 ME vs Voltage

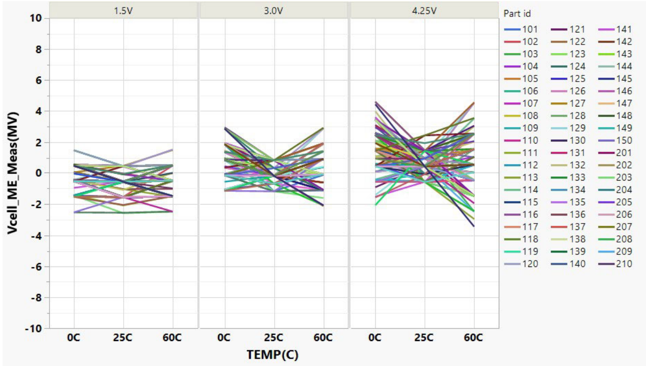


Figure 6. Cell 2 ME vs Voltage

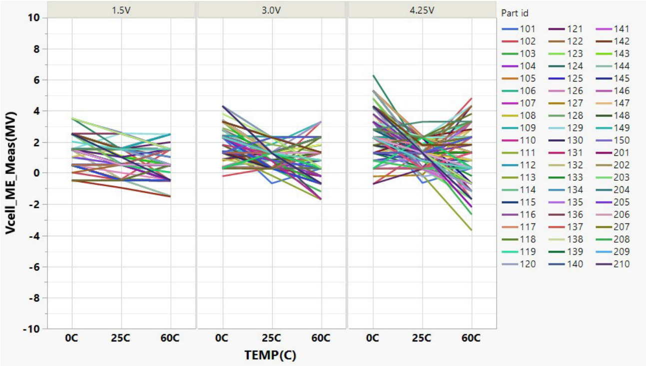


Figure 7. Cell 3 ME vs Voltage

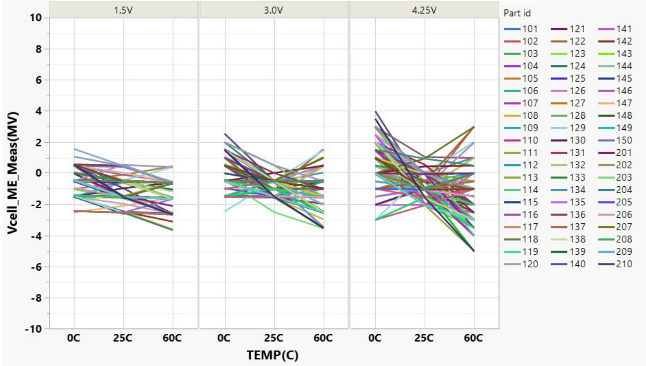


Figure 8. Cell 4 ME vs Voltage

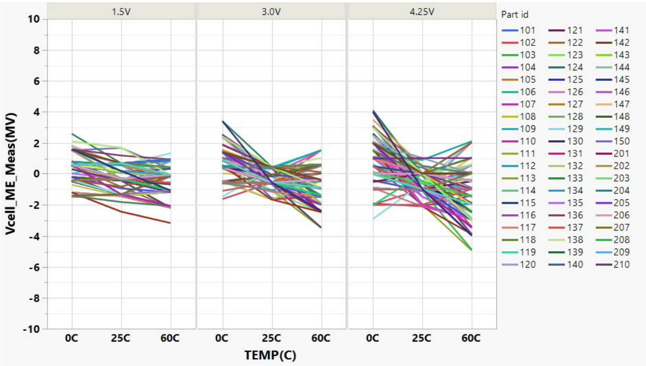


Figure 9. Cell 5 ME vs Voltage

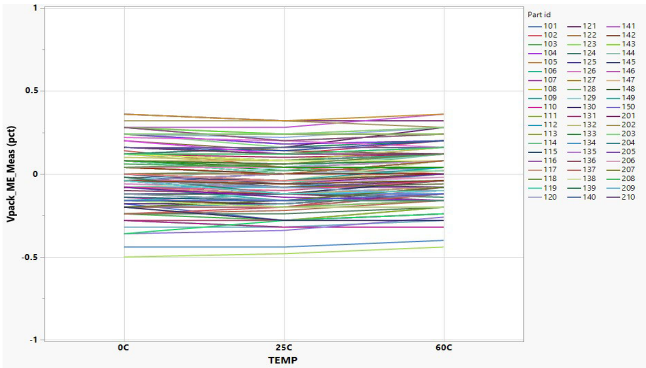


Figure 10. VPACK Pin Voltage ME

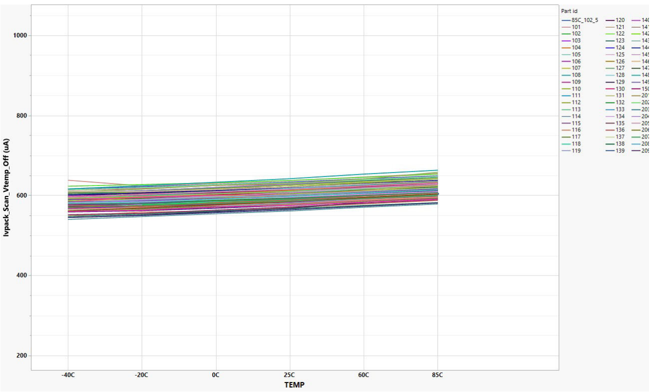


Figure 11. VPACK Current (SCAN)

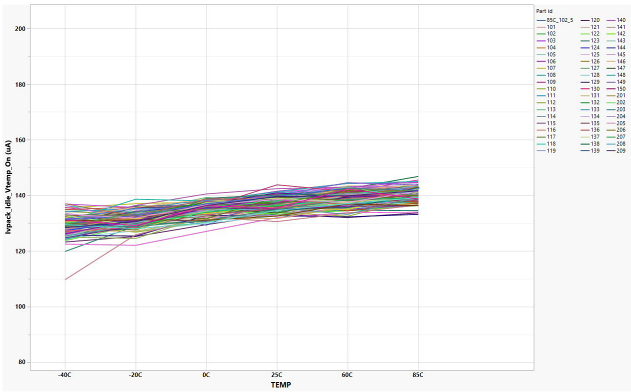


Figure 12. VPACK Current (IDLE, VTEMP ON)

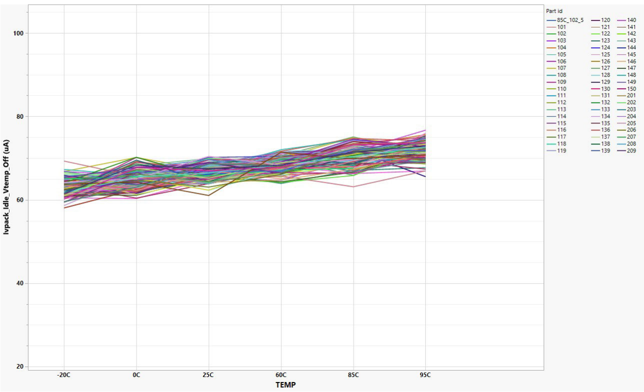


Figure 13. VPACK Current (IDLE, VTEMP OFF)

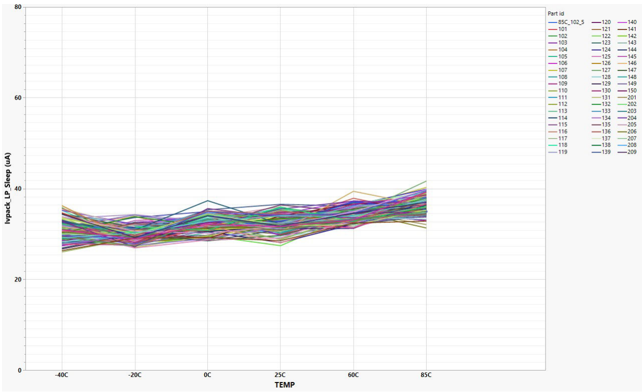


Figure 14. VPACK CURRENT (SLEEP, STRONG REG)

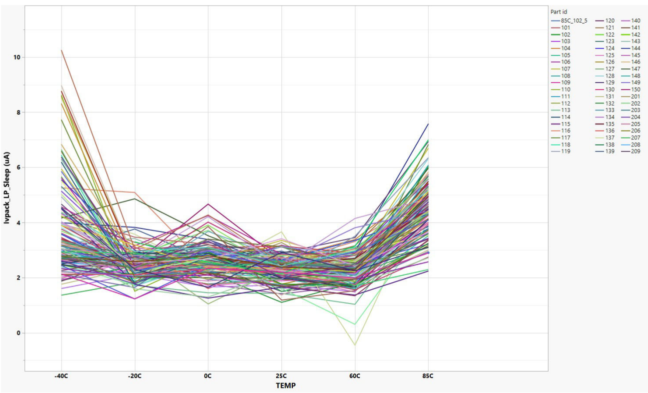


Figure 15. VPACK CURRENT (SLEEP, WEAK REG)

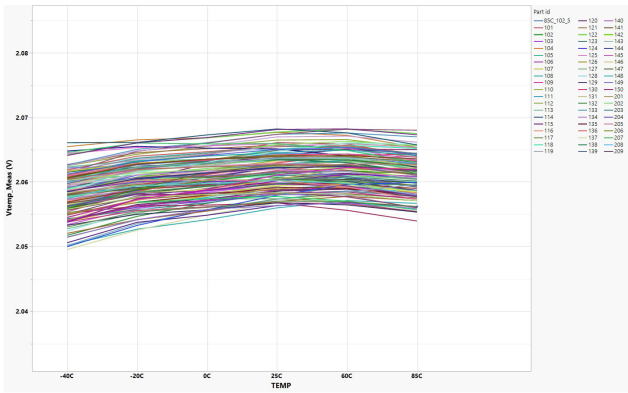


Figure 16. VTEMP Pin Voltage

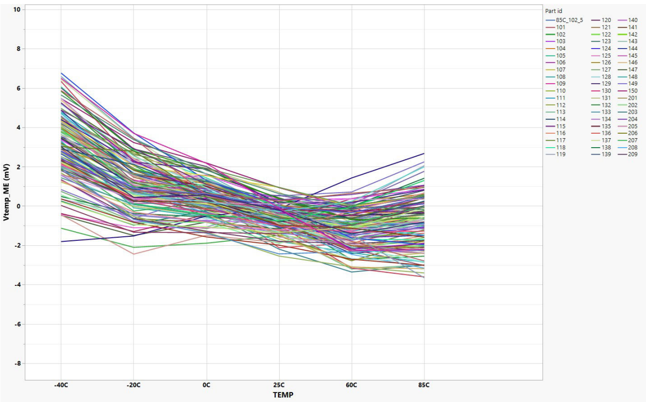


Figure 17. VTEMP Pin Voltage ME

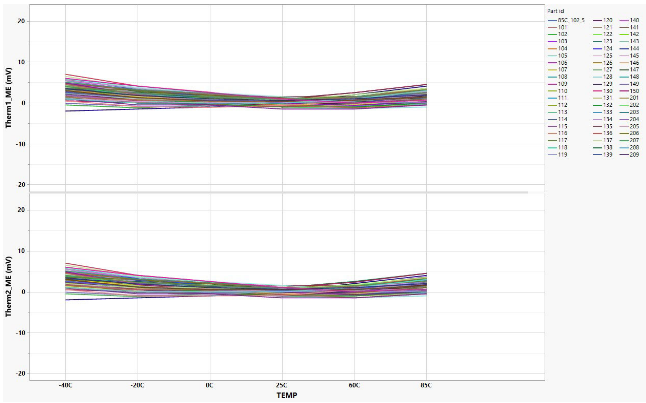


Figure 18. THERM Pins Voltage ME at 1.85V

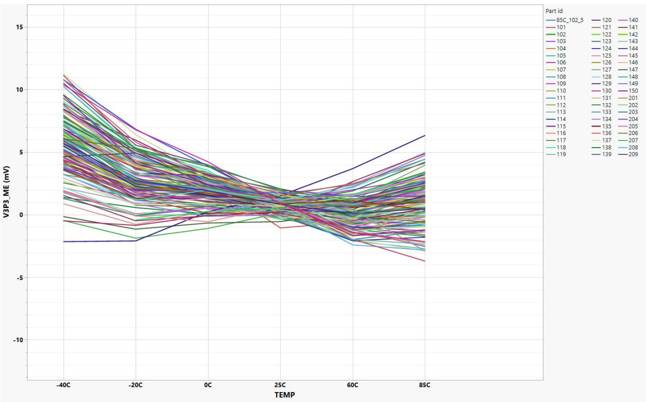


Figure 19. V3P3 Pin ME

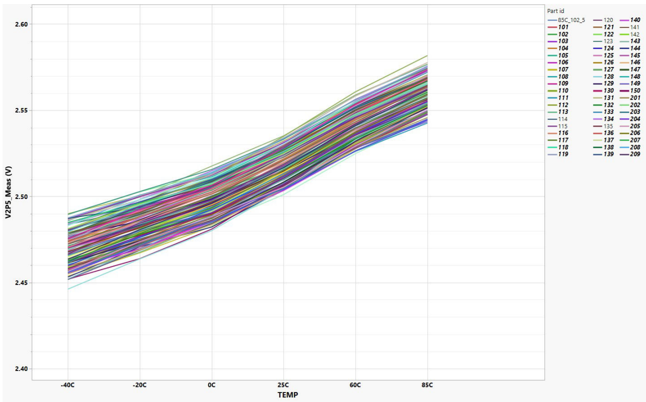


Figure 20. V2P5 Pin ME

5. State Machine Overview

The RAA489255 state machine flow diagram is illustrated Figure 21. This diagram shows the relationships between the device states and modes. A state executes its function then moves to the next state or mode, while modes can loop or remain static until another function or status change forces a transition out of the mode.

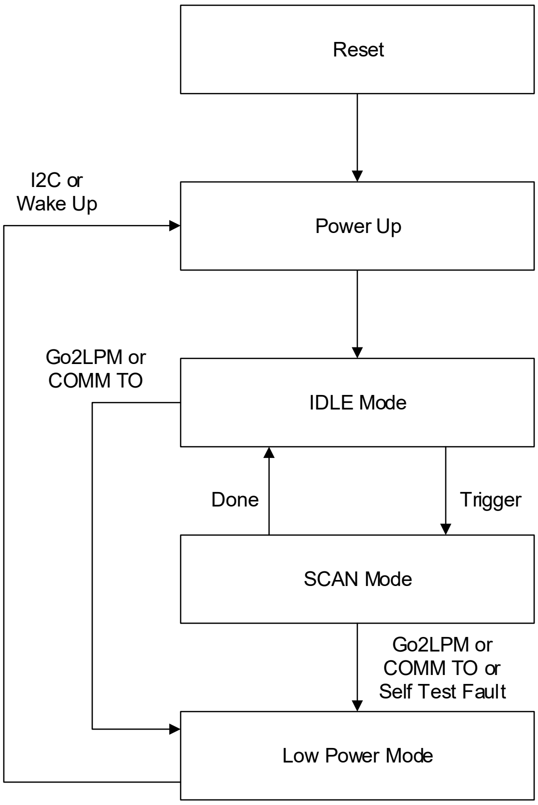


Figure 21. State Machine Flow Diagram

5.1 RESET State

At initial device power up the RAA489255 enters the RESET State. This state has the highest priority and is initiated by a momentary connection of the THERM2 pin to the V3P3 pin (RESET and THERM2) or a VPACK Pin 8 voltage lower than VPOR (V_{PORr}) or the V2P5 or V3P3 voltages (V3P3 & V2P5 Thresholds) falling below their Power-On Reset (POR) thresholds. A RESET interrupts any action the device is performing. Entering the RESET State also occurs when a 0x40.7 Soft Reset is executed.

The device turns off all regulators and oscillators when entering this state from a hard or soft reset. After completion of RESET, the device transitions to the Power Up State.

5.2 Power Up State

The Power Up State is entered from the RESET State. This state prepares the device for normal operation by executing device initialization followed by a check of the V3P3 and V2P5 PGOOD analog comparators.

The device turns on the oscillator and initializes logic states. It then reads trim/fuse settings, powers the monitor pins, the analog comparators, measurement amps and enables the ADC. Any faults detected in the Power Up State pauses the device in this state. A fault detected during IDLE or SCAN Mode by any of the V3P3 and V2P5 PGOOD analog comparators forces the device into the Power Up State until the fault clears.

On successful completion of initialization, the device transitions to IDLE Mode.

5.3 IDLE Mode

IDLE Mode is entered from the Power Up State, or on a wakeup detection (0x11.3 Trigger Wakeup, 0x11.2 COMM Wakeup, 0x11.1 HVGPIO5 Wakeup, or 0x11.0 Current Wakeup) from Low Power Mode.

By default, the MCU is in control of the system with the device in IDLE Mode. The MCU is responsible for triggering device measurements and fault reaction.

In IDLE Mode, the device executes commands from the MCU. The ALERT pin can assert for faults and for status bits provided the respective mask bit is cleared (see 0x10 Faults, 0x11 Status, and 0x40 Set Up 1).

Communication time out in IDLE Mode is controlled by bits 0x80.[14:13] Communication Time Out. If the SDA pin does not make a high-to-low transition while the SCL pin is high within the selected period, the device transitions to Low Power Mode. Setting bit 0x40.5 Go2LPM to 1 also transitions the device to LP Mode.

Executing 0x41.7 Trigger Measure causes a temporary transition to SCAN Mode to execute the setting of 0x41.[4:0] Measurement Select. When completed, the device transitions back to IDLE Mode to await the next MCU instruction.

5.4 SCAN Mode

The RAA489255 enters SCAN from IDLE Mode when a measurement is triggered and remains in SCAN Mode until the triggered measurement completes, then it transitions back to IDLE.

Communications Time-Out is active in both IDLE and SCAN Modes. The MCU must initiate communication with the device within the selected time (0x80.[14:13] Communication Time Out). Allowing the communication timer to expire causes a transition from IDLE or SCAN to Low Power Mode.

SCAN Mode allows the execution of a single measurement or an full Single System Scan sequence depending on the setting of 0x41.[4:0] Measurement Select. The flow chart for the Single System Scan sequence is shown in Figure 22. In SCAN mode, first a series of self tests are executed if enabled by setting bit 0x42.14 Self Test En to 1, by default this is disabled. Then, the thermistor voltages are measured based on the settings of 0x83.[7:6] Therm Enable. Finally, the Normal Measure portion of the Single System Scan, where the device performs a measurement sequence that checks the pack and cell voltages. Additionally, current measurements are performed if bit 0x80.8 Monitor Enable is set to 1.

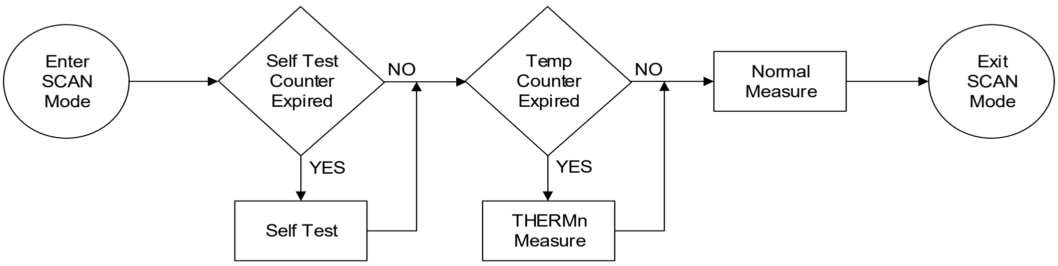


Figure 22. Single System Scan Sequence

5.4.1 Self Test Scan Sequence

Given that 0x42.14 Self Test En is enabled, depending on whether the bits 0x80.15 VCn Open Wire En or 0x83.[7:6] Therm Enable are enabled, the respective time taken for one system scan including Self Test, is shown in Figure 23. In Self Test sequence, the BandGap Voltage reference, V2P5 Voltage and VTEMP Voltage is digitally compared with HVBG voltage reference, whereas V3P3 Voltage is digitally compared with BandGap Voltage reference, the detailed block diagram is shown in Figure 3. For Open Wire tests on all VCn and THERM pins, the second reference voltage is derived from HVBG.

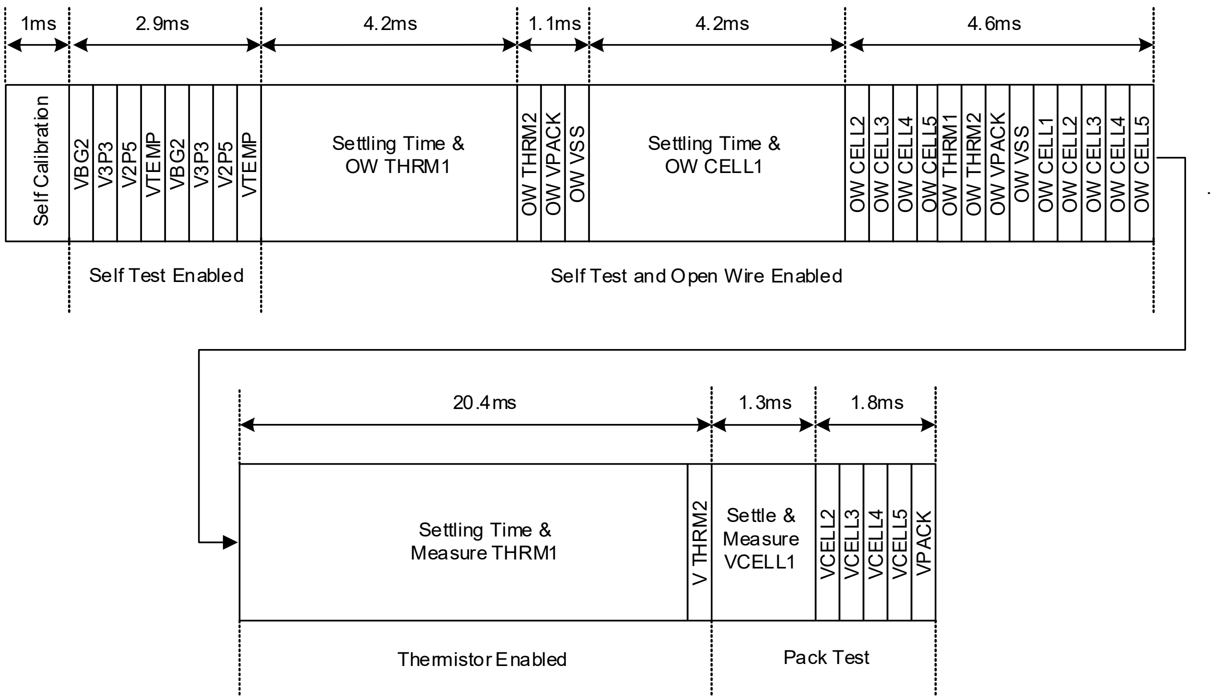


Figure 23. Scan Sequence Timing

5.5 Low Power Mode

The RAA489255 consumes the lowest current in Low Power (LP) Mode. All non-essential circuitry is shut off. In LP Mode, the device waits for a wakeup detection from pins MONITOR Pin 29, TRIGGER Pin 27, or HVGPIO5 Pin 25. An I^2C communication from the MCU, by asserting the SDA pin while the SCL pin is high, also exits LP to IDLE Mode.

The device transitions to LP Mode when a communication time out occurs or when the bit 0x40.5 Go2LPM is set to 1. Entry into LP Mode turns off the communication time out timer.

One bit controls power dissipation and regulator operation during LP Mode. The regulator has two possible settings in this Mode (see 0x42.13 LP Reg) one keeps it fully enabled, and the other reduces current consumption to a minimum.

Table 1. LP Mode Regulator Settings

0x42.13 LP REG Bit	Result
0	Weak Regulator; Register values are retained but external loads must be reduced.
1	Strong Regulator; Register values are retained; external loads and VTEMP can be Active

6. Register Summary

Table 2 lists the device registers.

Table 2. Device Register List

Addr (Hex)	Register Name	Pg#	Register Description[1]	Default (Hex)
Measurement Results (Read Only)				
00	Pack Voltage	21	[11:0] Step 9mV, Range: POR to 24V	0000
03	Thermistor 1	21	[11:0] Step 0.5mV, Range -0.128V to 1.92V	0000
04	Thermistor 2	21	[11:0] Step 0.5mV, Range -0.128V to 1.92V	0000
05	Monitor Pin Voltage Neg	22	[11:0] Step 0.5mV, Range -0.128V to 0V	0000
06	Monitor Pin Voltage Pos	22	[11:0] Step 0.5mV, Range 0V to 1.92V	0000
20	VTEMP Voltage	22	[11:0] Step 1mV, Range 0.512V to 4.608V	0000
21	VC1 Voltage	22	[11:0] Step 1mV, Range 0.512V to 4.608V	0000
22	VC2 Voltage		[11:0] Step 1mV, Range 0.512V to 4.608V	0000
23	VC3 Voltage		[11:0] Step 1mV, Range 0.512V to 4.608V	0000
24	VC4 Voltage		[11:0] Step 1mV, Range 0.512V to 4.608V	0000
25	VC5 Voltage		[11:0] Step 1mV, Range 0.512V to 4.608V	0000
Faults And Status (Read Only)				
10	Faults	23	[15] ALRTF [14] OWF [13] IOTF [12] VTEMPF [11] OSCF [10] STF [9] HVGPIOF [8] COMMTO [7] VPACK OWF [6] VSS OWF [5] REGF [4] VBGF [3] RSV [2] RSV [1] THERM1 OWF [0] THERM2 OWF	0000
11	Status	25	[15:10] HVGPIO 5 to 0 Pin Status; 1 - High (>VIL), 0 - Low [9] DCHRGI [8] CHRGI [7] BUSY [6] ALERT Pin Status; 1 - High (>VIL), 0 - Lo Status [5] IDLE; 0 - Not in IDLE Mode, 1 - In IDLE Mode [4] LPM; 0 - Not in LP Mode, 1 - Was In LP Mode [3] Trigger Wakeup [2] Comm Wakeup [1] HVGPIO5 Wakeup [0] Current Wakeup	FC20

Table 2. Device Register List (Cont.)

Addr (Hex)	Register Name	Pg#	Register Description[1]	Default (Hex)
Control (R/W)				
40	Set Up 1	27	[15] BUSY Mask [14] Wakeup Mask [13] Pin Fault Mask [12:8] RSV [7] Soft Reset; **0 - No Action**, 1 - Reset [6] Clear All Faults; **0 - No Action**, 1 - Clear All Faults and Counters [5] GO2LPM; **0 - No Action**, 1 - Go To LP Mode [4:3] RSV [2] ALERT Assert; 1 - Assert Pin, **0 - Deassert** [1:0] RSV	E000
41	Measurement	28	[15] Trigger Status; 1 - Triggered, **0 - Idle** [14:8] RSV [7] Trigger Measurement; 1 - Trigger, **0 - Idle** [6:5] RSV [4:0] Measurement Select	0000
42	Set Up 2	29	[15] VTEMP En; **0 - OFF**, 1 - ON [14] Self Test En; **0 - Disable**, 1 - Enable [13] LP Reg; 0 - Weak Regulator, **1 - Strong Regulator** [12:5] RSV [4:0] VCn ISRC; 1 - ON, **0 - Off**	2000
43	HVGPIO	30	[15:14] Pulse Duty Cycle [13:7] RSV [6] HVGPIO Pulse Enable; **0 - Disable**, 1 - Enabled [5:0] HVGPIO [5:0]; 1 - Assert Pin, **0 - De-assert (Hi -Z)**	0000
Configuration (R/W)				
80	System	31	[15] VCn OW Enable; **0 - Disable**, 1 - Enable [14:13] Comm Time Out [12:9] RSV [8] Measure Monitor En; **0 - Disable**, 1 - Enable [7] HVGPIO5 BUSY En; 0 - Disable, **1 - Enable** [6:0] RSV	6080
83	Thermistor	32	[15:8] RSV [7:6] THERM Enable; 00 - Off, 01 - THERM2, **10 - Both** [5:0] RSV	0080
84	RSV	32	[15:0] RSV	E000
85	Wakeup	32	[15:14] Current Wakeup Threshold [13:12] Current Wakeup Delay [11:1] RSV [0] Trigger Wakeup Polarity; 0 - Hi2Lo, **1 - Lo2Hi**	0001
Product Information (RO)				
FD	Die Revision	-	[3:0] Die Revision	0001
FE	Manufacturing ID	-	[7:0] Manufacturing ID	0049
FF	Device ID	-	[7:0] Device ID	0012

1. Bold text indicates default bit settings.

RAA489255 operation is determined by Control and Configuration registers. It is monitored by Measurement Results, Fault and Status registers. These are detailed in the following sections.

6.1 Measurement Results

A Battery Management System MCU monitors pack voltages and temperatures by accessing the RAA489255 Read Only measurement result registers. These voltages are measured and stored during the Single System Scan sequence or as single triggered measurements, see 0x41 Measurement on how to trigger measurements.

Equations, ranges, and step sizes in this section are typical values for calculation purposes and are not intended to imply operation at or beyond the Absolute Maximum Ratings.

6.1.1 0x00 Pack Voltage

The RAA489255 ADC measures the pack voltage using a buffered tap on a voltage divider between the VPACK Pin 8 and VSS Pins 31-32.

The measurement range, for calculation purposes, is from 3.834V (code 0x02AA) to 24V (code 0x0D80) with a step size of 9mV. Do not operate the device at or beyond the Absolute Maximum Ratings. Use Equation 1 to calculate the pin voltage from the register value.

(EQ. 1) $$VPACK = (RegVal) \times 9mV - 2.304V$$

6.1.2 0x03 THERM1 Voltage

The RAA489255 ADC measures the voltage at the THERM1 pin during the Single System Scan sequence. There are no temperature thresholds applied to this voltage with no related fault or status bits. The device does include open-wire testability, see 0x10.0 THERM1 OWF and THERMn Open-Wire Test for details.

The measurement range is from -128mV to 1.92V with a step size of 0.5mV. Use Equation 2 to calculate the pin voltage from the register value.

(EQ. 2) $$V_{THERM1} = (RegVal) \times 0.5mV - 128mV$$

The conversion from voltage to temperature is application specific, it is a function of the thermistor, pull-up resistor and VTEMP output voltage (see THERM2, VTEMP, THERM1 Pins 22-24).

If THERM1 is to be measured with a single triggered measurement then bit 0x42.15 VTEMP En must be set first, and then cleared following the measurement.

6.1.3 0x04 THERM2 Voltage

The RAA489255 ADC measures the voltage at the THERM2 pin during the Single System Scan sequence. There are no temperature thresholds applied to this voltage with no related fault or status bits. The device does include open-wire testability, see 0x10.1 THERM2 OWF and THERMn Open-Wire Test for details.

The measurement range is from -128mV to 1.92V with a step size of 0.5mV. Use Equation 3 to calculate the pin voltage from the register value.

(EQ. 3) $$V_{THERM2} = (RegVal) \times 0.5mV - 128mV$$

The conversion from voltage to temperature is application specific, it is a function of the thermistor, pull-up resistor and VTEMP output voltage (see THERM2, VTEMP, THERM1 Pins 22-24).

If THERM2 is to be measured with a single triggered measurement then bit 0x42.15 VTEMP En must be set first, and then cleared following the measurement.

6.1.3.1 Other Voltages

The RAA489255 includes additional measurement capabilities beyond those included in the Single System Scan with single triggered measurements (see 0x41 Measurement). Four additional measurements can be triggered, stored and accessed in the THERM2 Voltage register as indicated in Table 7.

For VINT Pin 15 and V2P5 Pin 17 the measurement range is from 0.512V to 4.608V with a step size of 1mV. Use Equation 4 to calculate the pin voltage from the register value.

(EQ. 4) $$VxP5 = (RegVal) \times 1mV + 512mV$$

The measurement range for internal VBG2 is from -127.5mV to 1.92V with a step size of 0.5mV. Use Equation 5 to calculate the pin voltage from the register value.

(EQ. 5) $$VBG2 = (RegVal) \times 0.5mV + 127.5mV$$

The Internal Temperature Reference Voltage can also be accessed using a single triggered measurement. The internal temperature reference voltage is designed to compare to the die over-temperature threshold.

6.1.4 0x05 Monitor NEG Voltage

The RAA489255 ADC measures the voltage at the MONITOR Pin 29 for later access by the system MCU. If bit 0x80.8 Monitor Enable is set to 1, the voltage is measured during the Single System Scan sequence. Negative voltages (Charge current) are stored in this register while positive voltages (Discharge Current) are stored in 0x06 Monitor POS Voltage.

The measurement range is from -128mV to 0V with a step size of 0.5mV. Use Equation 6 to calculate the pin voltage from the register value.

(EQ. 6) $$V_{MonNEG} = -1 \times \{(RegVal) \times 0.5mV - 128mV\}$$

6.1.5 0x06 Monitor POS Voltage

The RAA489255 ADC measures the voltage at the MONITOR Pin 29 for later access by the system MCU. If bit 0x80.8 Monitor Enable is set to 1, the voltage is measured during the Single System Scan sequence. Positive voltages (Discharge current) are stored in this register while negative voltages (Charge Current) are stored in 0x05 Monitor NEG Voltage.

The measurement range is from 0V to 1.92V with a step size of 0.5mV. Use Equation 7 to calculate the pin voltage from the register value.

(EQ. 7) $$V_{MonPOS} = (RegVal) \times 0.5mV - 128mV$$

6.1.6 0x20 VTEMP Voltage

The RAA489255 ADC measures the VTEMP pin voltage (THERM2, VTEMP, THERM1 Pins 22-24) during the Single System Scan if 0x42.14 Self Test En is set to 1.

The measurement range is from 0.520V to 4.608V with a step size of 1mV. Use Equation 8 to calculate the pin voltage from the register value.

(EQ. 8) $$VTEMP = (RegVal) \times 1mV + (512)mV$$

6.1.7 0x21-25 VCn Voltage

The RAA489255 ADC measures the cell voltages st the VCn Pins 1-6 for the MCU to use to limit the maximum charge and minimum discharge voltages.

The measurement range is from 0.512V to 4.608V with a step size of 1mV. Use Equation 9 to calculate the pin voltage from the register value.

(EQ. 9) $$VCn = (RegVal) \times 1mV + 512mV$$

6.2 Faults And Status

RAA489255 operation is monitored by accessing the Status and Fault registers.

6.2.1 0x10 Faults

The Fault Register is Read Only, all bits are latched. How and when each bit clears is specific to the bit, none clear on register read if the condition that sets them is still present. The ALERT pin is asserted when any of these bits are set, it is up to the MCU to react as the RAA489255 takes no other action. These bits are only updated in IDLE Mode and/or during a Single System Scan and are not cleared on exit from LP Mode.

This register and 0x11 Status register are intended to be read sequentially, see ALERT Pin 19. Reading the Fault register alone does not release the ALERT pin.

Table 3. 0x10 Register Definition

Register Address	Bit Function								Default (Hex)
	15/7 (MSB)	14/6	13/5	12/4	11/3	10/2	9/1	8/0 (LSB)	
0x10 (Upper Byte)	ALRTF	OWF	IOTF	VTMPF	OSCF	STF	HVGPIOF	COMMTO	00
0x10 (Lower Byte)	VPACK OWF	VSS OWF	REGF	VBGF	RSV	RSV	THERM1 OWF	THERM2 OWF	00

6.2.1.1 0x10.15 ALRTF

This ALERT pin Fault bit is set when the ALERT Pin 19 is externally forced to a different state from the programmed pin state. ALRTF is set based on a digital compare, the condition that sets this bit must clear before reading the register clears ALRTF.

There is a ~100µs delay following transition from LP to IDLE Mode before this pin state is tested.

6.2.1.2 0x10.14 OWF

The Open Wire Fault bit is set to 1 when any VCn pin fails the open-wire test. The test is a digital compare performed in the Self Test function of a Single System Scan if 0x42.14 Self Test En is set to 1 and 0x80.15 VCn Open Wire En is set to 1. Self Test and VCn Open Wire En are disabled by default. The relevant threshold is VOWth1.

The condition that sets this bit must be cleared during Self Test before reading the register clears OWF.

6.2.1.3 0x10.13 IOTF

The Internal Over Temperature Fault bit is set when the die temperature of the device exceeds 100C. The device monitors internal temperature continuously with an analog comparator. When IOTF sets the device takes no other action, this temperature is well above the operating range of the device. At some point above this temperature device operation may terminate.

This bit is not latched, it automatically clears only when the die temperature drops below ~100C.

6.2.1.4 0x10.12 VTMPF

The VTEMP Fault bit is set when the measured pin voltage violates either digital threshold VTEMPmax or VTEMPmin. These tests are a digital compare performed in the Self Test function of a Single System Scan if 0x42.14 Self Test En is set to 1. Self Test is disabled by default.

6.2.1.5 0x10.11 OSCF

The Oscillator Fault bit is set when normal operating range is exceeded. The oscillator is continuously monitored with an analog comparator when the device is not in LP Mode.

The condition that sets this bit must clear before reading the register clears OSCF.

6.2.1.6 0x10.10 STF

The Self Test Fault bit is set when any one of 0x10.15 **ALRTF**, 0x10.14 **OWF**, 0x10.11 **OSCF**, 0x10.9 **HVGPIOF**, 0x10.7 **VPACK OWF** or 0x10.6 **VSS OWF** fault bits are set.

The relevant threshold for VPACK and VSS OWF is VOWth2.

6.2.1.7 0x10.9 HVGPIOF

The HVGPIO Fault bit is set to 1 when one or more of the HVGPIO pins is externally forced to a different state from the programmed pin state. There is a 100µs delay following assert of the HVGPIO pin(s) before the state is tested with an analog compare. If the pin is asserted and takes longer to settle, due to a large capacitive load for example, the MCU must ignore and clear the fault bit by reading the status register until this extra delay period is over.

The HVGPIO Fault bit works only if 0x40.13 Pin Fault Mask is enabled(0), default setting is disabled(1).

6.2.1.8 0x10.8 COMMTO

The Communication Time Out bit is set to 1 when the device has not received a valid serial communications from the controller within the communication time out period. A communication time out fault transitions the device to LP Mode and is the only fault that does so. A valid serial communication is when the SDA line is pulled low by the controller while the SCL line is logically high. The time out period is programmable by setting the communication time out bits (0x80.[14:13] Communication Time Out).

The bit is set to 0 when the device resets or when a valid serial communication has been received.

6.2.1.9 0x10.7 VPACK OWF

The VPACK Open Wire Fault bit is set to 1 when VPACK pin fails the open-wire test. The test is a digital compare performed in the Self Test function of a Single System Scan if 0x42.14 Self Test En is set to 1 and 0x80.15 VCn Open Wire En is set to 1. Self Test and VCn Open Wire En are disabled by default.

6.2.1.10 0x10.6 VSS OWF

The VSS Open Wire Fault bit is set to 1 when the VSS or VC0 pin(s) fails the open-wire test. The test is a digital compare performed in the Self Test function of a Single System Scan if 0x42.14 Self Test En is set to 1 and 0x80.15 VCn Open Wire En is set to 1. Self Test and VCn Open Wire En are disabled by default.

6.2.1.11 0x10.5 REGF

The REG Fault bit reports under/over voltage digital compare detections at the V3P3 and V2P5 pins. The bit is set to 1 when the measured voltage exceeds the relevant digital threshold ($dV3P3_{OV}$, $dV3P3_{UV}$, $dV2P5_{OV}$, and $dV2P5_{UV}$). The V3P3 and V2P5 regulators have digital comparators that check these voltages during Self Test (if 0x42.14 Self Test En is set) and set this bit on failure.

These voltages also have analog comparators that monitor the voltages independent of ADC measurements, the REGF fault bit is not dependent on the analog comparators. If a V3P3 violation detection occurs on one of these the device transitions to the Wait State. A V2P5 violation causes a POR which may lead to a lack of I^2C communication if the voltage does not recover. The thresholds for these comparators can be found in the specification table, see PG_{V3P3_OV}, PG_{V3P3_UV}, PG_{V2P5_OV}, and PG_{V2P5_UV}.

6.2.1.12 0x10.4 VBGF

The BandGap Voltage reference Fault bit is set if the voltage fails the digital compare during the Self Test portion of a Single System Scan if 0x42.14 Self Test En is set to 1. Self Test is disabled by default.

6.2.1.13 0x10.1 THERM2 OWF

The THERM2 Open Wire Fault bit is set to 1 when the THERM2 pin (THERM2, VTEMP, THERM1 Pins 22-24) fails the open-wire test. The test is performed with a digital compare in the Self Test portion of a Single System Scan if 0x42.14 Self Test En is set to 1. Self Test is disabled by default. The relevant threshold is OWVtherm.

6.2.1.14 0x10.0 THERM1 OWF

The THERM1 Open Wire Fault bit is set to 1 when the THERM1 pin (THERM2, VTEMP, THERM1 Pins 22-24) fails the open-wire test. The test is performed with a digital compare in the Self Test portion of a Single System Scan if 0x42.14 Self Test En is set to 1. Self Test is disabled by default. The relevant threshold is OWVtherm.

6.2.2 0x11 Status

The Status Register is Read Only and the bits clear on read if the condition that sets them has cleared. Bits [15:5] are only updated in IDLE Mode while Bits [4:0] are updated on exit from LP Mode. All are cleared on entry into LP Mode. Due to their function, Bits [3:0] are referred to as the Wake-Up indicator bits.

This register and 0x10 Faults register are intended to be read sequentially, see ALERT Pin 19. Reading the Status register alone releases the ALERT pin but does not clear the Fault register.

Table 4. 0x11 Register Definition

Register Name	Bit Function								Default (Hex)
	15/7 (MSB)	14/6	13/5	12/4	11/3	10/2	9/1	8/0 (LSB)	
0x11 (Upper Byte)	HVGPIO5 State	HVGPIO4 State	HVGPIO3 State	HVGPIO2 State	HVGPIO1 State	HVGPIO0 State	DCHRGI	CHRGI	00
0x11 (Lower Byte)	BUSY	ALERT State	IDLE	LPM	Trigger Wakeup	COMM Wakeup	HVGPIO5 Wakeup	Current Wakeup	00

6.2.2.1 0x11.[15:10] HVGPIOn State

The HVGPIOn State bits report the status of the related HVGPIO pins. A value of 1 indicates the pin is pulled high. A value of 0 indicates the pin voltage is less than the VIL voltage.

All these bits indicate present status and are not latched. These bits can be reset with 0x40.6 Clear All Faults, but always indicate real-time status when not in LP Mode or RESET state.

6.2.2.2 0x11.9 DCHRGI

The Discharge Current Indicator bit sets if the voltage at the MONITOR Pin 29 is greater than threshold setting 0x85.[15:14] Current Wakeup Threshold. If the Monitor pin is connected through a resistor to the side of the current sense resistor that is not tied to VSS (for detection of current flow), this bit indicates charge is being removed from the battery pack.

This bit indicates present status and is not latched. This bit can be reset with 0x40.6 Clear All Faults, but always indicates real-time status when not in LP Mode or RESET state.

6.2.2.3 0x11.8 CHRGI

The Charge Current Indicator bit sets if the voltage at the MONITOR Pin 29 is more negative than threshold setting 0x85.[15:14] Current Wakeup Threshold. This threshold setting is interpreted as negative for CHRGI. If the Monitor pin is connected through a resistor to the side of the current sense resistor that is not tied to VSS, for detection of current flow, then this bit indicates charge is being added to the battery pack.

This bit indicates present status and is not latched. This bit can be reset with 0x40.6 Clear All Faults, but always indicates real-time status when not in LP Mode or RESET state.

6.2.2.4 0x11.7 BUSY

The Busy bit reports whether the device is busy measuring parameters or performing Self Test while the device is in SCAN or IDLE Modes. A Busy bit reading of 1 states that the device is busy measuring parameters or performing Self Test. A Busy bit reading of 0 states that device is idle.

This bit indicates present status and is not latched. The bit reports the current status of the measurement system. This bit can be reset with 0x40.6 Clear All Faults, but always indicates real-time status when not in LP Mode or RESET state.

The Busy bit status can be connected to the ALERT pin by clearing bit 0x40.15 BUSY Mask.

6.2.2.5 0x11.6 ALERT

The ALERT status bit reports the state of the ALERT pin when read back. A reading of 0 indicates the pin is pulled high. A reading of 1 indicates the pin voltage is less than the VIL voltage.

This bit indicates present status and is not latched. The bit reports the status of the ALERT Pin 19. This bit can be reset with 0x40.6 Clear All Faults, but always indicates real-time status when not in LP Mode or RESET state.

6.2.2.6 0x11.5 IDLE

The IDLE Mode status bit is set to 1 if the device is presently in IDLE Mode. This bit is cleared when the device exits IDLE Mode.

If this bit is clear and the device responds to I^2C reads then it is in the Power Up State, if it does not respond then it is in RESET State.

6.2.2.7 0x11.4 LPM

The Low Power Mode status bit is set to 1 if the device was previously in LP Mode. This bit is cleared when the device transitions to Low Power Mode and latched upon exiting LP Mode. The LP Mode Wakeup bits **0x11.[4:0]** can be cleared by executing 0x40.6 Clear All Faults.

6.2.2.8 0x11.3 Trigger Wakeup

The Trigger Wakeup status bit is set to 1 if the device was brought out of LP Mode by a TRIGGER Pin 27 wakeup detection. This bit allows the MCU to determine which mechanism wakes the device from LP Mode. It is cleared when the device transitions to Low Power Mode and latched upon exiting LP Mode. The LP Mode Wakeup bits **0x11.[4:0]** can be cleared by executing 0x40.6 Clear All Faults.

6.2.2.9 0x11.2 COMM Wakeup

The Communications Wakeup status bit is set to 1 if the device was brought out of LP Mode by a valid I^2C communication. A valid communication is detected when the SDA line is pulled low by the MCU while the SCL line is high. This bit allows the MCU to determine which mechanism wakes the device from LP Mode. It is cleared when the device transitions to LP Mode and latched upon exiting The LP Mode. LP Mode Wakeup bits **0x11.[4:0]** can be cleared by executing 0x40.6 Clear All Faults.

6.2.2.10 0x11.1 HVGPIO5 Wakeup

The HVGPIO Wakeup status bit is set to 1 if the device was brought out of LP Mode by a transition of the HVGPIO5 Pin 25. This bit allows the MCU to determine which mechanism wakes the device from LP Mode. It is cleared when the device transitions to Low Power Mode and latched upon exiting LP Mode. The LP Mode Wakeup bits **0x11.[4:0]** can be cleared by executing 0x40.6 Clear All Faults. Tie HVGPIO5 Pin 25 to VSS when this HVGPIO5 Wakeup feature is not used.

6.2.2.11 0x11.0 Current Wakeup

The Current Wakeup bit is set to 1 if the device was brought out of LP Mode by a current detection. The current voltage detection threshold is set by register bits 0x85.[15:14] Current Wakeup Threshold and detected at the MONITOR Pin 29. This bit allows the MCU to determine which mechanism wakes the device from LP Mode, see

0x11.9 DCHRGI and 0x11.8 CHRGI for current direction indication. This feature could also be used as Voltage Wakeup, as the mechanism to come out of LPM is via voltage detection at MONITOR Pin 29, with thresholds configurable by register bits 0x85.[15:14] Current Wakeup Threshold.

This bit is cleared when the device transitions to Low Power Mode and latched upon exiting LP Mode. The LP Mode Wakeup bits 0x11.[4:0] can be cleared by executing 0x40.6 Clear All Faults.

6.3 Control Registers

RAA489255 operation is directed by an MCU accessing the Control registers.

6.3.1 0x40 Set Up 1

This Read/Write register is used for device configuration and is only writable in IDLE Mode.

Table 5. 0x40 Register Definition

Register Name	Bit Function								Default(Hex)
	15/7 (MSB)	14/6	13/5	12/4	11/3	10/2	9/1	8/0 (LSB)	
0x40 (Upper Byte)	BUSY Mask	Wakeup Mask	Pin Fault Mask	RSV	RSV	RSV	RSV	RSV	E0
0x40 (Lower Byte)	Soft Reset	Clear All Faults	GO2LPM	RSV	RSV	ALERT Assert	RSV	RSV	00

6.3.1.1 0x40.15 BUSY Mask

The BUSY Mask bit connects the BUSY Bit (0x41.15 Trigger Status) status to the ALERT Pin 19 by asserting the pin to VSS when the device is making measurements. A mask bit setting of 0 connects the Busy bit status to the pin. A mask bit setting of 1 (default) disables this connection. A mask bit setting of 0 will cause the ALERT pin to assert for both Single System Scans and individual triggered measurements. The Busy Bit is only operational in SCAN and IDLE Modes.

6.3.1.2 0x40.14 Wakeup Mask

The Wakeup Mask bit connects the Wakeup status bits (see 0x11 Status, Bits [3:0]) status to the ALERT Pin 19 by asserting the pin to VSS when the device wakes from LP Mode. A mask bit setting of 0 connects the bit status of these bits to the ALERT pin. A mask bit setting of 1 (default) disables this connection. This signals the MCU the device has been brought out of LP Mode.

6.3.1.3 0x40.13 Pin Fault Mask

The Pin Fault Mask bit connects the pin fault status bits (0x10.15 ALRTF and 0x10.9 HVGPIOF) status to the ALERT Pin 19 by asserting it to VSS when the device detects a pin fault. A mask bit setting of 0 connects the bit status of these bits to the ALERT pin. A mask bit setting of 1 (default) disables this connection.

6.3.1.4 0x40.7 Soft Reset

Setting the Soft Reset bit to 1 resets all register values to the factory defaults, including data registers. The state machine jumps to the RESET State then proceeds to the Power Up State and finally to IDLE Mode. The bit action is equivalent to a hard reset or a power on reset event. All counters and state machines are set to their default states. This bit is cleared when the action is complete. The device takes ~4ms from the end of the I2C command to IDLE Mode to complete this action.

6.3.1.5 0x40.6 Clear All Faults

Write a 1 to the Clear ALL Faults bit to clear all counters, faults, and status bits. Other register settings are not affected by this command. On completion, the bit is automatically cleared to 0 (default).

Fault bits driven by analog comparators do not clear if the condition that sets them is present, see 0x10 Faults for specific bit descriptions. Use the Clear ALL Faults bit to clear faults retained when entering/exiting Low Power Mode.

6.3.1.6 0x40.5 Go2LPM

Write a 1 to the Go2LPM bit to force the device to transition to Low Power Mode immediately. The bit is only operable while in IDLE or SCAN Modes. Setting this bit during a measurement in SCAN Mode interrupts and stops measurements and the device transitions to LP Mode. The bit is automatically cleared to the default setting of 0 when the action is complete.

6.3.1.7 0x40.2 ALERT Assert

This bit enables testing of the ALERT pin by allowing the MCU to assert/de-assert it. When set to 1, this bit enables an internal NMOS, which provides a low impedance connection between the ALERT and VSS pins. Writing a 0 (default) to this bit turns OFF the NMOS, placing the pin in a high impedance state.

When asserted by this bit the ALERT pin stays low, this bit must be cleared for normal operation.

6.3.2 0x41 Measurement

This Read/Write register is used by the MCU to select and execute measurements and is only active while in IDLE Mode.

Table 6. 0x41 Register Definition

Register Name	Bit Function								Default (Hex)
	15/7 (MSB)	14/6	13/5	12/4	11/3	10/2	9/1	8/0 (LSB)	
0x41 (Upper Byte)	Trigger Status	RSV	RSV	RSV	RSV	RSV	RSV	RSV	00
0x41 (Lower Byte)	Trigger Measure	RSV	RSV	Measurement Select					00

6.3.2.1 0x41.15 Trigger Status

The Trigger Status bit indicates the status of the current measurement initiated by the trigger measure bit (0x41.7) and is read only. A value of 1 indicates that the device is performing a triggered measurement. The measurement result is available after this bit transitions from 1 to 0.

6.3.2.2 0x41.7 Trigger Measure

A 0 to 1 transition of this bit triggers the measurement selected with the Measurement Select bits. After the measurement has completed, the bit is automatically cleared to 0. All measurements are compared to their respective thresholds. The fault bit is set, but the device does not change modes when a digitally compared fault is detected.

6.3.2.3 0x41.[4:0] Measurement Select

The Measurement Select bits which measurements are made after Trigger Measure bit is set to 1. All measurement registers and fault/no current counters are updated for trigger measurements. Table 7 lists the actions the device can perform. The default selection is highlighted in gray.

Table 7. Measurement Selection

Measurement Select: D[4:0]					Measurement	Description
0	0	0	0	0	Single System Scan	One Complete System Scan with Self Test and Thermistor Measurements (if enabled). All measurement, fault and status registers are updated.
0	0	0	0	1	VTEMP	Measures the voltage at the VTEMP pin (THERM2, VTEMP, THERM1 Pins 22-24). The bit 0x42.15 VTEMP En must be set to 1 before measuring the pin. The result is stored in register 0x20 VTEMP Voltage.

Table 7. Measurement Selection (Cont.)

Measurement Select: D[4:0]					Measurement	Description
0	0	0	1	0	V3P3	Measures the voltage at the VINT Pin 15. The result is stored in the register 0x04 THERM2 Voltage.
0	0	0	1	1	V2P5	Measures the voltage at the V2P5 Pin 17. The result is stored in the register 0x04 THERM2 Voltage.
0	0	1	0	0	VBG2	Measures the VBG2 voltage. The result is stored in the register 0x04 THERM2 Voltage.
0	0	1	0	1	Internal Temperature	Measures the voltage at the Internal temperature sensor. The result is stored in the register 0x04 THERM2 Voltage.
0	0	1	1	0	THERM1	Measures the voltage at the THERM1 Pin (THERM2, VTEMP, THERM1 Pins 22-24). The result is stored in register 0x03 THERM1 Voltage. Bit 0x42.15 VTEMP En must be set (1).
0	0	1	1	1	THERM2	Measures the voltage at the THERM2 Pin (THERM2, VTEMP, THERM1 Pins 22-24). The result is stored in register 0x04 THERM2 Voltage. Bit 0x42.15 VTEMP En must be set (1).
0	1	0	0	0	VPACK	Measure the voltage at the VPACK pin. The result is stored in date register 0x00 Pack Voltage.
0	1	0	0	1	VC1	Measure the voltage at the VC1 pin (see VCn Pins 1-6). The result is stored in the VC1 data register (0x21-25 VCn Voltage).
0	1	0	1	0	VC2	Measure the voltage at the VC2 pin (see VCn Pins 1-6). The result is stored in the VC2 data register (0x21-25 VCn Voltage).
0	1	0	1	1	VC3	Measure the voltage at the VC3 pin (see VCn Pins 1-6). The result is stored in the VC3 data register (0x21-25 VCn Voltage).
0	1	1	0	0	VC4	Measure the voltage at the VC4 pin (see VCn Pins 1-6). The result is stored in the VC4 data register (0x21-25 VCn Voltage).
0	1	1	0	1	VC5	Measure the voltage at the VC5 pin (see VCn Pins 1-6). The result is stored in the VC5 data register (0x21-25 VCn Voltage).
1	0	1	1	0	Monitor VNEG	Measure the negative voltage between Monitor and VSS pins. The result is stored in register 0x05 Monitor NEG Voltage.
1	0	1	1	1	Monitor VPOS	Measure the positive voltage between Monitor and VSS pins. The result is stored in register 0x06 Monitor POS Voltage.
1	1	x	x	x	N/A	----- Reserved Do Not Program----.

6.3.3 0x42 Set Up 2

This Read/Write register is used for device configuration and is only writable in IDLE Mode.

Table 8. 0x42 Register Definition

Register Name	Bit Function								Default (Hex)
	15/7 (MSB)	14/6	13/5	12/4	11/3	10/2	9/1	8/0 (LSB)	
0x42 (Upper Byte)	VTEMP En	Self Test En	LP Reg	RSV	RSV	RSV	RSV	RSV	20
0x42 (Lower Byte)	RSV	RSV	RSV	VC5 I_{SRCE}	VC4 I_{SRCE}	VC3 I_{SRCE}	VC2 I_{SRCE}	VC1 I_{SRCE}	00

6.3.3.1 0x42.15 VTEMP En

The VTEMP Enable bit turns ON or OFF the VTEMP output. The default setting of 0 turns OFF the output while a setting of 1 turns it ON. This bit is only functional in IDLE Mode. This bit must be set to enable the VTEMP output before individual THERM Pin measurements are triggered using 0x41.[4:0] Measurement Select and 0x41.7 Trigger Measure. Disable the VTEMP output to save power following the measurement.

When a Single System Scan is executed, the device automatically controls the VTEMP output for thermistor measurement. The state machine turns ON and OFF the VTEMP output while executing the Therm and Self Test Loops while in system scan. The state machine does not change the state of this bit while in this mode.

6.3.3.2 0x42.14 Self Test En

The Self Test Enable bit setting of 1 includes the Self Test function during the Single System Scan sequence. See Figure 22. A setting of 0 (default) bypasses Self Test during the Single System Scan sequence, which prevents fault detection for faults dependent on Self Test. See section 0x10 Faults for the faults that are dependent on Self Test.

6.3.3.3 0x42.13 LP Reg

The Low Power Regulator bit defines VINT Pin 15 regulator operation while in Low Power Mode. A setting of 1 (default) enables the strong regulator in LP Mode allowing external loads to operate. The power-good comparators are enabled when the strong regulator is used. The current consumption of the device is higher while this regulator is enabled. A setting of 0 enables the weak regulator while in LP Mode reducing current consumption to minimum, though external loads must also be minimized.

For the lowest power consumption in LP Mode, the MCU should set LP Reg to 0 while the device is in IDLE Mode.

6.3.3.4 0x42.[4:0] VCn ISRC

Setting this bit to 1 turns on the open-wire current source that connects between the VCn pin and VSS. The default setting for these bit is 0.

6.3.4 0x43 HVGPIO

This Read/Write register controls the operation of the HVGPIO pins and is only writable in IDLE Mode. This register is cleared to the default values when the device transitions to LP Mode and remains cleared on Wakeup. This prevents the HVGPIO pins from dissipating pack power in LP Mode.

Table 9. 0x43 Register Definition

Register Name	Bit Function								Default (Hex)
	15/7 (MSB)	14/6	13/5	12/4	11/3	10/2	9/1	8/0 (LSB)	
0x43 (Upper Byte)	Pulse Duty Cycle		RSV	RSV	RSV	RSV	RSV	RSV	00
0x43 (Lower Byte)	RSV	Pulse Enable	HVGPIO5 Assert	HVGPIO4 Assert	HVGPIO3 Assert	HVGPIO2 Assert	HVGPIO1 Assert	HVGPIO0 Assert	00

6.3.4.1 0x43.[15:14] Pulse Duty Cycle

The Pulse Duty Cycle bits set the duty cycle to toggle on/off the HVGPIOs when used as outputs/LED drivers. The default setting is highlighted in gray.

Table 10. Duty Cycle Selections

D[15:14]	Duty Cycle
00	20%
01	40%
10	60%
11	80%

6.3.4.2 0x43.6 Pulse Enable

The Pulse Enable bit applies setting 0x43.[15:14] Pulse Duty Cycle to the HVGPIO outputs when set to 1 or disables the feature if set to 0 (default).

6.3.4.3 0x43.[5:0] HVPIOn Assert

The HVGPIOn Assert bits control the HVGPIO pin output states. If set to 0 (default), the related open-drain NMOS device is disabled, putting the HVGPIO pin in a hi-z state allowing the pin to float to its pull-up voltage. A setting of 1 turns on the NMOS forcing the pin low with a connection to VSS. The assertion is controlled by the settings of 0x43.[15:14] Pulse Duty Cycle and 0x43.6 Pulse Enable.

6.4 Configuration Registers

RAA489255 operation is directed by an MCU accessing the Configuration registers.

6.4.1 0x80 System

This Read/Write register is used for device configuration and is only writable in IDLE Mode.

Table 11. 0x80 Register Definition

Register Name	Bit Function								Default (Hex)
	15/7 (MSB)	14/6	13/5	12/4	11/3	10/2	9/1	8/0 (LSB)	
0x80 (Upper Byte)	VCn OW En	Communication Time Out		RSV		RSV		Monitor EN	60
0x80 (Lower Byte)	HVGPIO5 BUSY En	RSV	RSV	RSV	RSV	RSV	RSV	RSV	80

6.4.1.1 0x80.15 VCn Open Wire En

Setting the Cell Voltage Open Wire Enable bit to 1 includes open-wire test for cell connections in the Single System Scan sequence, only if 0x42.14 Self Test En is set to 1, Self Test is disabled by default. An open-wire test can be executed while in IDLE mode by triggering the single system scan with this bit set to 1. When set to 0 (default) open-wire test for the VCn pins is disabled.

6.4.1.2 0x80.[14:13] Communication Time Out

The Communication Timeout bits select the minimum time between MCU communications with the RAA489255 before the state machine transitions the device to LP Mode.

When the controller asserts the SDA pin while the SCL pin is high, the communication timer resets to 0. Table 12 lists the selectable times with the default setting highlighted in gray.

Table 12. COMM TO Selections

D[14:13]	Time Out Time (s)
00	OFF
01	0.1
10	1
11	5

6.4.1.3 0x80.8 Monitor Enable

Set this bit to 1 to enable measurement of the Monitor Pin voltage during the Single System Scan sequence. Measurement results are stored in registers 0x05 Monitor NEG Voltage and 0x06 Monitor POS Voltage depending on the polarity of the voltage.

When set to 0 (default) measurement of the pin voltage is disabled.

6.4.1.4 0x80.7 HVGPIO5 BUSY En

Set the HVGPIO5 BUSY Enable bit to 0 to disconnect BUSY Status from pin HVGPIO5. The default setting of 1 sets output 0x11.7 BUSY bit status (inverted) to the HVGPIO5 pin.

Note: If BUSY status is mapped to HVGPIO5, set bit 0x40.15 BUSY Mask to 1 to mask BUSY Status from the ALERT pin.

6.4.2 0x83 Thermistor

This Read/Write register is used for thermistor configuration and is only writable in IDLE Mode.

Table 13. 0x83 Register Definition

Register Name	Bit Function								Default (Hex)
	15/7 (MSB)	14/6	13/5	12/4	11/3	10/2	9/1	8/0 (LSB)	
0x83 (Upper Byte)	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	00
0x83 (Lower Byte)	Therm Enable		RSV	RSV	RSV	RSV	RSV	RSV	80

6.4.2.1 0x83.[7:6] Therm Enable

The Thermistor Enable bits select the thermistor configuration for the device measurement during the Single System Scan sequence. The bit selection choices are listed in Table 14 with the default setting highlighted in gray.

Table 14. Thermistor Enable Selection

Thermistor Enable Bits: D[7:6]		Action
0	0	OFF (no measurements)
0	1	THERM1
1	0	THERM1 and THERM2
1	1	THERM 1 and THERM2

6.4.3 0x85 Wakeup

This Read/Write register is used for configuration of wakeup control and is only writable in IDLE Mode.

Table 15. 0x85 Register Definition

Register Name	Bit Function								Default (Hex)
	15/7 (MSB)	14/6	13/5	12/4	11/3	10/2	9/1	8/0 (LSB)	
0x85 (Upper Byte)	Current Threshold		Current Delay		RSV	RSV	RSV	RSV	00
0x85 (Lower Byte)	RSV	RSV	RSV	RSV	RSV	RSV	RSV	Trigger Pol	01

6.4.3.1 0x85.[15:14] Current Wakeup Threshold

The current wakeup threshold setting determines the voltage threshold required at the MONITOR Pin 29 to wake up the device and set bit 0x11.0 Current Wakeup. The threshold is applied to both voltage polarities (Charge and Discharge current). A minimum time period determined by 0x85.[13:12] Current Wakeup Delay is also required to set the set the wakeup bit and wake the device. The threshold detection is accomplished with an analog comparator.

The bit selection choices are listed in Table 16 with the default setting highlighted in gray.

Table 16. Current Wakeup Threshold Selection

Current Wakeup Threshold Bits: D[15:14]		Threshold
0	0	6.25mV
0	1	12.5mV
1	0	25mV
1	1	50mV

6.4.3.2 0x85.[13:12] Current Wakeup Delay

The Current Wakeup Delay setting determines the time period the MONITOR Pin 29 voltage must remain above the 0x85.[15:14] Current Wakeup Threshold voltage before the device wakes up and bit 0x11.0 Current Wakeup is set.

The bit selection choices are listed in Table 17 with the default setting highlighted in gray.

Table 17. Current Wakeup Delay Selection

Current Wakeup Delay Bits: D[13:12]		Delay
0	0	1ms
0	1	2ms
1	0	4ms
1	1	8ms

6.4.3.3 0x85.0 Trigger Pol

The Trigger Polarity setting controls the wakeup detection method used by the TRIGGER Pin 27. A setting of 1 (default) wakes the device on a low to high transition (rising edge) of the pin voltage relative to VSS. Set the bit to 0 to wake the device on a high to low transition (falling edge) of the Trigger pin.

The rising and falling edge detection threshold is VTrThr with a hysteresis of VTrHys.

When the device wakes up bit 0x11.3 Trigger Wakeup is set to indicate the source.

7. I^{2}C Serial Interface

The RAA489255 includes a digital interface to configure device operation and monitor status. The device has an I^{2}C SMBus serial interface, which can be used (except during reset) to read the device faults and status.

This device supports a bidirectional bus-oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the controller. The device being controlled is the target. The controller always initiates data transfers and provides the clock for both transmit and receive operations. The RAA489255 operates as the target device for all applications.

The device uses command codes to perform block reads. The device does not support random sequential reads. A command code read is a block read with the starting register address and the number of bytes to read back digitally encoded into the device. Command codes support register read backs with and without CRC.

7.1 I^{2}C Target Address

The device can be used with any I^{2}C host device. Each device must have its own unique serial address. The device supports packet error checking. Packet error checking is enabled by a separate target address.

The target address for both CRC and non-CRC packages are listed in Table 18.

Table 18. I²C Address Values

Method	Address (7-Bit Binary)
Packets without CRC	0010 010
Packets with CRC	1010 110

7.2 Communication Packet Format

The device communicates with a controller that is complaint with the I²C protocol. The device processes read and write requests as word (2 byte) widths. A write action requires two bytes of data to change the individual bits within the register. The minimum data width for a read command is two bytes. The device supports command codes (Command Codes) in place of sequential reads.

The byte order is compliant to the little-endian standard. Little-endian sends the 1st 8-bit data byte containing data bits 7 through 0 of the 16-bit data 2-byte word first. The second data byte contains data bits 15 through 8. The most significant bit within the byte is data bit 7 for the first byte and data bit 15 for the second byte. The least significant bit for each byte is data bit 0 for the 1st byte and data bit 8 for the second byte.

The device processes the packet in byte widths. For example, if reading 0x8008 from a register, the device sends byte 0x08 first and 0x80 as the second byte (overall 0x0880). The write byte is ordered in the same manner. A register value of 0x12FE is sent to the device as 0xFE12. It is the responsibility of the controller to correctly order the bytes. Figure 24 shows the order of the data bytes for a read. Figure 25 shows the order of the data bytes for a write.

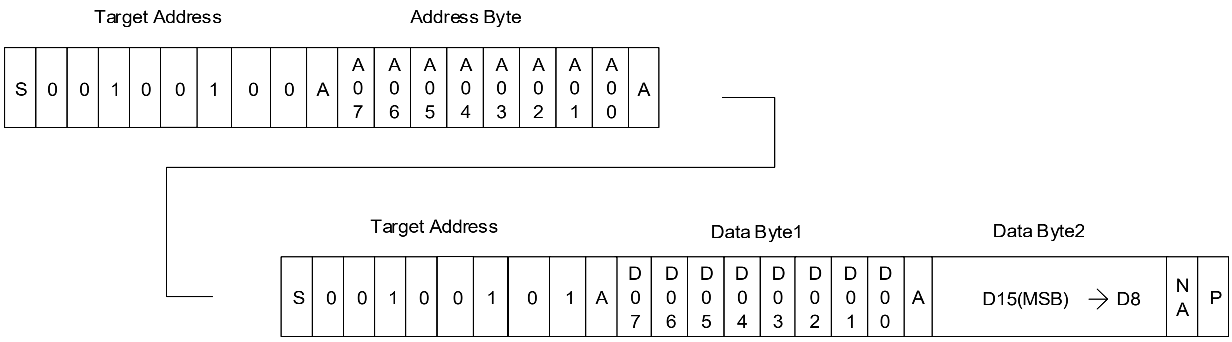


Figure 24. I²C Read Data Format

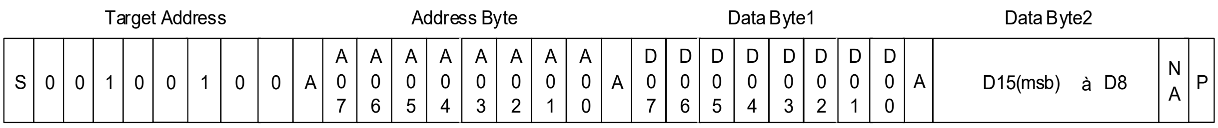


Figure 25. I²C Write Data Format

7.3 Cyclical Redundancy Check

The device has a Cyclical Redundancy Check (CRC) option for more secure communications between controller and target. The CRC code is a byte in length. The equation of the CRC is $X^8+X^2+X^1+1$ with a minimum Hamming Distance of 4 for payloads up to 247 bits.

For Read commands, the target sends CRC byte(s) as part of the read packet. It is the responsibility of the controller to compare the CRC byte to the CRC calculated by the controller. The controller writes several bytes to indicate a Read command, and to which register address to read from. The target responds to the controller and includes a CRC byte with the calculated value for the two target address bytes, the address byte, and the read word. Figure 32 illustrates the read format with a CRC byte.

For Write commands, the target device register is only changed if the transmitted CRC byte by the controller is the same value as the CRC byte calculated by the target. When the two CRC bytes agree, the target transmits an acknowledged bit (ACK) to the controller. If the byte values do not agree, then a NACK is transmitted. Figure 30 illustrates the write format with a CRC byte.

7.4 Protocol Conventions

The logic state on the SDA line can change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (see Figure 26). The device SDA pin is in the input mode at power-up.

All I^2C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The device continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (Figure 26). A START condition is ignored during the power-up sequence.

All I^2C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (Figure 26). A STOP condition at the end of a Read or Write returns the I^2C state machine to its initial state where it waits for the next START.

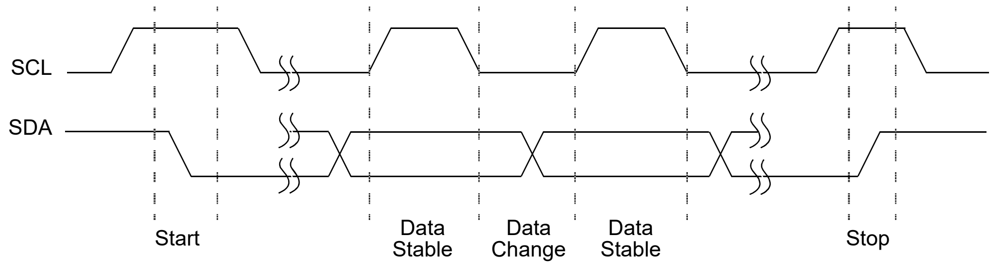


Figure 26. Valid Data, Start and Stop Conditions

An Acknowledge (ACK) is a software convention that indicates a successful data transfer. The transmitting device, either controller or target, releases the SDA line after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data as shown in Figure 27. The device responds with an ACK after recognition of a START condition followed by a valid Target Address byte, and once again after a successful receipt of the Register Address Byte. The device responds with an ACK after receiving each data byte of a write operation. The device indicates that the maximum number bytes have been received for a write packet by sending a NACK to the controller. The controller then sends a Stop bit to terminate the packet.

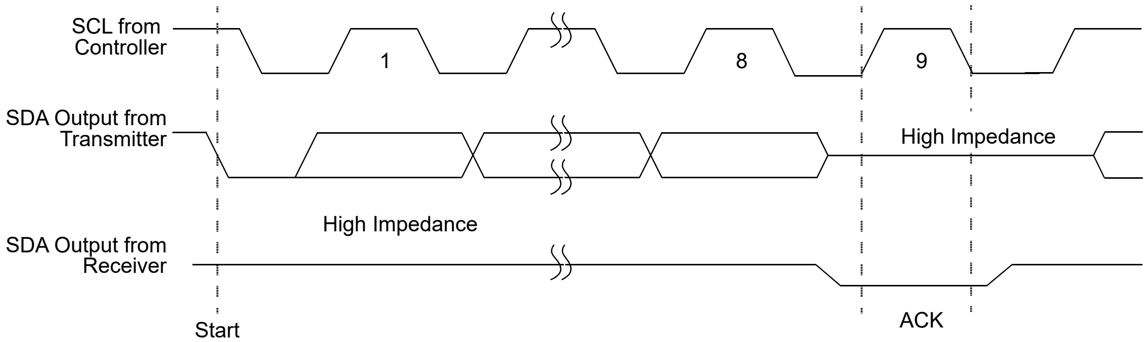


Figure 27. Ack from Receiver

For a read packet, the device sends an ACK after each byte sent by the controller. The controller sends an ACK bit following every byte transmitted by the device. The controller sends a NACK bit after the final read back byte. The target then sends a Stop bit to terminate the packet.

The last bit of the Target Address byte, referred to as the R/W bit, defines a read or write operation. When this bit is a 1, a Read operation is selected. A 0 selects a Write operation (Figure 29).

After loading the entire Target Address byte from the I²C bus, the device compares it with the internal Target Address. Upon a correct compare, the device outputs an acknowledge on the SDA line.

Other I²C specific timing is shown in Figure 28 below. See I²C Interface Specifications for values.

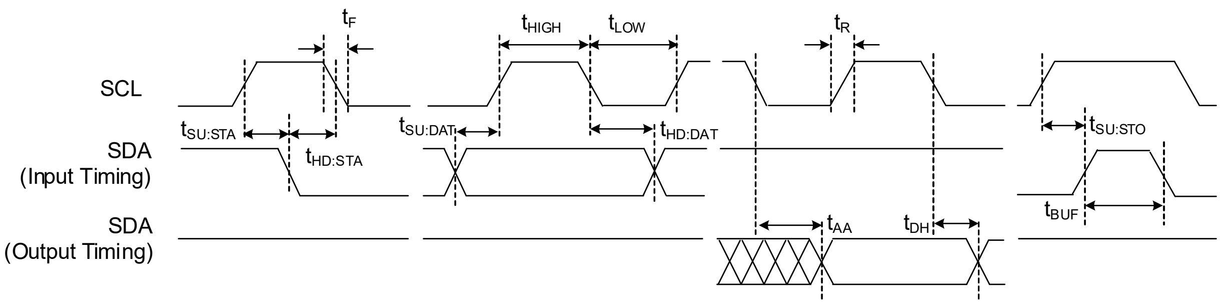


Figure 28. I²C Timing

7.4.1 Write Operation

A Write operation requires a START condition, followed by a Target Address byte, a Register Address byte, a word of Data, and a STOP condition (Figure 29). The target device responds with an ACK after successfully receiving each of the three bytes (or four bytes with CRC as in Figure 30). The content of the word of data is transferred to the device register at the rising edge of the SCL pin during the ACK and a successful comparison of the controller CRC byte versus the internally calculated CRC byte.

Target Address										Address Byte									Data Byte1									Data Byte2		
S	0	0	1	0	0	1	0	0	A	A07	A06	A05	A04	A03	A02	A01	A00	A	D07	D06	D05	D04	D03	D02	D01	D00	A	D15(msb) à D8	NA	P

Figure 29. I²C Write

Target Address										Address Byte									Data Byte1									Data Byte2		CRC Byte		
S	1	0	1	0	1	1	0	0	A	A07	A06	A05	A04	A03	A02	A01	A00	A	D07	D06	D05	D04	D03	D02	D01	D00	A	D15(msb) à D8	A	X8+X2+X1+1	NA	P

Figure 30. I²C Write with CRC

7.4.2 Read Operation

A Read operation consists of a 3-byte sequence, followed by one word of Data (Figure 31). The controller initiates the read operation by sending the following sequence of bits: a START bit, the Target Address byte with the R/W bit set to 0, a Register Address byte, a second START bit, and a second Target Address byte with the same seven MSBs but with the R/W bit set to 1. After each of the three bytes, the device responds with an ACK. The device transmits the word of Data (followed by a CRC byte as shown in Figure 32 if enabled) for as long as the controller responds with an ACK. The ACK bit occurs on the rising edge of the SCL pin for every 8 bits transmitted. The controller terminates the Read operation by issuing a NACK, and then a STOP condition.

The Data words received from the target are from the memory location indicated by an internal pointer. This initial value of the pointer is determined by the address byte in the Read operation instruction and increments by one during transmission of each word of data.

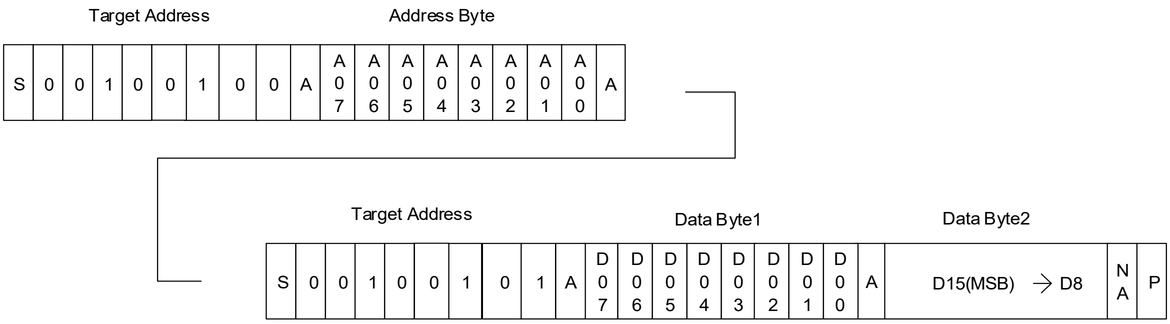


Figure 31. I²C Read

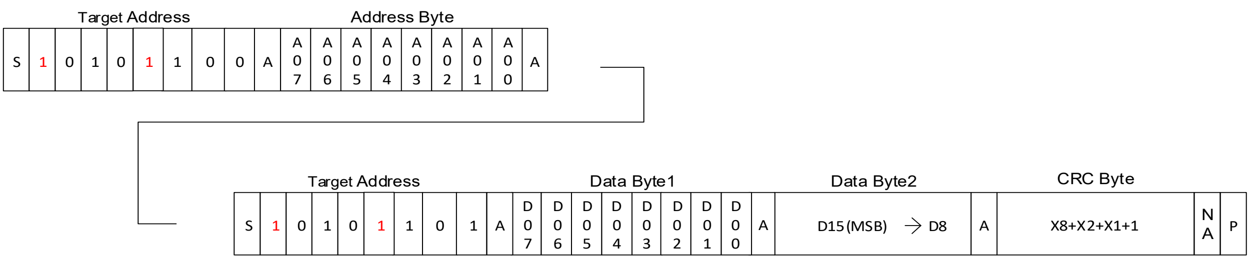


Figure 32. I²C Read with CRC

7.4.3 Command Codes

Command codes are block reads with register addresses to read back encoded into the device. Table 19 defines each command code and the registers that are read back, Byte Count and Read Time assume no CRC. The use of command codes is faster than individually reading each register.

A Fault and Status read command received by the device while the ALERT pin is latched results in the status bits clearing and unlatches the ALERT pin.

Table 19. Command Codes

Code	Command Read	Byte Count	Read Time at 400kbs (µs)	Data Registers Returned
0xC1	Fault and Status	3 + 4	202	Fault and Status (0x10, 0x11)
0xC2	All Measurements	3 + 22	757	VPACK, THERM1-2, Monitor Pos-Neg, VTEMP, VC1-VC5 (0x00, 0x03-0x06, 0x20-0x25)
0xC3	Monitor Pin	3 + 4	202	Monitor Neg and Monitor Pos (0x05, 0x06)
0xC4	Pack Voltages	3 + 12	449	VPACK, VC1-VC5 (0x00, 0x21-0x25)

Figure 33 and Figure 34 show the packet formats for command codes. The command codes support CRC. The CRC byte value is calculated from the value of each register word read back, the two target addresses and the command code. The calculation of the CRC is processed from the first target address byte to the final byte that is read back.

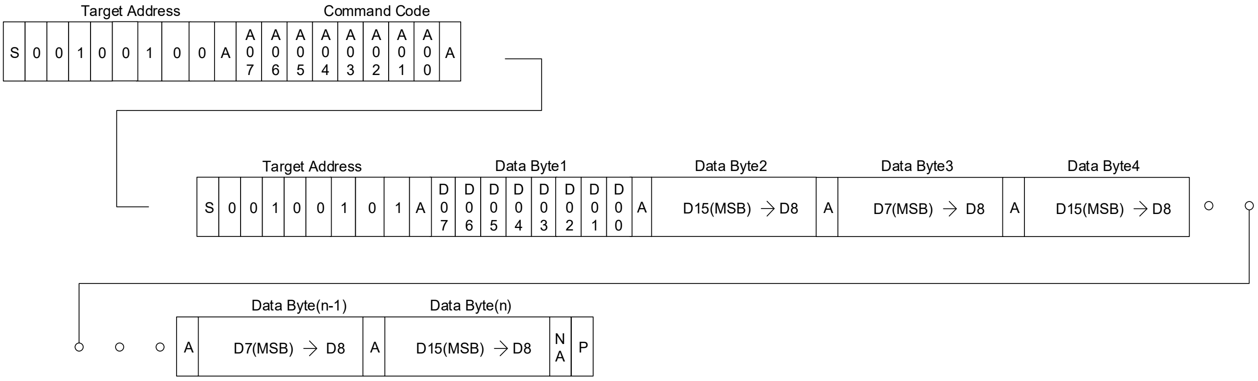


Figure 33. I²C Command Code

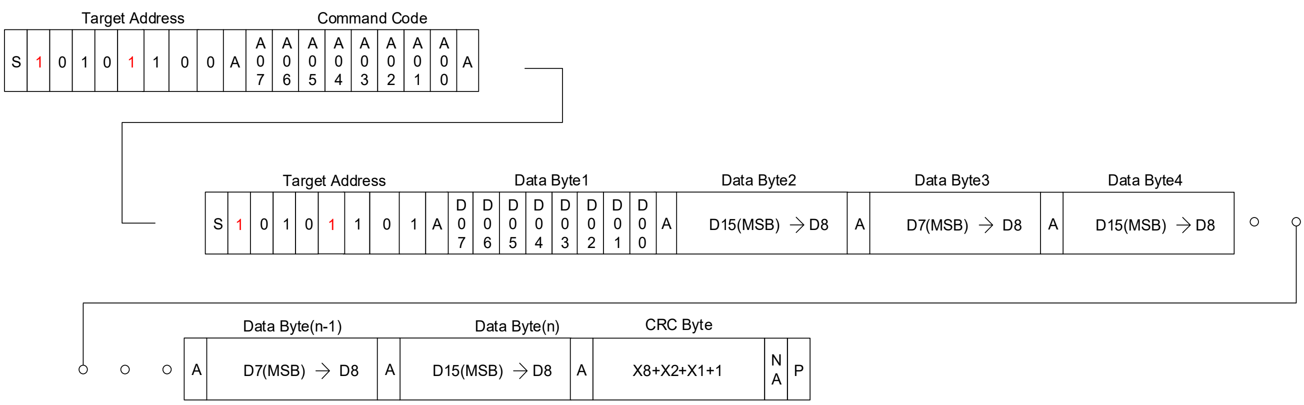


Figure 34. I²C Command Code with CRC

8. Detailed Pin Information

8.1 VCn Pins 1-6

The VCn pins are the voltage sense inputs of the device and are connected in pairs to differentially measure each cell voltage. Positive pin VCn and negative pin VCn-1 are connected to the ADC through a multiplexer. Each voltage sense input uses an external filter to protect against battery voltage transients. The basic input filter structure provides protection against transients and EMI for the cell inputs. They carry the loop currents produced by EMI and should be placed as close to the battery connector as possible. Place any vias in line to the signal inputs so that the inductance of these forms a low pass filter with the capacitors.

The filtered battery cell voltages internally connect to the cell voltage monitoring system. The monitoring system contains a multiplexer to select a specific input, and an analog to digital converter.

Figure 35 illustrates a typical VCn filter connection for the device. The differential capacitance (Cdiff) should be 0.1µf. The isolation resistance (RISO) should be 1kΩ. Using values greater than what is recommended may result in measurement accuracy errors or open connection test faults, lesser values could reduce Hot Plug tolerance.

Route the VC0 pin to the negative terminal of Cell 1 using a separate wire from the load/charge ground current path for best accuracy.

Route VC5 to the positive terminal of Cell 5 using a separate wire from the VPACK pin and load/charge current path for best accuracy.

The pin voltages are stored in registers 0x21-25 VCn Voltage.

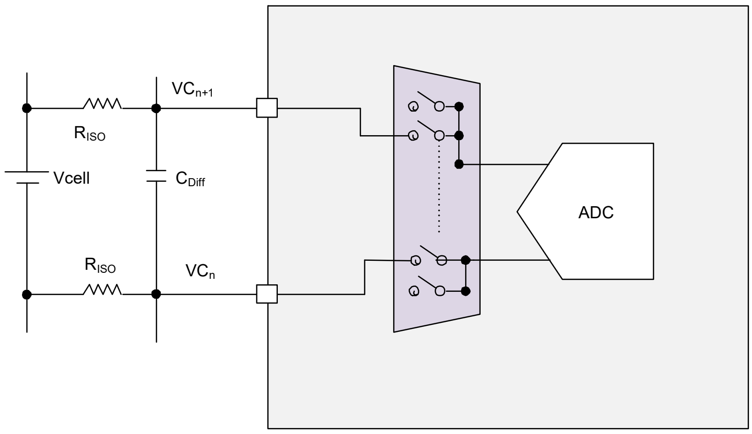


Figure 35. Voltage Sense Pin Connections

8.1.1 VCn Open Wire

The device performs an open-wire test by turning on a 275µA current source from the pin to VSS for each active VCn pin simultaneously. A VCn pin is active depending on the number of series cells the device is configured for. The current source on time is 10ms. After 7ms from turning on the pin current, the device performs a VCn scan to measure the cell voltages of the pack while current is being drawn from the pin. The cells are measured starting at cell 1 and proceeding to the top cell of the pack. If a cell reading measures below 0.6V (0x0058), an internal flag is set (0x10.14 OWF). The open-wire test must fail two times consecutively before the OWF bit is set 1. The open-wire test is performed in the Self Test Loop of the Single System Scan (detailed in Figure 22). The open-wire fault bit is set if any of the cell open-wire tests fail. To find the open-wire pin that failed, use the VCn pin current register (0x42.[4:0] VCn ISRC) to individually turn on the pin current source and trigger VCn/VPACK measurements. Figure 36 shows a simplified schematic for open-wire test.

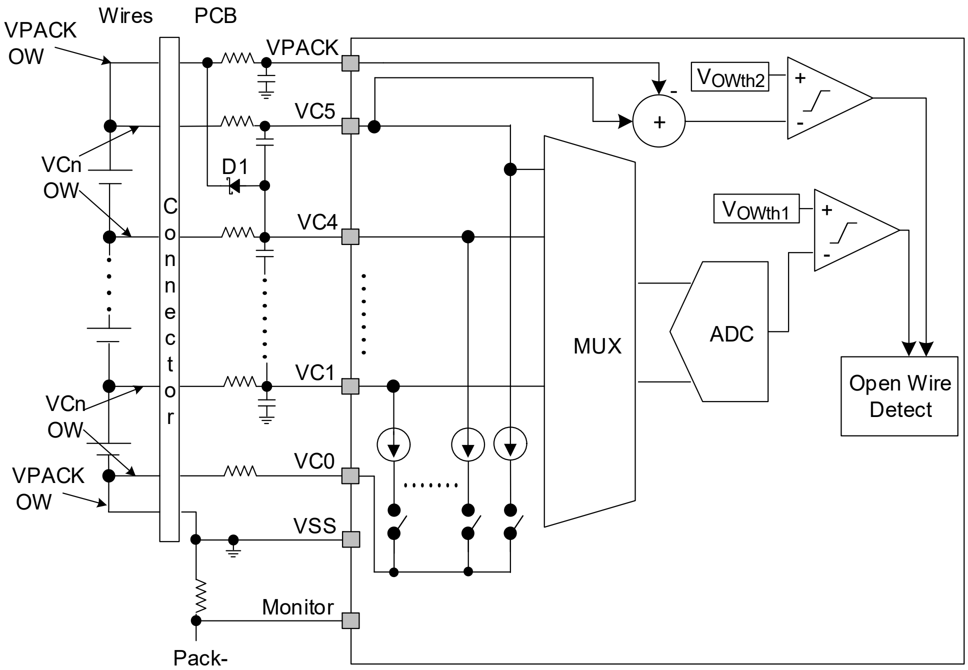


Figure 36. VCn/VPACK Open Wire

8.2 VPACK Pin 8

The VPACK pin is the power connection to the device. The pin is also the location at which the VPACK voltage measurement is made. Connect a series 10Ω resistor and a 10µF bypass capacitor to analog ground at the pin (Figure 36). The filter time constant for the VPACK pin should match the VCn pin filters.

The pin voltage is stored in register 0x00 Pack Voltage.

An open wire on VPACK removes power from the device forcing it into the RESET State unless Schottky D1 is included as shown in Figure 36. This diode provides an alternate supply current path to enable open-wire detection on this pin. Fault bit 0x10.7 VPACK OWF is set if the pin fails open-wire test during device Self Test.

8.3 HVGPIOn Pins 9-13

Five high voltage open-drain general purpose input/output digital pins are provided. These are useful for driving LEDs or Fuse blowing circuitry but can be used for application specific purposes. They are controlled by register 0x43.[5:0] HVPIOn Assert as outputs or accessed as inputs by reading 0x11.[15:10] HVGPIOn State. If these pins are not used for any purpose, then they can be left floating.

Fault register bit 0x10.9 HVGPIOF sets if an HVGPIOn pin is externally forced to a different state from the programmed pin state.

8.4 VINT Pin 15

The VINT pin is a connection to the internal 3.3V analog power supply. External connections must be limited to a decoupling capacitor to VSS. Connect a 4.7µF bypass capacitor to the analog ground plane.

The pin voltage is stored in register 0x04 THERM2 Voltage following a single triggered measurement, see 0x41.[4:0] Measurement Select and Other Voltages.

Fault bit 0x10.5 REGF is set if the pin voltage violates the Self Test thresholds.

8.5 V3P3 Pin 16

The V3P3 pin is the 3.3V regulator output. Connect a 10µF bypass capacitor to the analog ground plane (VSS). External loads can be connected but care must be taken to not overload the supply. This is especially important in Low Power Mode when the regulator may be in a “weak” setting (see 0x42.13 LP Reg).

The pin voltage is stored in register 0x04 THERM2 Voltage following a single triggered measurement, see 0x41.[4:0] Measurement Select and Other Voltages.

Fault bit 0x10.5 REGF is set if the pin voltage violates the Self Test thresholds.

8.6 V2P5 Pin 17

The V2P5 pin is the internal 2.5V digital power supply. External connections must be limited to a decoupling capacitor to DGND. This pin is for internal use only. Do not load or drive this pin from an external source. Connect a 1µF bypass capacitor to the digital ground plane.

The pin voltage is stored in register 0x04 THERM2 Voltage following a single triggered measurement, see 0x41.[4:0] Measurement Select and Other Voltages.

Fault bit 0x10.5 REGF is set if the pin voltage violates the Self Test thresholds.

8.7 DGND Pin 18

DGND is the digital ground reference pin for the device. It must have a solid connection to the digital ground plane. If separate digital and analog ground planes are used, connect them together at the VSS pins.

8.8 ALERT Pin 19

The ALERT pin is an active low open-drain digital output pin that indicates either a fault or status bit change has occurred. A pull-up of ~10kΩ to V3P3 or the MCU supply is recommended. This pin is high impedance while in LP Mode.

A change in state of the ALERT pin indicates: A Fault condition was detected, or the condition that caused the Fault has cleared, or the MCU reads the 0x10 Faults and 0x11 Status registers following a Fault detection. Figure 37 is an example of a fault condition clearing before the MCU reading Fault and Status registers resulting in two assertions of the Alert pin. Figure 38 is an example of a fault condition clearing after the MCU reading Fault and Status registers resulting in two assertions of the Alert pin. These figures demonstrate the necessity of reading the registers until the results align with the status of the Alert Pin.

All fault and status bits that are connected to ALERT pin are logically OR’d. A Status bit that has been masked prevents that bit from asserting the ALERT pin.

Pin status is in register bit 0x11.6 ALERT and the pin can be asserted for test with register bit 0x40.2 ALERT Assert. Register bit 0x10.15 ALRTF sets if the ALERT pin voltage is externally forced to a different state from the programmed pin state.

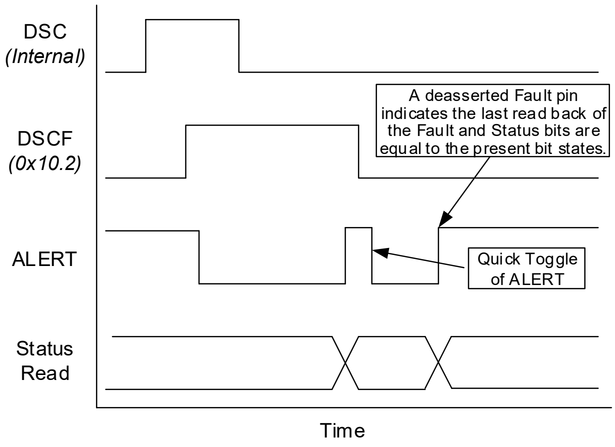


Figure 37. De-asserted Fault

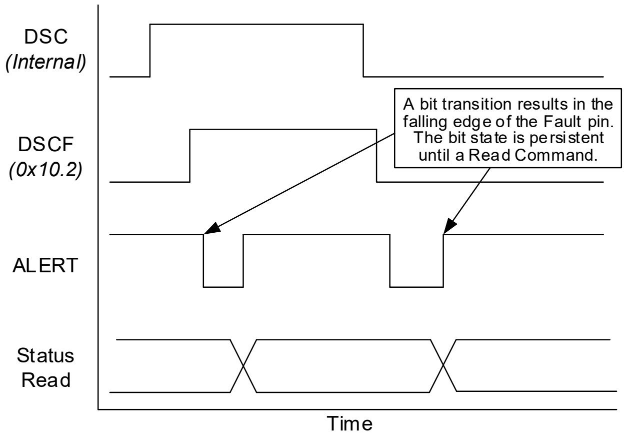


Figure 38. Persistent Fault

8.9 SCL Pin 20

The SCL pin is the clock input driven by the controller for I2C communications. Connect an optional 4.7kΩ (Min) pull-up resistor from the SCL pin to V3P3 to ensure it is pulled high in LP Mode so the wakeup with communication feature functions properly. If the MCU has a push-pull output and ensures this is high, then the resistor can be omitted to save power.

8.10 SDA Pin 21

The SDA pin is the serial data line for bidirectional I2C communications between controller and target. It is driven by the controller for sending the target address bytes and for the read commands. In this Mode, the device pin is an open drain. The pin is driven by the target for data reads. Connect a 4.7kΩ (Min) pull-up resistor from the SDA pin to V3P3.

8.11 THERM2, VTEMP, THERM1 Pins 22-24

The THERMn pins (22, 24) are analog voltage inputs that connect to the external thermistor circuitry. These pins are optimized to work with external NTC thermistors to monitor the temperature of the battery pack. The thermistors are biased by the VTEMP output pin (23), as shown in Figure 39.

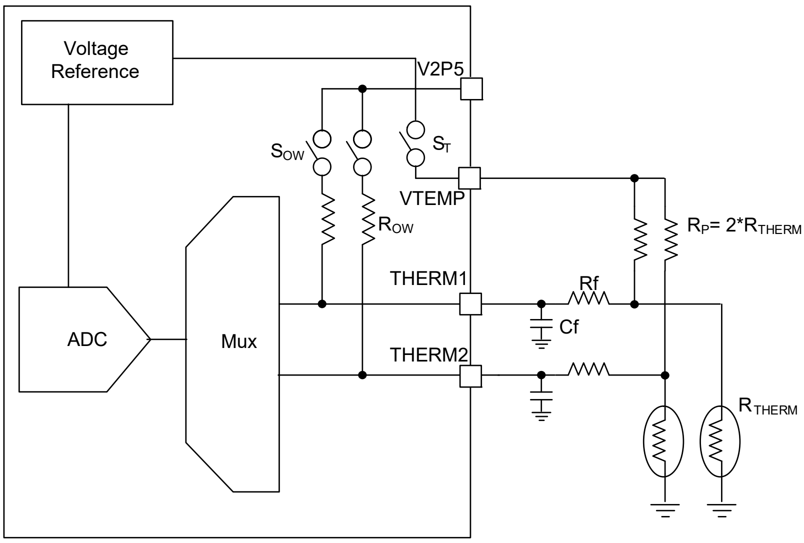


Figure 39. Thermistor Configuration

The Thermistor inputs are sampled as part of a Single System Scan (detailed in Figure 22). Before measuring the thermistors, the internal switch ST is closed, connecting the two pull-up resistors RP through the VTEMP pin to the reference voltage. This sets up a pair of voltage dividers consisting of RP and RTHERM. The voltage between these resistors is a function of the temperature. From the thermistor, an optional low-pass filter consisting of Rf and Cf connects to each THERMn input. Each of these inputs is then measured in sequence relative to VSS. Switches SOW are used for Open-Wire test as part of the Self Test Loop.

Following a Single System Scan, the relevant voltages are stored in registers 0x03 THERM1 Voltage, 0x04 THERM2 Voltage, and 0x20 VTEMP Voltage. These voltages are also accessible by triggering the measurements individually with 0x41.[4:0] Measurement Select.

Bit 0x10.12 VTMPF is set when the measured VTEMP voltage exceeds the digital thresholds (Self Test).

8.11.1 RESET and THERM2

A hard reset is initiated by connecting the THERM2 pin above the reset threshold voltage RST_{Vtherm} for t_{RESET} time. The Reset voltage threshold is defined with respect to (above) the voltage on the V2P5 pin. A switch with terminals connecting the THERM2 and the V3P3 pin is used on the evaluation boards. The Reset state is exited t_{RST_Exit} time after the falling edge on THERM2 pin occurs.

8.11.2 THERMn Open-Wire Test

The thermistor pins are tested for open wires in the Self Test Loop of a Single System Scan. If the measured result exceeds threshold OWVtherm for two consecutive tests, the device sets the relevant bit 0x10.1 THERM2 OWF or 0x10.0 THERM1 OWF to 1. The thermistor and resistor divider network as shown in Figure 39 must be chosen to remain below the Open Wire threshold over the range of operation.

8.12 HVGPIO5 Pin 25

The High Voltage General Purpose Input/Output 5 digital pin functions the same as the HVGPIOn Pins 9-13 plus extra features. A rising edge transition of the HVGPIO5 pin voltage through ~1.25V ($HVGPIO5_W$) wakes the device from LP Mode and sets bit 0x11.1 HVGPIO5 Wakeup. The device has a factory selectable option to invert this function to a falling edge detect. Tie this pin to VSS when 0x11.1 HVGPIO5 Wakeup feature is not used.

If bit 0x80.7 HVGPIO5 BUSY En is cleared, bit status 0x11.7 BUSY is output (inverted) on HVGPIO5. This allows the MCU to determine when new measurement results are available.

HVGPIO5 is controlled by register 0x43.[5:0] HVPIOn Assert as an output or accessed as an input by reading 0x11.[15:10] HVGPIOn State.

Note: The device disables all HVGPIO outputs when it transitions to LP Mode. If HVGPIO5 is asserted low before the transition to LP Mode, the pin voltage rises to the pull-up voltage and can trigger the device to wake up.

8.13 TRIGGER Pin 27

A rising edge transition of the Trigger Pin voltage through ~1.5V (VTrThr) wakes the device from LP Mode and sets bit 0x11.3 Trigger Wakeup. The device has an option to invert this function to a falling edge detect with bit 0x85.0 Trigger Pol. Connect this pin using a 10kΩ resistor.

8.14 MONITOR Pin 29

The Monitor Pin wakes the device from LP Mode with a detection of current flow. This is configured using 0x85.[15:14] Current Wakeup Threshold and 0x85.[13:12] Current Wakeup Delay. Connect the monitor pin using a 1kΩ resistor to the side of the current-sense resistor that is not tied to ground for detection of current flow.

The voltage on this pin is measured and stored in 0x05 Monitor NEG Voltage and 0x06 Monitor POS Voltage following a Single System Scan or a triggered single measurement (Measurement Selection).

8.15 VSS Pins 31-32

VSS is a device analog ground. It must have a solid connection to the ground plane(s). Connect the digital and analog ground planes together as close to the VSS pins as possible. Connect the Exposed Pad (EPAD) on the bottom of the device to VSS as well.

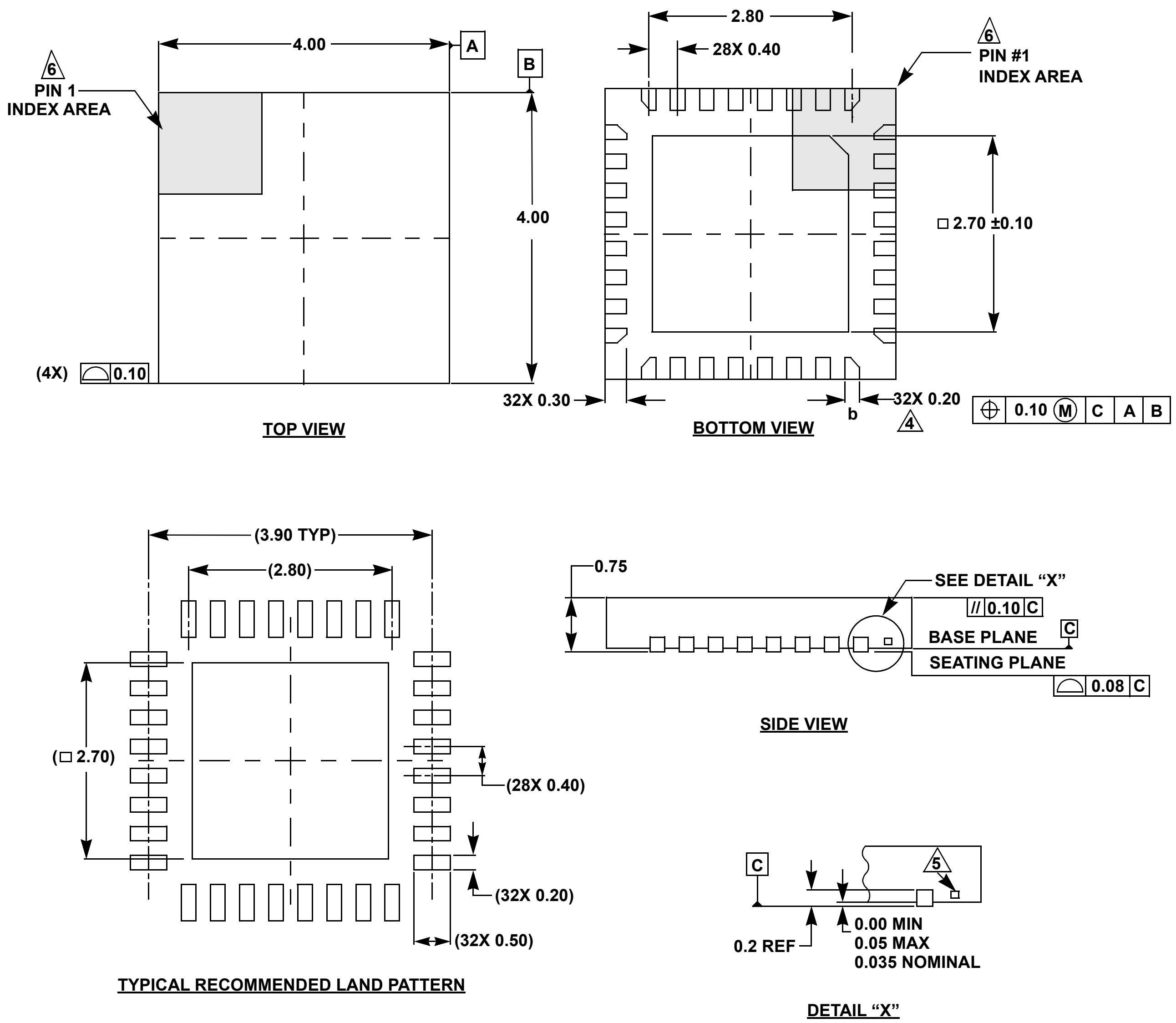
8.16 EPAD

Connect the Exposed Pad (EPAD) on the bottom of the device to analog ground. Never connect the exposed pad to any other node than VSS. Multiple vias are recommended for good thermal conductivity. The PCB footprint should always have an EPAD landing even if the pad is floating. Soldering to the EPAD provides mechanical stability.

9. Package Outline Drawing

For the most recent package outline drawing, see L32.4x4G.

L32.4x4G
32 Lead Thin Quad Flat No-Lead Plastic Package
Rev 0, 11/18



NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ±0.05.
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.25mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

10. Ordering Information

Part Number[1][2]	Part Marking	Package Description[3] (RoHS Compliant)	Pkg. Dwg. #	Carrier Type [4]	Temp Range
RAA4892553GNP#AA5	489255 03GNP	32 LD 4x4 QFN	L32.4x4G	Tube	-40 to +85°C
RAA4892553GNP#HA5				Reel, 6k	
RAA4892553GNP#MA5				Reel, 1k	
RTKA489255DE0000BU	Evaluation Board				

1. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. For Moisture Sensitivity Level (MSL), see the RAA489255 device page. For more information about MSL, see TB363.
3. For the Pb-Free Reflow Profile, see TB493.
4. See TB347 for details about reel specifications.

Table 20. Key Differences Between Family of Parts[1]

Part #	Cells Supported		Pack Voltage (Op)		Cell Bal.	I_{PACK} Sense	Fuel Gauge	Charge/ Discharge FET		Supply Current (µA)		Stand Alone	Int. MCU	Int. ADC	Daisy Chain
	Min	Max	Min (V)	Max (V)				Ctrl	Loc.	Norm.	Sleep				
RAA489255	3	5	6	27	N	N	N	N	N/A	20	2	N	N	12-bit	N
RAJ240100 /090	3	10/8	4	50	B	Low Side	Y	Y	High Side	50	1	Y	Y	18-bit	N
RAJ24080	2	5	4	25	B	Low Side	Y	Y	High Side	50	1	Y	Y	18-bit	N
RAA489206	4	16	12	59	B	Low Side	N	Y	Both	200	10	N	N	16-bit	N
ISL94208	4	6	8	27	B	Low Side	N	Y	Low Side	850	2	N	N	N	N
ISL94202	3	8	4	36	Ext.	High Side	N	Y	High Side	348	13	Y	N	12-bit	N

1. Int. = Internal, B = Both, Norm. = Normal, Bal. = Balance, Crtl = Control, Loc. = Location, Y = Yes, N = No

11. Revision History

Revision	Date	Description
1.01	Jun 6, 2025	Updated the VTEMP Voltage Accuracy minimum and typical values. Updated the V3P3 Voltage Accuracy minimum value.
1.00	Sep 27, 2024	Initial release.

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