RAA489000

Buck-Boost Configurable Battery Charger with USB Power Delivery and USB Type-C® Port Controller Interface (TCPCI)

The RAA489000 is a digitally configurable buck-boost battery charger with USB-C® Port Controller (TCPC). The battery charging function supports Narrow Voltage Direct Charging (NVDC) and USB Power Delivery (PD) programmable power supply output supplies. The TCPC controller integrates TCPC PHY, CC-Logic, and VCONN switches. All RAA489000 blocks connected to the adapter/USB pin (CC1, CC2, VBUS) are protected from input overvoltage events up to 28V. The back-to-back NFET driver and VBUS self-discharge control further simplify the USB PD designs. The RAA489000 supports reverse buck, boost, or buck-boost operation to the adapter/USB port from 2- to 4-cell batteries to allow configurations to support USB PD output for Programmable Power Supply (PPS) ports. Thanks to the on-chip TCPC and Renesas advanced R3™ Technology, RAA489000 is fully compliant with USB PD Sink Fast Role Swap (FRS) spec by monitoring CC line and bringing VBUS voltage back to a safe range rapidly. The RAA489000 has dual SMBus/I2C ports supporting simultaneous direct charger function programming and CC line traffic through TCPCI when operating with a USB-C Port Manager (TCPM) such as the Renesas R9A02G015 to form a complete USB PD compliant solution for single-port or multi-port applications. The RAA489000 battery charger supports all NFETs solution and supports system power from the adapter, battery, or a combination of both. The on-chip ADC monitors the charging input voltage/current, battery voltage, charging/discharging current, and the battery temperature. For Intel™ IMVP compliant systems, the RAA489000 includes PROCHOT#.

Features

- Buck-Boost NVDC charger for 2-, 3-, or 4-cell Li-ion batteries using all NFET transistors
- USB-C Port Controller (TCPC) with integrated TCPC PHY, CC-Logic
- Dual SMBus/I2C ports for charger programming and CC line traffic
- Internal 500mΩ VCONN MUX for up to 1.6A
- Input voltage range: 3.9V to 23.4V (no dead zone)
- System/battery output voltage: 3.9V to 18.304V
- 28V protection for CC1/CC2/VBUS
- Adapter Crash Prevention with adapter current and battery current regulation
- PROCHOT#, IMVP compliant
- Internal 8-bit ADC for charger operation telemetry
- Software configurable for DFP, UFP, or DRP
- USB-C PD Sink Fast Role Swap (FRS) and PPS support
- Pass-Through-Mode (PTM) in forward direction
- Battery Ship Mode - IC ultra-low power state
- Supports JEITA compliance autonomous charge
- Dynamic Voltage Compensation (DVC) support for multi-port charging applications
- USB Power Delivery (PD) 3.0 and Programmable Power Supply (PPS) Certified
- 5x5 40 Ld QFN package
- UL 2367, IEC 62368-1: File No. E520109

Applications

- Multi-cell tablets, notebooks, ultrabook, power bank
- Multi-Port USB-C applications with batteries

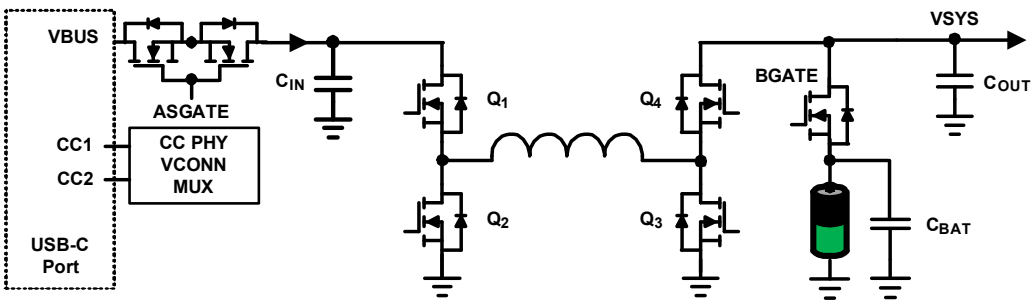


Figure 1. Typical Application

Contents

1. Overview

1.1 Simplified Application Circuits

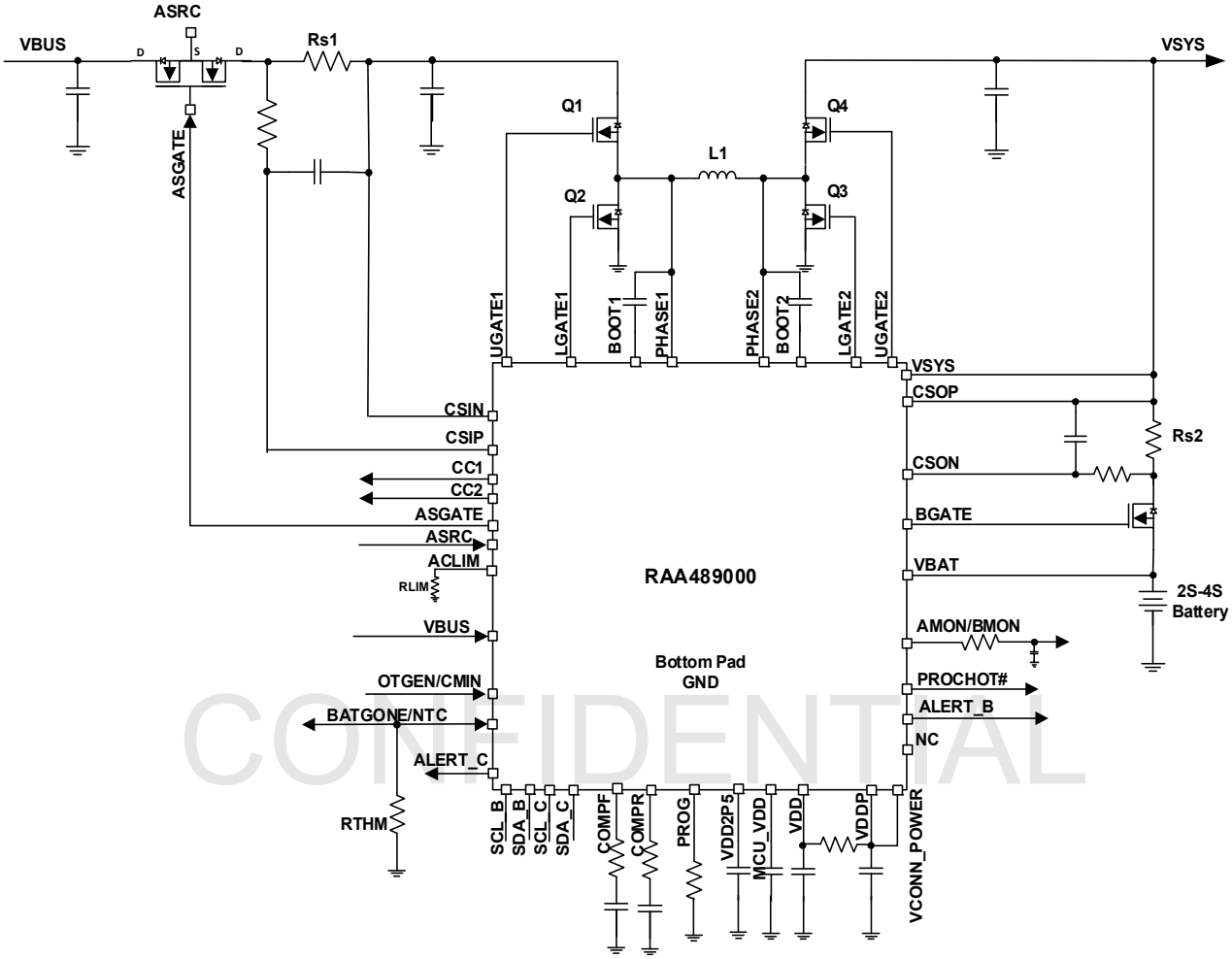


Figure 2. RAA489000 Simplified Application Diagram

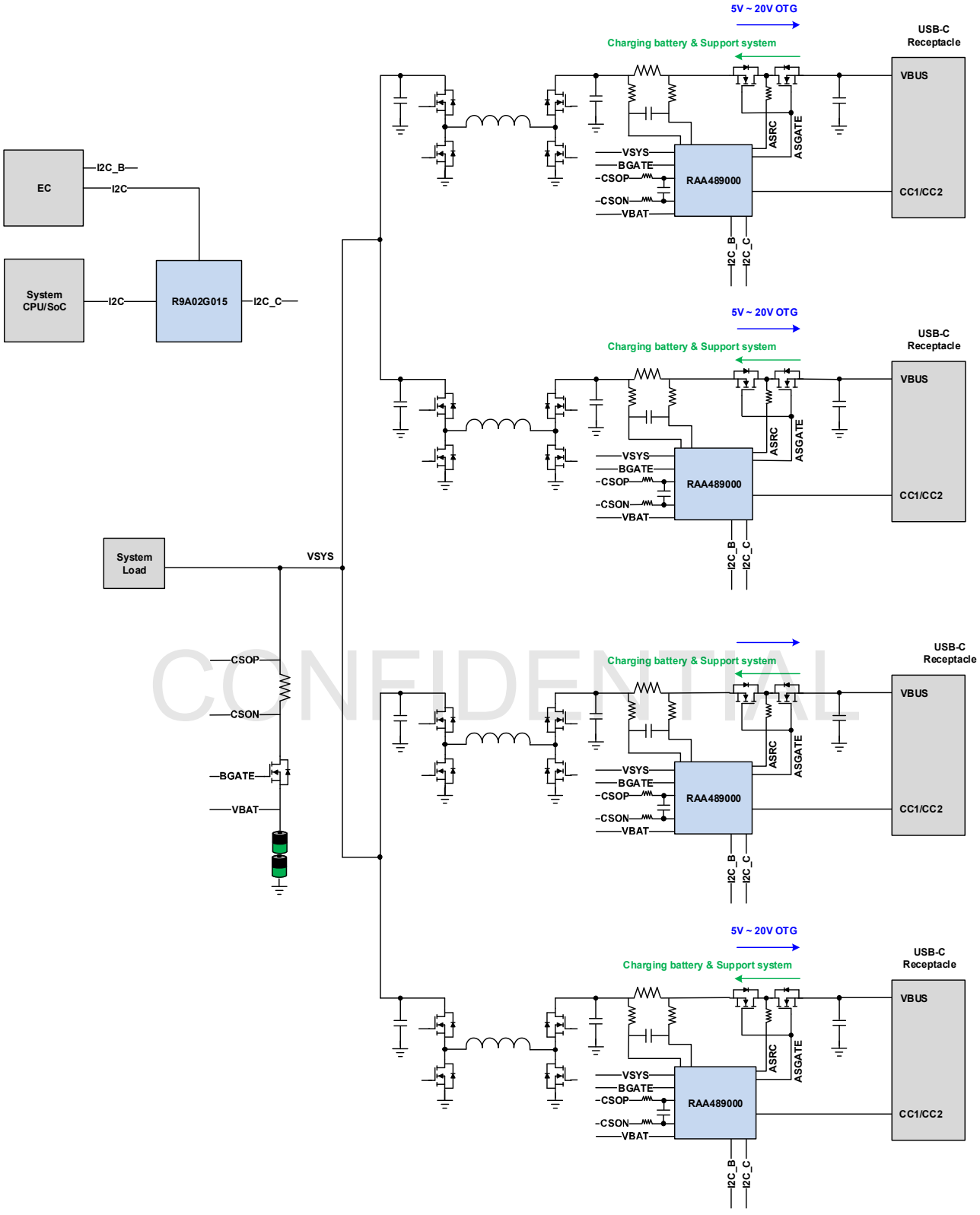


Figure 3. 4-Port USB-C Application Diagram with RAA489000, R9A02G015, and EC

1.2 Block Diagram

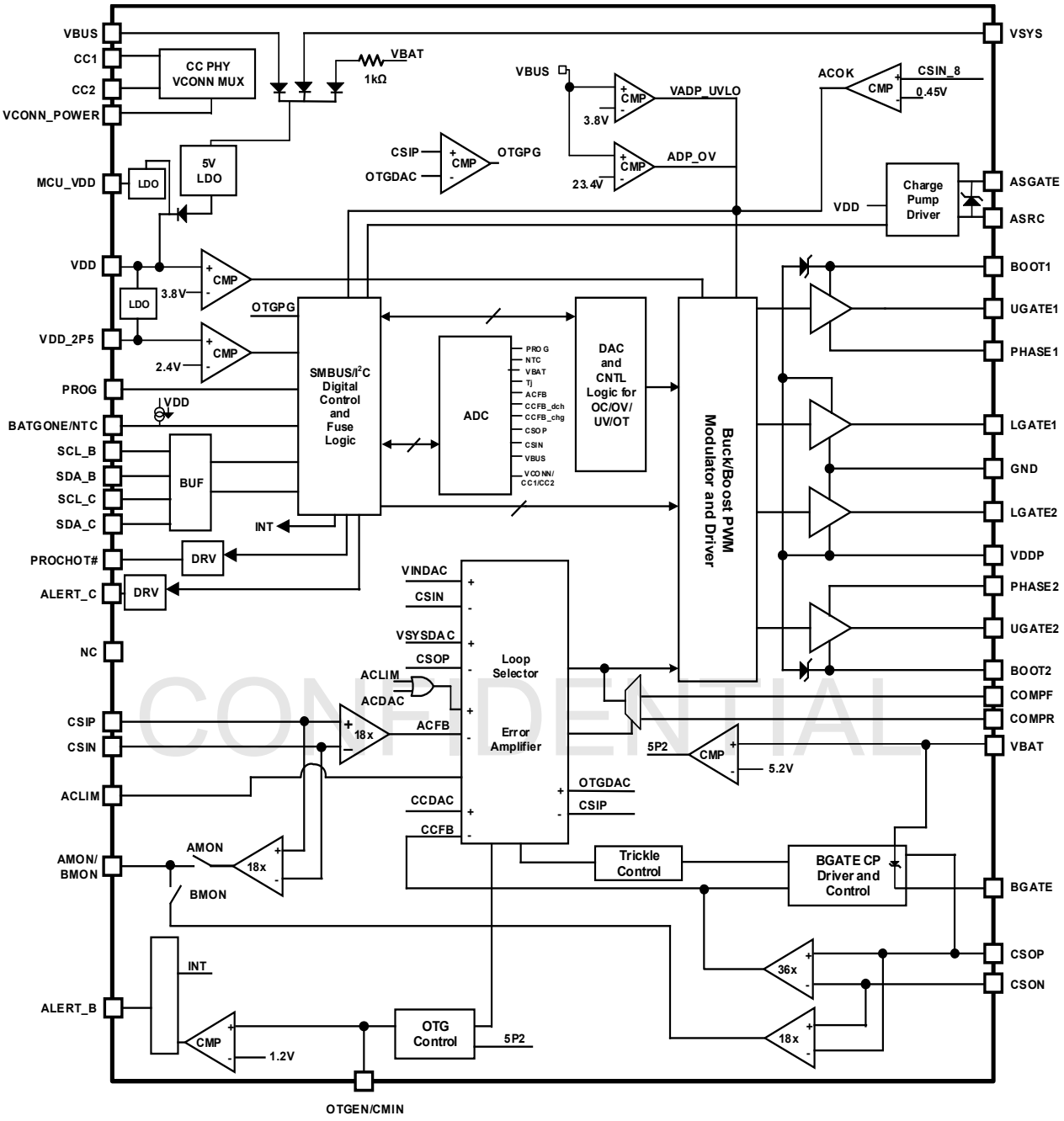
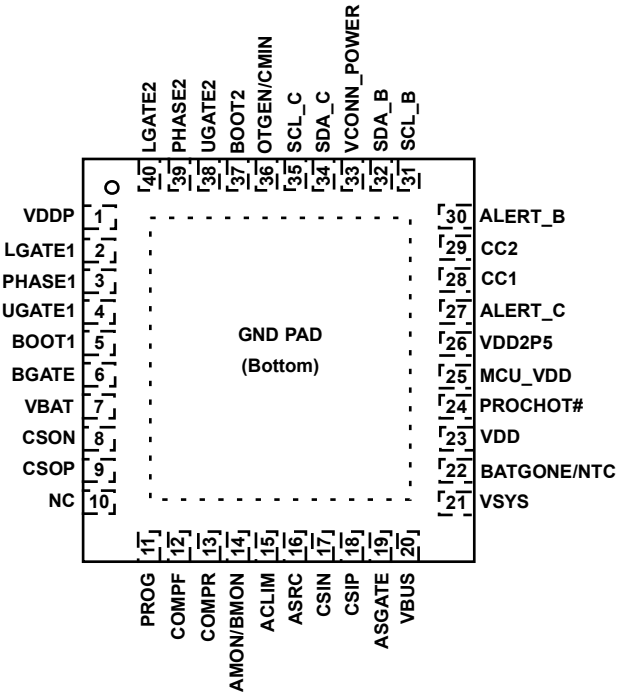


Figure 4. Block Diagram

Note: I2C address for CC line communication and charging commands are paired.

2. Pin Information

2.1 Pin Assignments



Top View

2.2 Pin Descriptions

Pin Number	Pin Name	Description
Bottom Pad	GND	Signal common to the IC. Unless otherwise stated, signals are referenced to the GND pin. Use the bottom pad as the thermal pad for heat dissipation.
1	VDDP	Power supply for the gate drivers. Connect VDDP to the VDD pin through a resistor and connect a ceramic capacitor to GND. The capacitor must have an effective capacitance higher than 0.4µF at 5V and x1.6 effective capacitance at the Boot pin at 5V.
2	LGATE1	Low-side MOSFET Q_2 gate drive.
3	PHASE1	Current return path for the high-side MOSFET Q_1 gate drive. Connect PHASE1 to the node consisting of the high-side MOSFET Q_1 source, the low-side MOSFET Q_2 drain, and the inductor input terminal.
4	UGATE1	High-side MOSFET Q_1 gate drive.
5	BOOT1	High-side MOSFET Q_1 gate driver supply. Connect an MLCC capacitor across the BOOT1 and PHASE1 pins. The boot capacitor is charged through an internal boot diode connected from the VDDP to BOOT1 pins when the PHASE1 pin drops below VDDP minus the voltage drop across the internal boot diode. The bootstrap capacitor must have an effective capacitance higher than 0.25µF at 5V and x50 effective high-side MOSFET gate capacitance.
6	BGATE	Battery Gate drive output to the N-channel MOSFET connecting the system and the battery. When BGATE turns on, it is pumped 5V above the VBAT input pin voltage.
7	VBAT	Battery voltage sensing. Used for trickle charging detection, Ideal Diode mode control, and as a charge pump reference for BGATE. Input to the HV selector for LDO power with a series 1kΩ resistor. Connect an optional ceramic capacitor >1µF from VBAT to GND.

Pin Number	Pin Name	Description
8	CSON	Battery current sense – input. Connect to the battery current resistor negative input. Place a ceramic capacitor between CSOP and CSON to provide Differential mode filtering.
9	CSOP	Battery current sense + input. Connect to the battery current resistor positive input. Place a ceramic capacitor between CSOP and CSON to provide Differential mode filtering. Input for sensing VSYS regulation to maximum system voltage and phase comparator.
10	NC	No connect. Reserved for future use.
11	PROG	A resistor from the PROG pin to GND sets the following configurations: ▪ Default number of battery cells in series ▪ Default SMBus/I^2C addresses ▪ Default adapter current limit value
12	COMPF	Error amplifier output for Forward/Charging mode. Connect a compensation network externally from COMPF to GND.
13	COMPR	Error amplifier output for Reverse/OTG mode. Connect a compensation network externally from COMPR to GND.
14	AMON/BMON	Adapter current, Reverse output current, battery charging current, or battery discharging current monitor output. ▪ V_{AMON} = 18x (V_{CSIP} - V_{CSIN}) for adapter current monitoring ▪ $V_{OTGCMON}$ = 18x (V_{CSIN} - V_{CSIP}) for OTG output current monitoring ▪ $V_{BMON\_DISCHARGING}$ = 18x (V_{CSON} - V_{CSOP}) for battery discharging current monitoring ▪ $V_{BMON\_CHARGING}$ = 36x (V_{CSOP} - V_{CSON}) for battery charging current monitoring Add an RC filter from the AMON pin to ground. Filter value (4.5kΩ resistor and 220nF capacitor).
15	ACLIM	The voltage on this pin sets the hardware-based adapter current limit. The lower value of the hardware-set adapter current limit and the SMBus set adapter current limit is the actual limit of the adapter current. The hardware-based adapter current limit also sets the regulated inrush current level for ASGATE MOSFET protection. The hardware-based current limit works in both forward and reverse directions.
16	ASRC	N-channel MOSFET source input reference for ASGATE/PD FETs.
17	CSIN	Input for sensing input voltage and phase comparator. Connect to the input current sense resistor negative input. Also used for sensing Q_1 drain for the modulator and VIN in forward-modes and VOUT for the modulator in reverse-modes. Use a Kelvin line between the voltage sense point and CSIN.
18	CSIP	Connect to the input current sense resistor positive input through a resistor. Place a ceramic capacitor between CSIP and CSIN to provide differential-mode filtering.
19	ASGATE	Gate drive output of the N-channel system back to back MOSFETs. When ASGATE is turned on it is pumped 5V above ASRC.
20	VBUS	Input to the HV selector for LDO power.
21	VSYS	Input to the HV selector for LDO power.
22	BATGONE/NTC	Input pin to the IC. Logic high on this pin indicates the battery has been removed. Logic low on this pin indicates the battery is present. BATGONE pin logic high (pull up to VDD) forces the BGATE FET to turn off in any circumstances. A current source on this pin pulls it high if open, but if a battery is present with an NTC to GND (10kΩ at +25°C thermistor), the NTC resistor pulls down on the pin, indicating a battery is present. The pull-up current source is then used to generate a voltage on the NTC that is measured by the part to determine temperature. If NTC and BATGONE are disabled, this pin can be used as a general ADC input. For any pin that is hot-plugged (such as BATGONE/NTC), a 10kΩ resistor is required to reduce any negative voltage on the pin.

Pin Number	Pin Name	Description
23	VDD	Output of the internal LDO; provides the bias power for the internal analog and digital circuit. Connect a ceramic capacitor to GND. If VDD is pulled below 2V, the RAA489000 resets all the SMBus register values to the default. The capacitor must have an effective capacitance higher than 0.4µF at 5V and x1.6 effective capacitance at the Boot pin at 5V.
24	PROCHOT#	Open-drain output. Pulled low when ACHOT, DCHOT, or Low_VSYS are detected. IMVP compliant. SMBus commands are available to pull low with OTGHOT, BATGONE, ACOK, and the general-purpose comparator.
25	MCU_VDD	Output for the 3.3V LDO to supply an external MCU or internal analog/digital circuitry. Connect a ceramic capacitor to GND. The effective capacitance of MCU_VDD capacitor should be at least 1µF at 3.3V.
26	VDD2P5	Output of the internal LDO; provides the bias power for the internal digital logic and TCPC transmitter. Connect a ceramic capacitor to GND. The effective capacitance of VDD2P5 capacitor should be at least 1µF at 2.5V. Do not apply additional load on the VDD2P5 pin.
27	ALERT_C	Interrupt line for the TCPC, SDA_C and SCL_C
28	CC1	Type C input communication lines, or output VCONN supply lines.
29	CC2	
30	ALERT_B	Open-drain output. Interrupt function output or the stand-alone comparator output. When configured, it is the interrupt for several functions. Must read status register flags to clear. The interrupt pin goes low when interrupt conditions are detected. When the interrupt function is disabled, the pin is used as a general purpose comparator output (if enabled).
31	SCL_B	SMBus clock I/O. Connect to the clock line from the host controller or smart battery. Connect a 1.2k pull-up resistor according to the SMBus specification.
32	SDA_B	SMBus data I/O. Connect to the data line from the host controller or smart battery. Connect a 1.2k pull-up resistor according to the SMBus specification.
33	VCONN_POWER	Input to the VCONN MUX providing power to the CCx lines. Bypass this pin with an MLCC capacitor.
34	SDA_C	SMBus data I/O. Connect to the data line from the host controller for TCPCi. Connect a 1.2k pull-up resistor according to the SMBus specification.
35	SCL_C	SMBus clock I/O. Connect to the clock line from the host controller for TCPCi. Connect a 1.2k pull-up resistor according to the SMBus specification.
36	OTGEN/CMIN	Input pin. OTG function enable pin, stand-alone comparator input pin. When the OTG function is enabled and the general purpose comparator is disabled, pulling this pin high can activate the OTG function. When the general purpose comparator is enabled, this pin is the general purpose comparator input.
37	BOOT2	High-side MOSFET Q_4 gate driver supply. Connect an MLCC capacitor across the BOOT2 and PHASE2 pins. The boot capacitor is charged through an internal boot diode connected from the VDDP to BOOT2 pins when the PHASE2 pin drops below VDDP minus the voltage drop across the internal boot diode. The bootstrap capacitor must have an effective capacitance higher than 0.25µF at 5V and x50 effective high-side MOSFET gate capacitance.
38	UGATE2	High-side MOSFET Q_4 gate drive.
39	PHASE2	Current return path for the high-side MOSFET Q_4 gate drive. Connect this pin to the node consisting of the high-side MOSFET Q_4 source, the low-side MOSFET Q_3 drain, and the one terminal of the inductor.
40	LGATE2	Low-side MOSFET Q_3 gate drive.

3. Specifications

3.1 Absolute Maximum Ratings

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
ASGATE	-0.3	+33	V
CC1, CC2, ASRC, CSIN, CSIP, VBUS	-0.3	+28	V
PHASE1	GND - 0.3	+28	V
PHASE1 (<20ns)	GND - 2	+28	V
PHASE2	GND - 0.3	+24	V
PHASE2 (<20ns)	GND - 2	+24	V
BOOT1, UGATE1	GND - 0.3	+33	V
BOOT2, UGATE2	GND - 0.3	+29	V
(UGATE1 - PHASE1), (UGATE2 - PHASE2)	-0.3	BOOT	V
(UGATE1 - PHASE1), (UGATE2 - PHASE2) (<20ns)	-2	BOOT + 2	V
LGATE1, LGATE2	GND - 0.3	+6.5	V
LGATE1, LGATE2 (<20ns)	GND - 2	+6.5	V
VSYS, VBAT, CSOP, CSON	-0.3	+24	V
VDD, VDDP, MCU_VDD, VCONN_POWER	-0.3	+6.5	V
COMPF, COMPR	-0.3	+6.5	V
BGATE	-0.3	+29	V
AMON/BMON, ACLIM, PROG	-0.3	+6.5	V
OTGEN/CMIN, BATGONE/NTC	-0.3	+6.5	V
ALERT_B, ALERT_C, PROCHOT#	-0.3	+6.5	V
(BOOT1 - PHASE1), (BOOT2 - PHASE2)	-0.3	+6.5	V
(ASGATE - ASRC), (BGATE - VBAT)	-0.3	+6.5	V
(CSIP - CSIN), (CSOP - CSON)	-0.5	+0.5	V
SDA_B, SCL_B, SDA_C, SCL_C	-0.3	+6.5	V
SDA_B, SCL_B, SDA_C, SCL_C, ALERT_B, ALERT_C, PROCHOT#		4	mA
VDD2P5	-0.3	3	V
ESD Ratings	**Value**		**Unit**
Human Body Model (Tested per JS-001-2017)	2		kV
Charged Device Model (Tested per JS-002-2014)	1		kV
Machine Model (Tested per JESD22-A115C)	200		V
Latch-Up (Tested per JESD78E; Class 2, Level A)	100		mA

3.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)[1]	θ_{JC} (°C/W)[2]
40 Ld TQFN Package	37	2

1. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
2. For θ_{JC}, the case temperature location is the center of the exposed metal pad on the package underside.

Parameter	Minimum	Maximum	Unit
Junction Temperature Range (T_J)	-40	+125	°C
Storage Temperature Range (T_S)	-65	+150	°C
Pb-Free Reflow Profile	see TB493		

3.3 Recommended Operation Conditions

Parameter	Minimum	Maximum	Unit
Ambient Temperature			
RAA489000ARGNP	-10	+100	°C
RAA489000A3GNP	-40	+105	°C
Junction Temperature	-10	+125	°C
Adapter Voltage	+5	+23	V

3.4 Electrical Specifications

Operating conditions: V_{BUS} = CSIP = CSIN = 5V and 20V, V_{SYS} = V_{BAT} = CSOP = CSON = 8V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -10°C to +125°C unless otherwise specified.**

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
UVLO/ACOK						
VADP (CSIN) ACOK threshold	VADP_ACOK_r	CSIN = V_{adp}	**3.5**	3.6	**3.7**	V
VADP (CSIN) ACOK hysteresis	VADP_ACOK_h			350		mV
VBUS OK Rising	VBUS_OK_r		**3.73**	3.84	**4.0**	V
VBUS OK Hysteresis	VBUS_OK_h			300		mV
VBAT 5P2V Rising	VBAT_5P2_r		**4.95**	5.2	**5.65**	V
VBAT 5P2V Hysteresis	VBAT_5P2_h			450		mV
VDD2p5 2P4 POR Rising[2]	VDD2p5_2P4_r	SMBus and BGATE/BMON Active	**2.3**	2.4	**2.5**	V
VDD2p5 2P4 POR Hysteresis[2]	VDD2p5_2P4_h			125		mV
VDD 2P7 POR Rising	VDD_2P7_r		**2.5**	2.7	**2.9**	V
VDD 2P7 POR Hysteresis	VDD_2P7_h			100		mV
VDD 3P8 POR Rising	VDD_3P8_r	Modulator and Gate Driver Active	**3.6**	3.8	**4**	V

Operating conditions: V_{BUS} = CSIP = CSIN = 5V and 20V, V_{SYS} = V_{BAT} = CSOP = CSON = 8V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -10°C to +125°C unless otherwise specified.** (Cont.)

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
VDD 3P8 POR Hysteresis	VDD_3P8_h			150		mV
VADP (CSIN) Low Falling	VADPLO_f		**7.05**	7.2	**7.45**	V
VADP (CSIN) Low Hysteresis	VADPLO_h			350		mV
CSIN_ON Rising	CSIN_ON_r		**2.35**	2.53	**2.65**	V
CSIN_ON Hysteresis	CSIN_ON_h			250		mV
Linear Regulator						
VDD Output Voltage	VDD	6V < V_{DCIN} < 23V, no load	**4.5**	5	**5.5**	V
VDD Dropout Voltage	VDD_dp	30mA, V_{DCIN} = 4V		150		mV
VDD Overcurrent Threshold	VDD_OC		**130**	160	**200**	mA
VDD2P5 Output Voltage	VDD2p5	3.6V < V_{DCIN} < 5.5V, no load	**2.45**	2.55	**2.7**	V
VDD2P5 Overcurrent Threshold	VDD2P5_OC		**15**	20	**25**	mA
VDD2P5 Overvoltage Rising	VDD2P5_OV_r		**3.1**	3.3	**3.5**	V
MCU_LDO Output Voltage	V_{MCU_LDO}	3.6V < V_{DCIN} < 5.5V, no load	**3.1**	3.3	**3.5**	V
MCU_LDO Dropout Voltage	MCU_LDO_dp	30mA, V_{DCIN} = 2.5V		75		mV
MCU_LDO Overcurrent Threshold	MCU_LDO_OC		**34**	40	**46**	mA
Battery Current	IBAT1	Battery only, BGATE off, GPCOMP off, BMON off, VBAT = 8.4V, VSYS current comes from battery, VCONN_POWER current comes from battery, CC1/CC2 open, MCU_LDO off, VCONN MUX off, sink dead battery Rd, I2CIDLE mode, IBAT = IVBAT + ICSOP + ICSON + IVSYS		40	**80**	µA
	IBAT2	Battery only, BGATE off, GPCOMP on, BMON on, VBAT = 8.4V to 16.8V, VSYS current comes from battery, VCONN_POWER current comes from battery, CC1/CC2 open, MCU_LDO on, VCONN MUX off, sink dead battery Rd, I2CIDLE mode, IBAT = IVBAT + ICSOP + ICSON + IVSYS		120	**150**	µA

Operating conditions: V_{BUS} = CSIP = CSIN = 5V and 20V, V_{SYS} = V_{BAT} = CSOP = CSON = 8V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -10°C to +125°C unless otherwise specified.** (Cont.)

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Battery Current (Continued)	IBAT3	Battery only, BGATE off, GPCOMP on, BMON on, VBAT = 8.4V to 16.8V, VSYS current comes from battery, VCONN_POWER current comes from battery, CC1/CC2 open, MCU_LDO on, VCONN MUX off, sink Rd, I2CIDLE mode, IBAT = IVBAT + ICSOP + ICSON + IVSYS		210	**250**	µA
	IBAT4	Battery only, BGATE off, GPCOMP on, BMON on, VBAT = 8.4V to 16.8V, VSYS current comes from battery, VCONN_POWER current comes from battery, DRP toggling, MCU_LDO on, VCONN MUX off, sink Rd, I2CIDLE mode, CC comparators on, IBAT = IVBAT + ICSOP + ICSON + IVSYS		330	**415**	µA
	IBAT5	Battery only, BGATE off, GPCOMP on, ADC on, BMON on, VBAT = 8.4V to 16.8V, VSYS current comes from battery, VCONN_POWER current comes from battery, DRP toggling, MCU_LDO on, VCONN MUX on, sink Rd, I2CIDLE mode, CC comparators on, IBAT = IVBAT + ICSOP + ICSON + IVSYS		1400	**1475**	µA
	IQ1	READY state, power down mode, VBAT = 10V, VBUS = 20V VCONN_POWER current comes from VDDP, GPCOMP on, MCU_LDO on, VCONN MUX off, sink Rd, 24MHz CLOCK on, CC comparators on, IQ = IVBAT + ICSOP + ICSON + IVSYS + IVBUS + ICSIP + ICSIN + IASRC		1.8	**1.9**	mA
	IQ2	VSYS state, no switching, VBAT = 10V, VBUS = 20V VCONN_POWER current comes from VDDP, GPCOMP on, ADC on, BMON on, MCU_LDO on, VCONN MUX off, sink Rd, 24MHz CLOCK on, CC comparators on, IQ = IVBAT + ICSOP + ICSON + IVSYS + IVBUS + ICSIP + ICSIN + IASRC + IPH1 + IPH2		2.8	**2.9**	mA
Adapter Current Regulation, Rs1 = 20mΩ, Forward Mode						
Adapter Current Accuracy		V_{CSIP} - V_{CSIN} = 80mV (4A)	**-2.25**		**2.25**	%
		V_{CSIP} - V_{CSIN} = 60mV (3A)	**-2.5**		**2.5**	%
		V_{CSIP} - V_{CSIN} = 40mV (2A)	**-2.5**		**2.5**	%
		V_{CSIP} - V_{CSIN} = 30mV (1.5A)	**-3**		**3**	%
		V_{CSIP} - V_{CSIN} = 15mV (0.748A)	**-5**		**5**	%
		V_{CSIP} - V_{CSIN} = 10mV (0.5A)	**-10**		**10**	%

Operating conditions: V_{BUS} = CSIP = CSIN = 5V and 20V, V_{SYS} = V_{BAT} = CSOP = CSON = 8V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -10°C to +125°C unless otherwise specified.** (Cont.)

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Adapter Current PROCHOT# Threshold Rs1 = 20mΩ		ACProchot = 0x1580H (5504mA)	**-1.5**		**1.5**	%
		ACProchot = 0x07E0H (2016mA)	**-3**		**3**	%
		ACProchot = 0x0400H (1024mA)	**-6**		**6**	%
System Voltage Regulation						
Maximum System Voltage Accuracy		MaxSystemVoltage for 2-Cell, 3-Cell and 4-Cell (8.4V, 12.6V and 16.8V) (T_J = -10°C to +85°C)	**-0.5**		**0.5**	%
		MaxSystemVoltage for 2-Cell, 3-Cell and 4-Cell (8.4V, 12.6V and 16.8V) (T_J = -40°C to +125°C)	**-0.6**		**0.6**	%
Minimum System Voltage Accuracy			**-3**		**3**	%
Input Voltage Regulation Accuracy		V_{CSIN} = 4.096V	**3.98**		**4.22**	V
Charge Current Regulation, Rs2 = 10mΩ (Limits apply across temperature range of 0°C to +60°C)						
Charge Current Accuracy		V_{CSOP} - V_{CSON} = 60mV (6A)	**-2**		**2**	%
		V_{CSOP} - V_{CSON} = 20mV (2A)	**-4**		**4**	%
		V_{CSOP} - V_{CSON} = 10mV (1A)	**-6**		**6**	%
		V_{CSOP} - V_{CSON} = 5mV (0.5A)	**-12**		**12**	%
Trickle Charging Current Regulation, Rs2 = 10mΩ (Limits apply across temperature range of 0°C to +60°C)						
Trickle Charge Current Accuracy		Control2 register Bit<15:13> = 001	**20**	64	**100**	mA
		Control2 register Bit<15:13> = 010	**55**	96	**135**	mA
		Control2 register Bit<15:13> = 011	**80**	128	**170**	mA
		Control2 register Bit<15:13> = 100	**112**	160	**208**	mA
		Control2 register Bit<15:13> = 101	**134**	192	**250**	mA
		Control2 register Bit<15:13> = 110	**157**	224	**291**	mA
		Control2 register Bit<15:13> = 111	**180**	256	**333**	mA
End of Charge Current Accuracy when Using Autonomous Charging	EOC	Control7 register Bit<9:8> = 00	**70**	125	**180**	mA
		Control7 register Bit<9:8> = 01	**20**	70	**120**	mA
		Control7 register Bit<9:8> = 10	**180**	230	**295**	mA
		Control7 register Bit<9:8> = 11	**125**	180	**240**	mA
Auto Recharge Threshold Relative to Maximum System Voltage	ART	2-cell battery		430		mV
		3-cell battery		600		mV
		4-cell battery		700		mV

Operating conditions: V_{BUS} = CSIP = CSIN = 5V and 20V, V_{SYS} = V_{BAT} = CSOP = CSON = 8V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -10°C to +125°C unless otherwise specified.** (Cont.)

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Ideal Diode Mode						
Entering Ideal Diode Mode VSYS Voltage Threshold		BGATE off, VSYS falling VVBAT - VVSYS	**110**	180	**255**	mV
Exiting Ideal Diode Mode Battery Discharging Current Threshold		Rs2 = 10mΩ		80		mA
Exiting Ideal Diode Mode Battery Charging Current Threshold		Rs2 = 10mΩ	**40**	160	**255**	mA
AMON/BMON						
Input Current Sense Amplifier, Rs1 = 20mΩ						
CSIP/CSIN Input Voltage Range	V_{CSIP}/V_{CSIN}		**4**		**23**	V
AMON Gain				17.97		V/V
AMON Accuracy V_{AMON} = AMON gain x (CSIP - CSIN)		V_{CSIP} - V_{CSIN} = 100mV (5A), CSIP = 5V to 20V	**-2.5**		**2.5**	%
		V_{CSIP} - V_{CSIN} = 20mV (1A), CSIP = 5V to 20V	**-6.5**		**6.5**	%
		V_{CSIP} - V_{CSIN} = 10mV (0.5A), CSIP = 5V to 20V	**-12**		**12**	%
		V_{CSIP} - V_{CSIN} = 2mV (0.1A), CSIP = 5V to 20V	**-55**		**55**	%
Reverse AMON Gain				17.9		V/V
AMON Accuracy VAMON = AMON gain x (CSIN - CSIP)		V_{CSIN} - V_{CSIP} = 80mV (4A), CSIP = 4V to 22V	**-3.5**		**3.5**	%
		V_{CSIN} - V_{CSIP} = 20mV (1A), CSIP = 4V to 22V	**-6.5**		**6.5**	%
		V_{CSIN} - V_{CSIP} = 10mV (0.5A), CSIP = 4V to 22V	**-12**		**12**	%
		V_{CSIN} - V_{CSIP} = 5.12mV (0.256A), CSIP = 4V to 22V	**-25**		**25**	%
AMON Minimum Output Voltage		V_{CSIP} - V_{CSIN} = 0V			**30**	mV
Discharge Current Sense Amplifier, Rs2 = 10mΩ						
BMON Gain (Battery Discharging)				17.97		V/V

Operating conditions: V_{BUS} = CSIP = CSIN = 5V and 20V, V_{SYS} = V_{BAT} = CSOP = CSON = 8V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -10°C to +125°C unless otherwise specified.** (Cont.)

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
BMON Accuracy VBMON = BMON Gain x (V_{CSON} - V_{CSOP})		V_{CSON} - V_{CSOP} = 100mV (10A), V_{CSON} = 8V	**-2**		**2**	%
		V_{CSON} - V_{CSOP} = 20mV (2A), V_{CSON} = 8V	**-6**		**6**	%
		V_{CSON} - V_{CSOP} = 10mV (1A), V_{CSON} = 8V	**-10**		**10**	%
		V_{CSON} - V_{CSO}P = 6mV (0.6A), V_{CSON} = 8V	**-20**		**20**	%
BMON Charging Accuracy, Rs2 = 10mΩ (Limits apply across temperature range of 0°C to +60°C)						
BMON Gain (Battery Charging)				35.78		V/V
BMON Accuracy VBMON = BMON Gain x (V_{CSON} - V_{CSOP})		V_{CSOP} - V_{CSON} = 60mV (6A), V_{CSON} = 8V	**-3**		**3**	%
		V_{CSOP} - V_{CSON} = 40mV (4A), V_{CSON} = 8V	**-4**		**4**	%
		V_{CSOP} - V_{CSON} = 10mV (1A), V_{CSON} = 8V	**-10**		**10**	%
		V_{CSOP} - V_{CSON} = 5mV (0.5A), V_{CSON} = 8V	**-25**		**25**	%
BMON Minimum Output Voltage		V_{CSOP} - V_{CSON} = 0V			**30**	mV
Discharging Current PROCHOT# Threshold	$I_{DIS\_HOT\_TH}$	Rs2 = 10mΩ, DCProchot = 2.048A	**1.77**	2.08	**2.39**	A
Discharging Current PROCHOT# Threshold, Battery Only	$I_{DIS\_HOT\_TH}$	Rs2 = 10mΩ, DCProchot = 12A	**9.4**	13	**19**	A
		Rs2 = 10mΩ, DCProchot = 6A	**4.5**	6	**9.5**	A
AMON/BMON Source Resistance[2]					**5**	Ω
AMON/BMON Sink Resistance[2]					**5**	Ω
BATGONE and OTGEN						
OTGEN High-Level Input Voltage			**0.9**			V
OTGEN Low-Level Input Voltage					**0.4**	V
BATGONE High-Level Input Voltage			**V_{DD} - 0.6**			V
BATGONE Low-Level Input Voltage					**V_{DD} - 1.2**	V
Pull-Up Current		VBATGONE = 3.3V, 5V; VOTGEN = 3.3V, 5V		1		µA
NTC Step1 Pull-Up Current			**62**	65	**68**	µA
NTC Step2 Pull-Up Current			**126**	130	**134**	µA

Operating conditions: V_{BUS} = CSIP = CSIN = 5V and 20V, V_{SYS} = V_{BAT} = CSOP = CSON = 8V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -10°C to +125°C unless otherwise specified.** (Cont.)

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
NTC Step3 Pull-Up Current			**250**	260	**270**	µA
PROCHOT#						
PROCHOT# Debounce Time[2]		PROCHOT# Debounce Control2 Bit<10:9> = 11	**0.85**	1	**1.15**	ms
		PROCHOT# Debounce Control2 Bit<10:9> = 10	**425**	500	**575**	µs
PROCHOT# Duration Time[2]		PROCHOT# Duration Control2 Bit<8:6> = 000	**8.5**	10	**11.5**	ms
		PROCHOT# Duration Control2 Bit<8:6> = 001	**17**	20	**23**	ms
Low VSYS PROCHOT# Trip Falling Threshold	$V_{LOW\_VSYS\_HOT}$	Control8 register Bit<10:6> = 00000	**5.4**	5.6	**5.8**	V
		Control8 register Bit<10:6> = 00001	**5.5**	5.7	**5.9**	V
		Control8 register Bit<10:6> = 00010	**5.6**	5.8	**6**	V
		Control8 register Bit<10:6> = 00011	**5.7**	5.9	**6.1**	V
		Control8 register Bit<10:6> = 00100	**5.8**	6	**6.2**	V
		Control8 register Bit<10:6> = 00101	**5.9**	6.1	**6.3**	V
		Control8 register Bit<10:6> = 00110	**6**	6.2	**6.4**	V
		Control8 register Bit<10:6> = 00111	**6.1**	6.3	**6.5**	V
		Control8 register Bit<10:6> = 01000	**6.2**	6.4	**6.6**	V
		Control8 register Bit<10:6> = 01001	**6.3**	6.5	**6.7**	V
		Control8 register Bit<10:6> = 01010	**6.4**	6.6	**6.8**	V
		Control8 register Bit<10:6> = 01011	**6.5**	6.7	**6.9**	V
		Control8 register Bit<10:6> = 01100	**6.6**	6.8	**7**	V
		Control8 register Bit<10:6> = 01101	**6.7**	6.9	**7.1**	V
		Control8 register Bit<10:6> = 01110	**6.8**	7	**7.2**	V
		Control8 register Bit<10:6> = 01111	**6.9**	7.1	**7.3**	V
		Control8 register Bit<10:6> = 10000	**7**	7.2	**7.4**	V
		Control8 register Bit<10:6> = 10001	**7.1**	7.3	**7.5**	V
		Control8 register Bit<10:6> = 10010	**7.2**	7.4	**7.6**	V
		Control8 register Bit<10:6> = 10011	**7.3**	7.5	**7.7**	V
		Control8 register Bit<10:6> = 10100 and above	**7.4**	7.6	**7.8**	V
PROCHOT#, Input Leakage Current					**1**	µA
PROCHOT#, Output Sink Current		VPROCHOT = 0.4V	**4**			mA

Operating conditions: V_{BUS} = CSIP = CSIN = 5V and 20V, V_{SYS} = V_{BAT} = CSOP = CSON = 8V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -10°C to +125°C unless otherwise specified.** (Cont.)

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Reverse Mode; USB source and OTG mode						
Reverse Mode Voltage		OTG voltage register, DAC = 0x0FA0h	**4.93**	5	**5.25**	V
Reverse Mode Current		Rs1 = 20mΩ OTG current register = 512mA	**450**	512	**585**	mA
		Rs1 = 20mΩ OTG current register = 736mA	**660**	736	**810**	mA
		Rs1 = 20mΩ OTG current register = 1024mA	**960**	1024	**1100**	mA
		Rs1 = 20mΩ OTG current register = 1504mA	**1429**	1504	**1580**	mA
		Rs1 = 20mΩ OTG current register = 3008mA	**2888**	3008	**3128**	mA
		Rs1 = 20mΩ OTG current register = 4096mA	**3975**	4096	**4240**	mA
Fast Role Swap						
V_{BUS} Top Window Comparator Falling Threshold		OTGVDAC = 5V	**5.25**	5.5	**5.75**	V
V_{BUS} Top Window Comparator Hysteresis[2]		OTGVDAC = 5V		1.15		V
V_{BUS} Bottom Window Comparator Rising Threshold		OTGVDAC = 5V	**4.25**	4.5	**4.75**	V
V_{BUS} Bottom Window Comparator Hysteresis[2]		OTGVDAC = 5V		1.15		V
V_{BUS} VSAFE Falling[2]	VBUS_SAFE_f	VSAFE5V_sel = 1	**5.55**	5.7	**5.85**	V
		VSAFE5V_sel = 0	**4.6**	4.75	**4.9**	
V_{BUS} VSAFE Hysteresis	VBUS_SAFE_h			100		mV
Analog Support of OTG Output (tSrcFRSwap)[2]		When configured OTG_EN = 1			**150**	µs
PPS and DVC						
V_{BAT} OV Rising	VBAT_OV_r	MaxSystemVoltage register value = 8.4V	**75**	150	**275**	mV
		MaxSystemVoltage register value = 12.6V	**150**	250	**400**	mV
		MaxSystemVoltage register value = 16.8V	**200**	350	**600**	mV
V_{BAT} OV Hysteresis	VBAT_OV_h			55		mV
CCHOT Rising, Rs2 = 10mΩ	CCHOT_r	Charge Current = 4A		4.27		A

Operating conditions: V_{BUS} = CSIP = CSIN = 5V and 20V, V_{SYS} = V_{BAT} = CSOP = CSON = 8V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -10°C to +125°C unless otherwise specified.** (Cont.)

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
ACLIM						
ACLIM Output Current			**4.57**	4.85	**5.11**	µA
ACLIM High Rising			**V_{DD} – 1.0**	V_{DD} – 0.8	**V_{DD} – 0.6**	V
General Purpose Comparator						
General Purpose Comparator Rising Threshold		Reference = 1.2V	**1.15**	1.2	**1.25**	V
		Reference = 2V (not available in Battery mode)	**1.95**	2	**2.05**	V
General Purpose Comparator Hysteresis		Reference = 1.2V	**25**	40	**50**	mV
		Reference = 2V (not available in Battery mode)	**25**	40	**50**	mV
Charger Protection						
VSYS Overvoltage Rising Threshold		MaxSystemVoltage register value = 8.4V	**8.9**	9.2	**9.45**	V
VSYS Overvoltage Hysteresis			**250**	400	**550**	mV
VSYS OK Threshold			**0.45**	0.6	**0.75**	V
VSYS OK Source Current			**8.5**	10	**13.5**	mA
Adapter Way Overcurrent Rising Threshold		Rs1 = 20mΩ	**8**	12	**15**	A
Battery Discharge Way Overcurrent Rising Threshold		Rs2 = 10mΩ	**12**	18	**24**	A
Over-Temperature Threshold[2]			**140**	150	**160**	°C
VBUS Overvoltage Rising Threshold			**22.5**	23.4	**24**	V
VBUS Overvoltage Hysteresis			**300**	400	**500**	mV
CSIN Overvoltage Rising Threshold			**22.5**	23.3	**24**	V
CSIN Overvoltage Hysteresis			**300**	400	**500**	mV
OTG Undervoltage Falling Threshold		OTG voltage setting = 5.0V Register 0x49 = 0x0FA0h	**3.45**	3.8	**4.25**	V
OTG Overvoltage Rising Threshold		OTG voltage setting = 5.0V Register 0x49 = 0x0FA0h	**5.8**	6.2	**6.6**	V
Oscillator						
Oscillator Frequency, Digital Core Only			**21.6**	24	**26.4**	MHz
			675	750	**825**	KHz
Digital Debounce Time Accuracy[2]			**-15**		**15**	%

Operating conditions: V_{BUS} = CSIP = CSIN = 5V and 20V, V_{SYS} = V_{BAT} = CSOP = CSON = 8V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -10°C to +125°C unless otherwise specified.** (Cont.)

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Miscellaneous						
Switching Frequency Accuracy		VCOMP > 1.7V and not in period stretching	**-15**		**15**	%
Battery Learn Mode Auto-Exit Threshold[2]		MinSystemVoltage = 5.376V Control1 register Bit<13> = 1	**5.05**	5.35	**5.7**	V
Gate Driver[2]						
UGATE1 Pull-Up Resistance	UG1RPU	100mA source current		800	**1200**	mΩ
UGATE1 Source Current	UG1SRC	VUGATE1 - VPHASE1 = 2.5V	**1.3**	2		A
UGATE1 Pull-Down Resistance	UG1RPD	100mA sink current		350	**475**	mΩ
UGATE1 Sink Current	UG1SNK	VUGATE1 - VPHASE1 = 2.5V	**1.9**	2.8		A
LGATE1 Pull-Up Resistance	LG1RPU	100mA source current		800	**1200**	mΩ
LGATE1 Source Current	LG1SRC	VLGATE1 - GND = 2.5V	**1.3**	2		A
LGATE1 Pull-Down Resistance	LG1RPD	100mA sink current		300	**450**	mΩ
LGATE1 Sink Current	LG1SNK	VLGATE1 - GND = 2.5V	**2.3**	3.5		A
LGATE2 Pull-Up Resistance	LG2RPU	100mA source current		800	**1200**	mΩ
LGATE2 Source Current	LG2SRC	VLGATE2 - GND = 2.5V	**1.3**	2		A
LGATE2 Pull-Down Resistance	LG2RPD	100mA sink current		300	**450**	mΩ
LGATE2 Sink Current	LG2SNK	VLGATE2 - GND = 2.5V	**2.3**	3.5		A
UGATE2 Pull-Up Resistance	UG2RPU	100mA source current		800	**1200**	mΩ
UGATE2 Source Current	UG2SRC	VUGATE2 - VPHASE2 = 2.5V	**1.3**	2		A
UGATE2 Pull-Down Resistance	UG2RPD	100mA sink current		300	**450**	mΩ
UGATE2 Sink Current	UG2SNK	VUGATE2 - VPHASE2 = 2.5V	**2.3**	3.5		A
UGATE1 to LGATE1 Dead Time	tUG1LG1DEAD		**10**	20	**40**	ns
LGATE1 to UGATE1 Dead Time	tLG1UG1DEAD		**10**	20	**40**	ns
LGATE2 to UGATE2 Dead Time	tLG2UG2DEAD		**10**	20	**40**	ns
UGATE2 to LGATE2 Dead Time	tUG2LG2DEAD		**10**	20	**40**	ns

Operating conditions: V_{BUS} = CSIP = CSIN = 5V and 20V, V_{SYS} = V_{BAT} = CSOP = CSON = 8V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -10°C to +125°C unless otherwise specified.** (Cont.)

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Charge Pump Gate Drivers						
ASGATE Gate Drive Current (Sink)		ASGATE Off ASGATE = VASRC + 2V	**165**	190	**250**	µA
BGATE Gate Drive Current (Sink)		BGATE Off BGATE = VVBAT + 2V	**165**	190	**250**	µA
ASGATE Gate Drive Current (Source)		ASGATE On VASGATE = VASRC + 2V, VASRC > 3.9V	**15**	40	**70**	µA
BGATE Gate Drive Current (Source)		BGATE On VBGATE = VVBAT + 2V, VVBAT > 2.7V	**15**	40	**70**	µA
VCONN Mux						
VCONN_POWER OK Rising			**2.55**	2.75	**2.95**	V
VCONN_POWER OK Hysteresis				120		mV
VCONN Switch $r_{DS(ON)}$				525		mΩ
VCONN Swtich Turn on Time[2]		Time from enable to fully on, with 10µF cap			**1.5**	ms
CCx Discharge						
FRS Discharge $r_{DS(ON)}$		With 200pF to 600pF cap range		5		Ω
VCONN Mux Discharge $r_{DS(ON)}$			**50**	100	**150**	Ω
VCONN Mux and CC-PHY Protection (Limits apply across the junction temperature range -10°C to +85°C)						
VCONN OC Rising		Control8 Bit<1:0> = 00 (default)	**710**	800	**890**	mA
		Control8 Bit<1:0> = 01	**300**	400	**460**	mA
		Control8 Bit<1:0> = 10	**1.52**	1.6	**1.91**	A
VCONN OC Blanking Time[2]			**4.25**	5	**5.75**	ms
CCx Short Threshold			**170**	240	**310**	mV
CCx Short Blanking Time[2]			**4.25**	5	**5.75**	ms
Over-Temperature Threshold[2]			**145**	155	**165**	°C
CCx Overvoltage Rising		Relative to VCONN_POWER voltage level	**250**	325	**400**	mV
CCx Overvoltage Hysteresis				100		mV
Cable Settings						
Rd Clamp			**0.6**	1.1	**1.3**	V
Ropen				5		MΩ
Rd Resistor			**4.59**	5.1	**5.61**	kΩ

Operating conditions: V_{BUS} = CSIP = CSIN = 5V and 20V, V_{SYS} = V_{BAT} = CSOP = CSON = 8V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -10°C to +125°C unless otherwise specified.** (Cont.)

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
IP Current		Default USB Power	**64**	80	**96**	µA
		1.5A at 5V	**166**	180	**194**	µA
		3A at 5V	**304**	330	**356**	µA
TX						
Bit Rate	$f_{BitRate}$		**270**	300	**330**	Kps
Fall Time	t_{Fall}	10% and 90% amplitude points, minimum is under an unload condition	**300**			ns
Rise Time	t_{Rise}	10% and 90% amplitude points, minimum is under an unload condition	**300**			ns
Voltage Swing	V_{Swing}	Applies to both no load condition and under the load condition specified in USB-PD Spec Rev.2.0 section 5.8.3.3	**1.05**		**1.2**	V
Output Impedance	zDrive	Source output impedance at the Nyquist frequency of [USB 2.0] low speed (750kHz) while the source is driving the CC line.	**33**		**75**	Ω
SMBus						
SDA_B/SCL_B Input Low Voltage					**0.7**	V
SDA_B/SCL_B Input High Voltage			**1.2**			V
SDA_B/SCL_B Input Bias Current					**1**	µA
SDA_B, Output Sink Current		VSDA_B = 0.4V, on	**4**			mA
SDA_C/SCL_C Input Low Voltage					**0.7**	V
SDA_C/SCL_C Input High Voltage			**1.2**			V
SDA_C/SCL_C Input Bias Current					**1**	µA
SDA_C, Output Sink Current		VSDA_B = 0.4V, on	**4**			mA
ALERT_B Input Leakage Current					**1**	µA
ALERT_B, Output Sink Current		VACOK = 0.4V	**4**			mA
ALERT_C Input Leakage Current					**1**	µA
ALERT_C, Output Sink Current		VACOK = 0.4V	**4**			mA

1. Parameters with Min and/or Max limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
2. Limits established by characterization and are not production tested.

3.5 SMBus Timing Specification

Parameters	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
SMBus Frequency	f_{SMB}	Supports Standard, Fast mode and Fast mode plus	400		1000	kHz
Bus Free Time	t_{BUF}		0.5			µs
Start Condition Hold Time from SCL	$t_{HD:STA}$		0.26			µs
Start Condition Set-Up Time from SCL	$t_{SU:STA}$		0.26			µs
Stop Condition Set-Up Time from SCL	$t_{SU:STO}$		0.26			µs
SDA Hold Time from SCL	$t_{HD:DAT}$		0			ns
SDA Set-Up Time from SCL	$t_{SU:DAT}$		50			ns
SCL Low Period	t_{LOW}		0.5			µs
SCL High Period	t_{HIGH}		0.26		50	µs
SMBus Inactivity Timeout		Maximum charging period without a SMBus Write to MaxSystemVoltage or ChargeCurrent register when enabled		175		s

1. Parameters with Min and/or Max limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

4. Typical Performance Graphs

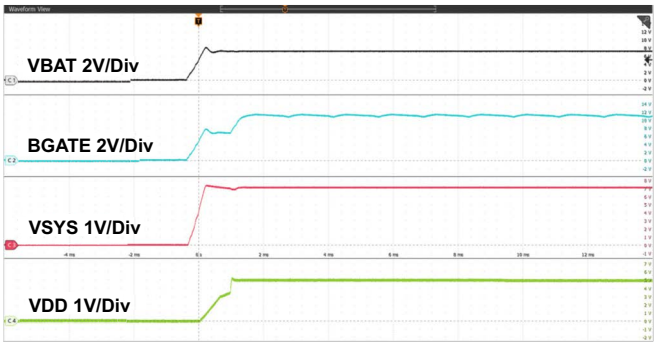


Figure 5. Start Up with Battery

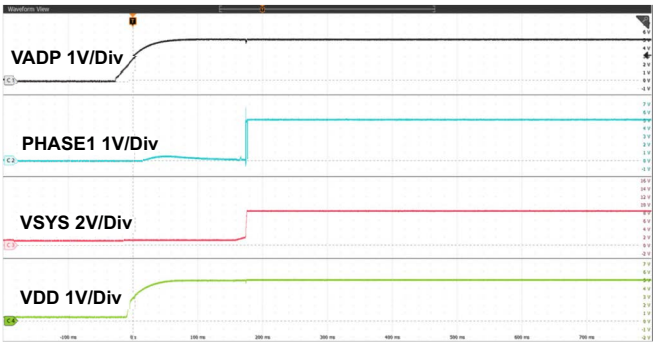


Figure 6. Start Up with 5V Adapter

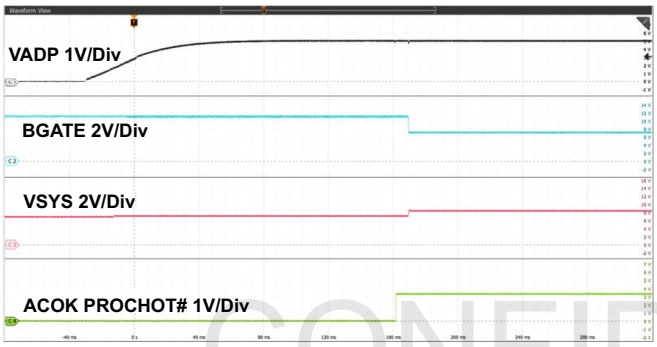


Figure 7. Start Up with Adapter and Battery, V_{ADP} = 5V, MaxSystemVoltage = 8.384V, V_{BAT} = 7V, Charge Current Limit = 0A

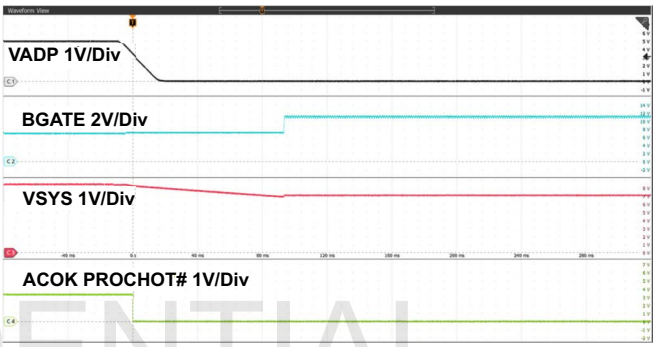


Figure 8. Adapter Removal, V_{ADP} = 5V, MaxSystemVoltage = 8.384V, V_{BAT} = 7V, Charge Current Limit = 0A, System Load = 0A

Figure 9. Adapter Voltage Ramp Up, Boost --> Buck_Boost --> Buck Operation Mode Transition

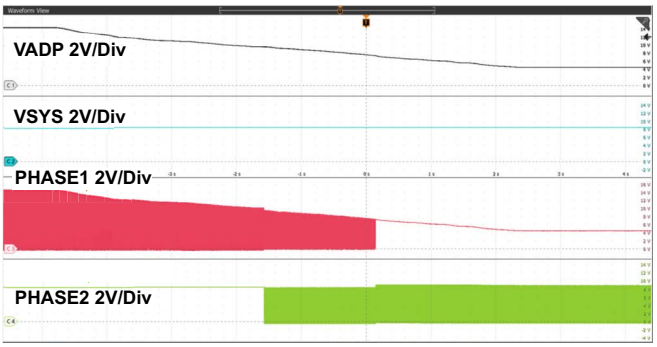


Figure 10. Adapter Voltage Ramp Down, Buck --> Buck_Boost --> Boost Operation Mode Transition

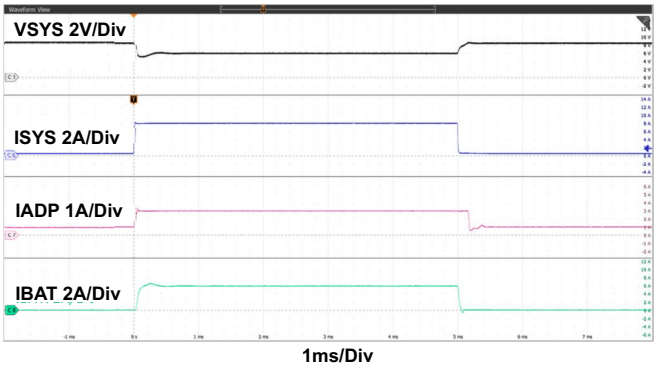


Figure 11. Boost Mode, Output Voltage Loop to Adapter Current Loop Transition, V_{ADP} = 5V, V_{BAT} = 7V, MaxSystemVoltage = 8.384V, Adapter_current_limit = 3A, Charge_current = 0A, System_load = 0.5A to 8A

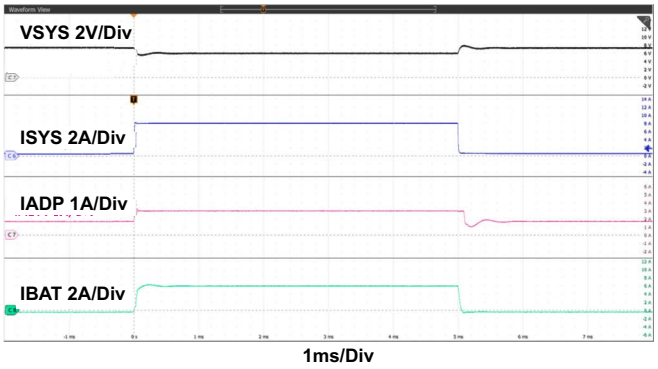


Figure 12. Boost Mode, Charge Current Loop to Adapter Current Loop Transition, V_{ADP} = 5V, V_{BAT} = 7V, MaxSystemVoltage = 8.384V, Adapter_current_limit = 3A, Charge_current = 0.5A, System_load = 0.5A to 8A

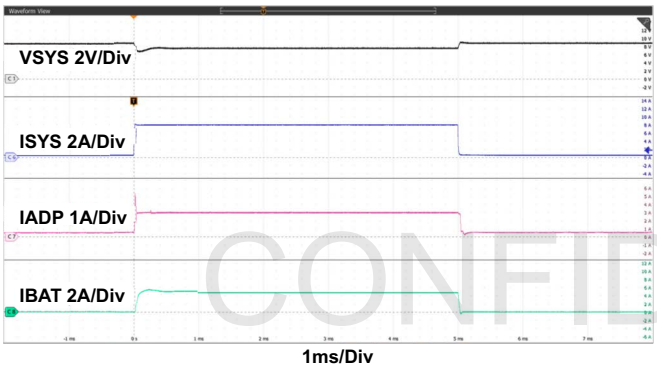


Figure 13. Buck_Boost Mode, Output Voltage Loop to Adapter Current Loop Transition, V_{ADP} = 9V, V_{BAT} = 8.4V, MaxSystemVoltage = 8.8V, Adapter_current_limit = 3A, Charge_current = 0A, System_load = 0.5A to 8A

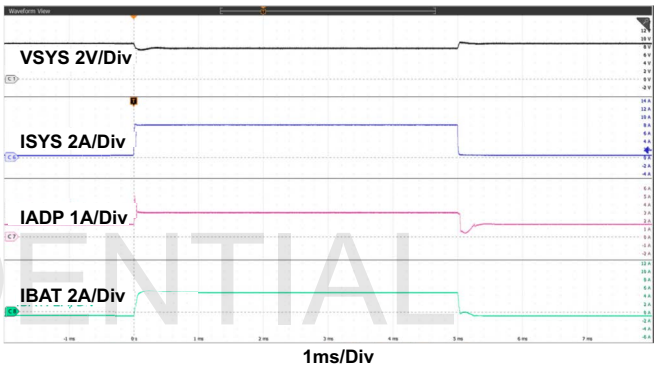


Figure 14. Buck_Boost Mode, Charge Current Loop to Adapter Current Loop Transition, V_{ADP} = 9V, V_{BAT} = 8.4V, MaxSystemVoltage = 8.8V, Adapter_current_limit = 3A, Charge_current = 1A, System_load = 0.5A to 8A

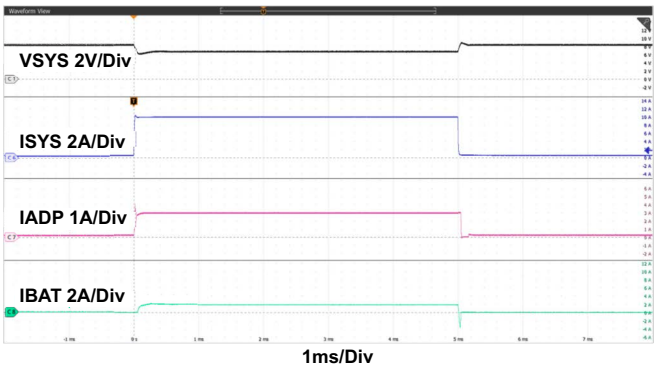


Figure 15. Buck Mode, Output Voltage Loop to Adapter Current Loop Transition, V_{ADP} = 20V, V_{BAT} = 7V, MaxSystemVoltage = 8.384V, Adapter_current_limit = 3A, Charge_current = 0A, System_load = 0.5A to 10A

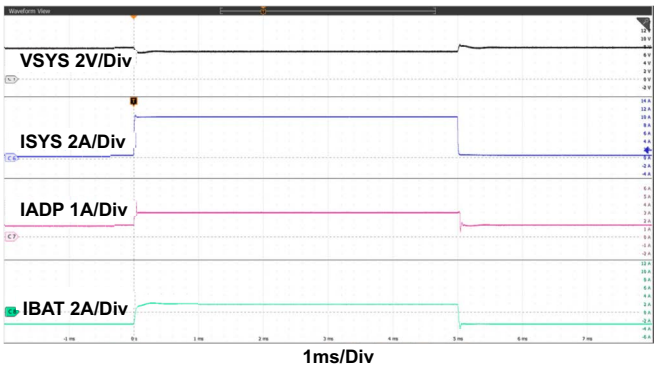


Figure 16. Buck Mode, Charge Current Loop to Adapter Current Loop Transition, V_{ADP} = 20V, V_{BAT} = 7V, MaxSystemVoltage = 8.384V, Adapter_current_limit = 3A, Charge_current = 3A, System_load = 0.5A to 10A

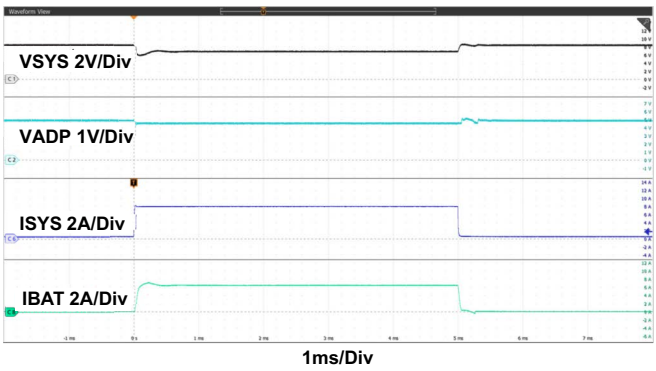


Figure 17. Boost Mode, Output Voltage Loop to Input Voltage Loop Transition, V_{ADP} = 5V, V_{BAT} = 8V, MaxSystemVoltage = 8.384V, Charge_current = 0A, System_load = 0.5A to 8A, Input_voltage_dac = 4.437V

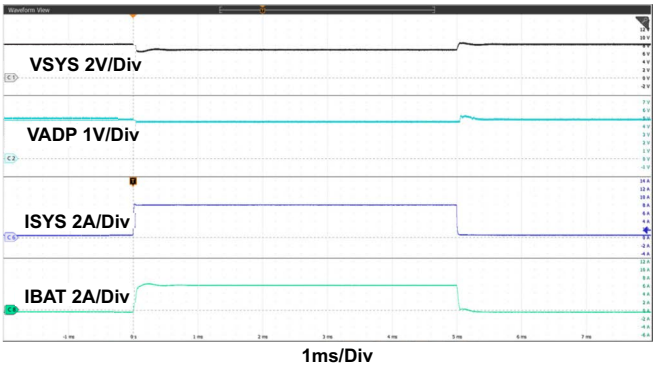


Figure 18. Boost Mode, Charge Current Loop to Input Voltage Loop Transition, V_{ADP} = 5V, V_{BAT} = 8V, MaxSystemVoltage = 8.384V, Charge_current = 0.5A, System_load = 0.5A to 8A, Input_voltage_dac = 4.437V

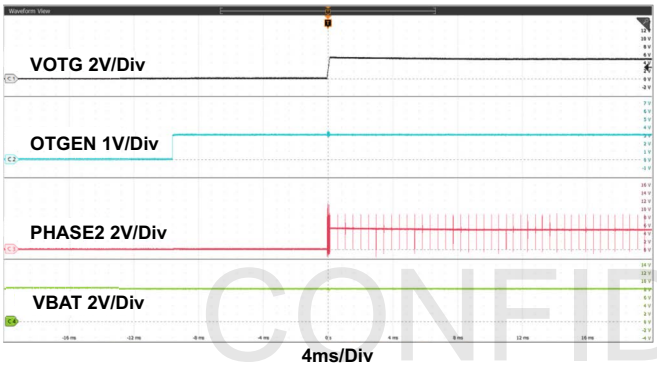


Figure 19. OTG Mode Enable Using OTGEN Pin, V_{BAT} = 8V, V_{OTG} = 5V, General Purpose Comparator Disabled, OTGEN Control Bit Enabled

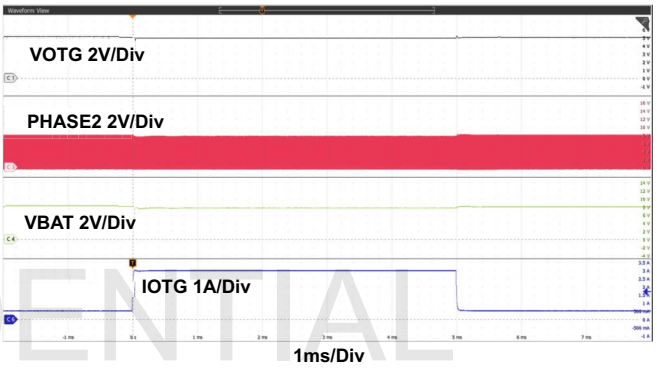


Figure 20. OTG Mode Transient. V_{BAT} = 8V, V_{OTG} = 5V, OTG Current = 3.2A, Load = 0.5A to 3A

5. General SMBus Architecture

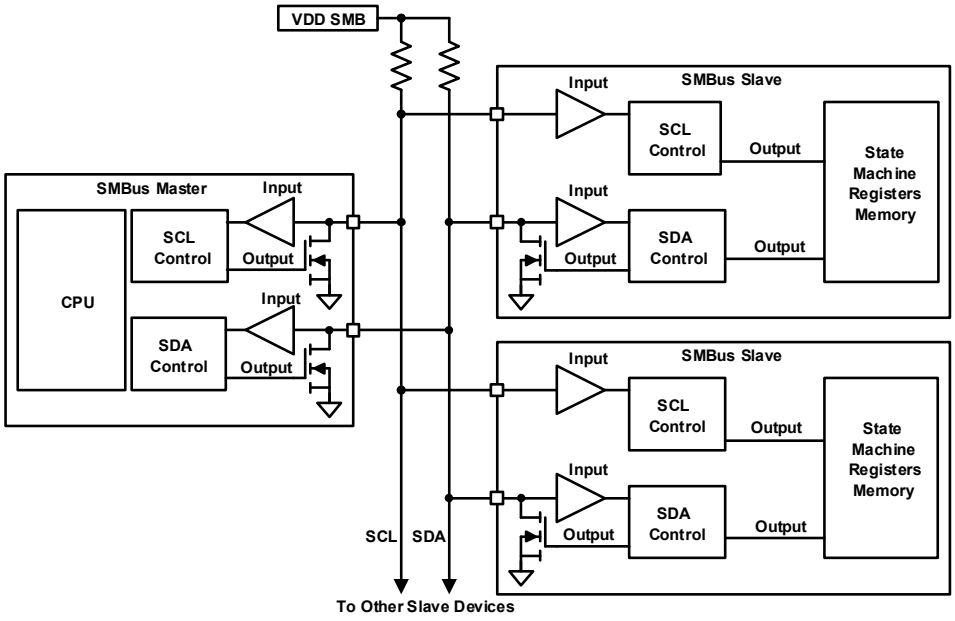


Figure 21. General SMBus Architecture

5.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the SCL unless generating a START or STOP condition. The HIGH or LOW state of the data line can change only when the clock signal on the SCL line is LOW. See Figure 22.

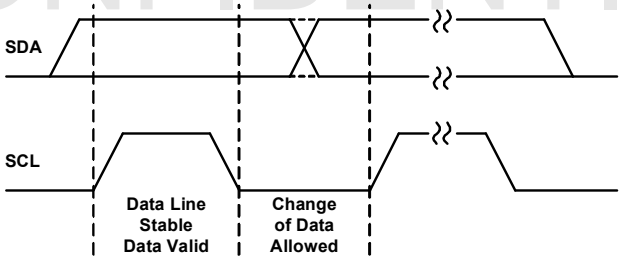


Figure 22. Data Validity

5.2 START and STOP Conditions

Figure 23 shows that the START condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The STOP condition is a LOW to HIGH transition on the SDA line while SCL is HIGH. A STOP condition must be sent before each START condition.

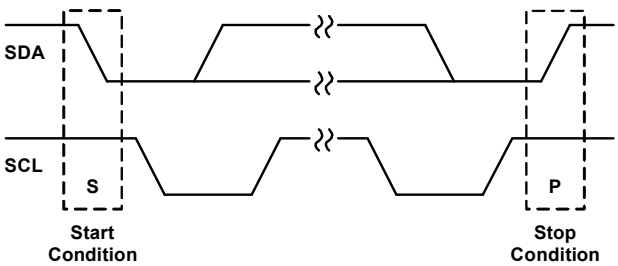


Figure 23. Start and Stop Waveforms

5.3 Acknowledge (ACK)

Each address and data transmission uses nine clock pulses. The ninth pulse is the Acknowledge bit (ACK). After the start condition, the master sends seven slave address bits and a R/$\overline{W}$ bit during the next eight clock pulses. During the ninth clock pulse, the device that recognizes its own address holds the data line LOW to acknowledge (see Figure 24). Both the master and slave use the ACK bit to acknowledge receipt of register addresses and data.

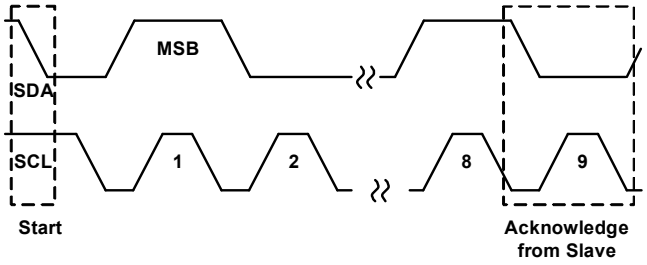


Figure 24. Acknowledge on the SMBus

5.4 SMBus Transactions

All transactions start with a control byte sent from the SMBus master device. The control byte begins with a Start condition, followed by seven bits of slave address (example: 0001001) and the R/W bit. The R/$\overline{W}$ bit is 0 for a WRITE or 1 for a READ. If any slave device on the SMBus bus recognizes its address, it acknowledges by pulling the Serial Data (SDA) line LOW for the last clock cycle in the control byte. If no slave exists at that address or it is not ready to communicate, the data line is 1, indicating a not acknowledge condition.

After the control byte is sent and the RAA489000 acknowledges it, the second byte sent by the master must be a register address byte, such as 0x14 for the ChargeCurrent register. The register address byte tells the RAA489000 which register the master writes or reads. See Table 1 for details about the registers. When the RAA489000 receives a register address byte, it responds with an acknowledge.

Both SMBus ports support ARA (Alert Response Address).

5.5 Byte Format

Every byte put on the SDA line must be eight bits long and must be followed by an ACK bit. Data is transferred with the Most Significant Bit (MSB) first and the Least Significant Bit (LSB) last. The LO BYTE data is transferred before the HI BYTE data. For example, when writing 0x41A0, 0xA0 is written first and 0x41 is written second.

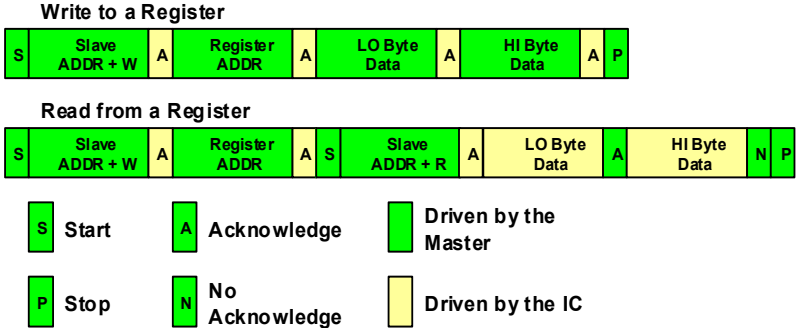


Figure 25. SMBus Read and Write Protocol

5.6 SMBus and I²C Compatibility

The RAA489000 SMBus minimum input logic high voltage is 2V, so it is compatible with an I²C with a pull-up power supply higher than 2V.

The RAA489000 SMBus registers are 16 bits, so it is compatible with a 16-bit I^2C or an 8-bit I^2C with auto-increment capability.

5.7 RAA489000 SMBus Commands

The RAA489000 receives control inputs from the SMBus interface after Power-On Reset (POR). The serial interface complies with the System Management Bus Specification, which can be downloaded from www.smbus.org. The RAA489000 uses the SMBus Read-word and Write-word protocols (see Figure 25) to communicate with the host system and a smart battery. The RAA489000 is an SMBus slave device and does not initiate communication on the bus. It responds to the 7-bit address 0b0001001_(RAA489000) as follows:

The Read and Write addresses for the RAA489000 charger are:

- Read address = 0b00010011 (0x13h)
- Write address = 0b00010010 (0x12h)

Other addresses are available on request and require programming resistor configuration (alternative write addresses are 0x92h, 0x94h, 0x96h).

The data (SDA) and clock (SCL) pins have Schmitt-trigger inputs that can accommodate slow edges. Choose pull-up resistors for SDA and SCL to achieve rise times according to the SMBus specifications.

Register DAC values in this datasheet are based on current-sensing resistors R_{s1} = 20mΩ and R_{s2} = 10mΩ unless otherwise specified.

To support TCPC, there is a dedicated SMBus interface. It uses SDA_C, SCL_C, and ALERT_C to communicate to the controller, which makes policy decisions. Information that is communicated on the CC1 or CC2 lines is buffered and presented to the SMBus.

5.8 Unlock Sequence

If TCPM connects to a locked version of RAA489000, it should write an unlock command sequence to RAA489000 after a power-on reset. After TCPM writes these unlock commands, it can access the RAA489000.

The unlock command register address is AAh. Write the following values to RAA489000.

- 1st access: DAA0h
- 2nd access: ACE0h
- 3rd access: 0D0Bh

6. RAA489000 Registers - Charger and TCPC

6.1 Charger Register Summary

Table 1. Detailed Summary of Registers

Register Names	Register Address	Read/ Write	# of Bits	Description	Default
ChargeCurrentLimit (Table 2)	0x14	R/W	11	[12:2]11-bit, LSB size 4mA, total range 6140mA with 10mΩ R_{S2} (0x0000h = disables fast charging)	0A
MaxSystemVoltage (Table 2)	0x15	R/W	12	[14:3]12-bit, LSB size 8mV, total range 18.304V (0x0000h = disables switching)	Set by PROG
					8.384V for 2-cell
					12.576V for 3-cell
					16.768V for 4-cell
Control10 (Table 11)	0x35	R/W	16	Configures DVC charging options	0x0000h
Control9 (Table 10)	0x36	R/W	8	Configures various charger options	0x0000h
Control 8 (Table 9)	0x37	R/W	16	Configures various charger options	0xA000h
Control7 (Table 8)	0x38	R/W	16	Configures two-level adapter current limit duration, Buck-boost period stretch, and other charger options	0x0000h
Control0 (Table 3)	0x39	R/W	16	Configures various charger options	0x0000h
Information1 (Table 13)	0x3A	R	16	Indicates various charger statuses	0x0000h
AdapterCurrentLimit2 (Table 2)	0x3B	R/W	11	[12:2]11-bit, LSB size 4mA, total range 6140mA with 20mΩ R_{S1}	1500mA
Control1 (Table 4)	0x3C	R/W	16	Configures various charger options	0x0282h
Control2 (Table 5)	0x3D	R/W	16	Configures various charger options	0x6000h
MinSystemVoltage (Table 2)	0x3E	R/W	8	[13:6]8-bit, LSB size 64mV, total range 16.320V (0x0000h = disables all battery charging)	0V
AdapterCurrentLimit1 (Table 2)	0x3F	R/W	11	[12:2]11-bit, LSB size 4mA, total range 6140mA with 20mΩ R_{S1}	Set by PROG pin
ACOK Reference (Table 2)	0x40	R/W	8	[13:6] 8-Bit, 0 to 27.132V in 106.4mV steps, value matches VIN ADC Channel 0x087h (0x0000h = disabled)	0x0000h (disabled)
Control6 (Table 12)	0x43	R/W	13	Interrupt trigger level direction 0 = Event went High to Low 1 = Event went Low to High	0x1FFFh
ACProchot# (Table 2)	0x47	R/W	8	[12:5] adapter current PROCHOT# threshold (0 to 6.14A) Default 3.072A, 32mA resolution for 20mΩ R_{s1}.	3.072A

Table 1. Detailed Summary of Registers (Cont.)

Register Names	Register Address	Read/ Write	# of Bits	Description	Default
DCProchot# (Table 2)	0x48	R/W	8	[13:6] Battery discharging current PROCHOT# threshold (to 12.3A) Default 4.096A, 64mA resolution for 10mΩ R_{s2}.	4.096A
OTG Voltage (Table 2)	0x49	R/W	12	[14:3] 12-bit, LSB size 10mV, 0 to 22.88V OTG mode voltage reference	4.77V
OTG Current (Table 2)	0x4A	R/W	8	[12:5] 8-bit, LSB size 32mA, total range 6.112A with 20mΩ R_{S1} OTG mode maximum current limit	0.512A
V_{IN} Voltage (Table 2)	0x4B	R/W	8	[13:6] 8-bit, LSB size 85.33mV, total range 16.384mV V_{IN} loop voltage reference	4.096V
Control3 (Table 6)	0x4C	R/W	16	Configures various charger options	0x0300h
Information2 (Table 14)	0x4D	R	16	Indicates various charger statuses	0x0000h
Control4 (Table 7)	0x4E	R/W	16	Configures various charger options	0x0000h
Control5 (Table 12)	0x4F	R/W	13	Interrupt mask control enable 0 = Not enabled/Masked 1 = Enabled/Unmasked	0x0000h
NTC ADC Results	0x80	R	10	ADC result for NTC/GP measurements, LSB = 8mV	Table 15
VBAT ADC Results	0x81	R	8	ADC result for VBAT measurements, LSB = 64mV	Table 15
TJ ADC Results	0x82	R	8	ADC result for internal T_J measurements, LSB = 8mV	Table 15
IADP ADC Results	0x83	R	8	ADC result for adapter current measurements, LSB = 22.2mA	Table 15
DC ADC Results	0x84	R	8	ADC result for battery discharge current measurements, LSB = 44.4mA	Table 15
CC ADC Results	0x85	R	8	ADC result for battery charge current measurements, LSB = 22.2mA	Table 15
VSYS ADC Results	0x86	R	8	ADC result for CSOP (VSYS) measurements, LSB = 96mV	Table 15
VIN ADC Results	0x87	R	8	ADC result for CSIN (VIN) measurements, LSB = 96mV	Table 15
VBUS ADC Results	0x89	R	8	ADC result for VBUS measurements, LSB = 96mV	Table 15
VCONN ADC Results	0x8A	R	8	ADC result for VCONN measurements, LSB = 24mV	Table 15
Information3	0x90	R	13	Interrupt status. Multiple events possible	Table 12
Information4	0x91	R	13	Interrupt real time status	Table 12
Product Revision	0xFD	R	8	Product revision register. Read only	0x0003h
Manufacturer ID	0xFE	R	8	Manufacturers ID register. Read only	0x0049h
Device ID	0xFF	R	8	Device ID register. Read only	0x0011h

6.2 DAC Register Summary

Table 2. DAC Summary Table

	Charge Current Limit (R_{s2} = 10mΩ)	Max System Voltage	Min System Voltage	Adapter Current Limit1 (R_{s1} = 20mΩ)	Adapter Current Limit2 (R_{s1} = 20mΩ)	V_{IN} Voltage (ADP Min Voltage)	ACOK Reference for V_{IN} Comparison	ACProchot# (ACHOT) (R_{s1} = 20mΩ)	DCProchot# (DCHOT) (R_{s2} = 10mΩ)	OTG Voltage	OTG Current (R_{s1} = 20mΩ)
ADDR	**0x14**	**0x15**	**0x3E**	**0x3F**	**0x3B**	**0x4B**	**0x40**	**0x47**	**0x48**	**0x49**	**0x4A**
<0>	-	-	-	-	-	-	-	-	-		-
<1>	-	-	-	-	-	-	-	-	-		-
<2>	4mA	-	-	4mA	4mA	-	-	-	-		-
<3>	8mA	8mV	-	8mA	8mA	-	-	-	-	10mV	-
<4>	16mA	16mV	-	16mA	16mA	-	-	-	-	20mV	-
<5>	32mA	32mV	-	32mA	32mA	-	-	32mA	-	40mV	32mA
<6>	64mA	64mV	64mV	64mA	64mA	85.33mV	106.4mV	64mA	64mA	80mV	64mA
<7>	128mA	128mV	128mV	128mA	128mA	171mV	212.8mV	128mA	128mA	160mV	128mA
<8>	256mA	256mV	256mV	256mA	256mA	341mV	425.6mV	256mA	256mA	320mV	256mA
<9>	512mA	512mV	512mV	512mA	512mA	683mV	851.2mV	512mA	512mA	640mV	512mA
<10>	1024mA	1024mV	1024mV	1024mA	1024mA	1365mV	1702.4mV	1024mA	1024mA	1280mV	1024mA
<11>	2048mA	2048mV	2048mV	2048mA	2048mA	2731mV	3404.8mV	2048mA	2048mA	2560mV	2048mA
<12>	4096mA	4096mV	4096mV	4096mA	4096mA	5461mV	6809.6mV	4096mA	4096mA	5120mV	4096mA
<13>	-	8192mV	8192mV	-	-	10923mV	13619.2mV	-	8192mA	10240mV	-
<14>	-	16384mV	-	-	-	-	-	-	-	20480mV	-
<15>	-	-	-	-	-	-	-	-	-	-	-
Default	0mA	PROG	0mV	PROG	1.5A	4096mV	Disabled - 0mV	3072mA	4096mA	4770mV	512mA
Value	11'h000	PROG	8'h00	PROG	11'h077	8'h30	8'h00	8'h60	8'h40	12'h1dd	8'h10
Max	6140mA	18.304V	16.32V	6140mA	6140mA	16.384V	27.132V	6140mA	12300mA	22.88V	6112mA

6.3 Control Registers

The Control0, Control1, Control2, Control3, Control4, and Control7 registers configure the operation of the RAA489000 charger. To change certain functions or options after POR, write a 16-bit control command to any control register address. The write-word protocol is shown in Figure 25 and the data format is shown in Table 3, Table 4, Table 5, and Table 6.

Table 3. Control0 Register 0x39H

Bit	Bit Name	Description
<15>	VBUS Control Sink/Discharge	Enables or turns on the discharge FET to pull down the VBUS 0 = Disable, 10mA sink turned off (default) 1 = Enable, 10mA sink turned on
<14>	CSIN Auto Sink/Discharge	Enables or disables the discharge path for VIN for 50ms when entering the READY state 0 = Disable (default) 1 = Enable
<13>	CSOP Sink	Enables or turns on the discharge FET to pull down the VSYS/CSOP 0 = Disable, 10mA sink turned off (default) 1 = Enable, 10mA sink turned on
<12>	BGATE Off when VSYS OV	0 = Disable (Default) 1 = Enable
<11>	PPS Mode	0 = OFF (Default) 1 = ON
<10>	BGATE Force On	0 = BGATE normal operation (default) 1 = BGATE Forced ON (BGATE = VBAT + 5V)
<9:8>	Dither Enable	00 = Disable dither (default) 01 = Dither1x 10 = Dither2x 11 = Dither3x ADC must be enabled for Dither function to work
<7>	SMBus Timeout	Default time is 175s (see Control3<12:11> and SMBus Timeout) 0 = Enable the SMBus timeout function (default) 1 = Disable the SMBus timeout function
<6>	Not Used	Not used
<5>	Pass Through Mode	Enables or disables Pass Through mode 0 = Disable (default) 1 = Enable
<4:3>	DCProchot# Threshold in Battery Only Mode (Low Power Mode)	Configures the battery discharging current DCProchot# threshold in battery only Low Power mode indicated by the Information1 register 0x3A Bit<15>.
<2>	Input Voltage Regulation	Enables or disables the input voltage regulation loop 0 = Enable (default) 1 = Disable

Bit<4:3>	R_{S2} = 10mΩ (A)	R_{S2} = 20mΩ (A)	R_{S2} = 5mΩ (A)
00	12 (default)	6 (default)	24 (default)
01	10	5	20
10	8	4	16

Table 3. Control0 Register 0x39H (Cont.)

Bit	Bit Name	Description
<1>	VSYS Regulation Offset Voltage Adder	Adds offset above the VSYSMAX register setting when not charging. 384mV is always added to VSYS in Trickle Charge mode 0 = 0mV (default) 1 = 384mV
<0>	Digital OV and OTGUV Control	0 = Normal digital overvoltage, shuts down switching after debounce time (default) 1 = Disables the undervoltage for OTG and overvoltage digital for OTG and VSYS (see CTRL7<7>)

Table 4. Control1 Register 0x3CH

Bit	Bit Name	Description
<15:14>	General Purpose Comparator Debounce Time	Configures the general-purpose comparator assertion debounce time 00 = 2µs (default) 01 = 12µs 10 = 2ms 11 = 100µs
<13>	Exit Learn Mode	Provides the option to exit Learn mode when the battery voltage is lower than the MinSystemVoltage register setting 0 = Stay in Learn mode even if V_{BAT} < MinSystemVoltage register setting (default) 1 = Exit Learn mode if V_{BAT} < MinSystemVoltage register setting
<12>	Learn Mode	Enables or disables the Battery Learn mode used in NVDC mode only (see Battery Learn Mode) 0 = Disable (default) 1 = Enable To enter Learn mode, the BATGONE pin needs to be low (a battery must be present)
<11>	OTG Function	Enables or disables the OTG function. 0 = Disable OTG (default) 1 = Enable OTG (Adapter Output Power Supply)
<10>	Not Used	Not used
<9:7>	Switching Frequency	Configures the switching frequency 000 = 1500kHz 001 = 1235kHz 010 = 1050kHz 011 = 913kHz 100 = 808kHz 101 = 724kHz (default) 110 = 656kHz 111 = 600kHz
<6>	BGATE Force Off	Disables BGATE and forces the BGATE FET to turn off and overwrite Turbo mode. See NVDC Charger Behavior Truth Table 0 = Normal operation (default) 1 = Force BGATE off (BGATE = VBAT) (also disables Turbo Mode/Ideal Diode Mode)
<5>	AMON/BMON Function in Battery Only mode	Enables or disables the current monitor function AMON and BMON 0 = Enable AMON/BMON (default) 1 = Disable AMON/BMON Bit<5> is valid in Battery Only mode only. When the adapter is present, AMON/BMON is automatically enabled and Bit<5> becomes invalid

Table 4. Control1 Register 0x3CH (Cont.)

Bit	Bit Name	Description
<4>	AMON/BMON Selection	Selects AMON or BMON as the output of the AMON/BMON pin (see Control3<3> for direction) 0 = AMON (default) 1 = BMON
<3>	Not Used	Not used
<2:0>	Not Used	Not used

Table 5. Control2 Register 0x3DH

Bit	Bit Name	Description
<15:13>	Trickle Charging Current	Configures the charging current in Trickle Charging mode (with 10mΩ R_{S2}). 000 = 32mA (do not use) 001 = 64mA 010 = 96mA 011 = 128mA (default) 100 = 160mA 101 = 192mA 110 = 224mA 111 = 256mA
<12>	Two-Level Adapter Current Limit	Enables or disables the two-level adapter current limit function. (see Adapter Current Loop and Current Limit 1 and 2 and Two Level Current Limit) 0 = Disable (default) 1 = Enable
<11>	Fault Timer Debounce Time for OT and WOCP	Configures the debounce fault time for die Over-Temperature (OT) or Way Overcurrent (WOC). 0 = 1.3s (default) 1 = 150ms
<10:9>	PROCHOT# Debounce	Configures the PROCHOT# debounce time before its assertion for ACProchot# and DCProchot#. 00 = 10µs (default) 01 = 100µs 10 = 500µs 11 = 1ms
<8:6>	PROCHOT# Duration	Configures the minimum duration of the PROCHOT# signal when asserted. 000 = 10ms (default) 001 = 20ms 010 = 15ms 011 = 5ms 100 = 1ms 101 = 500µs 110 = 100µs 111 = 0s
<5>	JEITA Control Bit<1>	JEITA control bit<1> (see Table 7), Control4<14> for JEITA control bit<0> JEITA bit<1:0> truth table; 00 = General-purpose ADC input, NTC current source OFF (default) 01 = Original JEITA profiles, NTC current source ON 10 = Profile 1, NTC current source ON 11 = Profile 2, NTC current source ON

Table 5. Control2 Register 0x3DH (Cont.)

Bit	Bit Name	Description
<4>	CMIN Reference	Configures the general-purpose comparator reference voltage. 0 = 1.2V (default) 1 = 2V
<3>	General Purpose Comparator	Enables or disables the general-purpose comparator. 0 = Enable (default) 1 = Disable (interrupt enabled. Allows interrupt functionality on pin)
<2>	Comparator output Polarity (ALERT_B pin)	Configures the general-purpose comparator output polarity when asserted. The comparator reference voltage is connected at the inverting input node. 0 = Not inverted, ALERT_B is High when CMIN is higher than the reference (default) 1 = Inverted, ALERT_B is Low when CMIN is higher than the reference
<1>	Internal Resistor Compensation for COMPR RCOMP	Changes the internal compensation resistor to speed up or slow down the loop response for reverse modulator operations. 0 = Slower (default) 1 = Faster
<0>	Internal Resistor Compensation for COMPF RCOMP	Changes the internal compensation resistor to speed up or slow down the loop response for forward modulator operation. 0 = Slower (default) 1 = Faster

Table 6. Control3 Register 0x4CH

Bit	Bit Name	Description
<15>	Disable VSYSOK Comparator	Enable or disable the VSYSOK comparator. 0 = Enable (default) 1 = Disable
<14>	ACLIM Reload	Reloads the AdapterCurrentLimit1 register with the value set by the last read of the PROG pin resistor on the falling edge of ACOK to prepare for a new adapter attaching. 0 = Reload AdapterCurrentLimit1 register (default) 1 = Do not reload
<13>	Autonomous Charging Termination Time	Configures autonomous charging termination time. 0 = 20ms (default) 1 = 200ms
<12:11>	SMBus Charger Timeout	Configures SMBus Timeout time (see SMBus Timeout) 00 = 175s (default) 01 = 87.5s 10 = 43.75s 11 = 5.5s
<10>	DCM/CCM Hysteresis	0 = Disabled (default) 1 = Enables hysteresis for DCM to CCM boundary
<9:8>	Not Used	Not used
<7>	Charge Control	Enables Autonomous Charging mode (see Autonomous Charging Mode) 0 = SMBus Control, Battery charging current control through SMBus only (default) 1 = Enable Autonomous Charging mode (resets if the autonomous charging timer expires or a Fault occurs, PROCHOT# configured for autonomous charging mode indicator, End of Charge enabled)

Table 6. Control3 Register 0x4CH (Cont.)

Bit	Bit Name	Description
<6>	AC and CC Current Feedback Gain	Configures AC and CC feedback gain for high current applications. 0 = x1.0 (default) 1 = x0.5
<5>	Input Current Limit Loop	Enables or disables the input current limit loop. 0 = Enable input current limit loop (default) 1 = Disable input current limit loop
<4>	Input Current Limit Loop when BATGONE = 1	Enables or disables the input current limit loop when BATGONE = 1. 0 = Enable ACLIM when BATGONE = 1 (default) 1 = Disable ACLIM when BATGONE = 1
<3>	AMON/BMON Direction	Configures AMON/BMON direction (see Control1<4> for AMON/BMON selection). 0 = Forward; Adapter current monitor/battery charging current monitor (default) 1 = Reverse; Reverse output current monitor/battery discharging current monitor
<2>	Digital Reset	Reset all SMBus register value to POR default value, including re-reading PROG settings. 0 = Idle (default) 1 = Reset
<1>	Buck-Boost T2 Time in DCM	Configure the Buck-Boost T2 time in DCM (T2DCM). Reduces input ripple in DCM mode. 0 = Reduced T2 time (increased switching frequency in DCM) (default) 1 = Normal T2 time
<0>	Enable ADC	Specifies when to enable the ADC. 0 = ADC is active only when the adapter is plugged in and charging (default) 1 = Enables ADC for all modes

Table 7. Control4 Register 0x4EH

Bit	Bit Name	Description
<15>	BATGONE Disable	Configures the BATGONE input. 0 = Normal BATGONE input (default) 1 = Ignore BATGONE input
<14>	JEITA Control Bit<0>	JEITA Control Bit<0> (see Table 5, Control2<5> for JEITA Control Bit<1>) JEITA Bit<1:0> truth table; 00 = General-purpose ADC input, NTC current source OFF (default) 01 = Original JEITA profiles, NTC current source ON 10 = Profile 1, NTC current source ON 11 = Profile 2, NTC current source ON
<13>	Slew Rate Control	Controls the slew rate of VSYS and OTG voltages. 0 = Slew Rate Control disabled (default). 1 = Slew Rate Control enabled to ramp DAC voltage; OTG 0.46875mV/µs and VSYS 0.375mV/µs; Not recommended in OTG mode until after establishing 5V to prevent OV issues
<12>	Disable General Purpose Comparator in Battery Only Mode	Enables or disables General Purpose comparator in Battery Only mode. 0 = Enabled for all modes (default) 1 = Disabled for Battery Only mode (REF = 1.2V in Battery Only mode)
<11>	Not Used	Not used
<10>	Forced Forward Buck Mode	Enables or disables the Forced Forward Buck mode. 0 = Disable Forced Buck mode (default) 1 = Enable Forced Buck mode

Table 7. Control4 Register 0x4EH (Cont.)

Bit	Bit Name	Description
<9>	WOCP Function	Enables or disables the Way Over-Current Protection (WOCP) function 0 = Enable (default) 1 = Disable
<8>	VSYS Short Check	Enables or disables SYS short detection before enabling the modulator. 0 = Enable (default) 1 = Disable
<7>	OTGCURRENT PROCHOT#	Enables or disables trigger PROCHOT# with OTGCURRENT. It also applies to VBUS current when TCPC controls VBUS. 0 = Disable (default) 1 = Enable
<6>	BATGONE PROCHOT#	Enables or disables trigger PROCHOT# with BATGONE. 0 = Disable (default) 1 = Enable
<5>	ACOK PROCHOT#	Enables or disables trigger PROCHOT# with ACOK. 0 = Disable (default) 1 = Enable
<4>	GP Comparator PROCHOT#	Enables or disables trigger PROCHOT# with general-purpose comparator rising. 0 = Disable (default) 1 = Enable
<3:2>	ACOK falling or BATGONE Rising Debounce	Configures the debounce time from ACOK falling or BATGONE rising to PROCHOT# trip. 00 = 3µs (default) 01 = 25µs 10 = 125µs 11 = 250µs
<1>	PROCHOT# Clear	Clears PROCHOT# 0 = Idle (default) 1 = Clear PROCHOT#
<0>	PROCHOT# Latch	Manually resets PROCHOT# 0 = PROCHOT# signal auto-clear (default) 1 = Hold PROCHOT# low when tripped. Must be cleared using Bit<1>

Table 8. Control7 Register 0x38H

Bit	Bit Name	Description
<15:13>	T2 - Time corresponding to Adapter Current Limit 2 (Two level ACLIM enabled)	Select the Time corresponding to Adapter Current Limit 2 when Two Level Current Limit is enabled. 000 = 10µs (default) 001 = 100µs 010 = 500µs 011 = 1ms 100 = 300µs 101 = 750µs 110 = 2ms 111 = 10ms
<12:10>	T1 - Time Corresponding to Adapter Current Limit 1 (Two level ACLIM enabled)	Select the Time corresponding to Adapter Current Limit 1 when Two Level Current Limit is enabled. 000 = 10ms (default) 001 = 20ms 010 = 15ms 011 = 5ms 100 = 1ms 101 = 0.5m 110 = 0.1ms 111 = 0ms
<9:8>	End of Charge (EOC) Settings	End of charge settings when using Autonomous Charging mode CTRL3<7>. 00 = 120mA (default) 01 = 70mA 10 = 220mA 11 = 170mA
<7>	Analog OV Control	Configure the analog overvoltage control (also see CTRL3<15>). 0 = Normal, OV pulls down on comp and disables switching (default) 1 = Disable
<6:2>	Not Used	Not used
<1:0>	Buck-Boost Stretch CCM Period	Select the buck-boost stretch CCM period (T2 TIME). 00 = 2x (default) 01 = 3x 10 = 1x 11 = 0.6x

Table 9. Control8 Register 0x37H

Bit	Bit Name	Description
<15>	MCU LDO - Global	Enable or disable MCU LDO global. 0 = Disable 1 = Enable (default)
<14>	MCU LDO - BAT State	Enable or disable MCU LDO in BAT state. 0 = Enable (default) 1 = Disable
<13>	ASGATE ON - Ready State	Enable or disable ASGATE in Ready state. 0 = Disable 1 = Enable (default)
<12>	External Reference	Enable or disable external reference 0 = Disable (default) 1 = Enable
<11>	BGATE Tri-state	Tri-state the BGATE driver. 0 = BGATE normal operation (default) 1 = BGATE Tri-state
<10:6>	Low VSYS PROCHOT# Reference	Select the VSYS low PROCHOT# trigger reference voltage. 00000 = 5.6V (default) 00001 = 5.7V 00010 = 5.8V 00011 = 5.9V 00100 = 6.0V 00101 = 6.1V 00110 = 6.2V 00111 = 6.3V 01000 = 6.4V 01001 = 6.5V 01010 = 6.6V 01011 = 6.7V 01100 = 6.8V 01101 = 6.9V 01110 = 7.0V 01111 = 7.1V 10000 = 7.2V 10001 = 7.3V 10010 = 7.4V 10011 = 7.5V 10100 (and higher) = 7.6V
<5>	CC2 OVP	Enable or disable OVP for CC2 0 = Enable (default) 1 = Disable
<4>	CC1 OVP	Enable or disable OVP for CC1 0 = Enable (default) 1 = Disable

Table 9. Control8 Register 0x37H (Cont.)

Bit	Bit Name	Description
<3:2>	Not Used	Not used
<1:0>	VCONN_CC OCP Settings	Select the VCONN_CC OCP threshold. 00 = 800mA (default) 01 = 400mA 10 = 1600mA 11 = Disable

Table 10. Control 9 Register 0x36H

Bit	Bit Name	Description
<15:8>	Not used	Not used
<7>	Not Used	Not used
<6>	Not Used	Not used
<5:4>	Refresh Period	Select the period for refreshing the boot capacitor in deep DCM. 00 = 512µs (default) 01 = 216µs 10 = 128µs 11 = 32µs
<3>	CSIN Sink	Enables or turns on the discharge FET to pull down on CSIN for 50ms. 0 = Disable (default) 1 = Enable
<2>	Current Slew Rate Control	Enables or disables the current slew rate control. 0 = Disable (default) 1 = Enable
<1>	Trickle Charge Exit Debounce	Select the debounce time for exiting trickle charge. 0 = 10µs (default) 1 = 500ms
<0>	Force VCONN OFF	Force turn off both the VCONN switches. 0 = Yes (default) 1 = No

Table 11. Control 10 Register 0x35H

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td><15></td><td>DVC Mode (Secondary RAA489000)</td><td>Enable or disable the DVC operating mode for the secondary RAA489000.
0 = Disable (default)
1 = Enable</td></tr>
<tr><td><14:10></td><td>Rp1 DAC (Secondary RAA489000)</td><td>Select the Rp1 resistor value for secondary RAA489000.
<table><tr><td>00000: Disable DVC mode
00001: Rp1 = 36mΩ
00010: Rp1 = 40mΩ
00011: Rp1 = 44mΩ
00100: Rp1 = 48mΩ
00101: Rp1 = 52mΩ
00110: Rp1 = 56mΩ
00111: Rp1 = 60mΩ</td><td>01000: Rp1 = 64mΩ
01001: Rp1 = 68mΩ
01010: Rp1 = 72mΩ
01011: Rp1 = 76mΩ
01100: Rp1 = 80mΩ
01101: Rp1 = 84mΩ
01110: Rp1 = 88mΩ
01111: Rp1 = 92mΩ</td><td>10000: Rp1 = 96mΩ
10001: Rp1 = 100mΩ
10010: Rp1 = 104mΩ
10011: Rp1 = 108mΩ
10100: Rp1 = 112mΩ
10101: Rp1 = 116mΩ
10110: Rp1 = 120mΩ
10111: Rp1 = 124mΩ</td><td>11000: Rp1 = 128mΩ
11001: Rp1 = 132mΩ
11010: Rp1 = 136mΩ
11011: Rp1 = 140mΩ
11100: Rp1 = 144mΩ
11101: Rp1 = 148mΩ
11110: Rp1 = 152mΩ
11111: Rp1 = 156mΩ</td></tr></table></td></tr>
<tr><td><9></td><td>DVC Charge Mode (Primary RAA489000)</td><td>Enable or disable the DVC charge mode for the primary RAA489000.
0 = Disable (default)
1 = Enable</td></tr>
<tr><td><8></td><td>Charge Current Loop (Secondary RAA489000)</td><td>Enable or disable charge current loop for secondary RAA489000 in DVC operation.
0 = Enable CC loop (default)
1 = Disable CC loop</td></tr>
<tr><td><7></td><td>DVC Auto Zero Reset</td><td>Reset the DVC Auto Zero to default.
0 = Idle (default)
1 = Reset</td></tr>
<tr><td><6></td><td>DVC Trickle Charge (Primary RAA489000)</td><td>Enable or disable the DVC trickle charge mode for primary RAA489000.
0 = Disable (default)
1 = Enable</td></tr>
<tr><td><5></td><td>DVC Auto Zero (Secondary RAA489000)</td><td>Enable or disable auto zero for secondary RAA489000 in DVC operation.
0 = Enable auto zero (default)
1 = Disable auto zero</td></tr>
<tr><td><4:0></td><td>Rp2 DAC (Secondary RAA489000)</td><td>Select the Rp2 resistor value for secondary RAA489000.
<table><tr><td>00000: Rp2 = 0mΩ
00001: Rp2 = 4mΩ
00010: Rp2 = 8mΩ
00011: Rp2 = 12mΩ
00100: Rp2 = 16mΩ
00101: Rp2 = 20mΩ
00110: Rp2 = 24mΩ
00111: Rp2 = 28mΩ</td><td>01000: Rp2 = 32mΩ
01001: Rp2 = 36mΩ
01010: Rp2 = 40mΩ
01011: Rp2 = 44mΩ
01100: Rp2 = 48mΩ
01101: Rp2 = 52mΩ
01110: Rp2 = 56mΩ
01111: Rp2 = 60mΩ</td><td>10000: Rp2 = 64mΩ
10001: Rp2 = 68mΩ
10010: Rp2 = 72mΩ
10011: Rp2 = 76mΩ
10100: Rp2 = 80mΩ
10101: Rp2 = 84mΩ
10110: Rp2 = 88mΩ
10111: Rp2 = 92mΩ</td><td>11000: Rp2 = 96mΩ
11001: Rp2 = 100mΩ
11010: Rp2 = 104mΩ
11011: Rp2 = 108mΩ
11100: Rp2 = 112mΩ
11101: Rp2 = 116mΩ
11110: Rp2 = 120mΩ
11111: Rp2 = 124mΩ</td></tr></table></td></tr>
</table>

6.4 Interrupt Functionality

The ALERT_B must be enabled by setting Control2 Bit<3> = 1. See Table 5 for information about disabling the comparator output function. After the ALERT_B pin is enabled, select whether to allow only the faults or flags to be masked or unmasked and whether to have the ALERT_B trigger. If the flag is a fault, it must be read to clear the ALERT_B. The interrupt control registers support 13 possible functions. ALERT_B is an active low, open-drain output that is shared with the GP comparator. ALERT_B pulls low to signal an interrupt event and requires a pull up source to toggle.

The Information4 register provides the event real-time status. It always shows the event flag even if the interrupt is not enabled. This could be as small as a one clock pulse and may not be useful without being latched, such as for Changed NTC Temperature Boundary.

Set the Control5 bit to 1 to enable the corresponding trigger interrupt. Set Control5 bit to 0 to mask a trigger interrupt and ignore the event.

The Control6 bit controls the logic level for a given interrupt signal. Setting Control6 to 0 causes the ALERT_B pin to go low when an interrupt occurs. Setting Control6 to 1 causes the ALERT_B pin to go high for a fault.

The Information3 register only shows results for unmasked/enabled events. Interrupt flags are cleared by reading the status bit in the Information3 register, but only if the fault condition has been removed or the level is changed. To catch the opposite edge, such as when leaving an event, toggle the appropriate bit in Control6.

Table 12. Interrupt Control and Status Registers

Bit #	Control Inputs			Flag Outputs			Description
	Control5 Interrupt Mask		Control6 Interrupt Trigger Level	Information3 Interrupt Status		Information4 Interrupt Real Time Status	
	Address:0x4F		Address:0x43	Address:0x90		Address:0x91	
	0 = Not enabled 1 = Enabled		0 = Event triggers when low 1 = Event is triggers when high	0 = No event 1 = Event Set interrupt flag		0 = Not in state 1 = In this state	
	R/W	Default	Default	R/W	Default	Default	
12	R/W	0	1	R	0	0	SMBus timeout timer expired
11	R/W	0	1	R	0	0	12-hour charge timer expired for Autonomous Charging mode only
10	R/W	0	1	R	0	0	SYS OV
9	R/W	0	1	R	0	0	ADP OV
8	R/W	0	1	R	0	0	ADP VMIN (selector info)
7	R/W	0	1	R	0	0	ADP current (selector info)
6	R/W	0	1	R	0	0	Thermal warning (T_J)
5	R/W	0	1	R	0	0	OTGPG
4	R/W	0	1	R	0	0	Battery charging terminated for Autonomous Charging mode only
3	R/W	0	1	R	0	0	Battery charging CC to CV
2	R/W	0	1	R	0	0	FET fault state
1	R/W	0	1	R	0	0	Enter READY
0	R/W	0	1	R	0	0	Changed NTC temperature boundary

6.5 Information Register

The information register contains SMBus readable information about Manufacturing mode and Operating mode. Tables 13 and 14 identify the bit locations of the information available.

Table 13. Information1 Register 0x3AH

Bit	Bit Name	Description
<0>	Ideal Diode Mode Status	0 = Ideal Diode mode is not active 1 = Ideal Diode mode is active
<1>	Not Used	Not used
<2>	ASGATE Charge Pump Status[1]	0 = ASGATE charge pump is not good 1 = ASGATE charge pump is good
<3>	Not used	Not used
<4>	Trickle Charge Mode Status	0 = Trickle Charging mode is not active 1 = Trickle Charging mode is active
<5>	VIN to VOUT Comparator Status	VIN to VOUT comparator (Rising threshold = +800mV, Falling threshold = +400mV) 0 = VIN < VSYS 1 = VIN > VSYS
<6>	BGATE Charge Pump Status[1]	0 = BGATE charge pump is not good 1 = BGATE charge pump is good
<7>	Not used	Not used
<8>	PPS Mode Status	0 = PPS Mode is not active 1 = PPS Mode is active
<9>	Pass Through Mode Status	0 = Pass Through Mode not active 1 = Pass Through Mode active
<10>	VSYS Low PROVHOT# Status	Indicates whether the Low_VSYS_Prochot# is tripped 0 = Low_VSYS PROCHOT# is not tripped 1 = Low_VSYS PROCHOT# is tripped
<11>	DCPROCHOT# Status	Indicates whether DCProchot# is tripped 0 = DCProchot# is not tripped 1 = DCProchot# is tripped
<12>	ACPROCHOT# Status	Indicates whether ACProchot#/OTGCURRENTProchot# is tripped 0 = ACProchot#/OTGCURRENTProchot# is not tripped 1 = ACProchot#/OTGCURRENTProchot# is tripped
<14:13>	Active Control Loop	Indicates the active control loop 00 = MaxSystemVoltage control loop is active 01 = Charging current loop is active 10 = Input adapter current limit loop is active 11 = Input voltage loop is active
<15>	VDD Status	Indicates whether VDD is above or below the 3.8V threshold. 0 = VDD is below 3.8V 1 = VDD is above 3.8V

1. Depending on the leakage on pin, the bit may or may not toggle unless set to 100% Charge Pump mode using CTRL3 Bit<6> (Tables 3).

Table 14. Information2 Register 0x4DH

Bit	Bit Name	Description
<4:0>	PROG Resistor Read-Out	Program resistor read out (See Table 84 on page 82). Number of battery cells I^2C address Adapter current limit 1
<7:5>	Power Stage Operation Mode	Indicates the RAA489000 operation mode 001 = Forward Boost mode 010 = Forward Buck mode 011 = Forward Buck-Boost mode 101 = Reverse Boost mode 110 = Reverse Buck mode 111 = Reverse Buck-Boost mode
<11:8>	State Machine	Indicates the RAA489000 state machine status. 0000 = RESET 0001, 0011, 0101, 1000, 1011 = STARTUP. The IC wakes up internal circuits biases, reads trim, and autozeros comparators. Wait state for VDD > 3.8V 0010 = ACHRG (Charge state). The system is charging the battery through the Autocharge setting. 0100 = BAT. Battery only mode with ADC, and OTG disabled (ACOK is low) 0110 = CHRG (Charge state). Charging is enabled and system is charging the battery through SMBus charging. 0111 = FAULT. OTP or WOCP is triggered 1001 = OTG. The charger is operating Reverse/OTG mode 1010 = READY. The charger is not switching but the circuits are biased and ready (for example, with the MaxSystemVoltage register set to 0). The READY state can also be reached by enabling ADC in Battery Only mode (from the BAT state). 1100 = VSYS. The charger is in the forward mode and switching. The system voltage or adapter current (or input voltage) can be regulated in this state. 1101 = DVCHRG. The charger is in the Dynamic Voltage Compensation (DVC) mode. The charger is operating as a VR and regulating system voltage to charge the battery.
<12>	BATGONE Pin Status	Indicates the BATGONE pin status. 0 = Battery is present 1 = No battery
<13>	General Purpose Comparator Status	Indicates the general purpose comparator output after debounce time. 0 = Comparator output is low 1 = Comparator output is high
<14>	ACOK Status	Indicates the ACOK status. 0 = No adapter 1 = Adapter is present
<15>	Not used	Not used

6.6 ADC Registers

Table 15. ADC Output Value Bits

ADDR	Description	LSB	Sample Window Time	Polling Time
Control3 Reg 0x4C Bit<0> (see Table 6)	0 = Disables ADC, except when required for charging state machine 1 = Enables ADC			
0x80	[9:0] NTC voltage If enabled as general-purpose ADC, voltage [9:0] = 0V to 2.040V	8mV	106.66µs (x3)	100ms
0x81	VBAT voltage [13:6] = 0V to 16.32V	64mV	106.66µs	853µs
0x82	Internal junction temperature [7:0] T_J voltage = 0V to 2.040V.	8mV	106.66µs	100ms
0x83	Input current (R_{s1} = 20mΩ)	22.2mA	106.66µs	853µs
0x84	Battery discharge current (R_{s2} = 10mΩ)	44.4mA	106.66µs	853µs
0x85	Battery charge current (R_{s2} = 10mΩ)	22.2mA	106.66µs	853µs
0x86	CSOP (VSYS) voltage [13:6] VSYS voltage = 0V to 24.48V.	96mV	106.66µs	853µs
0x87	CSIN (V_{IN}) voltage [13:6] V_{IN} voltage = 0V to 24.48V.	106.4mV	106.66µs	853µs
0x89	VBUS voltage [13:6] VSYS voltage = 0V to 24.48V.	96mV	106.66µs	853µs
0x8A	VCONN/CC1/CC2 voltage [13:6] V_{IN} voltage = 0V to 24.48V.	24mV	106.66µs	853µs

6.7 TCPC Registers

6.7.1 TCPC Registers - Register Map

Table 16. TCPC Register Map

Address	Register Name	Register Table	Type	Reset Value
00h...01h	VENDOR_ID	Table 18	R	045Bh
02h...03h	PRODUCT_ID	Table 19	R	0256h
04h...05h	DEVICE_ID	Table 20	R	0100h
06h...07h	USBTYPEC_REV	Table 21	R	0012h
08h...09h	USBPD_REV_VER	Table 22	R	3011h
0Ah...0Bh	PD_INTERFACE_REV	Table 23	R	2010h
0Ch...0Fh	Reserved			
10h...11h	ALERT	Table 24	R/W	0200h
12h...13h	ALERT_MASK	Table 25	R/W	6FFFh
14h	POWER_STATUS_MASK	Table 26	R/W	FFh
15h	FAULT_STATUS_MASK	Table 27	R/W	BFh
16h	EXTENDED_STATUS_MASK	Table 28	R/W	01h
17h	ALERT_EXTENDED_MASK	Table 29	R/W	07h
18h	Reserved			
19h	TCPC_CONTROL	Table 30	R/W	00h

Table 16. TCPC Register Map (Cont.)

Address	Register Name	Register Table	Type	Reset Value
1Ah	ROLE_CONTROL	Table 31	R/W	0Ah
1Bh	FAULT_CONTROL	Table 32	R/W	00h
1Ch	POWER_CONTROL	Table 33	R/W	60h
1Dh	CC_STATUS	Table 34	R	00h
1Eh	POWER_STATUS	Table 35	R	40h
1Fh	FAULT_STATUS	Table 36	R/W	80h
20h	EXTENDED_STATUS	Table 37	R	01h
21h	ALERT_EXTENDED	Table 38	R/W	00h
22h	Reserved			
23h	COMMAND	Table 39	W	00h
24h...25h	DEVICE_CAPABILITIES_1	Table 40	R	EEBFh
26h...27h	DEVICE_CAPABILITIES_2	Table 41	R	2AE3h
28h	STANDARD_INPUT_ CAPABILITIES	Table 42	R	00h
29h	STANDARD_OUTPUT_ CAPABILITIES	Table 43	R	00h
2Ah - 2Bh	Reserved			
2Ch...2Dh	GENERIC_TIMER	Table 44	W	0000h
2Eh	MESSAGE_HEADER_INFO	Table 45	R/W	02h
2Fh	RECEIVE_DETECT	Table 46	R/W	00h
RECEIVE_BUFFER (Always Read at Address 30h) for TCPCi 2.0				
30h	READABLE_BYTE_COUNT	Table 47	R	00h
	RX_BUF_FRAME_TYPE	Table 48	R	00h
	RX_BUF_BYTE_x	Table 49	R	00h
31h...4Fh	Reserved			
RECEIVE_BUFFER for TCPCi 1.0				
30h	RECEIVE_BYTE_COUNT	Table 50	R	00h
31h	RX_BUF_FRAME_TYPE	Table 51	R	00h
32h	RX_BUF_HEADER_BYTE_0	Table 52	R	00h
33h	RX_BUF_HEADER_BYTE_1		R	00h

Table 16. TCPC Register Map (Cont.)

Address	Register Name	Register Table	Type	Reset Value
34h	RX_BUF_OBJ1_BYTE_0	Table 53	R	00h
35h	RX_BUF_OBJ1_BYTE_1		R	00h
36h	RX_BUF_OBJ1_BYTE_2		R	00h
37h	RX_BUF_OBJ1_BYTE_3		R	00h
38h	RX_BUF_OBJ2_BYTE_0		R	00h
39h	RX_BUF_OBJ2_BYTE_1		R	00h
3Ah	RX_BUF_OBJ2_BYTE_2		R	00h
3Bh	RX_BUF_OBJ2_BYTE_3		R	00h
3Ch	RX_BUF_OBJ3_BYTE_0		R	00h
3Dh	RX_BUF_OBJ3_BYTE_1		R	00h
3Eh	RX_BUF_OBJ3_BYTE_2		R	00h
3Fh	RX_BUF_OBJ3_BYTE_3		R	00h
40h	RX_BUF_OBJ4_BYTE_0		R	00h
41h	RX_BUF_OBJ4_BYTE_1		R	00h
42h	RX_BUF_OBJ4_BYTE_2		R	00h
43h	RX_BUF_OBJ4_BYTE_3		R	00h
44h	RX_BUF_OBJ5_BYTE_0		R	00h
45h	RX_BUF_OBJ5_BYTE_1		R	00h
46h	RX_BUF_OBJ5_BYTE_2		R	00h
47h	RX_BUF_OBJ5_BYTE_3		R	00h
48h	RX_BUF_OBJ6_BYTE_0		R	00h
49h	RX_BUF_OBJ6_BYTE_1		R	00h
4Ah	RX_BUF_OBJ6_BYTE_2		R	00h
4Bh	RX_BUF_OBJ6_BYTE_3		R	00h
4Ch	RX_BUF_OBJ7_BYTE_0		R	00h
4Dh	RX_BUF_OBJ7_BYTE_1		R	00h
4Eh	RX_BUF_OBJ7_BYTE_2		R	00h
4Fh	RX_BUF_OBJ7_BYTE_3		R	00h
50h	TRANSMIT	Table 54	R/W	00h
TRANSMIT_BUFFER (Always Write at Address 51h) for TCPCi 2.0				
51h	I2C_WRITE_BYTE_COUNT	Table 55	W	00h
	TX_BUF_BYTE_x	Table 56	W	00h
TRANSMIT_BUFFER for TCPCi 1.0				
51h	TRANSMIT_BYTE_COUNT	Table 57	R/W	00h
52h	TX_BUF_HEADER_BYTE_0	Table 58	R/W	00h
53h	TX_BUF_HEADER_BYTE_1		R/W	00h

Table 16. TCPC Register Map (Cont.)

Address	Register Name	Register Table	Type	Reset Value
54h	TX_BUF_OBJ1_BYTE_0	Table 59	R/W	00h
55h	TX_BUF_OBJ1_BYTE_1		R/W	00h
56h	TX_BUF_OBJ1_BYTE_2		R/W	00h
57h	TX_BUF_OBJ1_BYTE_3		R/W	00h
58h	TX_BUF_OBJ2_BYTE_0		R/W	00h
59h	TX_BUF_OBJ2_BYTE_1		R/W	00h
5Ah	TX_BUF_OBJ2_BYTE_2		R/W	00h
5Bh	TX_BUF_OBJ2_BYTE_3		R/W	00h
5Ch	TX_BUF_OBJ3_BYTE_0		R/W	00h
5Dh	TX_BUF_OBJ3_BYTE_1		R/W	00h
5Eh	TX_BUF_OBJ3_BYTE_2		R/W	00h
5Fh	TX_BUF_OBJ3_BYTE_3		R/W	00h
60h	TX_BUF_OBJ4_BYTE_0		R/W	00h
61h	TX_BUF_OBJ4_BYTE_1		R/W	00h
62h	TX_BUF_OBJ4_BYTE_2		R/W	00h
63h	TX_BUF_OBJ4_BYTE_3		R/W	00h
64h	TX_BUF_OBJ5_BYTE_0		R/W	00h
65h	TX_BUF_OBJ5_BYTE_1		R/W	00h
66h	TX_BUF_OBJ5_BYTE_2		R/W	00h
67h	TX_BUF_OBJ5_BYTE_3		R/W	00h
68h	TX_BUF_OBJ6_BYTE_0		R/W	00h
69h	TX_BUF_OBJ6_BYTE_1		R/W	00h
6Ah	TX_BUF_OBJ6_BYTE_2		R/W	00h
6Bh	TX_BUF_OBJ6_BYTE_3		R/W	00h
6Ch	TX_BUF_OBJ7_BYTE_0		R/W	00h
6Dh	TX_BUF_OBJ7_BYTE_1		R/W	00h
6Eh	TX_BUF_OBJ7_BYTE_2		R/W	00h
6Fh	TX_BUF_OBJ7_BYTE_3		R/W	00h
70h...71h	VBUS_VOLTAGE	Table 60	R	0000h
72h...73h	VBUS_SINK_DISCONNECT_THRESHOLD	Table 61	R/W	008Ch
74h...75h	VBUS_STOP_DISCHARGE_THRESHOLD	Table 62	R/W	0020h
76h...77h	VBUS_VOLTAGE_ALARM_HI_CFG	Table 63	R/W	0000h
78h...79h	VBUS_VOLTAGE_ALARM_LO_CFG	Table 64	R/W	0000h
7Ah...7Bh	VBUS_NONDEFAULT_TARGET	Table 65	R/W	0000h
7Ch...7Fh	Reserved			
Vendor Defined				
80h...81h	TCPC_SETTING_1	Table 66	R/W	0000h

Table 16. TCPC Register Map (Cont.)

Address	Register Name	Register Table	Type	Reset Value
82h...83h	TCPC_PARAMETER_1	Table 67	R/W	0190h
84h...85h	TCPC_PARAMETER_2	Table 68	R/W	2858h
86h...87h	Reserved			
88h	TCPC_VENDOR_CONTROL_3	Table 69	R/W	00h
89h	Reserved			
8Ah	TCPC_VENDOR_STATUS_MASK	Table 70	R/W	00h
8Bh	TCPC_VENDOR_STATUS	Table 71	R	00h
8Ch...8Fh	Reserved			
90h…91h	VBUS_5V_TARGET	Table 72	R/W	0107h
92h...93h	VBUS_CURRENT_TARGET	Table 73	R/W	0064h
94h...95h	VBUS_OCP_UV_THRESHOLD	Table 74	R/W	0000h
96h...97h	STOP_DISCHARGE_THRESHOLD_VSAFE0V	Table 75	R/W	1010h
98h	VIN_STOP_DISCHARGE_THRESHOLD_VSAFE0V	Table 76	R/W	04h
99h	Reserved			
9Ah...9Bh	VBUS_PRESENT_THRESHOLD	Table 77	R/W	0096h
9Ch...9Dh	VCONN_VOLTAGE	Table 78	R	0000h
9Eh...BFh	Reserved			
C0h...C1h	TYPE_C_SETTING_1	Table 79	R/W	0000h
C2h...DFh	Reserved			
E0h...E1h	PD_PHYSICAL_SETTING_1	Table 80	R/W	0000h
E2h...E3h	PD_PHYSICAL_SETTING_2	Table 81	R/W	5000h
E4h...E7h	Reserved			
E8h...E9h	PD_PHYSICAL_PARAMETER_1	Table 82	R/W	6C07h
EAh...EBh	PD_PHYSICAL_PARAMETER_2	Table 83	R/W	0249h
ECh...FFh	Reserved			

6.7.2 Register Description

The following is the functional description for each register.

The table of register function is described with 16-bit units or 8-bit units for convenience. Table 17 defines the common abbreviations used.

Table 17. Common Abbreviations Used

Abbreviation	Definition
RW	Read/Write
R	Read Only (Write1/0 ignore)
W	Write Only
RW1C	Read. Write 1 Clear (Write 0 ignore)

6.7.2.1 VENDOR_ID (00h)

A Vendor ID, or VID, is used to identify the TCPC vendor.

Table 18. VENDOR_ID Register Definition

Bit(s)	Name	Type	Reset Value	Description
<15:0>	Vendor ID (VID)	R	045Bh	A unique 16-bit unsigned integer assigned by the USB-IF to the Vendor.

6.7.2.2 PRODUCT_ID (02h)

The Product ID, or PID, is used to identify the product.

Table 19. PRODUCT_ID Register Definition

Bit(s)	Name	Type	Reset Value	Description
<15:0>	USB Product ID (PID)	R	0256h	A unique 16-bit unsigned integer assigned uniquely by the Vendor to identify the TCPC.

6.7.2.3 DEVICE_ID (04h)

The Device ID (bcdDevice) is used to identify the release version of the product.

The TCPC indicates the input value of repvin in Bits [3:0].

Table 20. DEVICE_ID Register Definition

Bit(s)	Name	Type	Reset Value	Description
<15:0>	bcdDevice	R	0100h	A unique 16-bit unsigned integer assigned by the Vendor to identify the version of the TCPC bits [3:0] are programmable through TieHi/Lo cells

6.7.2.4 USBTYPEC_REV (06h)

This register refers to USB Type-C Cable and Connector Specification Revision, USB Type-C represented by a unique 16-bit unsigned register.

Table 21. USBTYPEC_REV Register Definition

Bit(s)	Name	Type	Reset Value	Description
<15:8>	Reserved	R	00h	Set to 0
<7:0>	bcdUSBTYPEC Release	R	12h	0001 0010 – Release 1.2

6.7.2.5 USBPD_REV_VER (08h)

This register refers to USB PD Specification Revision and Version, USB PD represented by a unique 16-bit unsigned integer.

Table 22. USBPD_REV_VER Register Definition

Bit(s)	Name	Type	Reset Value	Description
<15:8>	bcdUSBPD Revision	R	30h	0011 0000 – Revision 3.0
<7:0>	bcdUSBPD Version	R	11h	0001 0001 – Version 1.1

6.7.2.6 USB-Port Controller Interface Specification Revision (PD_INTERFACE_REV) (0Ah)

The USB-Port Controller Specification Revision register refers to this Specification Revision and Version represented by a unique 16-bit unsigned integer.

Table 23. PD_INTERFACE_REV Register Definition

Bit(s)	Name	Type	Reset Value	Description
<15:8>	bcd USB-PD Inter-Block Specification Revision	R	20h	0001 0000 – Revision 1.0 0010 0000 – Revision 2.0
<7:0>	bcd USB-PD Inter-Block Specification Version	R	10h	0001 0000 – Version 1.0

6.7.2.7 ALERT (10h)

This register is set by the TCPC and cleared by the TCPM.

This register is used to communicate a status change from the TCPC to the TCPM. After an event or condition occurs, the TCPC sets the corresponding bit in the ALERT register. The TCPC keeps the bit associated with the ALERT_C pin asserted until the TCPM writes a 1 to clear it. This register is initialized at power on.

The TCPC indicates an alert status change has occurred by presenting a logical 1 in the corresponding alert bit position in this register and asserting the ALERT_C pin. The TCPM clears the ALERT bit by writing a logical 1 to the respective ALERT bit position. The TCPM can clear any number of ALERT bits in a single write by setting multiple bits to logical 1 and the rest of the bits in the register to logical 0. The TCPM writing a logical 0 to any ALERT bit has no effect, and therefore does not cause those ALERT bits to be set or cleared. The ALERT_C pin remains asserted until all ALERT bits are cleared by the TCPM. If the TCPM writes a logical 1 to a bit that is already logical 0, the TCPC does not change the value of that bit.

Writing a 1 to ALERT.RxBufferOverflow does not clear it unless the TCPM also writes a 1 to ALERT.ReceiveSOP*MessageStatus. The ALERT.RxBufferOverflow is always asserted if the SOP* buffer registers are full, and those registers can only be cleared by writing a 1 to ALERT.ReceiveSOP*MessageStatus.

Table 24. ALERT Register Definition

Bit(s)	Name	Type	Reset Value	Description
<15>	Vendor Defined Alert	R/W1C	0b	0b: Cleared 1b: A vendor defined alert has been detected. Read the TCPC_VENDOR_STATUS register.
<14>	Alert Extended	R/W1C	0b	0b: Cleared 1b: An extended interrupt event has occurred. Read the ALERT_EXTENDED register.

Table 24. ALERT Register Definition (Cont.)

Bit(s)	Name	Type	Reset Value	Description
<13>	Extended Status	R/W1C	0b	0b: Cleared, 1b: Extended Status changed
<12>	Reserved	R	0b	Sets to zero by sender and ignored by receiver
<11>	VBUS Sink Disconnect Detected	R/W1C	0b	0b: Cleared 1b: A VBUS Sink Disconnect Threshold crossing has been detected This field asserts only when power role of TCPC is SNK and TCPM has set POWER_CONTROL.AutoDischargeDisconnect to 1. The TCPC detects VBUS falling below only VBUS_SINK_DISCONNECT_THRESHOLD.
<10>	Rx Buffer Overflow	R/W1C	0b	0b: TCPC Rx buffer is functioning properly 1b: TCPC Rx buffer has overflowed. Future GoodCRC are not sent. Writing 1 to this register acknowledges the overflow. The overflow is cleared by writing to ALERT.ReceiveSOP*MessageStatus
<9>	Fault	R/W1C	1b	0b: No fault 1b: A fault has occurred. Read the FAULT_STATUS register
<8>	VBUS Voltage Alarm Lo	R/W1C	0b	0b: Cleared 1b: A low-voltage alarm has occurred This field maintains assertion when a low-voltage alarm has occurred. If TCPM does not expect this detection, it should be set POWER_CONTROL.<5>(Disable Voltage Alarms) to 1.
<7>	VBUS Voltage Alarm Hi	R/W1C	0b	0b: Cleared 1b: A high-voltage alarm has occurred This field maintain assert during a high-voltage alarm has occurred. If TCPM does not expect this detection, it should be set POWER_CONTROL.<5> (Disable Voltage Alarms) to 1.
<6>	Transmit SOP* Message Successful	R/W1C	0b	0b: Cleared, 1b: Reset or SOP* message transmission successful. GoodCRC response received on SOP* message transmission.
<5>	Transmit SOP* Message Discarded	R/W1C	0b	0b: Cleared, 1b: Reset or SOP* message transmission not sent due to an incoming receive message. Transmit SOP* message buffer registers are empty.
<4>	Transmit SOP* Message Failed	R/W1C	0b	0b: Cleared, 1b: SOP* message transmission not successful, no GoodCRC response received on SOP* message transmission. Transmit SOP* message buffer registers are empty.
<3>	Received Hard Reset	R/W1C	0b	0b: Cleared, 1b: Received Hard Reset message
<2>	Received SOP* Message Status	R/W1C	0b	0b: Cleared, 1b: RECEIVE_BUFFER register changed. READABLE_BYTE_COUNT being set to 0 does not set this bit.

Table 24. ALERT Register Definition (Cont.)

Bit(s)	Name	Type	Reset Value	Description
<1>	Power Status	R/W1C	0b	0b: Cleared, 1b: Power Status changed There is a case when this field is asserted but some fields of POWER_STATUS are not asserted. See the following: ▪ This field will assert when TCPC has completed initialization and all registers are valid, and then the POWER_STATUS.B6 (TCP Initialization status) will be cleared. ▪ This field also asserts when TCPC wakes from I2CIdle and then TCPC does not assert any field of POWER_STATUS. More information is refer to 4.8.1 of TCPC specs.
<0>	CC Status	R/W1C	0b	0b: Cleared, 1b: CC Status changed TCPC does not assert this bit when CC_STATUS.Looking4Connection changes state if TCPC_CONTROL.EnableLooking4ConnectionAlert is set to 0. When TCPM sets TCPC_CONTROL. EnableLooking4ConnectionAlert set to 0, TCPC will not assert this field if CC_STATUS.Looking4Connection has changed. When TCPM sets ROLE_CONTROL.DRP to 0, CC2 to Open, and CC1 to Open, TCPC will not assert this field even if CC2 and CC1 status has changed.

6.7.2.8 ALERT_MASK (12h)

This is an event interrupt mask. It is masked and unmasked by the TCPM. The ALERT_MASK Register is cleared by the TCPM. This register is initialized at power on or Hard Reset.

The assertion of the ALERT_C pin is prevented when the corresponding bit in this register is set to zero by the TCPM. Setting any bits in this register has no effect on ALERT registers. (Even if TCPM sets each field to 0 (masked), each field of the ALERT register updates. This register masks only the ALERT_C pin, it has no effect on the ALERT register.)

Table 25. ALERT_MASK Register Definition

Bit(s)	Name	Type	Reset Value	Description
<15>	Vendor Defined Alert	R/W	0b	0b: Interrupt masked, 1b: Interrupt unmasked
<14>	Alert Extended Interrupt Mask	R/W	1b	0b: Interrupt masked, 1b: Interrupt unmasked
<13>	Extended Status Interrupt Mask	R/W	1b	0b: Interrupt masked, 1b: Interrupt unmasked
<12>	Reserved	R	0b	Sets to zero by sender and ignored by receiver
<11>	VBUS Sink Disconnect Detected	R/W	1b	0b: Interrupt masked, 1b: Interrupt unmasked
<10>	Rx Buffer Overflow	R/W	1b	0b: Interrupt masked, 1b: Interrupt unmasked
<9>	Fault	R/W	1b	0b: Interrupt masked, 1b: Interrupt unmasked
<8>	VBUS Voltage Alarm Lo	R/W	1b	0b: Interrupt masked, 1b: Interrupt unmasked

Table 25. ALERT_MASK Register Definition (Cont.)

Bit(s)	Name	Type	Reset Value	Description
<7>	VBUS Voltage Alarm Hi	R/W	1b	0b: Interrupt masked, 1b: Interrupt unmasked
<6>	Transmit SOP* Message successful Interrupt Mask	R/W	1b	0b: Interrupt masked, 1b: Interrupt unmasked
<5>	Transmit SOP* Message discarded Interrupt Mask	R/W	1b	0b: Interrupt masked, 1b: Interrupt unmasked
<4>	Transmit SOP* Message failed Interrupt Mask	R/W	1b	0b: Interrupt masked, 1b: Interrupt unmasked
<3>	Received Hard Reset Message Status Interrupt Mask	R/W	1b	0b: Interrupt masked, 1b: Interrupt unmasked (The Hard Reset should generally not be masked)
<2>	Receive SOP* Message Status Interrupt Mask	R/W	1b	0b: Interrupt masked, 1b: Interrupt unmasked
<1>	Power Status Interrupt Mask	R/W	1b	0b: Interrupt masked, 1b: Interrupt unmasked
<0>	CC Status Interrupt Mask	R/W	1b	0b: Interrupt masked, 1b: Interrupt unmasked

6.7.2.9 POWER_STATUS_MASK (14h)

This is an event interrupt mask. It is masked and unmasked by the TCPM. This register allows individual masking of power events. The POWER_STATUS_MASK Register is cleared by the TCPM. This register is initialized at power on or Hard Reset.

The POWER_STATUS_MASK is nested Alert. A POWER_STATUS change has to be unmasked in both the POWER_STATUS_MASK and the ALERT.PowerStatusInterruptMask to enable the ALERT_C pin.

The assertion of the ALERT_C pin is prevented when the corresponding bit is set to zero by the TCPM.

Table 26. POWER_STATUS_MASK Register Definition

Bit(s)	Name	Type	Reset Value	Description
<7>	Debug Accessory Connected Status Mask	R/W	1b	0b: Interrupt masked, 1b: Interrupt unmasked
<6>	TCPC Initialization Status Mask	R/W	1b	0b: Interrupt masked, 1b: Interrupt unmasked
<5>	Sourcing Nondefault Voltage Status Interrupt Mask	R/W	1b	0b: Interrupt masked, 1b: Interrupt unmasked
<4>	Sourcing VBUS Status Interrupt Mask	R/W	1b	0b: Interrupt masked, 1b: Interrupt unmasked
<3>	VBUS Detection Status Interrupt Mask	R/W	1b	0b: Interrupt masked, 1b: Interrupt unmasked
<2>	VBUS Present Status Interrupt Mask	R/W	1b	0b: Interrupt masked, 1b: Interrupt unmasked

Table 26. POWER_STATUS_MASK Register Definition (Cont.)

Bit(s)	Name	Type	Reset Value	Description
<1>	VCONN Present Status Interrupt Mask	R/W	1b	0b: Interrupt masked, 1b: Interrupt unmasked
<0>	Sinking VBUS Status Interrupt Mask	R/W	1b	0b: Interrupt masked, 1b: Interrupt unmasked

6.7.2.10 FAULT_STATUS_MASK (15h)

This is an event interrupt mask. It is masked and unmasked by the TCPM. This register allows individual masking of fault events. The FAULT_STATUS_MASK Register is cleared by the TCPM. The FAULT_STATUS_MASK Register is initialized on power on.

The FAULT_STATUS_MASK is nested Alert. A FAULT_STATUS change has to be unmasked in both the FAULT_STATUS_MASK and the ALERT.PowerStatusInterruptMask to enable the ALERT_C pin.

The assertion of the ALERT_C pin is prevented when the corresponding bit is set to zero by the TCPM.

Table 27. FAULT_STATUS_MASK Register Definition

Bit(s)	Name	Type	Reset Value	Description
<7>	AllRegistersResetTo Default	R/W	1b	0b: Interrupt masked, 1b: Interrupt unmasked The condition that generates a FAULT_STATUS.AllRegistersResetToDefault Interrupt also resets this bit; therefore, writing a 0b to this bit does not mask FAULT_STATUS.AllRegistersResetToDefault Interrupt.
<6>	Reserved	R	0b	Sets to zero by sender and ignored by receiver
<5>	Auto Discharge Failed Mask	R/W	1b	0b: Interrupt masked, 1b: Interrupt unmasked
<4>	Force Discharge Failed Mask	R/W	1b	0b: Interrupt masked, 1b: Interrupt unmasked
<3>	Internal OCP VBUS Overcurrent Protection Fault Interrupt Status Mask	R/W	1b	0b: Interrupt masked, 1b: Interrupt unmasked
<2>	Internal OVP VBUS Overvoltage Protection Fault Interrupt Status Mask	R/W	1b	0b: Interrupt masked, 1b: Interrupt unmasked
<1>	Vconn Overcurrent Fault Interrupt Status Mask	R/W	1b	0b: Interrupt masked, 1b: Interrupt unmasked
<0>	I^2C Interface Error Interrupt Status Mask	R/W	1b	0b: Interrupt masked, 1b: Interrupt unmasked

6.7.2.11 EXTENDED_STATUS_MASK (16h)

This is an event interrupt mask. It is masked and unmasked by the TCPM. The EXTENDED_STATUS_MASK register is cleared by the TCPM. This register is initialized at power on or Hard Reset.

The EXTENDED_STATUS_MASK is nested Alert. An EXTENDED_STATUS change has to be unmasked in both the EXTENDED_STATUS_MASK and the ALERT.ExtendedStatusInterruptMask to enable the ALERT_C pin.

The assertion of the ALERT_C pin is prevented when the corresponding bit is set to zero by the TCPM.

Table 28. EXTENDED_STATUS_MASK Register Definition

Bit(s)	Name	Type	Reset Value	Description
<7:1>	Reserved	R	0000000b	Sets to zero by sender and ignored by receiver
<0>	vSafe0V Status Mask	R/W	1b	0b: Interrupt masked, 1b: Interrupt unmasked

6.7.2.12 ALERT_EXTENDED_MASK (17h)

This is an event interrupt mask. It is masked and unmasked by the TCPM. The ALERT_EXTENDED_MASK register is cleared by the TCPM. This register is initialized on power on or Hard Reset.

The ALERT_EXTENDED_MASK is nested Alert. An ALERT_EXTENDED change has to be unmasked in both the ALERT_EXTENDED _MASK and the ALERT.AlertExtendedInterruptMask to enable the ALERT_C pin.

The assertion of the ALERT_C pin is prevented when the corresponding bit is set to zero by the TCPM.

Table 29. ALERT_EXTENDED_MASK Register Definition

Bit(s)	Name	Type	Reset Value	Description
<7:3>	Reserved	R	00000b	Sets to zero by sender and ignored by receiver
<2>	Timer Expired	R/W	1b	0b: Interrupt masked, 1b: Interrupt unmasked
<1>	Source Fast Role Swap Mask	R/W	1b	0b: Interrupt masked, 1b: Interrupt unmasked
<0>	Sink Fast Role Swap Mask	R/W	1b	0b: Interrupt masked, 1b: Interrupt unmasked

6.7.2.13 TCPC_CONTROL (19h)

This register is set and cleared only by the TCPM. The TCPM writes to the TCPC_ CONTROL register to set the Plug Orientation and enable/disable clock stretching.

The TCPC does not respond with NAK I^2C transfer regardless of the clock stretching setting chosen by the TCPM, unless the TCPM writes to a register/bit that is not implemented/reserved.

Table 30. TCPC_CONTROL Register Definition

Bit(s)	Name	Type	Reset Value	Description
<7>	Enable SMBus PEC	R/W	0b	0b: SMBus PEC is disabled (default) 1b: SMBus PEC is enabled Enables SMBus PEC according to Section 0.
<6>	Enable Looking4Connection Alert	R/W	0b	0b: Disable ALERT.CCStatus assertion when CC_STATUS.Looking4Connection changes (default) 1b: Enable ALERT.CCStatus assertion when CC_STATUS.Looking4Connection changes
<5>	Reserved	R	0b	Sets to zero by sender and ignored by receiver

Table 30. TCPC_CONTROL Register Definition (Cont.)

Bit(s)	Name	Type	Reset Value	Description
<4>	Debug Accessory Control	R/W	0b	0b: Controlled by TCPC (power on default) 1b: Controlled by TCPM. This bit has no effect to any function, it is always controlled by TCPC.
<3:2>	I^2C Clock Stretching Control	R/W	00b	Clock Stretching Control 00b: Disable clock stretching. TCPC does not perform any clock stretching during I^2C transfers. 01b: Reserved 10b: Enable clock stretching. TCPC is allowed limited clock stretching during each I^2C Transfer. 11b: Enable clock stretching only if the ALERT_C pin is not asserted. As soon as Alert is asserted, clock stretching is disabled by the TCPC. These bits don't effect to any function, TCPC never drives SCL.
<1>	BIST Test Mode	R/W	0b	Setting this bit to 1 is intended to be used only when a USB compliance tester is using USB BIST Test Data to test the PHY layer of the TCPC. The TCPM should clear this bit when a disconnect is detected. 0: Normal Operation. Incoming messages enabled by RECEIVE_DETECT passed to TCPM via Alert. 1: BIST Test Mode. Incoming messages enabled by RECEIVE_DETECT result in GoodCRC response but may not be passed to the TCPM via Alert. TCPC does not result in a Receive SOP* Message Status or a Rx Buffer Overflow alert.
<0>	Plug Orientation	R/W	0b	0b: When VCONN is enabled, apply it to the CC2 pin. Monitor the CC1 pin for BMC communications if PD messaging is enabled. 1b: When VCONN is enabled, apply it to the CC1 pin. Monitor the CC2 pin for BMC communications if PD messaging is enabled. TCPM should set Plug orientation to BMC side before it sets POWER_CONTROL.AutoDischargeDisconnect to 1

6.7.2.14 ROLE_CONTROL (1Ah)

This register is set and cleared only by the TCPM. The TCPM writes to this register to configure the CC pull-up (Rp) or pull-down (Rd) resistors.

The TCPM writes B6 (DRP) = 0b and Bits <3:0> (CC1/CC2) if it wishes to control the Rp/Rd directly instead of having the TCPC perform DRP toggling autonomously. When controlling Rp/Rd directly, the TCPM writes to Bits <3:0> (CC1/CC2) each time it wishes to change the CC1/CC2 values. This control is used for TCPM-TCPC implementing Source or Sink only as well as when a connection has been detected via DRP toggling but the TCPM wishes to attempt Try.Src or Try.Snk.

The TCPM can configure the TCPC to autonomously toggle the Rp/Rd when the TCPM-TCPC is implementing a DRP. When initiating autonomous DRP toggling, the TCPM writes B6 (DRP) = 1b and write the starting value of Rp/Rd to Bits <3:0> (CC1/CC2) to indicate DRP autonomous toggling mode to the TCPC. The TCPC does not start the DRP toggling until subsequently the TCPM writes to the COMMAND register to start the DRP toggling or there is a change in POWER_CONTROL.AutoDischargeDisconnect. Renesas recommends the TCPM write

ROLE_CONTROL.DRP = 0 before writing to POWER_CONTROL.AutoDischargeDisconnect and starting the DRP toggling using COMMAND.Look4Connection.

If DRP = 1b, the only allowed values for CC1/CC2 are Rp/Rp or Rd/Rd. COMMAND.Look4Connection does nothing if CC1/CC2 are not Rp/Rp or Rd/Rd.

Table 31. ROLE_CONTROL Register Definition

Bit(s)	Name	Type	Reset Value	Description
<7>	Reserved	R	0b	Sets to zero by sender and ignored by receiver
<6>	DRP	R/W	0b	0b: No DRP. Bits <3:0> determine Rp/Rd/Ra or open settings 1b: DRP. The TCPC does use the Rp value defined in <5:4> when a connection is resolved, such as on entry to Potential_Connect_as_Src in Figures 4-15 in the USB-Port Controller Specification Rev2.0 v1.0. The TCPC toggles CC1 and CC2 after receiving COMMAND.Look4Connection and until a connection is detected. On connection, the TCPC does resolve to either an Rp or Rd and report the CC1/CC2 State in the CC_STATUS register. The CC pins stay in Potential_Connect_as_Src or Potential_Connect_as_Sink until directed otherwise.
<5:4>	Rp Value	R/W	00b	00b: Rp default 01b: Rp 1.5A 10b: Rp 3.0A 11b: Reserved When TCPC connects to SNK with SRC, this fields can update RpValue for CC line.
<3:2>	CC2	R/W	10b	00b: Ra 01b: Rp (Use Rp definition in <5:4>) 10b: Rd 11b: Open (Disconnect or don't care) If TCPM sets this field to Ra, it does not affect the CC lines. TCPM should set this field according to TCPC specs for any control.
<1:0>	CC1	R/W	10b	00b: Ra 01b: Rp (Use Rp definition in <5:4>) 10b: Rd 11b: Open (Disconnect or don't care) See CC2.

6.7.2.15 FAULT_CONTROL (1Bh)

This register is set and cleared only by the TCPM. The TCPM writes to FAULT_CONTROL to enable/disable the FAULT circuitry.

Table 32. FAULT_CONTROL Register Definition

Bit(s)	Name	Type	Reset Value	Description
<7:4>	Reserved	R	0000b	Sets to zero by sender and ignored by receiver
<3>	VBUS Discharge Fault Detection Timer	R/W	0b	0b: VBUS Discharge Fault Detection Timer enabled 1b: VBUS Discharge Fault Detection Timer disabled This enables the timers for both FAULT_STATUTS.AutoDischargeFailed and FAULT_STATUS.ForceDischargeFailed
<2>	Internal OCP VBUS Overcurrent Protection Fault	R/W	0b	0b: Internal OCP circuit enabled 1b: Internal OCP circuit disabled If an OCP occurs with this bit set to 0, TCPC disables the Sourcing VBUS and ASGATE and discharge inside and outside VBUS to vSafe0V.
<1>	Internal OVP VBUS Overvoltage Protection Fault	R/W	0b	0b: Internal OVP circuit enabled 1b: Internal OVP circuit disabled If an OVP occurs with this bit set to 0, TCPC disables the Sinking VBUS and ASGATE and discharge inside VIN to vSafe0V. **Note:** cctop does not discharge VBUS outside ASGATE.
<0>	VCONN Overcurrent Fault	R/W	0b	0b: Fault detection circuit enabled 1b: Fault detection circuit disabled The detection circuit is always working, this field control an ALERT and FAULT_STATUS. If the Vconn OCP occurs with this bit set to 0, TCPC asserts the FUALT_STATUS. VCONN Overcurrent Fault and ALERT.FAULT_STATUS. In other case, TCPC not asserts both register. Regardless of the setting, if the TCPC detects Vconn OCP on providing Vconn, it turns off the Vconn for protect a TCPC.

6.7.2.16 POWER_CONTROL (1Ch)

This register is set and cleared by the TCPM.

The timing parameters for the TCPM in conjunction with the TCPC must meet the USB PD requirements.

The TCPM reads the CC_STATUS, POWER_STATUS, and optionally the VBUS_VOLTAGE registers to determine the connection state and the orientation of a USB Type-C port.

The TCPM takes the following steps to request sourcing VCONN over one of the CC pins:

1. The TCPM writes to TCPC_CONTROL.PlugOrientation to inform TCPC which CC pin (not connected through the cable) is repurposed as VCONN.
2. The TCPM sets POWER_CONTROL.EnableVCONN = 1b.

The TCPC source VCONN as TCPM requested irrespective of the status of VBUS and CC1, CC2 wires. The TCPC does not autonomously disable VCONN sourcing when VBUS is removed, or CC1, CC2 status has changed. The TCPM sets POWER_CONTROL.EnableVCONN = 0b to request disabling VCONN sourcing.

Table 33. POWER_CONTROL Register Definition

Bit(s)	Name	Type	Reset Value	Description
<7>	Fast Role Swap Enable	R/W	0b	0b: Disable Fast Role Swap function 1b: Enable Fast Role Swap function If system supports Fast Role Swap function, TCPM should set this bit to 1. In case of sink, TCPM should set POWER_CONTROL.AutoDischargeDisconnect to 0.
<6>	VBUS_VOLTAGE Monitor	R/W	1b	0b: VBUS_VOLTAGE Monitoring is enabled 1b: VBUS_VOLTAGE Monitoring is disabled Controls only VBUS_VOLTAGE Monitoring. VBUS_VOLTAGE reports all zeroes if disabled.
<5>	Disable Voltage Alarms	R/W	1b	0b: Voltage Alarms Power status reporting is enabled 1b: Voltage Alarms Power status reporting is disabled Controls VBUS_VOLTAGE_ALARM_HI_CFG and VBUS_VOLTAGE_ALARM_LO_CFG. The ALERT.VBUS_VOLTAGE_ALARM_HI/LOW_CFG stays asserted when VBUS voltage level meets assert conditions, so TCPM can avoid the ALERT assertion by using this register.
<4>	Auto Discharge Disconnect	R/W	0b	0b: The TCPC does not automatically discharge VBUS based on VBUS voltage 1b: The TCPC does automatically discharge Setting this bit in a Source TCPC triggers the following actions on a disconnect detection: 1. Disable sourcing power over VBUS and ASGATE turn off 2. VBUS discharge Sourcing power over VBUS is disabled before or at the same time as starting VBUS discharge. Setting this bit in a Sink TCPC triggers the following action on a disconnect detection: 1. Disable sinking power over VBUS and ASGATE turn off 2. VBUS discharge The TCPC does automatically disable discharge (without clearing this bit) once the voltage on VBUS is below vSafe0V (maximum). TCPC does not re-apply discharge circuit if VBUS rises above vSafe0V.
<3>	Reserved	R	0b	Sets to zero by sender and ignored by receiver
<2>	Force Discharge	R/W	0b	0b: Disable forced discharge (default) 1b: Enable forced discharge of VBUS. See Section 4.4.5.4.3 of the TCPC spec
<1>	VCONN Power Supported	R/W	0b	0b: Deliver at least 1W on VCONN 1b: Deliver at least the power indicated in DEVICE_CAPABILITIES.VCONNPowerSupported Refer to TCPC datasheet for actual power limit implemented
<0>	Enable VCONN	R/W	0b	0b: Disable VCONN Source (default) 1b: Enable VCONN Source to CC In the disconnect case, TCPC does not turn off the VCONN automatically, so TCPM should set PC.Enable VCONN to off. When TCPM is set to 0, the TCPC disables VCONN and discharges VCONN.

6.7.2.17 CC_STATUS (1Dh)

This register is set and cleared by the TCPC. The TCPC updates the CC_STATUS register within tSetReg of a change in ROLE_CONTROL.DRP or a change on the CC1 or CC2 wires, after debounce.

The TCPM starts the DRP toggling by writing to the COMMAND register.

The TCPM reads this register on detecting an ALERT_C and seeing the ALERT.CCStatus = 1. The TCPC indicates the Connection status, the Connection result, and the current CC state in this register.

The TCPC set CC_STATUS.Looking4Connection = 0b when it has detected a potential connection.

The TCPM reads the Looking4Connection to determine if the TCPC is toggling Rp/Rd when operating as a DRP. The TCPM reads the CC_STATUS.ConnectResult to determine if a DRP TCPC is presenting an Rp or Rd. The TCPM does read the CC1State and CC2State to determine the CC1 and CC2 states.

When reporting the state of the CC lines, the TCPC debounce for tTCPCfilter. The TCPC perform a minimal debounce and the TCPM must complete the debounce as defined in USB Type-C.

The TCPM as a Source detects a Sink attachment and detachment by reading CC1State and CC2State bits.

Table 34. CC_STATUS Register Definition

Bit(s)	Name	Type	Reset Value	Description
<7:6>	Reserved	R	00b	Sets to zero by sender and ignored by receiver
<5>	Looking4Connection	R	0b	0b: TCPC is not actively looking for a connection. A transition from ‘1’ to ‘0’ indicates a potential connection has been found. The transition condition to potential states are of TCPC specs. 1b: TCPC is looking for a connection (toggling as a DRP or looking for a connection as Sink/Source only condition)
<4>	ConnectResult	R	0b	0b: the TCPC is presenting Rp 1b: the TCPC is presenting Rd TCPC updates this bit when Looking4Connection changes to 0 from 1. This bit will also be updated to a new role if TCPM had instructed a PowerRoleSwap.

Table 34. CC_STATUS Register Definition (Cont.)

Bit(s)	Name	Type	Reset Value	Description

<3:2>	CC2 State	R	00b	If (ROLE_CONTROL.CC2 = Rp) or (ConnectResult = 0)
				00b: SRC.Open (Open, Rp)
				01b: SRC.Ra (below maximum vRa)
				10b: SRC.Rd (within the vRd range)
				11b: reserved
				If (ROLE_CONTROL.CC2 = Rd) or (ConnectResult = 1)
				00b: SNK.Open (Below maximum vRa)
				01b: SNK.Default (Above minimum vRd-Connect)
				10b: SNK.Power1.5 (Above minimum vRd-Connect) Detects Rp 1.5A
				11b: SNK.Power3.0 (Above minimum vRd-Connect) Detects Rp 3.0A
				If ROLE_CONTROL.CC2 = Ra, this field is set to 00b
				If ROLE_CONTROL.CC2 = Open, this field is set to 00b
				This field always returns 00b if (Looking4Connection = 1) or (POWER_CONTROL.EnableVconn = 1 and TCPC_CONTROL.PlugOrientation = 0).
				Otherwise, the returned value depends on ROLE_CONTROL.CC2.

<1:0>	CC1 State	R	00b	If (ROLE_CONTROL.CC1 = Rp) or (ConnectResult = 0)
				00b: SRC.Open (Open, Rp)
				01b: SRC.Ra (below maximum vRa)
				10b: SRC.Rd (within the vRd range)
				11b: Reserved
				If (ROLE_CONTROL.CC1 = Rd) or ConnectResult = 1)
				00b: SNK.Open (Below maximum vRa)
				01b: SNK.Default (Above minimum vRd-Connect)
				10b: SNK.Power1.5 (Above minimum vRd-Connect) Detects Rp-1.5A
				11b: SNK.Power3.0 (Above minimum vRd-Connect) Detects Rp-3.0A
				If ROLE_CONTROL.CC1 = Ra, this field is set to 00b
				If ROLE_CONTROL.CC1 = Open, this field is set to 00b
				This field always returns 00b if (Looking4Connection = 1) or (POWER_CONTROL.EnableVconn = 1 and TCPC_CONTROL.PlugOrientation = 1). Otherwise, the returned value depends on ROLE_CONTROL.CC1.

6.7.2.18 POWER_STATUS (1Eh)

This register is set and cleared by the TCPC. The TCPM reads this register on detecting an ALERT_C and reading the ALERT.PowerStatus bit set to 1. The TCPC indicates the current Power Status in this register.

The TCPM operating as a Sink at vSafe5V (with or without a USB PD Contract) detects VBUS presence and removal by reading the VBUSPresent bit.

The TCPM checks the state of the TCPC Initialization Status bit when it starts or resets. The TCPM does not start normal operation until the TCPC Initialization Status bit is cleared. The TCPC sets the TCPC Initialization Status bit to zero when initialization or reset is complete and all registers are valid.

Table 35. POWER_STATUS Register Definition

Bit(s)	Name	Type	Reset Value	Description
<7>	Debug Accessory Connected	R	0b	0b: No Debug Accessory connected 1b: Debug Accessory connected TCPC asserts this bit when it transitions to Debug Accessory state. If TCPC detects a disconnection, it deasserts this bit. TCPC detects Rd and Rd or Rp and Rp on Apply State, if the TCPC detects DebugAccessory device with tCCDebounce, it will transition to DebugAccessory.SRC or SNK.
<6>	TCPC Initialization Status	R	1b	0b: The TCPC has completed initialization and all registers are valid 1b: The TCPC is still performing internal initialization and the only registers that are guaranteed to return the correct values are 00h...0Fh. TCPC clears this field and asserts ALERT.POWER_STATUS after TCPC completes initialization of VBUS detection and the first VBUS detection.
<5>	Sourcing Nondefault Voltage	R	0b	0b: vSafe5V 1b: Nondefault VBUS voltage This bit does not control the power path, it just provides a monitor of the status. This bit is asserted as long as the TCPC is sourcing nondefault voltage over VBUS (such as not vSafe5V) as a response to TCPM writing to COMMAND.SourceNondefaultVbusVolage.
<4>	Sourcing VBUS	R	0b	0b: Sourcing VBUS is disabled 1b: Sourcing VBUS is enabled This bit does not control the path, just provides a monitor of the status. The TCPC controls this bit according to the command and each event (disconnect frs), indicates that Sourcing VBUS is in progress.
<3>	VBUS Detection Enabled	R	0b	0b: VBUS Detection Disabled 1b: VBUS Detection Enabled Indicates whether the TCPC is monitoring for VBUS Present and vSafe0V level. VBUS detection will be enabled automatically after TCPC_SETTING_1<4> is set to 1 and the TCPC initialization is complete.
<2>	VBUS Present	R	0b	0b: VBUS Disconnected 1b: VBUS Connected TCPC asserts VBUS_present when TCPC detects that VBUS rises above VBUS_PRESENT_THRESHOLD. Voltage trip point. TCPC de-asserts VBUS_present when TCPC detects that VBUS falls below VBUS_PRESENT_THRESHOLD. Voltage trip point - 100mV. TCPC checks a VBUS voltage from ADC every 853µs. This bit may toggle every 853µs. This bit is not valid when POWER_STATUS.VbusDetectionEnabled = 0b. If it is critical for TCPM, consider using a TCPC_SETTING.ADC_monitor_mode.

Table 35. POWER_STATUS Register Definition (Cont.)

Bit(s)	Name	Type	Reset Value	Description
<1>	VCONN Present	R	0b	0b: VCONN is not present 1b: This bit is asserted when VCONN presents CC1 or CC2. Threshold is fixed at 2.4V. TCPC deasserts this bit when TCPC detects VBUS falling below 2.4V. If POWER_CONTROL.EnableVCONN is disabled, this bit indicates a 0b.
<0>	Sinking VBUS	R	0b	0b: Sink is Disconnected 1b: TCPC is sinking VBUS to the system load The TCPC controls this bit according to the command and each event (disconnect frs), indicates that Sinking VBUS is in progress.

6.7.2.19 FAULT_STATUS (1Fh)

This register is set by TCPC and cleared by TCPM. The TCPM reads this register when detecting an ALERT_C and reading the ALERT.Fault bit set to 1. The TCPC indicates the current fault status in this register.

The TCPC indicates a Fault status change has occurred by presenting a logical 1 in the corresponding bit position in this register, presenting a logical 1 to the ALERT.Fault bit, and asserting the ALERT_C pin if the corresponding fault bit in FAULT_STATUS_MASK is 1 and ALERT_MASK.Fault is 1. The TCPM clears the FAULT bit by writing a logical 1 to the respective FAULT bit position and then writing a logical 1 to the ALERT.Fault bit after all bits in FAULT_STATUS have been cleared. The TCPM can clear any number of FAULT bits in a single write by setting multiple bits to logical 1 and the rest of the bits in the register to logical 0. The TCPM writing a logical 0 to any FAULT bit has no effect and therefore does not cause those FAULT bits to be set or cleared.

Table 36. FAULT_STATUS Register Definition

Bit(s)	Name	Type	Reset Value	Description
<7>	AllRegistersResetTo Default	R/W1C	1b	This bit is asserted when the TCPC resets all registers to their default value. This happens at initial power up or if an unexpected power reset occurs.
<6>	Reserved	R	0b	Sets to zero by sender and ignored by receiver
<5>	Auto Discharge Failed	R/W1C	0b	0b: No discharge failure 1b: Discharge commanded by the TCPM failed If POWER_CONTROL.AutoDischargeDisconnect is set, the TCPC reports discharge fails if VBUS is not below vSafe0V within tSafe0V.
<4>	Force Discharge Failed	R/W1C	0b	0b: No discharge failure 1b: Discharge commanded by the TCPM failed If POWER_CONTROL.ForceDischarge is set, the TCPC will report a discharge fails if VBUS is not below vSafe0V within tSafe0V.
<3>	Internal OCP VBUS Overcurrent Protection Fault	R/W1C	0b	0b: Not in an overcurrent protection state 1b: Overcurrent fault latched If VBUS falls below voltage of VBUS_CURRENT_UV_THRESHLD, TCPC will asserts this bit. The cctop disables a soursing VBUS and ASGATE and discharge inside and outside VBUS to vSafe0V.

Table 36. FAULT_STATUS Register Definition (Cont.)

Bit(s)	Name	Type	Reset Value	Description
<2>	Internal OVP VBUS Overvoltage Protection Fault	R/W1C	0b	0b: Not in an overvoltage protection state 1b: Overvoltage fault latched. TCPC will asserts this bit when charger notifies overvoltage. The cctop disables a sinking VBUS and ASGATE and discharge VBUS inside ASGATE to vSafe0V. **Note:** cctop does not discharge VBUS outside ASGATE.
<1>	VCONN Overcurrent Fault	R/W1C	0b	0b: No Fault detected 1b: Overcurrent VCONN fault latched TCPC will asserts this bit when charger notifies overcurrent with Vconn. Then TCPC turn off the Vconn but TCPM needs write POWER_CONTROL.EnableVconn to 0.
<0>	I2C Interface Error	R/W1C	0b	0b: No Error 1b: I2C error has occurred. Some of the conditions for asserting this bit: · TCPM writes to the TRANSMIT register when the TRANSMIT_BUFFER is empty · TCPM writes an invalid COMMAND· TCPM writes to the TRANSMIT_BUFFER when TCPC is transmitting the Fast Role Swap signal The other case is explained in the following.

FAULT_STATUS.I2C Interface Error assert under the following conditions:

- TCPM writes to the TRANSMIT register when the TRANSMIT_BUFFER is empty. (See 4.4.6.3 of TCPC specs.)
- TCPM writes to the TRANSMIT_BUFFER when TCPC is transmitting the Fast Role Swap signal. (Refer to 4.4.6.3 of TCPC specs.)
- TCPM writes an invalid COMMAND (Refer to 4.4.8 of specs.)
  - TCPM writes DisableVbusDetect when TCPC has sourcing or sinking power over VBUS enabled.
  - TCPM writes SinkVbus when TCPC has sourcing power over VBUS enabled.
  - TCPM writes SourceVbusDefaultVoltage when TCPC has sinking power over VBUS enabled.
  - TCPM writes SourceVbusNondefaultVoltage when TCPC is sinking from VBUS, or the TCPC does not have the ability to source voltages higher than vSafe5V.
  - TCPM writes SourceVbusNondefaultVoltage when TCPC is not already sourcing power over VBUS.
  - TCPM writes SendFRSwapSignal when POWER_CONTROL.FastRoleSwapEnable = 0b.
- If the TCPM writes to TRANSMIT requesting a transmission that is not Hard Reset, Cable Reset or BIST Carrier Mode 2 (for example, TRANSMIT.SOP*Message > 100b) and there are less than 2 bytes in the TX_BUF_BYTE_x register (for example, the transmit buffer pointer is less than offset 3), the TCPC generates a FAULT_STATUS.I2CinterfaceError (see section 4.4.15 of TCPC specs)
- If the I2C_WRITE_BYTE_COUNT is different than the number of bytes written in the buffer, the TCPC does assert ALERT.InterfaceError and ignore the write (see section 4.4.16 of TCPC specs)
- The TCPM writes 17 total bytes: I2C_WRITE_BYTE_COUNT (30) + TX_BUF_BYTE_0…TX_BUF_BYTE_15 (2 header bytes + 14 data bytes). The TCPM issues a Stop bit to abort the write transaction. The I^2C write is ignored and the pointer of TRANSMIT_BUFFER remains at offset 1. The TCPC does assert ALERT.InterfaceError (see section 4.7.2 Example #2 of TCPC specs)
- TCPC transition to Connected Invalid (see the figure *TCPC State Diagram after a Connection* in the TCPC specification)

6.7.2.20 EXTENDED_STATUS (20h)

This register is set and cleared by the TCPC. The TCPM reads this register when detecting an ALERT_C and reading the ALERT.ExtendedStatus bit set to 1.

Table 37. EXTENDED_STATUS Register Definition

Bit(s)	Name	Type	Reset Value	Description
<7:1>	Reserved	R	0000000b	Sets to zero by sender and ignored by receiver
<0>	vSafe0V	R	1b	0b: VBUS is not at vSafe0V 1b: VBUS is at vSafe0V The TCPC reports that VBUS is at vSafe0V when TCPC detects VBUS is below 0.8V. This bit is not valid when POWER_STATUS.VbusDetectionEnabled = 0b.

6.7.2.21 ALERT_EXTENDED (21h)

This register is set by TCPC and cleared by TCPM. The TCPM reads this register when detecting an ALERT_C and reading the ALERT.AlertExtended bit set to 1.

The TCPM clears an ALERT_EXTENDED bit by writing a logical 1 to the respective bit position and then writing a logical 1 to the ALERT.AlertExtended bit after all bits in ALERT_EXTENDED have been cleared. The TCPM can clear any number of ALERT_EXTENDED bits in a single write by setting multiple bits to logical 1 and the rest of the bits in the register to logical 0. The TCPM writing a logical 0 to any ALERT_EXTENDED bit has no effect and therefore does not cause those ALERT_EXTENDED bits to be set or cleared.

Table 38. ALERT_EXTENDED Register Definition

Bit(s)	Name	Type	Reset Value	Description
<7:3>	Reserved	R	000000b	Sets to zero by sender and ignored by receiver
<2>	Timer Expired	R/W1C	0b	0b: Generic timer is not expired 1b: Generic timer has expired TCPC starts counting the generic_timer when TCPM writes a new value to the GENERIC_TIMER.
<1>	Source Fast Role Swap	R/W1C	0b	0b: No Fast Role Swap signal sent 1b: Fast Role Swap signal sent due to detection of source voltage drop
<0>	Sink Fast Role Swap	R/W1C	0b	0b: No Fast Role Swap signal received 1b: Fast Role Swap signal received

6.7.2.22 COMMAND (23h)

The COMMAND register is issued and written by the TCPM. The COMMAND register is cleared by the TCPC after being acted on.

The TCPM issues COMMAND.Look4Connection to enable the TCPC to autonomously toggle the Rp/Rd. The initial Rp or Rd for toggling is determined by ROLE_CONTROL.CC1 and ROLE_CONTROL.CC2. If ROLE_CONTROL.CC1 and ROLE_CONTROL.CC2 are not the same value, the COMMAND.Look4Connection does have no effect.

The TCPM issues COMMAND.Look4Connection to enable the TCPC to restart Connection Detection in cases where the role is fixed as Source or Sink, ROLE_CONTROL.DRP = 0b. An example of this is when a potential connection as a Source occurred but was further debounced by the TCPM to find the Sink disconnected. In this case a Source Only or DRP should go back to its Unattached.Src state. This would result in ROLE_CONTROL staying the same.

COMMAND.I2Cidle is used to put the I2C interface into the idle state.

The TCPM send the COMMAND.WakeI2C as a throw away command to wake the I2C interface.

COMMAND.I2Cidle is decoupled from other Alert status detection mechanisms (such as CC_STATUS, POWER_STATUS, RECEIVE_DETECT, etc). For example, writing COMMAND. I2Cidle has no effect on ALERT.CCStatus, or the CC_STATUS register behavior. CC_STATUS detection may be disabled by writing to the ROLE_CONTROL register, but its behavior is not affected by the COMMAND.I2Cidle.

While there is a valid Source-to-Sink connection, the TCPM acting as a Sink writes COMMAND.DisableSinkVbus (if DEVICE_CAPABILITIES_1.SinkVbus = 1b) to remove the Sink connection on reception of or prior to transmitting a Power Role Swap or Hard Reset.

Table 39. COMMAND Register Definition[1]

Bit(s)	Name	Type	Reset Value	Register Setting	Description
<7:0>	Command	W	00h	0001 0001b	**WakeI2C** (no action is taken other than to wake the I2C interface).
<7:0>	Command	W	00h	0010 0010b	**DisableVbusDetect.** Disable VBUS present and vSafe0V detection. The TCPC ignores this command and assert the FAULT_STATUS.I2CInterfaceError if it has sourcing or sinking power over VBUS enabled. If the TCPC received this command validly, TCPC clear the POWER_STATUS.VBUS Detection Enable.
<7:0>	Command	W	00h	0011 0011b	EnableVbusDetect. Enable VBUS present and vSafe0V detection. If TCPC receives this command, TCPC sets POWER_STATUS.VBUS Detection Enable after update VBUS present and vSafe0V to latest status and it can notify the ALERT for POWER_STATUS.VBUS_present and EXTENDED_STATUS.vSafe0V.
<7:0>	Command	W	00h	0100 0100b	**DisableSinkVbus.** Disable sinking power over VBUS. This COMMAND does not disable POWER_STATUS.VBUSPresent detection. The TCPC clears FAULT_STATUS.InternalOCP and FAULT_STATUS.InternalOVP. The TCPC turn off VBus ASGATE. The TCPC does not discharge VBUS voltage.
<7:0>	Command	W	00h	0101 0101b	SinkVbus. Enable sinking power over VBUS and enable VBUS present detection. The TCPC ignores this command and assert the FAULT_STATUS.I2CInterfaceError if it has sourcing power over VBUS enabled. The TCPC turn on VBus ASGATE and stop VBUS discharge. If TCPC receives this command, TCPC completes setting charging and loading of VBUS. When TCPC detects VBUS removal, TCPC controls a discharge circuit if TCPM has set POWER_CONTROL.Auto Discharge Disconnect to 1. So TCPM does not need to write a COMMAND.DisableSinkVbus when TCPC has detect remover the VBUS.

Table 39. COMMAND Register Definition[1] (Cont.)

Bit(s)	Name	Type	Reset Value	Register Setting	Description
<7:0>	Command	W	00h	0110 0110b	**DisableSourceVbus.** Disable sourcing power over VBUS. The TCPC stops reporting FAULT_STATUS. Internal OCP or OVP Faults. This COMMAND does not disable POWER_STATUS.VBUSPresent detection. The TCPC turn off VBus ASGATE and discharge VBUS voltage to vSafe0V.
<7:0>	Command	W	00h	0111 0111b	**SourceVbusDefaultVoltage.** Enable sourcing vSafe5V over VBUS and enable VBUS present detection. Source transitions to vSafe5V if at a high voltage. The TCPC ignores this command and assert the FAULT_STATUS.I2CInterfaceError if it has sinking power over VBUS enabled. The TCPC turn on VBus ASGATE and stop VBUS discharge.
<7:0>	Command	W	00h	1000 1000b	SourceVbusNondefaultVoltage. Execute transitioning VBUS to a nondefault voltage level. This is an invalid COMMAND if the TCPC is currently sinking voltage from VBUS. This is also an invalid COMMAND if the TCPC is not already sourcing power over VBUS. The target VBUS voltage to be sourced may be set in a vendor defined manner. The TCPM may need to write to vendor defined register before sending this COMMAND.
<7:0>	Command	W	00h	1001 1001b	Look4Connection. Start DRP Toggling if ROLE_CONTROL.DRP = 1b. If ROLE_CONTROL.CC1/CC2 = 01b start with Rp, if ROLE_CONTROL.CC1/CC2 = 10b start with Rd. If ROLE_CONTROL.CC1/CC2 are not both 01b or 10b, then do not start toggling. The TCPM issues COMMAND.Look4Connection to enable the TCPC to restart Connection Detection in cases where the ROLE_CONTROL contents will not change. An example of this is when a potential connection as a Source occurred but was further debounced by the TCPM to find the Sink disconnected. In this case a Source Only or DRP should go back to its Unattached.Src state. This would result in ROLE_CONTROL staying the same.
<7:0>	Command	W	00h	1010 1010b	**RxOneMore.** Configure the receiver to automatically clear the RECEIVE_DETECT register after sending the next GoodCRC. This shutdowns reception of packets at a known point regardless of packet separation or the depth of the receive FIFO in the TCPC.
<7:0>	Command	W	00h	1100 1100b	**SendFRSwapSignal.** Source TCPC sends Fast Role Swap signal within tTCPCSendFRSwap after receiving this command if POWER_CONTROL.FastRoleSwapEnable = 1b. TCPC ignores this command and assert the FAULT_STATUS.I2CInterfaceError if POWER_CONTROL.FastRoleSwapEnable = 0b.

Table 39. COMMAND Register Definition[1] (Cont.)

Bit(s)	Name	Type	Reset Value	Register Setting	Description
<7:0>	Command	W	00h	1101 1101b	**ResetTransmitBuffer.** The TCPC resets the pointer of the TRANSMIT_BUFFER register to offset 1 and the contents of TRANSMIT_BUFFER becomes invalid when this command is issued by the TCPM. This command is supported by TCPC compliant with USB Port Controller Specification Revision 2.0.
<7:0>	Command	W	00h	1110 1110b	**ResetReceiveBuffer.** The TCPC resets the pointer of RX_BUFFER when this command is issued by the TCPM. TCPC does not clear the content of the buffer when receiving this command. The TCPM issues this command in order to re-read the RECEIVE_BUFFER.RX_BUF_BYTE_x. This command is supported by TCPC compliant with USB Port Controller Specification Revision 2.0,
<7:0>	Command	W	00h	1111 1111b	I^2C Idle

1. All other values are reserved; is ignored by the receiver.

6.7.2.23 DEVICE_CAPABILITIES_1 (24h)

This register describes features supported by the TCPC.

Table 40. DEVICE_CAPABILITIES_1 Register Definition

Bit(s)	Name	Type	Reset Value	Description
<15>	VBUS Nondefault Target	R	1b	0b: VBUS_NONDEFAULT_TARGET register not implemented 1b: VBUS_NONDEFAULT_TARGET register implemented
<14>	VBUS OCP Reporting	R	1b	0b: VBUS OCP is not reported by the TCPC 1b: VBUS OCP is reported by the TCPC
<13>	VBUS OVP Reporting	R	1b	0b: VBUS OVP is not reported by the TCPC 1b: VBUS OVP is reported by the TCPC
<12>	Bleed Discharge	R	0b	0b: No Bleed Discharge implemented in TCPC 1b: Bleed Discharge is implemented in the TCPC
<11>	Force Discharge	R	1b	0b: No Force Discharge implemented in TCPC 1b: Force Discharge is implemented in the TCPC
<10>	VBUS Measurement and Alarm Capable	R	1b	0b: No VBUS voltage measurement nor VBUS Alarms 1b; VBUS voltage measurement and VBUS Alarms
<9:8>	Source Resistor Supported	R	10b	00b: Rp default only 01b: Rp 1.5A and default 10b: Rp 3.0A, 1.5A, and default 11b: Reserved Rp values which may be configured by the TCPM via the ROLE_CONTROL register

Table 40. DEVICE_CAPABILITIES_1 Register Definition (Cont.)

Bit(s)	Name	Type	Reset Value	Description
<7:5>	Power Roles Supported	R	101b	000b: USB Type-C Port Manager can configure the Port as Source only or Sink only (not DRP) 001b: Source only 010b: Sink only 011b: Sink with accessory support 100b: DRP only 101b: Source, Sink, DRP, Adapter/Cable all supported 110b: Source, Sink, DRP 111b: Not valid
<4>	SOP'_DBG/SOP"_DBG Support	R	1b	0b: All SOP* except SOP'_DBG/SOP"_DBG 1b: All SOP* messages are supported Configured in RECEIVE_DETECT and TRANSMIT
<3>	Source VCONN	R	1b	0b: TCPC is not capable of switching the VCONN Source 1b: TCPC is capable of switching the VCONN Source
<2>	Sink VBUS	R	1b	0b: TCPC is not capable controlling the sink path to the system load 1b: TCPC is capable of controlling the sink path to the system load
<1>	Source Nondefault VBUS	R	1b	0b: TCPC is not capable of sourcing nondefault voltages over VBUS 1b: TCPC is capable of sourcing nondefault voltages over VBUS
<0>	Source VBUS	R	1b	0b: TCPC is not capable of controlling the source path to VBUS 1b: TCPC is capable of controlling the source path to VBUS

The Power Roles Supported field provides information of the device capabilities, The actual role should be set in ROLE_CONTROL register.

6.7.2.24 DEVICE_CAPABILITIES_2 (26h)

This register describes features supported by the TCPC.

Table 41. DEVICE_CAPABILITIES_2 Register Definition

Bit(s)	Name	Type	Reset Value	Description
<15>	Reserved	R	0b	Sets to zero by sender and ignored by receiver
<14>	Message Disable Disconnect	R	0b	0b: Sink TCPC disables PD message delivery when ALERT.VbusinkDisconnectDetected has been asserted 1b: Sink TCPC disables PD message delivery using the condition as defined in RECEIVE_DETECT.MessageDisableDisconnect
<13>	Generic Timer	R	1b	0b: GENERIC_TIMER register is not supported 1b: GENERIC_TIMER register is supported
<12>	Long Message	R	0b	0b: TCPC only supports 30 bytes content of the SOP* message. ▪ The value in READABLE_BYTE_COUNT is less than or equal to 31. ▪ The value in I2C_WRITE_BYTE_COUNT is less than or equal to 30. 1b: TCPC is capable of supporting 264 bytes content of the SOP* message.

Table 41. DEVICE_CAPABILITIES_2 Register Definition (Cont.)

Bit(s)	Name	Type	Reset Value	Description
<11>	SMBus PEC	R	1b	0b: TCPC_CONTROL.EnableSMBusPEC not implemented 1b: TCPC_CONTROL.EnableSMBusPEC implemented
<10>	Source FR Swap	R	0b	0b: Not capable of sending Fast Role Swap signal as Source when receiving COMMAND.SendFRSwapSignal. 1b: Capable of sending Fast Role Swap signal as Source TCPC when receiving COMMAND.SendFRSwapSignal.
<9>	Sink FR Swap	R	1b	0b: POWER_CONTROL.FastRoleSwapEnable not supported as Sink 1b: POWER_CONTROL.FastRoleSwapEnable supported as Sink
<8>	Watchdog Timer	R	0b	0b: TCPC_CONTROL.EnableWatchdogTimer not implemented 1b: TCPC_CONTROL.EnableWatchdogTimer implemented
<7>	Sink Disconnect Detection	R	1b	0b: VBUS_SINK_DISCONNECT_THRESHOLD not implemented, use POWER_STATUS.VbusPresent=0b to indicate a Sink disconnect. 1b: VBUS_SINK_DISCONNECT_THRESHOLD implemented
<6>	Stop Discharge Threshold	R	1b	0b: VBUS_STOP_DISCHARGE_THRESHOLD not implemented 1b: VBUS_STOP_DISCHARGE_THRESHOLD implemented
<5:4>	VBUS Voltage Alarm LSB	R	10b	00: TCPC has 25mV LSB for its voltage alarm and uses all 10 bits in ▪ VBUS_VOLTAGE_ALARM_HI_CFG and ▪ VBUS_VOLTAGE_ALARM_LO_CFG. 01: TCPC has 50mV LSB for its voltage alarm and uses only 9 bits. ▪ VBUS_VOLTAGE_ALARM_HI_CFG[0] and ▪ VBUS_VOLTAGE_ALARM_LO_CFG[0] are ignored by TCPC. 10: TCPC has 100mV LSB for its voltage alarm and uses only 8 bits. ▪ VBUS_VOLTAGE_ALARM_HI_CFG[1:0] and ▪ VBUS_VOLTAGE_ALARM_LO_CFG[1:0] are ignored by TCPC. 11: Reserved
<3:1>	VCONN Power Supported	R	001b	000b: 1.0W 001b: 1.5W 010b: 2.0W 011b: 3W 100b: 4W 101b: 5W 110b: 6W 111b: External
<0>	VCONN Overcurrent Fault Capable	R	1b	0b: TCPC is not capable of detecting a VCONN overcurrent fault 1b: TCPC is capable of detecting a VCONN overcurrent fault

6.7.2.25 STANDARD_INPUT_CAPABILITIES (28h)

This register describes the optional normative Standard Inputs and their capability.

The TCPC does not support the function of this register.

Table 42. STANDARD_INPUT_CAPABILITIES Register Definition

Bit(s)	Name	Type	Reset Value	Description
<7:5>	Reserved	R	000b	Sets to zero by sender and ignored by receiver
<4:3>	Source Fast Role Swap	R	00b	00b: Not present in TCPC 01b: Present in TCPC as an input only pin 10b: Present in TCPC as a bidirectional pin, sharing with the STANDARD OUTPUT SIGNAL VBUS Sink Disconnect Detect Indicator. 11b: Reserved
<2>	VBUS External Overvoltage Fault	R	0b	0b: Not present in TCPC 1b: Present in TCPC
<1>	VBUS External Overcurrent Fault	R	0b	0b: Not present in TCPC 1b: Present in TCPC
<0>	Force Off VBUS (Source or Sink)	R	0b	0b: Not present in TCPC 1b: Present in TCPC

6.7.2.26 STANDARD_OUTPUT_CAPABILITIES (29h)

This register describes the optional normative Standard Outputs and their capability.

The TCPC does not support the function of this register.

Table 43. STANDARD_OUTPUT_CAPABILITIES Register Definition

Bit(s)	Name	Type	Reset Value	Description
<7>	VBUS Sink Disconnect Detect Indicator	R	0b	0b: Not present in TCPC 1b: Present in TCPC
<6>	Debug Accessory Indicator	R	0b	0b: Not present in TCPC 1b: Present in TCPC
<5>	VBUS Present Monitor	R	0b	0b: Not present in TCPC 1b: Present in TCPC
<4>	Audio Adapter Accessory Indicator	R	0b	0b: Not present in TCPC 1b: Present in TCPC
<3>	Active Cable Indicator	R	0b	0b: Not present in TCPC 1b: Present in TCPC
<2>	MUX Configuration Control	R	0b	0b: Not present in TCPC 1b: Present in TCPC
<1>	Connection Present	R	0b	0b: No Connection 1b: Connection Controlled by the TCPM.
<0>	Connector Orientation	R	0b	0b: Not present in TCPC 1b: Present in TCPC

6.7.2.27 GENERIC_TIMER (2Ch)

The TCPM writes a non-zero value to this register to start the general purpose timer. If the TCPM writes a non-zero value to this register before the timer has expired, the timer is restarted with the last written non-zero value.

After the timer has expired, the timer does not restart until TCPM writes a non-zero value to this register. The timer stop when a zero value is written to this register.

ALERT_EXTENDED.TimerExpired is asserted when the last written non-zero timer value has expired. Clearing the ALERT_EXTENDED.TimerExpired has no effect to this register. To avoid a race condition, the TCPM may write a zero value to this register before writing a non-zero value to start the timer.

Table 44. GENERIC_TIMER Register Definition

Bit(s)	Name	Type	Reset Value	Description
<15:0>	GENERIC_TIMER	W	0000h	16-bit timer value with 0.1ms LSB. A non-zero value starts the timer. A value of zero stops the timer. The timer does not restart after it has expired. This timer stops on I2CIdle.

6.7.2.28 MESSAGE_HEADER_INFO (2Eh)

The TCPM may overwrite this register after TCPC initialization is complete.

On attach and after implementing the tCCDebounce, the TCPM updates the MESSAGE_HEADER_INFO Register first before writing to the RECEIVE_DETECT register.

Table 45. MESSAGE_HEADER_INFO Register Definition

Bit(s)	Name	Type	Reset Value	Description
<7:5>	Reserved	R	000b	Sets to zero by sender and ignored by receiver
<4>	Cable Plug	R/W	0b	0b: Message originated from Source, Sink, or DRP 1b: Message originated from a Cable Plug
<3>	Data Role	R/W	0b	0b: UFP 1b: DFP
<2:1>	USB PD Specification Revision	R/W	01b	00b: Revision 1.0 01b: Revision 2.0 10b: Revision 3.0 11b: Reserved
<0>	Power Role	R/W	0b	0b: Sink 1b: Source

6.7.2.29 RECEIVE_DETECT (2Fh)

This register set by the TCPM, cleared by the TCPM, or the TCPC in some instances.

The TCPM notifies the TCPC of the message type and/or signaling types to be detected. The TCPM should not set any bits in this register until it is able to respond. The TCPC responds to the enabled message type with a GoodCRC if it is a SOP* message, except in the case of a GoodCRC message.

The initial value of RECEIVE_DETECT is all zeroes. The bits must be written to be enabled. When the TCPM sets all bits in RECEIVE_DETECT to zero, the TCPC disables automatic transmission of GoodCRC message and discard COMMAND.RxOneMore if it has not been acted on.

The TCPC disable PD message delivery under the following conditions:

- When RECEIVE_DETECT.HardReset is set and a Hard Reset is received
- When the TCPM writes to TRANSMIT to request a Hard Reset transmission
- When RECEIVE_DETECT.CableReset is set and a Cable Reset is received
- On detection of a disconnect (Sink TCPC to use condition as defined in RECEIVE_DETECT.MessageDisableDisconnect)

The following happens when the TCPC disables PD message delivery:

- The TCPC disables automatic transmission of GoodCRC message.
- The TCPC discards COMMAND.RxOneMore if it has not been acted on.
- The TCPC sets all bits in RECEIVE_DETECT to zero
- The TCPC sets all bits in READABLE_BYTE_COUNT to zero

Transmitting CableReset by the TCPC has no effect on RECEIVE_DETECT register.

Table 46. RECEIVE_DETECT Register Definition

Bit(s)	Name	Type	Reset Value	Description
<7>	Message Disable Disconnect	R	0b	Sets to zero by sender and ignored by receiver This bit is not implemented by TCPC because it does not support CTVPD. It is fixed to zero.
<6>	Enable Cable Reset	R/W	0b	0b: TCPC does not detect Cable Reset signaling (default) 1b: TCPC detects Cable Reset signaling
<5>	Enable Hard Reset	R/W	0b	0b: TCPC does not detect Hard Reset signaling (default) 1b: TCPC detects Hard Reset signaling
<4>	Enable SOP_DBG'' message	R/W	0b	0b: TCPC does not detect SOP_DBG'' message (default) 1b: TCPC detects SOP_DBG'' message
<3>	Enable SOP_DBG' message	R/W	0b	0b: TCPC does not detect SOP_DBG' message (default) 1b: TCPC detects SOP_DBG' message
<2>	Enable SOP'' message	R/W	0b	0b: TCPC does not detect SOP'' message (default) 1b: TCPC detects SOP'' message
<1>	Enable SOP' message	R/W	0b	0b: TCPC does not detect SOP' message (default) 1b: TCPC detects SOP' message
<0>	Enable SOP message	R/W	0b	0b: TCPC does not detect SOP message (default) 1b: TCPC detects SOP message

6.7.2.30 RECEIVE_BUFFER for TCPCi 2.0

If TCPM wants to use a RECEIVE_BUFFER with TCPCi 2.0, it is not necessary to change register setting. As a result, the following registers work.

The RECEIVE_BUFFER comprises of three sets of registers: READABLE_BYTE_COUNT, RX_BUF_FRAME_TYPE and RX_BUF_BYTE_x. These registers can only be accessed by reading at a common register address 30h. These registers indicate the status of the received SOP* message buffer. These registers is read by the TCPM when the TCPC indicates a SOP* message was received in the Alert Status registers.

RECEIVE_BUFFER is read only.

READABLE_BYTE_COUNT (30h)

The TCPM reads the READABLE_BYTE_COUNT to determine the number of bytes in the RX_BUF_BYTE_x.

The TCPC sets the READABLE_BYTE_COUNT to 0 after the interrupt has been cleared.

The TCPC disables PD message delivery and set the READABLE_BYTE_COUNT to zero when detection of a disconnect.

Table 47. READABLE_BYTE_COUNT Register Definition

Bit(s)	Name	Type	Reset Value	Description
<7:0>	READABLE_BYTE_ COUNT	R	00h	Indicates the number of bytes in the RX_BUF_BYTE_x registers plus one (for the RX_BUF_FRAME_TYPE). The content of this register is undefined when the RECEIVE_BUFFER is cleared. The value in this register is less than or equal to 31.

RX_BUF_FRAME_TYPE (30h)

The TCPM reads the RX_BUF_FRAME_TYPE to determine the type of message.

Table 48. RX_BUF_FRAME_TYPE Register Definition

Bit(s)	Name	Type	Reset Value	Description
<7:3>	Reserved	R	00000b	Sets to zero by sender and ignored by receiver
<2:0>	Received SOP* Message	R	000b	000b: Received SOP 001b: Received SOP' 010b: Received SOP" 011b: Received SOP_DBG' 100b: Received SOP_DBG" 110b: Received Cable Reset All others are reserved.

RX_BUF_BYTE_x (30h)

The TCPM then reads the content of the USB PD message in RX_BUF_BYTE_x.

Table 49. RX_BUFFER_DATA Register Definition

Bit(s)	Name	Type	Reset Value	Description
<7:0>	Rx Buffer	R	00h	The TCPM reads the READABLE_BYTE_COUNT to determine the number of bytes in the RX_BUFFER_DATA. The TCPM then reads the content of the USB PD message in RX_BUFFER_DATA.

6.7.2.31 RECEIVE_BUFFER for TCPCi 1.0

If TCPM wants to use a RECEIVE_BUFFER with TCPCi 1.0, TCPC_SETTING_1.TCPC_v1.0_Enable should be set to 1. As a result, the following registers work.

This register indicates the status of the received SOP* message buffer in 30h..4Fh registers. This register is read by the TCPM when the TCPC indicates a SOP* message was received in the Alert Status registers.

If TCPM wants to read a RECEIVER_BUFFER with one I^2C transaction described in Reading the RECEIVE_BUFFER with TCPCi 1.0 mode, it should start from 30h: RECEIVE_BYTE_COUNT.

RECEIVE_BUFFER is read only.

RECEIVE_BYTE_COUNT (30h)

The TCPM reads the RECEIVE_BYTE_COUNT to determine the number of bytes in the RX_BUFFER_DATA_OBJECT.

The TCPC sets the RECEIVE_BYTE_COUNT to 0 after the interrupt has been cleared.

On detection of a Disconnect, the TCPC sets the RECEIVE_BYTE_COUNT to zero.

If TCPM wants to read a RECEIVER_BUFFER with one I²C transaction described in Reading the RECEIVE_BUFFER with TCPCi 1.0 mode, it should start from 30h:RECEIVE_BYTE_COUNT.

Table 50. RECEIVE_BYTE_COUNT Register Definition

Bit(s)	Name	Type	Reset Value	Description
<7:0>	RECEIVE_BYTE_COUNT	R	00h	Indicates number of bytes in this register that are not stale. The TCPM should read the first RECEIVE_BYTE_COUNT bytes in this register. This is the number of bytes in the RX_BUFFER_DATA_OBJECTS plus three (for the RX_BUF_FRAME_TYPE and RX_BUF_HEADER).

RX_BUF_FRAME_TYPE (31h)

The TCPM reads the RX_BUF_FRAME_TYPE to determine the type of message.

If TCPM would like to read a RECEIVER_BUFFER with one I²C transaction described in Reading the RECEIVE_BUFFER with TCPCi 1.0 mode, it should start from 30h:RECEIVE_BYTE_COUNT.

TCPM can read this register with TCPCi1.0 mode by one or two byte each as described in Reading Single Byte Registers or Reading Two-Byte Registers.

Table 51. RX_BUF_FRAME_TYPE Register Definition

Bit(s)	Name	Type	Reset Value	Description
<7:3>	Reserved	R	00000b	Sets to zero by sender and ignored by receiver
<2:0>	Received SOP* Message	R	000b	000b: Received SOP 001b: Received SOP' 010b: Received SOP'' 011b: Received SOP_DBG' 100b: Received SOP_DBG'' 110b: Received Cable Reset All others are reserved.

RX_BUF_HEADER (32h)

The TCPM then reads the information in the RX_BUF_HEADER.

If TCPM would like to read a RECEIVER_BUFFER with one I²C transaction described in Reading the RECEIVE_BUFFER with TCPCi 1.0 mode, it should start from 30h:RECEIVE_BYTE_COUNT.

TCPM can read this register with TCPCi1.0 mode by one or two byte each as described in Reading Single Byte Registers or Reading Two-Byte Registers.

Table 52. RX_BUF_HEADER Register Definition

Bit(s)	Name	Type	Reset Value	Description
<15:8>	RX_BUF_HEADER_BYTE_1	R	00h	Byte 1 (Bits <15:8>) of USB PD message header
<7:0>	RX_BUF_HEADER_BYTE_0	R	00h	Byte 0 (Bits <7:0>) of USB PD message header

RX_BUFFER_DATA_OBJECTS (34h~4Fh)

The TCPM then reads the information in the RX_BUFFER_DATA_OBJECT.

If TCPM would like to read a RECEIVER_BUFFER with one I2C transaction described in Reading the RECEIVE_BUFFER with TCPCi 1.0 mode, it should start from 30h:RECEIVE_BYTE_COUNT.

TCPM can read this register with TCPCi1.0 mode by one or two byte each like described in chapter Reading Single Byte Registers or Reading Two-Byte Registers.

Table 53. RX_BUFFER_DATA_OBJECTS Register Definition

Bit(s)	Name	Type	Reset Value	Description
<223:8>	RX_BUF_OBJn_ BYTE_m	R	00h	Byte m of nth data object
<7:0>	RX_BUF_OBJ1_ BYTE_0	R	00h	Byte 0 (Bits <7:0>) of 1st data object

6.7.2.32 TRANSMIT(50h)

The TCPM writes to this register to transmit a SOP* message where the SOP* message payload (i.e. the header bytes and the data bytes) was written into the TCPC's internal transmit buffer using the TRANSMIT_BUFFER register. The TCPC transmits the aggregate of data written to the TRANSMIT_BUFFER since the pointer was last reset either due to the TCPM writing to the TRANSMIT register or the TCPM writing to COMMAND.ResetTransmitBuffer (0xDD). The entire register is written at once and then sent. The TCPC clear the TRANSMIT register I2C_WRITE_BYTE_COUNT and its internal transmit buffer after executing the transmission regardless of the outcome (either successful, failed or discarded).

If the TCPM writes to TRANSMIT requesting a transmission that is not Hard Reset, Cable Reset or BIST Carrier Mode 2 (this means TRANSMIT.SOP*Message > 100b) and there are less than 2 bytes in the TX_BUF_BYTE_x register (this means the transmit buffer pointer is less than offset 3), the TCPC generate a FAULT_STATUS.I2CinterfaceError.

The tCableMessage timer (SOP' and SOP") is in the TCPM.

If the TCPM writes a Hard Reset command to this register while a transmission is in progress, a Hard Reset signal is sent as soon as possible.

The TCPM does not write to the TRANSMIT register to request a transmission other than Hard Reset while the TCPC is still processing a previous transmission (this means ALERT.TransmitSuccessful, TransmitFailed, or TransmitDiscarded have not yet been asserted since the last write to the TRANSMIT register). The TCPM does clear the resulting alert from a prior TRANSMIT write before writing to the TRANSMIT register again for anything other than a Hard Reset. If a previous TRANSMIT request has not yet completed when TRANSMIT is written requesting a Hard Reset, the TCPC assert the Transmission Discarded bit in the ALERT register.

The TCPM does not write to the TRANSMIT register to request a transmission other than Hard Reset until it has cleared all received message alerts. If the TCPM writes TRANSMIT when ALERT.ReceivedHardReset = 1 or ALERT.ReceivedSOP*MessageStatus = 1 the TCPC discard the transmit request and assert ALERT.TransmitSOP*MessageDiscarded.

The TCPC asserts one and only one of ALERT.TransmitSuccessful, TransmitFailed, or TransmitDiscarded following a write of the TRANSMIT register when a non-Hard Reset is transmitted. The TCPC asserts both ALERT.TransmitSuccessful and ALERT.TransmitFailed after it completes the sending of a Hard Reset. The TCPC clears the RECEIVE_DETECT and the READABLE_BYTE_COUNT register to disable the USB PD message passing when the TCPM writes the TRANSMIT register requesting a Hard Reset.

After the TCPC has transmitted the BIST Carrier Mode signaling and exited BIST Carrier Mode, the TCPC generate either ALERT.TransmitSuccessful (if successfully sent) or ALERT.TransmitDiscarded (if not successfully sent due to an incoming received message).

Table 54. TRANSMIT Register Definition

Bit(s)	Name	Type	Reset Value	Description
<7:6>	Reserved	R	00b	Sets to zero by sender and ignored by receiver
<5:4>	Retry Counter	R/W	00b	00b: No message retry is required 01b: Automatically retry message transmission once 10b: Automatically retry message transmission twice 11b: Automatically retry message transmission three times
<3>	Reserved	R	0b	Sets to zero by sender, is ignored by receiver
<2:0>	Transmit SOP* message	R/W	000b	000b: Transmit SOP 001b: Transmit SOP' 010b: Transmit SOP'' 011b: Transmit SOP_DBG' 100b: Transmit SOP_DBG'' 101b: Transmit Hard Reset 110b: Transmit Cable Reset 111b: Transmit BIST Carrier Mode 2 (TCPC exits the BIST mode no later than tBISTContMode max)

6.7.2.33 TRANSMIT_BUFFER for TCPCi 2.0

If TCPM wants to use a TRANSMIT_BUFFER with TCPCi 2.0, TCPC_SETTING_1.TCPC_v1.0_Enable should be set to 0. As a result, the following registers work.

The TRANSMIT_BUFFER holds the I2C_WRITE_BYTE_COUNT and the portion of the SOP* USB PD message payload (including the header and/or the data bytes) most recently written by the TCPM in TX_BUF_BYTE_x. TX_BUF_BYTE_x is "hidden" and can only be accessed by writing to register address 51h.

I2C_WRITE_BYTE_COUNT (51h)

Table 55. I2C_WRITE_BYTE_COUNT Register Definition

Bit(s)	Name	Type	Reset Value	Description
<7:0>	I2C_WRITE_BYTE_COUNT	W	00h	The number of bytes the TCPM intends to write to the TX_BUF_BYTE_x in the given I2C/SMBus transaction.

TX_BUFFER_DATA (51h)

The TCPM writes as many bytes in the buffer as defined in the I2C_WRITE_BYTE_COUNT in one I^2C write transaction. If the I2C_WRITE_BYTE_COUNT is different than the number of bytes written in the buffer, the TCPC asserts ALERT.InterfaceError and ignores the write (that is, no change in the TX_BUF_BYTE_x content and the offset).

Table 56. TX_BUFFER_DATA Register Definition

Bit(s)	Name	Type	Reset Value	Description
<7:0>	Tx Buffer	W	00h	The TCPM writes to this register to transmit a SOP* message where the SOP* message payload (i.e. the header bytes and the data bytes) was written into the TCPC's internal transmit buffer using the TX_BUFFER_DATA register.

6.7.2.34 TRANSMIT_BUFFER for TCPCi 1.0

If TCPM wants to use a TRANSMIT_BUFFER with TCPCi 1.0, TCPC_SETTING_1.TCPC_v1.0_Enable should be set to 1. As a result, the following registers work.

The TRANSMIT_BUFFER holds the TRANSMIT_BYTE_COUNT, the TX_BUF_HEADER, and the TX_BUFFER_DATA_OBJECTS (SOP* payload).

If TCPM wants to write a TRANSMIT_BUFFER with one I²C transaction described in Writing the TRANSMIT_BUFFER with TCPCi 1.0 mode, it should start from 51h:TRANSMIT_BYTE_COUNT.

TRANSMIT_BYTE_COUNT (51h)

If TCPM wants to write a TRANSMIT_BUFFER with one I²C transaction described in Writing the TRANSMIT_BUFFER with TCPCi 1.0 mode, it should start from 51h:TRANSMIT_BYTE_COUNT.

Table 57. TRANSMIT_BYTE_COUNT Register Definition

Bit(s)	Name	Type	Reset Value	Description
<7:0>	TRANSMIT_BYTE_COUNT	R/W	00h	The number of bytes the TCPM will write This is the number of bytes in the TX_BUFFER_DATA_OBJECTS plus two (for the TX_BUF_HEADER)

TX_BUF_HEADER (52h)

If TCPM would like to write a TRANSMIT_BUFFER with one I²C transaction as described in Writing the TRANSMIT_BUFFER with TCPCi 1.0 mode, it should start from 51h: TRANSMIT_BYTE_COUNT.

TCPM can write this register with TCPCi1.0 mode by one or two byte each as described in Writing Single Byte Registers or Writing Two-Byte Registers.

Table 58. TX_BUF_HEADER Register Definition

Bit(s)	Name	Type	Reset Value	Description
<15:8>	TX_BUF_HEADER_BYTE_1	R/W	00h	Byte 1 (Bits <15:8>) of USB PD message header
<7:0>	TX_BUF_HEADER_BYTE_0	R/W	00h	Byte 0 (Bits <7:0>) of USB PD message header

TX_BUFFER_DATA_OBJECTS (54h~6Fh)

If TCPM would like to write a TRANSMIT_BUFFER with one I²C transaction described in Writing the TRANSMIT_BUFFER with TCPCi 1.0 mode, it should start from 51h:TRANSMIT_BYTE_COUNT.

TCPM can write this register with TCPCi1.0 mode by one or two byte each as described in Writing Single Byte Registers or Writing Two-Byte Registers.

Table 59. TX_BUFFER_DATA_OBJECTS Register Definition

Bit(s)	Name	Type	Reset Value	Description
<223:8>	TX_BUF_OBJn_BYTE_m	R/W	00h	Byte m of nth data object
<7:0>	TX_BUF_OBJ1_BYTE_0	R/W	00h	Byte 0 (Bits <7:0>) of 1st data object

6.7.2.35 VBUS_VOLTAGE (70h)

The TCPM reads this register to determine the VBUS voltage measured on the Source or Sink at the USB Type-C Connector.

Table 60. VBUS_VOLTAGE Register Definition

Bit(s)	Name	Type	Reset Value	Description
<15:12>	Reserved	R	0000b	Sets to zero by sender and ignored by receiver
<11:10>	Scale Factor	R	00b	00: VBUS measurement not scaled. 01: VBUS measurement divided by 2 10: VBUS measurement divided by 4 11: reserved This field is fixed to 00b.
<9:0>	VBUS Voltage Measurement	R	000h	10-bit measurement of (VBUS / Scale Factor) TCPM multiplies this value by the scale factor to obtain the voltage measurement. All voltages meet ±2% absolute value or ±50mV, whichever is greater. The LSB is 25mV. This field is fixed to 10'h0 if POWER_CONTROL.VBUS_VOLTAGE monitor is zero.

6.7.2.36 VBUS_SINK_DISCONNECT_THRESHOLD (72h)

This register defines an edge-triggered threshold.

The TCPM writes to this register to set the threshold at which a Sink will start the Automatic Sink Discharge if it is in the Attached.SNK state.

Table 61. VBUS_SINK_DISCONNECT_THRESHOLD Register Definition

Bit(s)	Name	Type	Reset Value	Description
<15:10>	Reserved	R	000000b	Sets to 0
<9:0>	Voltage trip point	R/W	8Ch (3.5V)	10-bit for voltage threshold with 25mV LSB. (Default 3.5V) ±5% accuracy. A value of zero disables this threshold These fields are used for the ALERT.VBUS Sink Disconnect Detection. The TCPC will assert the ALERT if VBUS voltage crosses this value.

6.7.2.37 VBUS_STOP_DISCHARGE_THRESHOLD (74h)

This register defines an edge-triggered threshold for the Force Discharge circuit.

The TCPM writes to this register to set the threshold at which a Source stops the Forced Discharge circuit when POWER_CONTROL.Force Discharge = 1b.

A TCPC acting as a Source always discharge to vSafe0V on a disconnect, Hard Reset, or Power Role Swap.

Table 62. VBUS_STOP_DISCHARGE_THRESHOLD Register Definition

Bit(s)	Name	Type	Reset Value	Description
<15:10>	Reserved	R	000000b	Sets to 0
<9:0>	Voltage trip point	R/W	20h (0.8V)	10-bit for voltage threshold with 25mV LSB. (Default 0.8V) ±5% accuracy.

6.7.2.38 VBUS_VOLTAGE_ALARM_HI_CFG (76h)

This register defines the level triggered alarm thresholds.

The TCPM can write to POWER_CONTROL.DisableVoltageAlarms = 1b to disable the voltage alarms. The TCPM writes to VBUS_VOLTAGE_ALARM_HI_CFG to set the high voltage alarm level. The TCPC sets ALERT.VBUSVoltageAlarmHi to 1 when VBUS exceeds the high voltage alarm level. The TCPC re-assert ALERT.VBUSVoltageAlarmHi if the high voltage condition on VBUS prevails after the TCPM has cleared ALERT.VBUSVoltageAlarmHi unless the TCPM disables the voltage alarms by setting POWER_CONTROL.DisableVoltageAlarms to 1b.

Table 63. VBUS_VOLTAGE_ALARM_HI_CFG Register Definition

Bit(s)	Name	Type	Reset Value	Description
<15:10>	Reserved	R	000000b	Sets to 0
<9:0>	Voltage trip point	R/W	00h (0V)	10-bit for voltage threshold with 25mV LSB. ±5% accuracy.

6.7.2.39 VBUS_VOLTAGE_ALARM_LO_CFG (78h)

This register define the level triggered alarm thresholds.

The TCPM can write to POWER_CONTROL.DisableVoltageAlarms = 1b to disable the voltage alarms. The TCPM writes to VBUS_VOLTAGE_ALARM_LO_CFG to set the low voltage alarm level. The TCPC sets ALERT.VBUSVoltageAlarmLo to 1 when VBUS drops below the low voltage alarm level. The TCPC re-assert ALERT.VBUSVoltageAlarmLo if the low voltage condition on VBUS prevails after the TCPM has cleared ALERT.VBUSVoltageAlarmLo unless the TCPM disables the voltage alarms by setting POWER_CONTROL.DisableVoltageAlarms to 1b.

Table 64. VBUS_VOLTAGE_ALARM_LO_CFG Register Definition

Bit(s)	Name	Type	Reset Value	Description
<15:10>	Reserved	R	000000b	Sets to 0
<9:0>	Voltage trip point	R/W	00h (0V)	10-bit for voltage threshold with 25mV LSB. ±5% accuracy.

6.7.2.40 VBUS_NONDEFAULT_TARGET (7Ah)

The purpose of this register is to provide a normative way to set the target voltage for sourcing nondefault voltage over VBUS. The TCPM may write to this register to set the target voltage level of COMMAND.SourceVBUSNondefaultVoltage.

Table 65. VBUS_NONDEFAULT_TARGET Register Definition

Bit(s)	Name	Type	Reset Value	Description
<15:11>	Reserved	R	00h	Sets to 0
<10:0>	VBUS nondefault voltage target	R/W	000h (0V)	11-bit for the VBUS voltage target with 20mV LSB. ±5% accuracy.

6.7.2.41 Vendor Defined Registers

The TCPM should process/write Vendor Specific bits only if it recognizes the device and according to the specifications provided by that vendor.

TCPC_SETTING_1 (80h)

After the TCPC has set the power-on reset default values, this register is set and cleared only by the TCPM.

The ADC_monitor can set the number of moving average for ADC.

The TCPC Power Control can select I^2C interface of VBus control between Charger or TCPC.

The TCPC v1.0 Enable can change TCPC interface mode to Revision 1.0.

Table 66. TCPC_SETTING_1 Register Definition

Bit(s)	Name	Type	Reset Value	Description
<15:14>	ADC_monitor_mode	R/W	00b	00b: The ADC voltage is not used to calculate moving average 01b: The ADC voltage is calculated with 2 moving averages 10b: The ADC voltage is calculated with 4 moving averages 11b: The ADC voltage is not used to calculate moving average
<13>	ADC_control	R/W	0b	0b: ADC is enabled if TCPC Power Control bit is 1. 1b: ADC is disabled. This field provides instruction for disabling ADC circuit, however charger have some condition for disabling ADC. Therefore the ADC may not disable with this field set to disable.
<12:5>	Reserved	R	00b	Sets to zero by sender and ignored by receiver
<4>	TCPC Power Control	R/W	0b	VBUS TCPC Control 0b: Controlled by charger side I^2C. 1b: Controlled by TCPC side I^2C. TCPM can set charger registers in each setting.
<3:1>	Reserved	R	00b	Sets to zero by sender and ignored by receiver
<0>	TCPC Message Buffer Type	R/W	0b	0b: TCPC works with Revision 2.0 1b: TCPC works with Revision 1.0

TCPC_PARAMETER_1 (82h)

After the TCPC has set the power-on reset default values, this register is set and cleared only by the TCPM. The TCPM can set a tTCPC value.

If it needs, the TCPM writes to the TCPC_PARAMETER_1 register to set other values with 4µs LSB.

Table 67. TCPC_PARAMETER_1 Register Definition

Bit(s)	Name	Type	Reset Value	Description
<15:9>	Reserved	R	00h	Sets to zero by sender and ignored by receiver
<8:2>	tTCPCfilter	R/W	64h (400µs)	250~500µs Lower 2 Bits are fixed at 0
<1:0>		R	00b	

TCPC_PARAMETER_2 (84h)

After the TCPC has set the power-on reset default values, this register is set and cleared only by the TCPM. The TCPM can set a tFRSwapTx value and a tFRSwapRx value. If it needs, the TCPM writes to the TCPC_PARAMETER_2 register to set other value with 4µs LSB.

Table 68. TCPC_PARAMETER_2 Register Definition

Bit(s)	Name	Type	Reset Value	Description
<15:14>	Reserved	R	00b	Sets to zero by sender and ignored by receiver
<13:10>	tFRSwapRx	R/W	1010b (40µs)	Fast Role Swap request detection time (30~50µs) Lower 2-bits are read as 0
<9:8>		R	00b	
<7:2>	tFRSwapTx	R/W	010110b (88µs)	Fast Role Swap request transmit duration (60~120µs) Lower 2-bits are read as 0
<1:0>		R	00b	

TCPC_VENDOR_CONTROL_3 (88h)

After the TCPC has set the power-on reset default values, this register is set and cleared by the TCPM.

Table 69. TCPC_VENDOR_CONTROL_3 Register Definition

Bit(s)	Name	Type	Reset Value	Description
B7	Enable Sink Suspend Signal	R/W	0b	This bit is supposed to be set to zero. It is set to one only if the power consumption of the Arches cannot meet the pSnkSusp spec when both the vbus_sourcing_enable and the vbus_sinking_enable are deasserted. 0b: Disable to assert the vbus_sink_susp signal when both the vbus_sourcing_enable and the vbus_sinking_enable signals are deasserted. So that the vbus_sink_susp signal is always deasserted. 1b: Enable to assert the vbus_sink_susp signal when both the vbus_sourcing_enable and the vbus_sinking_enable signals are deasserted.
B6	Disable OV/UV Detection	R/W	0b	0b: The cctop HW controls vbus_dis_otg_uv signal. 1b: The vbus_dis_otg_uv signal is always high.
B5	Reserved	R	0b	Sets to zero by sender and ignored by receiver
B4	Auto Vconn Disable when Disconnect	R/W	0b	0b: The TCPC not automatically disable Vconn (default) 1b: The TCPC automatically disable when TCPC detects disconnect
B3	ATTSNK_EXIT_MODE	R/W	0b	Exit condition selection of the Attached.SNK bit (Move from C8h register) 0: VBUS Removed 1: VBUS Removed or SNK.Open If TCPM set this field to 1b, TCPC transition to Unattached state from Attached.SNK state when it detects SNK.Open with tPDDebounce (15ms).
B2	Reserved	R	0b	Sets to zero by sender and ignored by receiver

Table 69. TCPC_VENDOR_CONTROL_3 Register Definition (Cont.)

Bit(s)	Name	Type	Reset Value	Description
B1	Enable I2CSLV Clock Gating	R/W	0b	0b: 24MHz clock for I2CSLV is not gated 1b: 24MHz clock for I2CSLV is gated during no I^2C Transaction
B0	Enable PDCTRL Clock Gating	R/W	0b	0b: 24MHz clock for PDCTRL is not gated 1b: 24MHz clock for PDCTRL is gated during no PD Message

TCPC_VENDOR_STATUS_MASK (8Ah)

The TCPM can set MASK for VENDOR_STATUS.Operating Mode.

Table 70. TCPC_VENDOR_STATUS_MASK Register Definition

Bit(s)	Name	Type	Reset Value	Description
<7:2>	Reserved	R	00h	Sets to zero by sender and ignored by receiver
<1>	OTG OV/UV Detection Mask	R/W	0b	0b: Interrupt masked 1b: Interrupt unmasked
<0>	Operating Mode Interrupt Mask	R/W	0b	0b: Interrupt masked 1b: Interrupt unmasked This bit masked only field of operating mode.

TCPC_VENDOR_STATUS (8Bh)

The TCPM should read this register when ALERT.VENDOR_STATUS has asserted. The Operating mode may not be asserted because it is indicated in real-time.

Table 71. TCPC_VENDOR_STATUS Register Definition

Bit(s)	Name	Type	Reset Value	Description
<7:2>	Reserved	R	000h	Sets to zero by sender and ignored by receiver
<1>	OTG OV/UV Detected	R	0b	This bit is set when the otg_mode_on signal is changed from 1 to 0 and the POWER_STATUS.SourcingVBUS is 1. This bit is cleared when the SourceDefaultVbusVoltage or the SinkVbus command is received. 0b: OTG OV/UV is not detected 1b: OTG OV/UV has been detected
<0>	Operating Mode	R	0b	This bit provides a real-time indication of the Source's operating mode. 0b: Constant Voltage (CV). 1b: Current Limit (CL).

VBUS_5V_TARGET (90h)

The TCPM writes to this register to set the target voltage level of COMMAND.SourceVbusDefaultVoltage.

When the command is written, the value of this register is reflected in VBUS.

Table 72. VBUS_5V_TARGET Register Definition

Bit(s)	Name	Type	Reset Value	Description
<15:9>	Reserved	R	00b	Sets to zero by sender and ignored by receiver
<8:0>	VBUS voltage target	R/W	107h (5.26V)	9-bit for the VBUS voltage target with 20mV LSB. ±5% accuracy.

VBUS_CURRENT_TARGET (92h)

The TCPM writes to this register to set the target current level during Sourcing VBUS.

When Sourcing VBUS is enabled, the value of this register is always reflected in VBUS.

Table 73. VBUS_CURRENT_TARGET Register Definition

Bit(s)	Name	Type	Reset Value	Description
<15:8>	Reserved	R	00h	Sets to zero by sender and ignored by receiver
<7:0>	VBUS current target	R/W	64h (3.2A)	8-bit for the VBUS current target with 32mA LSB. The value 64h (3.2A) is based on Rs1 = 20mΩ. Scaling the register accordingly for different sense resistor selections. Please see Selecting the Sense Resistors.

VBUS_OCP_UV_THRESHOLD (94h)

The TCPM writes to this register to set the detect voltage level of overcurrent protection during Sourcing VBUS.

Table 74. VBUS_OCP_UV_THRESHOLD Register Definition

Bit(s)	Name	Type	Reset Value	Description
<15:10>	Reserved	R	00h	Sets to 0
<9:0>	Voltage trip point	R/W	000h (0V)	10-bit for voltage threshold with 25mV LSB. ±5% accuracy.

STOP_DISCHARGE_THRESHOLD_VSAFE0V (96h)

The TCPC uses the VCONN threshold when the TCPC discharges VCONN voltage.

The TCPC uses the VBUS threshold value when auto discharge function or COMMAND.DisableSourceVbus.

Table 75. STOP_DISCHARGE_THRESHOLD_VSAFE0V Register Definition

Bit(s)	Name	Type	Reset Value	Description
<15:8>	VCONN Voltage Trip Point	R/W	10h (0.4V)	8-bit for voltage threshold with 25mV LSB. ±5% accuracy.
<7:0>	VBUS Voltage Trip Point	R/W	10h (0.4V)	8-bit for voltage threshold with 25mV LSB. ±5% accuracy.

VIN_STOP_DISCHARGE_THRESHOLD_VSAFE0V (98h)

The TCPC uses this VIN threshold when the TCPC discharges VIN voltage.

Table 76. VIN_STOP_DISCHARGE_THRESHOLD_VSAFE0V Register Definition

Bit(s)	Name	Type	Reset Value	Description
<7:0>	VIN Voltage Trip Point	R/W	04h (425.6mV)	8-bit for voltage threshold with 25mV LSB (default 5.5V) ±5% accuracy.

VBUS_PRESENT_THRESHOLD (9Ah)

The TCPM writes to this register to set the voltage threshold of POWER_STAUS.VBUS Present.

Table 77. VBUS_PRESENT_THRESHOLD Register Definition

Bit(s)	Name	Type	Reset Value	Description
<15:10>	Reserved	R	000000b	Sets to zero by sender and ignored by receiver
<9:0>	Voltage Trip Point	R/W	096h (Default 3.75V)	10-bit for voltage threshold with 25mV LSB. ±5% accuracy.

VCONN_VOLTAGE (9Ch)

The TCPM can read Vconn volage when Enable_Vconn is 1 or TCPC is discharging Vconn. In other cases, it indicates voltage on Vconn Pin. The Scale Factor is fixed with 00b, so it is always indicated by 25mV LSB. TCPC indicates this value with 0 to 6.2V.

Table 78. VCONN_VOLTAGE Register Definition

Bit(s)	Name	Type	Reset Value	Description
<15:12>	Reserved	R	0000b	Sets to zero by sender and ignored by receiver

Table 78. VCONN_VOLTAGE Register Definition (Cont.)

Bit(s)	Name	Type	Reset Value	Description
<11:10>	Scale Factor	R	00b	00: Vconn measurement not scaled. 01: Vconn measurement divided by 2 10: Vconn measurement divided by 4 11: Reserved
<9:0>	Vconn voltage measurement	R	000h	10-bit measurement of (Vconn/Scale Factor) TCPM multiplies this value by the scale factor to obtain the voltage measurement. All voltages meet ±2% absolute value or ±50mV, whichever is greater. The LSB is 25mV. This register indicates the value of voltage of VCONN_POWER pin or CC1/CC2 pin. There are three cases: ▪ Sourcing Vconn: Indicates the voltage of VCONN_POWER pin ▪ Discharging Vconn: Indicates the voltage of CC1/CC2 pin ▪ Not using Vconn: Invalid

TYPE_C_SETTING_1 (C0h)

TCPC controls this register. TCPC sets Bit 0 to 6 only when necessary. After the TCPC has set the power on reset default values 0000h. TX2/1_SEL and RX2/1_SEL are set by TCPC.

Table 79. TYPE_C_SETTING_1 Register Definition

Bit(s)	Name	Type	Reset Value	Description
<15>	TX2_SEL	R/W	0b	Monitor and control CC-PHY interface signals and connection CC1/CC2. When USB PD communication is not permitted state (except Attached.SNK, Attached.SRC, DebugAccessory, PoweredAccessory), it is set to 00, If it is a permitted state, set to 01 or 10 by direction detection.
<14>	TX1_SEL	R/W	0b	See TX2_SEL
<13>	RX2_SEL	R/W	0b	Monitor and control CC-PHY interface signals and connection CC1/CC2. When USB PD communication is not permitted state (except Attached.SNK, Attached.SRC, DebugAccessory, PoweredAccessory), it is set to 00, If it is a permitted state, set to 01 or 10 by direction detection.
<12>	RX1_SEL	R/W	0b	See RX2_SEL
<11:10>	Reserved	R	00b	Is set to zero by sender and ignored by receiver
<9>	IP2_EN	R/W	0b	CC2 Rp Current Source Enable 0: Disable 1: Enable TCPM can set this bit and control the NMOS FET to protect CC2 from reverse current when the power is off.
<8>	IP1_EN	R/W	0b	CC1 Rp Current Source Enable 0: Disable 1: Enable TCPM can set this bit and control the NMOS FET to protect CC1 from reverse current when the power is off.

Table 79. TYPE_C_SETTING_1 Register Definition (Cont.)

<7>	RDOE	R/W	0b	CC-PHY interface signal RDOE control bit TCPM can write to this bit and control RDOE. 0: Hi-Z (Controlled by Dead Battery Rd) 1: High or Low (Controlled by TCPC or Type-C state) When the system is SRC only, TCPM should set this bit to 1 after ROLE_CONTROL.CC2/CC1 sets to Rp.
<6>	CC2_CMP3_EN	R/W	0b	CC2 Comparator 3 Enable TCPC controls CC2_CMP3_EN signal Automatically. TCPM controls CC2_CMP3_EN signal through this bit. The signal path of TCPC control and register are connected OR logic, so High value has priority. 0: Disable 1: Enable
<5>	CC2_CMP2_EN	R/W	0b	CC2 Comparator 2 Enable TCPC controls CC2_CMP2_EN signal Automatically. TCPM controls CC2_CMP2_EN signal through this bit. The signal path of TCPC control and register are connected OR logic, so High value has priority. 0: Disable 1: Enable
<4>	CC2_CMP1_EN	R/W	0b	CC2 Comparator 1 Enable TCPC controls CC2_CMP1_EN signal Automatically. TCPM controls CC2_CMP1_EN signal through this bit. The signal path of TCPC control and register are connected OR logic, so High value has priority. 0: Disable 1: Enable
<3>	CC1_CMP3_EN	R/W	0b	CC1 Comparator 3 Enable TCPC controls CC1_CMP3_EN signal Automatically. TCPM controls CC1_CMP3_EN signal through this bit. The signal path of TCPC control and register are connected OR logic, so High value has priority. 0: Disable 1: Enable
<2>	CC1_CMP2_EN	R/W	0b	CC1 Comparator 2 Enable TCPC controls CC1_CMP2_EN signal Automatically. TCPM controls CC1_CMP2_EN signal through this bit. The signal path of TCPC control and register are connected OR logic, so High value has priority. 0: Disable 1: Enable

Table 79. TYPE_C_SETTING_1 Register Definition (Cont.)

<1>	CC1_CMP1_EN	R/W	0b	CC1 Comparator 1 Enable TCPC controls CC1_CMP1_EN signal Automatically. TCPM controls CC1_CMP1_EN signal through this bit. The signal path of TCPC control and register are connected OR logic, so High value has priority. 0: Disable 1: Enable
<0>	CC_DB_EN	R/W	0b	CC debounce enable bit TCPC controls CC_DB_EN signal Automatically. TCPM controls CC_DB_EN signal through this bit. The signal path of TCPC control and register are connected OR logic, so High value has priority. 0: Disable debounce 1: Enable debounce **Note:** If this bit is 0, the debounce value is retained. Processing resumes when this bit is set from 0 to 1 during debounce processing.

PD_PHYSICAL_SETTING_1 (E0h)

The TCPM writes to this register to control the analog characteristics of the physical layer.

Table 80. PD_PHYSICAL_SETTING_1 Register Definition

Bit(s)	Name	Type	Reset Value	Description
<15:10>	Reserved	R	00b	Sets to zero by sender and ignored by receiver
<9>	Receiver Enable	R/W	0b	To set the rx enable for receiver comparator. 0b: Disable 1b: Enable
<8>	Squelch Enable	R/W	0b	To set the rx enable for squelch comparator. 0b: Disable 1b: Enable
<7:1>	Reserved	R	00h	Sets to zero by sender and ignored by receiver
<0>	Tx LDO11 Enable	R/W	0b	To set the tx enable for LDO11. 0b: Disable 1b: Enable

PD_PHYSICAL_SETTING_2 (E2h)

The TCPM may write to this register to control the analog characteristics of the physical layer.

Table 81. PD_PHYSICAL_SETTING_2 Register Definition

Bit(s)	Name	Type	Reset Value	Description
<15:12>	Tx LDO11 Gain Control	R/W	0101b	To set the tx gain for LDO11.
<11:8>	Tx Slew Rate Control	R/W	0000b	To set the tx slew rate.
<7:0>	Tx Gain Control	R/W	00h	To set the tx gain.

PD_PHYSICAL_PARAMETER_1 (E8h)

The TCPM may write to this register to control the digital characteristics of the physical layer.

Table 82. PD_PHYSICAL_PARAMETER_1 Register Definition

Bit(s)	Name	Type	Reset Value	Description
<15:13>	nTransitionCount	R/W	011b (3)	To set count number to judge squelch detection Count number depend on nTransitionCount in Power Delivery specification.
<12:8>	tTransitionWindow	R/W	01100b (12)	To set the time to judge squelch detection The judge time depend on tTransitionWindow in Power Delivery specification.
<7>	Reserved	R	0b	Sets to zero by sender and ignored by receiver
<6:5>	Rx Vth	R/W	00b	To set the Rx threshold for receiver comparator.
<4:0>	Noise Filter Count	R/W	00111b	To set Noise filter step of receiving data. 0: No filter > 0: Filter step number

PD_PHYSICAL_PARAMETER_2 (EAh)

The TCPM may write to this register to control the digital characteristics of the physical layer.

Table 83. PD_PHYSICAL_PARAMETER_2 Register Definition

Bit(s)	Name	Type	Reset Value	Description
<15:10>	Reserved	R	00h	Sets to zero by sender and ignored by receiver
<9>	Rx BMC Correction	R/W	1b	To set adjusting threshold value to judge 0 or 1 with BMC receive wave. 0b: Disable 1b : Enable
<8>	Rx Ordered Sets Correction	R/W	0b	To set whether to judge it as valid when three out of four order sets are correct. 0b : Disable 1b : Enable
<7>	Reserved	R	0b	Sets to zero by sender and ignored by receiver
<6:4>	FRSwapRx Detect Bit	R/W	100b	To select RxSquAmpl bit setting to detect Fast Role Swap signaling. 000b: RxSquAmpl[4] 001b: RxSquAmpl[5] 010b: RxSquAmpl[6] 011b: RxSquAmpl[7] 100b: RxSquAmpl[8] 101b: RxSquAmpl[9] 110b: RxSquAmpl[10] 111b: RxSquAmpl[11]
<3:0>	Rx Squelch Detect Threshold	R/W	1001b	To set threshold value for squelch detection. To judge squelch detection have done, if the difference between maximum value and minimum value form RxSeqAmpl signal input is over setting value.

7. Battery Charger Controller Application Information

7.1 Start-Up

The RAA489000 includes an LDO with a nominal 5V output and an internal input OR-ed from the VBUS, VBAT and VSYS inputs. The output of the LDO is connected to the VDD pin. The LDO has 2 modes:

- Low Power mode - With a current limit of around 30mA that is generally active in Battery Only mode.
- High Power mode - With a current limit of around 160mA that is generally active when adapter is present (or with certain features enabled in Battery Only mode).

The LDO provides the bias power and gate drive power for the RAA489000. The VDDP pin is the RAA489000 gate drive power supply input. Use an R-C filter to generate the VDDP pin voltage from the VDD pin voltage.

When V_{DD} > 2.7V, the 2.5V LDO is enabled. When the output of the 2.5V LDO rises above 2.4V POR threshold, the RAA489000 digital block is activated and the SMBus register is ready to communicate with the master controller. If the 2.5V LDO is not active, the chip is in idle state and the digital block is reset.

When the RAA489000 turns on the LDOs, it sources a current out of the PROG pin and reads the pin voltage to determine the PROG resistor value. The PROG resistor programs the configurations of the RAA489000. See Table 84.

When CSIN >3.6V, the RAA489000 pulls up on the internal ACOK signal. When ACOK is high and VDD is higher than 3.8V rising, the state machine starts moving and after a 150ms debounce time, the RAA489000 starts switching.

The ACOK (VBUSOK) indicates the presence of the adapter and readiness of the adapter to supply power to the system bus. ACOK does not go low when the RAA489000 enters FAULT state from VSYS or CHRG, so it does not create the ACOK PROCHOT#.

When VBUS is higher than 3.8V, ASGATE is turned on. ASGATE can be forced OFF if the RAA489000 is in READY state. Customers can use Control8 Bit<13> to force OFF ASGATE in READY state. ASGATE is used to turn on/off a part of back-to-back NFETs. Also, ASGATE controls the inrush current into the input cap to a maximum of around 139mA. **Note**: Control8 Bit<13> has no effect when ASGATE is controlled by TCPC.

Two thresholds affect ACOK, and the higher of the two is in control of ACOK. One threshold is fixed for CSIN >3.6V and the other threshold is programmable using the DAC (see Table 2 for the ACOKRef register). The Register 0x40 value sets the threshold. The default register value is set to 0x0000h and disables the programmable threshold detection. The programmable threshold is helpful for monitoring the input supply when targeting higher voltages using USB Power Delivery communications. The ADC is automatically enabled when the ACOK Ref register is programmed to a non-zero value. To detect an unplugged adapter, the adapter voltage has to fall below the ACOK threshold (the higher of 3.4V falling and the ACOK Ref register value).

In Battery Only mode, the RAA489000 enters Low Power mode if only the battery is present. The LDO enters high power mode when ADC is enabled (or when adapter is plugged in).

For certain applications, it may be necessary to use lower gate charge FETs. Buck-boost can also be run at lower frequency to keep the temperature within the desired operating range so that the total power drawn from VDD is within acceptable range.

The VCONN MUX provides power from the VCONN POWER to the appropriate CC1 or CC2 line. The RAA489000 can act as a UFP (sink), DFP (source), or DRP (both). The cable detection uses three comparators to determine orientation and attach/detach.

The Cable Setting places a pull-up current source on the CCx line to indicate a source (DFP). It places a pull-down resistor to indicate a sink (UFP). Or it toggles between the two for a Dual Role Port (DRP).

Dead battery: When there is no power and the battery is removed or discharged, the dead battery advertises a sink (UFP) on both CC1 and CC2, so that VBUS can get 5V applied. After powering up, the dead battery circuit is disabled.

All the voltages listed in this section are approximate values for reference only. The customer is advised to check the EC table for accurate voltage and current thresholds and limits.

7.2 Programming Resistor

A 1% or 0.1% (for 965Ω option only) resistor from the PROG pin to GND programs the configuration of the RAA489000.

The AdapterCurrentLimit2 register default value is 1.5A, which is not affected by this programming resistor.

Address: four selections, both TCPC and charger SMBUS/I2C (1 = Master default; 2, 3, and 4 = Slave default)

The addresses for the TCPC and Charger are paired.

- 1 - TCPC 0x44h CHG 0x12h
- 2 - TCPC 0x46h CHG 0x92h
- 3 - TCPC 0x48h CHG 0x94h
- 4 - TCPC 0x4Ah CHG 0x96h

Table 84 shows the programming options.

Table 84. PROG Pin Programming Table

PROG-GND Resistance (Ω)			Cell Count	I2C Address	Default Adapter current Limit 1 Reg (A)	Information2 <4:0>
Min	Nominal	Max				
229.68	232	234.32	2	1	0.476	00001
344.52	348	351.48	2	1	1.5	00010
470.25	475	479.75	2	2	0.476	00011
584.1	590	595.9	2	2	1.5	00100
707.85	715	722.15	2	3	0.476	00101
836.55	845	853.45	2	3	1.5	00110
964.035[1]	965[1]	965.965[1]	2	4	0.476	00111
1138.5	1150	1161.5	2	4	1.5	01000
1386	1400	1414	3	1	0.476	01001
1633.5	1650	1666.5	3	1	1.5	01010
1851.3	1870	1888.7	3	2	0.476	01011
2187.9	2210	2232.1	3	2	1.5	01100
2712.6	2740	2767.4	3	3	0.476	01101
3207.6	3240	3272.4	3	3	1.5	01110
3702.6	3740	3777.4	3	4	0.476	01111
4375.8	4420	4464.2	3	4	1.5	10000
5435.1	5490	5544.9	4	1	0.476	10001
6425.1	6490	6554.9	4	1	1.5	10010
7425.0	7500	7575.0	4	2	0.476	10011
8365.5	8450	8534.5	4	2	1.5	10100
9216.9	9310	9403.1	4	3	0.476	10101

Table 84. PROG Pin Programming Table (Cont.)

PROG-GND Resistance (Ω)			Cell Count	I²C Address	Default Adapter current Limit 1 Reg (A)	Information2 <4:0>
Min	Nominal	Max				
1089	11000	11110	4	3	1.5	10110
12573	12700	12827	4	4	1.5	10111

1. Tolerance is tighter for this selection; 0.1% required. Other selections are typically 1% tolerance.

The RAA489000 uses the default number of cells in series shown in Table 84 and sets the default MaxSystemVoltage register value accordingly, but the default MinSystemVoltage register is 0V to prevent charging.

The switching frequency can be changed through SMBus Control1 register Bit<9:7> after POR. See Table 4 for detailed information.

When VDD is turned on, the RAA489000 typically sources 130µA current out of the PROG pin and reads the PROG pin voltage to determine the resistor value. However, application environmental noise may pollute the PROG pin voltage and cause an incorrect reading. If noise is a concern, connect a capacitor from the PROG pin to GND to provide filtering. The resistor and the capacitor RC time constant should be less than 40µs so the PROG pin voltage can rise to steady state before the RAA489000 reads it.

By default, whenever the adapter is unplugged and ACOK goes from high to low, the RAA489000 resets the AdapterCurrentLimit1 register back to the default setting determined by the PROG pin resistor. This current limit reloading can be disabled using Control3 Bit <14> (see Table 6).

In Battery Only mode, the RAA489000 resets the MaxSystemVoltage register to the default value according to the PROG pin cell number setting.

The current limit values in this datasheet are based on current-sensing resistors R_{s1} = 20mΩ and R_{s2} = 10mΩ unless specified otherwise.

7.3 Charger Control Register Operations

7.3.1 System Voltage Regulation and Maximum Charging Voltage Regulation

If the battery is absent, or if a battery is present but BGATE is turned off, the RAA489000 regulates the system bus voltage at the MaxSystemVoltage register setting if Control0 register Bit<1> is set to 0. However, when Control0 register Bit<1> is set to 1, the system bus voltage is regulated to the MaxSystemVoltage register setting plus an offset of 384mV. The CSOP pin senses the system bus voltage. When a valid adapter voltage is not present and only the battery is present, the RAA489000 enters the low power state. In the low power state the BGATE is turned on and charge current is not controlled in case VSYS is raised above the battery. To set the maximum charging voltage or the system regulating voltage, write a 16-bit MaxSystemVoltage command to register address 0x15H using the Write-word protocol shown in Figure 25 and the data format shown in Table 2.

The MaxSystemVoltage register accepts any voltage command but only the valid register bits are written to the register and the maximum values are clamped. A 0x0000H command in REG 0x15H causes the RAA489000 to stop switching and enter the READY state.

When the RAA489000 is not charging but is in the VSYS state and Control0 register Bit<1> is a 0, the system voltage is regulated to the same setting as the DAC. However, when Control0 register Bit<1> is a 1, system voltage is regulated to the DAC plus an offset of 384mV, which is useful to avoid discharging a full battery in the VSYS state during a system load transient.

The MaxSystemVoltage register sets the battery full charging voltage limit. The MaxSystemVoltage register setting is also the system bus voltage regulation point when the battery is absent, or when the battery is present but is not in Charging mode. The MinSystemVoltage register setting is also the system voltage regulation point

when the battery is in Trickle Charging mode. The CSOP pin is the system voltage regulation sense point in Trickle Charging mode. The MinSystemVoltage register setting is also the system voltage regulation point when the battery is in Trickle Charging mode. The CSOP pin is the system voltage regulation sense point in Trickle Charging mode.

The CSOP pin senses the battery voltage for maximum charging voltage regulation. The CSOP pin is also the system bus voltage regulation sense point and controls the VSYS operating voltage.

7.3.2 Normal/Fast Battery Charging and Charging Current Limit

To set the charging current limit, write a 16-bit ChargeCurrentLimit command to register address 0x14H (see Table 2) using the Write-word protocol shown in Figure 25. Set ChargeCurrent Limit and MinSystemVoltage to non zero to start trickle or fast/normal charging. It is not recommended to set only one of these registers to 0.

By default, the adapter current-sensing resistor, R_{s1}, is 20mΩ and battery current-sensing resistor, R_{s2}, is 10mΩ. Using the R_{s1} = 20mΩ and R_{s2} = 10mΩ option results in a 4mA/LSB correlation in the SMBus current commands.

If the R_{s1} and R_{s2} values are different from the R_{s1} = 20mΩ and R_{s2} = 10mΩ option, the SMBus commands need to be scaled accordingly to obtain the correct current. Smaller current sense resistor values reduce the power loss, and larger current sense resistor values give better accuracy. For example, if $R_{s2,}$ = 5mΩ, multiply each value in the DAC table by 2.

The RAA489000 limits the charging current by limiting the CSOP - CSON voltage, which reduces the current sense resistor value double the current is being regulated to. By using the recommended current sense resistor values R_{s1} = 20mΩ and R_{s2} = 10mΩ, the register's LSB always translates to 4mA of charging current. The ChargeCurrentLimit register accepts any charging current command, but only the valid register bits are written to the register.

After POR, the ChargeCurrentLimit register is reset to 0x0000H which disables fast charging but not trickle charging. To enable fast charging the battery, write a non-zero number to the ChargeCurrentLimit register. The ChargeCurrentLimit register should be read back to verify its content.

When charging, system voltage is regulated to VBAT plus some IR drop due sense resistor and BFET ON-resistance. The system voltage is above the MinsystemVoltage DAC setting and below the MaxSystemVoltage DAC setting plus appropriate offsets.

7.3.3 Trickle Charging and Minimum System Voltage Regulation

Writing the MinSystemVoltage register, 0x3EH to 0x0000h disables all battery charging.

The RAA489000 supports trickle charging to an overly discharged battery. The RAA489000 can activate the trickle charging function when the battery voltage is lower than the MinSystemVoltage setting. The VBAT pin is the battery voltage sense point for Trickle Charge mode. While trickle charging the battery, the system regulation voltage is the DAC setting plus 384mV.

To set the minimum system voltage, write a 16-bit MinSystemVoltage command to register address 0x3EH using the Write-word protocol shown in Figure 25 and the data format shown in Table 2. To enable Trickle Charging, set the MinsystemVoltage register to a non-zero value higher than battery voltage. To disable trickle charging, set the MinsystemVoltage register to 0V. Setting register address 0x3EH to 0x0000h disables all charging, which is the default and must be changed to allow any charging. The MinSystemVoltage register accepts any voltage command, but only the valid register bits are written to the register. The MinSystemVoltage register value should be set lower than the MaxSystemVoltage register value.

See Table 88 for trickle charging control logic.

When using the standard sense resistor, the trickle charging current can be programmed through SMBus Control2 register Bit<15:13> (see Table 5).

In Trickle Charging mode, the RAA489000 regulates the system voltage to the MinSystemVoltage DAC setting with voltage sensed at the CSOP pin. Another independent control loop controls the BGATE FET so that the

trickle charge current is maintained at the current set in the Trickle Charging Current register Control2<15:13>. The CSOP pin is the system voltage sensing point in Trickle Charging mode.

When the battery voltage is charged above the MinSystemVoltage register value, the RAA489000 enters Fast Charging mode by limiting the charging current at the ChargeCurrentLimit register setting using just the buck-boost switcher. The BFET is fully turned on.

The MinSystemVoltage register sets the battery voltage threshold for entering and exiting Trickle Charging mode and for entering and exiting Learn mode. The VBAT pin senses the battery voltage to compare with the MinSystemVoltage register setting. See Battery Learn Mode for details.

7.3.4 Autonomous Charging Mode

Autonomous Charging mode enables automatic end of charge termination. This mode can be enabled or disabled through SMBus Control3 register Bit<7> (Table 6). When Autonomous Charging mode is enabled, the SMBus timeout timer is disabled. Autonomous Charging mode is not disabled by writing SMBus ChargingCurrentLimit or MaxSystemVoltage commands. If Autonomous Charging mode is set for 12 hours and the battery does not terminate charging, the control bit is reset, disabling Autonomous Charging. The control bit is also reset if a Fault occurs. Control7 register Bit<9:8> sets the End of Charging (EOC) current settings (Table 8) and the Control3 register Bit<13> sets the debounce time (Table 6).

The RAA489000 enters Autonomous Charging mode when the BGATE MOSFET is on and the battery voltage is lower than the MaxSystemVoltage by a certain threshold (See Auto Recharge Threshold Relative to Maximum System Voltage in the Electrical Specifications table) for 1ms debounce time.

In Autonomous Charging mode, the RAA489000 starts to charge the battery with the programmed value (REG0x14h), the PROCHOT# pin behaves as Autonomous Charging mode indication pin and is pulled down to GND, and the SMBus timeout timer is disabled. The RAA489000 exits Autonomous Charging mode when the battery charging current is less than the EOC setting for 20ms or 200ms in CV loop. The autonomous charging termination time can be set by Control3 register Bit<13>. The RAA489000 enters Autonomous Charging mode when the battery voltage falls below the MaxsystemVoltage - Auto Recharge Threshold for 1ms debounce time and the BGATE MOSFET is on. If the RAA489000 stays in Autonomous Charging mode for 12 hours, the battery charging current is higher than EOC and the battery can not be charged to MaxSystemVoltage for 12 hours. The RAA489000 then stops charging the battery and exits Autonomous Charging mode and the control bit is reset.

7.3.5 SMBus Timeout

The RAA489000 includes a watchdog timer to ensure the SMBus master is active and to prevent overcharging the battery. The RAA489000 terminates charging by turning off the BGATE FET if the charger has not received a write command to the MaxSystemVoltage or ChargeCurrent register within 175s (SMBus Control3 register Bit<12:11> = 00). The SMBus timeout time can be configured through SMBus Control3 register Bit<12:11>. When the charging is terminated by the SMBus timeout, the ChargeCurrent register retains its value instead of resetting to zero. If a timeout occurs, the MaxSystemVoltage or ChargeCurrent register must be written to re-enable charging. The charger does not terminate charging, but instead enters a CV charge state with a very small charging current. The termination and start of another recharge cycle is controlled by the SMBus master. If SMBus Timeout is disabled and a fault occurs, the RAA489000 stays in the fault mode until the disable bit is cleared.

Enabling Autonomous Charge disables the timer and sets PROCHOT# to be an Autonomous Charging indicator.

You can disable the SMBus timeout function through SMBus Control0 register Bit<7> as Table 3 shows.

7.3.6 BATGONE

The BATGONE pin is a dual-purpose pin that provides both an analog and a digital function. If pulled to VDD, the pin indicates a battery gone state (the digital function). In addition, an NTC can be connected from this pin to ground (the analog function).

A 1µA current pulls up the BATGONE pin when not making an NTC ADC sample. A BATGONE condition is indicated if the pin voltage exceeds V_{DD} minus a PMOS threshold.

If BATGONE goes high the devices exist BATTERY LEARN mode.

7.3.7 NTC for Supporting JEITA Profiles

In addition to the internal die temperature, you can use a thermistor for an NTC on the BATGONE pin. The NTC is sensed using a pulsed current source with three source current levels for reading the thermistor voltage on the pin. Table 85 shows the control truth table.

Table 85. JEITA Control Bits Truth Table

CTRL2<5> JEITA Bit<1>	CTRL4<14> JEITA Bit<0>	Description
0	0	No JEITA profiles enabled. Used for general purpose ADC input. Current source on the NTC is turned off.
0	1	JEITA profiles for 1-cell or 2- to 4-cell batteries enabled. NTC current source is turned on for measurements as shown in Figure 26 (1-cell) or Figure 27 (2- to 4-cell) batteries.
1	0	Profile 1 is enabled and the NTC current source is turned on for measurements as shown in Figure 28.
1	1	Profile 2 is enabled and the NTC current source is turned on for measurements as shown in Figure 29.

The RAA489000 charging profile follows one of the four JEITA profiles shown in Figure 26, 27, 28, and 29 if a thermistor with a 10k at 25°C (typically B = 3435) is used on the NTC pin. The temperature ranges for battery charging are followed if the JEITA charging profile is enabled. There are four automatic profiles, one for single cell batteries and the others for 2-4 cell batteries (cell count is determined by PROG pin). Different temperature ranges can be selected by modifying the resistor network on the NTC pin; however, the steps in the graphs remain the same, although at different temperatures.

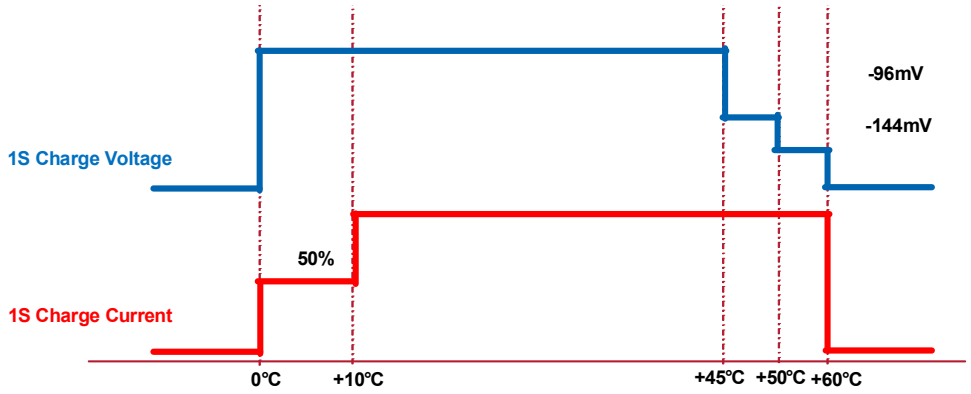


Figure 26. JEITA Profile for 1-Cell Batteries

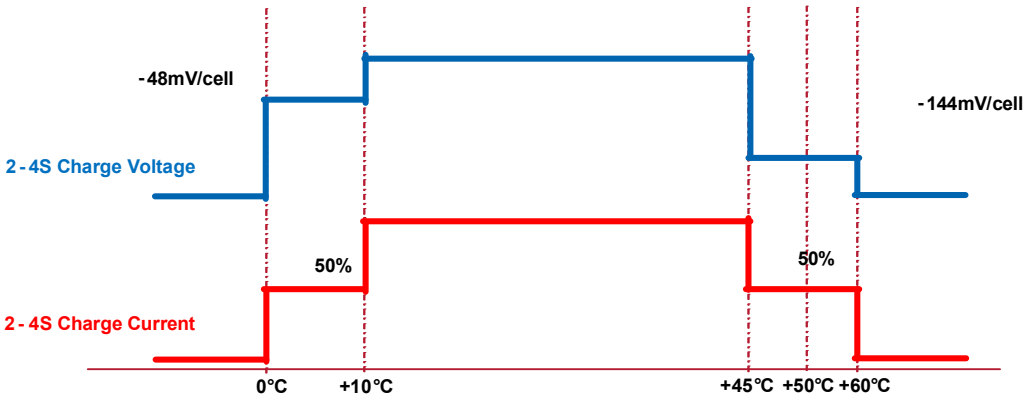


Figure 27. JEITA Profile for 2- to 4-Cell Batteries

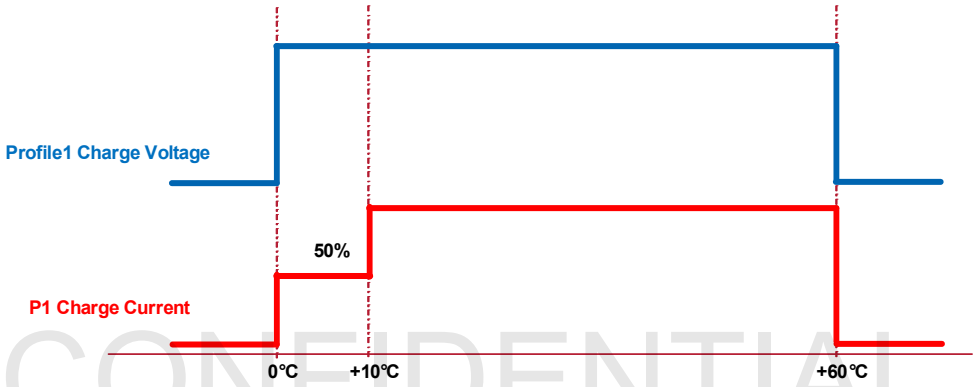


Figure 28. JEITA Profile 1

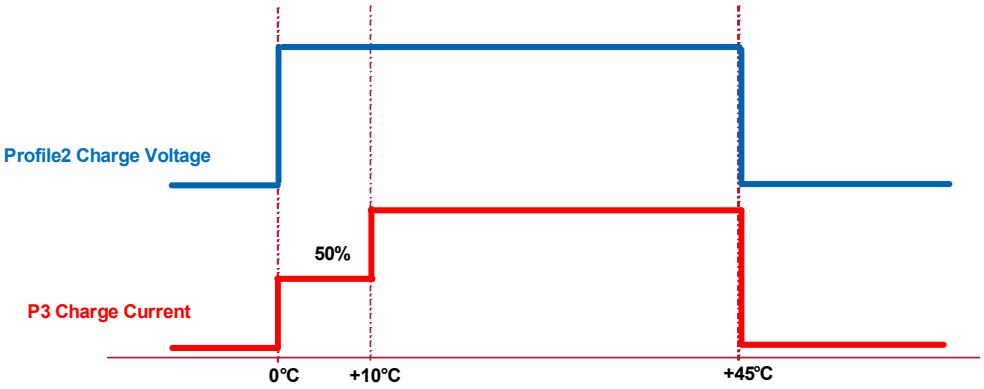


Figure 29. JEITA Profile 2

7.3.8 Battery Learn Mode

The RAA489000 supports Battery Learn mode when operating in NVDC mode. The RAA489000 enters Battery Learn mode when it receives the SMBus Control command.

Use Battery Learn mode to supply the system power from the battery even when the adapter is plugged in, such as during calibration of the battery fuel gauge.

When entering Battery Learn mode the RAA489000 turns on the BGATE FET.

In Battery Learn mode, the RAA489000 turns on BGATE and turns off the buck-boost switcher regardless of whether the adapter is present.

The three ways of exiting Battery Learn mode are:

- Receive the Battery Learn mode exit command through SMBus (Control1 Bit<12> setting)
- Battery voltage is less than the MinSystemVoltage register setting (Control1 Bit<13> setting)
- BATGONE pin voltage goes from logic LOW to HIGH

In all these cases, the RAA489000 resumes switching immediately to supply power to the system bus from the adapter to prevent system voltage collapse.

7.3.9 Battery Only Operation Mode

When VDD is above 3.8V and VBUS is less than 3.8V, the RAA489000 operates in Battery Only mode. During Battery Only mode, the RAA489000 turns on the BGATE to connect the battery to the system. In Battery Only mode, the RAA489000 consumes very low power. The battery discharging current monitor BMON can be turned on during this mode to monitor the battery discharging current.

Turning on the additional functionality increases current consumed.

7.3.10 Battery Ship Mode

Battery Ship mode sets the lowest power state for the IC. Battery Ship mode can only be entered from Battery Only mode. To achieve the lowest power, several analog functions must be disabled; many are disabled by default and do not need to be written, but all are listed for completeness. However, the power level may be customized to suit the system functionality. TCPC is set to dead battery mode. MCU_LDO can be turned off by Control bit to save power but can still wake up when adapter is plugged in.

- Control0 0x39h
  - Bit<10> = 0, BGATE normal operation
- Control1 0x3Ch
  - Bit<6> = 1, force BGATE off
  - Bit<5> = 1, disable AMON/BMON
- Control3 0x4Ch
  - Bit<0> = 0, ADC active only if adapter is plugged in and charging is enabled
- Control4 0x4Eh
  - Bit<12> = 1, disable GP comparator for Battery Only mode
- Control8 0x37h
  - Bit<14> = 1, disable MCU_LDO in battery state
- TCPC registers
  - Set TCPC_SETTING_1 register (0x80h) = 0x0010 (This step can be skipped if it has been set after Power-On Reset)
  - Set ROLE CONTROL register (0x1Ah) bits<1:0> = 10b and bits<3:2> = 10b
  - Set TYPE_C_SETTING_1 register (0xC0h). bit<7> = 0b
  - Set TCPC_SETTING_1 register (0x80h) = 0x0000
  - Set COMMAND register (0x23h) = 0xFF

To exit Battery Ship mode, either plug in an adapter or use the SMBus to change the control bits.

7.3.11 Pass-Through Mode (PTM)

Enable Pass-Through mode with Control register. When the Pass-Through mode control bit is enabled, the REF ramps to the input voltage and the switcher continues switching until the output voltage is in the 300mV window to the input. When the regulating voltage is withing the 300mV window to the input voltage, the latch is set to stop switching. Q1 and Q4 are always on while Q2 and Q3 are always off. The charger enters Pass-Through mode and all protections are still valid. The following methods can be used to exit Pass-Through mode.

- Unprogram Control register. The REF ramps to the DAC and switching resumes
- Enable charging with any non-zero value
- Enable adapter OV triggers
- Any fault is triggered
- Ideal DE mode is enabled or the battery discharge current is higher than 160mA
- The current limit loop turns on for more than 1ms

Before entering Pass-Through mode, it is recommended to:

1. Ensure CV mode operation
2. Enable Voltage Slew Rate Control4<13>=1
3. Change MaxSystemVoltage (0x15) setting close to VBUS as much as possible.

7.3.11.1 Programmable Power Supply (PPS) Sink

Always use the Programmable Power Supply (PPS) sink function along with the Pass Through Mode function. If the PPS sink function is required, enable both PTM (Control0<5>) and PPS Mode (Control0<11>) together. Set the ChargeCurrentLimit (0x14) to the maximum charge current allowed into the battery.

When PPS sink is enabled, the same steps are carried out by the IC as PTM. In addition to these steps, BGATE is turned on.

The following are the exit conditions for PPS sink in addition to all PTM exit conditions:

- When the charge current exceeds the ChargeCurrentLimit (0x14) setting for more than 1ms.
- When battery voltage exceeds MaxsysVoltage + 8*Vos, where Vos = 21mV for 2-cell, 31.5mV for 3-cell and 42mV for 4-cell. See Battery Overvoltage Protection (For PPS Mode exit) and Electrical Specifications.
- When the battery voltage falls below the MinSystemVoltage (0x3E) setting.

When PPS sink mode is exited, the charger may go to the PTM or NVDC operation.

7.3.12 Dynamic Voltage Compensation (DVC)

The RAA489000 can operate in Dynamic Voltage Compensation (DVC) mode. In DVC mode, the battery can be charged through a secondary RAA489000 operating as a Voltage Regulator (VR) maintaining the system voltage to the desired level. The DVC mode is used to fast track and autonomously fine tune the charge current for any high dynamic load variation without any significant involvement from the system controller. The DVC mode reduces the stress on the system controller while allowing the BGATE FET to be operated in either the ON or OFF condition for protection purposes only.

The DVC mode offers an alternative solution for charging batteries in multi-port applications. The Multi-Port USB-C Application Information section describes a traditional multi-port charging application where BGATE, CSOP, CSON, VBAT connections are routed to the second RAA489000 charger for controlling the battery charging process. The routing might be a challenge if the second charger is located far away. The DVC mode provides an alternative solution for these cases to charge the battery through the second RAA489000 without routing all these traces for a traditional dual-port application. This offers more flexibility in routing and selecting charger location.

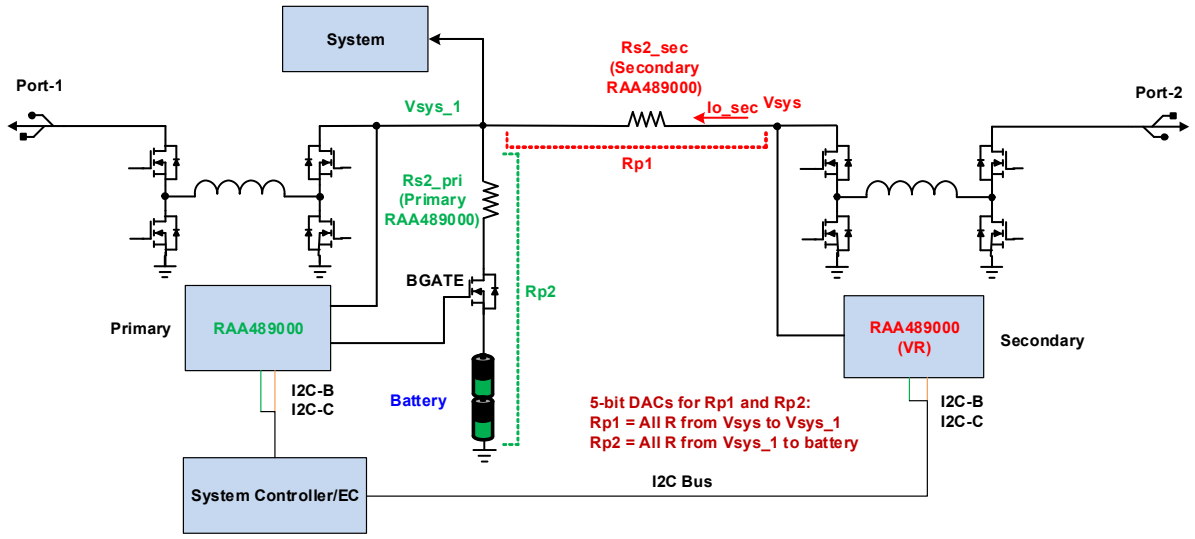


Figure 30. Simplified Application Diagram for Dynamic Voltage Compensation (DVC)

Figure 30 shows a typical application of the RAA489000 working in DVC mode. If the adapter is connected to Port-1, the battery is charged through the primary RAA489000. In this case, regular fast charge or trickle charge method is followed. If the adapter is connected to Port-2, the primary RAA489000 is in the BAT state. The battery is charged through the secondary RAA489000 operating as a VR and system controller initiates DVC operating mode. Depending on the actual measured battery voltage, the system controller enables DVC trickle charge or DVC fast charge.

Steps for enabling DVC trickle charge mode:

1. Set secondary RAA489000 MaxSVsys DAC to MinSVsys DAC + 300mV
2. Disable charge current loop for secondary RAA489000 by Control10<8>
3. Set primary RAA489000 charge current DAC to a value that indicates over charging if reached
4. Set primary RAA489000 MaxSVsys DAC to a value that indicates battery overvoltage if reached
5. Set trickle charge current level for primary RAA489000 by Control2<15:13> (default 128mA)
6. Enable DVC trickle charge by Control10<6> and enable DVC charge mode by Control10<9> for primary RAA489000

The primary RAA489000 moves from BAT state to DVC CHRG state and controls BGATE in linear mode to regulate trickle charge current. When the battery is charged enough, disable the DVC trickle charge by setting Control10<6> bit low and set the secondary RAA489000 MaxSVsys DAC value. The primary RAA489000 exits DVC trickle charge, fully turns ON BGATE and enters DVC fast charge.

Steps for enabling DVC fast charge mode:

1. Set primary RAA489000 charge current DAC to a value that indicates overcharging if reached
2. Set primary RAA489000 MaxSVsys DAC to a value that indicates battery overvoltage if reached
3. Set Rp1 and Rp2 DACs for the secondary RAA489000 according to the calculated values. No DVC is applied if Rp1 DAC is set to all 0.
4. Enable DVC mode for secondary RAA489000 by setting Control10<15>
5. Disable charge current loop for secondary RAA489000 by Control10<8>
6. Set secondary RAA489000 MaxSVsys DAC to a value that gives the desired charge current and also set the charge current DAC to the desired charge current value
7. Enable DVC fast charge mode by Control10<9> for primary RAA489000

The primary RAA489000 moves from BAT state to DVC CHRG state and turns BGATE fully ON to enable fast charge. Battery voltage and battery charge current are monitored for overvoltage and overcurrent protection. If Battery Overvoltage (BATOV) is detected, BGATE is turned OFF after 10µs debounce. If Overcharge Current (CCHOT) is detected, then BGATE is turned OFF after 1ms debounce.

7.3.12.1 DVC Learn Mode

DVC learning mode can be initiated by the system controller when there is an adapter present in Port-2 and the system is in idle or sleep status. During Learn mode, the system load is assumed to be zero or very low. Vsys_1 is the VOUT sensing point voltage for the primary RAA489000, which is closer to the battery voltage and Vsys is the system voltage set by the secondary RAA489000 operating as a VR. The primary RAA489000 reports the voltage at Vsys_1 and the secondary RAA489000 reports the voltage at Vsys and the current through Rs2_sec (Io_sec). The system controller calculates the Rp1 and Rp2 using Equation 1 and Equation 2:

(EQ. 1) $$Rp1 = \frac{(Vsys - Vsys\_1)}{Io\_sec}$$

(EQ. 2) $$Rp2 = \frac{(Vsys\_1 - Vbat)}{Io\_sec}$$

The 5-bit Rp1 and Rp2 DACs for the secondary RAA489000 are set according to the calculated values.

Rp1 is the total resistance from the right-hand side of secondary board sense resistor Rs2_sec to the VSYS_1 node. It should include:

- Resistance of secondary board sense resistor (Rs2_sec)
- Connector/cable resistance
- Secondary board PCB resistance to VSYS_1 node

Rp2 is the total resistance from VSYS_1 node to the battery. It should include:

- Resistance of primary board sense resistor (Rs2_pri)
- $r_{DS(ON)}$ of BGATE FET
- Primary board PCB resistance to the battery
- Battery internal resistance

7.3.13 Hardware-Based Adapter Current Limit

The ACLIM pin voltage set hardware-based adapter current limit provides an extra level of protection in the unlikely event of an SMBus communication failure.

Equation 3 gives the relationship between the ACLIM pin voltage and the hardware-based adapter current limit, where VACLIMHW is the ACLIM pin voltage in volts and IACLIMHW is the hardware-based adapter current limit in amperes.

(EQ. 3) $$I_{ACLIMHW} = \frac{V_{ACLIMHW}}{18 \times Rs1} = \frac{R_{ACLIMHW} \times 5\mu A}{18 \times Rs1}$$

Equation 3 is true for all current sensing resistor configurations.

The RAA489000 uses the lower value of the hardware-set adapter current limit and the SMBus programmed adapter current limit as the actual adapter current limit.

The ACLIM current limit function can be disabled through SMBus Control3 register Bit<5> after ACOK assertion.

7.4 Reverse Modes

7.4.1 USB Power Delivery (PD) Source

The RAA489000 operates in Reverse Buck, Reverse Boost, or Reverse Buck-Boost mode when it is configured as the USB PD source.

The source voltage and current limit levels can be configured through TCPC registers. RAA489000 also provides a configurable OCP/UV threshold for protection when the load exceeds the current limit and pulls down the VBUS.

As a simplified example, RAA489000 can be configured as the USB PD source by TCPM with the following steps:

1. Set TCPC_SETTING_1.TCPC Power Control = 1 so the VBUS is controlled by TCPC.
2. Set VBUS_CURRENT_TARGET for the desired current limit.
3. Issue COMMAND.SourceVbusDefaultVoltage to enable sourcing vSafe5V over VBUS.

7.4.1.1 USB PD Source Voltage Register

The RAA489000 provides a vendor-defined TCPC register VBUS_5V_TARGET(90h) to adjust the VBUS voltage target and compensate USB cable voltage drop, the default is 5.26V. TCPM may configure the target voltage for sourcing nondefault voltage over VBUS through VBUS_NONDEFAULT_TARGET(7Ah) to set the target voltage level of COMMAND.SourceVBUSNondefaultVoltage.

7.4.1.2 USB PD Source Current Register

The RAA489000 provides a vendor-defined TCPC register VBUS_CURRENT_TARGET(92h) to set the target current limit level, the default is 3.2A for R_{S1} = 20mΩ.

7.4.1.3 USB PD Source Over Current Protection Threshold Register

The RAA489000 provides a vendor-defined TCPC register VBUS_OCP_UV_THRESHOLD(94h) to set VBUS over current protection threshold, see Overcurrent Protection (VBUS OCP) for more details.

7.4.2 USB On-The-Go (OTG)

The RAA489000 operates in Reverse Buck, Reverse Boost, or Reverse Buck-Boost mode when the OTG function is enabled with the SMBus command and OTGEN pin and if battery voltage VBAT is higher than 5.2V.

When the RAA489000 receives the command to enable the OTG function, it starts switching after a short delay.

When the OTG output voltage reaches the OTG output voltage set by Register 0x49 Bit<14:3>, OTG power-good OTGPG is internally set.

Before OTG mode starts switching, the CSIN pin voltage first needs to drop below the OTG output overvoltage protection threshold (OTGVDAC + 100mV).

The RAA489000 includes the OTG output undervoltage and overvoltage protection functions. The UVP threshold is the OTG output voltage - 1.2V and the OVP threshold is the OTG output voltage +1.2V. If OTG output is in undervoltage condition for more than 32ms, the charger will go to Battery only mode, wait for 1.3s and then try to restart.

The UVP threshold can be disabled for USB-C Programmable Power Supply (PPS) support.

When OV is detected, the RAA489000 stops switching and deasserts OTGPG. It resumes switching 100µs after the OTG voltage drops below the OTG OV threshold. The OTG Power Good (OTGPG) is asserted when the OTG Mode is enabled and OTGUV and OTGOV signals are not high. The OTGPG function can be selected as an interrupt (see Table 12).

OTG mode only works when TCPC Power Control bit = 0. When the TCPC Power Control bit is set to 1, VBUS (adapter) power is controlled by the TCPC.

7.4.2.1 OTG Voltage Register

The OTG voltage register contains SMBus readable and writable OTG mode output regulation voltage references. The default is 5.004V. This register accepts any voltage command. Renesas does not recommend programming the register higher than 23.4V due to internal overvoltage protection (OVP), but the register does accept the value.

OTG mode can be enabled only if the battery voltage is above 5.2V.

7.4.2.2 OTG Current Register

The OTG current register contains SMBus readable and writable OTG current limits. The default is 512mA. The register accepts any current command, but only the valid register bits are written to the register. The maximum value is clamped at 6112mA when the current is sensed across R_{S1} = 20mΩ.

7.4.3 Programmable Power Supply (PPS)

The RAA489000 supports USB PD Programmable Power Supply (PPS), which allows for small step-wise changes in voltage and current. This feature is an effective way to reduce conversion loss during charging.

RAA489000 supports PPS through either TCPC mode (TCPC_SETTING_1.TCPC Power Control = 1) or OTG mode (TCPC_SETTING_1.TCPC Power Control = 0 and Control1.OTG Function = 1).

7.4.3.1 Programmable Power Supply Voltage

Under TCPC mode, PPS voltage can be configured through TCPC register VBUS_NONDEFAULT_TARGET (7Ah) with 20mV LSB.

Under OTG mode, PPS voltage can be configured through Charger register OTG Voltage (49h) with 10mV LSB.

7.4.3.2 Programmable Power Supply Current Limit

Under TCPC mode, PPS current limit can be configured through TCPC register VBUS_CURRENT_TARGET (92h) with 32mA LSB for R_{S1} = 20mΩ.

Under OTG mode, PPS current limit is configured through Charger register OTG Current (4Ah) with 32mA LSB for R_{S1} = 20mΩ.

7.4.4 Fast Role Swap

The RAA489000 supports USB-C Power Delivery Sink Fast Role Swap (FRS). Sink FRS means the initial Sink rapidly becomes the new Source and start supplying vSafe5V after VBUS has dropped below vSafe5V due to the disconnection of an external power supply.

The Sink FRS process of RAA489000 (TCPC Power Control Bit = 1) can be described as follows:

1. RAA489000 detects the FRS signal and asserts the Sink Fast Role Swap bit in the ALERT_EXTENDED register.
2. RAA489000 disables sinking VBUS.
3. RAA489000 checks VBUS and changes the operation to new Source when:
   a. VBUS falls below vSafe5V(max) if VBUS is above vSafe5V (max) at step 1, or
   b. FRS signal is detected if VBUS is below vSafe5V (max) at step 1.
   c. FRS message process directed from the TCPM.

Alternatively, to support the Sink FRS when TCPC Power Control Bit = 0, enable OTG mode using the external pin, set up the OTG Voltage register for 5V, and when the FRS command is detected, toggle the external pin for OTGEN/CMIN to enable OTG mode. If the adapter voltage is higher than 5V, the RAA489000 remains idle until CSIN is within 100mV of the 5V DAC target.

7.4.5 Reverse Mode Discharge Current Loop

When the charger is in reverse mode of operation (VBUS sourcing, OTG), there is a discharge current limit loop that is set by 2xCharge Current Limit register (0x14). The discharge current limit loop is disabled when charge current (0x14) is zero. When the charge current is a non-zero value, the charger limits the battery discharge current to be less than the Discharge current, which is set by 2xCharge current limit register setting. This function is used to limit inrush current from the battery when the VBUS voltage ramps up or down (in addition to the slew rate function).

7.5 Monitoring

7.5.1 Current Monitor

The RAA489000 provides an adapter current monitor/OTG current monitor or a battery charging current monitor/battery discharging current monitor through the AMON/BMON pin. The AMON output voltage is 18x (CSIP - CSIN) and 18x (CSIN - CSIP) voltage and the BMON output voltage is 18x (CSON - CSOP) and 36x (CSOP - CSON) voltage.

The AMON and BMON functions can be enabled or disabled (in battery only mode) through SMBus Control1 register Bit<5>. AMON or BMON can be selected through SMBus Control1 register Bit<4> and the AMON/BMON direction can be configured through SMBus Control3 register Bit<3>.

7.5.2 PROCHOT#

PROCHOT# is an open-drain output used to support IMVP protocols. On systems that do not need IMVP, this pin can be used as an additional interrupt pin.

In Autonomous Charging mode, the RAA489000 starts to charge the battery with the programmed value (REG0x14h). The PROCHOT# pin behaves as the Autonomous Charging mode indication pin and is pulled down to GND while charging.

7.5.2.1 Setting PROCHOT# Threshold for Adapter Overcurrent Conditions

To set the PROCHOT# assertion threshold for adapter overcurrent conditions, write a 16-bit ACProchot# command to register address 0x47H using the Write-word protocol shown in Figure 25 and the data format shown in Table 2. By using the recommended current sense resistor values, the register's LSB always translates to 128mA of adapter current. The ACProchot# register accepts any current command, but only the valid register bits are written to the register and the maximum value is clamped at 6400mA for R_{s1} = 20mΩ.

After POR, the ACProchot# register is reset to 0x0C00H. The ACProchot# register can be read back to verify its content.

If the adapter current exceeds the ACProchot# register setting, the PROCHOT# signal asserts after the debounce time programmed by the Control2 register Bit<10:9> and latches on for a minimum time programmed by Control2 register Bit<8:6>.

7.5.2.2 Setting PROCHOT# Threshold for Battery Over Discharging Current Conditions

To set the PROCHOT# signal assertion threshold for battery over discharging current conditions, write a 16-bit DCProchot# command to register address 0x48H using the Write-word protocol shown in Figure 25 and the data format shown in Table 2. By using the recommended current sense resistor values, the register's LSB always translates to 256mA of adapter current. The DCProchot# register accepts any current command but only the valid register bits are written to the register and the maximum values is clamped at 12.8A for R_{s2} = 10mΩ.

The DCProchot# register can be read back to verify its content. If the battery discharging current exceeds the DCProchot# register setting, the PROCHOT# signal asserts after the debounce time programmed by the Control2 register Bit<10:9> and latches on for a minimum time programmed by Control2 register Bit<8:6>.

In Battery Only and Low Power modes, the DCProchot# threshold is set by Control0 register Bit<4:3>. In Battery Only mode, the DCProchot# function using the DAC (0x48H) works only when ADC is enabled because the

charger is in READY state (not BAT state) when these two functions are enabled. When the charger is in READY state, DCProchot# works using the 0x48H register. When in BAT state, DCProchot# is set by Control 0<4:3>.

7.5.2.3 Low_VSYS PROCHOT#

Low_VSYS is configured using Control register settings. Eight settings are available and are described in Table 4. For one-cell selection, Low_VSYS is held to 2.4V only.

7.5.2.4 Other PROCHOT# Configuration

Control4 Bits<7:4> (see Table 7) can be used to configure the PROCHOT# to be asserted for the following triggers: OTG Current, BATGONE, ACOK, or General Purpose Comparator.

7.5.2.5 Setting PROCHOT# Debounce Time and Duration Time

Control2 register Bit<10:9> (see Table 5) configures the PROCHOT# signal debounce time before its assertion for ACProchot# and DCProchot#.

The low system (VSYS_LOW) voltage PROCHOT# has a fixed debounce time of 7µs.

Control2 register Bit<8:6> configures the minimum duration of the PROCHOT# signal when asserted for VSYS_LOW, ACPROCHOT#, and DCPROCHOT#.

For the ACOK and BATGONE, Control4 Bits<3:2> (see Table 7) can be used to configure the debounce time before PROCHOT# is asserted.

7.5.2.6 Setting PROCHOT# Clear and Latch Control Bits

Control4 Bit<0> (see Table 7) can be used to configure the PROCHOT# to latch and hold its state, which is useful as an interrupt flag to allow the system to determine the error. If this bit is set, the Control4 Bit<1> (see Table 7) must be used to clear the PROCHOT# that is asserted.

7.5.3 ADC Operation

The Analog to Digital Converter (ADC) is a successive-approximation 8-bit converter. Table 15 identifies the bit locations of the control and available information. The ADC monitors and loops though measuring, battery voltage, current and temperature through NTC, input current, and internal die temperature. The sampling frequency was designed at 400kHz. The ADC is always disabled if V_{DD} 3P8 debounce goes low because values are not accurate below this level. The first number is the sample window time. The second number, polling rate, is how often a reading is updated. Data is always valid to be read as a raw number from the last completed sample and updates once per polling rate.

Example timing windows are shown in Figure 31.

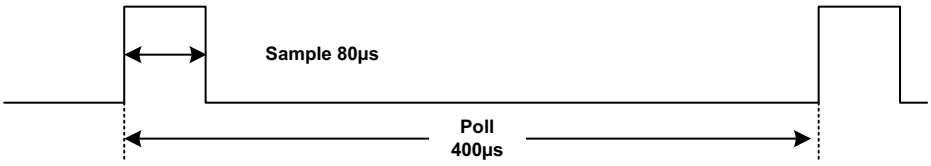


Figure 31. ADC Sample and Polling Time

7.6 Protection

7.6.1 Adapter Overvoltage Protection

If the adapter voltage sensed on the CSIN pin voltage exceeds 23.275V for more than 2µs or the voltage on VBUS exceeds 23.4V, the RAA489000 determines that an adapter overvoltage condition occurred. The RAA489000 stops switching to isolate the adapter from the system, starts to turn off ASGATE and BGATE turns on for the

battery to support the system load. After the OV condition goes away, RAA489000 starts to turn on ASGATE and resumes switching again if there is no other fault.

7.6.2 Battery Protection

The battery is monitored by the ADC by reading register 0x81h and is controlled using a NMOS FET (BFET). The gate (BGATE) of the BFET acts as a source follower in Trickle mode to protect the battery from excessive voltages. The switching modulator controls the charging current using register 0x14h. An NTC input provides thermal protection to protect the battery from charging when outside of normal operating region. For excessive voltage during constant current phase, the system overvoltage protection prevents excessive voltage on the battery.

When no valid adapter voltage is present and only the battery is present, the RAA489000 enters a low power state. In this state the BGATE is turned on, but charge current is not controlled if VSYS is raised above the battery.

7.6.3 Battery Overvoltage Protection (For PPS Mode exit)

Battery Overvoltage condition arises when the voltage on VBAT pin exceeds MaxsystemVoltage register + 8*Vos.

Where Vos = 21mV for 2-cell, 31.5mV for 3-cell and 42mV for 4-cell. Battery overvoltage condition goes away when the battery voltage falls below the above threshold with a 1ms debounce time.

Battery overvoltage protection is only for PPS mode and is one of the exit conditions for PPS Mode.

7.6.4 System Voltage Rail Short Protection

The RAA489000 provides system rail short protection that is checked before switching or enabling the modulator from the READY state to prevent powering on the system rail into a short-circuit. When the VSYS voltage is below 0.6V, the RAA489000 does not allow switching and sources a 10mA current from VDD to charge VSYS. When the VSYS pin is charged above 0.6V, the internal timer starts to count. After 10µs debounce time of the VSYS voltage being above 0.6V, the RAA489000 transitions back to the VSYS state, stops sourcing 10mA current, and allows the RAA489000 to start switching. Any time a transition occurs from the READY state (disable switching with MaxSystemVoltage = 0V) back to the VSYS state, the 10mA turns on again and the CSOP voltage has to be above 0.6V to allow switching again. After switching starts, if VSYS drops below 0.6V again at any time, after 1ms debounce, VSYS not OK fault will be generated (state machine transitions from VSYS state to FAULT state, after the timeout, it transitions back to READY state) and the 10mA current source will be enabled again. Switching can start if VSYS can rise above 0.6V.

7.6.5 System Voltage Overvoltage Protection

The RAA489000 provides system rail overvoltage protection. If the system voltage VSYS is 800mV higher than MaxSystemVoltage register set value, the RAA489000 declares the system overvoltage and stops switching. It resumes switching without debounce when VSYS drops 400mV below the system overvoltage threshold. This signal is valid only when the charger is not in reverse operation.

7.6.6 Way Overcurrent Protection (WOCP)

If the system bus is shorted (either a MOSFET short or an inductor short) the input current could be high. The RAA489000 includes input overcurrent protection to stop switching.

The RAA489000 provides adapter current and battery discharging current Way Overcurrent Protection (WOCP) function against MOSFET shorts, system bus shorts, and inductor shorts. The RAA489000 monitors the CSIP - CSIN voltage and CSON - CSOP voltage and compares them with the WOCP threshold (12A for adapter current and 18A for battery discharge current - see Electrical Specifications for accurate data).

When the WOC comparator is tripped, the RAA489000 increments a timer every 10µs. When the timer reaches 7 counts, the RAA489000 stops switching immediately. The timer is reset every 50ms. After the 1.3s or 150ms debounce time set by Control2 register Bit<11>, it goes through the start-up sequence to retry. If SMBus Timeout is disabled and a fault occurs, the RAA489000 stays in the fault mode until the disable bit is cleared.

The WOCP function can be disabled through Control4 register Bit<9>.

7.6.7 TCPC Protection Features

The protection features included in the TCPC are described here.

7.6.7.1 Overcurrent Protection (VBUS OCP)

The RAA489000 provides VBUS Overcurrent Protection defined by the TCPC. If the current limit loop is active and VBUS voltage falls below the setting value of VBUS_OCP_UV_THRESHOLD register, the RAA489000 disables sourcing VBUS and turns off ASGATE. The overcurrent detection is temporarily disabled during the VBUS voltage transitions.

7.6.7.2 Overvoltage Protection (VBUS OVP)

The RAA489000 provides VBUS Overvoltage Protection defined by the TCPC. If the VBUS voltage exceeds 23.4V, the RAA489000 disables sinking VBUS and turns off ASGATE. The overvoltage detection is temporarily disabled during the VBUS voltage transitions.

7.6.7.3 Vconn Current Protection (VCONN OCP)

The RAA489000 provides VCONN Overcurrent Protection defined by the TCPC. If the VCONN current exceeds 800mA (default), the RAA489000 turns off VCONN.

7.6.7.4 CCx Overvoltage Protection (CCx OVP)

The RAA489000 also provides CCx Overvoltage Protection when the CC line voltage reaches (VCONN_POWER+CCx Overvoltage Rising). The CCx OVP can be configured by Control8<5> and Control8<4>.

7.6.8 Over-Temperature Protection

The RAA489000 stops switching for self-protection when the junction temperature exceeds +140°C.

When the temperature falls below +120°C for 100µs and after the 1.3s or 150ms delay, the RAA489000 starts switching.

Thermal warning is available on the interrupt line, internal die temperature can be monitored using the ADC, and firmware can update parameters to avoid thermal shutdown.

In addition to the internal die temperature, you can use a thermistor for an NTC on the BATGONE pin to control charging in accordance to the JEITA profiles. See section on BATGONE for more details.

7.7 Additional Features

7.7.1 Stand-Alone Comparator

The RAA489000 includes a general purpose stand-alone comparator. The OTGEN/CMIN pin is the comparator input. The internal comparator reference is connected to the inverting input of the comparator and is configured by Control2 register Bit<4> as 1.2V or 2V (Table 5). The comparator output is the ALERT_B pin. The output polarity when the comparator is tripped can be configured through the SMBus register bit.

- When Control2 register Bit<2> = 0 for normal comparator output polarity, if CMIN > Reference, ALERT_B = High; if CMIN < Reference, ALERT_B = Low.
- When Control2 register Bit<2> = 1 for inversed comparator output polarity, if CMIN > Reference, ALERT_B = Low; if CMIN < Reference, ALERT_B = High.

The stand-alone comparator is disabled by default in Battery Only mode. The comparator can be configured to be active in Battery Only mode using Control4 register Bit<12> (Table 7); however, the reference is set to 1.2V. If Disable the comparator to allow the interrupt function that is controlled by Control2 register Bit<3>.

Table 86 shows the OTG mode and stand-alone comparator truth table.

The table below applies only when TCPC Power Control bit = 0 in the TCPC_SETTING_1 register.

Table 86. OTG and Comparator Truth Table

Inputs			Output	Description
Control1 Register 0x3C Table 4	Control2 Register 0x3D Table 5	PIN-36	PIN-30	
Bit<11> OTG Function Enable	Bit<3> Comparator Disable	OTGEN/CMIN	ALERT_B	
0	0	Comparator Input Pin CMIN	Comparator Output Pin ALERT_B	OTG function is disabled. Comparator is enabled.
0	1	X	ALERT_B	ALERT_B Function Both OTG function and comparator are disabled
1	0	Comparator Input Pin CMIN	Comparator Output Pin ALERT_B	Both OTG function and comparator are enabled. OTG function is enabled when V_{BAT} > 5.2V and Control1 register Bit<11> = 1 without OTG power-good pin indication. Information2 register 0x4Dh Bit<7> = 1 indicates OTG mode.
1	1	OTG Enable Input Pin OTGEN	OTG Power-Good Indication Pin ALERT_B	Comparator is disabled and ALERT_B becomes interrupt. OTG function is enabled when V_{BAT} > 5.2.V, OTGEN pin = High, and Control1 register Bit<11> = 1

8. USB-C Port Controller (TCPC) Application Information

8.1 Writing and Reading Registers

This section defines the protocol for the TCPM to read and write the I^2C registers.

8.1.1 Writing Single Byte Registers

When writing to a single byte register, use the following transaction.

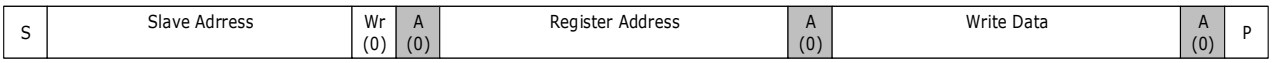


Figure 32. Writing Single Byte Registers

8.1.2 Reading Single Byte Registers

When reading a single byte register, use the following transaction.

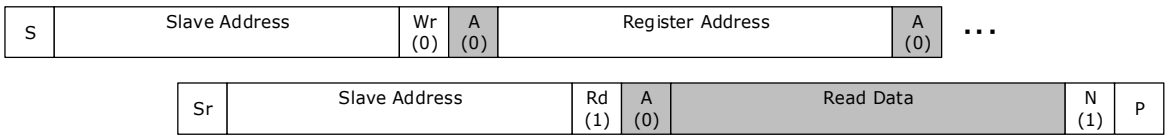


Figure 33. Reading Single Byte Registers

8.1.3 Reading Single Byte Registers without Repeated Start

When reading a single byte register without register address, use the following transaction.

Note: This transaction uses the last configured register address.

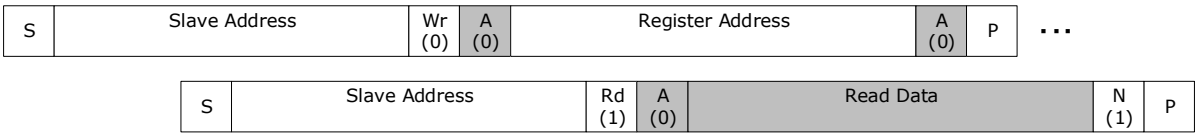


Figure 34. Reading Single Byte Registers without Repeated Start

8.1.4 Writing Two-Byte Registers

When writing to a two-byte register, use the following transaction.

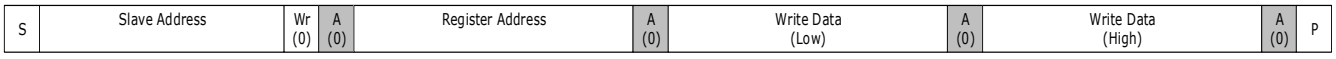


Figure 35. Writing Two-Byte Registers

8.1.5 Reading Two-Byte Registers

When reading a two-byte register, use the following transaction.

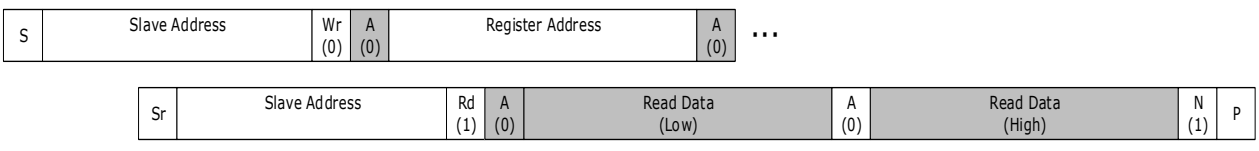


Figure 36. Reading Two-Byte Registers

8.1.6 Reading Two-Byte Registers without Repeated Start

When reading a two-byte register without register address, use the following transaction.

Note: This transaction uses the last configured register address.

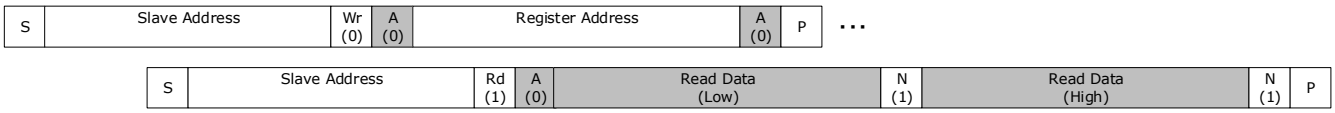


Figure 37. Reading Two-Byte Registers without Repeated Start

8.1.7 Writing the TRANSMIT_BUFFER

When writing to the TRANSMIT_BUFFER register, use the following transaction.

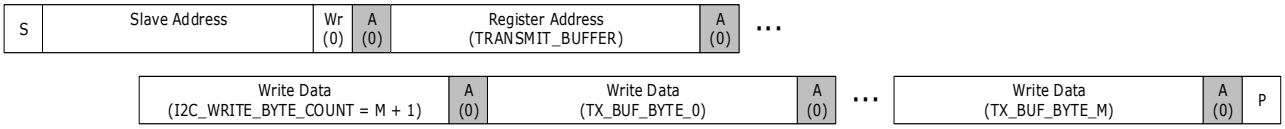


Figure 38. Writing the TRANSMIT_BUFFER

8.1.8 Reading the RECEIVE_BUFFER

When reading the RECEIVE_BUFFER register, use the following transaction.

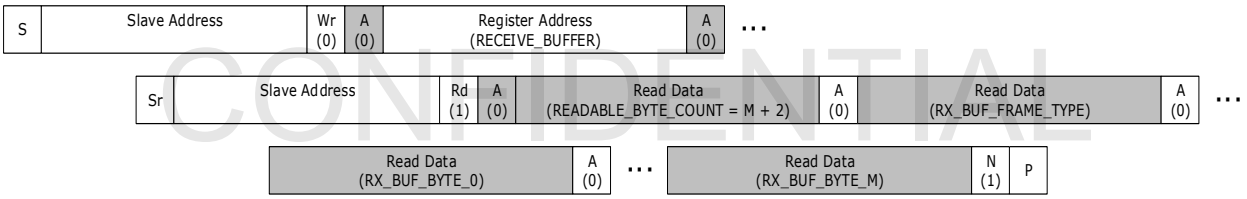


Figure 39. Reading the RECEIVE_BUFFER

8.1.9 Reading the RECEIVE_BUFFER without Repeated Start

When reading the RECEIVE_BUFFER register without register address, use the following transaction.

Note: This transaction uses the last configured register address.

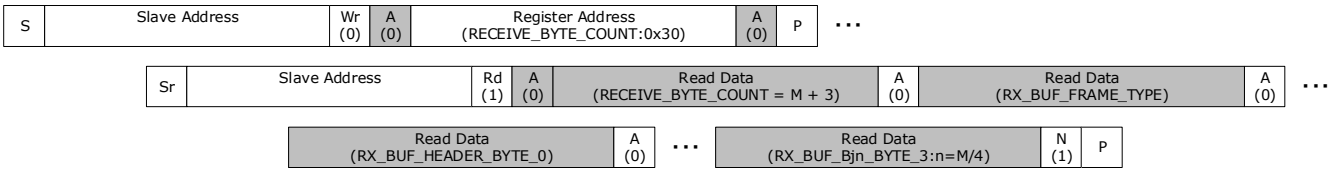


Figure 40. Reading the RECEIVE_BUFFER without Repeated Start

8.1.10 Reading the Alert Response Address

When reading the Alert Response Address register, use the following transaction.

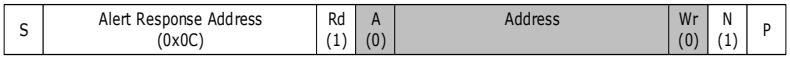


Figure 41. Reading the Alert Response Address

8.1.11 Writing Single Byte Registers using SMBus with PEC

When writing to a single byte register using SMBus with PEC, use the following transaction.

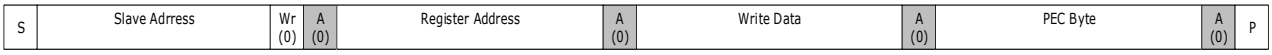


Figure 42. Writing Single Byte Registers using SMBus with PEC

8.1.12 Reading Single Byte Registers using SMBus with PEC

When reading a single byte register using SMBus with PEC, use the following transaction.

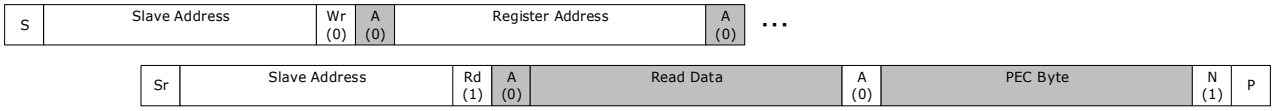


Figure 43. Reading Single Byte Registers using SMBus with PEC

When reading a single byte register without register address using SMBus with PEC, use the following transaction. Note: This transaction uses the last configured register address.

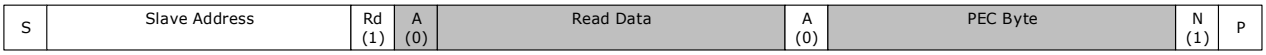


Figure 44. Reading Single Byte Registers without Register Address using SMBus with PEC

8.1.13 Writing Two-Byte Registers using SMBus with PEC

When writing to a two-byte register using SMBus with PEC, use the following transaction.

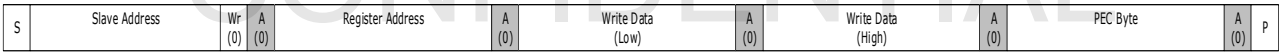


Figure 45. Writing Two-Byte Registers using SMBus with PEC

8.1.14 Reading Two-Byte Registers using SMBus with PEC

When reading a two-byte register using SMBus with PEC, use the following transaction.

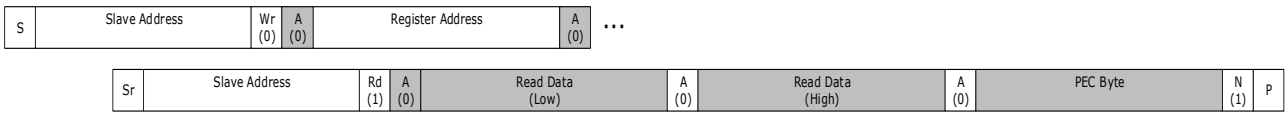


Figure 46. Reading Two-Byte Registers using SMBus with PEC

When reading a two-byte register without register address using SMBus with PEC, use the following transaction.

Note: This transaction uses the last configured register address.

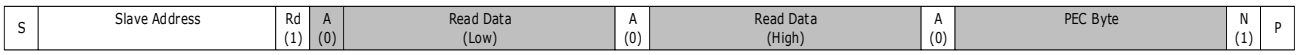


Figure 47. Reading Two-Byte Registers without Register Address using SMBus with PEC

8.1.15 Writing the TRANSMIT_BUFFER using SMBus with PEC

When writing to the TRANSMIT_BUFFER register using SMBus with PEC, use the following transaction.

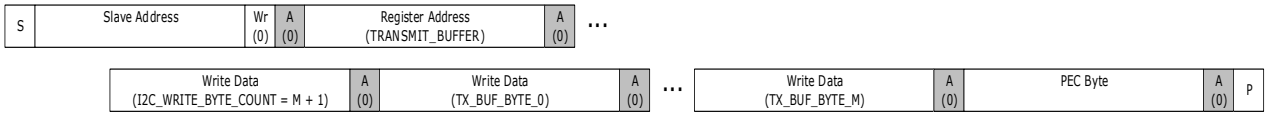


Figure 48. Writing the TRANSMIT_BUFFER using SMBus with PEC

8.1.16 Reading the RECEIVE_BUFFER using SMBus with PEC

When reading the RECEIVE_BUFFER register using SMBus with PEC, use the following transaction.

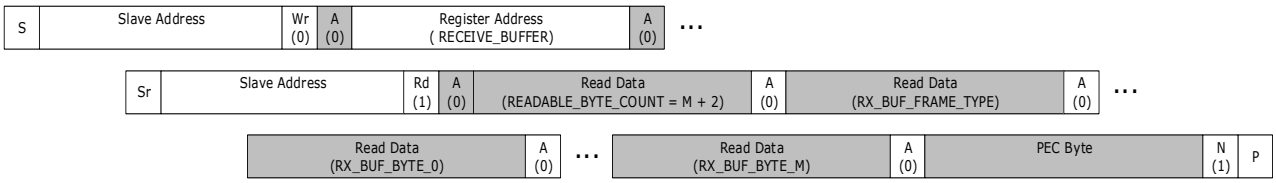


Figure 49. Reading the RECEIVE_BUFFER using SMBus with PEC

When reading the RECEIVE_BUFFER register without register address using SMBus with PEC, use the following transaction.

Note: This transaction uses the last configured register address.

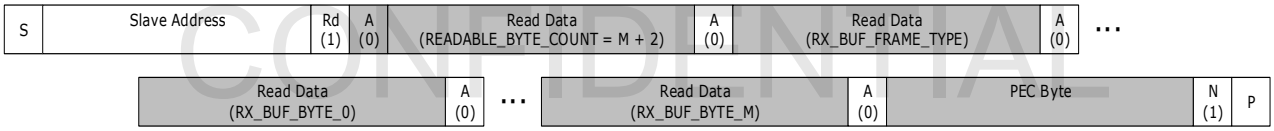


Figure 50. Reading the RECEIVE_BUFFER without Register Address using SMBus with PEC

8.1.17 Reading the Alert Response Address using SMBus with PEC

When reading the Alert Response Address register using SMBus with PEC, use the following transaction.

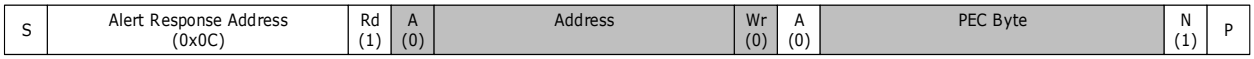


Figure 51. Reading the Alert Response Address using SMBus with PEC

9. Multi-Port USB-C Application Information

When there are many USB-C ports in the system, the customer can multiple RAA489000 as shown below and get additional features like sharing of power. Contact Renesas support for more details on the multi-port application.

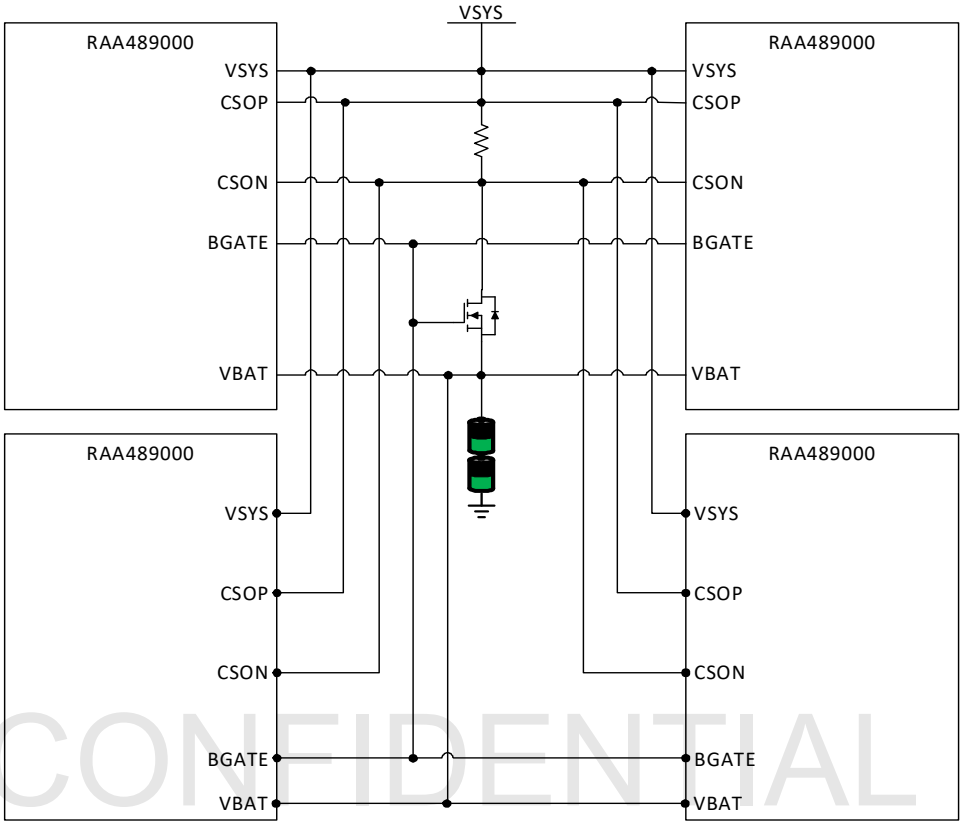


Figure 52. Multi-Port Application

10. Modulator Information

10.1 RAA489000 Buck-Boost Charger Modes of Operation

The RAA489000 buck-boost charger drives an external N-channel MOSFET bridge made up of two transistor pairs as shown in Figure 53. The first pair, Q_1 and Q_2, is a buck arrangement with the transistor center tap connected to an inductor “input” as is the case with a buck converter. The second transistor pair, Q_3 and Q_4, is a boost arrangement with the transistor center tap connected to the same inductor’s “output” as is the case with a boost converter. This arrangement supports bucking from a voltage input higher than the battery and boosting from a voltage input lower than the battery.

In reverse operation, the output sensing point is the CSIN pin.

Table 87. Operation Mode

Mode	Q_1	Q_2	Q_3	Q_4
Buck	Control FET	Sync. FET	OFF	ON
Boost	ON	OFF	Control FET	Sync. FET
Buck-Boost	Control FET	Sync. FET	Control FET	Sync. FET
Pass Through Mode	ON	OFF	OFF	ON
Reverse Buck	ON	OFF	Sync. FET	Control FET
Reverse Boost	Sync. FET	Control FET	OFF	ON
Reverse Buck-Boost	Sync. FET	Control FET	Sync. FET	Control FET

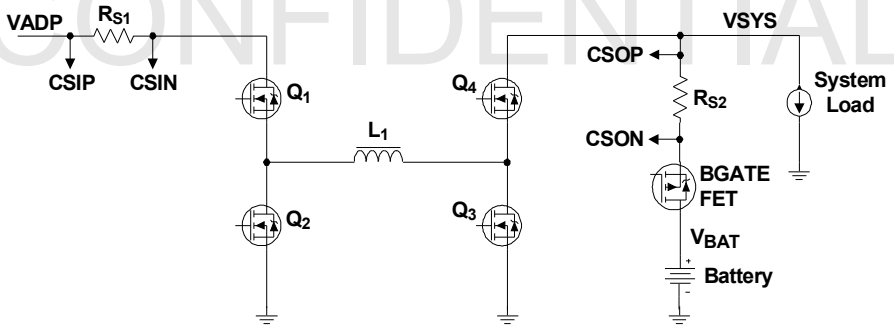


Figure 53. Buck-Boost Charger Topology

The RAA489000 optimizes the Operation mode transition algorithm by considering the input and output voltage ratio and the load condition. When adapter voltage V_{ADP} (CSIN) is rising and is higher than 94% of the system bus voltage VSYS, the RAA489000 transitions from Boost mode to Buck-Boost mode; if V_{ADP} (CSIN) is higher than 112% of VSYS, the RAA489000 is forced to transition from Buck-Boost mode to Buck mode regardless of other conditions. At heavier load, the mode transition point changes accordingly to accommodate the duty cycle change due to the power loss on the charger circuit.

When the adapter voltage V_{ADP} (CSIN) is falling and is lower than 106% of the system bus voltage VSYS, the RAA489000 transitions from Buck mode to Buck-Boost mode; if V_{ADP} (CSIN) is lower than 92% of VSYS, the RAA489000 transitions from Buck-Boost mode to Boost mode.

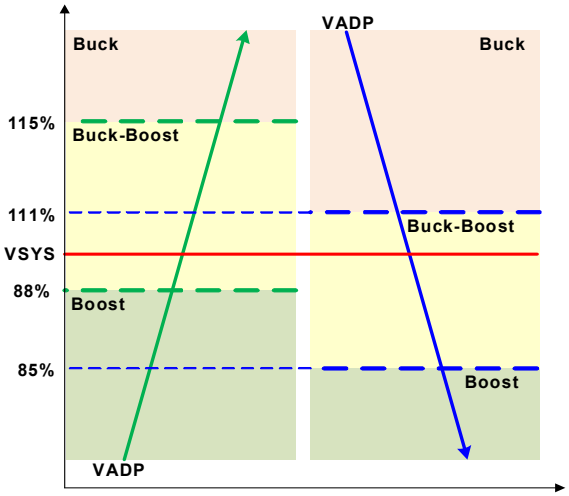


Figure 54. Operation Mode

When the OTG function is enabled with the SMBus command and OTGEN pin and if battery voltage V_{BAT} is higher than 5.2V, the RAA489000 operates in OTG mode. Fast role swap is similar to OTG but uses shorter filters to allow a very quick response to hold up the input when the adapter is detected as unplugged.

10.2 Modulator Control Loops

The four main control loops for the modulator are shown in Figure 55. Each loop has a DAC register to provide settings as needed for each system.

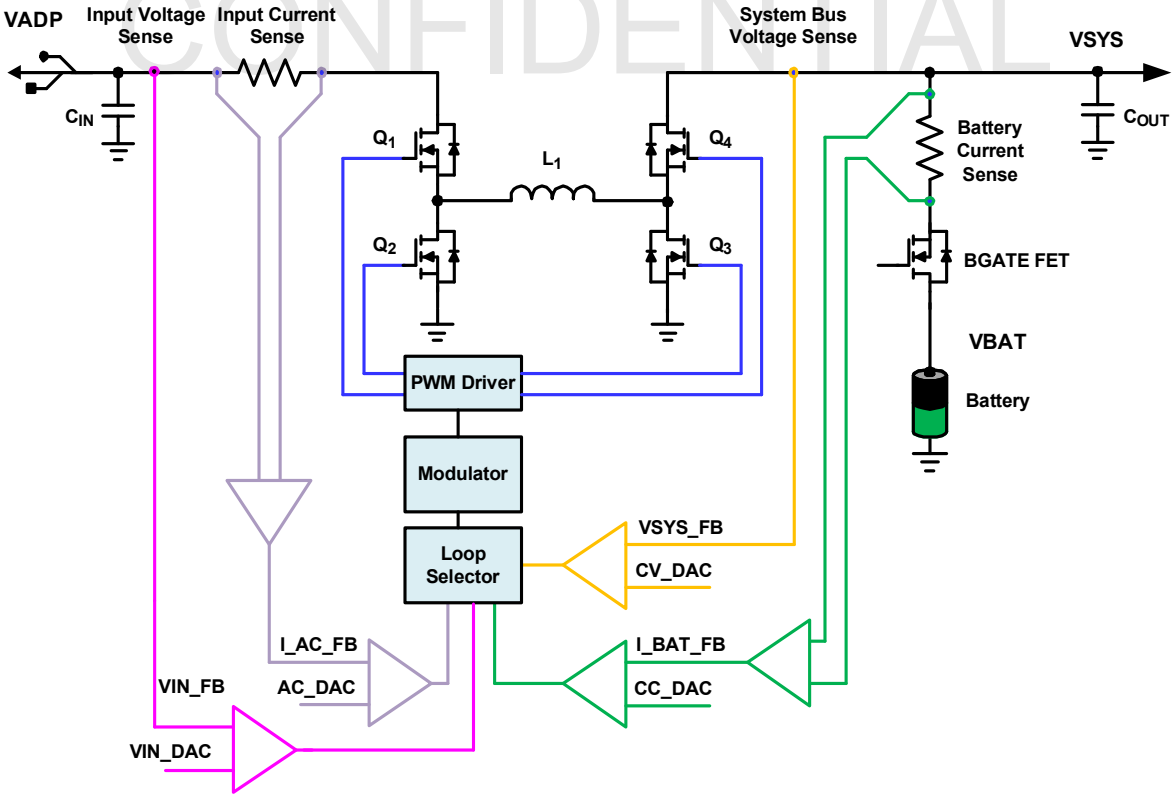


Figure 55. Charger Control Loops

10.2.1 Adapter Current Loop and Current Limit 1 and 2 and Two Level Current Limit

To set the adapter current limit, write a 16-bit AdapterCurrentLimit1 command to register address 0x3FH and/or AdapterCurrentLimit2 command to register address 0x3BH using the Write-word protocol shown in Figure 25 for a 20mΩ R_{s1}. For the DAC summary of values, see Table 2.

The RAA489000 limits the adapter current by limiting the CSIP - CSIN voltage. By using the recommended current sense resistor values, the register's LSB always translates to 4mA of adapter current. Any adapter current limit command is accepted, but only the valid register bits are written to the AdapterCurrentLimit1 and AdapterCurrentLimit2 registers, and the maximum value is clamped.

After adapter POR, the AdapterCurrentLimit1 register is reset to the value programmed through the PROG pin resistor. The AdapterCurrentLimit2 register is set to its default value of 1.5A or keeps the value that is written to it previously if the battery is present first. The AdapterCurrentLimit1 and AdapterCurrentLimit2 registers can be read back to verify their content. The two level adapter current limit is disabled by default.

The AdapterCurrentLimit2 register has the same specification as the AdapterCurrentLimit1 register.

The two-level adapter current limit function can be enabled and disabled through SMBus Control2 register Bit<12>. The t1 and t2 settings are configured by the Control7 register (Table 8). When the two-level adapter current limit function is disabled, only the AdapterCurrentLimit1 value is used as the adapter current limit and AdapterCurrentLimit2 value is ignored.

In a real system, a Turbo event usually does not last very long. It is often no longer than milliseconds, a time during which the adapter can supply current higher than its DC rating. The RAA489000 employs a two-level adapter current limit to fully take advantage of adapter's surge capability and minimize the power drawn from the battery.

Figure 56 shows the two SMBus programmable adapter current limit levels, AdapterCurrentLimit1 and AdapterCurrentLimit2, as well as the durations t1 and t2. The two-level adapter current limit function is initiated when the adapter current is fewer than 100mA lower than the AdapterCurrentLimit1 register setting. The adapter starts at AdapterCurrentLimit2 for t2 duration and changes to AdapterCurrentLimit1 for t1 duration before repeating the pattern. The parameters can set the adapter current limit with an envelope that allows the adapter to temporarily output surge current without requiring the charger to enter Turbo mode. This operation maximizes battery life.

The AdapterCurrentLimit1 register value can be higher or lower than AdapterCurrentLimit2 value.

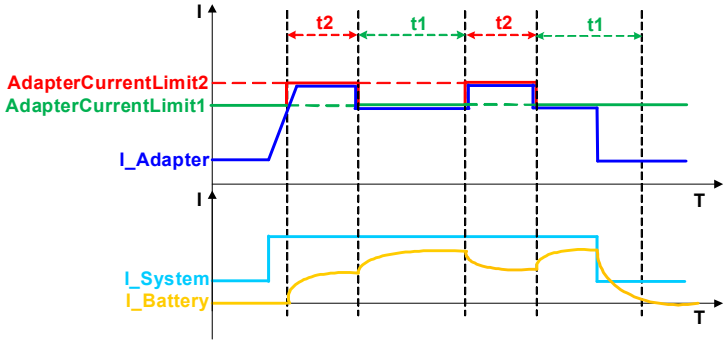


Figure 56. Two-Level Adapter Current Limit

10.2.1.1 USB-PD On-the-Go Output Current

The OTG output current regulation register DAC (Table 2) contains the SMBus readable and writable current that the current sense loop tries to regulate. This loop reuses the input current sense amplifier. If USB-PD Programmable Power Supply is required, this is the current limit loop. **Note**: The OTG_UV needs to be disabled (see CTRL0 Bit<0> in Table 3).

This register accepts any current command, but only the valid register bits are written to the register and the maximum value is clamped.

10.2.2 Input Voltage Regulation Loop

10.2.2.1 Adapter Support Voltage

The input voltage regulation register DAC (Table 2) contains the SMBus readable and writable input voltage limit at which the input voltage loop tries to regulate when the input voltage is dropping. When the ADP is browning out or weak, the input voltage can droop and the input voltage loop tries to regulate to this setting by reducing battery charging current and system power to try to hold up the input voltage. The system voltage may start to droop if the input power is not high enough to support the system.

This register accepts any current command, but only the valid register bits are written to the register and the maximum value is clamped.

10.2.2.2 USB-PD On-the-Go Output Voltage

The OTG output voltage regulation register DAC (Table 2) contains the SMBus readable and writable voltage that the voltage loop tries to regulate. The loop reuses the input voltage sense amp.

This register accepts any current command, but only the valid register bits are written to the register and the maximum value is clamped.

10.2.3 System Voltage Regulation Loop

The system voltage regulation loop works for two different voltage settings: MaxSystemVoltage and MinSystemVoltage.

If the battery is absent, or if a battery is present but BGATE is turned off or not charging, the system voltage is regulated to the same setting as the DAC if Control0 register Bit<1> is a 0. However, when Control0 register Bit<1> is a 1, the system voltage is regulated to the DAC plus an offset of 384mV (Table 3).The additional offset is useful to avoid discharging a full battery in the VSYS state when there is a system load transient.

To set the maximum charging voltage or the system regulating voltage, write a 16-bit MaxSystemVoltage command to register address 0x15H using the Write-word protocol shown in Figure 25 and the data format shown in Table 2. A 0V command causes the RAA489000 to stop switching and enter the READY state.

The RAA489000 supports trickle charging to an overly discharged battery. It can activate the trickle charging function when the battery voltage is lower than the MinSystemVoltage setting. The VBAT pin is the battery voltage sense point for Trickle Charge mode. While trickle charging the battery, system regulation voltage is the DAC setting plus 384mV.

To enable Trickle Charging, set the MinsystemVoltage register to a non-zero value higher than battery voltage. To disable trickle charging, set the MinsystemVoltage register to 0V. See Table 88 for trickle charging control logic.

The CSOP pin senses the system voltage for MaxSystemVoltage and MinSystemVoltage during trickle charging and controls the VSYS operating voltage.

10.2.4 Charging Current Loop

The charging current loop uses the charge current DAC (Table 2) to set the fast charging current limit.

In Trickle Charging mode, the RAA489000 regulates the MinSystemVoltage through the buck-boost switcher. Another independent control loop controls the BGATE FET so that the trickle charge current is maintained at the current set in the Trickle Charging Current register Control2<15:13>.

To set the charge current limit, write a 16-bit ChargeCurrentLimit command to register address 0x14H (Table 2) using the Write-word protocol shown in Figure 25.

The RAA489000 limits the charging current by limiting the CSOP - CSON voltage, so reducing the current sense resistor value doubles the current being regulated. By using the recommended current sense resistor values

R_{s1} = 20mΩ and R_{s2} = 10mΩ, the register's LSB always translates to 4mA of charging current. The ChargeCurrentLimit register accepts any charging current command, but only the valid register bits are written to the register.

10.3 Buck Boost Configurable Charger

The RAA489000 is a Buck-Boost battery charger. RAA489000 operates in NVDC mode by default.

See the RAA489000 device page for firmware documentation.

10.3.1 NVDC Charger

For NVDC mode configuration, the inductor supports the full system power and the power for charging the battery. The inductor typically needs to be larger sized because it supports both charging and system.

The RAA489000 automatically selects the adapter and/or the battery as the source for system power. The BGATE pin drives an N-channel MOSFET (NFET) gate that connects or disconnects the battery from the system and the switcher.

10.3.1.1 Normal Charging

For NVDC mode configuration, the charging current is selected for the charge rate into the battery. However, the input current limit should be set for the total system plus battery charging current.

If VDD is higher than 3.8V, the RAA489000 enters Forward Buck, Forward Boost, or Forward Buck-Boost mode depending on the adapter and system voltage VSYS duty cycle ratio. The system bus voltage is regulated at the voltage set on the MaxSystemVoltage register. If the charge current register is programmed (non-zero), the RAA489000 charges the battery either in Trickle Charging mode or Fast Charging mode, as long as BATGONE is low.

10.3.1.2 Turbo Support

In the NVDC charger configuration and Turbo mode (also known as Ideal Diode Mode (IDM)), the RAA489000 turns on the BGATE FET to limit the adapter current at the adapter current limit set point while the battery supplies the rest of the power required by the system. To turn on BGATE in Turbo mode, the CSON pin voltage needs to be 175mV lower than the VBAT pin voltage. If the RAA489000 detects 160mA charging current or if the battery discharging current is less than 80mA for 40ms, the RAA489000 turns off BGATE to exit Turbo mode. See Table 88 for BGATE operation.

In most systems, a Turbo event usually does not last very long. It is often no longer than milliseconds, a time during which the adapter can supply current higher than its DC rating. The RAA489000 employs a two-level adapter current limit to take full advantage of adapter's surge capability and minimize the power drawn from the battery.

Table 88. NVDC Charger Behavior Truth Table

Turbo - BGATE Force Off Control Bit	Charging Enabled CC ≠ 0; VSYSMIN ≠ 0	BGATE On/Off	
0 = Enable 1 = Disable	0 = Disabled Charging 1 = Enabled Charging	System Load Not in Turbo Mode Range	System Load in Turbo Mode Range
0	0	Off	On
0	1	ON for fast charge; trickle charge enabled	On
1	0	Off	Off
1	1	ON for fast charge; trickle charge enabled	On

10.4 R3 Modulator

The RAA489000 uses the Renesas Robust Ripple Regulator (R3) modulation scheme. The R3 modulator combines the best features of fixed frequency PWM and hysteretic PWM while eliminating many of their shortcomings. Figure 57 conceptually shows the R3 modulator circuit and Figure 58 shows the operation principles in steady state.

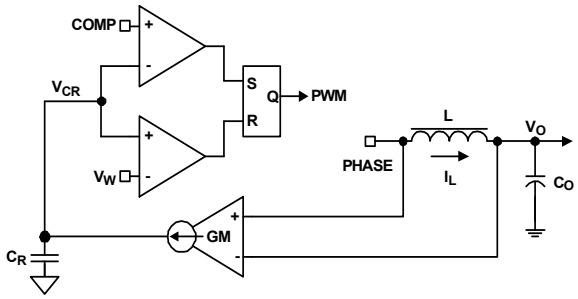


Figure 57. R3 Modulator

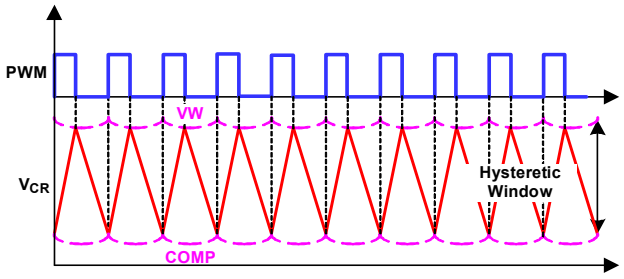


Figure 58. R3 Modulator Operation Principles in Steady State

A fixed voltage window (VW window) exists between VW and COMP. The modulator charges the ripple capacitor C_R with a current source equal to g_m (V_{IN}-V_O) during PWM on-time and discharges the ripple capacitor C_R with a current source equal to $g_m V_O$ during PWM off-time where g_m is a gain factor. The C_r voltage V_{CR} therefore emulates the inductor current waveform. The modulator turns off the PWM pulse when V_{CR} reaches VW and turns on the PWM pulse when it reaches COMP.

Because the modulator works with V_{cr}, which is a large amplitude and noise free synthesized signal, it achieves lower phase jitter than conventional hysteretic mode modulators.

Figure 59 shows the operation principles during dynamic response. The COMP voltage rises during dynamic response, temporarily turning on PWM pulses earlier and more frequently, which allows for higher control loop bandwidth than conventional fixed frequency PWM modulators at the same steady state switching frequency.

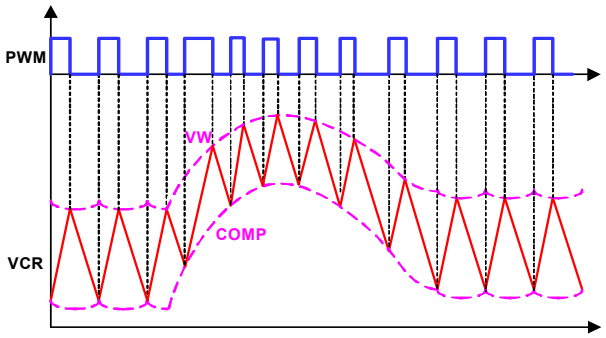


Figure 59. R3 Modulator Operation Principles in Dynamic Response

10.4.1 DE (Diode Emulation) Operation

In Diode Emulation (DE) mode, the RAA489000 employs a phase comparator to monitor the PHASE node voltage during the low-side switching FET on-time to detect the inductor current zero crossing. The phase comparator needs a minimum on-time of the low-side switching FET for it to recognize inductor current zero crossing. If the low-side switching FET on-time is too short for the phase comparator to successfully recognize the inductor zero crossing, the RAA489000 might lose diode emulation ability. To prevent diode emulation loss, the RAA489000 employs a minimum low-side switching FET on-time. When the intended low-side switching FET on-time is

shorter than the minimum value, the RAA489000 stretches the switching period to keep the low-side switching FET on-time at the minimum value, which causes the CCM switching frequency to drop below the set point.

The R3 modulator can operate in DE mode to increase light-load efficiency. In DE mode, the low-side MOSFET conducts when the current is flowing from source-to-drain and does not allow reverse current, emulating a diode. As shown in Figure 60, when LGATE is on, the low-side MOSFET carries current, creating negative voltage on the phase node due to the voltage drop across the ON-resistance. The IC monitors the current by monitoring the phase node voltage. It turns off LGATE when the phase node voltage reaches zero to prevent the inductor current from reversing the direction and creating unnecessary power loss.

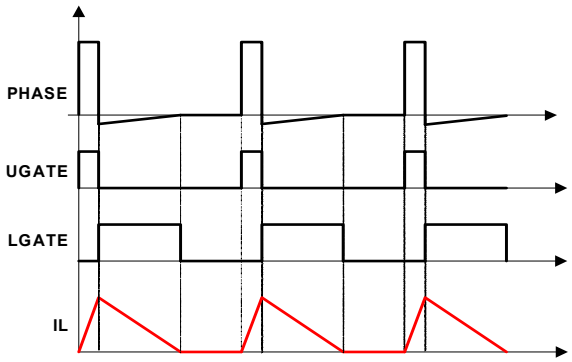


Figure 60. Diode Emulation

If the load current is light enough, as Figure 60 shows, the inductor current reaches and stays at zero before the next phase node pulse and the regulator is in Discontinuous Conduction Mode (DCM). If the load current is heavy enough, the inductor current never reaches 0A and the regulator is in Continuous Conduction Mode (CCM) although the controller is in DE mode.

Figure 61 shows the operation principle of DE mode at light load. The load gets incrementally lighter in the three cases from top to bottom. The PWM on-time is determined by the VW window size, and therefore is the same, making the inductor current triangle the same in the three cases. The R3 modulator clamps the ripple capacitor voltage V_{CR} in DE mode to make it mimic the inductor current. The COMP voltage takes longer to reach V_{CR}, naturally stretching the switching period. The inductor current triangles move farther apart from each other, so that the inductor current average value is equal to the load current. The reduced switching frequency helps increase light-load efficiency.

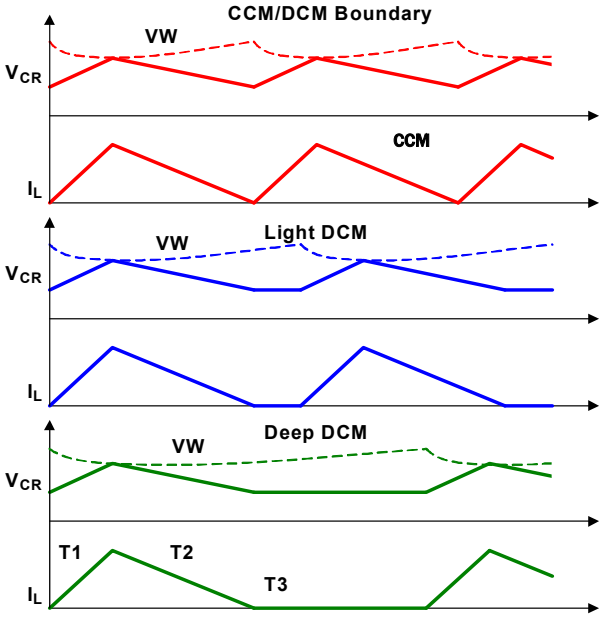


Figure 61. Period Stretching

11. Design Guide

This design guide provides a high-level explanation of the steps necessary to design a single-phase power converter. It is assumed that the reader is familiar with many of the basic skills and techniques referenced in the following section. Complete reference designs that include schematics, bill of materials, and example board layouts are provided.

11.1 Selecting the Sense Resistors

Sense resistors are the easiest and most flexible method of monitoring/controlling current in the battery charge or discharge path or the adapter input/output current. Most of the electrical specifications in this datasheet use R_{s1} = 20mΩ and R_{s2} = 10mΩ. However, any value can be selected because the voltage across the CSIN/CSIP and CSON/CSOP pins are used for the control loops.

A sense resistor can introduce significant voltage drop and power loss to the load. In an application with high current requirements, the sense resistors require the use of a low value sense resistor or a parallel combination of multiple sense resistors to support the higher power.

Appropriate scaling of the current values should be based on the voltage across the CSIN/CSIP (for adapter/VBUS current) and CSON/CSOP (for battery/output current).

For example, if DAC is set for 2A at R = 20mΩ, V_{sx} = 40mV; with R = 10mΩ, which is half the previous value, the DAC setting is doubled to 4A to preserve the V_{sx} = 40mV.

11.1.1 Adapter Sense Resistor

The adapter sense resistor (R_{s1}) controls the current being pulled from an adapter when in forward mode and senses the maximum current for ACProchot#. In reverse mode, the sense resistor regulates the output current for reverse operation.

11.1.2 Battery Sense Resistor

The battery sense resistor (R_{s2}) controls the battery charging current when in forward mode. In reverse mode, the sense resistor senses the battery discharging current for DCProchot#.

11.2 Selecting the LC Output Filter

The duty cycle of an ideal buck converter in CCM is a function of the input and the output voltage. This relationship is written by Equation 4:

(EQ. 4) $$D = \frac{V_{OUT}}{V_{IN}}$$

The output inductor peak-to-peak ripple current is written by Equation 5:

(EQ. 5) $$I_{P-P} = \frac{V_{OUT} \cdot (1 - D)}{f_{SW} \cdot L}$$

A typical step-down DC/DC converter has an I_{P-P} of 20% to 40% of the maximum DC output load current for a practical design. The value of I_{P-P} is selected based on several criteria such as MOSFET switching loss, inductor core loss, and the resistive loss of the inductor winding.

The DC copper loss of the inductor can be estimated by Equation 6 where I_{LOAD} is the converter output DC current.

(EQ. 6) $$P_{COPPER} = I_{LOAD}^{2} \cdot DCR$$

The copper loss can be significant, so select DCR carefully. Also consider the inductor's saturation characteristics at elevated temperatures. A saturated inductor can destroy circuit components.

A DC/DC buck regulator must have output capacitance C_O into which ripple current I_{P-P} can flow. Current I_{P-P} develops a corresponding ripple voltage V_{P-P} across C_O, which is the sum of the voltage drop across the capacitor ESR and of the voltage change stemming from charge moved in and out of the capacitor. These two voltages are written by Equation 7 and 8:

(EQ. 7) $$\Delta V_{ESR} = I_{P-P} \cdot ESR$$

(EQ. 8) $$\Delta V_C = \frac{I_{P-P}}{8 \cdot C_O \cdot f_{SW}}$$

If the output of the converter has to support a load with high pulsating current, several capacitors need to be paralleled to reduce the total ESR until the required V_{P-P} is achieved. The inductance of the capacitor can cause a brief voltage dip if the load transient has an extremely high slew rate. Low inductance capacitors should be considered in this scenario. A capacitor dissipates heat as a function of RMS current and frequency. Be sure that I_{P-P} is shared by a sufficient quantity of paralleled capacitors so that they operate below the maximum rated RMS current at f_{SW}. Take into account that the rated value of a capacitor can fade as much as 50% as the DC voltage across it increases.

11.3 Adapter Input Filter

The adapter cable parasitic inductance and capacitance can cause some voltage ringing or an overshoot spike at the adapter connector node when the adapter is hot plugged in. The voltage spike can damage the RAA489000 pins connecting to the adapter connector node. One low cost solution is to add an R-C snubber circuit at the adapter connector node to clamp the voltage spike as shown in Figure 62. A practical value of the R-C snubber is 2.2Ω to 2.2µF while the appropriate values and power rating should be carefully characterized based on the actual design. It is not recommended to add a pure capacitor at the adapter connector node, which can cause an even bigger voltage spike because of the adapter cable or the adapter current path parasitic inductance.

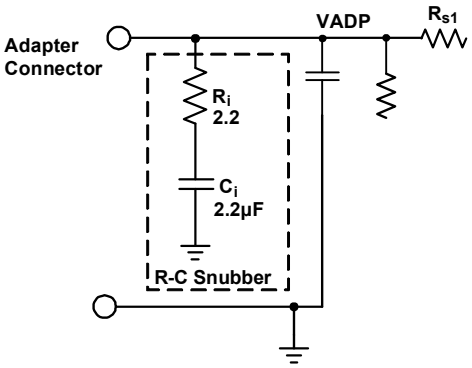


Figure 62. Adapter Input R-C Snubber Circuit

11.4 Selecting the Input Capacitor

The important parameters for the input capacitance are the voltage rating and the RMS current rating. For reliable operation, select capacitors with voltage and current ratings above the maximum input voltage and that are capable of supplying the RMS current required by the switching circuit. Their voltage rating should be at least 1.25 times greater than the maximum input voltage, while a voltage rating of 1.5 times is a preferred rating. Figure 63 is a graph of the input capacitor RMS ripple current, normalized relative to output load current, as a function of duty cycle and is adjusted for converter efficiency.

The normalized RMS ripple current calculation is written as Equation 9:

(EQ. 9) $$I_{C_{IN}(RMS,NORMALIZED)} = \frac{I_{MAX} \cdot \sqrt{D \cdot (1-D) + \frac{D \cdot k^2}{12}}}{I_{MAX}}$$

where:

- I_{MAX} is the maximum continuous I_{LOAD} of the converter
- k is a multiplier (0 to 1) corresponding to the inductor peak-to peak ripple amplitude expressed as a ratio of I_{MAX} (0 to 1)
- D is the duty cycle that is adjusted to take into account the efficiency of the converter, which is written as Equation 10:

(EQ. 10) $$D = \frac{V_{OUT}}{V_{IN} \cdot EFF}$$

In addition to the capacitance, some low ESL ceramic capacitance is recommended to decouple between the drain of the high-side MOSFET and the source of the low-side MOSFET.

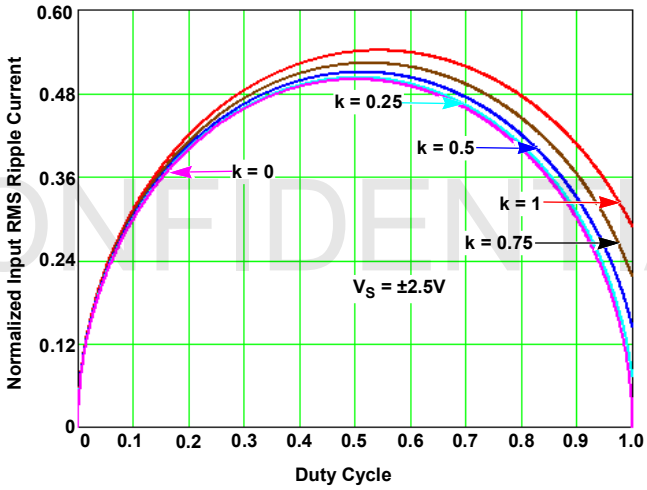


Figure 63. Normalized RMS Input Current at EFF = 1

11.5 Selecting the Switching Power MOSFET

11.5.1 Switching Power MOSFET Gate Capacitance

The RAA489000 includes an internal 5V LDO output at the VDD pin that can provide the switching MOSFET gate driver power through the VDDP pin with an R-C filter. The 5V LDO output overcurrent protection threshold is 115mA (see Electrical Specifications for accurate data), nominal. When selecting the switching power MOSFET, carefully consider the MOSFET gate capacitance to avoid overloading the 5V LDO, especially in Buck-Boost mode when four MOSFETs are switching at the same time. For one MOSFET, the gate drive current can be estimated by Equation 11:

(EQ. 11) $$I_{driver} = Q_g \bullet f_{SW}$$

where:

- Q_g is the total gate charge, which can be found in the MOSFET datasheet

- f_{SW} is switching frequency

11.5.2 Switching Power MOSFET Power

Typically, a MOSFET cannot tolerate even brief excursions beyond its maximum drain-to-source voltage rating. The MOSFETs used in the power stage of the converter should have a maximum VDS rating that exceeds the sum of the upper voltage tolerance of the input power source and the voltage spike that occurs when the MOSFET switches off.

Several readily available power MOSFETs are optimized for DC/DC converter applications. The preferred High-Side (HS) MOSFET emphasizes low gate charge so that the device spends the least amount of time dissipating power in the linear region and does not exceed the VDDP current rating. Unlike the Low-Side (LS) MOSFET, which has the drain-to-source voltage clamped by its body diode during turn off, the HS MOSFET turns off with a VDS of approximately VIN - VOUT, plus the spike across it. The preferred LS MOSFET emphasizes low $r_{DS(ON)}$ when fully saturated to minimize conduction loss. Note that this is an optimal configuration of MOSFET selection for low duty cycle applications (D < 50%). For higher output, low input voltage solutions, a more balanced MOSFET selection for HS and LS devices may be warranted.

For the LS MOSFET, the power loss can be assumed to be conductive only and is written as Equation 12:

(EQ. 12) $$P_{CON\_LS} \approx I_{LOAD}^{2} \cdot r_{DS(ON)\_LS} \cdot (1 - D)$$

For the HS MOSFET, the conduction loss is written by Equation 13:

(EQ. 13) $$P_{CON\_HS} = I_{LOAD}^{2} \cdot r_{DS(ON)\_HS} \cdot D$$

For the HS MOSFET, the switching loss is written as Equation 14:

(EQ. 14) $$P_{SW\_HS} = \frac{V_{IN} \cdot I_{VALLEY} \cdot t_{SWON} \cdot f_{SW}}{2} + \frac{V_{IN} \cdot I_{PEAK} \cdot t_{SWOFF} \cdot f_{SW}}{2}$$

where:

- I_{VALLEY} is the difference of the DC component of the inductor current minus 1/2 of the inductor ripple current
- I_{PEAK} is the sum of the DC component of the inductor current plus 1/2 of the inductor ripple current
- $t_{SW(ON)}$ is the time required to drive the device into saturation
- $t_{SW(OFF)}$ is the time required to drive the device into cut-off
- Renesas recommends using a 4.7µF (10V) VDD/VDDP capacitor, which has an effective capacitance higher than 0.4µF at 5V and x1.6 effective capacitance at the BOOT pin at 5V.

11.6 Selecting the Bootstrap Capacitor

The selection of the bootstrap capacitor is written by Equation 15:

(EQ. 15) $$C_{BOOT} = \frac{Q_g}{\Delta V_{BOOT}}$$

where:

- Q_g is the total gate charge required to turn on the high-side MOSFET
- ΔV_{BOOT} is the maximum allowed voltage decay across the boot capacitor each time the high-side MOSFET is switched on.

For example, suppose the high-side MOSFET has a total gate charge Q_g, of 25nC at V_{GS} = 5V and a ΔV_{BOOT} of 200mV. The calculated bootstrap capacitance is 0.125µF; for a comfortable margin, select a capacitor that is double the calculated capacitance. In this example, 0.22µF suffices. Use an X7R or X5R ceramic capacitor.

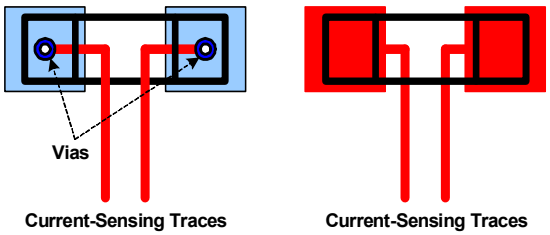
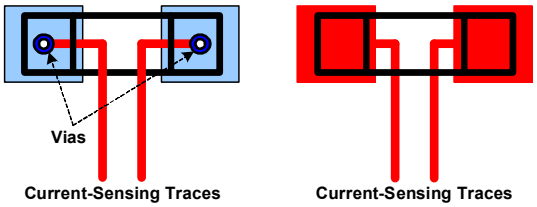
Renesas recommends using a bootstrap capacitor of 0.47µF (25V), which has an effective capacitance higher than 0.25µF at 5V and x50 effective high-side MOSFET gate capacitance.

One additional consideration is the gate charge power loss written by Equation 16 and the VDDP current consumption. Keep Pg below the VDDP overcurrent threshold.

(EQ. 16) $$Pg = (Qg(LS)) + (Qg(HS)) \bullet V_{GS} \bullet SFW$$

12. Layout Guidelines

Pin #	Pin Name	Layout Guidelines
1	VDDP	Place the decoupling capacitor in the general proximity of the controller. Run the trace connecting to the VDDP pin with sufficient width.
2	LGATE1	Switching pin. Run the LGATE1 trace in parallel with the UGATE1 and PHASE1 traces on the same PCB layer. Use sufficient width. Avoid any sensitive analog signal trace from crossing over or getting close.
3	PHASE1	Run these two traces in parallel fashion with decent width. Avoid any sensitive analog signal trace from crossing over or getting close. Renesas recommends routing the PHASE1 trace to the high-side MOSFET source pin instead of general copper. Place the IC close to the switching gate terminals of the MOSFET and keep the gate drive signal traces short for a clean MOSFET drive. The IC can be placed on the opposite side of the switching MOSFETs. Place the input capacitors as close as possible to the switching high-side MOSFET drain and the low-side MOSFET source and use shortest PCB trace connection. Place these capacitors on the same PCB layer as the MOSFETs. Do not place the capacitors on different layers with via connections. Place the inductor terminal to the switching high-side MOSFET drain and low-side MOSFET source terminal as close as possible. Minimize the phase node area to lower the electrical and magnetic field radiation but make the phase node area large enough to carry the current. Place the inductor and the switching MOSFETs on the same layer of the PCB.
4	UGATE1	
5	BOOT1	Switching pin. Place the bootstrap capacitor in the general proximity of the controller. Use sufficiently wide traces. Avoid any sensitive analog signal trace from crossing over or getting close.
6	BGATE	Use a sufficiently wide trace from the IC to the BGATE N-type MOSFET gate. Place the capacitor from BGATE to ground close to the MOSFET.
7	VBAT	Place the optional RC filter in the general proximity of the controller. Run a dedicated trace from the battery positive connection point to the IC.

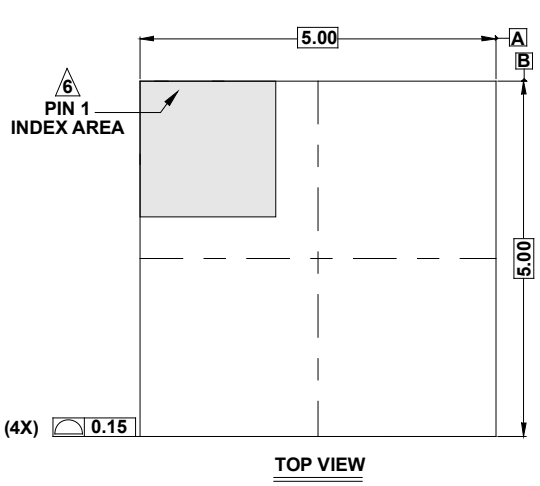
Pin #	Pin Name	Layout Guidelines
8	CSON	Run two dedicated traces with sufficient width in parallel (close to each other to minimize the loop area) from the two terminals of the battery current-sensing resistor to the IC. Place the battery current-sensing resistor close to the high-side MOSFET of the boost leg. Place the differential mode and common-mode RC filter components in the general proximity of the controller. Route the current-sensing traces through vias to connect the center of the pads or route the traces into the pads from the inside of the current-sensing resistor. The following drawings show the two preferred ways of routing current-sensing traces. 
9	CSOP	
10	NC	NC
11	PROG	Signal pin. Place the PROG programming resistor in the general proximity of the controller.
12	COMPF	Place the compensation components in the general proximity of the controller. Avoid any switching signal from crossing over or getting close.
13	COMPR	
14	AMON/BMON	No special consideration. Place the optional RC filter in the general proximity of the controller.
15	ACLIM	Place the ACLIM resistor in the general proximity of the controller.
16	ASRC	Run this trace with sufficient width in parallel fashion with the ASGATE trace.
17	CSIN	Run two dedicated traces with sufficient width in parallel (close to each other to minimize the loop area) from the two terminals of the adapter current-sensing resistor to the IC. Place the Differential mode and common-mode RC filter components in the general proximity of the controller. Keep the CSIN node near the Q_1 drain. Route the current-sensing traces through vias to connect the center of the pads or route the traces into the pads from the inside of the current-sensing resistor. The following drawings show the two preferred ways of routing current-sensing traces. 
18	CSIP	
19	ASGATE	Run this trace with sufficient width in parallel fashion with the ASRC trace.
20	VBUS	Run a dedicated trace from the bus to the pin and do not route near the switching traces.
21	VSYS	Run a dedicated trace from the system to the pin and do not route near the switching traces.
22	BATGONE/NTC	Digital pin (BATGONE), Analog Pin (NTC). Place the 10kΩ resistor series in the BATGONE signal trace and the optional decoupling capacitor in the general proximity of the controller.
23	VDD	Place the RC filter connecting with VDD pin in the general proximity of the controller. Run the trace connecting to the VDD pin with sufficient width.
24	PROCHOT#	Digital pin, open-drain output. No special consideration.
25	MCU_VDD	Place the decoupling capacitor in the general proximity of the controller. Route the trace with sufficient width.
26	VDD2P5	
27	ALERT_C	Digital pin, open-drain output. No special consideration.

Pin #	Pin Name	Layout Guidelines
28	CC1	Route the trace with sufficient width. Place decoupling capacitor to filter the noise. Renesas recommends placing the charger CC pins as close to the USB connector as possible, avoid stubs on the CC lines, and route the CC lines with about the same length.
29	CC2	
30	ALERT_B	Digital pin, open-drain output. No special consideration.
31	SCL_B	Digital pins. No special consideration. Run the SDA and SCL traces in parallel.
32	SDA_B	
33	VCONN_POWER	Place the decoupling capacitor in the general proximity of the controller. Route the trace with sufficient width.
34	SDA_C	Digital pins. No special consideration. Run the SDA and SCL traces in parallel.
35	SCL_C	
36	OTGEN/CMIN	Digital pins. No special consideration.
37	BOOT2	Switching pin. Place the bootstrap capacitor in the general proximity of the controller. Use sufficiently wide trace. Avoid any sensitive analog signal trace from crossing over or getting close.
38	UGATE2	Run these two traces in parallel fashion with sufficient width. Avoid any sensitive analog signal trace from crossing over or getting close. Renesas recommends routing the PHASE2 trace to the high-side MOSFET source pin instead of general copper. Place the IC close to the switching MOSFET's gate terminals and keep the gate drive signal traces short for a clean MOSFET drive. The IC can be placed on the opposite side of the switching MOSFETs. Place the output capacitors as close as possible to the switching high-side MOSFET drain and the low-side MOSFET source and use shortest PCB trace connection. Place these capacitors on the same PCB layer as the MOSFETs. Do not place the capacitors on different layers with via connections. Place the inductor terminal to the switching high-side MOSFET drain and low-side MOSFET source terminal as close as possible. Minimize this phase node area to lower the electrical and magnetic field radiation but make this phase node area large enough to carry the current. Place the inductor and the switching MOSFETs on the same layer of the PCB.
39	PHASE2	
40	LGATE2	Switching pin. Run the LGATE2 trace in parallel with the UGATE2 and PHASE2 traces on the same PCB layer. Use sufficient width. Avoid any sensitive analog signal trace from crossing over or getting close.
Bottom Pad	GND	Connect this ground pad to the ground plane through a low impedance path. Renesas recommends using at least five vias to connect to ground planes in the PCB to ensure sufficient thermal dissipation directly under the IC.

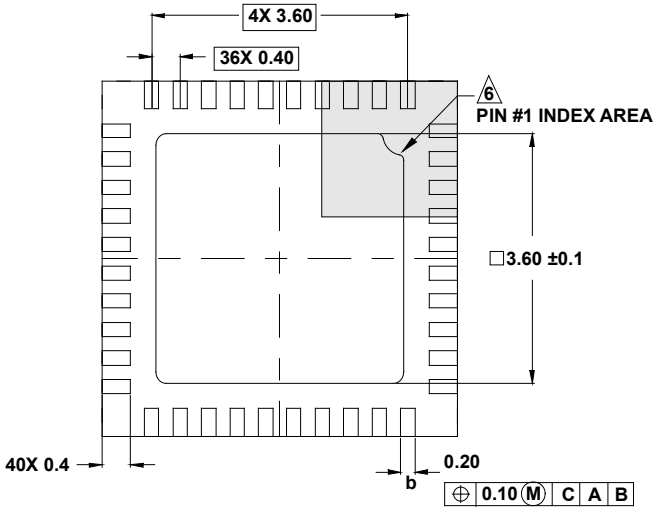
13. Package Outline Drawing

For the most recent package outline drawing, see L40.5x5C.

L40.5x5C
40 Lead Quad Flat No-Lead Plastic Package
Rev 0, 8/10

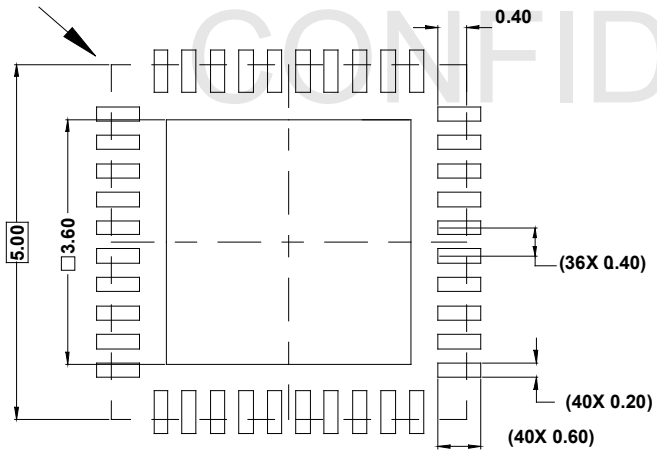


TOP VIEW

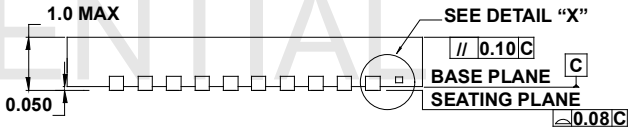


BOTTOM VIEW

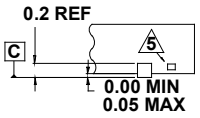
PACKAGE OUTLINE



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.27mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

14. Ordering Information

Part Number[1][2]	Part Marking	Package Description (RoHS Compliant)	Pkg. Dwg. #	Carrier Type[3]	Temp. Range
RAA489000ARGNP#AA0	489000 ARGNPA	40 Ld 5x5 QFN	L40.5x5C	Tray	-10 to +100°C
RAA489000ARGNP#HA0				Reel, 6k	
RAA489000A3GNP#AA0	489000 A3GNPA			Tray	-40 to +105°C
RAA489000A3GNP#HA0				Reel, 6k	
RTKA489000DE0000BU	Evaluation Board				

1. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. For Moisture Sensitivity Level (MSL), see the RAA489000 device page. For more information about MSL, see TB363.
3. See TB347 for details about reel specifications.

15. Revision History

Revision	Date	Description
3.01	Jan 21, 2025	In 3.4 Electrical Specifications, removed test condition for VADP (CSIN) Low Falling.
3.00	Nov 26, 2024	Updated the ASGATE and BGATE Gate Drive Current (sink) Max specs from 215µA to 250µA.
2.02	Oct 4, 2024	Corrected note in section 10.2.1.1, USB-PD On-the-Go Output Current.
2.01	Feb 16, 2023	Updated Pin Description for MCU_VDD and OTGEN/CMIN. Updated section 7.2 Programming Resistor and 7.3.13 Hardware-Based Adapter Current Limit.
2.00	May 11, 2022	Updated IBAT1 maximum specification from 65µA to 80µA. Updated SDA_B/SCL_B Input High Voltage minimum specification from 1.5V to 1.2V. Updated SDA_B/SCL_C Input High Voltage minimum specification from 1.5V to 1.2V.
1.03	Jan 6, 2022	Added evaluation board to Ordering Information.
1.02	Oct 7, 2021	Updated Figure 25, removed stop bit from the Read protocol. Updated 5.7, paragraph 3 and 7.1, paragraph 7.
1.01	May 14, 2021	In 3.4 Electrical Specifications, updated VCONN Mux and CC-PHY Protection with “Limits apply across the junction temperature range -10°C to +85°C”. Updated Pin 20. Updated 7.1, paragraph six. Updated 7.3.11, *from* Ideal DE mode is enabled or the battery discharge current is higher than 300mA *to* Ideal DE mode is enabled or the battery discharge current is higher than 160mA Added 7.3.11.1 Programmable Power Supply (PPS) Sink.
1.00	Apr 5, 2021	Initial release.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.