Data Sheet

RAA462113FYL#AC2

CMOS Image Sensor (PDAF)

R18DS0033EJ0100
Rev. 1.00
Feb 15, 2021

1. Outline

1.1 Description

The RAA462113FYL is BSI CMOS Image Sensor that achieved High-sensitivity, Low-noise and Low-power with 8M pixels for UHD (Ultra High Definition). The sensor features HDR (High Dynamic Range), PDAF (Phase Detection Auto Focus) functions and selectable output formats, MIPI-CSI2 or SLVS, which support 60fps (12bit digital output).

1.2 Features

Table 1 Features

Category	Item	Description
PKG (Package)	CLGA	144pin (pitch=1.0mm) 15.0mm x 13.3mm
Sensor	Optical format	1/1.9 inch
	Effective area	3872(H) x 2192(V)
	HOB (Horizontal Optical Black)	32 pixels
	VOB (Vertical Optical Black)	32 pixels
	Unit cell size	1.85um x 1.85um
	Primary color filter array	Bayer pattern
Power Supply	Power supply voltage	1.2V, 1.8V, 2.8V
	Power consumption	0.9W @ 60fps (typ.)
Read Mode	UHD (Ultra High Definition)	Single exposure Max. 60fps (Active area:3840x2160)
	UHD-HDR (High Dynamic Range)	Double exposure (Line by Line) Max. 30fps (Active area:3840x2160))
Output Mode	MIPI-CSI2 (Camera Serial Interface)	RAW12, RAW10
	SLVS (Scalable Low Voltage Signaling)	12bit, LSB-first
Output I/F (Interface)	Output lane	8lane+1clock, 4lane+1clock
	Data rate	891Mbps, 445.5Mbps / lane
Serial Communication	I2C (Inter-Integrated Circuit)	Fast mode, Fast mode plus
	4-wire (SCE, SCK, SDI, SDO)	2address=1word=16bit, MSB-first
A/D Converter, Gain	Resolution of A/D converter	12bit
	Gain amplifier	Analog: 0~30dB, Digital: 0~24dB
Timing Assist	Input: TRIG	Start trigger for Multi-sensor
	Output: SACK	Register write enable during movie
	Output: SYNC	Start of frame
PDAF Assist	Phase Detection Auto Focus assist function	L-open pixel R-open pixel

1.3 Block Diagram

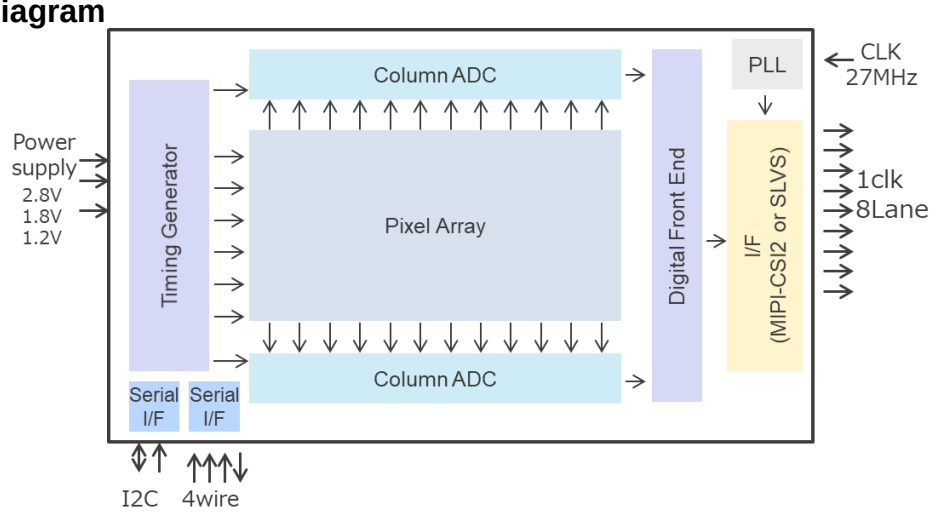


Figure 1 Block diagram

1.4 Pixel Array Structure

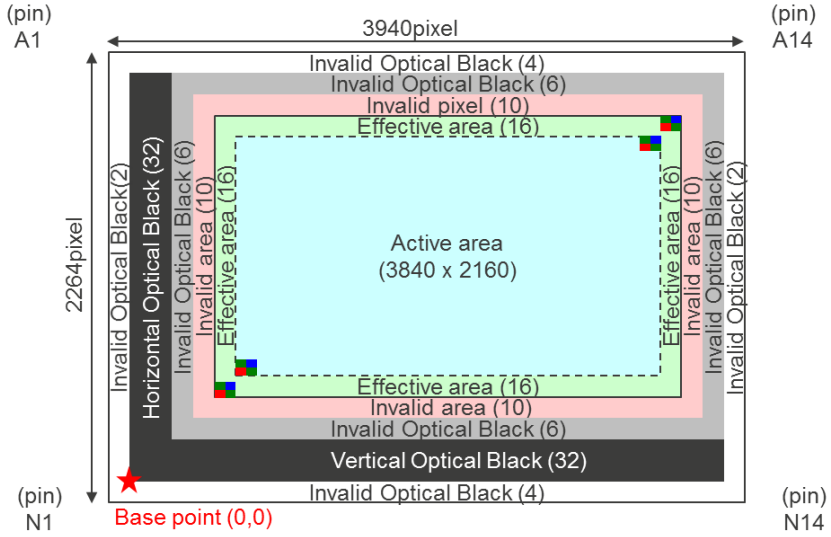


Figure 2 Pixel array structure (Top view)

1.5 PDAF pixel coordinates

L-open / R-open pixel coordinates (Unit: pixels)

Sensor don’t output Invalid data; refer to section 4.1 Read Mode.

PDAF pixel coordinates in sensor output image is shown in next expression; refer to Figure 3.

L-open pixel (Odd)

X = 16m + 48 (m = 0, 1, 2, 3, ⋯, 239)

Y = 16n + 49 (n = 0, 1, 2, 3, ⋯, 134)

L-open pixel (Even)

X = 16m + 60 (m = 0, 1, 2, 3, ⋯, 239)

Y = 16n + 57 (n = 0, 1, 2, 3, ⋯, 134)

R-open pixel (Odd)

X = 16m + 56 (m = 0, 1, 2, 3, ⋯, 239)

Y = 16n + 49 (n = 0, 1, 2, 3, ⋯, 134)

R-open pixel (Even)

X = 16m + 52 (m = 0, 1, 2, 3, ⋯, 239)

Y = 16n + 57 (n = 0, 1, 2, 3, ⋯, 134)

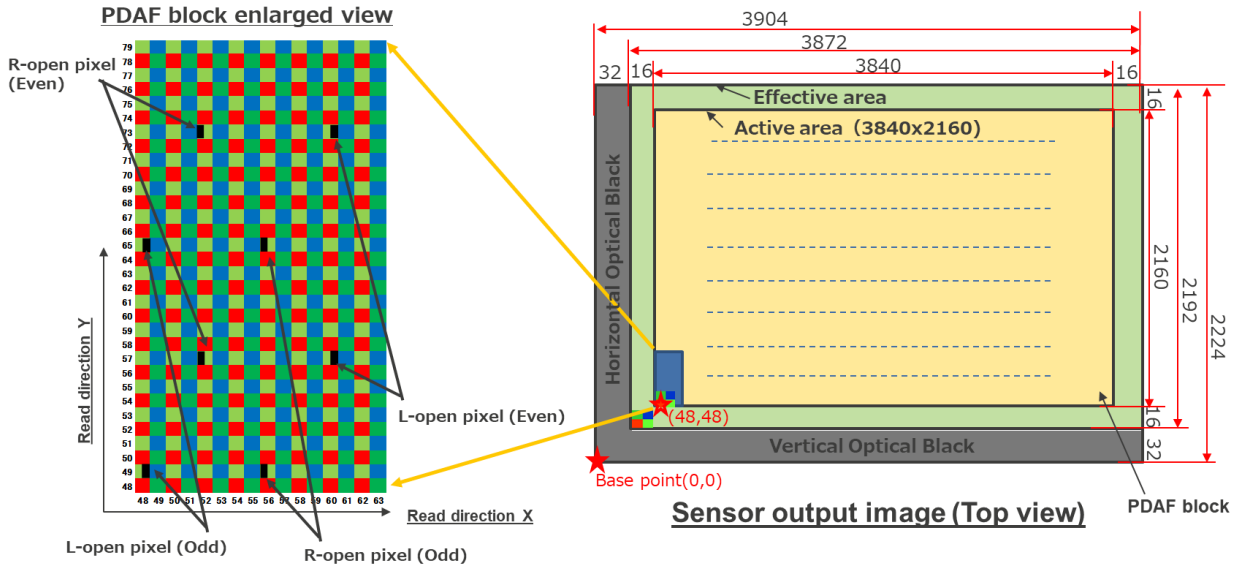


Figure 3 PDAF pixel coordinates

1.6 PKG Structure

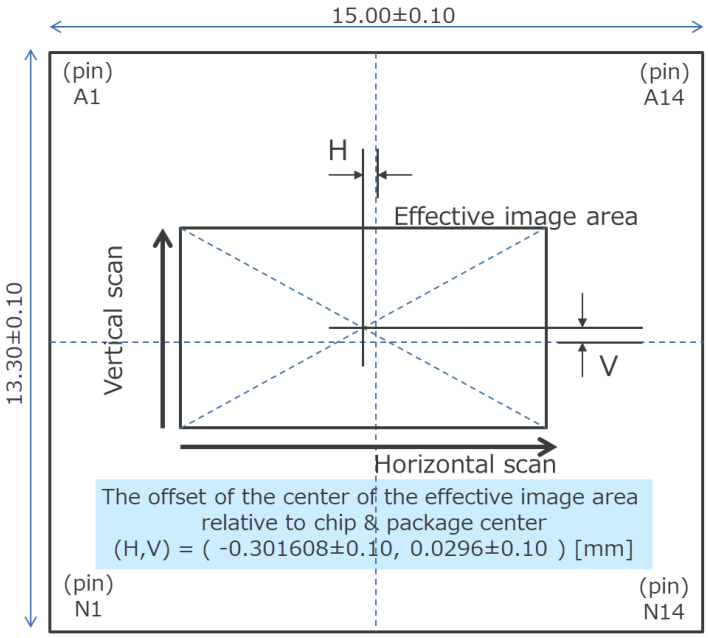
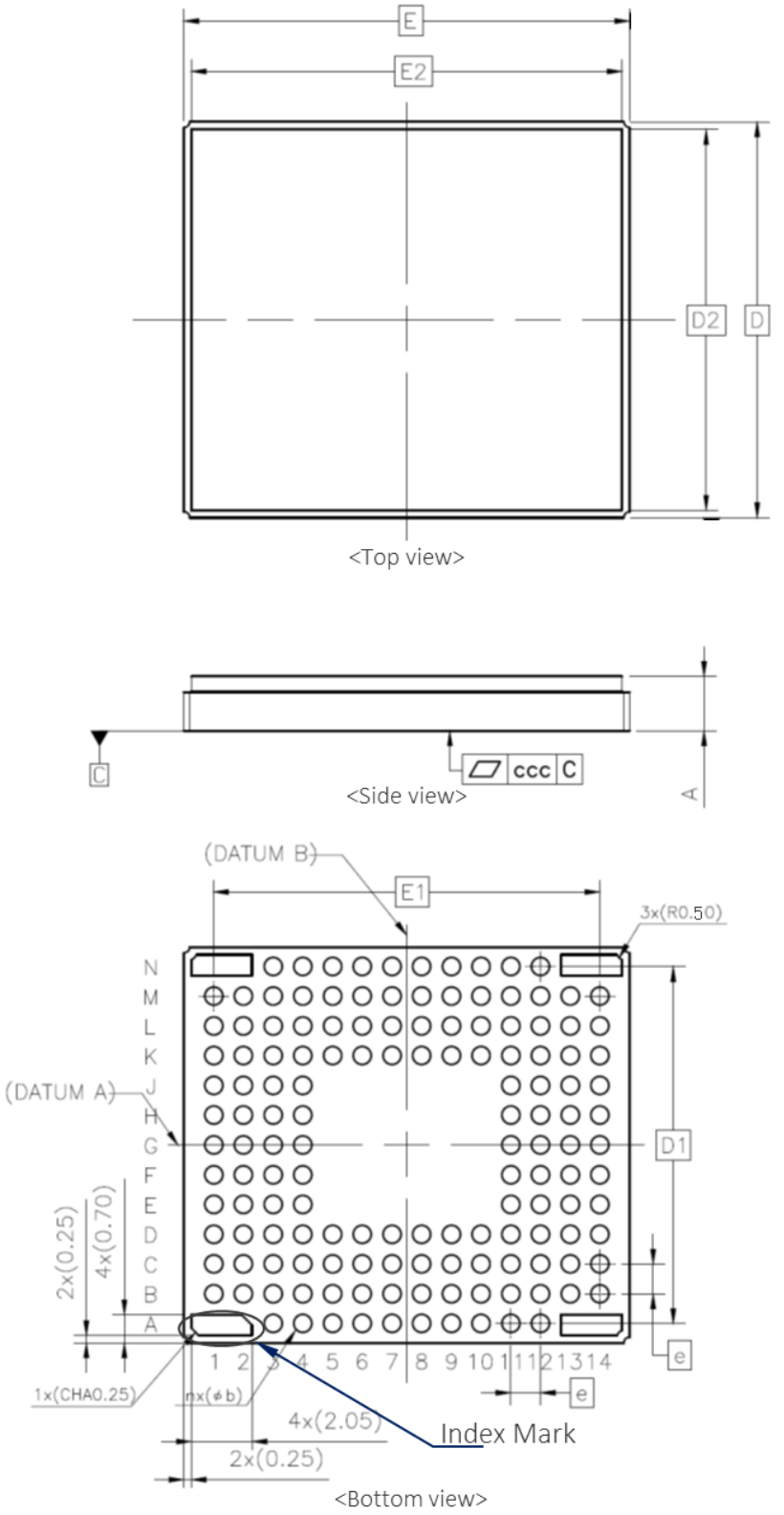


Figure 4 Chip center (Top view)



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	13.20	13.30	13.40
D2	12.70	12.80	12.90
E	14.90	15.00	15.10
E2	14.40	14.50	14.60
D1	-	12.00	-
E1	-	13.00	-
A	-	-	2.03
b	-	0.60	-
e	-	1.00	-
ccc	-	-	0.05
n	-	144	-

Figure 5 PKG structure

2 Pin Description

2.1 Pin Description

Table 2 Pin description (Power / Analog / Ground)

No.	Pin Name	I/O	Description	Note
1	VDD_PX	PWR	Analog power supply (2.8V)	
2	VDD_RG	PWR	Analog power supply (2.8V)	
3	VDD_AN	PWR	Analog power supply (2.8V)	
4	VDD_AD_N	PWR	Analog power supply (2.8V)	
5	VDD_AD_S	PWR	Analog power supply (2.8V)	
6	VDD_AD_V	PWR	Analog power supply (2.8V)	
7	VDD_AD_C	PWR	Analog power supply (2.8V)	
8	VDD_IO_N	PWR	Digital power supply (1.8V)	
9	VDD_IO_I2C	PWR	Digital power supply (1.8V)	
10	VDD_DG	PWR	Digital power supply (1.2V)	
11	VDD_DG_SL	PWR	Analog power supply (1.2V)	
12	VDD_DG_PL1	PWR	Analog power supply (1.2V)	
13	VDD_DG_PL2	PWR	Analog power supply (1.2V)	
14	VCAP_VTXH	PWR	Analog power supply (2.8V)	
15	VCAP_VDRS	AIO	Capacitor connection (6.8uF)	
16	VCAP_VTXL	AIO	Capacitor connection (22uF)	
17	VCAP_PX_N	AIO	Capacitor connection (1.0uF)	
18	VCAP_PX_S	AIO	Capacitor connection (1.0uF)	
19	IREF	AIO	Resister connection (10kΩ)	
20	VREF	AI	Reference voltage (1.8V)	
21	GND_PX	GND	Analog ground	
22	GND_RG	GND	Analog ground	
23	GND_AN	GND	Analog ground	
24	GND_AD_N	GND	Analog ground	
25	GND_AD_S	GND	Analog ground	
26	GND_AD_V	GND	Analog ground	
27	GND_AD_C	GND	Analog ground	
28	GND_IO_N	GND	Digital ground	
29	GND_IO_I2C	GND	Digital ground	
30	GND_DG	GND	Digital ground	
31	GND_DG_SL	GND	Analog ground (Dedicated to SLVS)	

Table 3 Pin description (Interface)

No.	Pin Name	I/O	Description	Note
34	D1P	DO	MIPI-CSI2 / SLVS output (Data lane-1 positive polarity)	
35	D1N	DO	MIPI-CSI2 / SLVS output (Data lane-1 negative polarity)	
36	D2P	DO	MIPI-CSI2 / SLVS output (Data lane-2 positive polarity)	
37	D2N	DO	MIPI-CSI2 / SLVS output (Data lane-2 negative polarity)	
38	D3P	DO	MIPI-CSI2 / SLVS output (Data lane-3 positive polarity)	
39	D3N	DO	MIPI-CSI2 / SLVS output (Data lane-3 negative polarity)	
40	D4P	DO	MIPI-CSI2 / SLVS output (Data lane-4 positive polarity)	
41	D4N	DO	MIPI-CSI2 / SLVS output (Data lane-4 negative polarity)	
42	D5P	DO	MIPI-CSI2 / SLVS output (Data lane-5 positive polarity)	
43	D5N	DO	MIPI-CSI2 / SLVS output (Data lane-5 negative polarity)	
44	D6P	DO	MIPI-CSI2 / SLVS output (Data lane-6 positive polarity)	
45	D6N	DO	MIPI-CSI2 / SLVS output (Data lane-6 negative polarity)	
46	D7P	DO	MIPI-CSI2 / SLVS output (Data lane-7 positive polarity)	
47	D7N	DO	MIPI-CSI2 / SLVS output (Data lane-7 negative polarity)	
48	D8P	DO	MIPI-CSI2 / SLVS output (Data lane-8 positive polarity)	
49	D8N	DO	MIPI-CSI2 / SLVS output (Data lane-8 negative polarity)	
50	CK1P	DO	MIPI-CSI2 / SLVS output (Clock lane positive polarity)	
51	CK1N	DO	MIPI-CSI2 / SLVS output (Clock lane negative polarity)	
52	CLK_RF1	DI	Reference clock signal input (27MHz)	
53	RSTN	DI	System reset (Low: reset, High: release)	
54	SDA	DIO	Data input / output for I2C serial communication	
55	SCL	DI	Clock input for I2C serial communication	
56	SCE	DI	Data input for 4-wire serial communication	
57	SCK	DI	Clock input for 4-wire serial communication	
58	SDI	DI	Data input for 4-wire serial communication	
59	SDO	DO	Data output for 4-wire serial communication	
60	TRIG	DI	Data input for Synchronization	
61	SYNC	DO	Timing pulse of Start of Frame	
62	SACK	DO	Timing pulse of serial communication write enable	
63	CM4W	DI	Mode select (Low: I2C, High: 4-wire)	
64	CMHP	DI	I2C mode select (Low: fast-mode, High: fast-mode plus)	
65	CMHV	DI	I2C driver select for large load capacitor or Pull-up voltage > 2.5V	

Table 4 Pin description (Test)

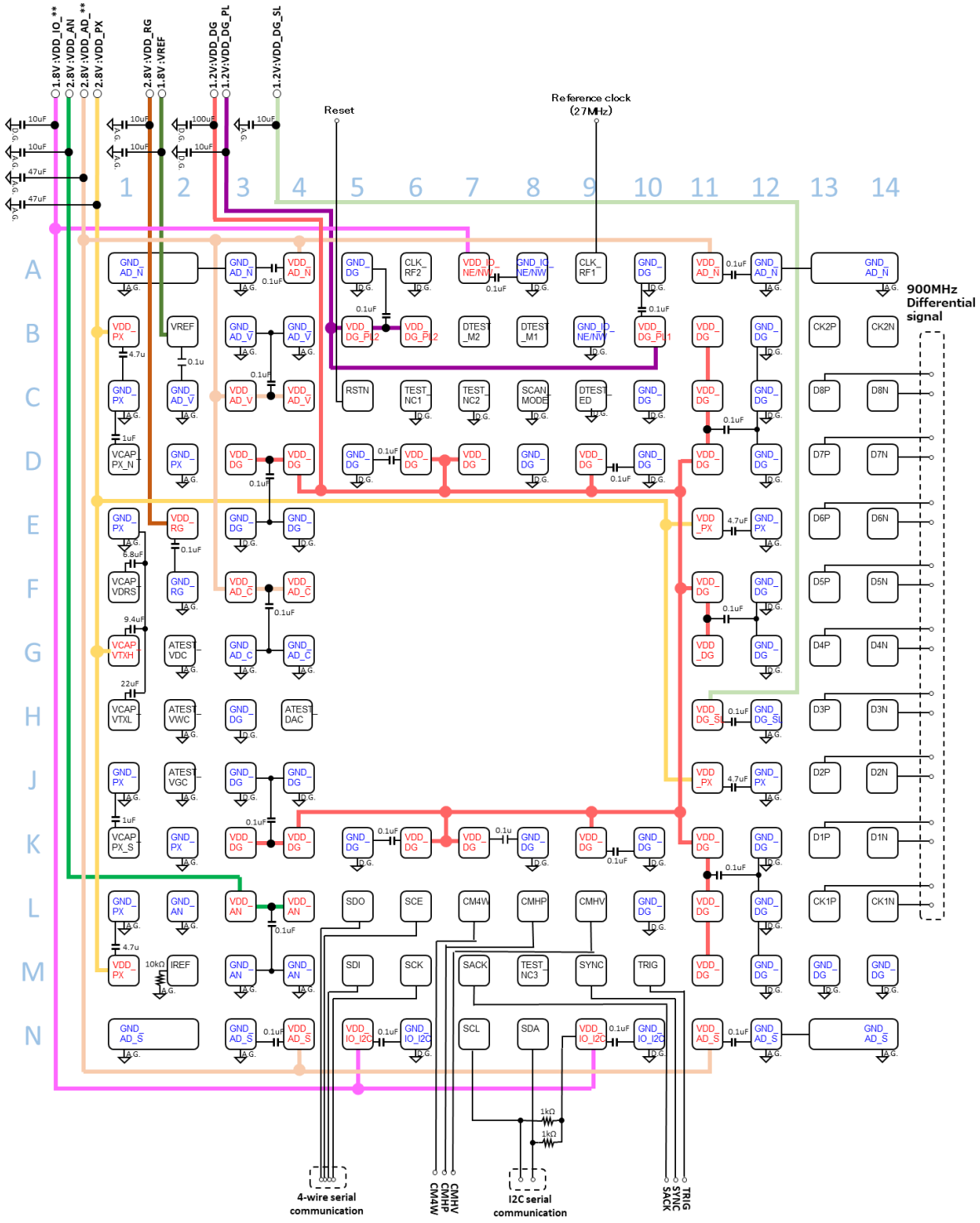
No.	Pin Name	I/O	Description	Note
66	CK2P	DO	Test pin (No connection)	
67	CK2N	DO	Test pin (No connection)	
68	CLK_RF2	DI	Test pin (It must be connected to Digital ground by users.)	
69	ATEST_VDC	AI	Test pin (It must be connected to Analog ground by users.)	
70	ATEST_VWC	AI	Test pin (It must be connected to Analog ground by users.)	
71	ATEST_VGC	AI	Test pin (It must be connected to Analog ground by users.)	
72	ATEST_DAC	AO	Test pin (No connection)	
73	DTEST_ED	DI	Test pin with pull down which internally connects to Digital ground	
74	DTEST_M1	DO	Test pin (No connection)	
75	DTEST_M2	DO	Test pin (No connection)	
76	SCAN_MODE	DI	Test pin with pull down which internally connects to Digital ground	
77	TEST_NC1	DIO	Test pin (No connection)	
78	TEST_NC2	DIO	Test pin (No connection)	
79	TEST_NC3	DO	Test pin (No connection)	

2.2 Pin Assignment

Table 5 Pin assignment (Top view)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	GND_AD_N		GND_AD_N	VDD_AD_N	GND_DG	CLK_RF2	VDD_D_NEAR	GND_D_NEAR	CLK_RF1	GND_DG	VDD_AD_N	GND_AD_N	GND_AD_N	
B	VDD_PX	VREF	GND_AD_V	GND_AD_V	VDD_DG_PL2	VDD_DG_PL2	DTEST_M2	DTEST_M1	GND_D_NEAR	VDD_DG_PL1	VDD_DG	GND_DG	CK2P	CK2N
C	GND_PX*	GND_AD_V	VDD_AD_V	VDD_AD_V	RSTN	TEST_NC1	TEST_NC2	SCAN_MODE	DTEST_ED	GND_DG	VDD_DG	GND_DG	D8P	D8N
D	VCAP_PX_N	GND_PX*	VDD_DG	VDD_DG	GND_DG	VDD_DG	VDD_DG	GND_DG	VDD_DG	GND_DG	VDD_DG	GND_DG	D7P	D7N
E	GND_PX*	VDD_RG	GND_DG	GND_DG							VDD_PX	GND_PX	D6P	D6N
F	VCAP_VDRS	GND_RG	VDD_AD_C	VDD_AD_C							VDD_DG	GND_DG	D5P	D5N
G	VCAP_VTXH	ATEST_VDC	GND_AD_C	GND_AD_C							VDD_DG	GND_DG	D4P	D4N
H	VCAP_VTXL	ATEST_VWC	GND_DG	ATEST_DAC							VDD_DG_SL	GND_DG_SL	D3P	D3N
J	GND_PX*	ATEST_VGC	GND_DG	GND_DG							VDD_PX	GND_PX	D2P	D2N
K	VCAP_PX_S	GND_PX*	VDD_DG	VDD_DG	GND_DG	VDD_DG	VDD_DG	GND_DG	VDD_DG	GND_DG	VDD_DG	GND_DG	D1P	D1N
L	GND_PX*	GND_AN*	VDD_AN	VDD_AN	SDO	SCE	CM4W	CMHP	CMHV	GND_DG	VDD_DG	GND_DG	CK1P	CK1N
M	VDD_PX	IREF	GND_AN*	GND_AN*	SDI	SCK	SACK	TEST_NC3	SYNC	TRIG	VDD_DG	GND_DG	GND_DG	GND_DG
N	GND_AD_S		GND_AD_S	VDD_AD_S	VDD_I2C	GND_I2C	SCL	SDA	VDD_I2C	GND_I2C	VDD_AD_S	GND_AD_S	GND_AD_S	

Figure 6 Example of external circuit (Top view)



3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 6 Absolute maximum ratings

Item	Symbol	Min	Max	Unit
VDD_PX, VDD_RG, VDD_AD_N, VDD_AD_S, VDD_AD_V VDD_AD_C,VDD_AN, VCAP_VTXH,VREF,IREF, VCAP_VDRS VCAP_PX_N, VCAP_PX_, VDD_IO_N, VDD_IO_I2C SDA, SCL,SCE,SCK,SDI,CM4W, CMHP, CMHV CLK_RF1, RSTN,TRIG,SDO, SACK, SYNC ATEST_VDC, ATEST_VWC,ATEST_VGC,ATEST_DAC DTEST_ED, SCAN_MODE,CLK_RF2, DTEST_M1, DTEST_M2 TEST_NC1, TEST_NC2, TEST_NC3	AVH	-0.3	3.6V	V
VCAP_VTXL	AVN	-0.9	0.3	V
VDD_DG, VDD_DG_PL1, VDD_DG_PL2, VDD_DG_SL D*P, D*N, {*: Lane Number (1~8) },CK1P, CK1N,CK2P, CK2N	AVL	-0.3	1.32	V
Storage temperature	Tstg	-20	110	°C
Operating temperature	Ta	-20	85	°C
Storage and operating humidity	-	No condensation		%

3.2 Power Supply

Table 7 Power supply voltage

Item	Symbol	Min	Typ	Max	Unit	Condition
2.8V power supply (analog) VDD_PX, VDD_RG VDD_AD_N, VDD_AD_S VDD_AD_V, VDD_AD_C VDD_AN , VCAP_VTXH	VDA28	2.66	2.80	2.94	V	
1.8V power supply (digital) VDD_IO_N, VDD_IO_I2C	VDD18	1.71	1.80	1.89	V	
1.8V power supply (analog) VREF	VDA18	1.71	1.80	1.89	V	
1.2V power supply (digital) VDD_DG	VDD12	1.14	1.20	1.26	V	
1.2V power supply (analog) VDD_DG_PL1, VDD_DG_PL2 VDD_DG_SL	VDA12	1.14	1.20	1.26	V	

Table 8 Current consumption

Ta=25°C, power supply voltage: typical if not specified

Item	Symbol	Min	Typ	Max	Unit	Condition
2.8V power supply (analog) VDD_PX, VDD_RG VDD_AD_N, VDD_AD_S VDD_AD_V, VDD_AD_C VDD_AN , VCAP_VTXH	IVDA28	-	190	210	mA	
1.8V power supply (digital) VDD_IO_N, VDD_IO_I2C	IVDD18	-	0.1	4	mA	
1.8V power supply (analog) VREF	IVDA18	-	0.1	1	mA	
1.2V power supply (digital) VDD_DG	IVDD12	-	300	340	mA	
1.2V power supply (analog) VDD_DG_PL1, VDD_DG_PL2 VDD_DG_SL	IVDA12	-	9	12	mA	

3.3 Pixel Characteristics

3.3.1 Image Sensor Characteristics

Table 9 Sensor characteristics w/o PDAF Pixels

Tj=60°C, power supply voltage: typical if not specified

Item	Symbol	Min	Typ	Max	Unit	Condition
Sensitivity	SENS_G	2100	-	-	LSB	*1
Sensitivity ratio R/G	SENS_R/G	35	-	49	%	*1,*2
Sensitivity ratio B/G	SENS_B/G	64	-	88	%	*1,*2
Maximum output	OUT_MAX	4000	-	-	LSB	
Dark Shading	D_SHAD	-	-	17	LSB	*3
Line crawl R	LINE_C_R	-6		6	%	*4
Line crawl G	LINE_C_G	-6		6	%	*4
Line crawl B	LINE_C_B	-6		6	%	*4

Light Source: D50 (defined in JIS8720 5000K) telecentric illuminator with heat-absorbing filter HOYA HA-50 and color correction filter HOYA CM500S.

*1 Sensitivity

(1) Apply 5x5 pixels median filter for image data, R/Gb/Gr/B respectively. ------ (a)

(2) For image (a), calculate average of R/Gb/Gr/B data on center area ------- (b)
center area : please refer to Figure 7.

(3) calculate data(b) – offset level (OB data) ------ SENS_R/SENS_G((Gr+Gb)/2)/SENS_B

*2 Sensitivity ratio

(1) calculate SENS_R/SENS_G ------ SENS_R/G

(2) calculate SENS_B/SENS_G ------ SENS_B/G

*3 Dark shading

(1) ZoneII divide to 48×27 blocks. 1 block is 80×80, 96×96, 96×80 or 80×96 pixels. Please refer to Figure 7.

(2) Averaging output data in a block, R/G/B respectively.

(3) SHADE_R/G/B=(MAX-MIN)/(Ave.@center area)

*4 Line Crawl R/G/B

(1) ZoneII divide to 48×27 blocks. Please refer to Figure 7.

(2) Averaging output data in a block, Gb and Gr respectively. ------ AVE_Gb/AVE_Gr

(3) LINE_C_R/G/B=(AVE_Gr-AVE_Gb)/{(AVE_Gr+AVE_Gb)/2}×100

<Lighting condition>

LINE_C_R : Red

LINE_C_G : Green

LINE_C_B : Blue

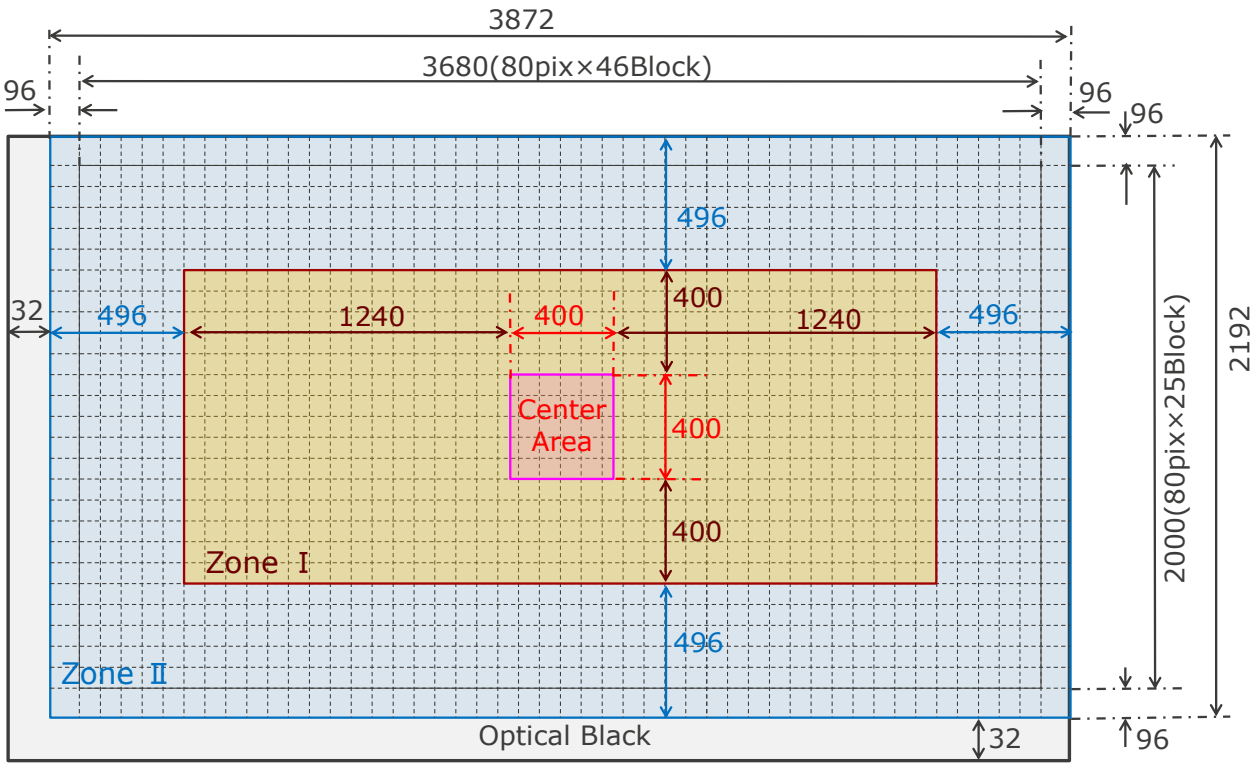


Figure 7 Pixel characteristics calculation area

Table 10 Sensor characteristics of PDAF Pixels

Tj=60°C, power supply voltage: typical if not specified

Item	Symbol	Min	Typ	Max	Unit	Condition
Sensitivity ratio L-open/R-open	SENS_PL/PR	0.67	1	1.5	-	*1
PDAF Sensitivity	SENS_PL, SENS_PR	656	-	-	LSB	*1

Note) This chip doesn't have the function to correct the sensitivity ratio; L-open/R-open inside. When you use PDAF function, please correct the sensitivity ratio to 1 in calculation.

Ex. You should multiply R-open PDAF output data by SENSE_PL/PR or multiply L-open PDAF pixel output data by 1/(SENSE_PL/PR).

Light Source: D50 (defined in JIS8720 5000K) telecentric illuminator with heat-absorbing filter HOYA HA-50 and color correction filter HOYA CM500S.

*1 PDAF Sensitivity, Sensitivity ratio L-open/R-open

(1) Apply 5x5 pixels median filter for image data, L-open/R-open respectively. ------ (a)
(2) For image (a), calculate average of L-open/R-open data of all PDAF pixels ------- (b)
(3) calculate data(b) – offset level (OB data) ------ SENS_PL, SENS_PR
(4) calculate SENS_PL/SENS_PR------ SENS_PL/PR

3.3.2 Spectral Characteristics

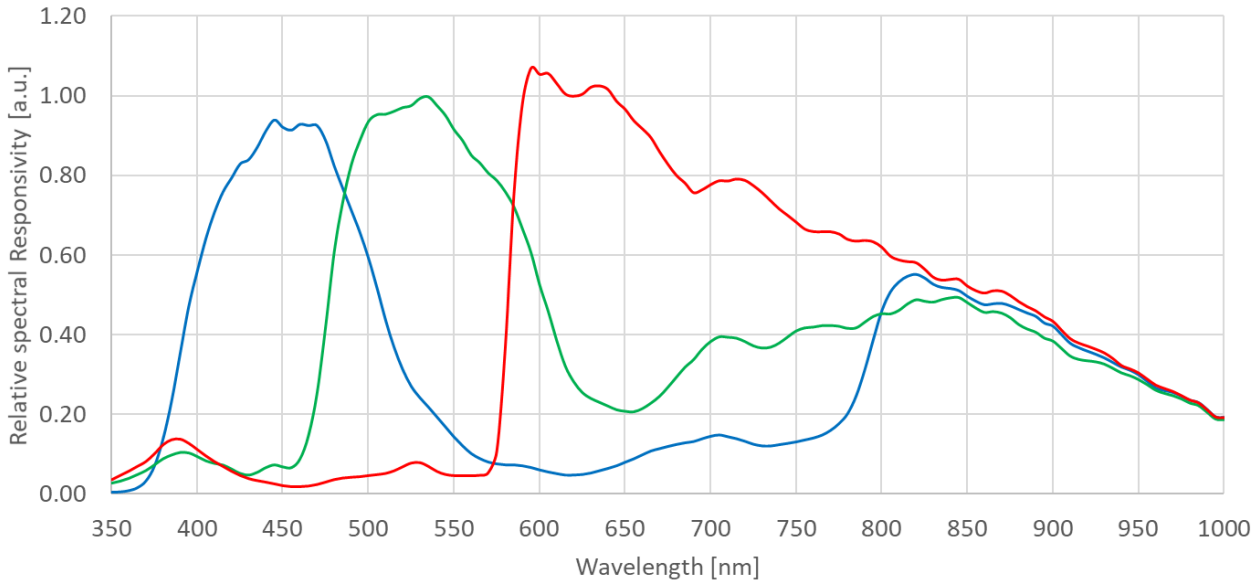


Figure 8 Spectral characteristics

Note: Spectral characteristics has possibility to change in sensor development.

3.3.3 Pixel Defect Specifications

Table 11 Pixel defect specifications

Tj=60°C, power supply voltage: typical if not specified

Item	Symbol	Min	Typ	Max	Unit	Condition
Shine spot defect at Dark	WHI	-	-	1999	pixel	*1
Shine/Black spot defect at Bright（w/o PDAF）	SHIN	-	-	1999	pixel	*2
Shine spot defect at Dark (PDAF)	WHI_P			31	pixel	*3
Shine/Black spot defect at Bright（PDAF）	SHIN_P	-	-	31	pixel	*4
Pixel defect pattern (Mass defect)	MASS_D	-	-	0	pixel	*5
PDAF pixel spot defect in any 16x8 PDAF pixel region	MASS_PDAF			1	pixel	*6

*1 Shine spot defect at Dark
(1) Take dark image @ Analog Gain 30dB------ (a)
(2) Apply 5x5 pixels median filter for image data ------- (b)
(3) Calculate (a)-(b) each pixel on zone II------ (c)
(4) Count shine spot defect on data_(c)

*2 Shine/Black spot defect at Bright
(1) Take image @ Analog Gain 0dB------ (a)
(2) Apply 5x5 pixels median filter for image data (R, Gb, Gr and B respectively) ------- (b)
(3) Calculate (a)-(b) each pixel on zone II------ (c)
(4) Calculate I/((b)-Dark_offset) x 100 each pixel on zone II------ (d)
(5) Shine spot defect is over 15% on data (d)
(6) Black spot defect is under -15% on data (d)

*3 Shine spot defect at Dark (PDAF)
(1) Take image and pick up PDAF image data @ Analog gain 30dB ------- (a)
(2) Apply 5x5 pixel median filter for PDAF image data ------ (b)
(3) Calculate (a)-(b) each pixel ------ (c)
(4) Count shine spot defect on data_(c).

*4 Shine/Black spot defect at Bright（PDAF）
(1) Take image and pick up PDAF image data @ Analog Gain 0dB------ (a)
(2) Apply 5x5 pixels median filter for PDAF image data ------- (b)
(3) Calculate (a)-(b) each pixel ------ (c)
(4) Calculate I/((b)-Dark_offset) x 100 each pixel ------ (d)
(5) Shine spot defect is over 15% on data (d)
(6) Black spot defect is under -15% on data (d)

*5 Pixel defect pattern
Devices which include three or less pixel defects at each color in 3 x 3 Bayer area are not rejected.

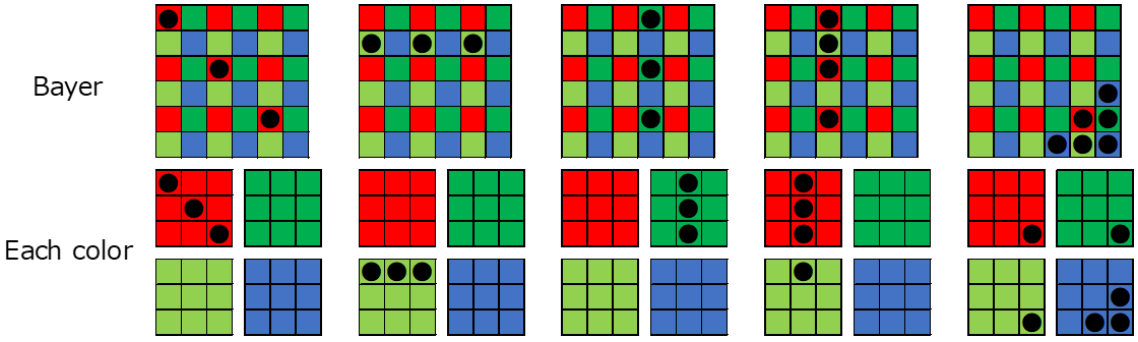


Figure 9 Examples of allowed pixel defect patterns

However, devices which include following pattern (1) or (2) are rejected.
Pattern (1) : Devices which include four or more pixels defect at each color in 4 x 4 Bayer area are rejected.

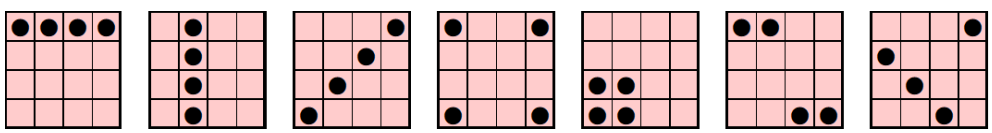


Figure 10 Examples of not allowed pixel defect patterns

Pattern (2) : Devices which include consecutive defects at all colors in 3 x 3 Bayer area even including three pixel defects at each color are rejected.

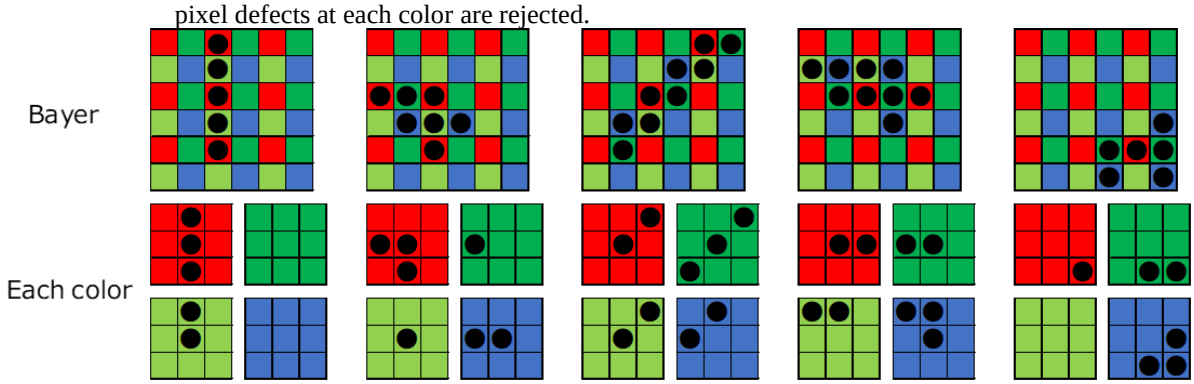


Figure 11 Examples of not allowed pixel defect patterns

*6 PDAF pixel spot defect in each 16 x 8 PDAF pixel region

Devices which include two L-open PDAF pixel defects in each 16 x 8 PDAF L-open pixel area are rejected.

Devices which include two R-open PDAF pixel defects in each 16 x 8 PDAF R-open pixel area are rejected.

3.4 Digital I/O (Input/Output)

Table 12 DC characteristics (Common)

Digital input pin: CLK_RF1, RSTN, TRIG, CM4W, CMHP, CMHV
Digital output pin: SYNC, SACK
Ta=25°C, power supply voltage: typical if not specified

Item	Symbol	Min	Typ	Max	Unit	Condition
Digital Input Voltage at High	VIH	VDD18 x0.8		VDD18 +0.2	V	
Digital Input Voltage at Low	VIL	-0.2		VDD18 x0.2	V	
Digital Output Voltage at High	VOH	VDD18 -0.2		-	V	IOH=1mA
Digital Output Voltage at Low	VOL			0.20	V	IOL=1mA

Table 13 AC characteristics (Clock)

Clock: CLK_RF1
Ta=25°C, power supply voltage: typical if not specified

Item	Symbol	Min	Typ	Max	Unit	Condition
Clock cycle time	tCLKcyc	typ -20 ppm	1/27M	typ +20 ppm	s	
High level pulse width	tCLKH	tCLKcyc x0.42		tCLKcyc x0.58	s	
Low level pulse width	tCLKL	tCLKcyc x0.42		tCLKcyc x0.58	s	
Clock Rise Time	tCLKr			1	ns	20% - 80%
Clock Fall Time	tCLKf			1	ns	80% - 20%
Clock Jitter	tCLKj	-15		+15	ps	

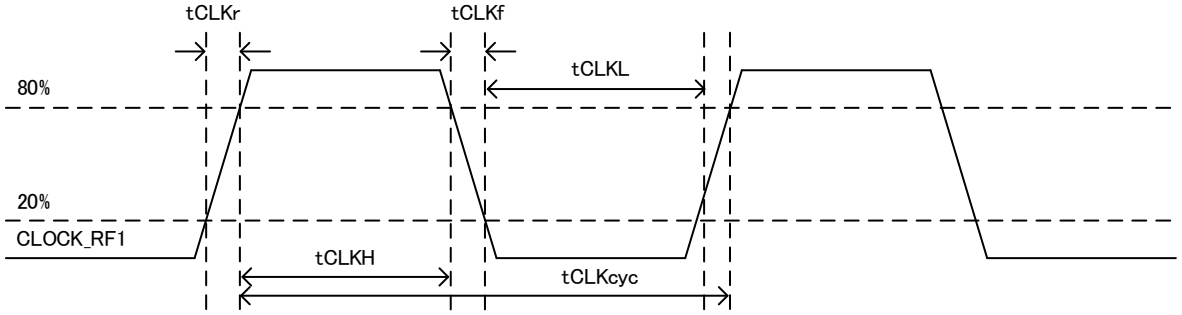


Figure 12 CLK_RF1 waveform

Table 14 AC characteristics (Digital input pin)

Digital input pin: TRIG, RSTN, CM4W, CMHP, CMHV
Ta=25°C, power supply voltage: typical if not specified

Item	Symbol	Min	Typ	Max	Unit	Condition
Rise Time	tR			5	ns	20% - 80%
Fall Time	tF			5	ns	80% - 20%
High level pulse width for TRIG	tTRIGH	75		3000	ns	

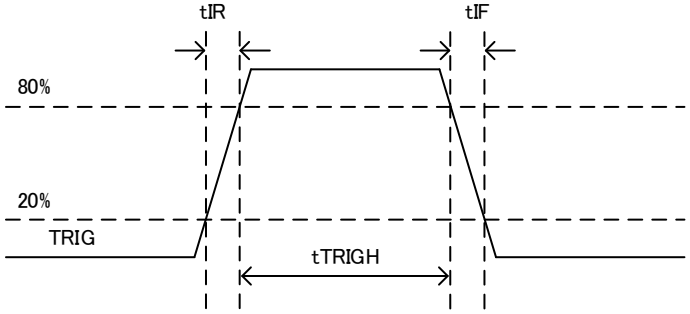


Figure 13 TRIG waveform

3.5 Serial Communication

3.5.1 I2C

Table 15 I2C bus DC characteristics

Ta=25°C, power supply voltage: typical if not specified

Item	Symbol	Min	Typ	Max	Unit	Condition
Pull-up voltage	VDI	1.72	1.8		V	
Pull-up resistor (CB=total capacitance of one bus line in pF)	RP	VDI *0.7 /3		250/ 0.8473 /CB	kΩ	fast mode
		VDI *0.7 /20		120/ 0.8473 /CB		fast mode plus
LOW level input voltage	VIL	-0.5		VDI *0.3	V	
HIGH level input voltage	VIH	VDI *0.7		VDI +0.5	V	
Hysteresis of Schmitt trigger inputs	VHYS	VDI *0.05		-	V	
LOW level output voltage (open drain) at 2mA sink current	VOL	0		VDI *0.2	V	
HIGH level output voltage	VOH	VDI *0.8		-	V	
Low level output current (VOL=0.4V)	IOL	3		-	mA	fast mode
		20		-		fast mode plus
Output fall time from VIHmin to VILmax with bus capacitance (CB) from 10 pF to 400 pF	tOF	VDDI *20 /5.5		250	ns	fast mode : <400pF
		VDDI *20 /5.5		120		fast mode plus : <550pF
Pulse width of spikes which shall be suppressed by the input filter	tSP	0		50	ns	
Input current each I/O pin with an input voltage between 0.1 VDI and 0.9 VDI	It	-10		10	uA	
Input/Output capacitance (SDA)	CI/O	-		8	pF	
Input capacitance (SCL)	CI	-		6	pF	

Table 16 I2C bus timing characteristics

Ta=25°C, power supply voltage: typical if not specified

Item	Symbol	Min	Typ	Max	Unit	Condition
SCL clock frequency	fSCL	0	-	400	kHz	fast mode
		0	-	1000		fast mode plus
Hold time (repeated) START condition. After this period, the first clock pulse is generated	tHD;STA	0.6	-	-	us	fast mode
		0.26	-	-		fast mode plus
LOW period of the SCL clock	tLOW	1.3	-	-	us	fast mode
		0.5	-	-		fast mode plus
HIGH period of the SCL clock	tHIGH	0.6	-	-	us	fast mode
		0.26	-	-		fast mode plus
Setup time for a repeated START condition	tSU;STA	0.6	-	-	us	fast mode
		0.26	-	-		fast mode plus
Data hold time	tHD;DAT	0	-	0.9	us	fast mode
		0	-	0.45		fast mode plus
Data set-up time	tSU;DAT	100	-	-	ns	fast mode
		50	-	-		fast mode plus
Rise time of both SDA and SCL signals (CB=total capacitance of one bus line in pF)	tR	20	-	300	ns	fast mode
		-	-	120		fast mode plus
Fall time of both SDA and SCL signals (CB=total capacitance of one bus line in pF)	tF	VDI *20 /5.5	-	300	ns	fast mode
		VDI *20 /5.5	-	120		fast mode plus
Set-up time for STOP condition	tSU;STO	0.6	-	-	us	fast mode
		0.26	-	-		fast mode plus
Bus free time between a STOP and START condition	tBUF	1.3	-	-	us	fast mode
		0.5	-	-		fast mode plus
Capacitive load for each bus line	CB	10	-	400	pF	fast mode
		10	-	550		fast mode plus
Noise margin at the LOW level for each connected device (including hysteresis)	VnL	0.18	-	-	V	

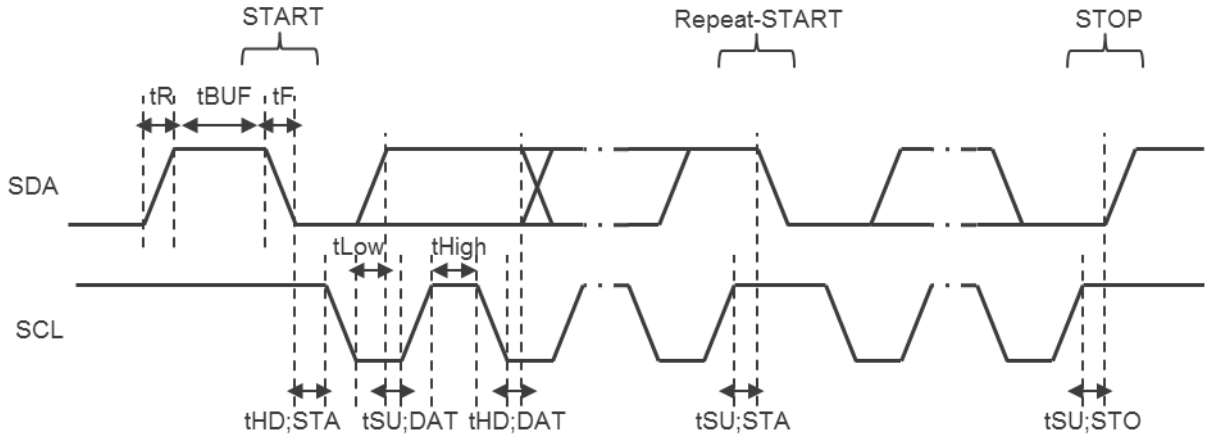


Figure 14 I2C bus timing

3.5.2 4-wire

Table 17 4-wire DC/AC characteristics

Input Pin: SCE, SCK, SDI
Output Pin: SDO
Ta=25°C, power supply voltage: typical if not specified

Item	Symbol	Min	Typ	Max	Unit	Condition
Digital Input Voltage at High	VIH	VDD18 x0.8		VDD18 +0.2	V	
Digital Input Voltage at Low	VIL	-0.2		VDD18 x0.2	V	
Digital Output Voltage at High	VOH	VDD18 -0.2		-	V	IOH=1mA
Digital Output Voltage at Low	VOL	-		0.20	V	IOL=1mA
SCE setup time	tSSCE	40		-	ns	
SCE hold time	tHSCE	40		-	ns	
SCK Cycle time	tSCK	93		-	ns	
SDI input setup time	tSUS	20		-	ns	
SDI input hold time	tHOS	20		-	ns	
SDO output delay	tDLY	-		30	ns	output capacitance 5pF

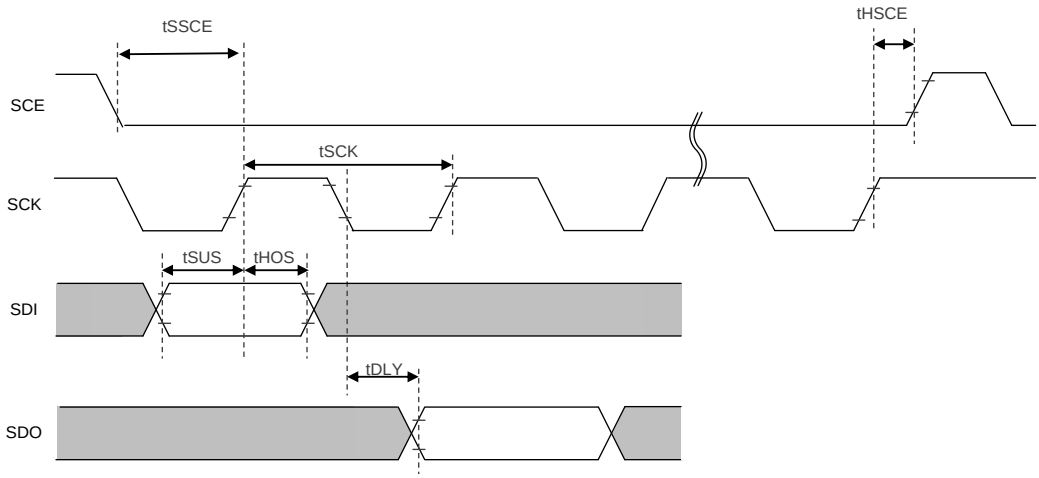


Figure 15 Timing chart of 4-wire

3.6 Image data output Interfaces

3.6.1 MIPI-CSI2 (Low-power mode)

Table 18 Low-power mode DC characteristics

Ta=25°C, power supply voltage: typical if not specified

Item	Symbol	Min	Typ	Max	Unit	Condition
Thevenin output high level	V_{OH}	1.1	1.2	1.3	V	*1
Thevenin output low level	V_{OL}	-50		50	mV	*1
Output impedance of LP transmitter	Z_{OLP}	110			Ω	

*1: The value is specified when the output pin is unloaded.

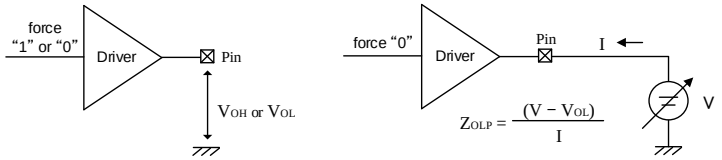


Figure 16 Load circuits for CSI2 Low-power mode

Table 19 Low-power mode AC characteristics

Ta=25°C, power supply voltage: typical if not specified

Item	Symbol	Min	Typ	Max	Unit	Condition
Load capacitance condition		0	-	70	pF	
15%-85% fall time	T_{FLP}	-	-	25	ns	
30%-85% rise time	T_{REOT}	-	-	35	ns	
Slew rate @ C_{LOAD} = 0pF	$\delta V/\delta t_{SR}$	-	-	500	mV/ns	*1
Slew rate @ C_{LOAD} = 5pF		-	-	300	mV/ns	*1
Slew rate @ C_{LOAD} = 20pF		-	-	250	mV/ns	*1
Slew rate @ C_{LOAD} = 70pF		-	-	150	mV/ns	*1
Slew rate @ C_{LOAD} = 0 to 70pF (Falling Edge Only)		30	-	-	mV/ns	*2
Slew rate @ C_{LOAD} = 0 to 70pF (Rising Edge Only)		30	-	-	mV/ns	*3
Slew rate @ C_{LOAD} = 0 to 70pF (Rising Edge Only) VO,INST : instantaneous output voltage in mV		30 – 0.075 (VO,INST – 700)	-	-	mV/ns	*4

*1: When the output voltage is between VOL and VOH.
*2: When the output voltage is between 400mV and 930mV.
*3: When the output voltage is between 400mV and 700mV.
*4: When the output voltage is between 700mV and 930mV.

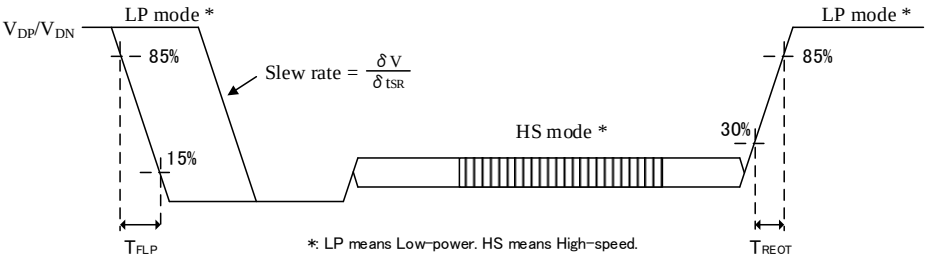


Figure 17 CSI2 Low-power and High-speed

3.6.2 SLVS and MIPI-CSI2 (High-speed mode)

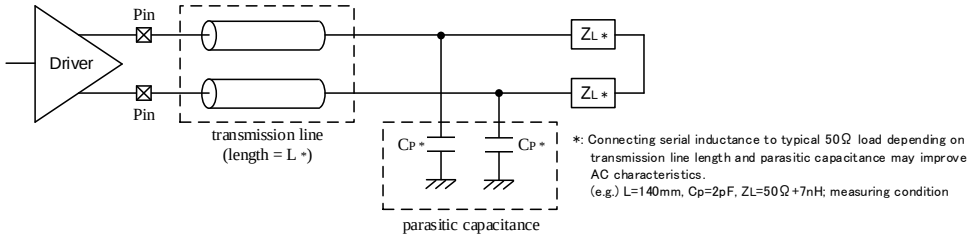


Figure 18 Load circuits for SLVS and CSI2 High-speed mode

Table 20 MIPI-CSI2 High-speed mode DC characteristics

Ta=25°C, power supply voltage: typical if not specified

Item	Symbol	Min	Typ	Max	Unit	Condition
HS transmit static common-mode voltage	V_{CMTX}	150	200	250	mV	
V_{CMTX} mismatch when output is Differential-1 or Differential-0	$\|\Delta V_{CMTX(1,0)}\|$	-		5	mV	
HS transmit differential voltage	$\|V_{OD}\|$	140	200	270	mV	
V_{OD} mismatch when output is Differential-1 or Differential-0	$\|\Delta V_{OD}\|$	-	-	14	mV	
HS output high voltage	V_{OHHS}	-	-	360	mV	
Single ended output impedance		40	50	62.5	Ω	
Single ended output impedance mismatch		-	-	10	%	

Table 21 SLVS DC characteristics

Ta=25°C, power supply voltage: typical if not specified

Item	Symbol	Min	Typ	Max	Unit	Condition
Common-mode voltage	V_{CMTX}	150	-	250	mV	
V_{CMTX} mismatch when output is Differential-1 or Differential-0	$\|\Delta V_{CMTX(1,0)}\|$	-	-	50	mV	
Differential output voltage	$\|V_{OD}\|$	70	-	-	mV	
Single ended high output voltage	V_{OHHS}		-	380	mV	
Single ended low output voltage	V_{OLHS}	40	-	-	mV	
V_{CMTX} mismatch of lane-to-lane		-	-	100	mV	*1

*1: The voltage between the highest V_{CMTX} and the lowest V_{CMTX} among all output lanes.

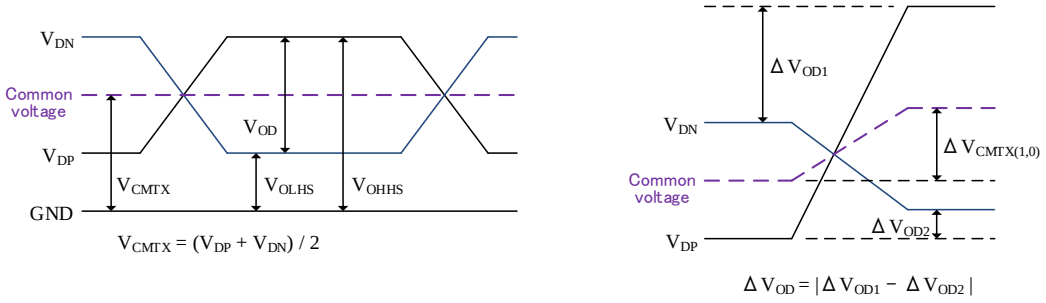


Figure 19 DC characteristics for SLVS and CSI2 High-speed mode

Table 22 MIPI-CSI2 High-speed mode AC characteristics

Ta=25°C, power supply voltage: typical if not specified

Item	Symbol	Min	Typ	Max	Unit	Condition
Output bit rate condition	Bitrate	-	891	-	Mbps	
Data clock frequency	Freq	-	445.5	-	MHz	
Common-level variation	$\Delta V_{CMTX(LF)}$	-	-	25	mV_{PEAK}	
Data to Clock skew	Tskew	-168.4	-	168.4	ps	
Clock jitter		-	-	224.4	ps	*1
20%-80% rise time and fall time	t_R and t_F	-	-	0.3	UI	
		150	-	-	ps	

*1: The value is specified as jitter of unit interval (UI).

Table 23 SLVS AC characteristics

Ta=25°C, power supply voltage: typical if not specified

Item	Symbol	Min	Typ	Max	Unit	Condition
Output bit rate condition	Bitrate	-	891	-	Mbps	
Data clock frequency	Freq	-	445.5	-	MHz	
Eye opening	Teye	0.5	-	-	UI	
20%-80% Rise time	t_R	-	-	0.3	UI	
20%-80% Fall time	t_F	-	-	0.3	UI	

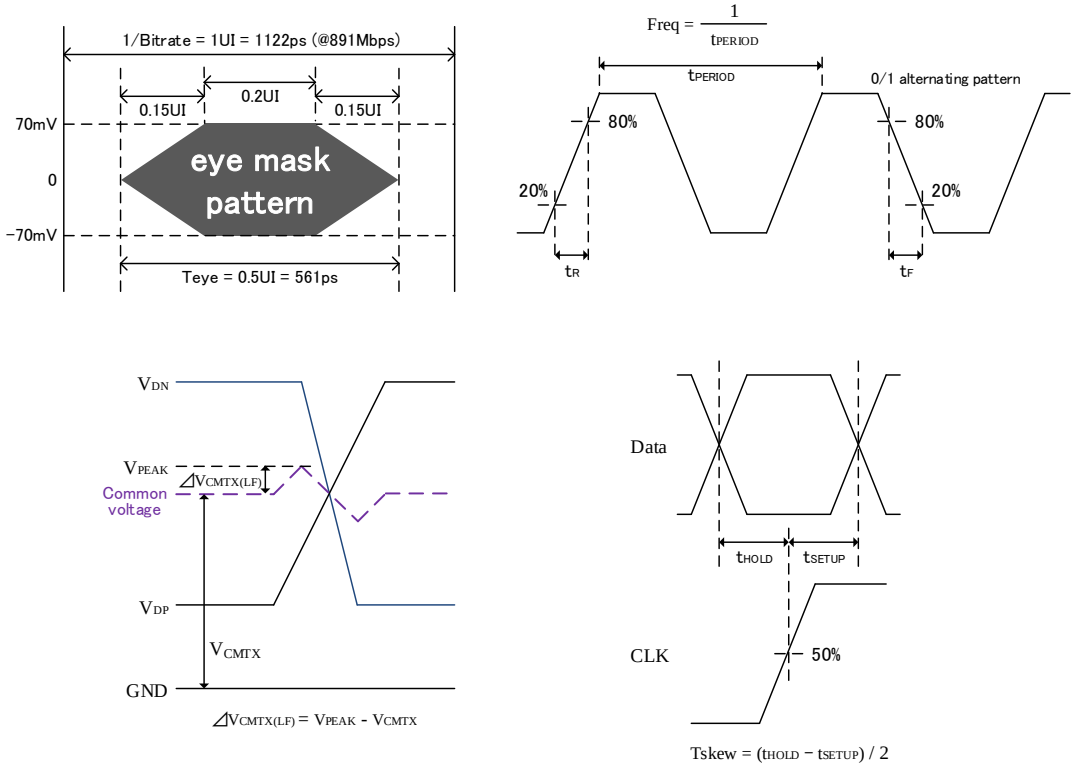


Figure 20 AC characteristics for SLVS and CSI2 High-speed mode

4. Imaging Format

4.1 Read Mode

Table 24 explains the read modes and the maximum frame rates.
- UHD: 3904 x 2224 pixels, Single Exposure.
- UHD-HDR: 3904 x 2224 pixels, Double Exposure (Long exposure & Short exposure, Line by Line).

Each mode, except UHD 10bit mode has two selectable output interfaces, SLVS or MIPI.

Table 24 Read mode

EXP: Exposure, 2: Long & Short,

No.	Read mode	Maximum frame rate [frame/sec]	ADC resolution [bit]	The number of pixels			Output I/F		
				EXP	H	V	Format	Lane	Data rate
1-1	UHD	60	12	1	3904pix.	2224pix.	MIPI-CSI2	8data 1clock	891Mbps
1-2							SLVS		
2-1	UHD	60	10	1	3904pix.	2224pix.	MIPI-CSI2	8data 1clock	891Mbps
3-1	UHD	30	12	1	3904pix.	2224pix.	MIPI-CSI2	4data 1clock	891Mbps
3-2							SLVS		
4-1	UHD	30	12	1	3904pix.	2224pix.	MIPI-CSI2	8data 1clock	445.5Mbps
4-2							SLVS		
5-1	UHD-HDR	30	12	2	3904pix.	2224pix.	MIPI-CSI2	8data 1clock	891Mbps
5-2							SLVS		
6-1	UHD-HDR	15	12	2	3904pix.	2224pix.	MIPI-CSI2	8data 1clock	445.5Mbps
6-2							SLVS		

Figure 21 shows the pixel array structure. 16 pixels in the horizontal invalid area between HOB and Effective, which corresponds to the sum of Invalid Optical Black (6 pixels) and Invalid (10 pixels) depicted in Figure 2, will not be read out. As well as the horizontal invalid areas, 16 pixels in the vertical invalid area between VOB and Effective will not be read out. Therefore, the number of pixels to be read out will be 3904 x 2224.

Regarding to the order of pixels to be read, the first will be the pixel on the lower left corner (Figure 21 Base Point). The next to be read will be the right of the first pixel. In other words, the order of pixels to be read will be rightward from Base Point.

There isn’t the read mode to output only PDAF data without normal image data inside chip.

4.1.2 HDR (Line by Line)

Figure 23 indicates the operation of HDR, which will enlarge the sensor dynamic range. Compared with Frame by Frame HDR, Line by Line HDR will realize small time lag between the long exposure and the short exposure.

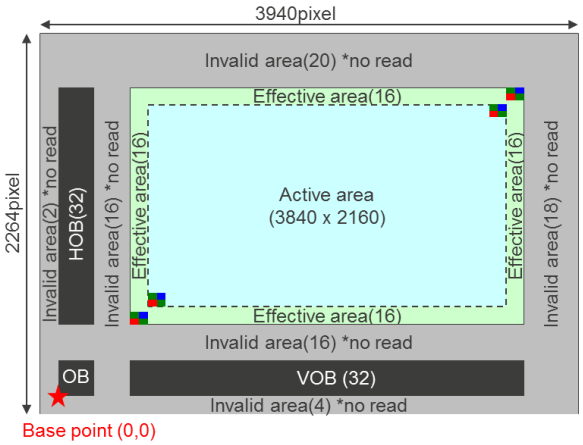


Figure 21 Pixel array structure (Readout area)

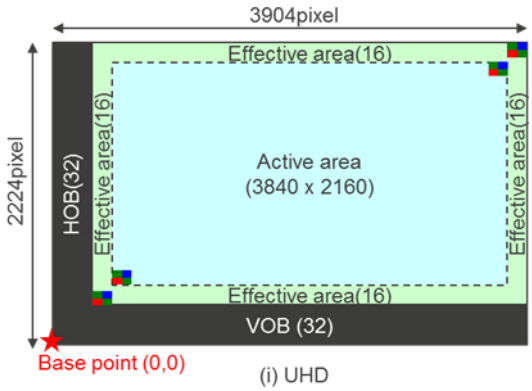


Figure 22 Pixel data

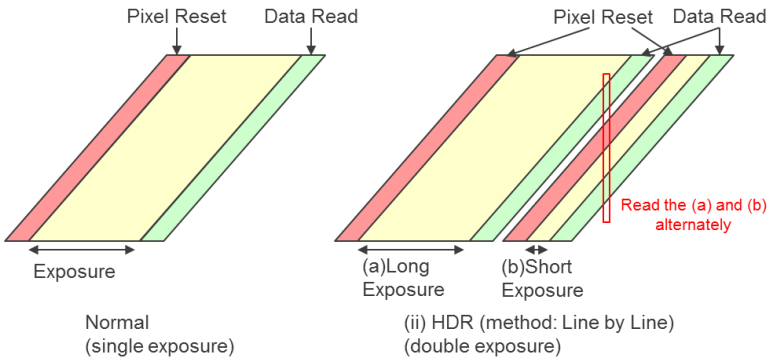


Figure 23 HDR (Line by Line)

4.2 Output I/F Format

4.2.1 Protocol #1 (SLVS)

Figure 24 and Figure 25 shows the data format of source synchronous SLVS. The typical source synchronous clock's rise edge shall be at the center of data [0]. A word consists of 12bit data. A frame consists of pixel data, SOL, SOF, EOL, EOF (synchronous codes), VBLANK and HBLANK (dummy data) as follows.

- SOL: Start of Line
- SOF: Start of Frame
- EOL: End of Line
- EOF: End of Frame
- VBLANK: Vertical Blank
- HBLANK: Horizontal Blank

Be careful that there are eight synchronous codes in case of HDR (long exposure and short exposure).

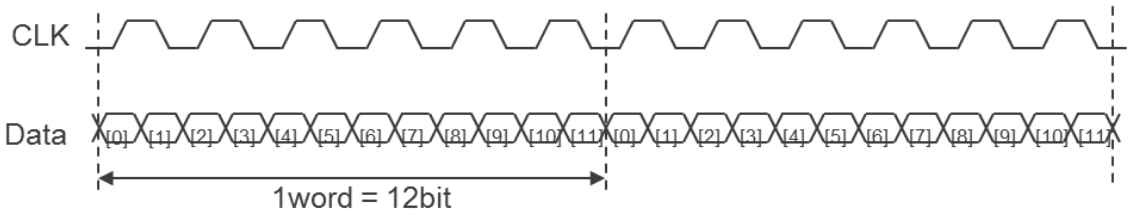


Figure 24 Timing chart of CLK and Data

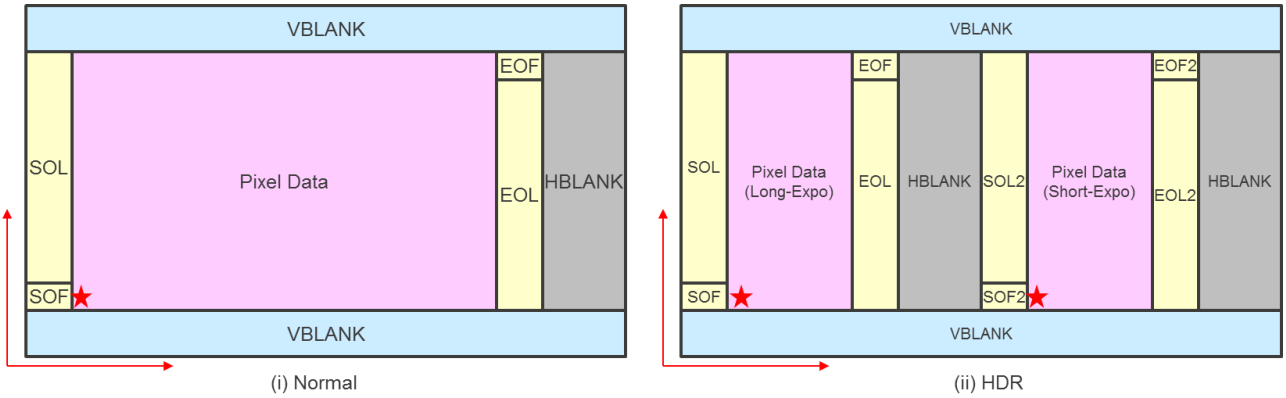


Figure 25 Data format

Table 25 Setting value (Synchronous code and dummy data)

Category	Name	Data	Value (1st_2nd_3rd_4th)	Note
Synchronous code	SOF (start of frame)	4word	FFF_000_000_"XXX"	XXX is set by register
	EOF (end of frame)	4word	FFF_000_000_"XXX"	XXX is set by register
	SOL (start of line)	4word	FFF_000_000_"XXX"	XXX is set by register
	EOL (end of line)	4word	FFF_000_000_"XXX"	XXX is set by register
	SOF2 (start of frame)	4word	FFF_000_000_"XXX"	XXX is set by register
	EOF2 (end of frame)	4word	FFF_000_000_"XXX"	XXX is set by register
	SOL2 (start of line)	4word	FFF_000_000_"XXX"	XXX is set by register
	EOL2(end of line)	4word	FFF_000_000_"XXX"	XXX is set by register
Dummy Data	VBLANK	1word	"XXX"	XXX is set by register
	HBLANK	1word	"XXX"	XXX is set by register

Lane-8	START CODE	OB 7	OB 15	OB 23	OB 31	Gr 39	Gr 47	Gr 55	Gr 63	- - -	Gr 3895	Gr 3903	END CODE	Blank
Lane-7	START CODE	OB 6	OB 14	OB 22	OB 30	R 38	R 46	R 54	R 62	- - -	R 3894	R 3902	END CODE	Blank
Lane-6	START CODE	OB 5	OB 13	OB 21	OB 29	Gr 37	Gr 45	Gr 53	Gr 61	- - -	Gr 3893	Gr 3901	END CODE	Blank
Lane-5	START CODE	OB 4	OB 12	OB 20	OB 28	R 36	R 44	R 52	R 60	- - -	R 3892	R 3900	END CODE	Blank
Lane-4	START CODE	OB 3	OB 11	OB 19	OB 27	Gr 35	Gr 43	Gr 51	Gr 59	- - -	Gr 3891	Gr 3899	END CODE	Blank
Lane-3	START CODE	OB 2	OB 10	OB 18	OB 26	R 34	R 42	R 50	R 58	- - -	R 3890	R 3898	END CODE	Blank
Lane-2	START CODE	OB 1	OB 9	OB 17	OB 25	Gr 33	Gr 41	Gr 49	Gr 57	- - -	Gr 3889	Gr 3897	END CODE	Blank
Lane-1	START CODE	OB 0	OB 8	OB 16	OB 24	R 32	R 40	R 48	R 56	- - -	R 3888	R 3896	END CODE	Blank

Lane-8	START CODE	OB 7	OB 15	OB 23	OB 31	B 39	B 47	B 55	B 63	- - -	B 3895	B 3903	END CODE	Blank
Lane-7	START CODE	OB 6	OB 14	OB 22	OB 30	Gb 38	Gb 46	Gb 54	Gb 62	- - -	Gb 3894	Gb 3902	END CODE	Blank
Lane-6	START CODE	OB 5	OB 13	OB 21	OB 29	B 37	B 45	B 53	B 61	- - -	B 3893	B 3901	END CODE	Blank
Lane-5	START CODE	OB 4	OB 12	OB 20	OB 28	Gb 36	Gb 44	Gb 52	Gb 60	- - -	Gb 3892	Gb 3900	END CODE	Blank
Lane-4	START CODE	OB 3	OB 11	OB 19	OB 27	B 35	B 43	B 51	B 59	- - -	B 3891	B 3899	END CODE	Blank
Lane-3	START CODE	OB 2	OB 10	OB 18	OB 26	Gb 34	Gb 42	Gb 50	Gb 58	- - -	Gb 3890	Gb 3898	END CODE	Blank
Lane-2	START CODE	OB 1	OB 9	OB 17	OB 25	B 33	B 41	B 49	B 57	- - -	B 3889	B 3897	END CODE	Blank
Lane-1	START CODE	OB 0	OB 8	OB 16	OB 24	Gb 32	Gb 40	Gb 48	Gb 56	- - -	Gb 3888	Gb 3896	END CODE	Blank

Figure 26 Lane distribution (UHD, 8-lane)

Lane-5~8 Not use

Lane-4	START CODE	OB 3	OB 7	- - -	OB 31	Gr 35	Gr 39	Gr 43	Gr 47	- - -	Gr 3899	Gr 3903	END CODE	Blank
Lane-3	START CODE	OB 2	OB 6	- - -	OB 30	R 34	R 38	R 42	R 46	- - -	R 3898	R 3902	END CODE	Blank
Lane-2	START CODE	OB 1	OB 5	- - -	OB 29	Gr 33	Gr 37	Gr 41	Gr 45	- - -	Gr 3897	Gr 3901	END CODE	Blank
Lane-1	START CODE	OB 0	OB 4	- - -	OB 28	R 32	R 36	R 40	R 44	- - -	R 3896	R 3900	END CODE	Blank

Lane-5~8 Not use

Lane-4	START CODE	OB 3	OB 7	- - -	OB 31	B 35	B 39	B 43	B 47	- - -	B 3899	B 3903	END CODE	Blank
Lane-3	START CODE	OB 2	OB 6	- - -	OB 30	Gb 34	Gb 38	Gb 42	Gb 46	- - -	Gb 3898	Gb 3902	END CODE	Blank
Lane-2	START CODE	OB 1	OB 5	- - -	OB 29	B 33	B 37	B 41	B 45	- - -	B 3897	B 3901	END CODE	Blank
Lane-1	START CODE	OB 0	OB 4	- - -	OB 28	Gb 32	Gb 36	Gb 40	Gb 44	- - -	Gb 3896	Gb 3900	END CODE	Blank

Figure 27 Lane distribution (UHD, 4-lane)

4.2.2 Protocol #2 (MIPI-CSI2)

This protocol is based on the MIPI CSI2 specification. *MIPI: Mobile Industry Processor Interface Alliance

This protocol has two types of packet structures, Short Packet and Long Packet. For each packet structure, exit from the Low Power State followed by the Start of Transmission sequence indicates the start of the packet. The End of Transmission sequence followed by the Low Power State indicates the end of the packet.

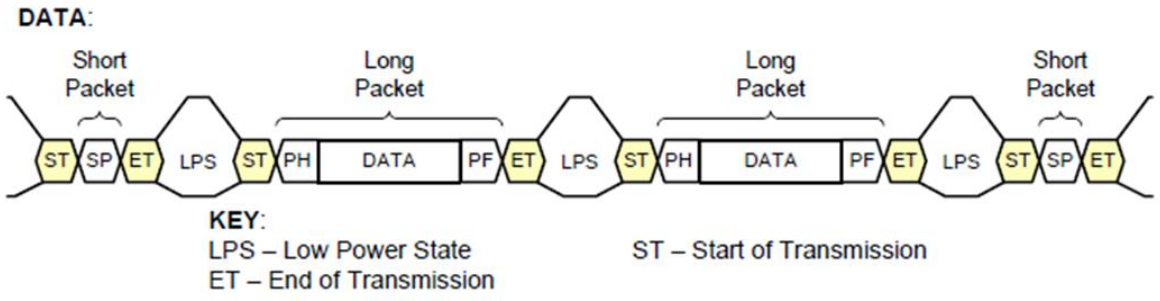


Figure 28 MIPI-CSI2

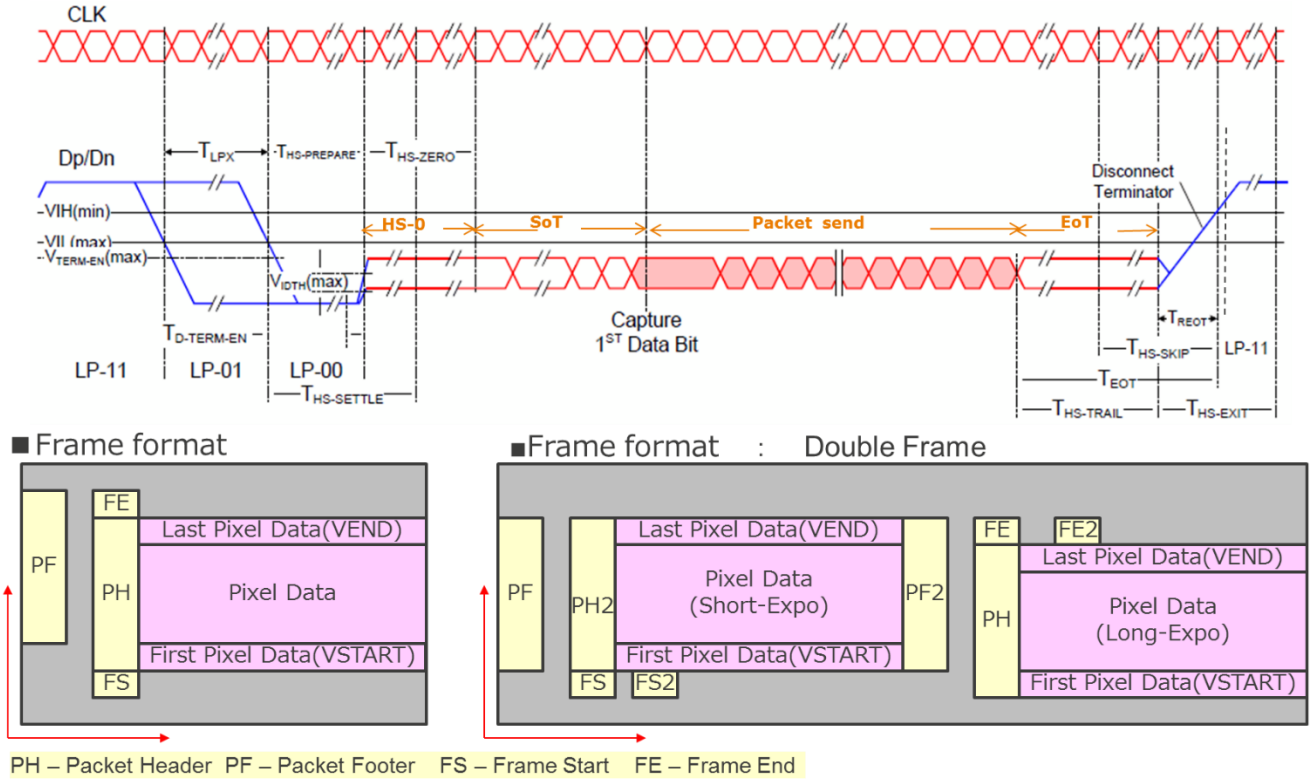


Figure 29 MIPI-CSI2 format

- Structure of Short Packet

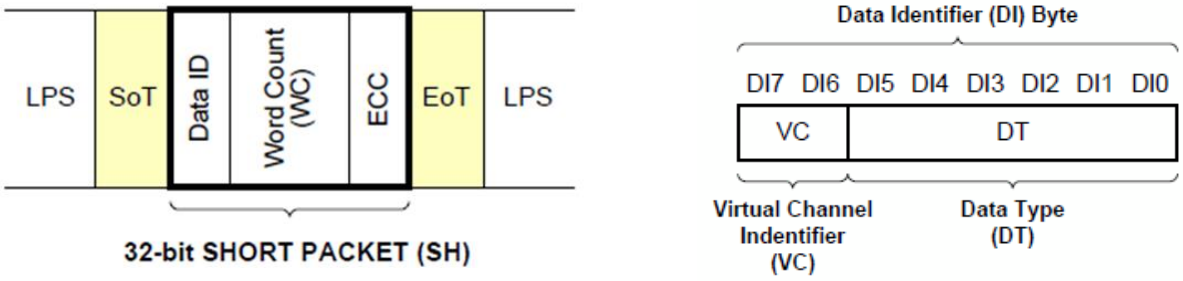


Figure 30 Short packet

- SoT
  Start of Transmission (8bit) = 00011101.

- Data ID
  Data Identifier byte contains Virtual Channel Identifier (2bit) and Data Type (6bit).
  Virtual Channel Identifier allows both long exposure and short exposure images within a single data stream.
  Virtual Channel Identifier = 00 at the long exposure image of HDR mode.
  Virtual Channel Identifier = 01 at the short exposure image of HDR mode.
  Data Type = 000000, when the packet is Frame Start Code.
  Data Type = 000001, when the packet is Frame End Code.

- WC
  Word Count (16bit) = 0x0000.

- ECC
  Hamming-Modified Code (8bit) to correct single-bit error and to detect 2-bit errors in the packet header.

- EoT
  End of Transmission = all one-state, when the last payload data bit is zero-state.
  End of Transmission = all zero-state, when the last payload data bit is one-state.

- Structure of Long Packet

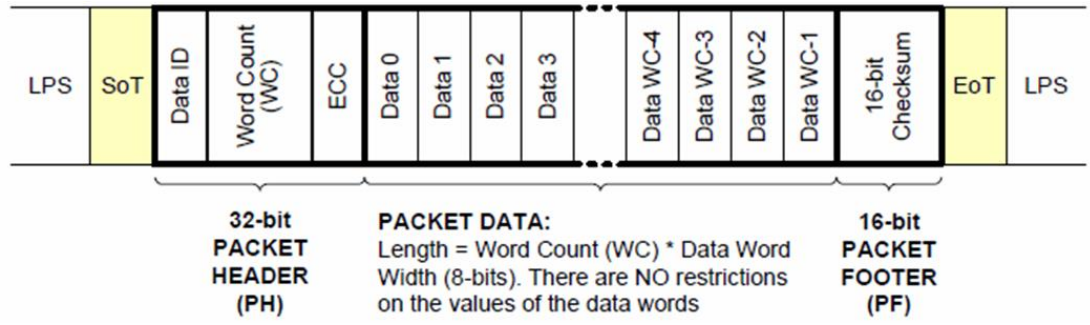


Figure 31 Long packet

- SoT
  Start of Transmission (8bit) = 00011101.

- Data ID
  Data Identifier byte contains Virtual Channel Identifier (2bit) and Data Type (6bit).
  Virtual Channel Identifier allows both long exposure and short exposure images within a single data stream.
  Virtual Channel Identifier = 00 at the long exposure image of HDR mode.
  Virtual Channel Identifier = 01 at the short exposure image of HDR mode.
  Data Type = 101011, when the data format is RAW10.
  Data Type = 101100, when the data format is RAW12.

- WC
  Word Count (16bit) defines the number of 8-bit data words in the payload data.
  Neither the Packet Header nor the Packet Footer is included in the Word Count.

- ECC
  Hamming-Modified Code (8bit) to correct single-bit error and to detect 2-bit errors in the packet header.

- Checksum
  Cyclic Redundancy Code (16bit) to detect possible errors in the payload data.

- EoT
  End of Transmission = all one-state, when the last payload data bit is zero-state.
  End of Transmission = all zero-state, when the last payload data bit is one-state.

- Supported Data Format

➢ RAW10

The transmission of 10-bit Raw Data is done by packing the four 10-bit pixel data to look like 8-bit data format.
1st byte is upper 8-bits of 1st pixel data.
2nd byte is upper 8-bits of 2nd pixel data.
3rd byte is upper 8-bits of 3rd pixel data.
4th byte is upper 8-bits of 4th pixel data.
5th byte is lower 2-bits of 1st, 2nd, 3rd and 4th pixel data.

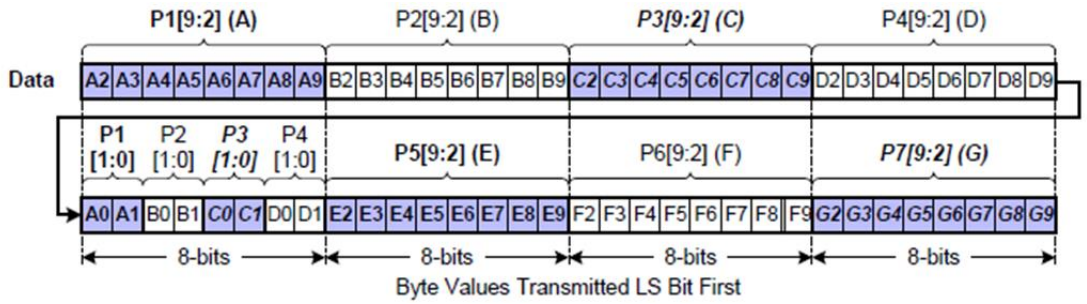


Figure 32 RAW10 format

➢ RAW12

The transmission of 12-bit Raw Data is done by packing the two 12-bit pixel data to look like 8-bit data format.
1st byte is upper 8-bits of 1st pixel data.
2nd byte is upper 8-bits of 2nd pixel data.
3rd byte is lower 4-bits of 1st and 2nd pixel data.

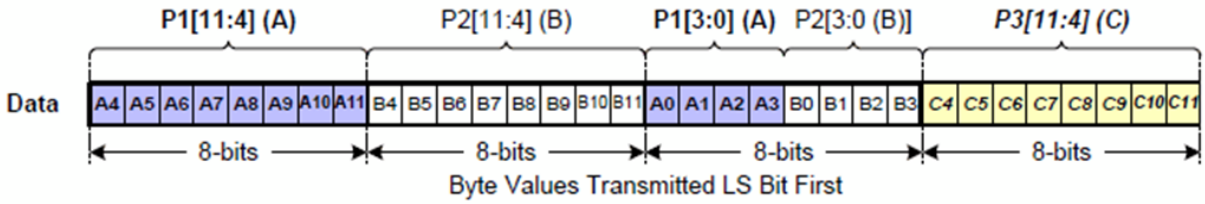


Figure 33 RAW12 format

- Lane Distribution

  4-Lane and 8-Lane system are supported as follows.

Lane-8	SoT 00011101	Pix_2 [11:4]	Pix_6&7 [3:0]x2	Pix_13 [11:4]	----------	Pix_3901 [11:4]	EoT ALL0 / ALL1	
Lane-7	SoT 00011101	Pix_0&1 [3:0]x2	Pix_7 [11:4]	Pix_12 [11:4]	----------	Pix_3900 [11:4]	EoT ALL0 / ALL1	
Lane-6	SoT 00011101	Pix_1 [11:4]	Pix_6 [11:4]	Pix_10&11 [3:0]x2	----------	Pix_3898&3899 [3:0]x2	PF CRC[15:8]	EoT ALL0/ALL1
Lane-5	SoT 00011101	Pix_0 [11:4]	Pix_4&5 [3:0]x2	Pix_11 [11:4]	----------	Pix_3899 [11:4]	PF CRC[7:0]	EoT ALL0/ALL1
Lane-4	SoT 00011101	PH ECC[7:0]	Pix_5 [11:4]	Pix_10 [11:4]	----------	Pix_3898 [11:4]	Pix_3902&3903 [3:0]x2	EoT ALL0/ALL1
Lane-3	SoT 00011101	PH WC[15:8]	Pix_4 [11:4]	Pix_8&9 [3:0]x2	----------	Pix_3896&3897 [3:0]x2	Pix_3903 [11:4]	EoT ALL0/ALL1
Lane-2	SoT 00011101	PH WC[7:0]	Pix_2&3 [3:0]x2	Pix_9 [11:4]	----------	Pix_3897 [11:4]	Pix_3902 [11:4]	EoT ALL0/ALL1
Lane-1	SoT 00011101	PH DI[7:0]	Pix_3 [11:4]	Pix_8 [11:4]	----------	Pix_3896 [11:4]	Pix_3900&3901 [3:0]x2	EoT ALL0/ALL1

Figure 34 UHD RAW12 (8-lane)

Lane-8								
Lane-7								
Lane-6								
Lane-5								
Lane-4	SoT 00011101	PH ECC[7:0]	Pix_2 [11:4]	Pix_5 [11:4]	----------	Pix_3902&3903 [3:0]x2	EoT ALL0 / ALL1	
Lane-3	SoT 00011101	PH WC[15:8]	Pix_0&1 [3:0]x2	Pix_4 [11:4]	----------	Pix_3903 [11:4]	EoT ALL0 / ALL1	
Lane-2	SoT 00011101	PH WC[7:0]	Pix_1 [11:4]	Pix_2&3 [3:0]x2	----------	Pix_3902 [11:4]	PF CRC[15:8]	EoT ALL0/ALL1
Lane-1	SoT 00011101	PH DI[7:0]	Pix_0 [11:4]	Pix_3 [11:4]	----------	Pix_3900&3901 [3:0]x2	PF CRC[7:0]	EoT ALL0/ALL1

Figure 35 UHD RAW12 (4-lane)

5. Sensor Control

5.1 Sequence

Sequence control flow of this device is shown in Figure 36. Figure 37 and Figure 38 shows the power-up and power-down sequence, respectively. Be careful that the output voltage of SACK will follow VDD18, because the power supply of the output buffer is 1.8V power supply voltage. All registers should be written from front to back at the initial power-up sequence. In case of Control Pin CM4W = Low (I2C fast mode / fast mode plus), SCE should keep High drawn by the black lines in Figure 37 and Figure 38 during the serial communication (I2C). In case of Control Pin CM4W = High (4-wire), SCE should become Low drawn by the red lines in Figure 37 and Figure 38 during the serial communication (4-wire). In case of mode change with the output frequency's change, RSTN should be set to Low before register setting (I2C or 4wire).

Table 26 describes the wait time to run Start command after setting all registers. Please take care of the necessary wait time which depends on the serial communication mode. Major registers relating image acquisitions (Frame rate, Exposure time, Gain) should not be changed during the imaging operation.

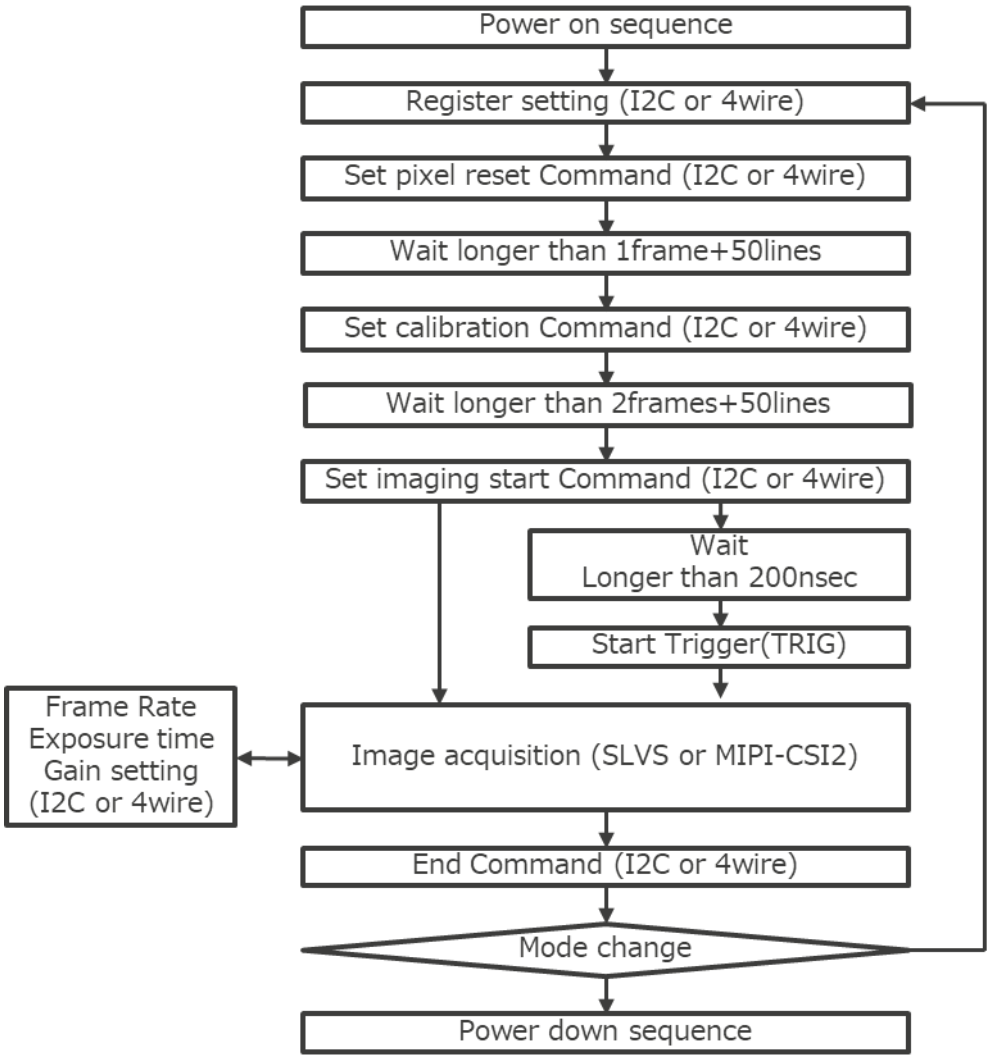


Figure 36 Sequence control flow

Table 26 Wait time between the end of register setting and start command

Serial communication mode	Frequency	Register write time	Wait time
I2C fast mode	400kHz	20.6 ms	0.0ms
I2C fast mode plus	1.0MHz	8.3 ms	8.0ms
4-wire	10MHz	0.8 ms	13.9ms

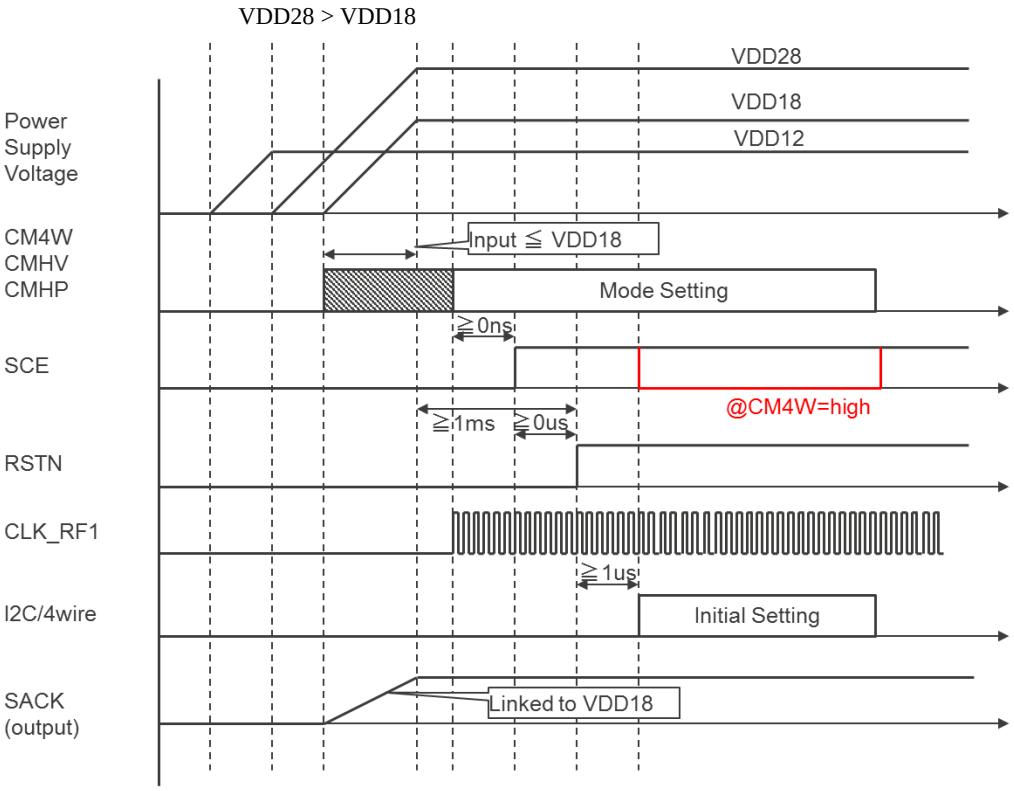


Figure 37 Power-up sequence

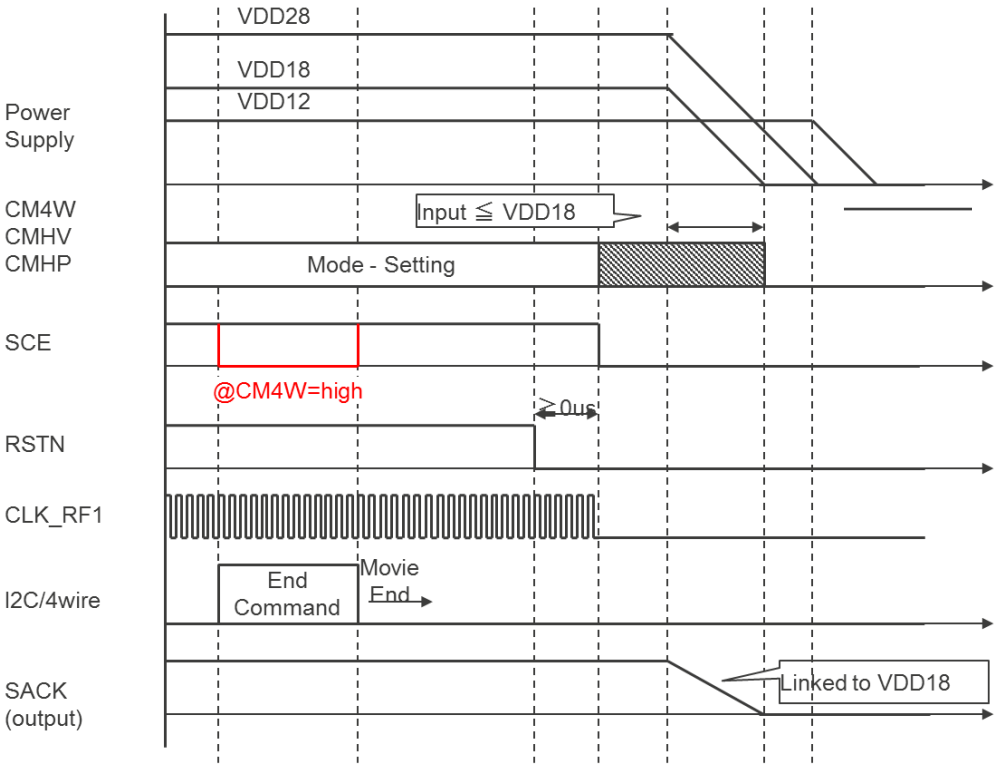


Figure 38 Power-down sequence

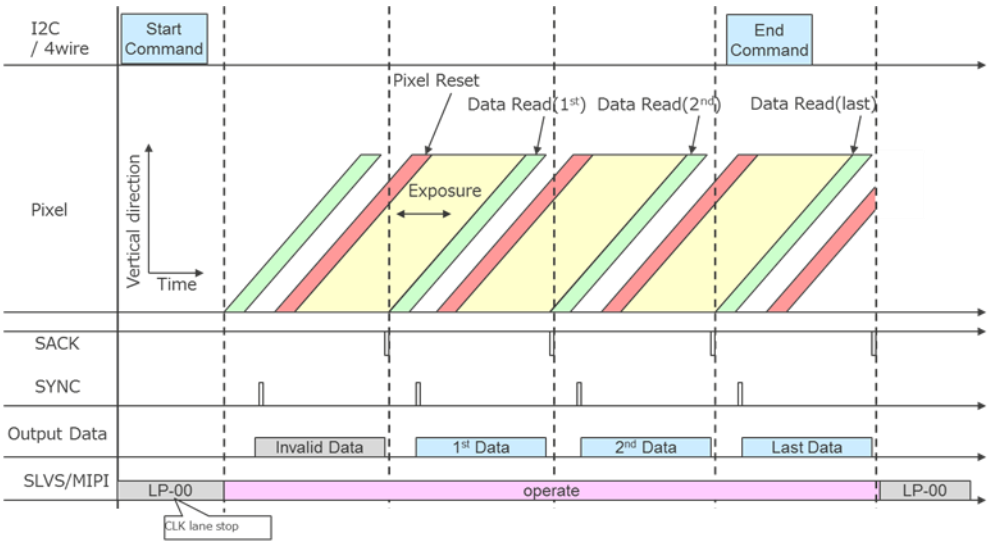


Figure 39 Data acquisition

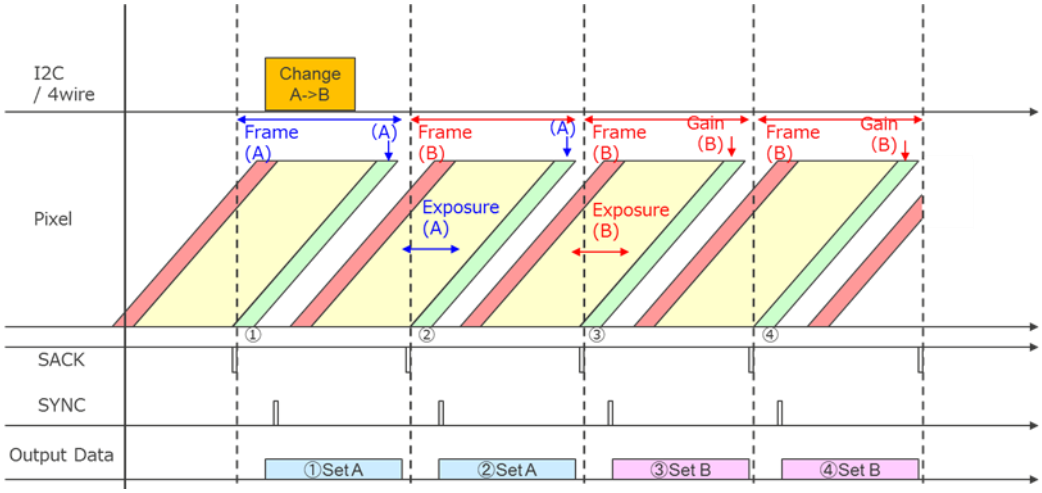


Figure 40 Setting sequence of movie

Table 27 Register setting

Register setting	Setting sequence of movie	Latency from the register setting	Constraint
Frame Rate	Support	After 2frame data	1. Write once at burst mode. 2. Don't write registers while SACK = low. 3. Don't write registers during the next frame after Gain Setting was changed.
Exposure Time	Support	After 2frame data	
Gain	Support	After 2frame data	
HDR: ON/OFF	Not support	-	Hardware reset and initial settings are required
Output Rate(891/445.5 Mbps)	Not support	-	
Output Lane(8/4 lane)	Not support	-	
Format(SLVS / MIPI)	Not support	-	
Other	Not support	-	

5.2 Register Setting

The commonly used registers are introduced in this section.

5.2.1 OPECODE

OPECODE is short for Operation-code.

Table 28 OPECODE

OPECODE	State transition	Note
Start command (self-mode)	Movie start	
Start command (Trigger-mode)	Ready mode	Movie start when TRIG is asserted
End command	Movie end	
Pixel reset command	Idle	
Calibration command	Idle	

5.2.2 Frame Rate Setting

It is possible to set arbitrary frame rate by setting VBLANK period and the exposure time.
- Minimum frame rate = 1fps
- Maximum frame rate = 60fps (Refer Table 24)

5.2.3 Exposure Time Setting

Figure 41 indicates long exposure time and short exposure time for HDR, compared with non-HDR. X-axis is time and Y-axis is horizontal line number of the pixel array. The formula filled in Table 29 explains the possible setting of the exposure time, which will be set by the register “1H_width”.

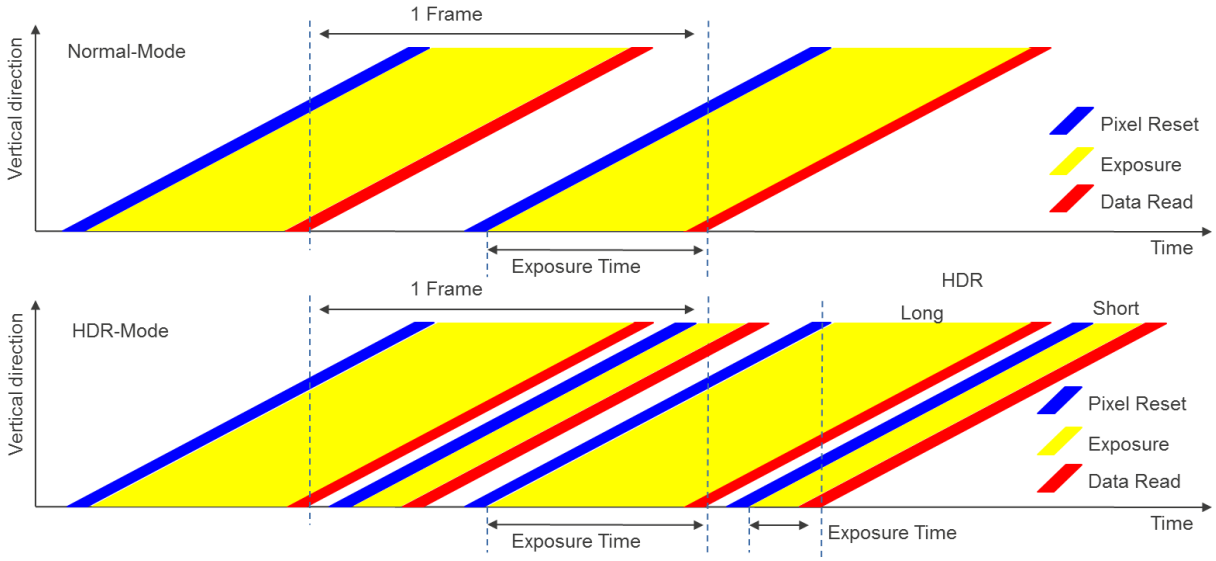


Figure 41 Exposure time

Table 29 Exposure time

1H_width: internal period (7.22us/14.4us)

	Normal	HDR @ long	HDR @ short
Max	1 frame – 8 x1H_width	1 frame – 66 x1H_width	44 x1H_width
Min	4 x1H_with	7 x1H_with	7 x1H_with
Step	1H_width	1H_width	1H_width

5.2.4 Gain Setting

Block diagram (Figure 42) and Gain setting table (Table 30) summarizes how users can set their arbitrary gain.
- Analog Gain (Extract): 1bit register is assigned to select 0dB or 2.44dB.
- Analog Fine Gain (Fine): Two sets of 10bits registers setting provide fine tuning as shown in Figure 44.
- Analog Gain (Coarse): Can be selected 0dB to 12.04dB (6.02dB step) by using 2bits registers.
- Digital Gain (Digital): Can be selected 0dB to 24.08dB (6.02dB step) by using 3bits registers.

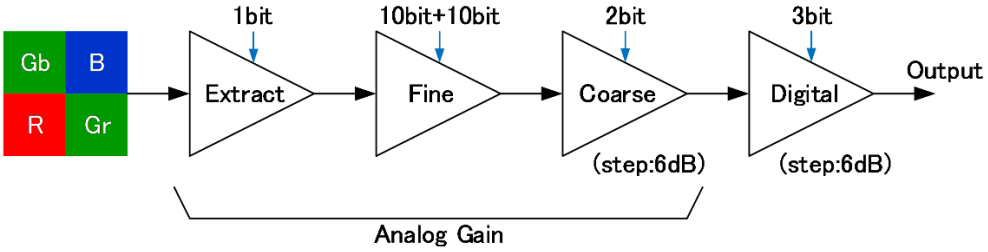


Figure 42 Gain diagram

Table 30 Recommended gain setting (Estimated)

No	Total Gain	Analog Gain			Digital Gain
		Extra	Coarse	Fine	
A	0.00dB ~ 2.44dB	0.00dB	0.00dB	0.00dB ~ 2.44dB	0.00dB
B	2.44dB ~ 6.02dB	2.44dB		0.00dB ~ 3.58dB	
C	6.02dB ~ 12.04dB			3.58dB ~ 9.60dB	
D	12.04dB ~ 18.06dB		6.02dB		
E	18.06dB ~ 24.08dB		12.04dB		
F	24.08dB ~ 30.11dB			9.60dB ~ 15.63dB	
G	30.11dB ~ 36.13dB				6.02dB
H	36.13dB ~ 42.15dB				12.04dB
I	42.15dB ~ 48.17dB				18.06dB
J	48.17dB ~ 54.19dB				24.08dB

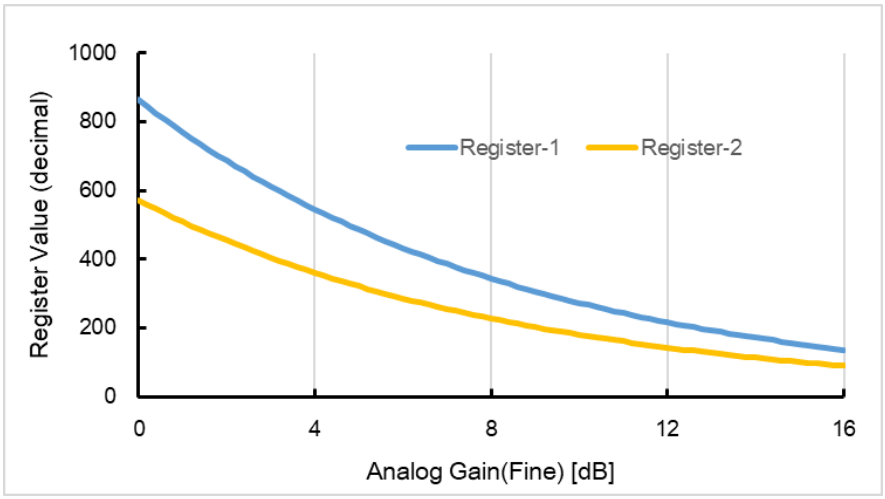


Figure 43 Example of analog gain setting (Fine)

5.3. Serial Communication

There are three types of serial communication modes, I2C fast mode, I2C fast mode plus and 4-wire (Table 31). Each mode can be selected by control pins (CM4W, CMHP and CMHV).

Table 31 Hardware control of serial communication

Serial mode	Drive mode	Hardware control (low=GND, high=VDD18)			Condition of CB			Data control
		CM4W	CMHP	CMHV	VDI @ typ 1.8V	VDI @ typ 2.5V	VDI @ typ 3.3V	sensor control Write (/Read)
I2C fast-mode	Normal	Low	Low	Low	Any	<300pF	<200pF	I2C
	High			High	-	>300pF	>200pF	
I2C fast-mode plus	Normal		High	Low	Any	<300pF	<200pF	
	High			High	-	>300pF	>200pF	
4-wire	-	High	Low	Low	-	-	-	4wire

Table 32 Serial communication setting and control

Item	I2C	4-wire
Identification code	Slave address: 7b'0110110	ID: 7b'00000001
Read/Write selection	0:write 1:read	0:write 1:read
Register address	Sub address 16bit	Base address 16bit
Data-unit	2-address=16bit, MSB-first	2-address=16bit, MSB-first
Address access control	Even number only	Even number only
Max data rate	400kHz(fast mode) 1MHz(fast mode plus)	10.8MHz
Pin information	SDA: input/output data SCL: clock	SCE : enable SDI : input data SCK : clock SDO : output data
Control condition	Start : fall of SDA when SCL is high Repeat start : same of "start" End : rise of SDA when SCL is high CM4W=low : read / write CM4W=high: no use	Enable : SCE is low Disable : SCE is high CM4W=low: read only CM4W=high: read / write
Burst mode	Continuous writing or reading Access address is incremented by 2	

Table 33 Register map

Address (hex)	Category	During imaging	Type	Note
0000	Sensor control	Write enable	Normal	OPECODE
0002 ~ 0004	Sensor control	Don't access	Normal	
0006 ~ 0036	Sensor control	Write enable	Normal	Exposure
0038 ~ 038E	Sensor control	Don't access	Normal	
0390 ~ 04A0	Test data	Don't access	Read only	

5.3.1 I2C Serial Communication Protocol

An example of I2C serial communication is shown below. The serial communication can't abort until sending all necessary data.

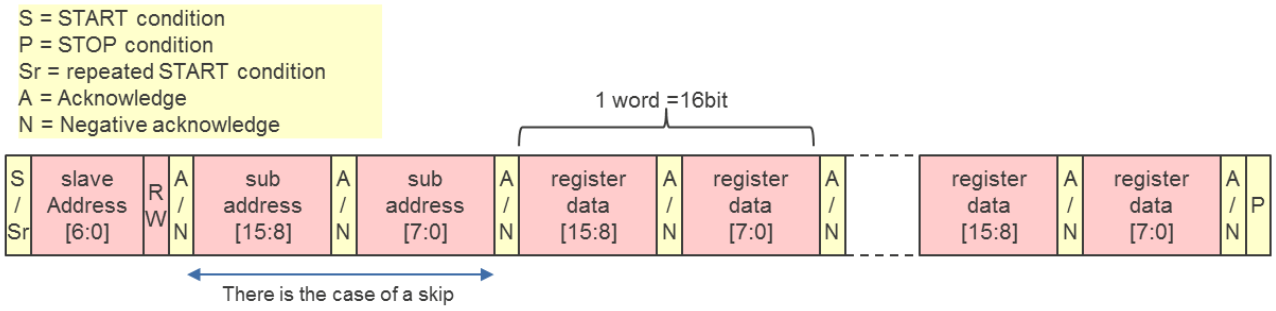


Figure 44 I2C format

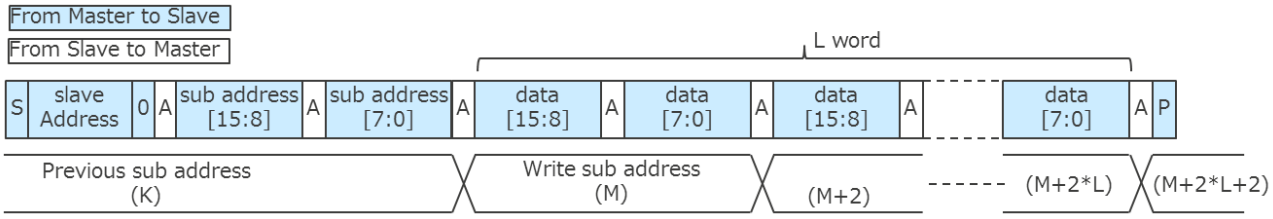


Figure 45 Example of sequential write

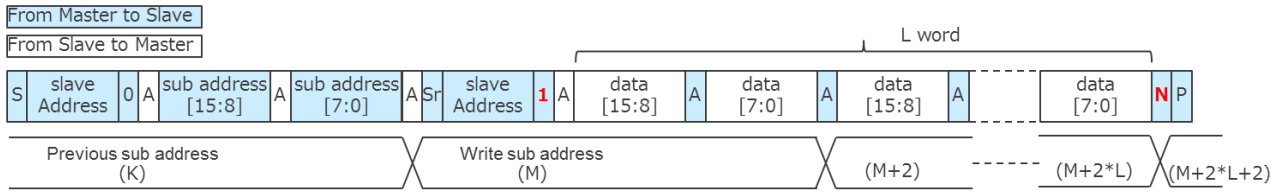


Figure 46 Example of sequential read (Random access)

5.3.2 4-wire Serial Communication Protocol

An example of 4-wire serial communication is shown in Figure 47. While SCE is low, the serial communication will be enabled, and can't abort until sending all necessary data.

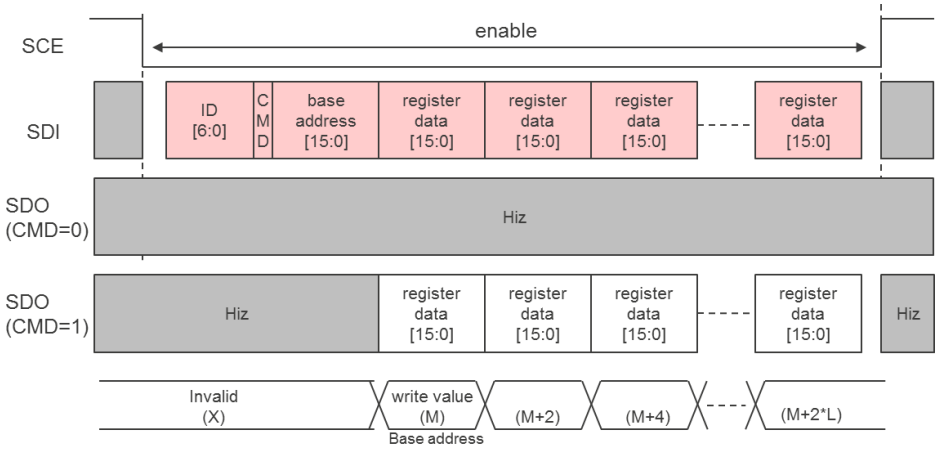


Figure 47 4-wire format

Revision History	RAA462113FYL Data Sheet

Rev.	Date	Description	
		Page	Summary
0.01	Jan. 7. 2020		Preliminary Version
0.02	Jun 4. 2020	1	Table 1 Features: Removed AF Assist function. Removed “assist data update” comment in Output sync
		2	Figure 1; error correction MIPI CIS2 -> MIPI CSI2
		3	Add PDAF pixel coordinates (Figure 3).
		12	Error correction 1 block is 8080 or 96×96 pixels or 96×80 or 80×96. ->1 block is 80×80, 96×96, 96×80 or 80×96 pixels.
		13	Add a note in sensor characteristics of PDAF Pixels Add specification limit of Sensitivity ratio L-open/R-open Add specification of PDAF Sensitivity.
		14	Update spectral characteristics graph. Add Note: change possibility of spectral characteristics.
		15	Table 11; Pixel defect specifications Defined # of PDAF spot defect. Table 11; Shine spot defect at Dark (PDAF) Table 11; add PDAF defect in each 16 x 8 PDAF pixel region
		17	Modify Table 12, Table 13 and Figure 12. Add Table 14 and Figure 13.
		24	Add comment for a read mode to output only PDAF data.
		35	Table 27; Removed Assist function.
		-	Remove Assist function.
		-	Renumbering Table and Figure.
0.03	Dec. 23. 2020	2	Modify Figure 1.
		4	Modify Figure 4.
		14	Update spectral characteristics graph.
		23	Change the specifications of Data to Clock skew and Clock jitter of MIPI and SLVS AC characteristics.
		33	Remove comment on AF assist function in section 5.1. Remove Assist function in Figure 36.
		35	Remove Assist function in Figure 39 and Figure 40.
		38	Remove comment on AF assist function in section 5.3. Remove AF assist function in Table 31 and Table 33
1.00	Feb. 15. 2021	13	Change the specification of sensitivity ratio L-open/R-open.

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(Rev.5.0-1 October 2020)

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