RAA2S4252B

Automotive Sensor Signal Conditioner with Analog Output

Description

The RAA2S4252B is a member of Renesas' family of CMOS integrated circuits for highly accurate amplification and sensor-specific correction of differential bridge sensor signals. Featuring a maximum analog pre-amplification of 900 with analog sensor offset correction (XSOC), the RAA2S4252B is adjustable to nearly all resistive bridges.

Conditioning calculation is accomplished via a 16-bit RISC microcontroller. Calibration coefficients and configuration data are stored in the non-volatile memory (NVM), which is reliable in automotive applications.

Measured values are provided via a ratio-metric analog output signal. End-of-line calibration is also supported through this output pin via a One-Wire Interface (OWI). Digital calibration helps keep assembly cost low as no trimming by external devices or lasers is needed.

The RAA2S4252B is optimized for harsh automotive environments by over-voltage and reverse polarity protection circuitry, excellent electromagnetic compatibility, and multiple diagnostic features.

Typical Applications

- Pressure sensing in hydraulic and pneumatic systems
- HVAC pressure measurement
- Differential and single ended bridge sensor readout

Available Support

- Evaluation Kit
- Application Notes
- Calculation Tools

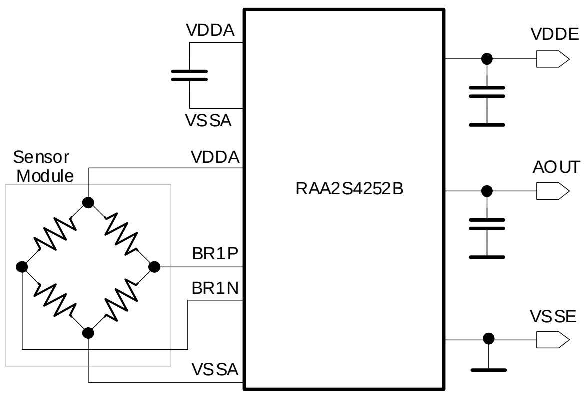
Features

- Differential bridge sensor input with selectable on-chip or external PN-junction temperature sensor
- 0.5mV/V to 800mV/V sensor span with 12 to 18bit resolution; supported sensor offset/span ratio of 10
- Compensation for offset, gain, and higher order nonlinearity as well as for temperature coefficients of measured bridge sensor input signal
- Accuracy: 1% full scale (FS) at -40°C to 150°C
- Third order digital LPF with cut-off frequency of 10Hz to 1000Hz, and configurable transfer characteristic
- One-pass, end-of-line calibration algorithm minimizes production costs: fast in calibration. Statistical based temperature calibration point minimization is supported.
- Minimum amount of external components enables design of sensor modules with best-in-class form factor
- Qualified according to AEC-Q100 Grade 0; operating temperature range: -40°C to 150°C

Physical Characteristics

- Operation supply: 4.5V to 5.5V
- Protection up to ±40V; robust in automotive environment
- Output resolution: 12-bit analog output; signed 16-bit readout for raw data acquisition
- Package: 8-SOIC (4.9mm × 3.9mm)

RAA2S4252B Basic Circuit



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1. Pin Assignments

The RAA2S4252B is available in an 8-SOIC (4.9mm × 3.9mm) RoHS-conformant package.

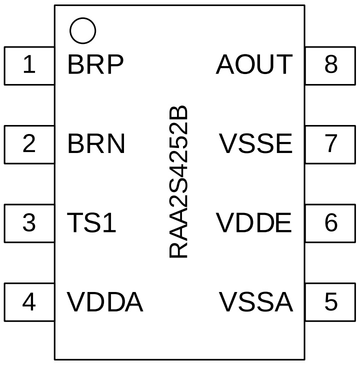


Figure 1. Pin Assignments for 4.9mm × 3.9mm 8-SOIC – Top View

2. Pin Descriptions

Table 1. Pin Description

8-SOIC Pin #	Pin Name	Type	Description
1	BRP	Analog	Positive bridge sensor input
2	BRN	Analog	Negative bridge sensor input
3	TS1	Analog	External temperature sensor input 1
4	VDDA	Supply	Internal supply and positive bridge supply voltage
5	VSSA	Ground	Internal ground and negative bridge supply voltage
6	VDDE	Supply	External supply
7	VSSE	Ground	External ground
8	AOUT	Analog	Analog output and One-Wire Interface (OWI) input/output

3. Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the RAA2S4252B at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions might affect device reliability. In addition, extended exposure to stresses above the operating conditions given in section 4 might affect device reliability.

See section 7.9 for information about over-voltage protection, reverse-polarity, and short-circuit protection.

Table 2. Absolute Maximum Ratings

Requirement	Parameter	Symbol	Conditions	Min	Max	Unit
DS_001	Supply voltage	V_{DDE_MAX}	$V_{DDE} = V_{VDDE} – V_{VSSE}$	-40	40	V
DS_002	Voltage at AOUT pin	V_{AOUT_MAX}	To VSSE	-40	40	V
DS_003	Pin voltage difference	V_{PIN_MAX}	Voltage between any two of these pins: VDDE, AOUT and VSSE	-40	40	V
DS_004	Analog supply voltage	V_{DDA_MAX}	$V_{DDA} = V_{VDDA} – V_{VSSA}$; on-chip controlled voltage; do not supply externally	-0.3	6.0	V
DS_005	Voltage at all other pins	V_{PIN}	Maximum voltage is V_{VDDA} + 0.3V	-0.3	6.0	V
DS_006	Junction temperature	T_J		-40	160	°C
DS_007	Storage temperature	T_{STG}		-55	165	°C

4. Operating Conditions

The operation conditions in Table 3 specify the conditions that the application circuit must provide to the device in operation for proper function. Unless otherwise stated, the parameter limits in this section are applied as test conditions for the electrical parameters specified in sections 5.

Table 3. Operating Conditions

Requirement	Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DS_050	Supply voltage	V_{DDE}	$V_{DDE} = V_{VDDE} – V_{VSSE}$	4.5	5	5.5	V
DS_051	Ambient temperature [3] [7] [8]	T_{AMB_TQE}	Extended Temperature Range (TQE)	-40		150	°C
		T_{AMB_TQA}	Advanced-Performance Temperature Range (TQA)	-40		125	°C
Informational	Thermal resistance SOIC8 [1] [4] [5]	R_{th_SOIC8}	According to JESD 51		93		K/W
DS_052	Bridge resistance [1] [2] [6]	R_{BR}	Output range 5% to 95%	2		15	kΩ
		$R_{BR\_10\text{-}90}$	Output range 10% to 90%	1		15	kΩ

[1] No measurement in mass production; parameter is guaranteed by design and/or quality observation.

[2] R_{BR} up to 22kΩ is allowed but may result in higher noise

[3] Temperature stress over lifetime is restricted to temperature profiles that are equivalent to the HTOL qualification described in section 11.

[4] Assuming application conditions according to test board design as per JESD51-7 and natural convection test conditions as per JESD51-2.

[5] Package-related parameter.

[6] Symmetric behavior and identical electrical properties (including the low-pass characteristic) of the differential bridge sensor inputs are required. Unsymmetrical conditions of the sensor and/or external components connected to the sensor input pins can generate a failure in signal operation.

[7] Definition of ambient temperature according to JESD 402-1.

[8] The end user of RAA2S4252B determines the exact worst case condition of the junction temperature in the field of operation. It is recommended to perform a thermal simulation of the module integrating the RAA2S4252B if the effective context of use is significantly different than the ones stated in this datasheet.

5. Electrical Parameters

Unless otherwise defined, all parameters are related to the device itself, and are valid for the operating conditions specified in section 4. All internal voltages are referenced to VSSA.

The following parameters are specified based on a RAA2S4252B main channel configuration setup using:

- PGA gain of <200
- Resulting ADC input range usage of ≥ 50% full scale.
- ADC resolution of >14 bits,
- 2-step A/D conversion scheme using AdcMsbRsl ≥8 and AdcLsbRsl ≥6 bits
- ADC clock frequency of nominal 1MHz (first step) / 2MHz (second step).

Table 4. Electrical Parameters

Note: See important table notes at the end of the table.

№	Parameter	Symbol	Descriptions/Conditions	Min	Typ	Max	Unit
Supply Current and System Operation Conditions							
DS_100	Supply current [1]	I_S	f_{OSC}=8MHz		5	7	mA
DS_102	Oscillator frequency	f_{OSC}	Calibrated	7.2	8.0	8.8	MHz

№	Parameter	Symbol	Descriptions/Conditions	Min	Typ	Max	Unit
DS_103	Oscillator frequency, advanced	$f_{OSC;adv}$	Calibrated	10.5	12.0	13.5	MHz
DS_104	Bridge sensor supply voltage	V_{SENS}	$V_{SENS} = V_{TOP} - V_{BOT}$ where: V_{TOP}: voltage at internal TOP pin V_{BOT}: voltage at internal BOT pin TOP and BOT are internally connected to VDDA and VSSA.	0.9		1	V_{DDA}
Informational	Analog supply voltage	V_{DDA}	Do not supply V_{DDA} externally. Note: V_{DDA} is limited if V_{DDE} exceeds the threshold of $V_{OV\_LIM\_TH}$	0.925			V_{DDE}
Analog Front-End Characteristics							
DS_120	Differential input span[5][6]	V_{IN_SPAN}	Analog gain: 1…912	0.5		800	mV/V
DS_121	Differential input offset cancellation range	$V_{IN\_OFFS\_XSOC}$	Including Extended Sensor Offset Compensation (XSOC); Depends on gain adjust; see section 7.4.5.	-1000		1000	% V_{IN_SPAN}
DS_122	Input voltage range	V_{IN_RNG1}	Analog gain = 1; corresponds to V_{ADC_IN}	0.05		0.95	V_{SENS}
DS_123		V_{IN_RNG2}	Analog gain = 3 to 912	0.3		0.65	V_{DDA}
DS_124	Settling time at input pins [2]	LTC	For calculation of the capacitance either between pins BRP, BRN to VSSA or between BRP and BRN see section 9. Settling time is dependent on the configuration settings		75		µs
A/D Conversion Refer to section 7.4.6.							
DS_130	ADC resolution [2]	r_{ADC}		12		18	Bit
DS_131	ADC input range [2]	V_{ADC_IN}		0.05		0.95	V_{SENS}
DS_132	DNL [2]	DNL_{ADC}	Best fit; overall AFE; V_{ADC_IN} according to DS_131			0.95	LSB
DS_133	INL	INL_{ADC_TQA}	Best fit, temperature range TQA [2], nominal MSB clock ≤1MHz			5	LSB_{14}
			Best fit, temperature range TQA [2]			10	LSB_{14}
DS_134	INL	INL_{ADC_TQE}	Best fit, temperature range TQE, nominal MSB clock ≤1MHz			8	LSB_{14}
			Best fit, temperature range TQE			15	LSB_{14}
Temperature Measurement Refer to section 7.3.2.							
Informational	On-chip Proportional-to-Absolute Temperature (PTAT) measurement range [2]	OPR_{TS}	Important: This range exceeds operating conditions for junction temperature T_{J_ABS}.	-60		200	°C
DS_140	On-chip PTAT measurement sensitivity	ST_{TSI}		20			LSB /K
DS_141	External temperature diode gain	A_{TSE_D}		25			LSB /mV
DS_142	External temperature diode bias current	I_{TSE_D}	Selectable nominal values: 20µA and 100µA	10		150	µA
DS_143	External temperature diode input range [2]	V_{TSE_D}	Related to VDDA	-1		-0.2	V

№	Parameter	Symbol	Descriptions/Conditions	Min	Typ	Max	Unit
Bridge Sensor Diagnostic Tasks							
DS_151	Sensor connection loss detection threshold [2]	R_{SCC}	Covered by fault check BRSC2. Threshold can be adjusted.	40		300	kΩ
DS_152	Sensor short detection threshold [2]	R_{SSC}	Covered by fault check BRSC. Threshold can be adjusted.	50		1000	Ω
DAC and Analog Output (Pin AOUT)							
DS_160	Analog Output Range	$AOUT_{RNG}$	R_{LOAD} ≥ 2kΩ R_{LOAD} ≥ 1kΩ	5 10		95 90	$\%V_{DDE}$
DS_161	DAC resolution [2]	r_{DAC}	Analog output		12		Bit
DS_162	Output current sink/source	$\lvert I_{OUT\_SRC/SINK} \rvert$	V_{AOUT}: 5-95%, R_{LOAD} ≥ 2kΩ			2.75	mA
DS_163			V_{AOUT}: 10-90%, R_{LOAD} ≥ 1kΩ			5.5	mA
DS_164	Absolute output current driving capability [2] [3]	I_{OUT_LIM}	AOUT connected to VSSE or VDDE with OutbufCurLimGndAdj = 0	3.75			mA
DS_165	Absolute short-circuit current [3]	$\lvert I_{OUT\_SHRT} \rvert$	AOUT connected to VSSE or VDDE with OutbufCurLimGndAdj = 3			30	mA
DS_170	Output slew rate [2]	SR_{OUT}	C_{LOAD} < 50nF	0.1			V/µs
DS_171	Output resistance in Diagnostic Mode [2]	R_{OUT_DIA}	Diagnostic Range: < $4\%V_{DDE}$ for R_{LOAD} ≥ 2kΩ < $8\%V_{DDE}$ for R_{LOAD} ≥ 1kΩ			80	Ω
DS_172	DNL	DNL_{OUT}	r_{DAC} =12bit (in Analog Output Range $AOUT_{RNG}$)			0.99	LSB
DS_173	INL @ TQA [2]	INL_{OUT_TQA}	Best fit, r_{DAC} = 12bit (in Analog Output Range $AOUT_{RNG}$)			5	LSB
DS_174	INL @ TQE	INL_{OUT_TQE}	Best fit, r_{DAC} = 12bit (in Analog Output Range $AOUT_{RNG}$)			8	LSB
DS_250	AOUT leakage current in TQA [2]	$I_{AOUT\_VSSELOSS\_TQA}$	Pull-down resistor at ECU side. The SSC is disconnected from VSSE	-15		0.1	µA
DS_251		$I_{AOUT\_VDDELOSS\_TQA}$	Pull-up resistor at ECU side. The SSC is disconnected from VDDE	-0.1		7.5	µA
DS_252	AOUT leakage current in TQE	$I_{AOUT\_VSSELOSS\_TQE}$	Pull-down resistor at ECU side. The SSC is disconnected from VSSE.	-20		0.1	µA
DS_253		$I_{AOUT\_VDDELOSS\_TQE}$	Pull-up resistor at ECU side. The SSC is disconnected from VDDE.	-0.1		10	µA
System Response							
DS_180	Startup time [2]	$t_{STARTUP}$	Time to first valid output after power-on; V_{DDE} slew rate > 0.1V/µs			5	ms
DS_181	Output update rate [2]	OUR	depends on configuration		1.25	10	kHz
DS_182	Bandwidth [2]	BW	66% step response			3	kHz
DS_184	Failure messaging time [2]	FMT	Time between occurrence of a failure event and reporting on analog output assuming one failure confirmation, main-to-auxiliary measurement ratio equal to one. Depends on configuration			20	ms
DS_185	Analog output noise peak-to-peak [2]	$V_{NOISE,PP}$	DAC and output buffer only; bandwidth ≤ 10kHz			10	mV

№	Parameter	Symbol	Descriptions/Conditions	Min	Typ	Max	Unit
DS_186	Analog output noise RMS [2]	$V_{NOISE,RMS}$	DAC and output buffer only; bandwidth ≤ 10kHz			3	mV
DS_187	Ratiometricity error [2]	$RE_{OUT\_0.5}$	Maximum error (@ V_{DDE} = 5V +/- 0.5V)	-1000		1000	ppm
DS_188	Ratiometricity error [2]	$RE_{OUT\_0.25}$	Maximum error (@ V_{DDE} = 5V +/- 0.25V)	-500		500	ppm
DS_189	Deviation from calibrated and temperature compensated output characteristic including INL, gain, offset, and temperature impacts; excluding sensor caused effects [2] [4]	F_{ALL}	Temperature range TQA			0.5	% FSO
			Temperature range TQE			1.0	
Power Management							
DS_210	Power-on threshold	V_{PWR_ON}		3.3		3.9	V
DS_211	Power-off threshold	V_{PWR_OFF}		3.0		3.6	V
DS_212	Power-on reset hysteresis [2]	V_{POR_HYST}			0.4		V
DS_213	Over-voltage switch-off threshold [2]	V_{OV_DISC}		8		15	V
DS_214	Over-voltage switch-off delay [2]	t_{OV_DISC}				10	ms
DS_215	Over-voltage limitation threshold	$V_{OV\_LIM\_TH}$	Limitation threshold of internal supply voltage in case of over-voltage	5.55	5.8	6.0	V
DS_216	Over-voltage power consumption [1] [2]	P_{OV}	5.5V < V_{DDE} < 40V			250	mW

[1] Excluding bridge supply current and excluding output current at AOUT pin.

[2] No measurement in mass production; parameter is guaranteed by design and/or quality observation.

[3] Nominal analog output current limitation is adjustable between 7.5mA and 20mA.

[4] Full-scale output (FSO). No sensor-caused effects included in overall error. ADC input range from 10% to 90% of VSENS; DAC from 5% to 95% of output range.

[5] Using 0.5mV/V includes digital processing by the SSC

[6] Using 800mV/V requires input impedance to be less than 20kΩ

6. Interface Characteristics and Non-volatile Memory

Table 5. Interface Characteristics and Non-volatile Memory

Requirement	Parameter	Symbol	Descriptions/Conditions	Min	Typ	Max	Unit
ZACwire™ One-Wire Interface (OWI)							
DS_220	Start window [1]	$t_{OWI\_STARTWIN}$	V_{DDE} slew rate > 0.1V/µs	100	225	350	ms
DS_221	Communication start time [1]	t_{COMM_STRT}	V_{DDE} slew rate > 0.1V/µs; time to be ready for communication after power-on			4	ms
DS_222	Bit time [1]	$t_{OWI\_BIT\_NL}$	No output load	0.02		4	ms
		t_{OWI_BIT}	10nF ≤ C_{LOAD} ≤ 100nF	1		4	ms
DS_223	OWI input voltage level HIGH [1]	$V_{OWI\_IN\_H}$	Master to slave	0.8			V_{DDE}
DS_224	OWI input voltage level LOW [1]	$V_{OWI\_IN\_L}$	Master to slave			0.2	V_{DDE}
DS_225	OWI output level LOW [1]	$V_{OWI\_OUT\_L}$	I_{OL} ≤ 2mA			0.1	V_{DDE}
Non-volatile Memory (NVM)							
DS_230	Junction temperature for NVM programming [2]	T_{JUN_NVM}		-40		150	°C
DS_231	Re-write cycles	N_{NVM}		100			cycle
DS_233	Data retention [1]	t_{NVM_RET}	Operation conditions over lifetime must comply with the temperature profile [3]	15			years
DS_234	Programming time [1]	t_{NVM_WRI}	Per programmed data word		3	6	ms

[1] No measurement in mass production; parameter is guaranteed by design and/or quality observation.

[2] Consider additional package and temperature range restrictions.

[3] Over lifetime and valid for the dice. Note that package can cause additional restrictions.

7. Circuit Description

7.1 General Operation Description

The RAA2S4252B is a sensor signal conditioner (SSC) for highly accurate amplification and sensor-specific correction of resistive bridge sensors. Digital compensation of sensor offset, sensitivity, temperature drift, and non-linearity is accomplished via an internal 16-bit RISC microcontroller running a ROM based correction algorithm with calibration coefficients stored in an NVM.

The RAA2S4252B is adjustable to nearly all resistive sensor element types. Measured values are provided at the analog voltage output. The digital one-wire interface (OWI) can be used for a simple PC-controlled calibration procedure in order to program a set of calibration coefficients into an on-chip NVM. The specific sensor element and the RAA2S4252B can be quickly calibrated together. The RAA2S4252B and the calibration equipment communicate digitally, so the noise sensitivity is greatly reduced. Digital calibration helps keep assembly cost low as no trimming by external devices or lasers is needed.

The RAA2S4252B is optimized for automotive environments by over-voltage and reverse-polarity protection circuitry, excellent electromagnetic compatibility, full automotive temperature range, and multiple diagnostic features.

Figure 2 provides a block diagram of the RAA2S4252B. Refer to section 15 for definitions of abbreviations.

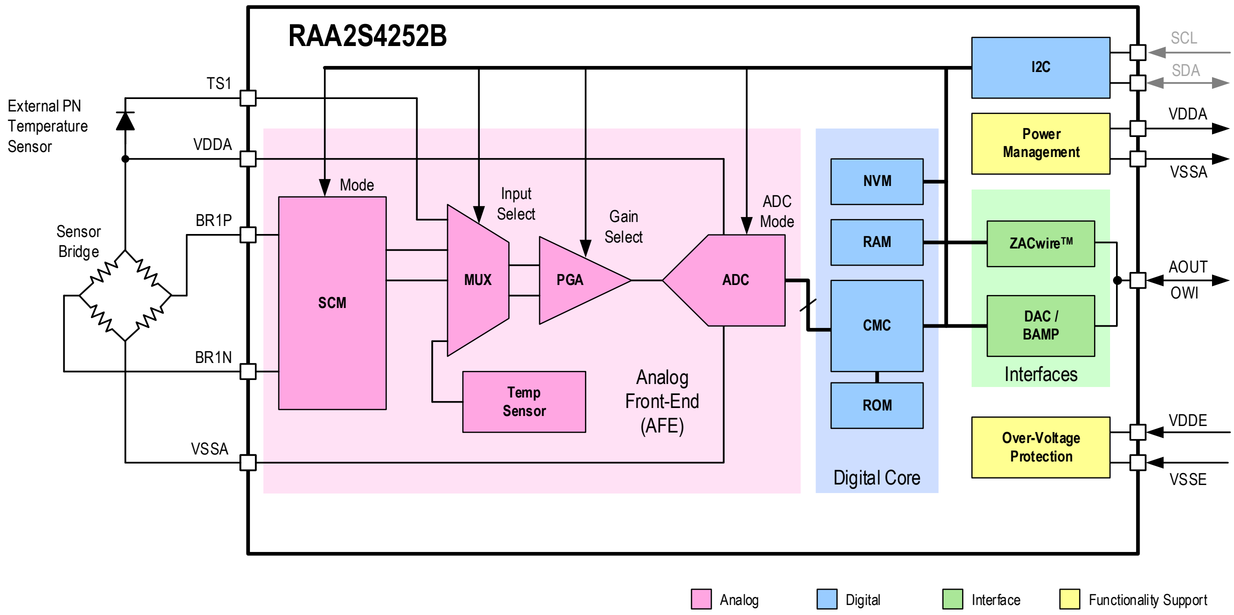


Figure 2. RAA2S4252B Block Diagram

7.2 Signal Path

The RAA2S4252B signal path consists of the analog front-end (AFE), the digital signal processing unit, and the analog output stage. In addition, the device also has a serial digital one-wire interface (ZACwire™) for calibration purposes.

The resistive bridge sensor signal is applied to the BRP and BRN and is handled as a fully differential signal. Both signal lines have a dynamic range symmetrical to the common mode potential (equal to $V_{DDA}/2$) in order to process both positive and negative differential input signals. These differential signals are pre-amplified by the programmable gain amplifier (PGA) and are converted to digital values by the A/D converter (ADC).

A multiplexer (MUX) selects and transmits the signals from either the bridge sensor or the selected temperature sensor to the analog-to-digital converter (ADC) in a defined sequence. The temperature sensor can either be an external diode or the internal on-chip proportional-to-absolute-temperature (PTAT) source selected by NVM configuration.

The digital signal correction is processed in the calibration microcontroller (CMC) using ROM-resident correction formulas and sensor-specific coefficients stored in the NVM. The configuration data and the conditioning coefficients are programmed into the NVM during the calibration process by digital one-wire communication via the AOUT pin.

During the calibration process, raw measurement values can be requested via the digital interfaces.

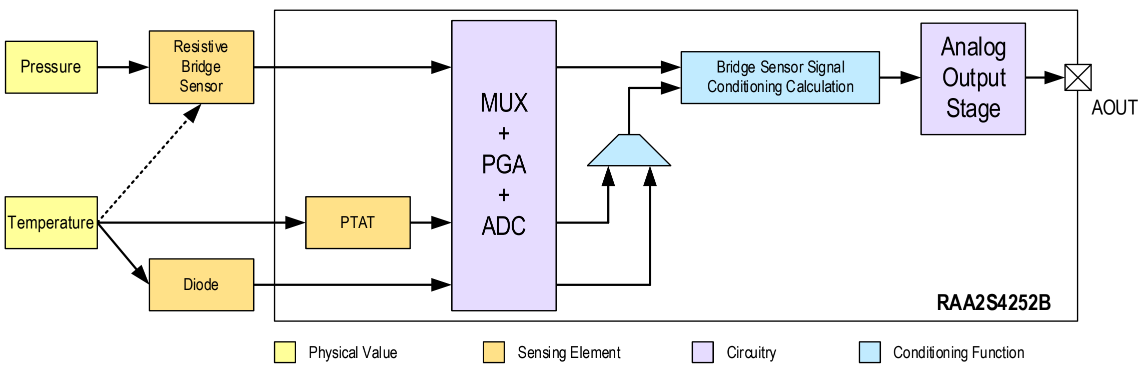


Figure 3. Main Signal Path

7.3 Signal Measurement

7.3.1. Full Bridge Sensor Measurement

The RAA2S4252B measures a differential bridge sensor element signal (BRP to BRN). The signal path is ratiometric and fully differential. The ratiometric reference voltage V_{REF} is equal to (V_{TOP} – V_{BOT}). V_{TOP} equals to V_{DDA} and VBOT equals to V_{SSA} since both voltage references are shorted internally.

7.3.2. Temperature Measurements

The RAA2S4252B supports two methods for acquiring temperature data needed for the conditioning of the sensor signal:

- An on-chip PTAT sensor.
- An external PN-junction diode connected to the TS1 pin and referenced to the sensor top potential (VDDA pin).

7.3.3. Measurement Cycle

The measurement cycle is the sequence of measurements processed during the Normal Operation Mode (NOM). It delivers the raw measurement results from all connected sensor elements and from the supervision functions. The measurements are processed sequentially, all using the same ADC to convert the analog input voltages to a digital value.

7.4 Analog Front-End

7.4.1. Overview

The analog front-end (AFE) consists of the sensor check module (SCM), the multiplexer (MUX), the programmable gain amplifier (PGA), and the analog-to-digital converter (ADC) and the internal PTAT. The internal offset of the analog front-end is eliminated by an auto-zero compensation.

7.4.2. SCM

The sensor check module (SCM) implements the self-diagnostic features for the analog front-end. The SCM provides the sensor connection checks (short and open circuit) as well as several other diagnostic functions.

7.4.3. Input Multiplexer

The input multiplexer (MUX) selects one of the various inputs and connects it to the signal path utilizing a single ADC. It allows a very flexible signal routing between the connected sensor and the RAA2S4252B.

7.4.4. Programmable Gain Amplifier

The sensor signal can be amplified by the on-chip programmable amplifier (PGA) using a gain between 3 and 548.6, or between 24 and 912 if Extended Sensor Offset Compensation is used – see 7.4.5. Alternatively, the PGA can be bypassed and the sensor signal is applied directly to the ADC. In this case the gain is equal to 1. The gain is adjustable for every single bridge sensor measurement task individually in order to provide an ADC input signal span of greater than 50% FS.

Table 6 shows the adjustable gains of the PGA, the corresponding signal spans, and the common mode range limits.

Table 6. Adjustable PGA Gains and Resulting Sensor Signal Spans

Select Value PgaGainSel	PGA Gain a_{PGA}	Maximum[1] Sensor Differential Voltage V_{IN_SPAN} [mV] with V_{TOP_BOT}=5000mV	Maximum[1] Sensor Differential Voltage V_{IN_SPAN} [mV/V], relative to V_{TOP_BOT}
0	1.0	4690	938
1	3.0	1560	312

Select Value PgaGainSel	PGA Gain a_{PGA}	Maximum[1] Sensor Differential Voltage V_{IN_SPAN} [mV] with V_{TOP_BOT}=5000mV	Maximum[1] Sensor Differential Voltage V_{IN_SPAN} [mV/V], relative to V_{TOP_BOT}
2	3.5	1340	268
3	4.2	1120	224
4	5.0	938	188
5	5.9	794	159
6	7.0	670	134
7	8.4	558	112
8	10.0	469	93.8
9	11.8	397	79.4
10	14.0	335	67.0
11	16.9	277	55.4
12	20.0	234	46.8
13	24.0	195	39.0
14	28.5	164	32.8
15	34.3	137	27.4
16	40.7	115	23.0
17	48.0	97.7	19.5
18	57.0	82.2	16.4
19	68.6	68.3	13.7
20	81.4	57.6	11.5
21	96.0	48.8	9.76
22	114.0	41.1	8.22
23	137.1	34.2	6.84
24	162.9	28.8	5.76
25	192.0	24.4	4.88
26	228.0	20.6	4.12
27	274.3	17.1	3.42
28	325.7	14.4	2.88
29	384.0	12.2	2.44
30	456.0	10.3	2.06
31	548.6	8.54	1.71

[1] Exceeding the Maximum Sensor Span results in saturation of the AFE, AdcRngSh="0.0625"

Recommendation: To achieve the best stability and linearity performance of the AFE, operate the PGA in a differential output voltage range within 10% to 90% of the ratiometric reference voltage $V_{REF} = V_{SENS} = (V_{TOP} – V_{BOT})$. V_{TOP} equals to V_{DDA} and V_{BOT} equals to V_{SSA} since both voltage references are shorted internally. The gain must be selected to guarantee this constraint for the entire operating temperature range of the application and for the specified sensor bridge tolerances.

7.4.5. Compensation of Large Sensor Offsets

The RAA2S4252B supports both analog and digital sensor offset compensation:

Analog sensor offset compensation (XSOC): supports the compensation of large sensor offset values up to 10 times higher than the span as shown in Table 7. An offset compensation voltage is added before analog amplification as otherwise the sensor signal would overdrive the analog frontend. XSOC is adjustable with 64 steps for every polarity.

Digital sensor offset compensation (digital zooming): processed as part of the digital signal conditioning by the CMC unit. It is applicable for large sensor offsets up to three times higher than the span. It generates a loss of resolution of up to 3 bits and therefore requires measurement of the sensor signal with higher resolution.

Two columns (Maximum Sensor Span with XSOC) show the maximum value of the differential input signal that can be supplied to the BRP/BRN pins without saturating the ADC. This signal depends on the selected gain (PGA Gain with XSOC). The analog offset compensation is controlled by a 7 bit value, that results in 63 values for compensating positive and 63 values for compensating negative offset. The maximum and the minimum compensation values, in relation to the input of the SSC are given in the last two columns of Table 7. The minimum value is also equal to step size when the XSOC is changed.

Table 7: Extended Sensor Offset Compensation (XSOC) Adjustments

Select Value PgaGainSel	PGA Gain with XSOC a_{PGA_XSOC}	Maximum[1] Sensor Differential Voltage with XSOC $V_{IN\_SPAN\_XSOC}$ [mV] with V_{TOP_BOT}=5000mV	Maximum[1] Sensor Differential Voltage with XSOC $V_{IN\_SPAN\_XSOC}$ [mV/V], relative to V_{TOP_BOT}	Input Related XSOC Value [mV/V]	
				Minimum (Step size)	Maximum
0	n.a.	n.a.	n.a.	n.a.	n.a.
1	24.0	195	39.0	7.8	492.2
2	28.5	164	32.8	7.8	492.2
3	34.3	137	27.4	5.5	344.5
4	40.7	115	23.0	5.5	344.5
5	48.0	97.7	19.5	3.9	246.1
6	57.0	82.2	16.4	3.9	246.1
7	68.6	68.3	13.7	2.7	172.3
8	81.4	57.6	11.5	2.7	172.3
9	96.0	48.8	9.76	2.0	123.0
10	114.0	41.1	8.22	2.0	123.0
11	137.1	34.2	6.84	1.4	86.1
12	162.9	28.8	5.76	1.4	86.1
13	192.0	24.4	4.88	1.0	61.5
14	228.0	20.6	4.12	1.0	61.5
15	274.3	17.1	3.42	0.7	43.1
16	325.7	14.4	2.88	0.7	43.1
17	384.0	12.2	2.44	0.5	30.8
18	456.0	10.3	2.06	0.5	30.8
19	548.6	8.54	1.71	0.3	21.5
20	651.4	7.20	1.44	0.3	21.5
21	768.0	6.10	1.22	0.2	15.4
22	912.0	5.14	1.03	0.2	15.4

[1] – exceeding the Maximum Sensor Span results in saturation of the AFE, AdcRngSh="0.0625"

7.4.6. Analog-to-Digital Converter

The analog-to-digital converter is implemented using the fully-differential switched-capacitor technique. The conversion is largely insensitive to instabilities of the clock frequency. The ADC provides adjustable input range shift.

7.5 Bridge Sensor Signal Conditioning

The bridge sensor signal conditioning is processed every time a new measurement value is available from the analog-to-digital conversion. The conditioning calculation provides compensation of the temperature dependent offset and gain, and of the non-linearity. Both the external temperature sensor signal and the on-chip PTAT signal can be selected for compensating the temperature dependency of the bridge sensor signal.

The conditioning coefficients are stored to the NVM during the calibration process.

The RAA2S4252B provides the following filter functions:

- Averaging low-pass filter
- IIR filter of third order
- Non-linear noise cancelation filter.

The conditioning result for the bridge sensor signal is stored to the RAM Output Memory.

7.6 Output Modes

In typical application the RAA2S4252B provides analog voltage output at the pin AOUT. The analog output is continuously updated with the bridge sensor signal conditioning result.

Two output modes are available, which only differ in the final transfer characteristics from the bridge-sensor conditioning result to the analog output value:

- Analog Output
- Switch Output

An unity gain output buffer drives the analog output potential. A 12-bit resistor-string DAC generates the input signal for the buffer. The output buffer, which is a rail-to-rail operation amplifier, is offset compensated and current limited. Therefore, a short-circuit of the analog output to ground or the power supply does not damage the RAA2S4252B.

7.7 Digital One-Wire Interface

For configuration and calibration purposes, the RAA2S4252B provides serial digital communication via a one-wire interface (OWI). It can also be used as a communication interface in Normal Operation Mode (NOM) to read the bridge sensor signal conditioning result on request. The OWI pin is an open-drain topology.

7.8 NVM

Configuration and calibration data are stored in an on-chip non-volatile memory (NVM), which is using the floating gate storage principle. The NVM stores data based on differential bit cells.

The NVM supports:

- A write lock option prevents overwriting the configuration data. Releasing the write lock via OWI communication is not possible.
- Traceability Data

7.9 Over-Voltage, Reverse-Polarity, and Short-Circuit Protection

RAA2S4252B is designed for a 5V supply provided by an electronic control unit (ECU).

RAA2S4252B and the connected sensor elements are protected from over-voltage and reverse-polarity damage by an internal supply voltage regulator with a current limitation function. The analog output pin AOUT is protected regarding short-circuit, over-voltage and reverse polarity. These functions are described in Table 8 and are valid for operation of the RAA2S4252B in the application circuit shown in section 9 within the specifications according to the absolute maximum ratings given in section 3.

The pins VDDE, VSSE and AOUT are protected against over-voltage conditions up to ±40V related to the VSSE pin as defined in absolute maximum ratings (see Table 2) if the external components shown in application circuit shown in section 9 are implemented.

Note: When the over-voltage protection is active, the device might have a higher power dissipation. Depending on the ambient temperature and on the external sensor characteristics, the higher power dissipation of the device may lead to a violation of the maximum junction temperature.

Table 8. Protection Features

No.	VSSE Pin	AOUT Pin	VDDE Pin	Comment
DS_300	0	0 to 5V	5V	Normal Mode
DS_301	0	Open	40V	VDDE to VSSE
DS_302	0	Open	-40V	Reverse voltage
DS_303	0	40V	Open	AOUT to VSSE
DS_304	0	-40V	Open	Reverse voltage
DS_305	Open	0	40V	VDDE to AOUT
DS_306	Open	0	-40V	Reverse voltage
DS_307	0	0	40V	VDDE to (AOUT+VSSE)
DS_308	0	0	-40V	Reverse voltage
DS_309	0	40V	40V	(VDDE+AOUT) to VSSE
DS_310	0	40V	5.0V	AOUT to VSSE
DS_311	0	-40V	-40V	Reverse voltage
DS_312	0	40V	0	AOUT to (VDDE+VSSE)
DS_313	0	-40V	0	Reverse voltage AOUT
DS_314	0	-35V	5V	Reverse voltage AOUT

8. Fault-Safe Operation

8.1 Overview

Fault checks verify the operation of the RAA2S4252B and of the connected sensing element at power-on and during Normal Operation Mode (NOM). If a fault is detected, the Diagnostic Mode (DM) is activated and the fault status is messaged.

8.2 Fault Messaging

In diagnostic mode, the analog output is either high-ohmic or driven to lower diagnostic range (LDR).

The RAA2S4252B has two different diagnostic modes with different behavior:

Static Diagnostic Mode

- The measurement and conditioning cycle is stopped.
- The analog output is set to lower diagnostic range.
- The one-wire communication interface is enabled for reading detailed diagnostic status information.
- If enabled, the RAA2S4252B is reset, including a reset of all status registers.
- The RAA2S4252B can be restarted by a power-off/power-on sequence.

Temporary Diagnostic Mode

- The measurement and conditioning cycle keeps running.
- Fault checks are continuously processed, including update of fault status.
- The analog output is set to lower diagnostic range.
- The one-wire communication interface is enabled for reading detailed diagnostic status information.
- The RAA2S4252B returns to Normal Operation Mode, including analog output of sensor signal, if fault checks no longer detect errors.

8.3 Fault Checks

Table 9 lists the available fault checks.

Table 9. Fault Checks

Requirement	Identifier	Fault Check
Device Self-Supervision Fault Checks		
DS_400	VDDAPOR	Analog supply voltage (VDDA) under-voltage reset; power-on reset (POR)
DS_401	VDDDBOD	Digital supply voltage (VDDD) under-voltage reset; brownout detection (BOD)
DS_402	OSCFAIL	Oscillator fail check; reset after oscillator restart
DS_403	NVMCRC	NVM content CRC check
DS_405	CYCCRC	Measurement and conditioning cycle CRC check
DS_406	RAMPRTY	RAM content parity check
DS_407	ROMCRC	ROM content CRC check
DS_408	WWDG	Windowed watchdog; CMC alive supervision
DS_409	COMP	Computational check; CMC code processing and peripheral bus access check
DS_410	CHIPP	Chipping check
Sensing Element Fault Checks		
DS_420	BRSC	Bridge sensor short and connection check
Environment and Operation Condition Fault Checks		
DS_430	BRSRNG	Bridge sensor signal range check
DS_431	PTATRNG	On-chip temperature range check
DS_432	TRNG	Temperature range check

9. Application Circuit and External Components

Application features:

- The SSC is part of a 5V module, which is powered by the electronic control unit (ECU)
- Sensor module with 3-pin connector provides pressure measurement data via Analog voltage output
- Temperature signal for pressure signal correction can be obtained either from the on-chip PTAT or from an external diode (connected to TS1)
- End-of-line calibration uses one-wire communication via the AOUT pin
- Valid only for the Main BRS measurement
- The maximum value of the capacitors C_{IN} can be calculated using the equation below.

$$C_{IN} \leq \frac{LTC}{(8 + \ln(PGA_{GAIN})) \cdot R_{BR}}$$

where,

LTC – Settling time, see Table 5
PGA_{GAIN} – the PGA gain that is used
R_{BR} – the resistance of the sensor bridge

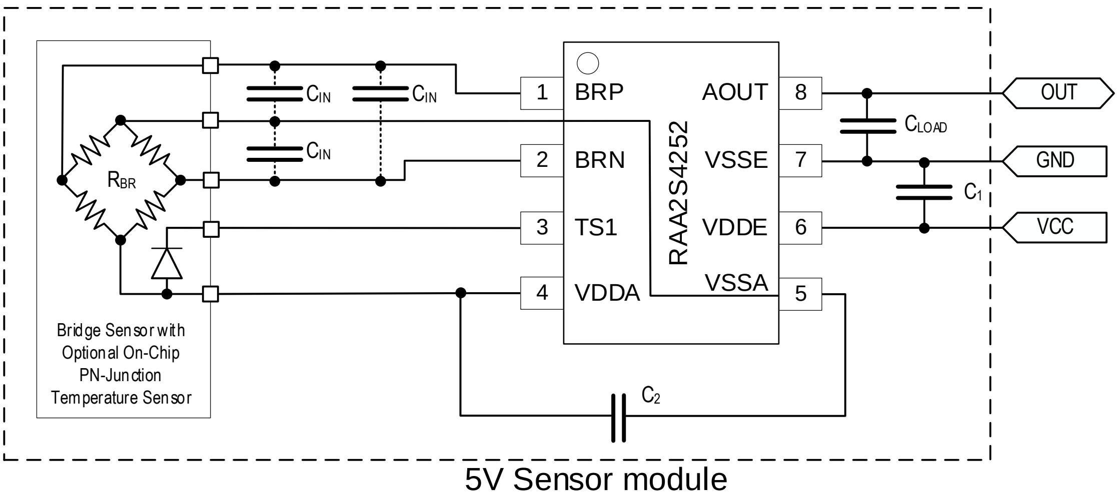


Figure 4. Application Circuit Example of a Pressure and Temperature Sensor with Analog Output

Table 10. Dimensioning of External Components for the Application Example

No.	Component	Symbol	Conditions	Min	Typical	Max	Unit
Informational	Capacitor	C_1	V_{MAX} ≥ 60V, Low ESR type		100 ± 20%		nF
Informational	Capacitor	C_2	V_{MAX} ≥ 10V, Low ESR type	47 ± 20%	100 ± 20%	220 ± 20%	nF
Informational	Capacitor	C_{LOAD}	V_{MAX} ≥ 60V, Low ESR type	10 ± 20%	47 ± 20%	470 ± 20%	nF

[1] The component values are examples and must be adapted to the requirements of the application, in particular to the EMC requirements.

10. ESD Protection and EMC Specification

10.1 ESD Protection

All pins have an ESD protection of ≥ 2000V according to the Human Body Model (HBM with 1.5kOhm/100pF, based on JEDEC JS-001-2017). The VDDE, VSSE, and AOUT pins have an additional ESD protection of ≥ 4000V (HBM with 1.5kΩ/100pF, based on JEDEC JS-001-2017).

The level of ESD protection are tested with devices in SOIC 8 (4.9mm × 3.9mm) packages during the product qualification.

10.2 Latch-Up Immunity

All pins pass ±100mA latch-up test based on testing that conforms to the standard EIA/JESD 78.

10.3 Electromagnetic Emission

The conducted electromagnetic emission of externally connected pins of the device is measured according to the following standard: *IEC 61967_4:2002 + A1:2006.*

Measurements are performed with the application circuits described in section 9.

For the off-board pins, the spectral power measured with the 150Ω method must not exceed the limits according to *IEC 61967_4k, Annex B.4 code H10kN* in the >200kHz range. For the VSSE pin, the spectral power measured with the 1Ω method must not exceed the limits according to *IEC 61967_4k, Annex B.4 code 15KmO.*

10.4 Conducted Susceptibility

The conducted susceptibility of externally connected pins of the device is measured according to the IEC 62132-4 standard, which describes the direct power injection (DPI) test method.

Measurements are performed with the following conditions:

- The application circuit described in the section 9.
- Internal temperature sensor for temperature compensation.
- The main sensing element is replaced by a resistive divider.
- The DUT is configured to provide 50% of VDDA on its output.

Table 11 gives the specifications for the DPI tests.

Table 11. Conducted Susceptibility (DPI) Tests

No.	Test	Frequency Range	Target (dBm)	Load Pins	Protocol	Error Band	Coupling Impedance
DS_350	DPI, direct coupled	1MHz to 300MHz	26	VDDE, AOUT	Analog out	±1%	5kΩ / 10nF
DS_351	DPI, direct coupled	300MHz to 1000MHz	32	VDDE, AOUT	Analog out	±1%	5kΩ / 10nF

11. Reliability and RoHS Conformity

The RAA2S4252B is qualified according to the AEC-Q100 standard, operating temperature grade 0. A fit rate <10 FIT (junction temperature = 55°C, confidence level = 70%, activation energy = 0.7eV) is estimated.

A typical fit rate for TSMC's CV018BCD technology, which is used for the RAA2S4252B, is < 1 FIT (temperature = 55°C, confidence level = 60%, activation energy = 0.7eV).

The reliability calculation is based on the product qualification, with stress time equivalent to at least 3000 hours high temperature operating life (HTOL) at an ambient temperature of 150°C under normal operating conditions.

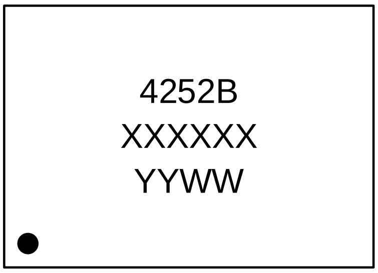
The RAA2S4252B complies with the RoHS directive and does not contain hazardous substances. The complete RoHS declaration update can be downloaded from https://www.renesas.com/eu/en/about/corporate-responsibility-citizenship.

12. Package Outline Drawings

The package outline drawings are accessible from the link below. The package information is the most current data available.

Package Outline Drawing Package Code:DCG8D4 8-SOIC 4.9 x 3.9 x 1.75 mm Body, 1.27mm Pitch (renesas.com)

13. Marking Diagram



1. "4252B" is the truncated part number.
2. "XXXXX" is the last digits of the lot number.
3. "YYWW" is the last digits of the year and week that the part was assembled.

14. Ordering Information

Part Number	Description and Package	MSL Rating	Shipping Packaging	Temperature
RAA2S4252B5HSP#JA0	8-Lead Small Outline (SOIC) Package	MSL1	Reel (13 inch)	-40°C to 150°C
RAA2S425XKIT	RAA2S425X SSC Evaluation Kit: Evaluation Board, 5 RAA2S4251B Samples.			
RAA2S4252EXT	RAA2S4252B adapter board with 5 RAA2S4252B samples			

15. Glossary

Term	Description	Term	Description
A/D	Analog-to-Digital	LSB	Least Significant Bit
ADC	Analog-to-Digital Converter	MSB	Most Significant Bit
AEC	Automotive Electronics Council	MUX	Multiplexer
AFE	Analog Front-End	NOM	Normal Operation Mode
AOUT	Analog Out	NVM	Nonvolatile Memory
BOD	Brownout Detection	OWI	One-Wire Interface
BR	Bridge Sensor	PCB	Printed Circuit Board
CDM	Charged Device Model	PGA	Programmable Gain Amplifier
CM	Command Mode	PTAT	Proportional-to-Absolute Temperature
CMC	Calibration Microcontroller	PTC	Thermistor – Positive Temperature Coefficient Resistor
CMOS	Complementary Metal-Oxide Semiconductor	PWR	Power Management and Protection Unit
CRC	Cyclic Redundancy Check	QFN	Quad-Flat No-Leads – IC package
DAC	Digital-to-Analog Converter	RAM	Random Access Memory
DM	Diagnostic Mode	RISC	Reduced Instruction Set Computing
DNL	Differential Nonlinearity	RoHS	Restriction of Hazardous Substances
DPI	Direct Power Injection	ROM	Read-Only Memory
DSP	Digital Signal Processing	RMS	Root-Mean-Square
ECU	Electronic Control Unit	RTD	Resistance Temperature Device
EMC	Electromagnetic Compatibility	SCL	Serial Clock
ESD	Electrostatic Discharge	SCM	Sensor Check Module
FIT	Failures in Time	SDA	Serial Data
FOUR	Fast output update rate	SG	Safety Goal
FSO	Full Scale Output	sint	Signed integer value
HBM	Human Body Model	SSC	Sensor Short Check (diagnostic feature) or Sensor Signal Conditioner
HTOL	High Temperature Operating Life	TQA, TQE	Temperature range identifier. See DS_051 for definition.
HVAC	Heating, Ventilation and Air Conditioning	UDR	Upper Diagnostic Range
I2C	Inter-Integrated Circuit—serial two-wire data bus	uint	Unsigned integer value
IIR	Infinite Impulse Response	ZACwire™	RENESAS-specific One-Wire Interface
INL	Integral Nonlinearity	XSOC	Analog Sensor Offset Correction
LDR	Lower Diagnostic Range		

16. Revision History

Revision	Date	Description
2.0	Sep.30.24	▪ Change of the definition of parameter DS_189, DS_133, DS_134 ▪ DS_103 added
1.2	Jul.13.23	▪ Correcting the ESD standard ▪ Updating Reliability and RoHS section. ▪ AOUT leakage current for pull up and pull down scenarios
1.1	Apr.24.23	▪ Requirements updated. ▪ Updated values for certain parameters ▪ Updated descriptions for readability and clarity.
1.0	Jun.17.22	Initial release.

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
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