RAA271050

4A, High Efficiency Synchronous Buck Regulator for Automotive Applications

RAA271050 is an automotive grade 4A synchronous step-down voltage regulator with integrated high-side and low-side MOSFETs. It supports an input voltage range of 4.0V to 42V and provides an OTP-programmable fixed output voltage of 5.0V or 3.3V. The RAA271050 is highly versatile and can be used as a high-efficiency primary regulator for companion secondary power management ICs or as a point-of-load regulator.

The RAA271050 uses peak current mode control, coupled with the high 2.2MHz fixed frequency, provides component selection flexibility to minimize the total solution size. For applications with flexible solution sizes, a 440kHz fixed frequency option is available, which provides higher efficiency. Its protection features include input UVLO, output overcurrent, overvoltage, undervoltage, and thermal overload protection.

The RAA271050 has been developed on an ISO26262-compliant development process. It can support system safety goals up to ASIL D. It implements safety monitoring features that ensure the output voltage and temperature are all within their expected operation ranges. This IC also implements dual-reference voltages to ensure the safety mechanisms are free of common-cause failure with the regulation blocks.

The RAA271050 is available in a 4×4mm 22-pin step-cut QFN (SC-QFN) package. The device is qualified per AEC-Q100 Grade 1, supporting an ambient temperature range of -40°C to 125°C.

Features

- V_{IN} operating range from 4.0V to 42V
- V_{OUT} = 5.0V or 3.3V (factory programmable)
- High efficiency synchronous buck regulator with efficiency up to:
  - 95%; V_{IN} = 12V; V_{OUT} = 5V; F = 440kHz
  - 92%; V_{IN} = 12V; V_{OUT} = 5V; F = 2.2MHz
- 2% V_{OUT} accuracy over temperature, load, line
- Switching frequency: 2.2MHz or 440kHz
- Optional Spread Spectrum Modulation (SSM)
- Factory programmable soft-start
- Soft-stop output discharge during disable
- RSTb fail-safe output
- Bootstrap supply UVLO
- AEC-Q100 qualified, Grade 1: -40°C to +125°C

Applications

- Automotive power
- R-CAR processor PMICs
- DC/DC POL modules

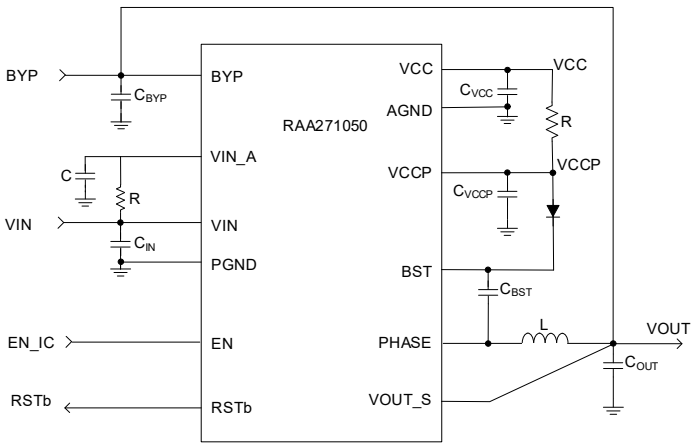


Figure 1. Typical Application Diagram

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1. Overview

1.1 Typical Application Schematics

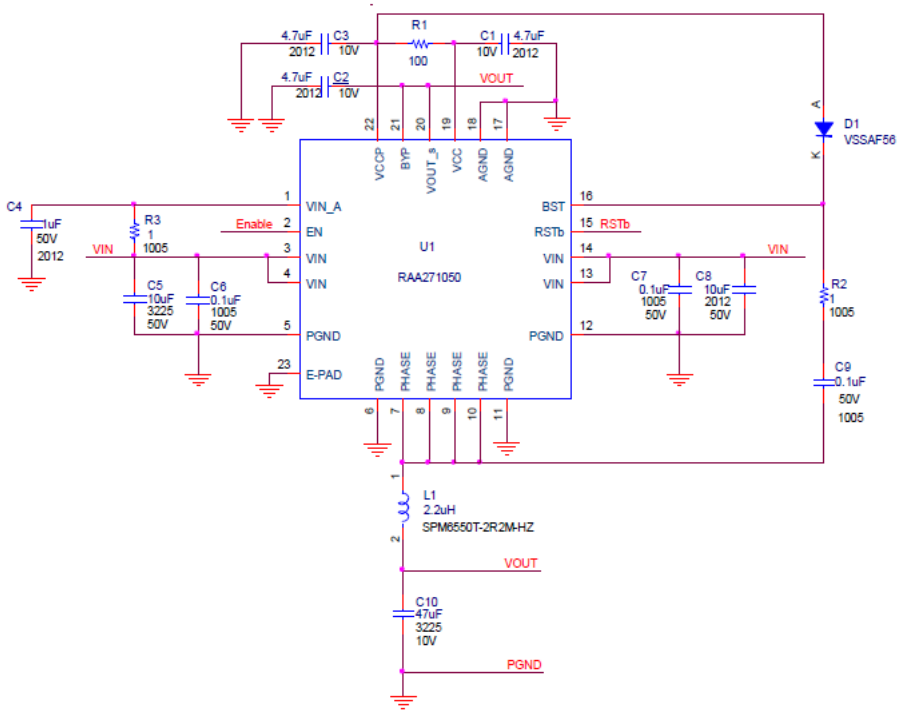


Figure 2. 2.2MHz Switching Frequency Schematic

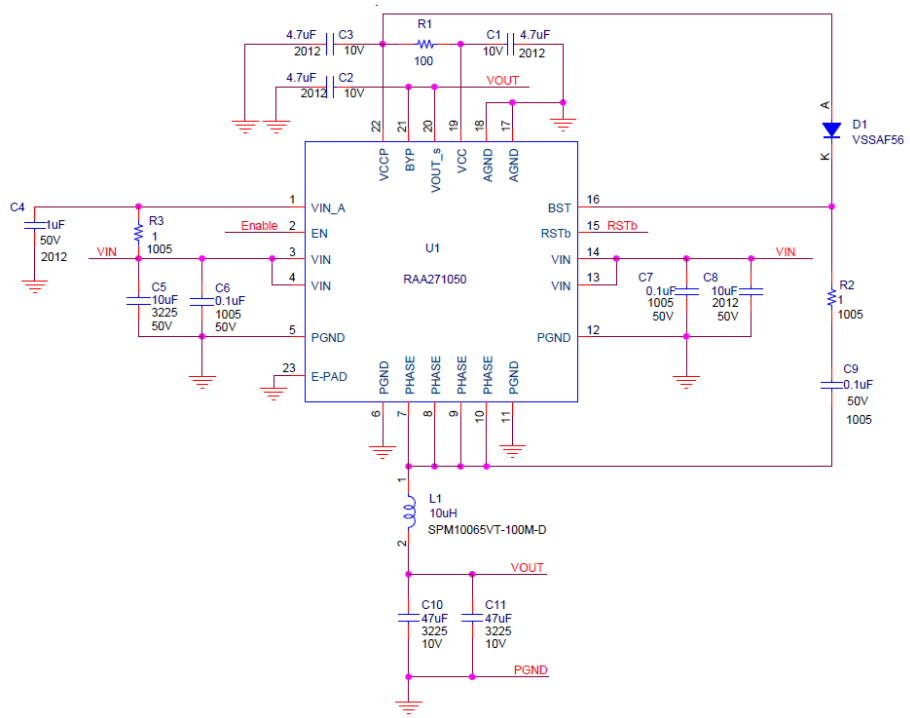


Figure 3. 440kHz Switching Frequency Schematic

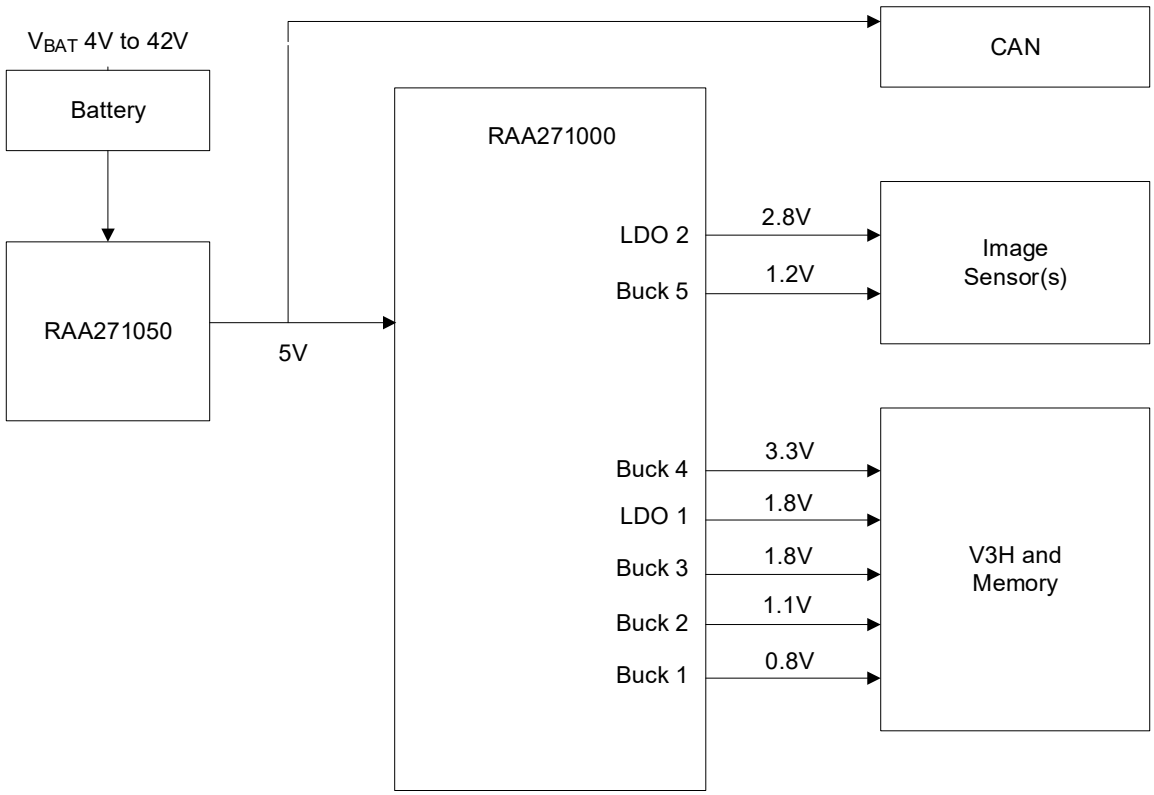


Figure 4. Target Application

1.2 Block Diagram

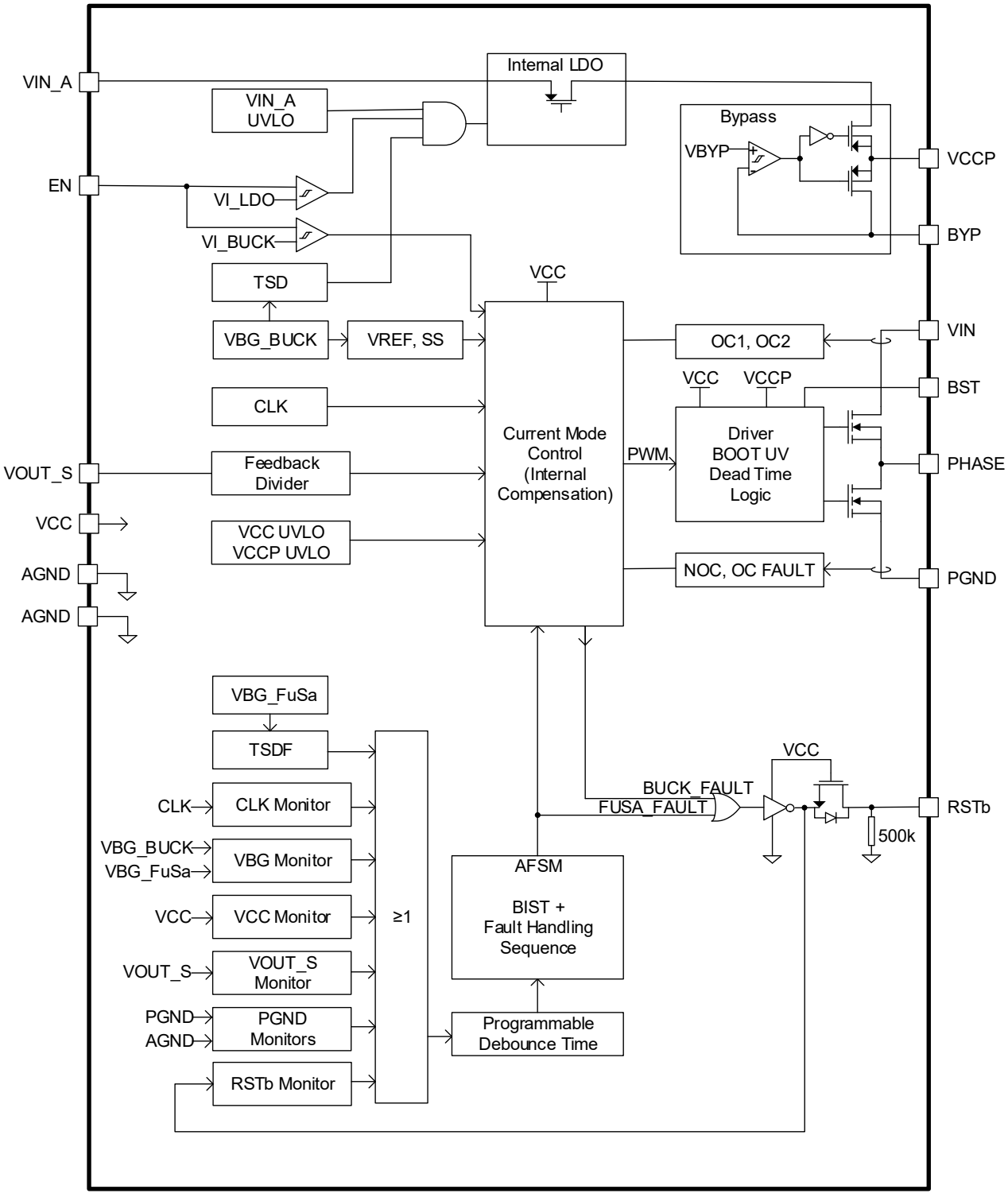
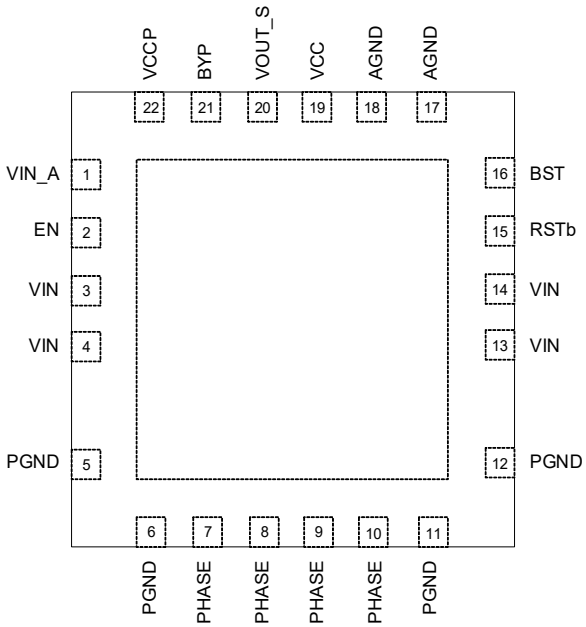


Figure 5. Block Diagram

2. Pin Information

2.1 Pin Assignments



Top View

2.2 Pin Descriptions

Pin Number	Pin Name	Description
1	VIN_A	Input supply voltage for the internal LDO (VCCP). Connect through 1Ω resistor to VIN pin, and place 1µF capacitor for filtering.
2	EN	Enable control input. EN is a threshold-sensitive enable input to the chip. When EN > 1.2V, the VCCP LDO is activated, IC circuits are powered up, the device goes into standby, and no switching occurs. When EN > 1.85V, the Buck begins switching. When EN falls below 0.45V, the IC is disabled, and all fault states are cleared. EN can be tied to VIN for automatic startup.
3, 4, 13, 14	VIN	Supply input for the IC and Buck switching regulator. VIN supplies the high-side MOSFET of the Buck switching regulator and the internal VCCP regulator that powers IC circuits. Place a 10µF ceramic capacitor parallel with a 0.1µF ceramic capacitor from VIN to PGND on each side and as close as possible to the IC for minimum switching loop and smallest spikes due to fast switching.
5, 6, 11, 12	PGND	This pin provides the return path for the low-side MOSFET. This pin carries a noisy driving current, so the traces connecting from this pin to the low-side MOSFET source and VCCP decoupling capacitor ground pad should be as short as possible. All the sensitive analog signal traces should not share common traces with this driver return path. Connect this pin to the ground copper plane (wiring away from the IC instead of connecting through the IC bottom PAD) through several vias as close as possible to the IC.
7, 8, 9, 10	PHASE	This pin is the switching node of Buck. PHASE is the connection point between the Buck high-side N-channel MOSFET and low-side N-channel MOSFET switches. PHASE is a high-dV/dt node that should be isolated from sensitive traces as much as possible.

Pin Number	Pin Name	Description
15	RSTb	System reset output. The RSTb is an active low/active high output that provides a hard reset-low signal to the system MCU when an output fault occurs. Faults that trigger the RSTb output are listed in RSTb Output and Monitors sections. *Note:* When the RSTb output is high, it is internally driven to the diode below the VCC voltage.
16	BST	Buck high-side MOSFET driver supply. BST provides bias voltage for the Buck high-side MOSFET driver. An external bootstrap diode is required between BST and VCCP suitable to drive the Buck internal high-side N-channel MOSFET. Renesas recommends placing a 0.1µF ceramic capacitor between the BST and PHASE pins. The external bootstrap circuit recharges the boot capacitor when the Buck low-side switch is on. BST is a high-dV/dt node that should be isolated from sensitive traces as much as possible. This pin provides bias voltage to the high-side MOSFET driver. The VCCP provides the bias to BST through a fast-switching diode.
17, 18	AGND	Analog ground connection
19	VCC	The VCC operating range is 3.3V to 5.5V. Use a 100Ω resistor between VCCP and VCC and a minimum 4.7µF decoupling ceramic capacitor between VCC and AGND.
20	VOUT_S	Buck output voltage feedback input. Connect VOUT_S to the output of Buck to provide the feedback sense voltage for the Buck regulator. An internal resistor divider at FB sets the output voltage. The Buck output voltage is factory-programmable to either be 3.3V or 5V. Route the VOUT_S trace away from noisy or high-dV/dt signals. This pin is discharged by a 56Ω pull-down resistor when the device is disabled.
21	BYP	Input that bypasses the internal LDO to supply VCCP, VCC, and BST when voltage is greater than V_{BYP}. BYP can be tied to an external supply or the output of the buck, VOUT, to reduce power dissipation caused by the internal LDO. Use a minimum 4.7µF decoupling ceramic capacitor between this pin and the ground plane close to PGND. If BYP is not used, connect to GND.
22	VCCP	The output of the internal linear regulator, nominally 4.3V, provides bias for the low-side and high-side drivers (VCCP connected to BST through a diode).
E-pad		E-pad must be soldered to a large ground plane on the PCB that does not contain noisy power flow. Use as many vias as possible in PAD to help reduce the θ_{JA} of the IC package. E-pad does not have an electrical connection.

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
VIN to PGND	-0.3	45	V
VIN_A, EN	-0.3	45	V
RSTb to AGND	-0.3	51.5	V
PHASE to PGND	-0.3	V_{IN} + 0.3	V
PHASE to PGND (<10ns Pulse Width, 10µJ))	-10	V_{IN} + 0.3	V
BST to PHASE	-0.3	6.5	V
VCCP, VCC, BYP, VOUT_S to AGND, AGND	-0.3	6.5	V
AGND to PGND	-0.3	0.3	V
Maximum Junction Temperature	-	+150	°C
Maximum Storage Temperature Range	-65	+150	°C
Human Body Model (Tested per JS-001-2017)	-	2	kV
Charged Device Model (Tested per JS-002-2018)	-	1	kV
Latch-Up (Tested per JESD78E; Class 2, Level A)	-	100	mA

3.2 Thermal Specifications

Parameter[1]	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	22 Ld 4x4 QFN Package	θ_{JA}[2]	Junction to air, still air	37	°C/W
		θ_{JC}[3]	Junction to case	2.5	°C/W

1. Thermal consideration: θ_{JA} and θ_{JC} are given with JEDEC testing standard and provide a reference to compare various ICs. Improved thermal performance can be achieved through better PCB design, air flow across the device, or a combination of both. See the PCB Layout Guidelines for further information.
2. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
3. For θ_{JC}, the case temperature location is the center of the exposed metal pad on the package underside.

3.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Supply Voltage, VIN	4	42	V
Ambient Temperature	-40	+125	°C
Output Voltage	3.3	5	V

3.4 Electrical Specifications

Recommended operating conditions, V_{IN} = 14V with typical values at T_A = +25°C, unless otherwise specified. **Boldface limits apply across the operating temperature range (-40°C to +150°C, Junction).**[1]

Parameter	Symbol	Test Conditions	Min[2]	Typ	Max[2]	Unit
Input Supply						
Input Voltage Operating Range	V_{IN}	Normal Operation	**4**	-	**42**	V
Supply Operating Current	I_{Q_VIN}	$V_{EN} > V_{IH_BUCK}$; no switching	-	1.7	-	mA
		V_{OUT} = 5; $V_{EN} > V_{IH_BUCK}$; f_{SW} = 440kHz	-	14	-	mA
		V_{OUT} = 5; $V_{EN} > V_{IH_BUCK}$; f_{SW} = 2.2MHz	-	32	-	mA
		$V_{IH_LDO} < V_{EN} < V_{IH_BUCK}$; Including Current into VCC Pin	-	108	-	µA
Shutdown Current	I_{SD}	-	-	1.2	-	µA
UVLO Rising Threshold	V_{UVLOR}	V_{IN_A}, V_{IN}	**4.25**	4.5	**4.75**	V
UVLO Falling Threshold	V_{UVLOF}	V_{IN_A}, V_{IN}	**3.5**	3.65	**3.8**	V
UVLO Delay	V_{UVLOD}	VIN_A, V_{IN}; Slew Rate = 100mV/µs	-	16	-	µs
EN Pin						
Enable Rising Threshold	V_{IH_LDO}	Enable internal LDO	**0.72**	1.2	**1.52**	V
Enable Falling Threshold	V_{IL_LDO}	Disable IC	**0.45**	0.91	**1.24**	V
Enable Rising Logic Threshold	V_{IH_BCK}	Enable for buck regulator	**1.75**	1.85	**1.95**	V
Enable Falling Logic Threshold	V_{IL_BCK}	Disable for buck regulator	**1.55**	1.65	**1.75**	V
Enable Pin Current	I_{EN}	EN = 4V to 42V	-	425	-	nA
V_{OUT_S} Pull-Down Resistance	R_{VOUT_S}	EN = 0V	-	56	-	Ω
BYP Pin (Bypass)						
Bypass Rising Threshold	V_{BYP_R}	Entering BYP Mode	**4.17**	4.27	**4.353**	V
Bypass Falling Threshold	V_{BYP_F}	Entering Internal LDO Mode	**4.1**	4.19	**4.27**	V
Bypass Hysteresis	V_{BYP_HYST}	-	-	90	-	mV
Internal Linear Regulator (VCCP), VCC Pin						
VCCP Voltage	V_{CCP}	$V_{EN} > V_{IH_LDO}$; I_{LOAD} = 50mA	**4**	4.3	**4.5**	V
Linear Regulator Dropout Voltage	V_{DO}	V_{IN} = 4V; $V_{EN} > V_{IH_LDO}$; I_{LOAD} = 50mA	-	200	**500**	mV
Linear Regulator Current Limit	I_{LIM}	$V_{IH_LDO} < V_{EN} < V_{IH_BUCK}$	**100**	160	**230**	mA
VCC, VCCP UVLO Rising	V_{CC_UVLOR}, V_{CCP_UVLOR}	VCC, VCCP UVLO rising	**3.42**	3.6	**3.85**	V
VCC, VCCP UVLO Falling	V_{CC_UVLOF}, V_{CCP_UVLOF}	VCC, VCCP UVLO falling	**2.8**	3.03	**3.25**	V
UVLO Hysteresis	$V_{CC_UVLO_HYST}$, $V_{CCP_UVLO_HYST}$	VCC, VCCP UVLO hysteresis	-	570	-	mV
Switching Step-Down Regulator						
Output Voltage Accuracy	V_{OUT}	Output voltage accuracy; factory programmable: 3.3V or 5.0V	**-2**	-	**2**	%
Pulse Skipping Voltage Threshold	V_{SKIP}	-	-	19.6	-	V

Recommended operating conditions, V_{IN} = 14V with typical values at T_A = +25°C, unless otherwise specified. **Boldface limits apply across the operating temperature range (-40°C to +150°C, Junction).**[1] **(Cont.)**

Parameter	Symbol	Test Conditions	Min[2]	Typ	Max[2]	Unit
Pulse Skipping Voltage Hysteresis	V_{SKIP_HYST}	-	-	1	-	V
High-Side Switch ON-Resistance	R_{DS_H}	V_{IN} = 14V; BST - PHASE = 3.8V; I_{PHASE} = 100mA	-	90	-	mΩ
Low-Side Switch ON-Resistance	R_{DS_L}	V_{IN} = 14V; I_{PHASE} = 100mA	-	65	-	mΩ
Minimum On-Time	t_{ON}	-	-	55	-	ns
Minimum Off-Time	t_{OFF}	-	-	55	-	ns
Peak Current Limit	I_{OC}	-	**5**	6.5	**8**	A
Peak Current Limit 2	I_{OC2}	-	-	8.5	-	A
Low-Side Current Limit	I_{LSOC}	-	-	7	-	A
I_{OCP} Blanking Time	t_{OCP}	-	-	65	**100**	ns
BOOT UVLO	V_{BOOT_UVLO}	Boot falling	-	2	-	V
Negative Current Limit	I_{NEG}	-	-	-3	-	A
I_{NEG} Blanking Time	-	-	-	60	**100**	ns
Frequency						
Switching Frequency	f_{SW}	Factory programmable:440kHz or 2.2MHz	-	2.2	-	MHz
Switching Frequency Tolerance	f_{SW_TOL}		**-10**	-	**10**	%
Spread Spectrum Modulation Frequency Range	f_{SSF}	Factory programmable (0, ±1%, ±2%, ±3%)	**-3**	-	**3**	%
Thermal Shutdown						
Regulation Thermal Shutdown	TH_{SD1}	Temperature rising	**160**	170	**180**	°C
Thermal Hysteresis	TH_{HYS}	Falling hysteresis	-	15	-	°C
Monitors						
Output Voltage Undervoltage	V_{OUTUV}	Factory programmable (-6%, -8%, -12%, 2.8V)	**-2**	-	**2**	%
Output Voltage Overvoltage	V_{OUTOV}	Factory programmable (-6%, -8%, -12%)	**-2**	-	**2**	%
V_{CC} UV Threshold	V_{CC_UVF}	V_{CC} falling threshold	**3.2**	3.3	**3.4**	V
V_{CC} OV Threshold	V_{CC_OVR}	V_{CC} rising threshold	**5.25**	5.375	**5.5**	V
Health Check						
Thermal Shutdown Monitor	TH_{SD2}	Temperature rising	**151**	160	**170**	°C
Clock Monitor Over Frequency Fault Threshold	-	Regulation clock deviation over from 2.2MHz or 440kHz	-	+50	-	%
Clock Monitor Under Frequency Fault Threshold	-	Regulation clock deviation under from 2.2MHz or 440kHz	-	-50	-	%

1. These parts are designed and adjusted for accuracy with all errors in the voltage loop included. Verified by design and/or characterization.
2. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.

4. Typical Performance Curves

Unless otherwise specified, the operating condition is: V_{IN} = 14V, T_A = 25°C.

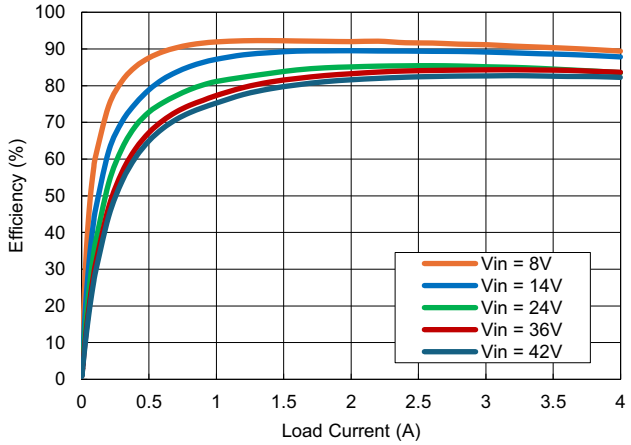


Figure 6. Efficiency at V_{OUT} = 5V
f_{SW} = 2.2MHz, Byp = 5V

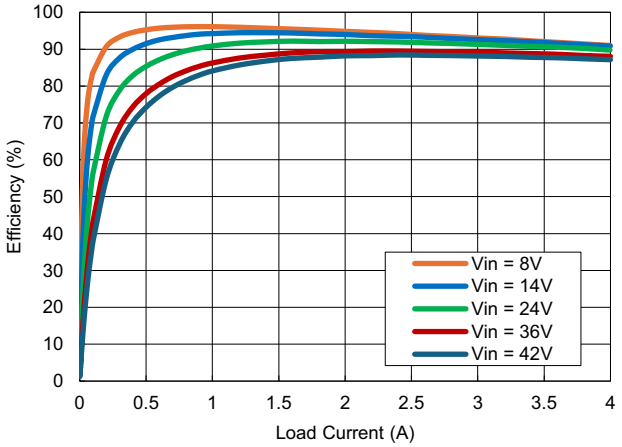


Figure 7. Efficiency at V_{OUT} = 5V
f_{SW} = 440kHz, Byp = 5V

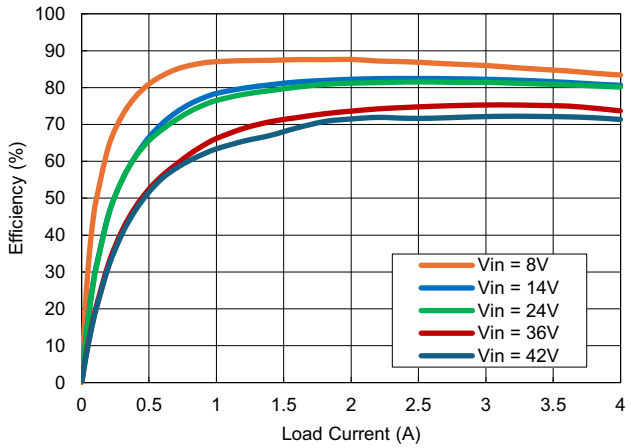


Figure 8. Efficiency at V_{OUT} = 3.3V
f_{SW} = 2.2MHz

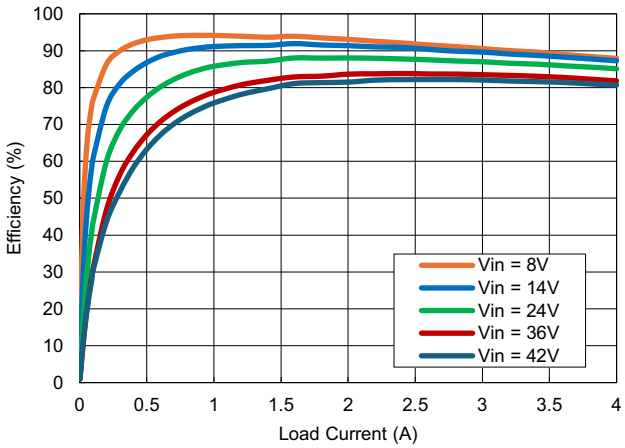


Figure 9. Efficiency at V_{OUT} = 3.3V
f_{SW} = 440kHz

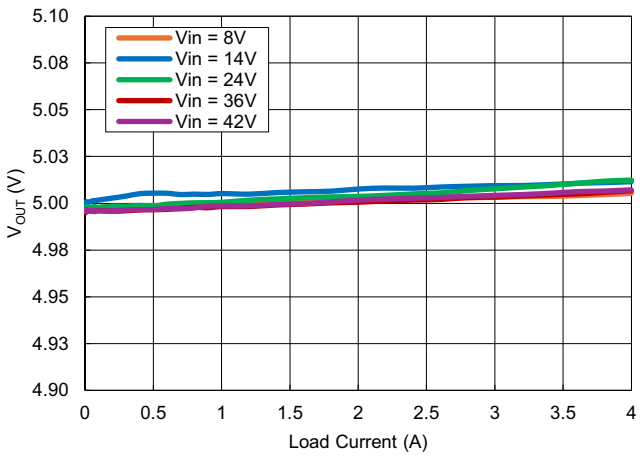


Figure 10. Load and Line Regulation at V_{OUT} = 5V
f_{SW} = 2.2MHz

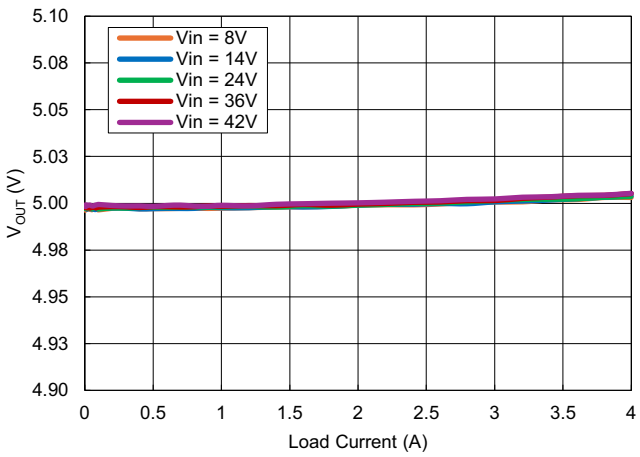


Figure 11. Load and Line Regulation at V_{OUT} = 5V
f_{SW} = 440kHz

Unless otherwise specified, the operating condition is: V_{IN} = 14V, T_A = 25°C.

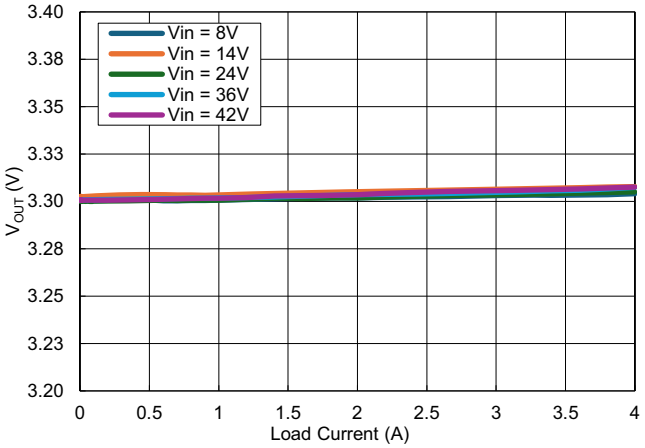


Figure 12. Load and Line Regulation at V_{OUT} = 3.3V f_{SW} = 2.2MHZ

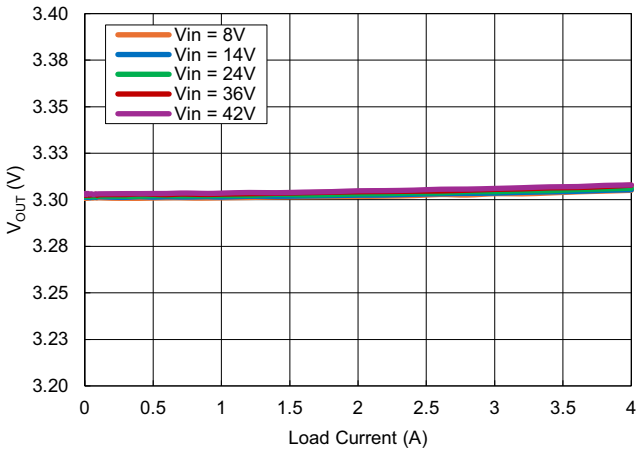


Figure 13. Load and Line Regulation at V_{OUT} = 3.3V f_{SW} = 440kHZ

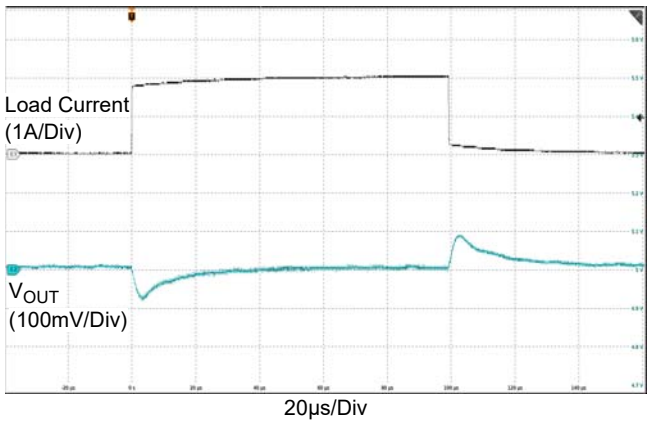


Figure 14. Load Transient at V_{IN} = 14V to V_{OUT} = 5V f_{SW} = 2.2MHz, C_{OUT} = 1x47µF Load Current Stepping from 1A - 3A

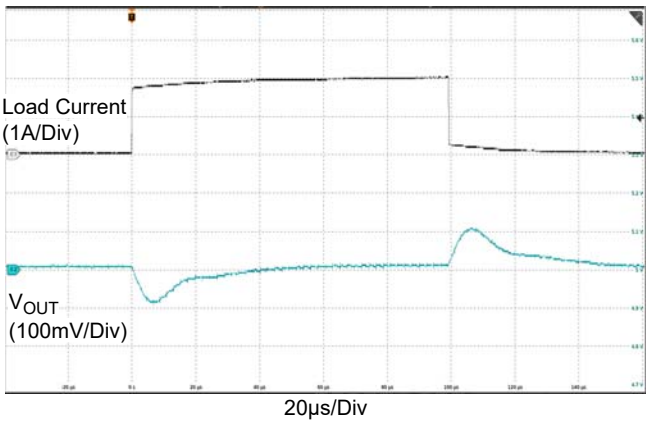


Figure 15. Load Transient at V_{IN} = 14V to V_{OUT} = 5V f_{SW} = 440kHz, C_{OUT} = 2x47µF Load Current Stepping from 1A - 3A

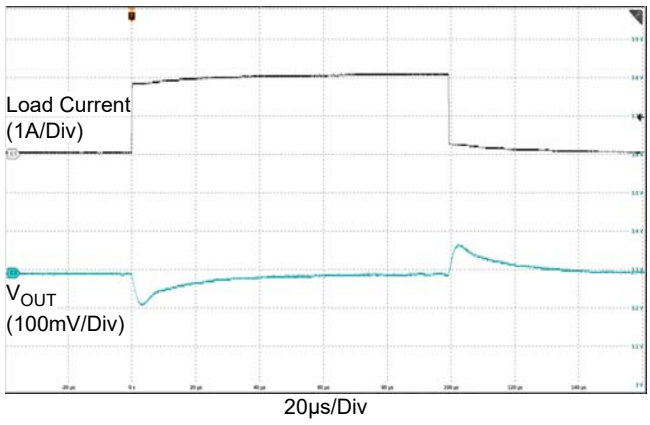


Figure 16. Load Transient at V_{IN} = 14V to V_{OUT} = 3.3V f_{SW} = 2.2MHz, C_{OUT} = 1x47µF Load Current Stepping from 1A - 3A

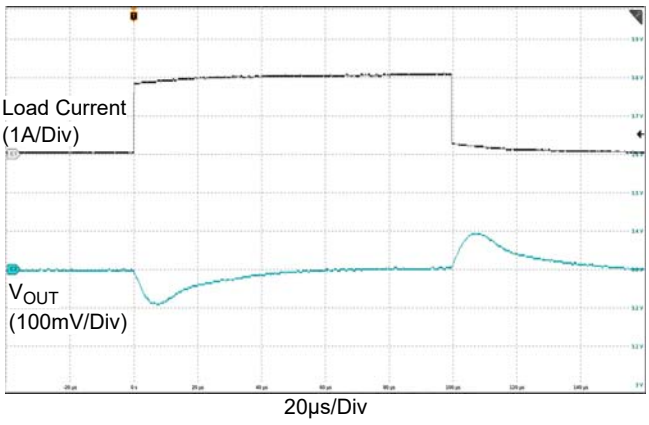


Figure 17. Load Transient at V_{IN} = 14V to V_{OUT} = 3.3V f_{SW} = 440kHz, C_{OUT} = 2x47µF Load Current Stepping from 1A - 3A

Unless otherwise specified, the operating condition is: V_{IN} = 14V, T_A = 25°C.

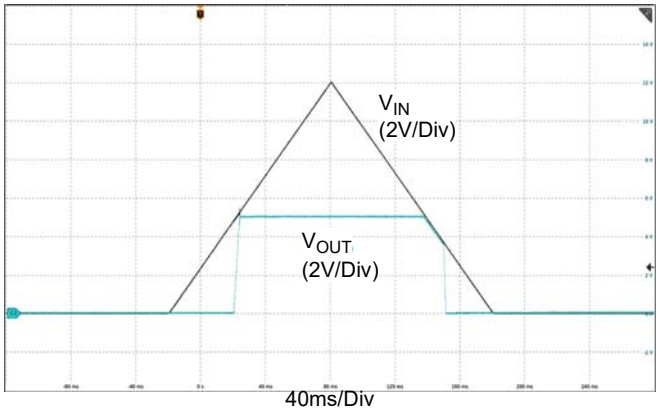


Figure 18. Startup and Dropout Performance at V_{OUT} = 5V, f_{SW} = 440kHz, Load = 250mA

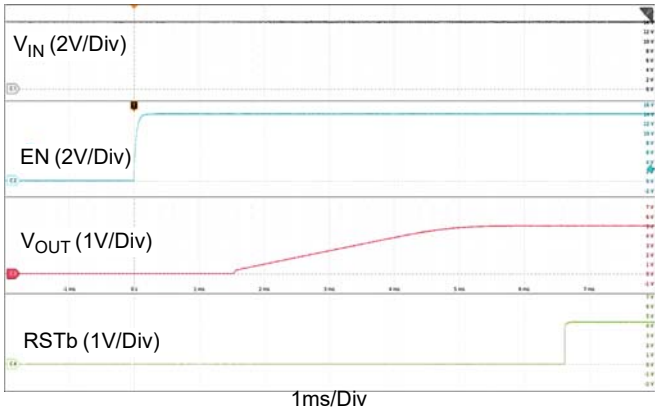


Figure 19. Startup Waveform at V_{OUT} = 5V f_{SW} = 440kHz

5. Applications

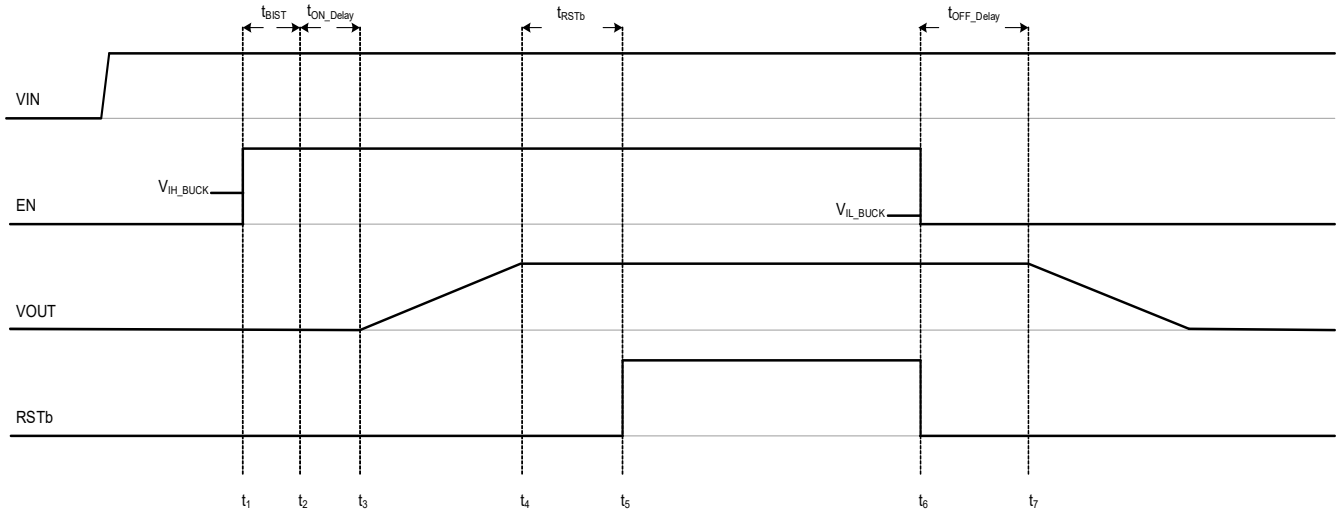
5.1 Factory Programmable Output Voltage

The RAA271050 IC supports input voltages from 4V to 42V, typically from a 12V car battery, and produces a fixed output voltage of either 3.3V or 5V, programmable at the factory.

5.2 Soft-Start and Enable Delay

To ensure that there is not a large inrush current or overshoot of output voltage at the output of the buck regulator, the RAA271050 has four programmable time settings for soft-start. Figure 20 shows this timing as t_3-t_4.

Also, to allow more flexibility for sequencing when using the RAA271050, there is an additional programmable t_{ON} delay of 0ms to 63ms from when the Enable pin is asserted high. Figure 20 shows this timing as t_2-t_3. When the Enable pin de-asserts, the RSTb pin asserts low, and there is a programmable delay (t_{OFF}) for when the output of the Buck stops regulating. Figure 20 shows this timing as t_6-t_7.



Notes:
1) Timing diagram is not drawn to scale.
2) $t_2 - t_1$ = 1.5ms
3) $t_3 - t_2$ = Programmable (0ms – 63ms)
4) $t_4 - t_3$ = Programmable (See Table 1. Soft-Start Timing Values.)
5) $t_5 - t_4$ = 1.5ms
6) $t_7 - t_6$ = Programmable (0ms – 63ms)

Figure 20. Soft-Start Timing

Table 1. Soft-Start Timing Values

Nominal Soft-Start Time (ms)	Maximum Soft-Start Time (f_{SW} = 440kHz) (ms)	Maximum Soft-Start Time (f_{SW} = 2.0MHz) (ms)
1.28	2.11	1.44
2.56	4.23	2.89
5.12	8.46	5.79
12.8	21.15	14.47

5.3 Output Undervoltage and Overvoltage Protection

The RAA271050 offers undervoltage (UV) and overvoltage (OV) protection thresholds for the buck and the VCCP regulator. The buck UV and OV sense point is at the VOUT_S pin; the undervoltage protection threshold is factory programmable and can be set to -6%, -8%, -12% of the programmed output voltage, or a fixed 2.8V. The fixed 2.8V setting allows the buck to operate in dropout. If the output voltage drops below the programmed threshold, the regulator disables and the RSTb signal toggles low.

Like undervoltage protection, the overvoltage protection threshold is also programmable to settings of +6%, +8%, or +12% of the programmed output voltage setting. If the output voltage exceeds the programmed threshold, the regulator disables and the RSTb signal toggles low.

5.4 Input Undervoltage Lockout

The VIN Undervoltage Lockout (UVLO) has, by default, a fixed rising edge of 4.5V (typical) and a falling edge of 3.65V (typical).

Note: VIN must exceed the rising UVLO threshold before the IC can power up, and the enable voltage is $>V_{IH_LDO}$. Although the device can operate with VIN as low as 4V, the device cannot start up until VIN reaches 4.5V.

While the regulator operates with input voltages as low as 4V, the output voltage of the buck and VCCP can fall below regulation if the input voltage drops too low to maintain the output voltage under existing load and temperature conditions.

5.5 EN Input

EN is an input pin that can tolerate voltages up to $42V_{DC}$ and can be connected directly to VIN.

The following describes the different behaviors of the RAA271050, based on the voltage level of the EN pin:

- If EN < V_{IL_LDO}, the device is fully shut down, and the current drawn from V_{IN} is typically < 1µA.
- If EN > V_{IH_LDO} but EN < V_{IH_BUCK}, the internal LDO regulator VCCP turns on and begins to regulate to 4.3V. This LDO provides the bias circuitry to the IC in addition to the bias circuitry to the monitoring portion of the IC through the VCC pin.
- If EN > V_{IH_BUCK}, the device begins the startup cycle for the buck regulator.

5.6 RSTb Output

The RSTb pin has dual functionality; it serves as a fault indicator, and it also serves as a conventional PGOOD indicator when it is high. RSTb is a push-pull output voltage pin whose logic high level depends on whether the bypass feature is used. When BYP is < V_{BYP_R}, the high level of the RSTb pin is VCC minus a diode drop. However, when the BYP > V_{BYP_R}, the high level of the RSTb pin is BYP minus a diode drop. In RCAR applications, the RSTb pin is typically connected to the enable pin of the RCAR processor PMIC.

The dual functionality of the RSTb pin ensures that whether a Monitor fault or regulation fault occurs, the RSTb pin toggles low. If a Monitor fault occurs, there is a programmable debounce time that delays the reaction of RSTb pin toggling low. If the fault recovers within the debounce time, RSTb does not toggle low. This debounce time is programmable to 12.5µs, 25µs, 50µs, or 100µs.

5.7 Monitors

The RAA271050 has implemented self-diagnostics to ensure that the IC is always functioning at its optimal performance. It also lets the system know through the RSTb pin if its internal systems are not operating under expected conditions.

These internal systems are:

- FB Monitor – FB Monitor monitors VOUT_S voltage for undervoltage (UV) and overvoltage (OV) conditions. As specified in Output Undervoltage and Overvoltage Protection, the (UV) threshold is factory programmable to be set to -6%, -8%, -12% of the programmed output voltage or a fixed 2.8V, and the (OV) threshold is programmable to settings of +6%, +8%, or +12% of the programmed output voltage setting. An FB Monitor fault occurs if the VOUT_S pin exceeds the expected range and the RSTb pin asserts low.
- VBG Monitor – The RAA271050 has two independent bandgaps within the IC. The VBG Monitor serves as a bandgap health check for both bandgaps and ensures they are within 10% of each other.
- PGND Monitor – The PGND Monitor detects whether PGND bond wires become disconnected. The PGND and AGND pins are internally compared, and if their difference to each other varies by more than 250mV, a Monitor fault is detected, and the RSTb pin toggles low. (PGND - AGND) > 250mV results in a PGND OV Monitor fault, and (PGND - AGND) < 250mV results in a PGND UV Monitor fault, and the RSTb pin asserts low.
- RSTb Monitor – During the start-up of the buck regulator, the IC compares the voltage level of the RSTb pin to a 300mV internal reference. If the level is as expected, the buck regulator continues with its start-up sequence. However, if the level is higher than this 300mV reference, the RSTb pin asserts low, and the buck regulator does not attempt to start up.
- VCC Monitor – VCC Monitor detects whether VCC exceeds the acceptable range. Monitor faults if VCC goes above the OV threshold (typical 5.375V) or below the UV threshold (typical 3.3V).
- CLK Monitor – CLK Monitor monitors the system clock for under-frequency, over-frequency, and high/low conditions. The typical over-frequency threshold is +50% of the CLK frequency, and the typical under-frequency threshold is -50% of the CLK frequency. An over-frequency or under-frequency fault triggers if the clock frequency reaches the respective threshold.
- AFSM Monitor – The Asynchronous Finite State Machine (AFSM) allows for proper sequencing from BIST to normal Buck operation. If a fault occurs, it sequences to the Monitor fault state with the RSTb pin asserted low. Additionally, a redundant AFSM checks the state of the main AFSM. If these two state machines do not agree, an AFSM fault is triggered.
- Thermal Shutdown Monitor – If the junction temperature typically exceeds +160°C, the output of the regulator shuts down, and a primary regulator restart (EN toggling) needs to occur for the output voltage to regulate again. The IC continues to monitor the temperature through the Regulation Thermal Shutdown, which disables the IC (Regulation and Monitoring) if the temperature exceeds +170°C. The IC remains off until the junction temperature cools down to typically +155°C.

5.8 Overcurrent Protection

The RAA271050 offers multiple current protection that limits the inductor current. With this feature, it helps to protect from overload current or a short-circuit.

The following are the current protections:

- High-Side Overcurrent (HSOC) – The high-side current limit is cycle-by-cycle protection and detects the inductor current when it is too high. If the current flowing through the high-side FET is higher than the threshold (HSOC), the high-side driver turns off the high-side FET. If the high-side FET cannot turn off fast enough and the current continues to increase, another overcurrent comparator trips at a secondary threshold (HSOC2). If the second overcurrent comparator trips, the buck latches off.
- Low-Side Overcurrent (LSOC)/Negative Overcurrent (NOC) – The low-side current limit uses the low-side FET to sense the load current and detect for positive current limit and negative current limit. The typical positive current limit is 6.5A, and the negative current limit is -3A. The respective LSOC or NOC fault is triggered if a low-side current limit is detected. If the LSOC comparator trips, the buck latches off. If the NOC comparator trips, the low-side FET turns off.

5.9 Hiccup/Latch-Off

The RAA271050 response to a fault can be programmed to either hiccup mode or latch-off. When hiccup mode is selected and a fault occurs, the regulator stops switching for 200ms before attempting to restart. If the fault

continues to persist, the regulator continues hiccuping every 200ms until the fault is cleared. When latch-off is selected and a fault occurs, the regulator stops switching and stays off until power is cycled or EN is toggled.

5.10 Pulse Skipping

The pulse skipping function is enabled when V_{IN} typical voltage level is above 19V. Occasionally high pulses in the PHASE switching node are skipped when enabled, allowing for a lower switching frequency.

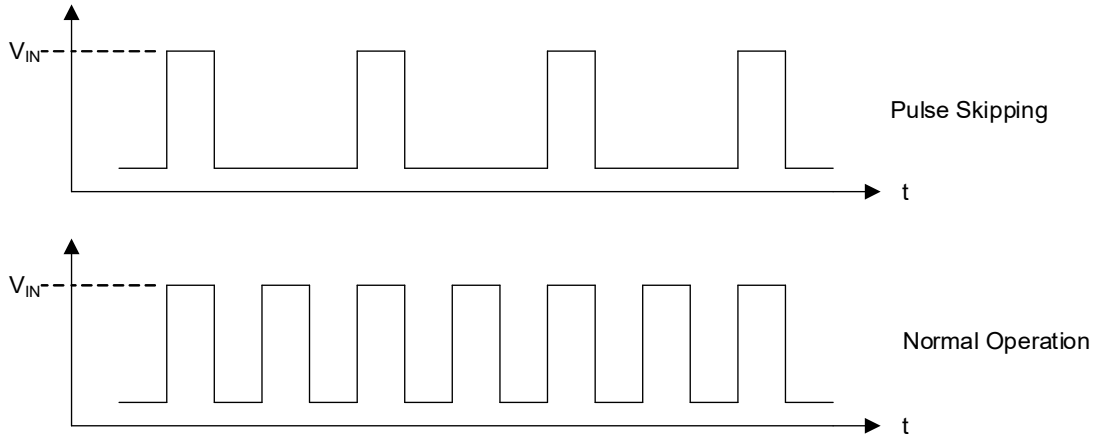


Figure 21. Pulse Skipping Feature

5.11 Recommended Component Setting

Depending on the switching frequency setting, the recommended inductor and output capacitor values are provided in Table 2. The inductor should be selected to handle the maximum pulse current and output voltage across the temperature range. These component values provide the best stability and transient response. De-rating because of operating conditions, such as bias voltage, temperature, and size, should be considered part of the output capacitor selection.

Table 2. Recommended Inductor and Output Capacitor Values

V_{OUT} (V)	f_{SW} (kHz)	L (µH)	C_{OUT}
5.0	440	10	2×47µF
3.3	440	10	2×47µF
5.0	2200	2.2	1×47µF
3.3	2200	2.2	1×47µF

5.12 Layout Guidelines

For optimal performance, the placement of the capacitors should be symmetrical across the RAA271050. Place one small 1µF input capacitor close to each side of the RAA271050, Pins 3, 4, and Pins 13, 14. Place an additional 10µF capacitor parallel to each of the small 1µF capacitors. Cluster the output capacitors near the inductor to minimize the power loop from V_{IN} to GND. Choose these capacitors with proper voltage rating to avoid capacitor degrading, which can cause regulator instability.

The Buck regulator power delivery loop consists of the output inductor (L), the output capacitor (C_{OUT}), the PHASE switching node pins, and the PGND pins.

Important: Make the power delivery or current flow loop as small as possible. The PCB connecting traces among these components and pins should be direct, short, and wide. Apply the same practice to the trace connections of the VIN pins, the input capacitor (C_{IN}), and PGND.

The PCB copper for the input voltage (V_{IN}) and the output voltage (V_{OUT}) should be wide enough to minimize the current conduction loss. It is helpful to have multiple solid ground layers to reduce the current flow resistance, improve thermal dissipation, and improve EMI performance. Remember to use enough vias to connect all the GND layers.

Figure 22 shows the recommended component layout.

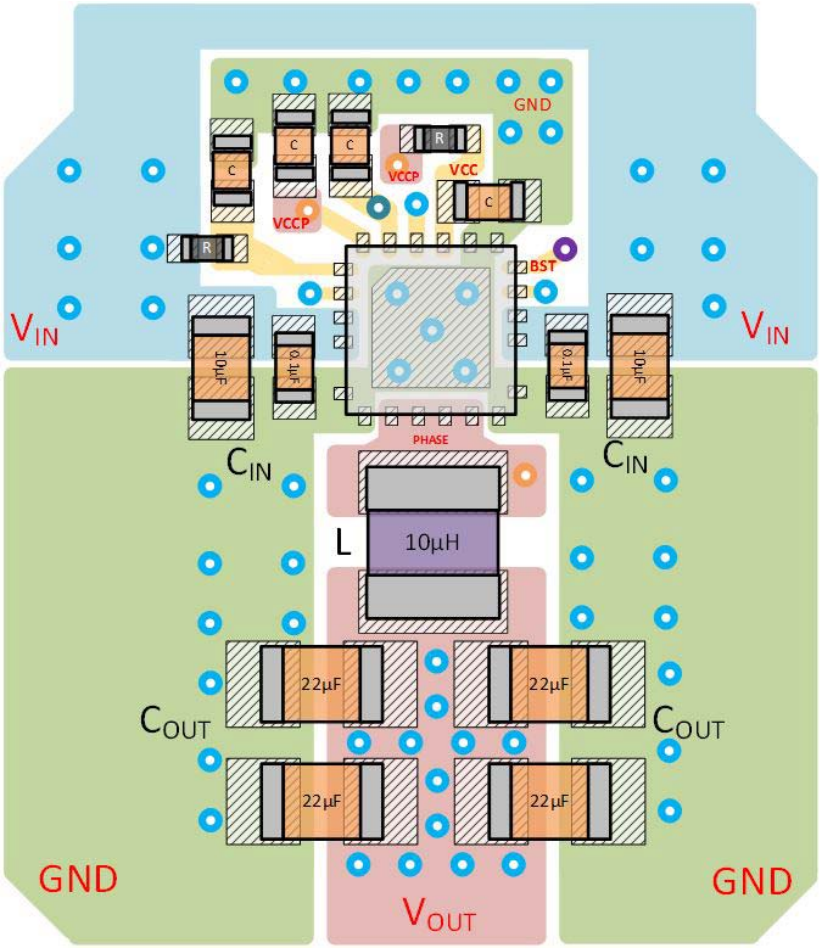


Figure 22. RAA271050 Recommended Layout (Top View)

List of guidelines for the RAA271050 layout:

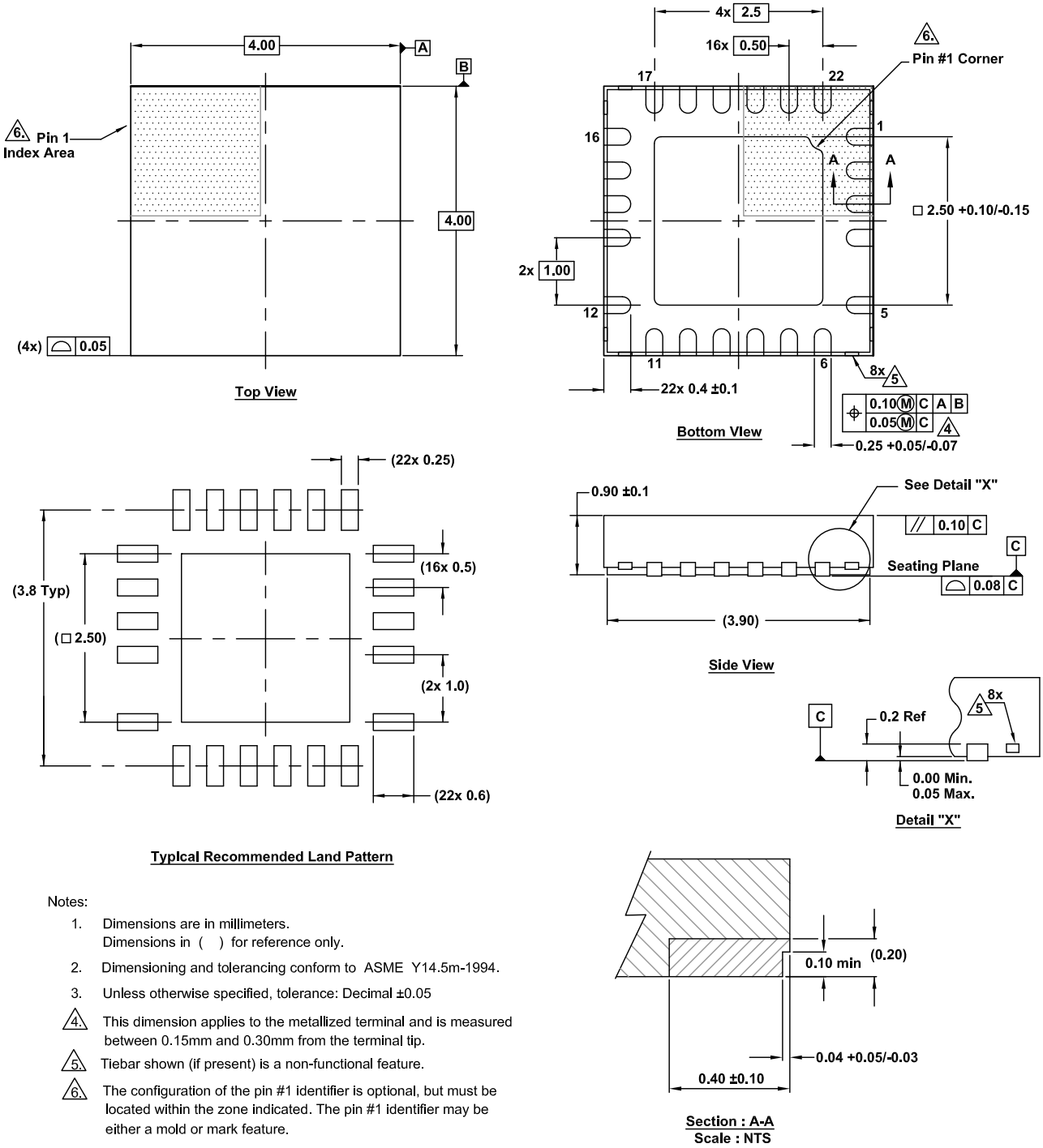
- Place the input capacitors as close as possible to the VIN and PGND pins.
- Route the Buck switching phase nodes with short, wide traces, and avoid any sensitive signals.
- Route output voltage sensing traces to the load point and the high frequency ceramic bank to minimize the feedback noise.
- Run the output voltage sensing traces away from the switching BST and PHASE via/trace/copper and high-speed digital signals, shield with GND copper.
- Minimize the input capacitor GND and the output capacitor GND distance and resistance.
- Use enough vias and PCB trace width for improved current flow capacity.
- Further improvement of θ_{JA} is made through better PCB design, air flow through the part, or a combination of both. These parameters depend on the target design requirement and goals of the customer.

6. Package Outline Drawing

For the most recent package outline drawing, see L22.4x4.

L22.4x4

22 Lead Step Cut Quad Flat No-Lead Plastic Package (SCQFN)
Rev 0, 1/19



Notes:

1. Dimensions are in millimeters.
   Dimensions in ( ) for reference only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ±0.05
4. This dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

7. Ordering Information

Part Number[1][2]	Part Marking	f_{SW} (Hz)	V_{OUT} (V)	Package Description[3] (RoHS Compliant)	Pkg. Dwg. #	Carrier Type[4]	Temp Range
RAA2710504R42HNP#HA0	27105 0D4HN	440k	3.3	22 Ld QFN	L22.4x4	Reel, 6k	-40 to +125°C
RAA2710504R43HNP#HA0		2.2M					
RAA2710504R44HNP#HA0		440k	5.0				
RAA2710504R45HNP#HA0		2.2M					
RTKA271050E00010BU	Evaluation Kit						

1. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. The Moisture Sensitivity Level (MSL) rating is 3. For more information about MSL, see TB363.
3. For the Pb-Free Reflow Profile, see TB493.
4. See TB347 for details about reel specifications.

Table 3. Default Settings

Soft-Start Time	Output ON Delay	Output OFF Delay	V_{OUT} UV Threshold	V_{OUT} OV Threshold	Debounce Time	Spread Spectrum	Hiccup
3.5ms	0ms	63ms	2.8V	+12%	25µs	OFF	Enabled

8. Revision History

Rev.	Date	Description
1.03	Nov 11, 2026	In the Soft-Start and Enable Delay section: ▪ Updated the Notes in Figure 20. ▪ Added Table 1.
1.02	May 13, 2026	Updated Figure 4.
1.01	Aug 22, 2024	In 3.2 Thermal Specifications, added footnote 1. In 3.4 Electrical Specifications, corrected Health Check parameter to Thermal Shutdown Monitor. In 4. Typical Performance Curves, updated Figures 6 to 13. In 5.7 Monitors, updated description of Thermal Shutdown Monitor. In 5.12 Layout Guidelines, added final layout guideline. In 7. Ordering Information, corrected Table 2 heading from Speed Spectrum to Spread Spectrum.
1.00	Jul 11, 2023	Initial release

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