

# N0400P

R07DS0500EJ0200

Rev.2.00

Aug 19, 2011

## MOS FIELD EFFECT TRANSISTOR

### Description

The N0400P is P-channel MOS Field Effect Transistor designed for high current and 2.5 V drive switching applications.

### Features

- 2.5 V drive available
- Super low on-state resistance  
 $R_{DS(on)1} = 40 \text{ m}\Omega \text{ MAX. (} V_{GS} = -4.5 \text{ V, } I_D = -7.5 \text{ A)}$   
 $R_{DS(on)2} = 73 \text{ m}\Omega \text{ MAX. (} V_{GS} = -2.5 \text{ V, } I_D = -3.8 \text{ A)}$
- Built-in gate protection diode

### Ordering Information

PART NUMBER	LEAD PLATING	PACKING	PACKAGE
N0400P-ZK-E1-AY <sup>Note</sup>	Pure Sn (Tin)	Tape 2500 p/reel	TO-252 (MP-3ZK)
N0400P-ZK-E2-AY <sup>Note</sup>			

**Note** Pb-free (This product does not contain Pb in external electrode.)

### Absolute Maximum Ratings ( $T_A = 25^\circ\text{C}$ )

Drain to Source Voltage ( $V_{GS} = 0 \text{ V}$ )	$V_{DSS}$	-40	V
Gate to Source Voltage ( $V_{DS} = 0 \text{ V}$ )	$V_{GSS}$	$\mp 12$	V
Drain Current (DC) ( $T_C = 25^\circ\text{C}$ )	$I_{D(DC)}$	$\mp 15$	A
Drain Current (pulse) <sup>Note1</sup>	$I_{D(pulse)}$	$\mp 45$	A
Total Power Dissipation ( $T_C = 25^\circ\text{C}$ )	$P_{T1}$	25	W
Total Power Dissipation ( $T_A = 25^\circ\text{C}$ )	$P_{T2}$	1.0	W
Channel Temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$
Single Avalanche Current <sup>Note2</sup>	$I_{AS}$	-16	A
Single Avalanche Energy <sup>Note2</sup>	$E_{AS}$	25	mJ

**Notes 1.**  $PW \leq 10 \mu\text{s}$ , Duty Cycle  $\leq 1\%$

**2.** Starting  $T_{ch} = 25^\circ\text{C}$ ,  $V_{DD} = -20 \text{ V}$ ,  $R_G = 25 \Omega$ ,  $V_{GS} = -12 \rightarrow 0 \text{ V}$

### Thermal Resistance

Channel to Case Thermal Resistance	$R_{th(ch-C)}$	5.0	$^\circ\text{C/W}$
Channel to Ambient Thermal Resistance	$R_{th(ch-A)}$	125	$^\circ\text{C/W}$

The mark <R> shows major revised points.

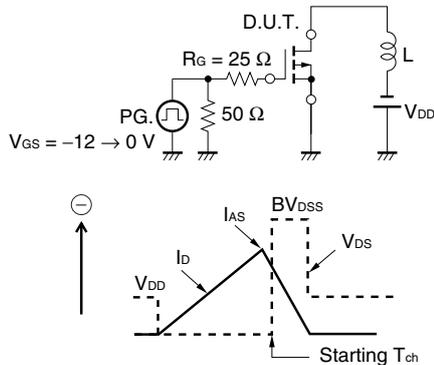
The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

Electrical Characteristics (T<sub>A</sub> = 25°C)

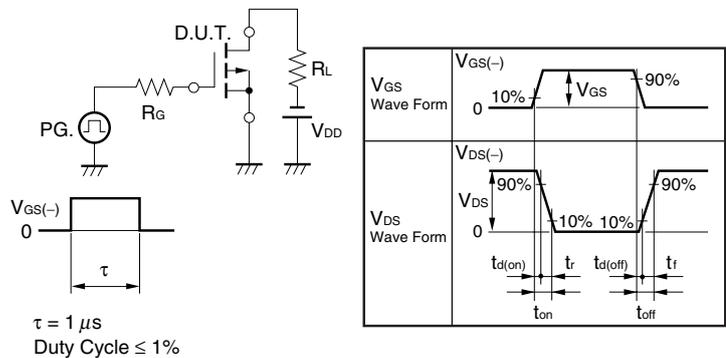
	CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = -40 V, V <sub>GS</sub> = 0 V			-10	μA
<R>	Gate Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±12 V, V <sub>DS</sub> = 0 V			±10	μA
	Gate to Source Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -1 mA	-0.5	-1.0	-1.5	V
	Forward Transfer Admittance <sup>Note</sup>	y <sub>fs</sub>	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -7.5 A	6.0			S
	Drain to Source On-state Resistance <sup>Note</sup>	R <sub>DS(on)1</sub>	V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -7.5 A		31	40	mΩ
		R <sub>DS(on)2</sub>	V <sub>GS</sub> = -2.5 V, I <sub>D</sub> = -3.8 A		40	73	mΩ
<R>	Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = -10 V,		1400		pF
	Output Capacitance	C <sub>OSS</sub>	V <sub>GS</sub> = 0 V,		200		pF
	Reverse Transfer Capacitance	C <sub>rss</sub>	f = 1 MHz		155		pF
	Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = -20 V, I <sub>D</sub> = -7.5 A,		11		ns
	Rise Time	t <sub>r</sub>	V <sub>GS</sub> = -4.5 V,		16		ns
	Turn-off Delay Time	t <sub>d(off)</sub>	R <sub>G</sub> = 0 Ω		104		ns
	Fall Time	t <sub>f</sub>			93		ns
	Total Gate Charge	Q <sub>G</sub>	V <sub>DD</sub> = -32 V,		16		nC
	Gate to Source Charge	Q <sub>GS</sub>	V <sub>GS</sub> = -4.5 V,		3		nC
	Gate to Drain Charge	Q <sub>GD</sub>	I <sub>D</sub> = -15 A		7		nC
	Body Diode Forward Voltage <sup>Note</sup>	V <sub>F(S-D)</sub>	I <sub>F</sub> = -15 A, V <sub>GS</sub> = 0 V		0.94	1.5	V
<R>	Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = -15 A, V <sub>GS</sub> = 0 V,		31		ns
	Reverse Recovery Charge	Q <sub>rr</sub>	di/dt = -100 A/μs		33		nC

Note Pulsed: PW ≤ 350 μs, Duty Cycle ≤ 2%

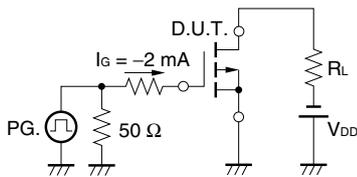
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

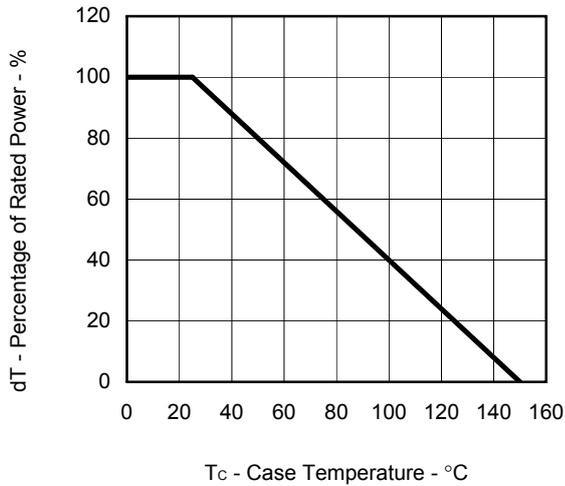


TEST CIRCUIT 3 GATE CHARGE

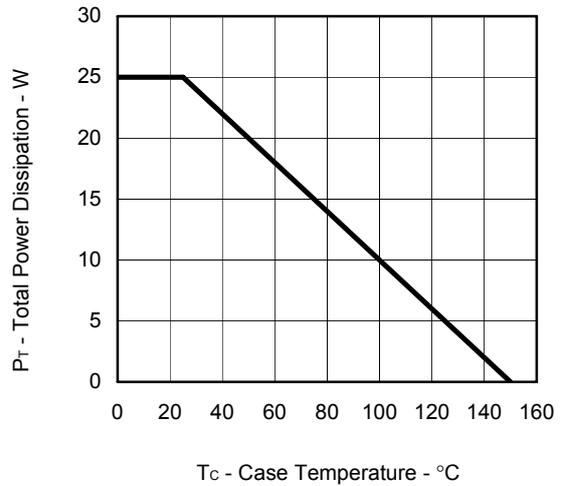


Typical Characteristics (T<sub>A</sub> = 25°C)

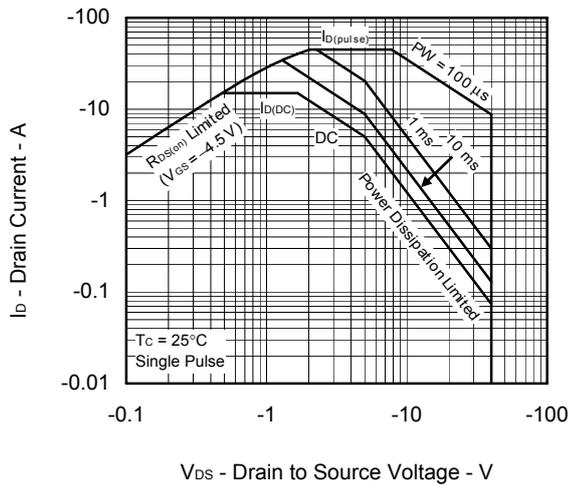
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



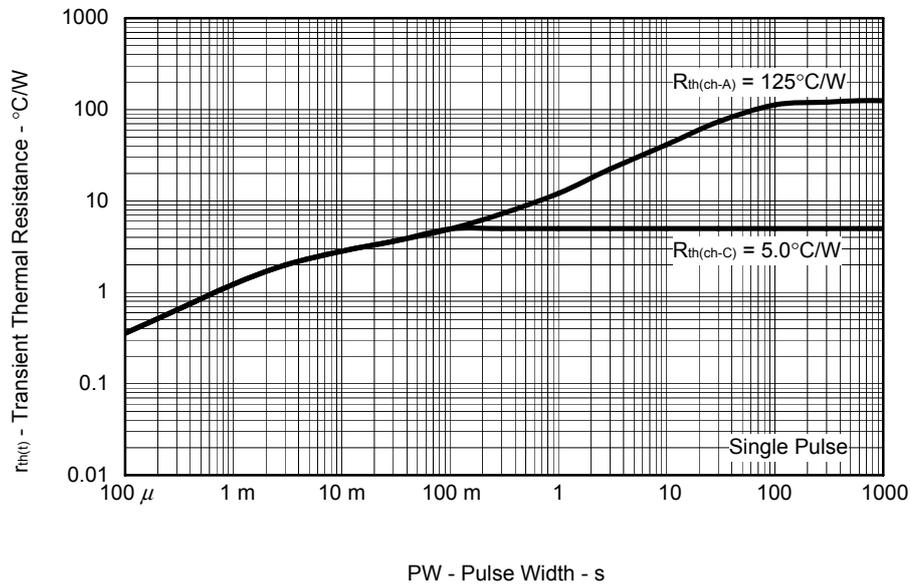
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



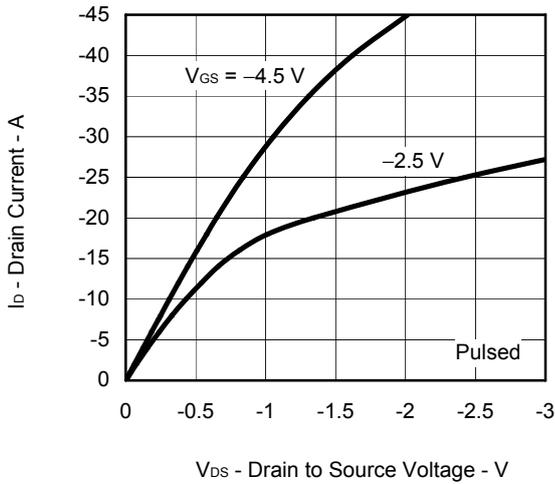
FORWARD BIAS SAFE OPERATING AREA



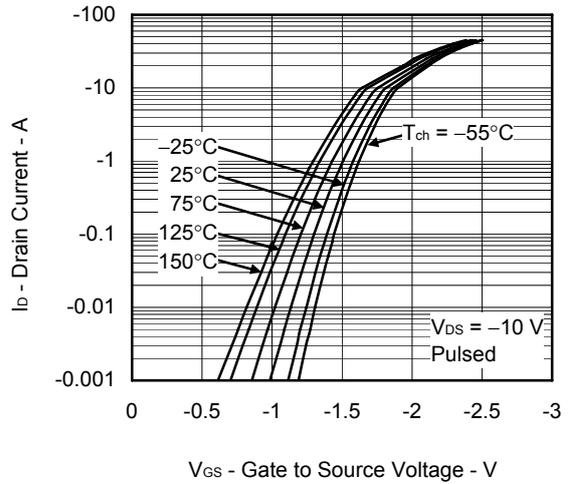
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



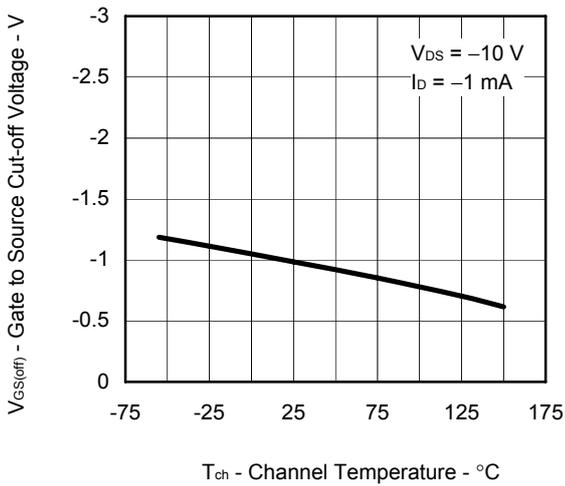
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



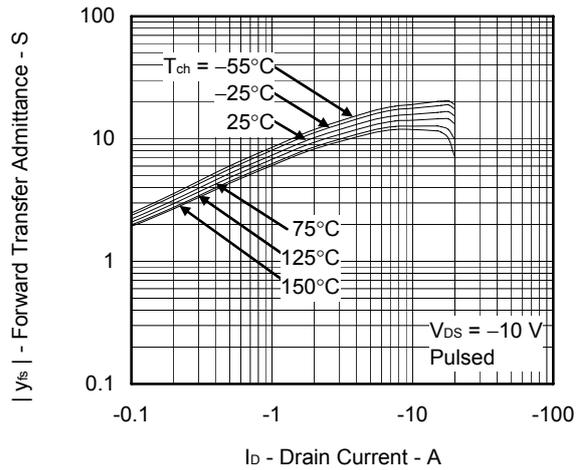
FORWARD TRANSFER CHARACTERISTICS



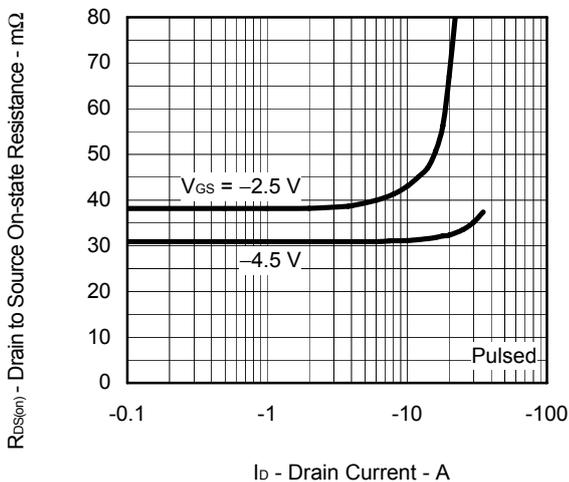
GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



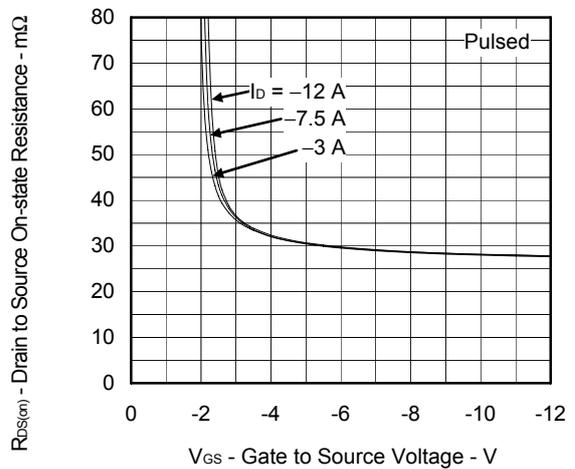
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



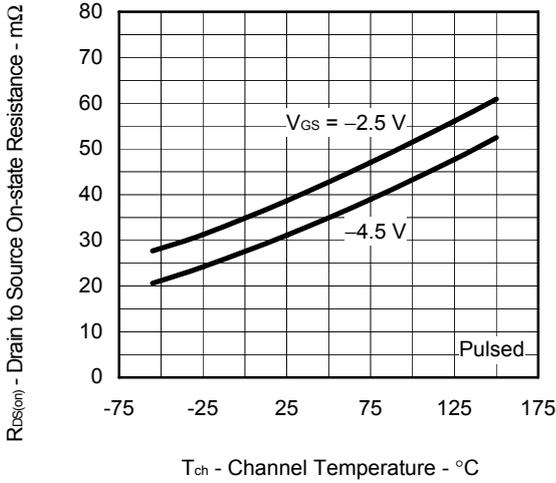
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



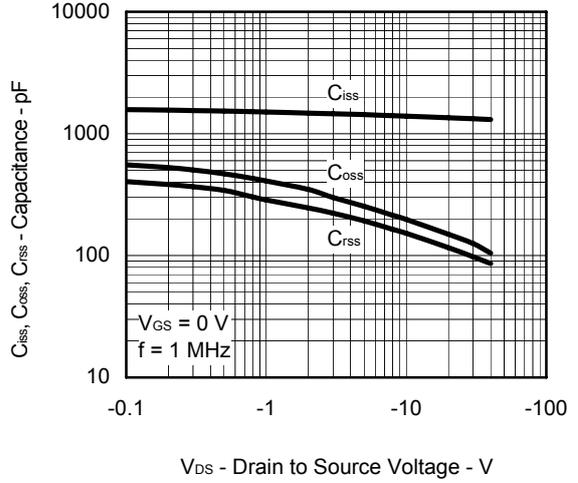
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



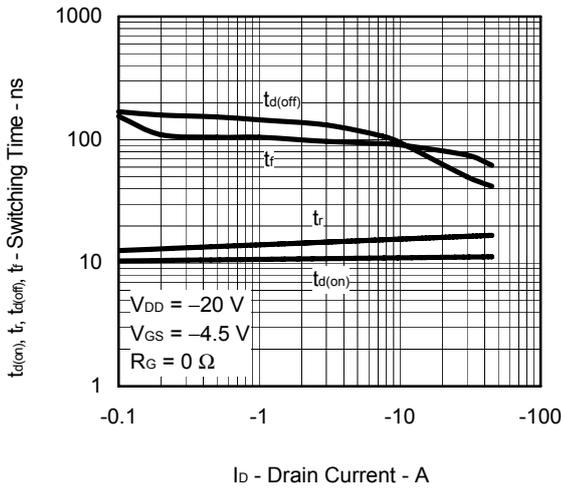
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



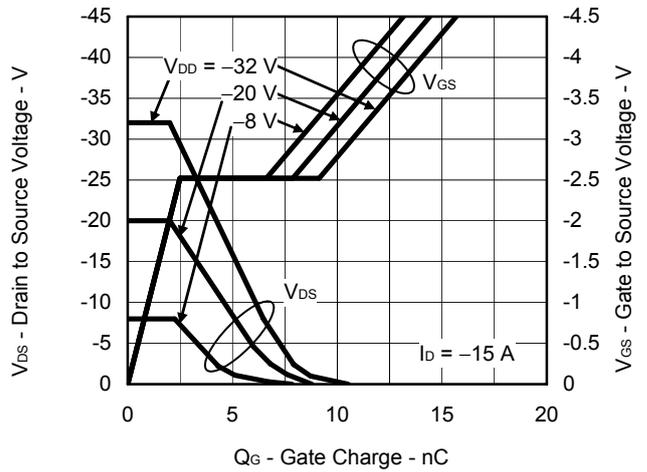
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



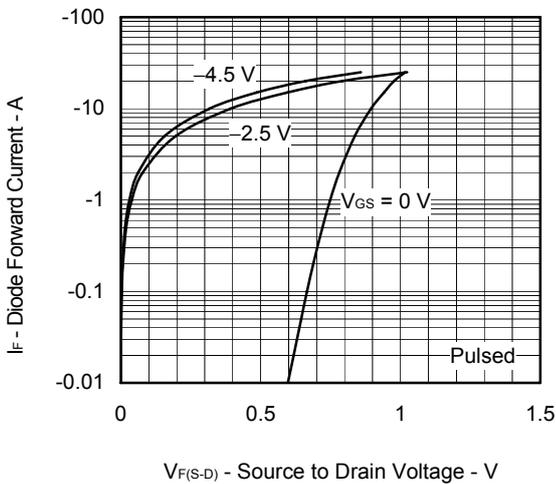
SWITCHING CHARACTERISTICS



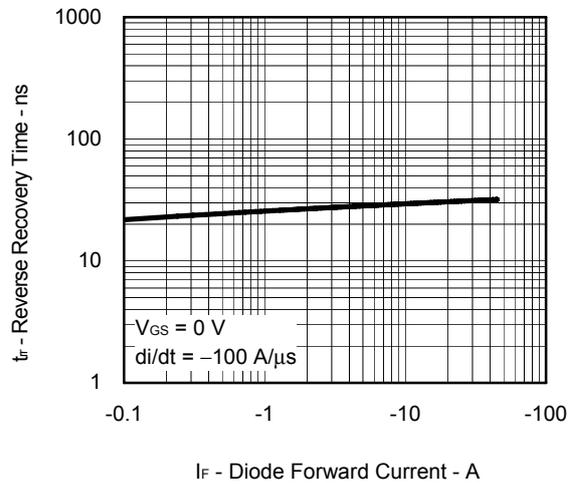
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



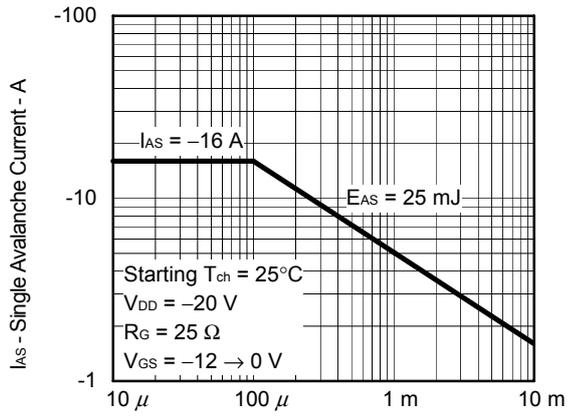
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT

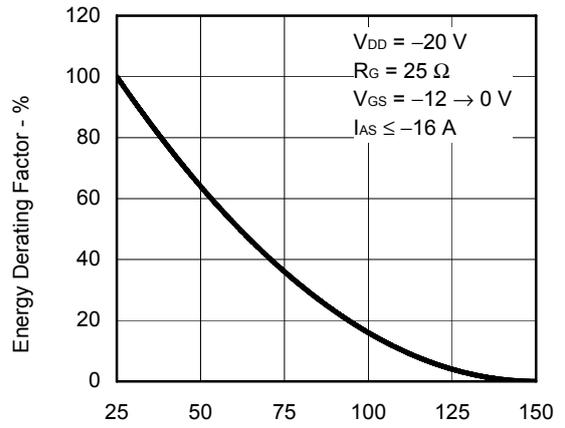


SINGLE AVALANCHE CURRENT vs.  
INDUCTIVE LOAD



L - Inductive Load - H

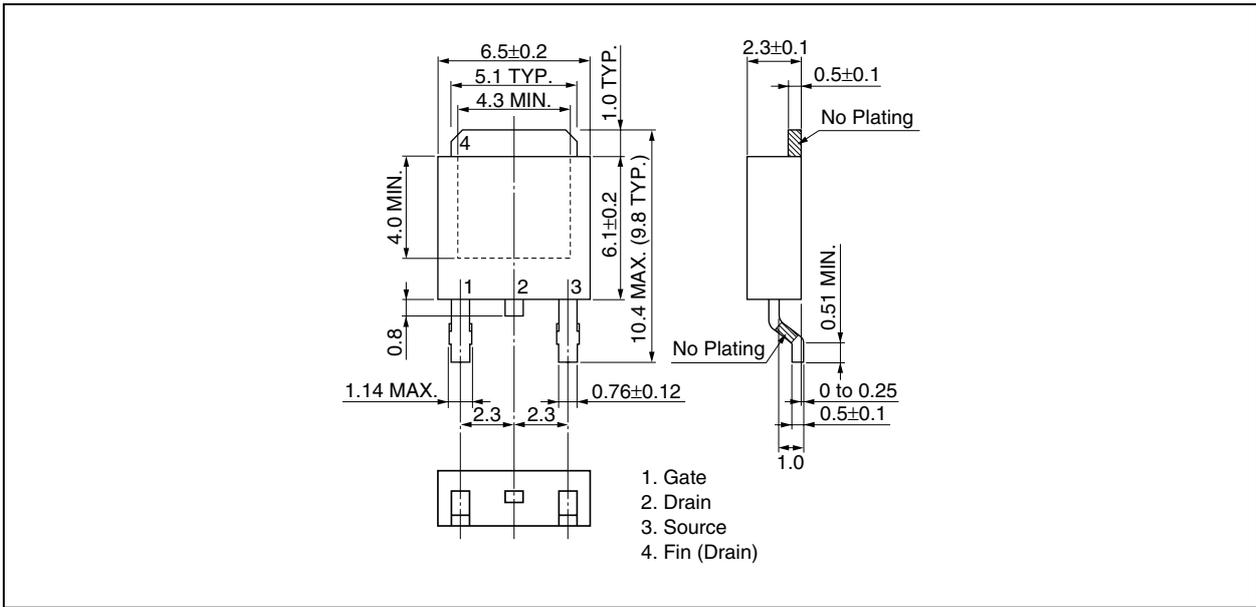
SINGLE AVALANCHE ENERGY  
DERATING FACTOR



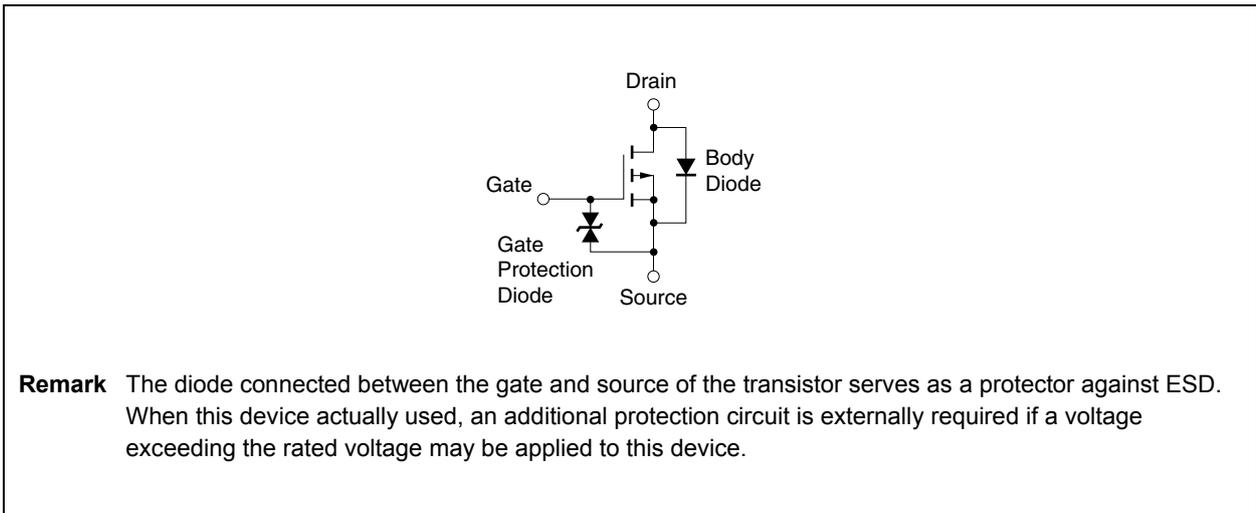
Starting  $T_{ch}$  - Starting Channel Temperature -  $^\circ\text{C}$

Package Drawings (Unit: mm)

TO-252 (MP-3ZK)



Equivalent Circuit



<b>Revision History</b>	<b>N0400P Data Sheet</b>
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Rev.	Date	Description	
		Page	Summary
-	Feb 2011	-	Previous No. : D19676EJ1V0DS00
2.00	Aug 19, 2011	p.2	Modification of <b>Electrical Characteristics</b>

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