Low-Power Off-Line Digital Green-Mode PWM Controller

1 Description

The iW1707 is a high performance AC/DC power supply controller which uses digital control technology to build peak current mode PWM flyback power supplies. The device directly drives a power BJT and operates in quasi-resonant mode to provide high efficiency along with a number of key built-in protection features while minimizing the external component count, simplifying EMI design and lowering the total bill of material cost. The iW1707 features a distinctive soft-start scheme, which allows for fast and yet smooth start-up with both small and large capacitive loads. The iW1707 removes the need for secondary feedback circuitry while achieving excellent line and load regulation. It also eliminates the need for loop compensation components while maintaining stability over all operating conditions. Pulse-by-pulse waveform analysis allows for a loop response that is much faster than traditional solutions, resulting in improved dynamic load response. The built-in power limit function enables optimized transformer design in universal off-line applications and allows for a wide input voltage range.

Dialog's innovative propietary technology ensures that power supplies built with the iW1707 can achieve both highest average efficiency and less than 100mW no-load consumption, and have fast yet smooth start-up with a wide range of capacitive loads with output voltage up to 12V, and are ideal for network and home appliance power supplies applications.

2 Features

- Primary-side feedback eliminates optoisolators and simplifies design
- Adaptively controlled soft start enables fast and smooth start-up for a wide range of capacitive loads (from 330µF to 6,000µF)
- Active start-up scheme enables shortest possible turn-on delay
- Direct drive of low-cost BJT switch
- Very tight constant voltage regulation
- ***EZ-EMI***® design enhances manufacturability
- Intrinsically low common mode noise
- Optimized 72kHz maximum PWM switching frequency achieves best size and efficiency
- Adaptive multi-mode PWM/PFM control improves efficiency
- Quasi-resonant operation for highest overall efficiency
- Dynamic base current control
- No external compensation components required
- Complies with EPA 2.0 energy-efficiency specifications with ample margin
- Built-in short circuit protection and output overvoltage protection
- Built-in current sense resistor short circuit protection
- Constant current control enables output current limit and overload protection
- No audible noise over entire operating range

3 Applications

- Network power adapters for ADSL, wireless access points, routers
- AC/DC power supplies in home appliances

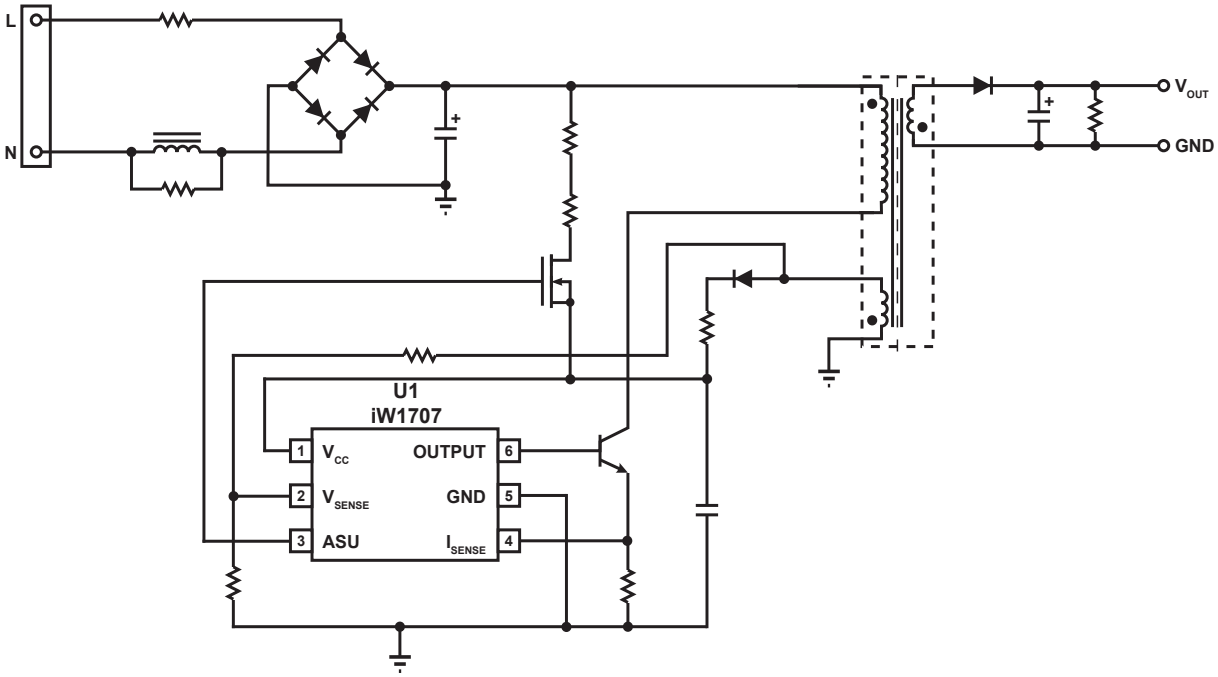


Figure 3.1 : iW1707 Typical Application Circuit
(Using Depletion Mode NFET as Active Start-up Device)

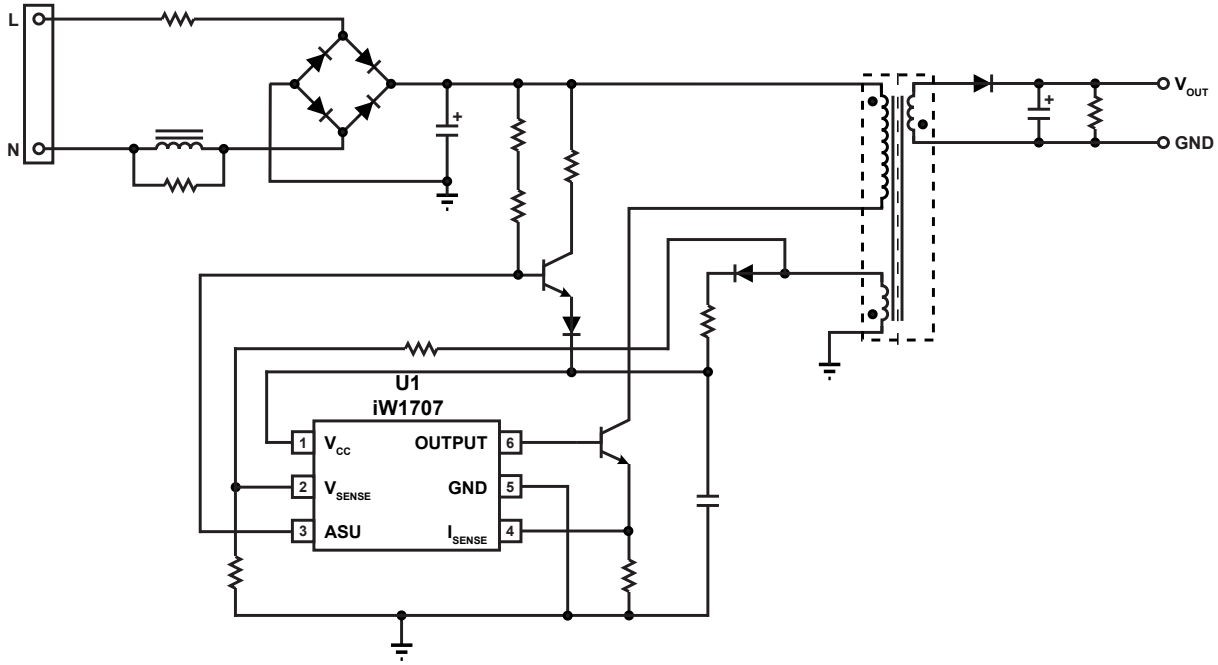


Figure 3.2 : iW1707 Alternate Application Circuit
(Using NPN BJT as Active Start-up Device)

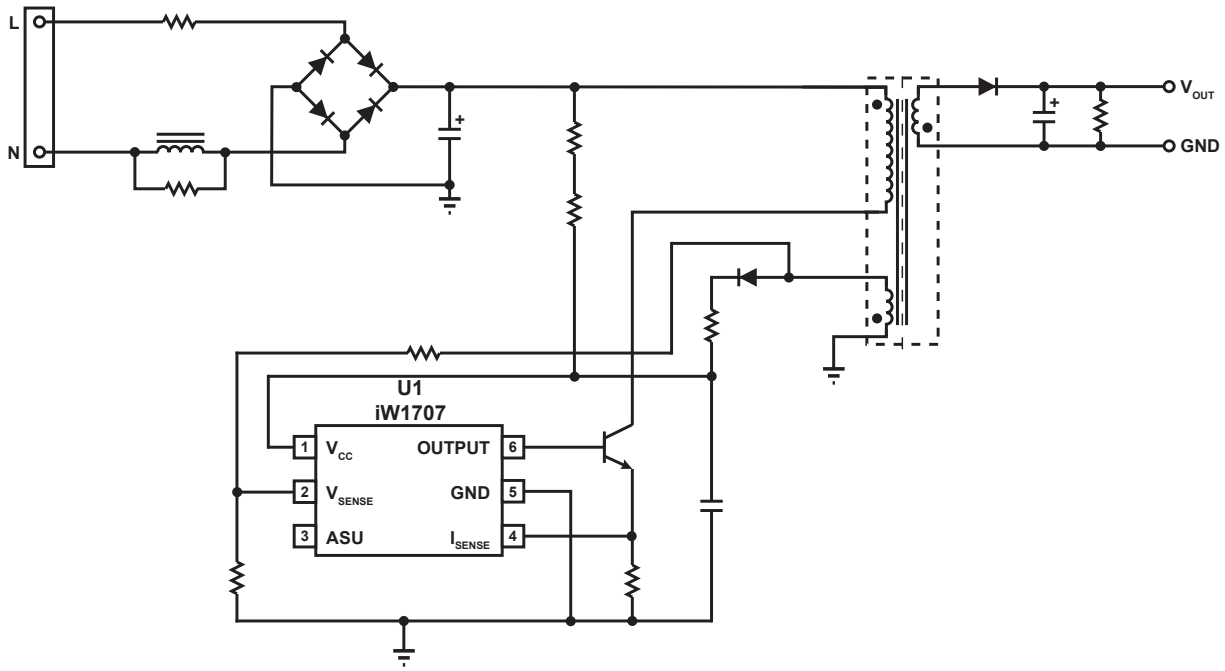


Figure 3.3 : iW1707 Alternate Application Circuit without Active Start-up Device
Pin 3 (ASU) can be left unconnected if an active start-up device is not needed in the application circuit

4 Pinout Description

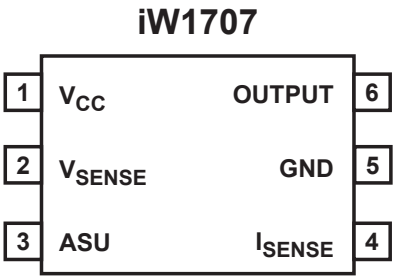


Figure 4.1 : 6 Lead SOT-23 Package

Pin Number	Pin Name	Type	Pin Description
1	V_{CC}	Power Input	Power supply for control logic.
2	V_{SENSE}	Analog Input	Auxiliary voltage sense (used for primary regulation).
3	ASU	Output	Control signal for active start-up device (BJT or depletion NFET).
4	I_{SENSE}	Analog Input	Primary current sense. Used for cycle-by-cycle peak current control and limit.
5	GND	Ground	Ground.
6	OUTPUT	Output	Base drive for BJT.

5 Absolute Maximum Ratings

Absolute maximum ratings are the parameter values or ranges which can cause permanent damage if exceeded. For maximum safe operating conditions, refer to Electrical Characteristics in Section 6.

Parameter	Symbol	Value	Units
DC supply voltage range (pin 1, I_{CC} = 20mA max)	V_{CC}	-0.3 to 18	V
Continuous DC supply current at V_{CC} pin (V_{CC} = 15 V)	I_{CC}	20	mA
ASU output (pin 3)		-0.3 to 18	V
OUTPUT (pin 6)		-0.3 to 4.0	V
V_{SENSE} input (pin 2, I_{VSENSE} ≤ 10 mA)		-0.7 to 4.0	V
I_{SENSE} input (pin 4)		-0.3 to 4.0	V
Maximum junction temperature	$T_{J\ MAX}$	150	°C
Storage temperature	T_{STG}	-65 to 150	°C
Lead temperature during IR reflow for ≤ 15 seconds	T_{LEAD}	260	°C
Thermal Resistance Junction-to-Ambient	θ_{JA}	190	°C/W
ESD rating per JEDEC JESD22-A114		±2,000	V
Latch-Up test per JESD78D		±100	mA

6 Electrical Characteristics

V_{CC} = 12V, -40°C ≤ T_A ≤ 85°C, unless otherwise specified.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
V_{SENSE} SECTION (Pin 2)						
Input leakage current	I_{BVS}	V_{SENSE} = 2V			1	µA
Nominal voltage threshold	$V_{SENSE(NOM)}$	T_A = 25°C, negative edge	1.518	1.533	1.548	V
Output OVP threshold -00 (Note 1)	$V_{SENSE(MAX)}$	T_A = 25°C, negative edge		1.834		V
Output OVP threshold -01 (Note 1)	$V_{SENSE(MAX)}$	T_A = 25°C, negative edge Load = 100%		1.855		V
Output OVP threshold -03 (Note 1)	$V_{SENSE(MAX)}$	T_A = 25°C, negative edge Load = 100%		1.901		V
I_{SENSE} SECTION (Pin 4)						
Overcurrent threshold	V_{OCP}	On state	1.11	1.15	1.19	V
I_{SENSE} regulation upper limit (Note 3)	$V_{IPK(HIGH)}$			1.00		V
I_{SENSE} regulation lower limit (Note 3)	$V_{IPK(LOW)}$			0.23		V
Input leakage current	I_{LK}	I_{SENSE} = 1.0V			1	µA
OUTPUT SECTION (Pin 6)						
Output low level ON-resistance	$R_{DS(ON)LO}$	I_{SINK} = 5mA		1	3	Ω
Switching frequency (Note 2)	f_{SW}	> 50% load		72		kHz
V_{CC} SECTION (Pin 1)						
Maximum operating voltage (Note 1)	$V_{CC(MAX)}$				16	V
Start-up threshold	$V_{CC(ST)}$	V_{CC} rising	10.0	11.0	12.0	V
Undervoltage lockout threshold	$V_{CC(UVL)}$	V_{CC} falling	3.8	4.0	4.2	V
Start-up current	$I_{IN(ST)}$	V_{CC} = 10V	1.0	1.7	3.0	µA
Quiescent current	I_{CCQ}	No I_B current		2.7	4.0	mA
Zener breakdown voltage	V_{ZB}	Zener current = 5mA T_A = 25°C	18.5	19.5	20.5	V
ASU SECTION (Pin 3)						
Maximum operating voltage (Note 1)	$V_{ASU(MAX)}$				16	V
Resistance between V_{CC} and ASU	R_{VCC_ASU}		600	830	1100	kΩ

6 Electrical Characteristics (Cont.)

Notes:

Note 1: These parameters are not 100% tested. They are guaranteed by design and characterization.

Note 2: Operating frequency varies based on the load conditions, see Section 9.6 for more details.

Note 3: These parameters are not 100% tested, guaranteed by design and characterization. Refer to Section 9 for operation details.

7 Typical Performance Characteristics

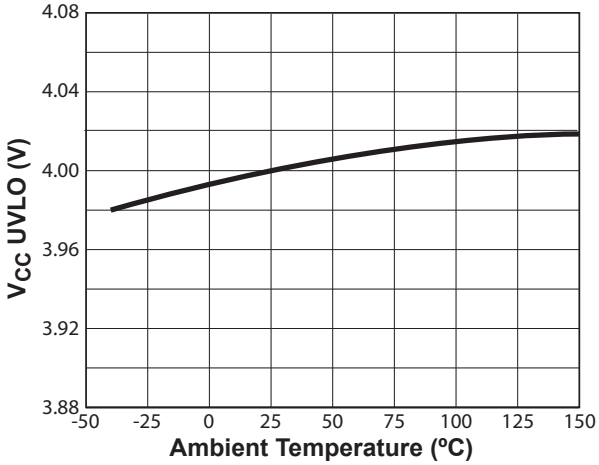


Figure 7.1 : V_{CC} UVLO vs. Temperature

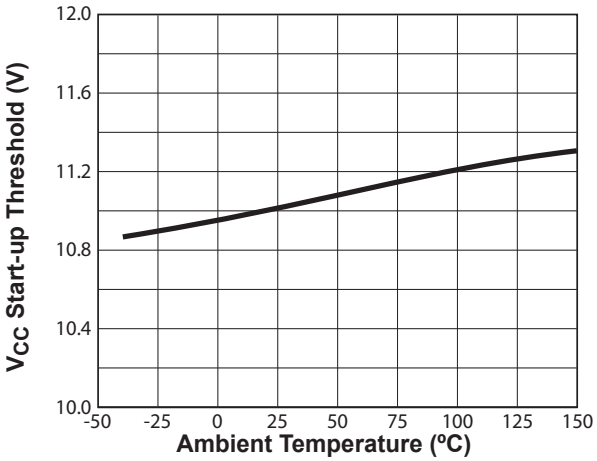


Figure 7.2 : Start-Up Threshold vs. Temperature

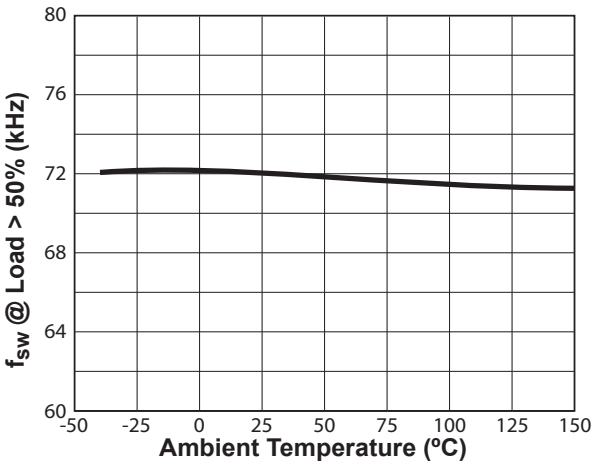


Figure 7.3 : Switching Frequency vs. Temperature[1]

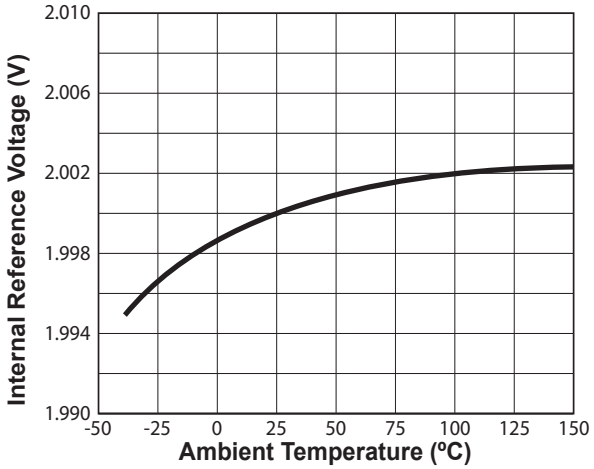


Figure 7.4 : Internal Reference vs. Temperature

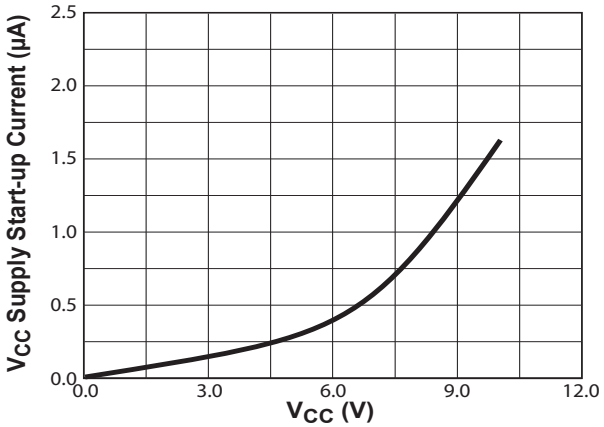


Figure 7.5 : V_{CC} vs. V_{CC} Supply Start-up Current

Note:

Note 1: Operating frequency varies based on the load conditions, see Section 9.6 for more details.

8 Functional Block Diagram

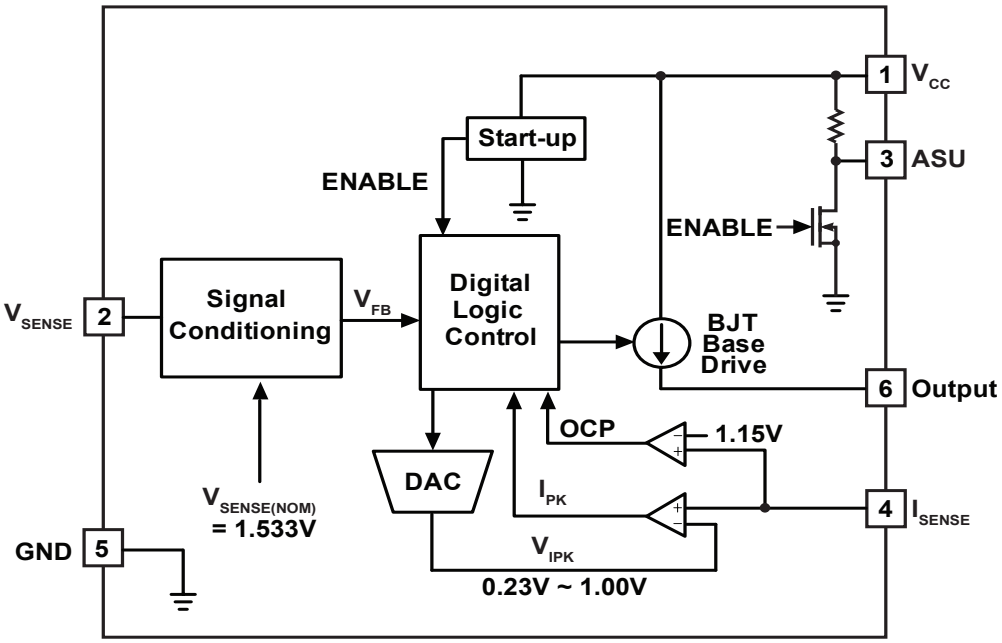


Figure 8.1 : iW1707 Functional Block Diagram

9 Theory of Operation

The iW1707 is a digital controller which uses a new, proprietary primary-side control technology to eliminate the opto-isolated feedback and secondary regulation circuits required in traditional designs. This results in a low-cost solution for low power AC/DC adapters. The core PWM processor uses fixed-frequency Discontinuous Conduction Mode (DCM) operation at higher power levels and switches to variable frequency operation at light loads to maximize efficiency. Furthermore, Dialog's digital control technology enables fast dynamic response, tight output regulation, and full featured circuit protection with primary-side control.

Referring to the block diagram in Figure 8.1, the iW1707 operates in peak current mode control. The digital logic control block generates the switching on-time and off-time information based on the output voltage and current feedback signal and provides commands to dynamically control the external BJT base current. The I_{SENSE} is an analog input configured to sense the primary current in a voltage form. In order to achieve the peak current mode control and cycle-by-cycle current limit, the V_{IPK} sets the threshold for the I_{SENSE} to compare with, and it varies in the range of 0.23V (typical) and 1V (typical) under different line and load conditions. The system loop is automatically compensated internally by a digital error amplifier. Adequate system phase margin and gain margin are guaranteed by design and no external analog components are required for loop compensation. The iW1707 uses an advanced digital control algorithm to reduce system design time and increase reliability.

Furthermore, accurate secondary constant-current operation is achieved without the need for any secondary-side sense and control circuits.

The iW1707 uses adaptive multi-mode PWM/PFM control to dynamically change the BJT switching frequency for efficiency, EMI, and power consumption optimization. In addition, it achieves unique BJT quasi-resonant switching to further improve efficiency and reduce EMI. Built-in single-point fault protection features include overvoltage protection (OVP), output short circuit protection (SCP), over current protection (OCP), and I_{SENSE} fault detection. In particular, it ensures that power supplies built with the iW1707 are best suited for power adapter applications such as ADSL modems that have large input capacitance.

Dialog's digital control scheme is specifically designed to address the challenges and trade-offs of power conversion design. This innovative technology is ideal for balancing new regulatory requirements for green mode operation with more practical design considerations such as lowest possible cost, smallest size and high performance output control.

9.1 Pin Detail

Pin 1 – V_{CC}

Power supply for the controller during normal operation. The controller will start up when V_{CC} reaches 11.0V (typical) and will shut-down when the V_{CC} voltage is 4.0V (typical). A decoupling capacitor of 0.1µF or so should be connected between the V_{CC} pin and GND.

Pin 2 – V_{SENSE}

Sense signal input from auxiliary winding. This provides the secondary voltage feedback used for output regulation.

Pin 3 – ASU

Control signal for active startup device. This signal is pulled low after start-up is finished to cut off the active device. This pin can be left unconnected if an active start-up device is not needed in the application circuit.

Pin 4 – I_{SENSE}

Primary current sense. Used for cycle-by-cycle peak current control and limit.

Pin 5 – GND

Ground.

Pin 6 – OUTPUT

Base drive for the external power BJT switch.

9.2 Active Start-up and Adaptively Controlled Soft Start

The iW1707 features an innovative proprietary soft-start scheme to achieve fast yet smooth build-up of output voltage with a wide range of output loads, including capacitive loads typically from 330µF to 6,000µF, and for output voltage covering typically from 5V to 12V. In addition, the active start-up schemes enable shortest possible turn-on delay without sacrificing no-load power loss.

Refer to Figure 3.1 and Figure 3.2 for active start-up circuits using external depletion NFET and BJT respectively. Prior to start-up, the ENABLE signal is low, and the ASU pin voltage closely follows the V_{CC} pin voltage, as shown in Figure 9.1. Consequently, the depletion NFET or the BJT is turned on, allowing the start-up current to charge the V_{CC} bypass capacitor. When the V_{CC} bypass capacitor is charged to a voltage higher than the start-up threshold $V_{CC(ST)}$, the ENABLE signal becomes high and the iW1707 commences the soft start function. During the soft-start process, the primary-side peak current is limited cycle-by-cycle by the I_{PEAK} comparator. The whole soft-start process can break down into several stages based on the output voltage levels, which is indirectly sensed by V_{SENSE} signal at the primary side. At different stages, the iW1707 adaptively controls the switching frequency and primary-side peak current such that the output voltage can always build up very fast at the early stages and smoothly transition to the desired regulation voltage at the final stage, regardless of any capacitive and resistive loads that the applications may incur. With a lowest system cost, this adaptively controlled soft start feature makes the iW1707 ideal in network power adapter applications such as ADSL modems where the adapter needs to drive large capacitive loads with 12V output voltage.

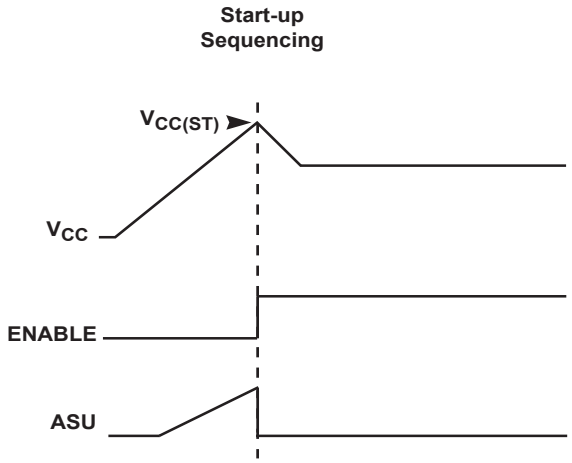


Figure 9.1 : Start-up Sequencing Diagram

While the ENABLE signal initiates the soft-start process, it also pulls down the ASU pin voltage at the same time, which turns off the depletion NFET or the BJT, thus minimizing the no-load standby power consumption. For the active startup scheme in Figure 3.2, the start-up resistors connected between the base of the BJT and DC input still conduct current after start-up is finished. Their resistance needs to be large enough to minimize no-load power consumption; meanwhile the BJT with ample gain should be selected in order to obtain a sufficient charge current for a fast start-up.

If at any time the V_{CC} voltage drops below under voltage lockout (UVLO) threshold $V_{CC(UVL)}$ then the iW1707 goes to shutdown. At this time ENABLE signal becomes low, the depletion NFET or BJT turns on, and the V_{CC} capacitor begins to charge up again towards the start-up threshold to initiate a new soft-start process.

In applications where the active start-up is not needed, the start-up resistor can be directly connected to the V_{CC} pin without using the active start-up device, and the ASU pin can be left unconnected. Refer to Figure 3.3 for the application circuit.

9.3 Understanding Primary Feedback

Figure 9.2 illustrates a simplified flyback converter. When the switch Q1 conducts during $t_{ON}(t)$, the current $i_g(t)$ is directly drawn from rectified sinusoid $v_g(t)$. The energy $E_g(t)$ is stored in the magnetizing inductance L_M. The rectifying diode D1 is reverse biased and the load current I_O is supplied by the secondary capacitor C_O. When Q1 turns off, D1 conducts and the stored energy $E_g(t)$ is delivered to the output.

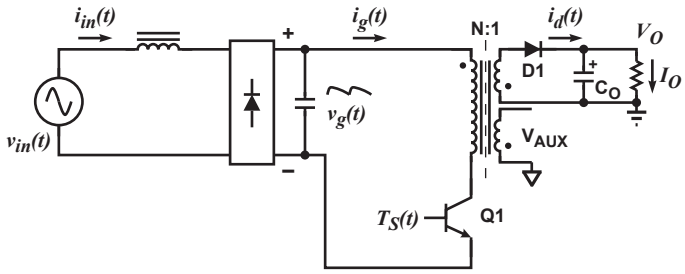


Figure 9.2 : Simplified Flyback Converter

In order to tightly regulate the output voltage, the information about the output voltage and load current need to be accurately sensed. In the DCM flyback converter, this information can be read via the auxiliary winding or the primary magnetizing inductance (L_M). During the Q1 on-time, the load current is supplied from the output filter capacitor C_O. The voltage across L_M is $v_g(t)$, assuming the voltage dropped across Q1 is zero. The current in Q1 ramps up linearly at a rate of:

$$\frac{di_g(t)}{dt} = \frac{v_g(t)}{L_M} \qquad (9.1)$$

At the end of on-time, the current has ramped up to:

$$i_{g\_peak}(t) = \frac{v_g(t) \times t_{ON}}{L_M} \qquad (9.2)$$

This current represents a stored energy of:

$$E_g = \frac{L_M}{2} \times i_{g\_peak}(t)^2 \qquad (9.3)$$

When Q1, turns off at t_O, $i_g(t)$ in L_M forces a reversal of polarities on all windings. Ignoring the communication-time caused by the leakage inductance L_K at the instant of turn-off t_O, the primary current transfers to the secondary at a peak amplitude of:

$$i_d(t) = \frac{N_P}{N_S} \times i_{g\_peak}(t) \qquad (9.4)$$

Assuming the secondary winding is master, and the auxiliary winding is slave,

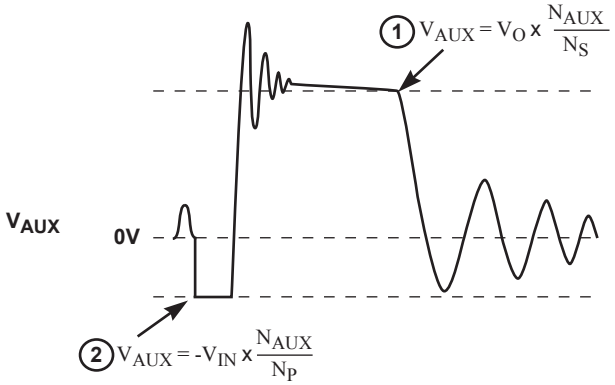


Figure 9.3 : Auxiliary Voltage Waveforms

The auxiliary voltage is given by:

$$V_{AUX} = \frac{N_{AUX}}{N_S}(V_O + \Delta V) \qquad (9.5)$$

and reflects the output voltage as shown in Figure 9.3.

The voltage at the load differs from the secondary voltage by a diode drop and IR losses. Thus, if the secondary voltage is always read at a constant secondary current, the difference between the output voltage and the secondary voltage will be a fixed ΔV. Furthermore, if the voltage can be read when the secondary current is small, ΔV will also be small. With the iW1707, ΔV can be ignored.

The real-time waveform analyzer in the iW1707 reads this information cycle-by-cycle. The part then generates a feedback voltage V_{FB}. The V_{FB} signal precisely represents the output voltage under most conditions and is used to regulate the output voltage.

9.4 Constant Voltage Operation

After soft-start has been completed, the digital control block measures the output conditions. It determines output power levels and adjusts the control system according to a light load or heavy load. If this is in the normal range, the device operates in the Constant Voltage (CV) mode, and changes the pulse width (T_{ON}) and off time (T_{OFF}) in order to meet the output voltage regulation requirements.

If no voltage is detected on V_{SENSE} it is assumed that the auxiliary winding of the transformer is either open or shorted and the iW1707 shuts down.

9.5 Current Limit and Constant Current Operation

At overload condition, the iW1707 enters constant current (CC) mode to limit the output current on cycle-by-cycle basis. During this mode of operation the output current is limited to a constant level regardless of the output voltage, while avoiding continuous conduction mode operation. In case of very heavy loading, when the output voltage is low enough, the iW1707 shuts down.

The iW1707 senses the load current indirectly through the primary current, which is detected by the pin I_{SENSE} through a resistor from the BJT emitter to ground.

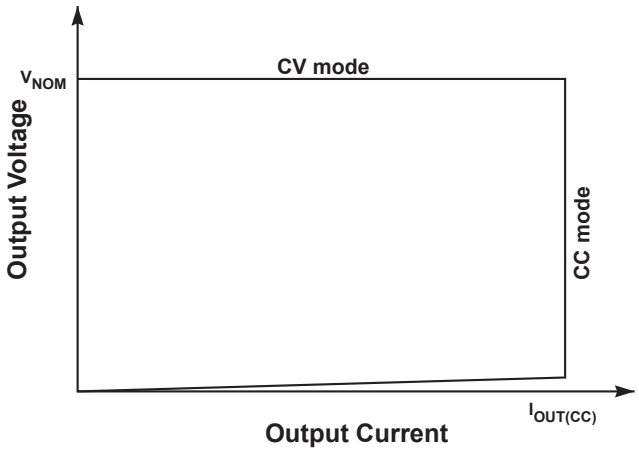


Figure 9.4 : Power Envelope

9.6 Multi-Mode PWM/PFM Control and Quasi-Resonant Switching

The iW1707 uses a proprietary adaptive multi-mode PWM/PFM control to dramatically improve the light-load efficiency and thus the overall average efficiency.

During the constant voltage (CV) operation, the iW1707 normally operates in a pulse-width-modulation (PWM) mode during heavy load conditions. In the PWM mode, the switching frequency keeps around constant. As the output load I_{OUT} is reduced, the on-time t_{ON} is decreased, and the controller adaptively transitions to a pulse-frequency-modulation (PFM) mode. During the PFM mode, the BJT is turned on for a set duration under a given instantaneous rectified AC input voltage, but its off time is modulated by the load current. With a decreasing load current, the off time increases and thus the switching frequency decreases.

When the switching frequency approaches to human ear audio band, the iW1707 transitions to a second level of PWM mode, namely Deep PWM mode (DPWM). During the DPWM mode, the switching frequency keeps around 25kHz in order to avoid audible noise. As the load current is further reduced, the iW1707 transitions to a second level of PFM mode, namely Deep PFM mode (DPFM), which can reduce the switching frequency to a very low level. Although the switching frequency drops across the audible frequency range during the DPFM mode, the current in the power converter has reduced to an insignificant level in the DPWM mode before transitioning to the DPFM mode. Therefore, the power converter practically produces no audible noise, while achieving high efficiency across varying load conditions.

The iW1707 also incorporates a unique proprietary quasi-resonant switching scheme that achieves valley-mode turn on for every PWM/PFM switching cycle, during all PFM and PWM modes, and in both CV and CC operations. This unique feature greatly reduces the switching loss and dv/dt across the entire operating range of the power supply. Due to the nature of quasi-resonant switching, the actual switching frequency can vary slightly cycle by cycle, providing the additional benefit of reducing EMI. Together these innovative digital control architecture and algorithms enable the iW1707 to achieve highest overall efficiency and lowest EMI, without causing audible noise over entire operating range.

9.7 Variable Frequency Operation Mode

At each of the switching cycles, the falling edge of V_{SENSE} will be checked. If the falling edge of V_{SENSE} is not detected, the off-time will be extended until the falling edge of V_{SENSE} is detected. The maximum allowed transformer reset time is 110µs. When the transformer reset time reaches 110µs, the iW1707 shuts off.

9.8 Internal Loop Compensation

The iW1707 incorporates an internal Digital Error Amplifier with no requirement for external loop compensation. For a typical power supply design, the loop stability is guaranteed to provide at least 45 degrees of phase margin and -20dB of gain margin.

9.9 Voltage Protection Features

The secondary maximum output DC voltage is limited by the iW1707. When the V_{SENSE} signal exceeds the output OVP threshold at point 1 indicated in Figure 9.3 the iW1707 shuts down.

The iW1707 protects against input line undervoltage by setting a maximum T_{ON} time. Since output power is proportional to the squared $V_{IN}T_{ON}$ product then for a given output power as V_{IN} decreases the T_{ON} will increase. Thus by knowing when the maximum T_{ON} time occurs the iW1707 detects that the minimum V_{IN} is reached, and shuts down. The maximum t_{ON} limit is set to 13.8µs. Also, the iW1707 monitors the voltage on the V_{CC} pin and when the voltage on this pin is below UVLO threshold the IC shuts down immediately.

When any of these faults are met the IC remains biased to discharge the V_{CC} supply. Once V_{CC} drops below UVLO threshold, the controller resets itself and then initiates a new soft-start cycle. The controller continues attempting start-up until the fault condition is removed.

9.10 PCL, OCP and SRS Protection

Peak-current limit (PCL), over-current protection (OCP) and sense-resistor short protection (SRSP) are features built-in to the iW1707. With the I_{SENSE} pin the iW1707 is able to monitor the peak primary current. This allows for cycle by cycle peak current control and limit. When the primary peak current multiplied by the I_{SENSE} resistor is greater than 1.15V over current (OCP) is detected and the IC will immediately turn off the base driver until the next cycle. The output driver will send out a switching pulse in the next cycle, and the switching pulse will continue if the OCP threshold is not reached; or, the switching pulse will turn off again if the OCP threshold is reached. If the OCP occurs for several consecutive switching cycles, the iW1707 shuts down.

If the I_{SENSE} resistor is shorted there is a potential danger of the over current condition not being detected. Thus, the IC is designed to detect this sense-resistor-short fault after startup and shut down immediately. The V_{CC} will be discharged since the IC remains biased. Once V_{CC} drops below the UVLO threshold, the controller resets itself and then initiates a new soft-start cycle. The controller continues attempting to startup, but does not fully startup until the fault condition is removed.

9.11 Dynamic Base Current Control

One important feature of the iW1707 is that it directly drives a BJT switching device with dynamic base current control to optimize performance. The BJT base current ranges from 13mA to 40mA, and is dynamically controlled according to the power supply load change. The higher the output power, the higher the base current. Specifically, the base current is related to V_{IPK}, as shown in Figure 9.5.

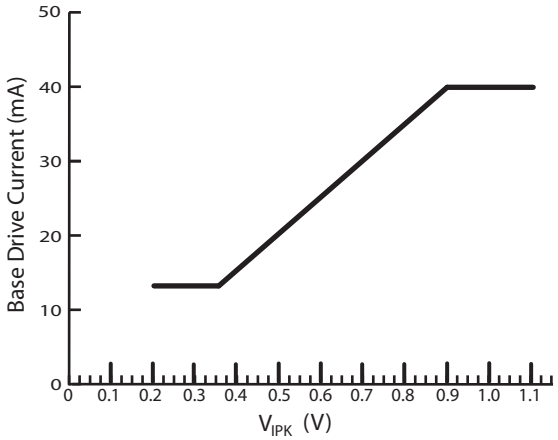


Figure 9.5 : Base Drive Current vs. V_{IPK}

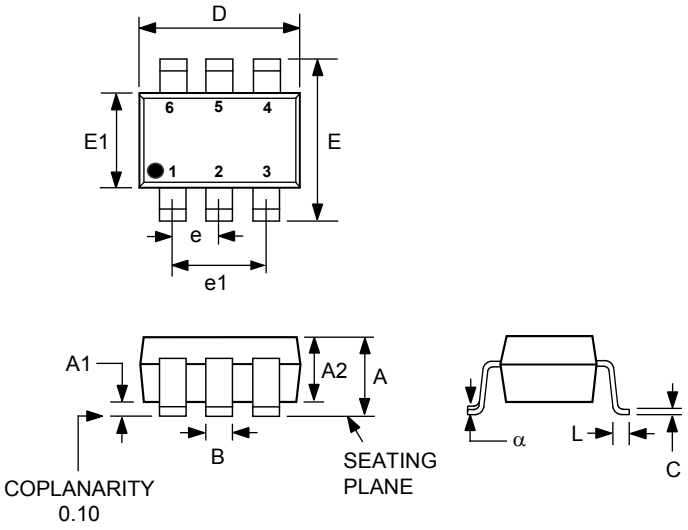
9.12 Cable Drop Compensation

The iW1707 incorporates an innovative method to compensate for any IR drop in the secondary circuitry including cable and cable connector. A 6W adapter with 12V DC output has 1.26% deviation at 0.5A load current due to the drop across a 24 AWG, 1.8 meter DC cable without cable compensation. The iW1707 compensates for this voltage drop by providing a voltage offset to the feedback signal based on the amount of load current detected.

The “Cable Comp” specified in the Table in Section 10 refers to the voltage increment at PCB end from no-load to full-load conditions in the CV mode, with the assumption that the secondary diode voltage drop can be ignored at the point when the secondary voltage is sensed. Also, the “Cable Comp” is specified based on the nominal output voltage of 5V. For different output voltage, the actual voltage increment needs to be scaled accordingly.

To calculate the amount of cable compensation needed, take the resistance of the cable and connector and multiply by the maximum output current.

6-Lead SOT Package



Symbol	Millimeters	
	MIN	MAX
A	-	1.45
A1	0.00	0.15
A2	0.90	1.30
B	0.30	0.50
C	0.08	0.22
D	2.90 BSC	
E	2.80 BSC	
E1	1.60 BSC	
e	0.95 BSC	
e1	1.90 BSC	
L	0.30	0.60
α	0°	8°

Compliant to JEDEC Standard MO-178AB

Controlling dimensions are in millimeters

This package is RoHS compliant and Halide free.

Soldering Temperature Resistance:
[a] Package is IPC/JEDEC Std 020D Moisture Sensitivity Level 1
[b] Package exceeds JEDEC Std No. 22-A111 for Solder Immersion Resistance; packages can withstand 10 s immersion < 260ºC

Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.25 mm per side.

The package top may be smaller than the package bottom. Dimensions D and E1 are are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs and interlead flash, but including any mismatch between top and bottom of the plastic body.

Figure 9.6 : Physical dimensions, 6-lead SOT-23 package

10 Ordering Information

Part Number	Options	Package	Description
iW1707-00	Cable Comp = 0mV	SOT-23	Tape & Reel[1]
iW1707-01	Cable Comp = 75mV	SOT-23	Tape & Reel[1]
iW1707-03	Cable Comp = 225mV	SOT-23	Tape & Reel[1]

Note 1: Tape & Reel packing quantity is 3,000/reel. Minimum ordering quantity is 3,000.

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