ISL98608IIH

High Efficiency Single Inductor Positive/Negative Power Supply

FN8724
Rev.2.01
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The ISL98608IIH is a high efficiency power supply for small size displays, such as smart phones and tablets requiring ±supply rails. It integrates a boost regulator, LDO, and inverting charge pump that are used to generate two output rails: +5V (default) and -6 (default). The ±5V output voltages can be adjusted from ±4.5V up to ±7V with 50mV steps using the I^2C interface.

The device integrates synchronous rectification MOSFETs for the boost regulator and inverting charge pump, which maximizes conversion efficiency.

The ISL98608IIH integrates all compensation and feedback components, which minimizes BOM count and reduces the solution PCB size to $18mm^2$.

The input voltage range, high efficiency operation and very low shutdown current make the device ideal for use in single cell Li-ion battery operated applications.

The ISL98608IIH is offered in a 1.744mm x 1.744mm WLCSP package, and the device is specified for operation across the -40°C to +85°C ambient temperature range.

Features

- Two outputs:
  - VP = +5V (default)
  - VN = -5V (default)
- 2.5V to 5.5V input voltage range
- ±4.5 to ±7V wide output range
- >89% efficiency with 12mA load between VP and VN
- $18mm^2$ solution PCB area
- Fully integrated FETs for synchronous rectification
- Integrated compensation and feedback circuits
- I^2C adjustable output voltages and settings
- Integrated VP/VN discharge resistors
- 1µA shutdown supply current
- Programmable turn-on and turn-off sequencing
- 1.744mm x 1.744mm, 4x4 array WLCSP with 0.4mm pitch

Applications

- TFT-LCD smart phone displays
- Small size/handheld displays
- Hi-Fi audio amplifier supply

Typical Application Circuits

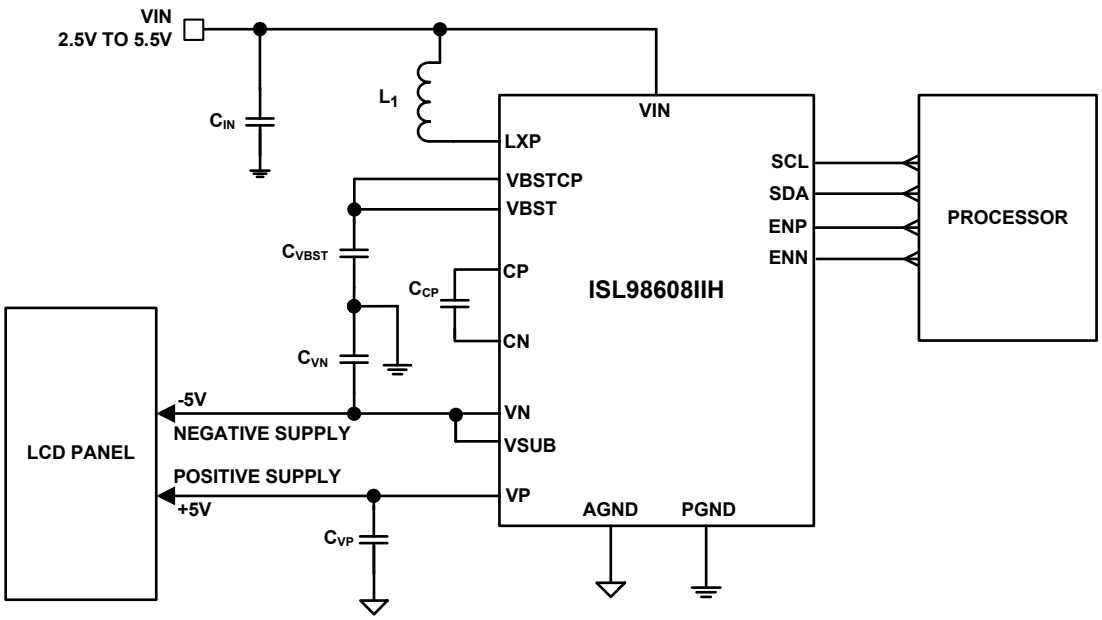

FIGURE 1. TYPICAL APPLICATION CIRCUIT: TFT-LCD SMART PHONE DISPLAY

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Typical Application Circuits (Continued)

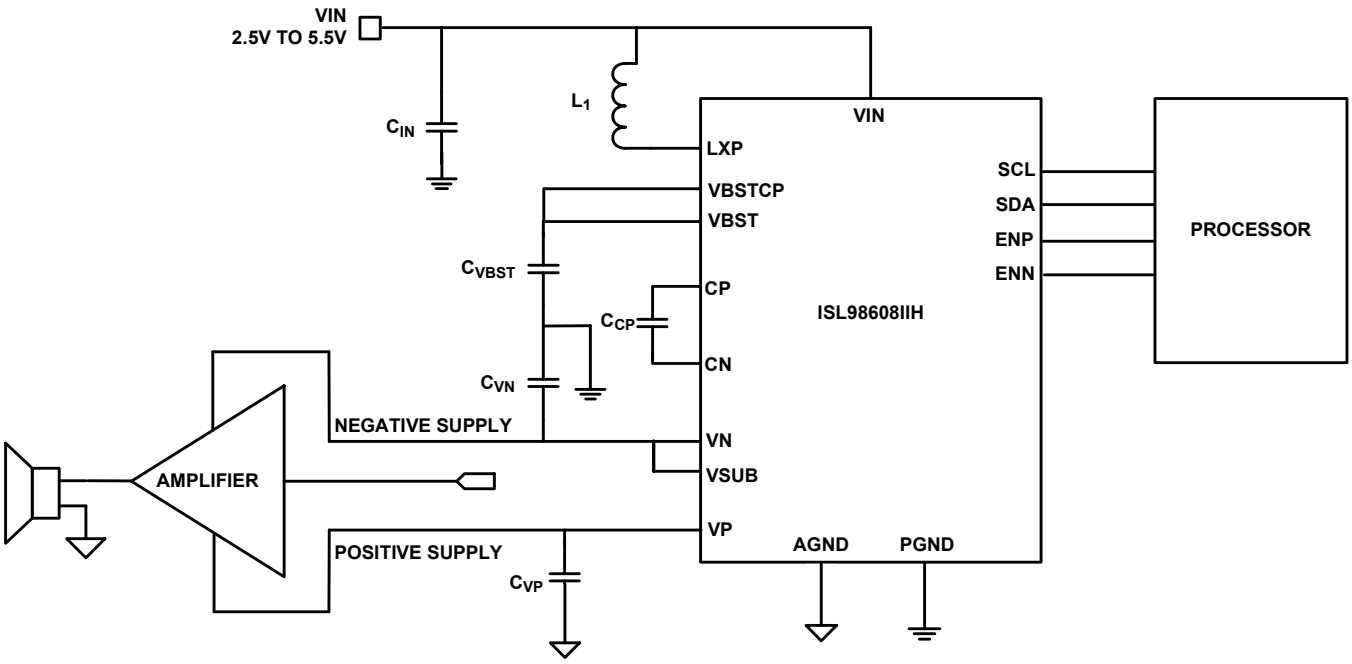

FIGURE 2. TYPICAL APPLICATION CIRCUIT: HI-FI AUDIO AMPLIFIER POWER SUPPLY

Block Diagram

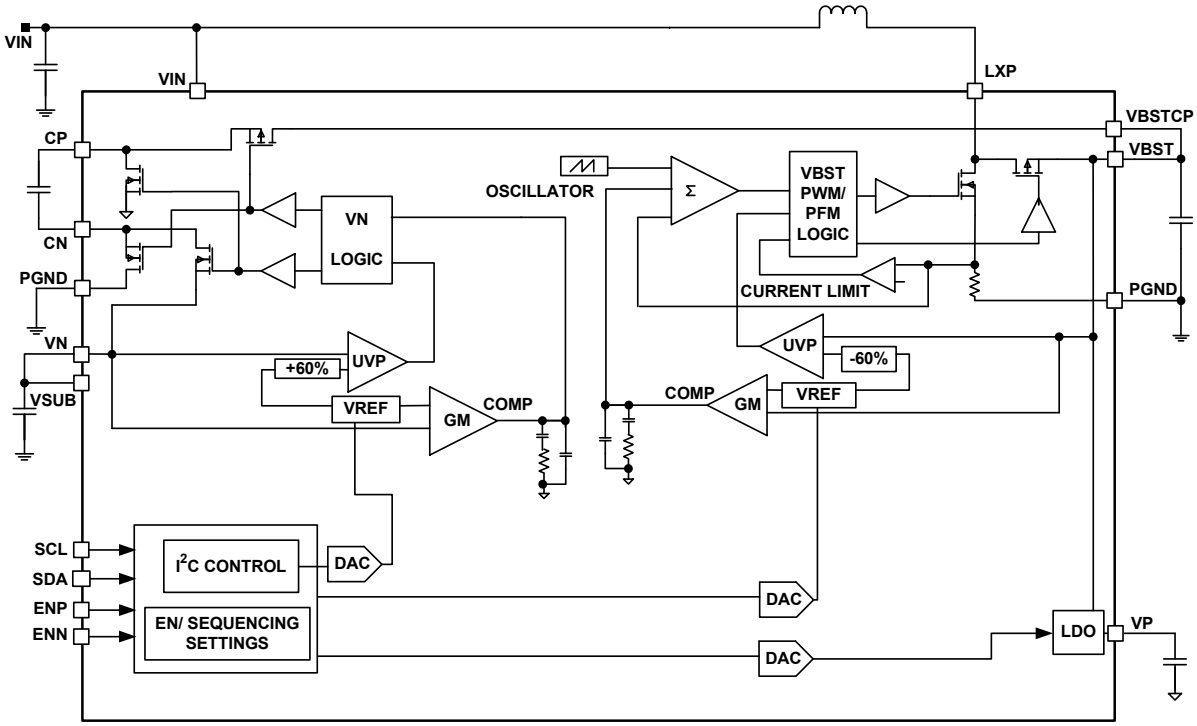

FIGURE 3. BLOCK DIAGRAM

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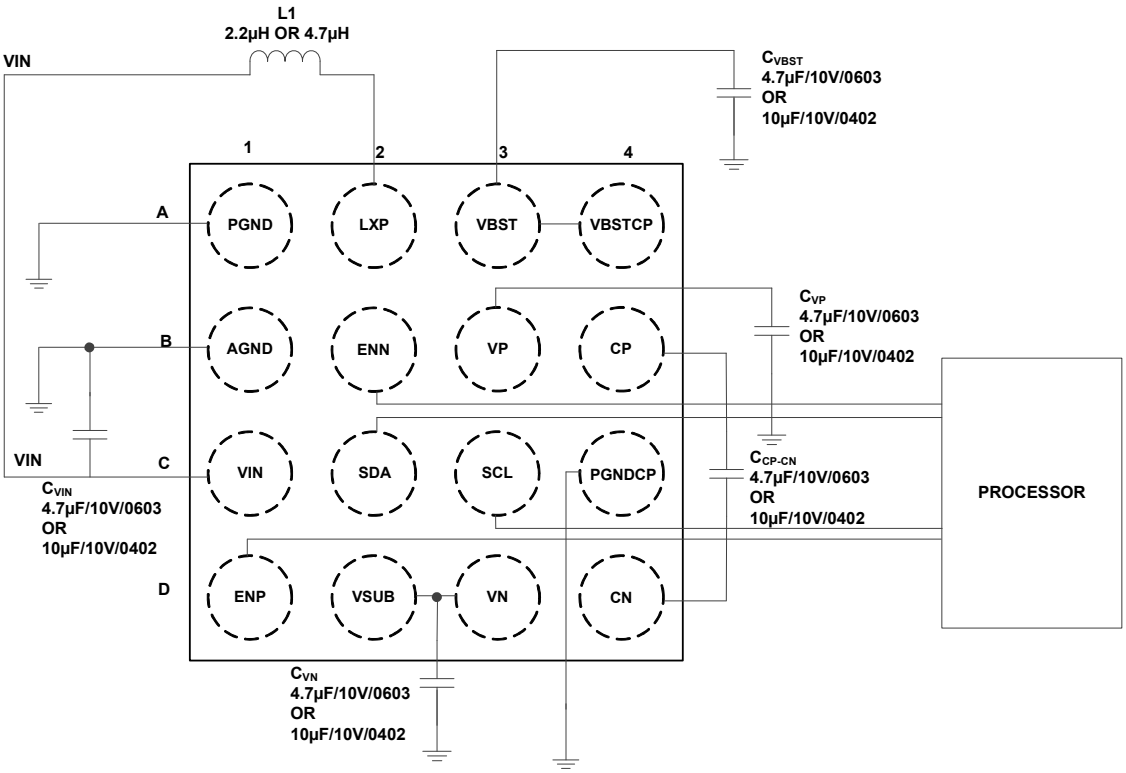
Application Circuit Diagram



Ordering Information

PART NUMBER (Notes 2, 3)	PART MARKING	PACKAGE DESCRIPTION (RoHS Compliant)	PKG. DWG. #	CARRIER TYPE (Note 1)	TEMP RANGE
ISL98608IIHZ-T	608H	16 Ball (4x4 bump, 0.4mm pitch) WLCSP	W4x4.16G	Reel, 3k	-40 to +85°C
ISL98608HEVAL1Z	Evaluation Board				

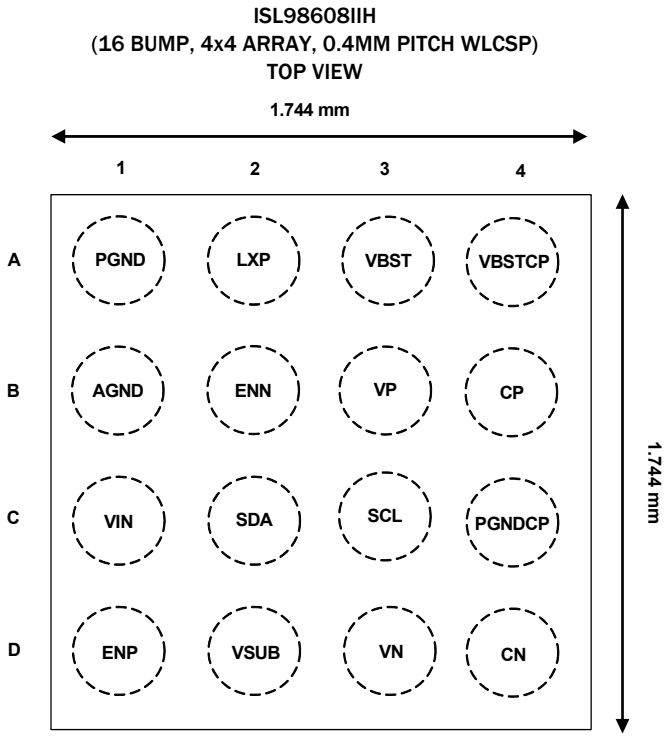
NOTES:

1. See TB347 for details on reel specifications.
2. These Pb-free WLCSP packaged products employ special Pb-free material sets; molding compounds/die attach materials and SnAgCu - e1 solder ball terminals, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free WLCSP packaged products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see the ISL98608IIH product information. For more information on MSL, see TB363.

TABLE 1. KEY DIFFERENCES BETWEEN FAMILY OF PARTS

PART NUMBER	VIN (V)	MAXIMUM OUTPUT CURRENT (mA)	VBST VOLTAGE (V)	VP VOLTAGE (V)	VN VOLTAGE (V)
ISL98608	2.5 to 5	100	5.65	5.5	-5.5
ISL98608IIH	2.5 to 5.5	200	5.4	5	-5

Pin Configuration



Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
A1	PGND	Power ground for the boost converter.
A2	LXP	Switch node for boost converter. Connect an inductor between the VIN and LXP pins for boost converter operation.
A3	VBST	Boost Converter Output. The boost converter output supplies the power to the negative charge pump and LDO. Connect a 4.7µF/0603 or 10µF/0402 capacitor to ground.
A4	VBSTCP	Charge pump input. This pin must be connected to VBST on the PCB, so that the boost regulator provides the input voltage supply for the charge pump.
B1	AGND	Analog Ground
B2	ENN	VBST and VN enable input. (Note 4)
B3	VP	Positive regulator output. Connect a 4.7µF/0603 or 10µF/0402 capacitor to ground.
B4	CP	Charge pump flying capacitor positive connection. Place a capacitor between CP and CN.
C1	VIN	Input supply voltage. Connect a 4.7µF/0603 or 10µF/0402 bypass capacitor from VIN to ground.
C2	SDA	Serial data connection for I^2C Interface. If this pin not used, connect this pin to VIN.
C3	SCL	Serial data connection for I^2C Interface. If this pin not used, connect this pin to VIN.
C4	PGNDCP	Power ground for the VN regulator.
D1	ENP	VBST and VP enable input. (Note 4)
D2	VSUB	Substrate connection. VSUB must be the most negative potential on the IC, connect VSUB to VN.
D3	VN	Negative charge pump output. Connect a 4.7µF/0603 or 10µF/0402 capacitor to ground. Connecting either two 4.7µF/0603 or 10µF/0402 capacitors to ground will lower the negative charge pump output voltage ripple.
D4	CN	Charge pump flying capacitor negative connection. Place a capacitor between CP and CN.

NOTE:

4. This pin has 1MΩ (typical) pull-down to AGND.

Absolute Maximum Ratings

VBST, VBSTCP, CP, VP to AGND . . . . . -0.3V to 8.5V
VN to AGND . . . . . +0.3V to -8.5V
VIN, SCL, SDA, ENN, ENP to AGND . . . . . -0.3V to 6V
LXP to AGND . . . . . -0.3V to VBST + 0.3V
CN to AGND . . . . . VN - 0.3V to PGND + 0.3V
Maximum Average Current
Out of VBST Pin 1A
Into LXP Pin 1A
Into CN, CP Pin . . . . . -1A
ESD Rating
Human Body Model (Tested per JESD22-A114F) 3000V
Machine Model (Tested per JESD22-A115C) 300V
Charged Device Model (Tested per JESD22-C101F) 1000V
Latch-up (Tested per JESD78D; Class II) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JB} (°C/W)
4x4 Bump 0.4mm pitch WLCSP (Notes 5, 6)	76	18

Maximum Junction Temperature . . . . . +125°C
Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

Ambient Temperature Range . . . . . -40°C to +85°C
VIN . . . . . 2.5V to 5.5V
VP . . . . . +4.5V to +7V
VN . . . . . -4.5V to -7V
VBST . . . . . +4.65V to +7.3V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

NOTES:

5. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
6. For θ_{JB}, the board temperature is taken on the board near the edge of the package, on a copper trace at the center of one side. See TB379,

Electrical Specifications

V_{IN} = 3.7V, unless otherwise noted. Typical specifications are characterized at T_A = +25°C unless otherwise noted. **Boldface limits apply across the operating temperature range, -40°C to +85°C.**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
GENERAL						
V_{IN}	V_{IN} Supply Voltage Range		**2.5**		**5.5**	V
	V_{IN} Minimum Supply Voltage (Note 9)	At 200mA		3		V
I_{IN}	V_{IN} Supply Current	ENP = ENN = SDA = SCL = 3.7V Enabled, LXP not switching		700		µA
I_{SHUTDN}	V_{IN} Supply Current when Shutdown	ENP = ENN = SDA = SCL = 0V		1		µA
V_{UVLO}	Undervoltage Lockout Threshold	V_{IN} rising		2.32	**2.44**	V
V_{UVLO_HYS}	Undervoltage Lockout Hysteresis			216		mV
BOOST REGULATOR (VBST)						
V_{VBST}	VBST Output Voltage	Register 0x06 = 0x00, 10mA load		5.4		V
V_{VBSTA}	VBST Output Voltage Accuracy	2.5V < V_{IN} < 4.6V, Register 0x06 = 0x00	-2.5		2.5	%
V_{VBSTR}	VBST Output Voltage Programmable Range	Programmable in 50mV steps	4.65		7.3	V
I_{LIM_VBST}	Boost nFET Current Limit		**1.2**	1.45	**1.7**	A
I_{VBSTO}	VBST Output Current	2.5V < V_{IN} <5V, VBST = 5.4V, Register 0x06 = 0x00)	**350**			mA
r_{ON_VBSTL}	Low-Side Switch ON-Resistance	T_A = +25°C, I_{LOAD_VBST} = 100mA, LXP to PGND		110		mΩ
r_{ON_VBSTH}	High-Side Switch ON-Resistance	T_A = +25°C, I_{LOAD_VBST} = 100mA, LXP to VBST		145		mΩ
I_{L_LXP}	LXP Leakage Current	VLXP = 6V, ENP = ENN = 0V			**10**	µA
D_{MIN}	Boost Minimum Duty Cycle	Boost frequency = 1.45MHz		12.5		%
D_{MAX}	Boost Maximum Duty Cycle	Boost frequency = 1.45MHz		91		%
f_{SWV_VBST}	Boost Switching Frequency	Boost frequency = default	**1.3**	1.45	**1.6**	MHz
t_{SS_VBST}	Boost Soft-Start Time	C_{VBST} = 10µF (not derated), VIN > V_{UVLO}		0.59	**0.85**	ms
NEGATIVE REGULATOR (VN)						
V_{VN}	VN Output Voltage	VN = -5V, Register 0x08 = 0x00 no load		-5		V

Electrical Specifications V_{IN} = 3.7V, unless otherwise noted. Typical specifications are characterized at T_A = +25°C unless otherwise noted. **Boldface limits apply across the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
V_{VNR}	VN Output Voltage Programmable Range	Programmable in 50mV steps	-7		-4.5	V
V_{ACC_VN}	VN Output Voltage Accuracy	VN = -5V, Register 0x08 = 0x00, Register 0x06 = 0x00, -100mA < I_{LOAD_VN} < 0mA	**-2**		**2**	%
f_{SW_VN}	Charge Pump Switching Frequency	CP Frequency = default, 50% duty cycle	**1.3**	1.45	**1.6**	MHz
I_{L_CP}	Charge Pump Leakage Current	CP pin, CP = 6V, ENN = 0V			**10**	µA
R_{DCH_VN}	VN Discharge Resistance	VN = -1V		35		Ω
t_{SS_VN}	VN Soft-Start Time	C_{VN} = 10µF (not derated), VN = -5V, Register 0x08 = 0x00, Register 0x05 b_7 = 0		1.96	**2.39**	ms
POSITIVE REGULATOR (VP)						
V_{VP}	VP Output Voltage	VP = 5V, Register 0x09 = 0x00, no load		5		V
V_{VPR}	VP Output Voltage Programmable Range	Programmable in 50mV steps	4.5		7	V
V_{ACC_VP}	VP Output Voltage Accuracy	VP = 5V, Register 0x09 = 0x00, Register 0x06 = 0x00, 0mA < I_{LOAD_VP} < 100mA	**-2**		**2**	%
V_{DRP_VP}	VP Dropout Voltage	I_{LOAD_VP} = 100mA			**100**	mV
I_{L_VP}	VP Leakage Current	VP pin, VP = 0V, ENP = 0V			**2**	µA
R_{DCH_VP}	VP Discharge Resistance	VP = 1V		80		Ω
t_{SS_VP}	VP Soft-Start	C_{VP} = 10µF (not derated), VP = 5V, Register 0x05 b_7 = 0		1.23	**1.53**	ms
PROTECTION						
T_{OFF}	Thermal Shutdown Temperature	Die temperature (rising) when the device will disable/shutdown all outputs until it cools by T_{HYS}°C		150		°C
T_{HYS}	Thermal Shutdown Hysteresis	Die temperature below T_{OFF}°C when the device will re-enable the outputs after shutdown		20		°C
V_{UVP_VBST}	VBST Undervoltage Limit			70% of VBST		V
V_{UVP_VP}	VP Undervoltage Protection Threshold			60% of VP		V
V_{UVP_VN}	VN Undervoltage Protection Threshold			60% of VN		V
$V_{UVDELAY}$	Undervoltage Delay	Undervoltage delay for VBST, VN, VP		100		µs
LOGIC/DIGITAL						
V_{IL}	Logic Input Low Voltage	ENN, ENP, SCL, SDA			0.4	V
V_{IH}	Logic Input High Voltage	ENN, ENP, SCL, SDA	1.1			V
f_{CLK}	I^2C SCL Clock Frequency	(Note 8)			**400**	kHz
t_d	Debounce Time	ENN, ENP		10		µs
R_{EN}	Internal Pull-Down Resistance	ENN, ENP		1		MΩ

NOTES:

7. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
8. For more detailed information regarding I^2C timing characteristics refer to Table 2 on page 17.
9. Parameters established by bench testing and/or design. Not production tested.

Typical Performance Curves

T_A = +25°C, V_{IN} = 3.7V, L_1 = 1239AS-H-2R2M (2.5mmx2mm), C_{VBST} = 10µF/0402, C_{VP} = 10µF/0402, C_{VN} = 2 x 10µF/0402, C_{CP} = 10µF/0402 unless otherwise noted.

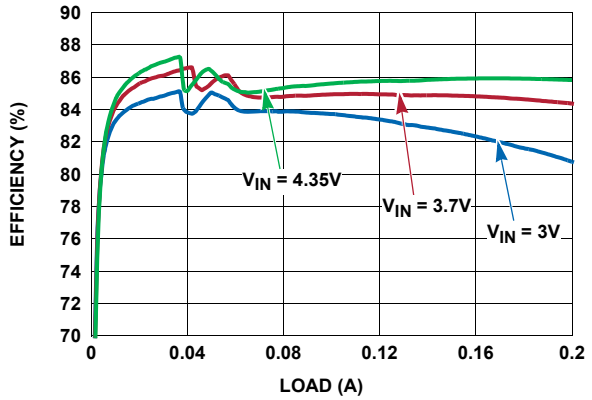


FIGURE 4. DISPLAY POWER SYSTEM EFFICIENCY, VP/VN = ±5V

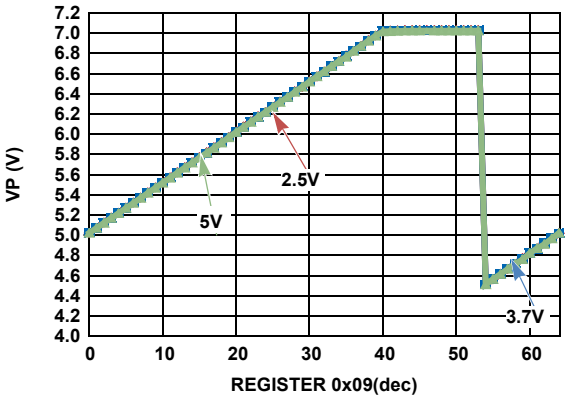


FIGURE 5. VP OUTPUT VOLTAGE RANGE

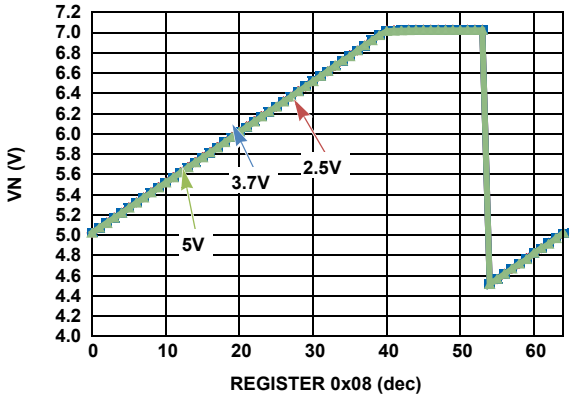


FIGURE 6. VN OUTPUT VOLTAGE RANGE

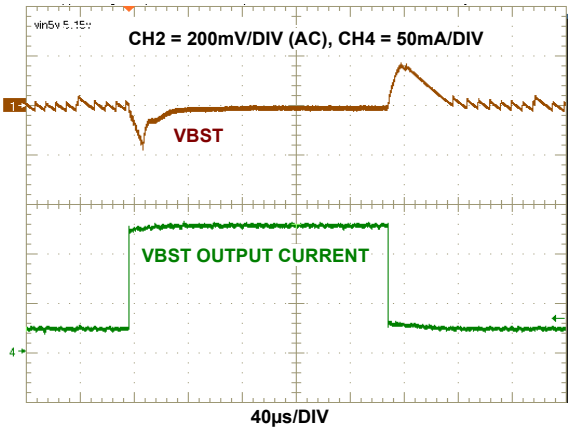


FIGURE 7. VBST LOAD TRANSIENT, VBST = 5.15V

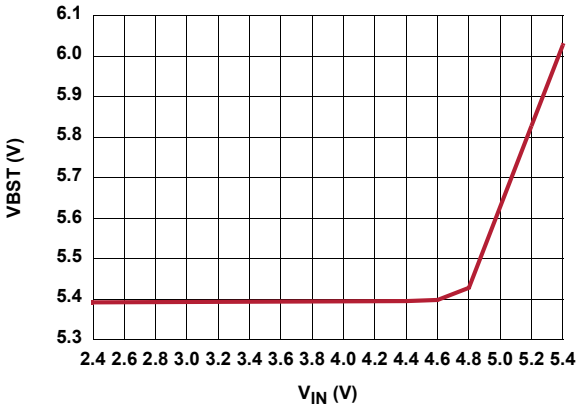


FIGURE 8. VBST, V_{IN} HEADROOM TRACKING, VBST = 5.4V

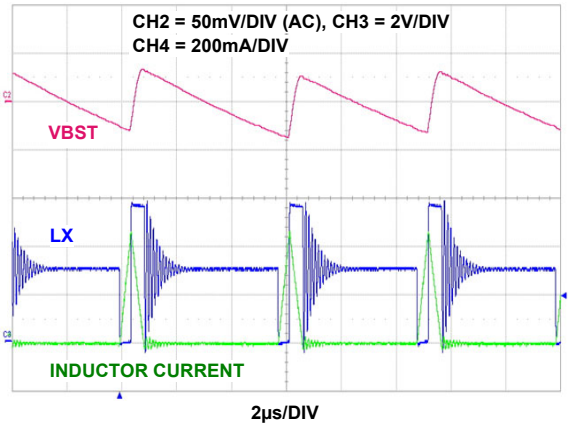


FIGURE 9. VBST RIPPLE, 10mA LOAD, VBST = 5.4, V_{IN} = 3V

Typical Performance Curves

T_A = +25°C, V_{IN} = 3.7V, L_1 = 1239AS-H-2R2M (2.5mmx2mm), C_{VBST} = 10µF/0402, C_{VP} = 10µF/0402, C_{VN} = 2 x 10µF/0402, C_{CP} = 10µF/0402 unless otherwise noted. **(Continued)**

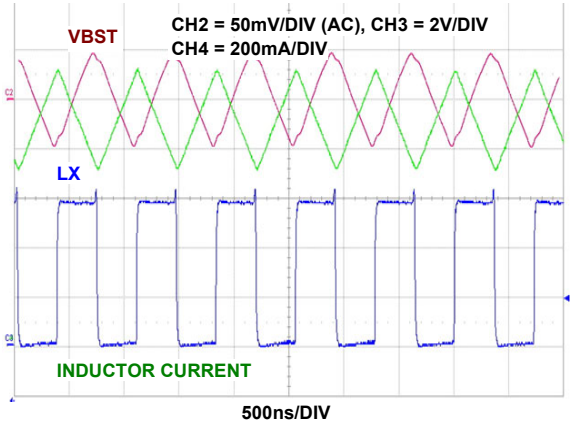


FIGURE 10. VBST RIPPLE, 450mA LOAD, VBST = 5.4V, V_{IN} = 3V

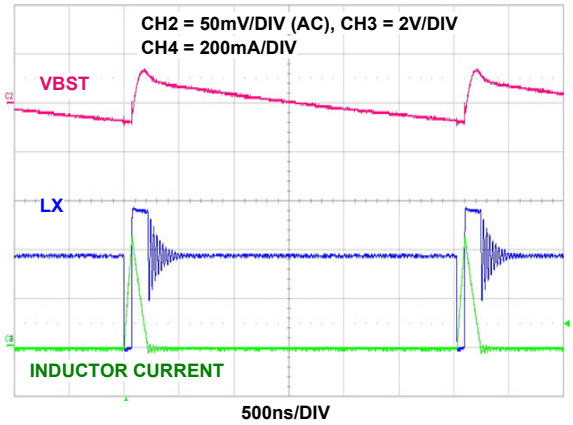


FIGURE 11. VBST RIPPLE, 10mA LOAD, VBST = 5.4V, V_{IN} = 3.7V

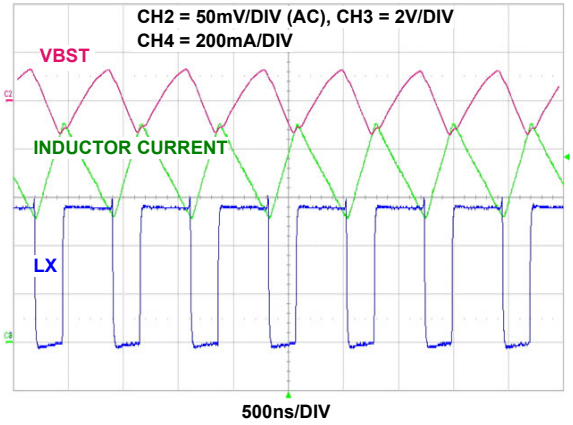


FIGURE 12. VBST RIPPLE, 10mA LOAD, VBST = 5.65V

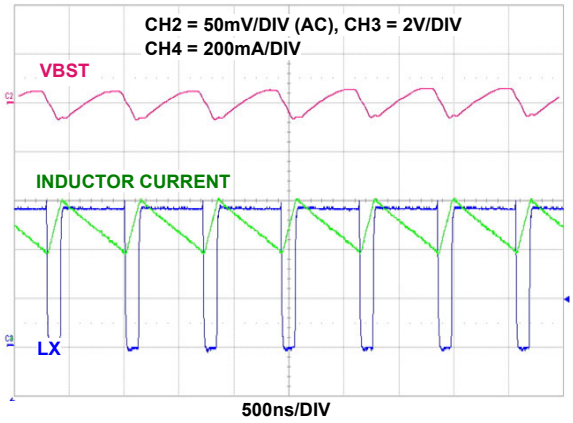


FIGURE 13. VBST RIPPLE, 150mA LOAD, VBST = 5.65V

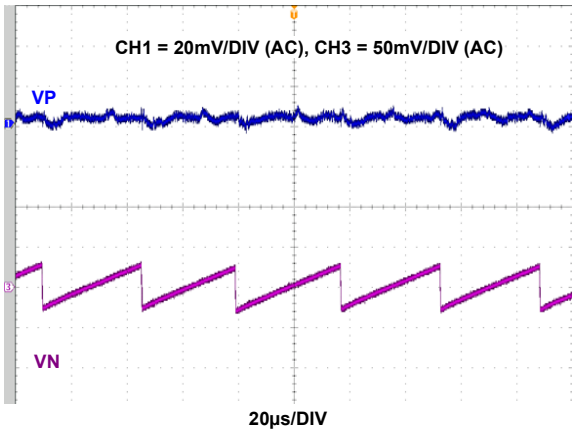


FIGURE 14. VP/VN (±5V) OUTPUT VOLTAGE RIPPLE, 5mA LOAD, V_{IN} = 3V

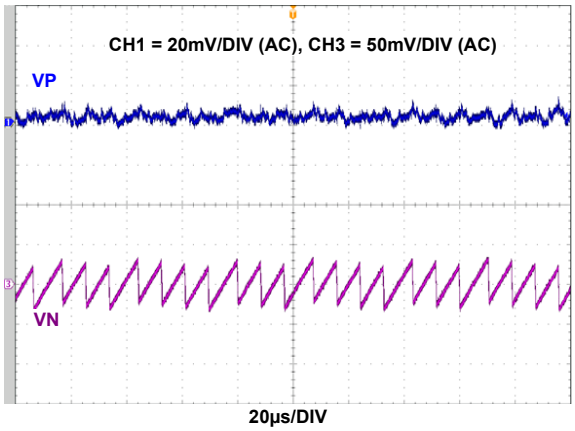


FIGURE 15. VP/VN (±5V) OUTPUT VOLTAGE RIPPLE, 20mA LOAD, V_{IN} = 3V

Typical Performance Curves

T_A = +25°C, V_{IN} = 3.7V, L_1 = 1239AS-H-2R2M (2.5mmx2mm), C_{VBST} = 10µF/0402, C_{VP} = 10µF/0402, C_{VN} = 2 x 10µF/0402, C_{CP} = 10µF/0402 unless otherwise noted. **(Continued)**

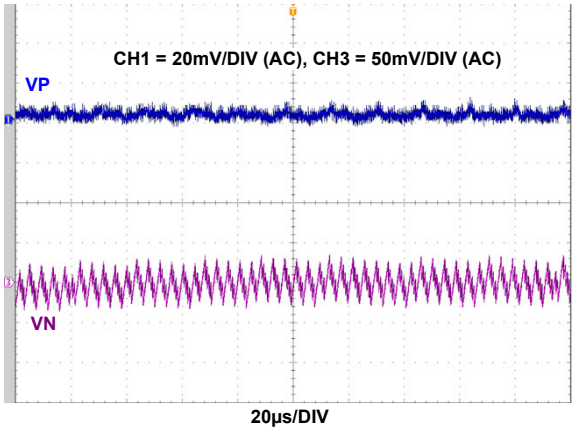


FIGURE 16. VP/VN (±5V) OUTPUT VOLTAGE RIPPLE, 100mA LOAD, V_{IN} = 3V

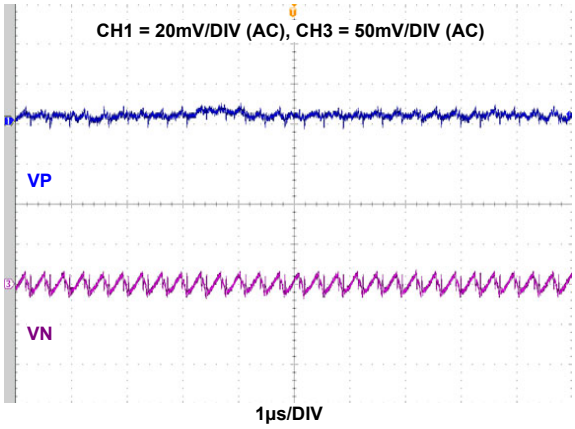


FIGURE 17. VP/VN (±5V) OUTPUT VOLTAGE RIPPLE, 200mA LOAD, V_{IN} = 3V

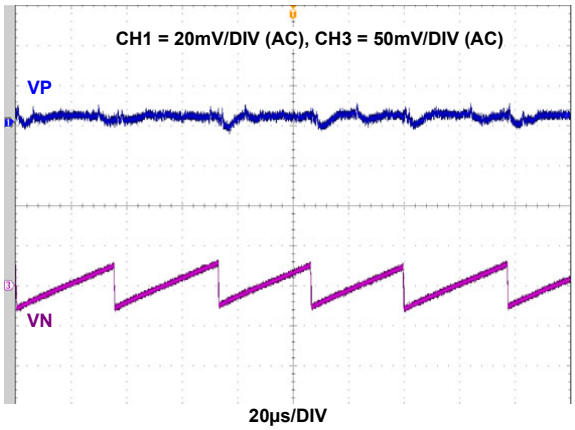


FIGURE 18. VP/VN (±5V) OUTPUT VOLTAGE RIPPLE, 5mA LOAD, V_{IN} = 3.7V

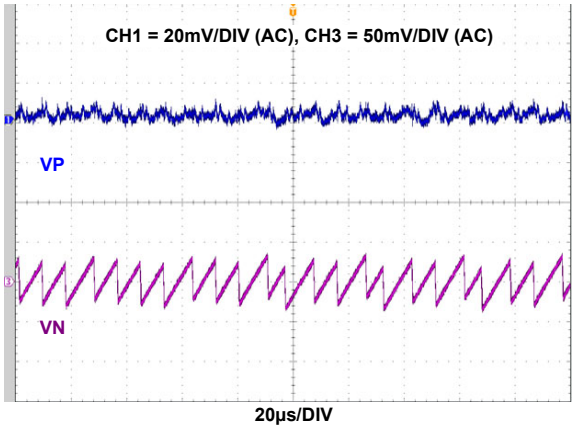


FIGURE 19. VP/VN (±5V) OUTPUT VOLTAGE RIPPLE, 20mA LOAD, V_{IN} = 3.7V

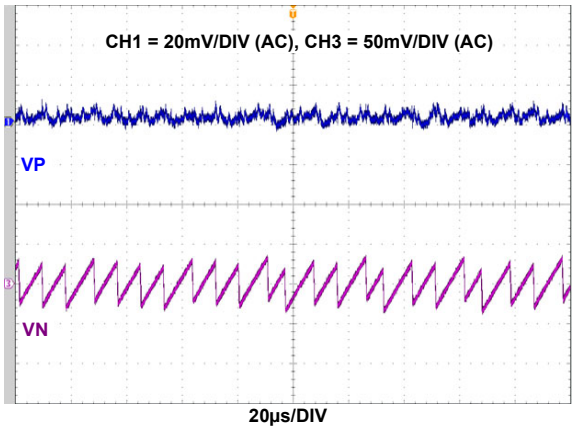


FIGURE 20. VP/VN (±5V) OUTPUT VOLTAGE RIPPLE, 100mA LOAD, V_{IN} = 3.7V

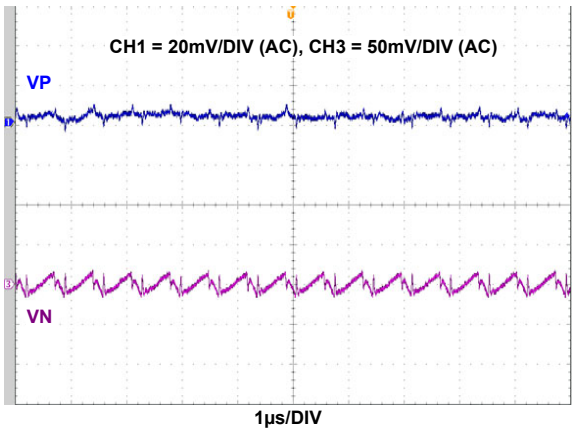


FIGURE 21. VP/VN (±5V) OUTPUT VOLTAGE RIPPLE, 200mA LOAD, V_{IN} = 3.7V

Typical Performance Curves

T_A = +25°C, V_{IN} = 3.7V, L_1 = 1239AS-H-2R2M (2.5mmx2mm), C_{VBST} = 10µF/0402, C_{VP} = 10µF/0402, C_{VN} = 2 x 10µF/0402, C_{CP} = 10µF/0402 unless otherwise noted. **(Continued)**

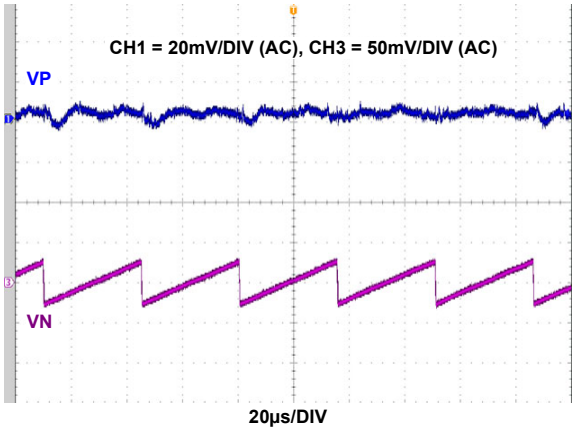


FIGURE 22. VP/VN (±5V) OUTPUT VOLTAGE RIPPLE, 5mA LOAD, V_{IN} = 4.35V

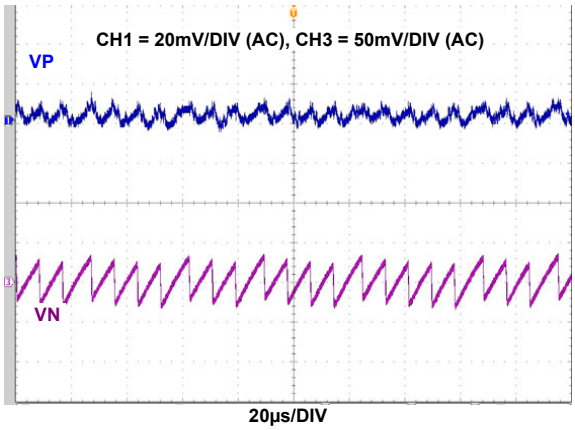


FIGURE 23. VP/VN (±5V) OUTPUT VOLTAGE RIPPLE, 20mA LOAD, V_{IN} = 4.35V

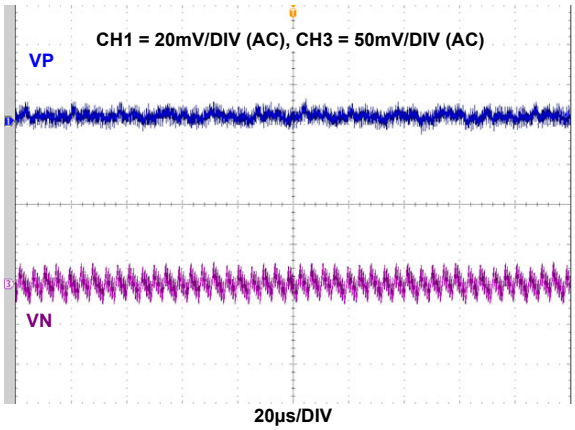


FIGURE 24. VP/VN (±5V) OUTPUT VOLTAGE RIPPLE, 100mA LOAD, V_{IN} = 4.35V

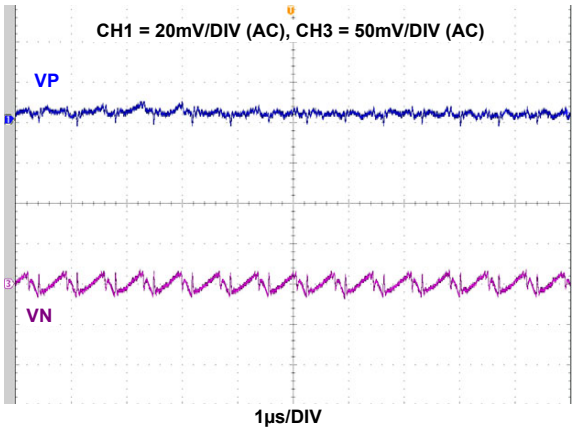


FIGURE 25. VP/VN (±5V) OUTPUT VOLTAGE RIPPLE, 200mA LOAD, V_{IN} = 4.35V

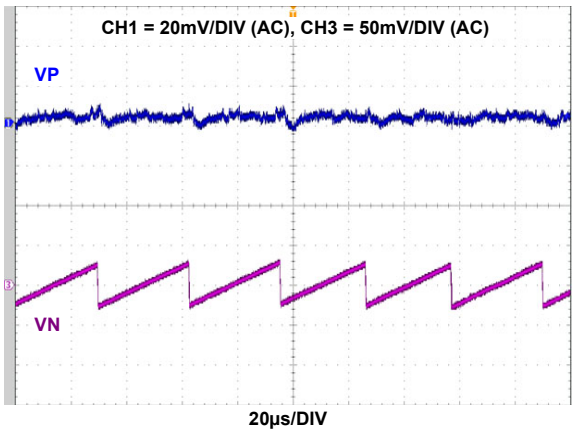


FIGURE 26. VP/VN (±5V) OUTPUT VOLTAGE RIPPLE, 5mA LOAD, V_{IN} = 5V

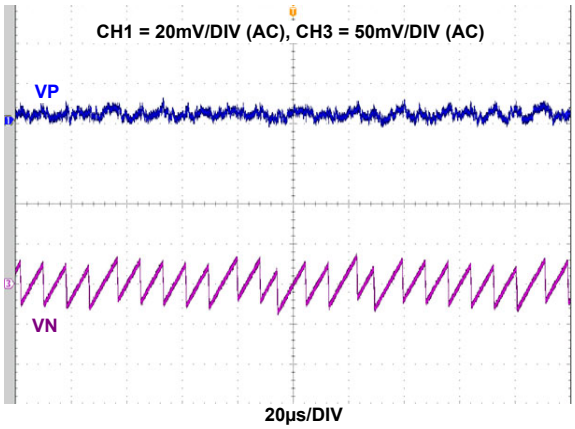


FIGURE 27. VP/VN (±5V) OUTPUT VOLTAGE RIPPLE, 20mA LOAD, V_{IN} = 5V

Typical Performance Curves

T_A = +25°C, V_{IN} = 3.7V, L_1 = 1239AS-H-2R2M (2.5mmx2mm), C_{VBST} = 10µF/0402, C_{VP} = 10µF/0402, C_{VN} = 2 x 10µF/0402, C_{CP} = 10µF/0402 unless otherwise noted. **(Continued)**

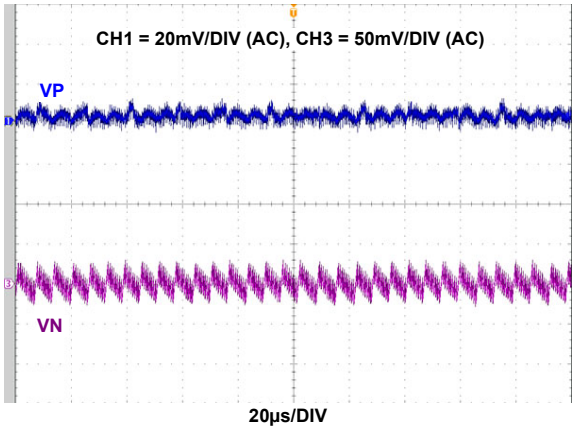


FIGURE 28. VP/VN (±5V) OUTPUT VOLTAGE RIPPLE, 100mA LOAD, V_{IN} = 5V

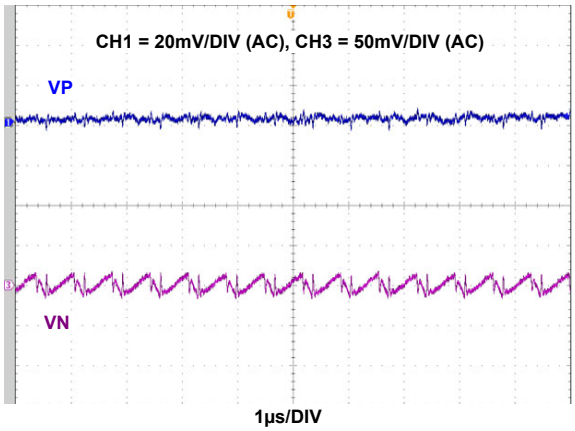


FIGURE 29. VP/VN (±7V) OUTPUT VOLTAGE RIPPLE, 100mA LOAD

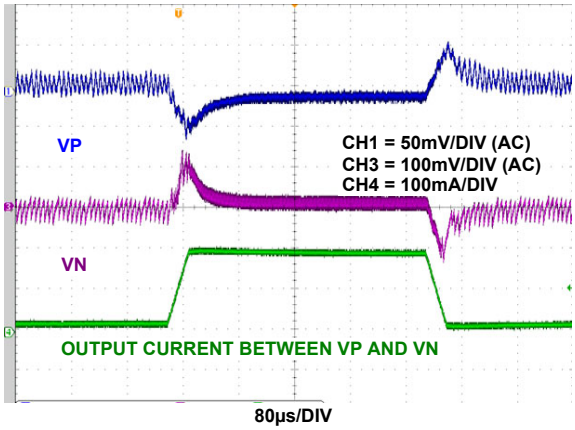


FIGURE 30. VP AND VN LOAD TRANSIENT, VP/VN = ±5V, V_{IN} = 3.7V

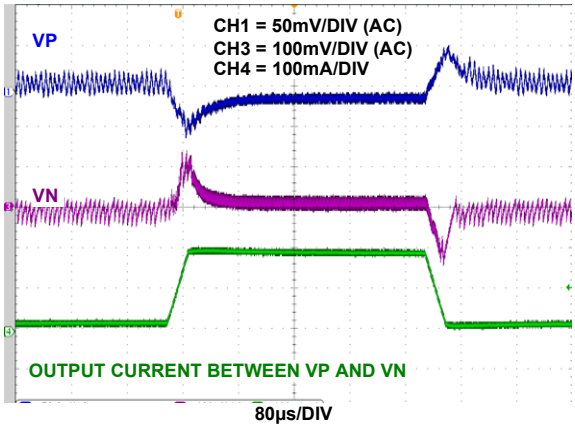


FIGURE 31. VP AND VN LOAD TRANSIENT, VP/VN = ±5V, V_{IN} = 4.35V

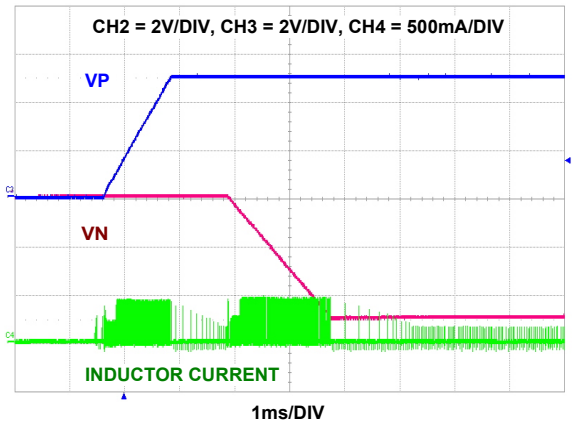


FIGURE 32. VP AND VN (±5V) SOFT-START AT 2.5V INPUT VOLTAGE, VP/VN SEQUENCED (Reg 0x04 <b_4> = 0)

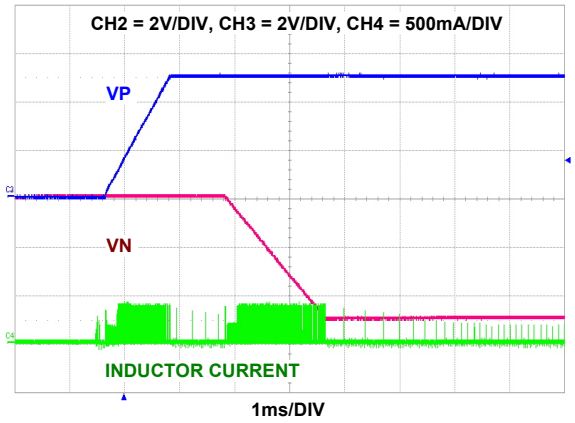


FIGURE 33. VP AND VN (±5V) SOFT-START AT 3.7V INPUT VOLTAGE, VP/VN SEQUENCED (Reg 0x04 <b_4> = 0)

Typical Performance Curves

T_A = +25°C, V_{IN} = 3.7V, L_1 = 1239AS-H-2R2M (2.5mmx2mm), C_{VBST} = 10µF/0402, C_{VP} = 10µF/0402, C_{VN} = 2 x 10µF/0402, C_{CP} = 10µF/0402 unless otherwise noted. **(Continued)**

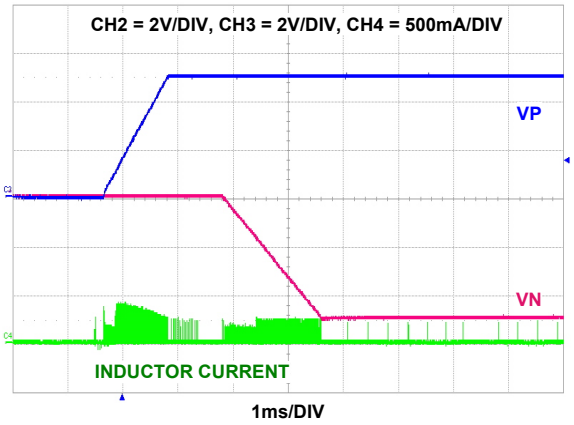


FIGURE 34. VP AND VN (±5V) SOFT-START AT 5V INPUT VOLTAGE, VP/VN SEQUENCED (Reg 0x04 <b_4> = 0)

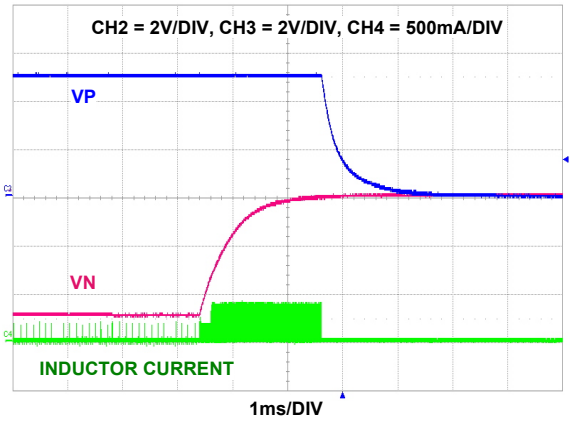


FIGURE 35. VP AND VN (±5V) SHUTDOWN, VP/VN SEQUENCED (Reg 0x05 <b_4> = 0)

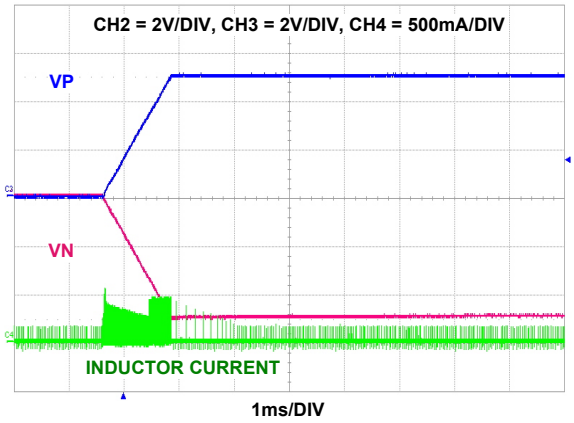


FIGURE 36. VP AND VN (±5V) SOFT-START AT 2.5V INPUT VOLTAGE, VP/VN START TOGETHER (Reg 0x04 <b_4> = 1)

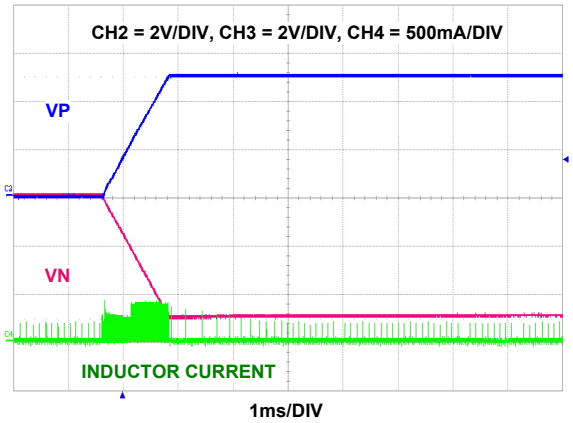


FIGURE 37. VP AND VN (±5V) SOFT-START AT 3.7V INPUT VOLTAGE, VP/VN START TOGETHER (Reg 0x04 <b_4> = 1)

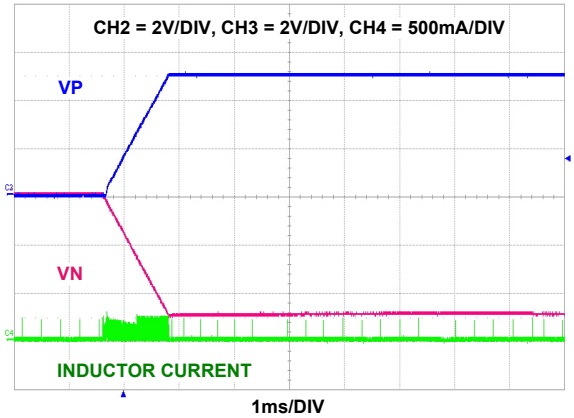


FIGURE 38. VP AND VN (±5V) SOFT-START AT 5V INPUT VOLTAGE, VP/VN START TOGETHER (Reg 0x04 <b_4> = 1)

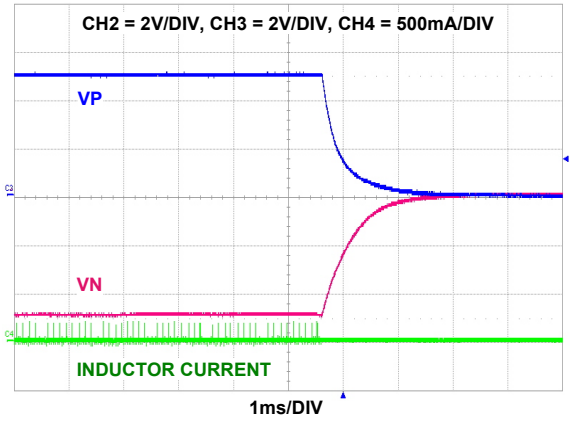


FIGURE 39. VP AND VN (±5V) SHUTDOWN, VP/VN SHUTDOWN TOGETHER (Reg 0x05 <b_4> = 1)

Typical Performance Curves

T_A = +25°C, V_{IN} = 3.7V, L_1 = 1239AS-H-2R2M (2.5mmx2mm), C_{VBST} = 10µF/0402, C_{VP} = 10µF/0402, C_{VN} = 2 x 10µF/0402, C_{CP} = 10µF/0402 unless otherwise noted. **(Continued)**

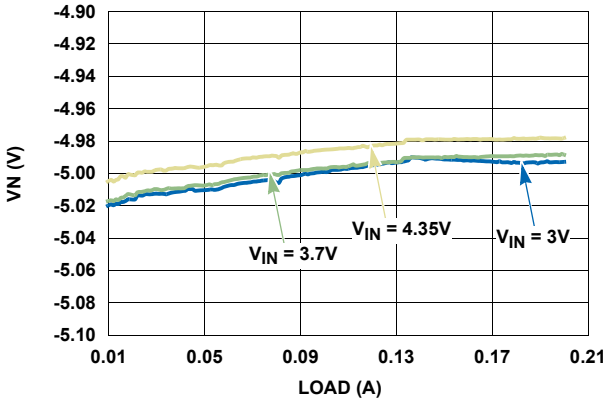


FIGURE 40. VN LOAD REGULATION, -5V

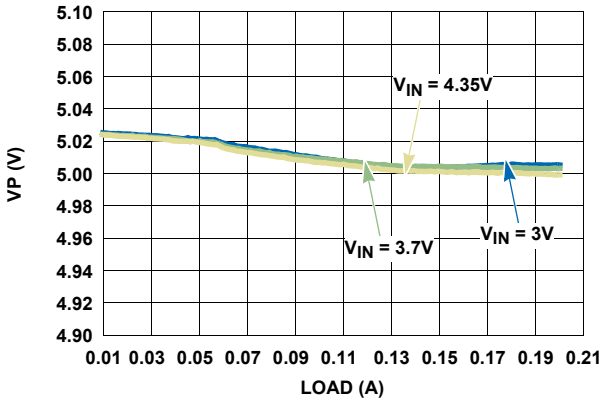


FIGURE 41. VP LOAD REGULATION, 5V

Application Information

Description

The ISL98608IIH is a display PMIC and can be used to supply power to an LCD display. Figure 42 shows the typical system application block diagram. For display power, the ISL98608IIH integrates a boost regulator (VBST), low dropout linear regulator (VP) and an inverting charge pump regulator (VN). The boost voltage is generated from a battery voltage ranging from 2.5V to 5.5V and boost regulator output can be programmed from 4.60V to 7.3V. The VBST regulator integrates low-side NFET and high-side PFET MOSFETs for synchronous rectification.

The output voltage of VBST is the input to the linear regulator (VP). The VBST output and VP regulator input are connected internally in the IC. The VP regulator supplies a positive voltage in the range of +4.5V to +7V with 50mV resolution. An 80Ω discharge resistor discharges residual voltage when the power-off sequence is initiated, which helps avoid ghost image issues. The LDO is an ideal solution for the positive supply due to its low ripple, fast load transient response, higher efficiency and low dropout voltage.

The VN voltage is generated by a regulated inverting charge pump topology. VBSTCP is the input to the inverting charge pump, which should be connected to the VBST pin on the PCB. The VN regulator supplies negative voltage from -7V to -4.5V with 50mV resolution. Similar to the VP regulator, the VN regulator also integrates a discharge resistor and the value of discharge resistor is 35Ω. The VN is an ideal solution for negative supply due to low ripple, fast load transient response and higher efficiency.

Modes of Operation

SHUTDOWN MODE

The ISL98608IIH is in shutdown mode when the enable pins, namely ENN and ENP are pulled low. When the ENN and ENP pins are all pulled low, all the regulators are powered off and the IC is placed in shutdown mode where the current consumed from the battery is only 1µA (typical).

OPERATING MODE

The IC is in normal operating mode when the ENN and ENP are pulled high and the current consumed from the battery is only 1mA (excluding VBST and VN switching current). After the ENN/ENP signals are pulled high, VBST, VP and VN go through power-on sequencing. Refer to "Power-On/Off Sequence" on page 23 for more details.

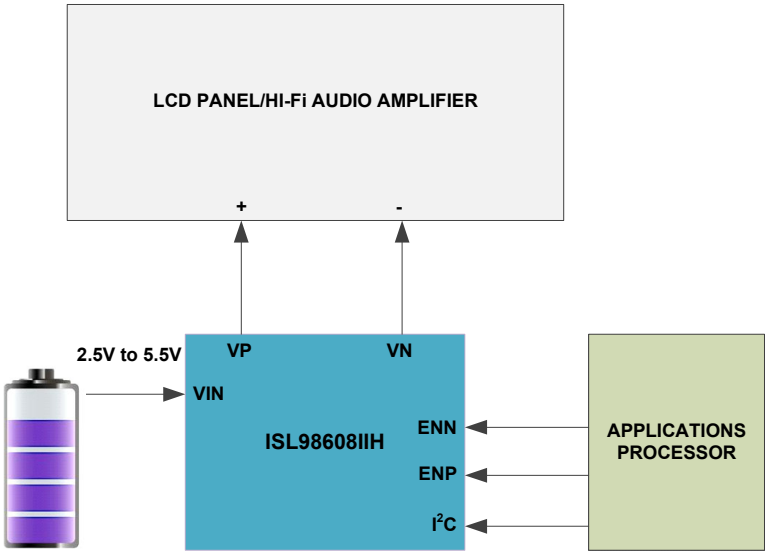
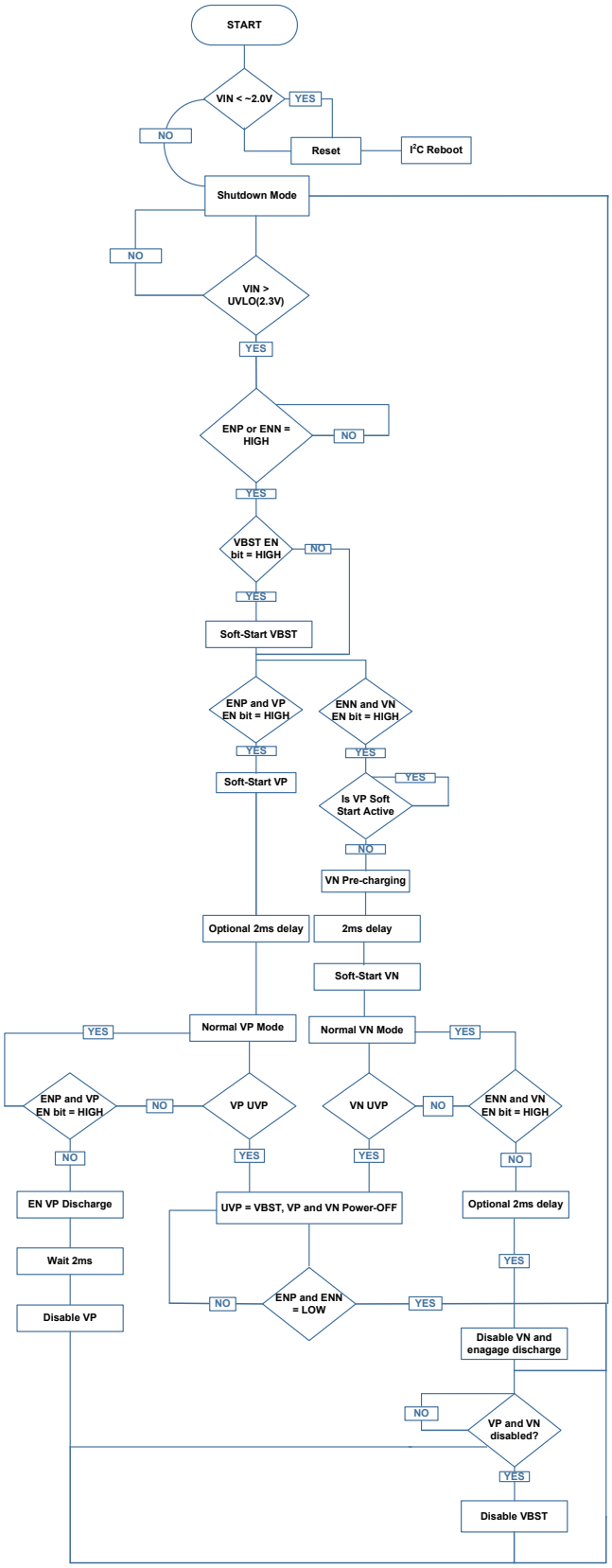


FIGURE 42. TYPICAL SYSTEM APPLICATION BLOCK DIAGRAM



Optional 2ms delay : If register 0x02 b<6> is set to "1" then 2ms delay is performed on both VP and VN.

FIGURE 43. START-UP FUNCTIONAL BLOCK DIAGRAM

I²C Digital Interface

The ISL98608IIH uses a standard I²C interface bus for communication. The two-wire interface links a Master(s) and uniquely addressable Slave devices. The Master generates clock signals and is responsible for initiating data transfers. The serial clock is on the SCL line and the serial data (bidirectional) is on the SDA line. The ISL98608IIH supports clock rates up to 400kHz (Fast mode) and is backwards compatible with standard 100kHz clock rates (Standard mode).

The SDA and SCL lines must be HIGH when the bus is free - not in use. An external pull-up resistor (typically 2.2kΩ to 4.7kΩ) or current source is required for SDA and SCL.

The ISL98608IIH meets standard I²C timing specifications, see Figure 44 and Table 2, which show the standard timing definitions and specifications for I²C communication.

START AND STOP CONDITION

All I²C communication begins with a START condition (indicating the beginning of a transaction) and ends with a STOP condition (signaling the end of the transaction).

A START condition is signified by a HIGH to LOW transition on the serial data line (SDA) while the serial clock line (SCL) is HIGH. A STOP condition is signified by a LOW to HIGH transition on the SDA line while SCL is HIGH. See timing specifications in Table 2.

The Master always initiates START and STOP conditions. After a START condition, the bus is considered "busy." After a STOP condition, the bus is considered "free." The ISL98608IIH also supports repeated STARTs, where the bus will remain busy for continued transaction(s).

DATA VALIDITY

The data on the SDA line must be stable (clearly defined as HIGH or LOW) during the HIGH period of the clock signal. The state of the SDA line can only change when the SCL line is LOW (except to create a START or STOP condition). See timing specifications in Table 2.

The voltage levels used to indicate a logical '0' (LOW) and logical '1' (HIGH) are determined by the V_{IL} and V_{IH} thresholds, respectively, see the "Electrical Specifications" table on page 7.

BYTE FORMAT

Every byte transferred on SDA must be 8 bits in length. After every byte of data sent by the transmitter there must be an Acknowledge bit (from the receiver) to signify that the previous 8 bits were transferred successfully. Data is always transferred on SDA with the Most Significant Bit (MSB) first. See "Acknowledge (ACK)" on page 18.

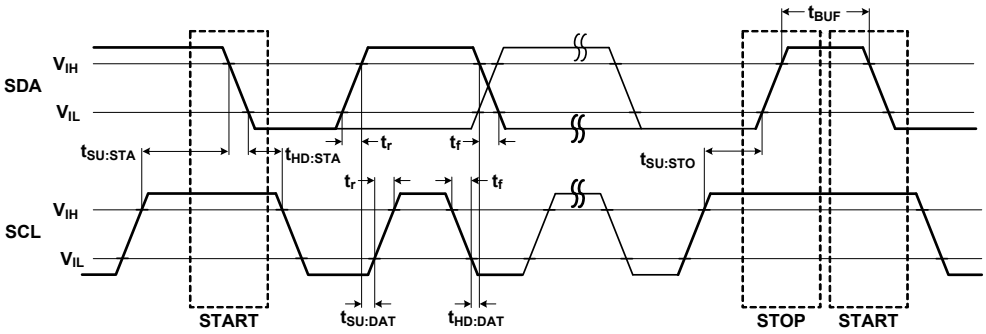


FIGURE 44. I²C TIMING DEFINITIONS

TABLE 2. I²C TIMING CHARACTERISTICS

PARAMETER	SYMBOL	FAST-MODE		STANDARD-MODE		UNIT
		MIN	MAX	MIN	MAX	
SCL Clock Frequency	f_{SCL}	0	400	0	100	kHz
Set-Up Time for a START Condition	$t_{SU:STA}$	0.6	-	4.7	-	µs
Hold Time for a START Condition	$t_{HD:STA}$	0.6	-	4.0	-	µs
Set-Up Time for a STOP Condition	$t_{SU:STO}$	0.6	-	4.0	-	µs
Bus Free Time between a STOP and START Condition	t_{BUF}	1.3	-	4.7	-	µs
Data Set-Up Time	$t_{SU:DAT}$	100	-	250	-	ns
Data Hold Time	$t_{HD:DAT}$	0	-	0	-	µs
Rise Time of SDA and SCL (Note 10)	t_r	$20 + 0.1C_b$	300	-	1000	ns
Fall Time of SDA and SCL (Note 10)	t_f	$20 + 0.1C_b$	300	-	300	ns
Capacitive Load on Each Bus Line (SDA/SCL)	C_b	-	400	-	400	pF

NOTE:

10. C_b = Total capacitance of one bus line in pF.

ACKNOWLEDGE (ACK)

Each 8-bit data transfer is followed by an Acknowledge (ACK) bit from the receiver. The Acknowledge bit signifies that the previous 8 bits of data was transferred successfully (master to slave or slave to master).

When the Master sends data to the Slave (e.g., during a WRITE transaction), after the 8th bit of a data byte is transmitted, the Master tri-states the SDA line during the 9th clock. The Slave device acknowledges that it received all 8 bits by pulling down the SDA line, generating an ACK bit.

When the Master receives data from the Slave (e.g., during a data READ transaction), after the 8th bit is transmitted, the Slave tri-states the SDA line during the 9th clock. The Master acknowledges that it received all 8 bits by pulling down the SDA line, generating an ACK bit.

NOT ACKNOWLEDGE (NACK)

A Not Acknowledge (NACK) is generated when the receiver does not pull-down the SDA line during the acknowledge clock (i.e., SDA line remains HIGH during the 9th clock). This indicates to the Master that it can generate a STOP condition to end the transaction and free the bus.

A NACK can be generated for various reasons, for example:

- After an I^{2}C device address is transmitted, there is NO receiver with that address on the bus to respond.
- The receiver is busy performing an internal operation (e.g., reset, recall, etc) and cannot respond.
- The Master (acting as a receiver) needs to indicate the end of a transfer with the Slave (acting as a transmitter).

DEVICE ADDRESS AND R/$\overline{W}$ BIT

Data transfers follow the format shown in Figures 46 and 47 on page 19. After a valid START condition, the first byte sent in a transaction contains the 7-bit Device (Slave) Address plus a direction (R/$\overline{W}$) bit. The Device Address identifies which device (of up to 127 devices on the I^{2}C bus) the Master wishes to communicate with.

After a START condition, the ISL98608IIH monitors the first 8 bits (Device Address Byte) and checks for its 7-bit Device Address in the MSBs. If it recognizes the correct Device Address, it will ACK and becomes ready for further communication. If it does not see its Device Address, it will sit idle until another START condition is issued on the bus.

To access the ISL98608IIH, the 7-bit Device Address is 0x29 (0101001x), located in MSB bits <b_7:b_1>. The eighth bit of the Device Address byte (LSB bit <b_0>) indicates the direction of transfer, READ or WRITE (R/$\overline{W}$). A “0” indicates a WRITE operation - the Master will transmit data to the ISL98608IIH (receiver). A “1” indicates a Read operation - the Master will receive data from the ISL98608IIH (transmitter) (see Figure 45).

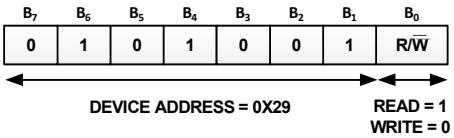


FIGURE 45. DEVICE ADDRESS BYTE FORMAT

Write Operation

A WRITE sequence requires an I^{2}C START condition, followed by a valid Device Address Byte with the R/$\overline{W}$ bit set to ‘0’, a valid Register Address Byte, a Data Byte and a STOP condition. After each valid byte is sent, the ISL98608IIH (slave) responds with an ACK. When the Write transaction is completed, the Master should generate a STOP condition. For sent data to be latched by the ISL98608IIH, the STOP condition should occur after a full byte (8 bits) is sent and ACK. If a STOP is generated in the middle of a byte transaction, the data will be ignored. See Figure 46 on page 19 for the ISL98608IIH I^{2}C Write protocol.

Read Operation

A READ sequence requires the Master to first write to the ISL98608IIH to indicate the Register Address/pointer to read from. First, Send a START condition, followed by a valid Device Address Byte with the R/$\overline{W}$ set to ‘0’ and then a valid Register Address Byte. Then the Master generates either a Repeat START condition or a STOP condition followed by a new START condition and a valid Device Address Byte with the R/$\overline{W}$ bit set to ‘1’. Then the ISL98608IIH is ready to send data to the Master from the requested Register Address.

The ISL98608IIH sends out the Data Byte by asserting control of the SDA pin while the Master generates clock pulses on the SCL pin. When transmission of the desired data is complete, the Master generates a NACK condition followed by a STOP condition and this completes the I^{2}C Read sequence. See Figure 47 on page 19 for the ISL98608IIH I^{2}C Read protocol.

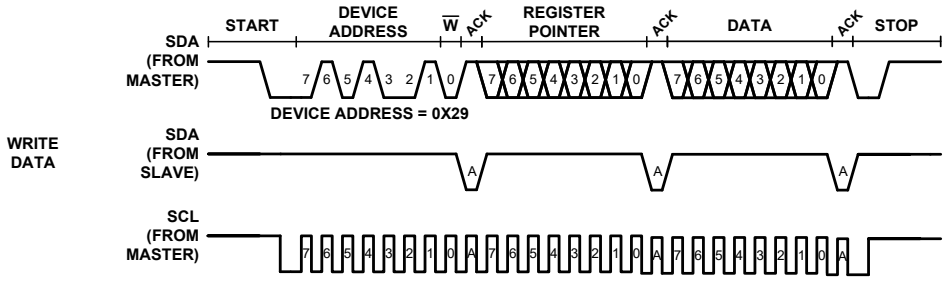


FIGURE 46. I²C WRITE TIMING DIAGRAM

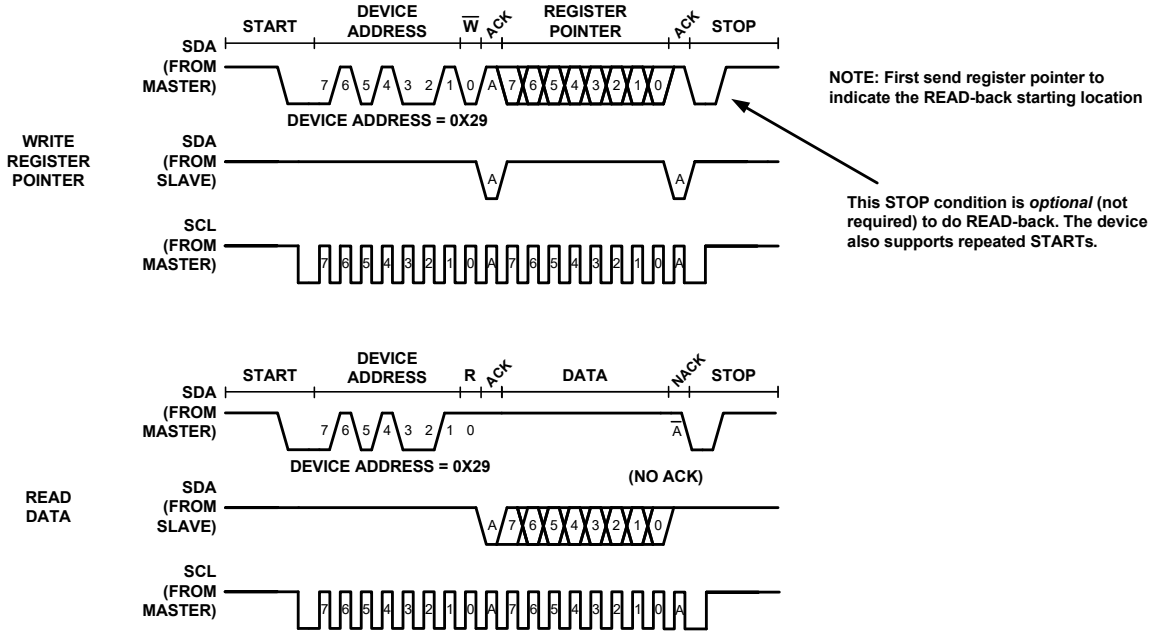


FIGURE 47. I²C READ TIMING DIAGRAM

Register Descriptions and Addresses

The "Register Map" on page 21 contains the detailed register map, with descriptions and addresses for ISL98608IIH registers. Each volatile register is one byte (8-bit) in size. When writing data to adjust register settings using I²C, the data is latched-in after the 8th bit (LSB) is received.

The ISL98608IIH has default register settings that are applied at IC power-up, and in some cases, updated based on fuse values at first enable. The default register settings are indicated with **BOLD** face text.

NOTE: To clear/reset all the volatile registers to the default values, power cycle VIN or clear the register 0x04 bit <b_7>.

Register Functions

The ISL98608IIH has various registers that can be used to adjust and control IC operating voltages, modes, thresholds and sequences.

FAULT

The "FAULT" register (Register Address 0x04) can be used to read back the current fault status of the IC. The fault conditions that can be read back by I²C are VBST undervoltage fault, VP undervoltage fault, VN undervoltage fault and over-temperature protection (OTP) fault.

If FAULT register bit <b_0> (OTP status bit) is latched high for an OTP fault, it can be reset by simultaneously cycling ENP and ENN.

If FAULT register bit <b_1> (VBST status bit) is latched high for a VBST undervoltage fault, it can be reset by cycling ENP and ENN together.

If FAULT register bit <b_2> (VN status bit) is latched high for a VN undervoltage fault, it can be reset by cycling ENN.

If FAULT register bit <b_3> (VP status bit) is latched high for a VP undervoltage fault, it can be reset by cycling ENP.

All fault bits can be cleared by cycling VIN or with a software reboot (clearing register 0x04 bit<b_7>). This will reset the entire part to default settings and disable all outputs until they have sequenced up again.

ENABLE

The "ENABLE" register (Register Address 0x05) can be used to control the enable/disable state of the boost (VBST), positive LDO (VP) and negative charge pump (VN). This can also be used to sequence the regulators. Refer to "Enable Timing Control Options for VP and VN Regulators" on page 26 for details regarding the control of output regulators using the enable and I^2C control. Using this register the VP and VN pull-down resistor can be enabled or disabled, soft-start time of VP and VN can be adjusted and the timing of VP sequencing can be adjusted.

Bit<4> of ENABLE register controls the delay between the ENP signal going low and the VP regulator power-off. If Bit<4> is set to 0, the VP regulator is disabled 2ms after ENP going low. If Bit<4> is set to 1, the VP regulator is disabled as soon as ENP goes low.

Bit<5> of ENABLE register controls shutdown behavior of VBST, VP and VN regulators after OTP or UV event. If Bit<5> is set to 1, then VBST, VP and VN regulators are shut off after OTP or UV event. To turn on the regulators, IC should be out of fault condition and ENP and ENN signals are recycled. Regulators can also be turned on by recycling the enable bit in the I^2C register. If Bit<5> is set to 0, then regulators will turn back on as soon as fault condition is removed.

Bit<6> controls the VN and VP discharge resistor. If Bit<6> is programmed to "0", then it will enable the discharge resistor where as "1" will disable the discharge resistor.

Bit<7> controls the soft-start time of VN and VP regulators. If Bit<7> is set to "0", then soft-start time of VN is 1.8ms and for VP is 1.2ms whereas when set to "1", soft-start time of both VP and VN regulator is 0.7ms.

VBST/VN/VN VOLTAGE

The output voltages of VBST, VP and VN regulators can be changed using the registers "VBST Voltage", "VP Voltage" and "VN Voltage," respectively. VBST voltage is at Register Address 0x06, VN voltage is at Register Address 0x08 and VP voltage is at Register Address 0x09. The output voltages of all regulators can be changed from their default values using I^2C.

- The VBST regulator can be programmed from +4.65V to +7.3V
- The VP regulator can be programmed from +4.5V to +7V
- The VN regulator can be programmed from -7V to -4.5V
- All are adjustable with 50mV step size.

Once the maximum VBST voltage (7.3V) is reached the algorithm will wrap around to give VBST voltage from 4.65V to 5.1V. Similarly, when maximum VP and VN voltage are reached (±7V), the algorithm will wrap around to give VP/VN voltage from ±4.5V to ±4.95V.

To determine the expected output voltage for a specific register value, see the following section "Output Voltage Calculation for VBST, VP and VN".

NOTE: Output voltage registers should not be changed during their respective soft-start sequence.

Output Voltage Calculation for VBST, VP and VN

The expected output voltage for each regulator can be determined using Equations 1 through 3. Note, *N* is the 5-bit register settings from 0x06, 0x08 and 0x09 in decimal.

The expected VBST voltage can be determined using Equation 1.

$$VBST(V) = VBST(Default)V + N \times 50mV \quad \text{(EQ. 1)}$$

Once the maximum VBST voltage is reached, the algorithm will wrap around to give VBST voltage from 4.65V to 5.1V.

The expected VP voltage can be determined using Equation 2.

$$VP(V) = VP(Default)V + N \times 50mV \quad \text{(EQ. 2)}$$

Once the maximum VP voltage is reached, the algorithm will wrap around to give VP voltage from 4.50V to 4.95V.

The expected VN voltage can be determined using Equation 3.

$$VN(V) = VN(Default)V - N \times 50mV \quad \text{(EQ. 3)}$$

Once the minimum VN voltage is reached, the algorithm will wrap around to give VN voltage from -4.50V to -4.95V.

Example Calculations:

If N = 10 (decimal) VBST(Default) = 5.15V, VP/VN(Default) = ±5V:

$$VBST(V) = 5.15V + 10 \times 50mV = 5.65V$$

$$VP(V) = 5V + 10 \times 50mV = 5.5V$$

$$VN(V) = -5V - 10 \times 50mV = -5.5V$$

The default output voltage of VBST, VP, and VN regulators can be determined by factory configurable settings. The output voltage can be changed using I^2C control when V_{IN} > POR (Power-On Reset) voltage. When powered up, Registers 0x06, 0x08, and 0x09 read value 0x00 and VBST, VN, VP voltage levels are at respective default voltage. Using I^2C control, the voltage can be changed by changing the value of Registers 0x06, 0x08, and 0x09. As V_{IN} < POR (Power-On Reset) voltage, Registers 0x06, 0x08, and 0x09 read 0x00.

VBST CONTROL

In addition to output voltage adjustments, key operation parameters can be changed using I^2C to optimize the ISL98608IIH performance.

The "VBST CNTRL and VBST/VN Frequency" register (Register Address 0x0D) can be used to control boost PFM mode, boost FET slew rate and switching frequency of the boost and charge pump.

Register Map

REGISTER ADDRESS (HEX)	REGISTER NAME	R/W	FUNCTION	BIT <b_7>	BIT <b_6>	BIT <b_5>	BIT <b_4>	BIT <b_3>	BIT <b_2>	BIT <b_1>	BIT <b_0>	DEFAULT VALUE (HEX)	IC RESET
0x04	**FAULT/ STATUS**	R/W[7] R[6:0]	Fault Status Read-back	Reboot 1 = Reset all digital (reverts to 0 once reboot completes) **0 = Normal operation**	Not used		Start VP and VN together **0 = Sequenced** 1 = Start together	VP UVP **0 = Output Voltage OK** 1 = UVP Detect if VP <60% for >100µs	VN UVP **0 = Output Voltage OK** 1 = UVP Detect if VN <60% for >100µs	VBST UVP **0 = Output Voltage OK** 1 = UVP Detect if VBST <70% for >100µs	OTP **0 = Temp Ok** 1 = OTP detected, Temp =+150°C for >10µs	0x00	Cycle VIN or Bit 0 - cycle ENN and ENP Bit 1 - cycle ENN and ENP Bit 2 - cycle ENN Bit 3 - Cycle ENP
0x05	**ENABLE**	R/W	IC Enable/ Sequencing	VP/VN soft-start times **0 = VP = 1.2ms VN = 1.8ms** 1 = VP = VN = 0.7ms	VP/VN Discharge Resistor **0 = Enabled** 1 = Disabled	Enable shutdown of VBST/VP/VN at OTP or if any is UV after start-up. 0 = Disabled **1 = Enabled**	Delay VP off **0 = VP off 2ms after ENP** 1 = VP off with ENP	Reserved	VP Enable: 0 = Disable **1 = Enable**	VN Enable: 0 = Disable **1 = Enable**	VBST Enable: 0 = Disable **1 = Enable**	0x27	Cycle VIN or clear the register 0x04 bit <b7>
0x06	**VBST VOLTAGE**	R/W	VBST Voltage Adjustment	Not Used	VBST Voltage <5:0> VBST = VBST(Default)V + N x 50mV Once the maximum voltage is reached the algorithm will wrap around to give 4.65V to 5.1V options							0x00	Cycle VIN or clear the register 0x04 bit <b7>
0x08	**VN VOLTAGE**	R/W	VN Voltage Adjustment	Not Used	VN Voltage <5:0> VN = VN(Default)V - N x 50mV Once the min voltage is reached the algorithm will wrap around to give -4.5V to -4.95V options							0x00	Cycle VIN or clear the register 0x04 bit <b7>
0x09	**VP VOLTAGE**	R/W	VP Voltage Adjustment	Not Used	VP Voltage <5:0> VP = VP(Default)V + N x 50mV Once the maximum voltage is reached the algorithm will wrap around to give 4.5V to 4.95V options							0x00	Cycle VIN or clear the register 0x04 bit <b7>
0x0D	**VBST control and VBST/VN FREQUENCY**	R/W	VBST control and VBST/VN frequency	Reserved	Reserved	Power FET slew rate control 00 = Slowest 01 = Slow 10 = Fast **11 = Fastest**		PFM mode **0 = Enabled** 1 = Disabled	VBST and VN switching frequency 000 = 1.00MHz 001 = 1.07MHz 010 = 1.23MHz 011 = 1.33MHz **100 = 1.45MHz** 101 = 1.60MHz 110 = 1.78MHz 111 = 2.00MHz			0xB4	Cycle VIN or clear the register 0x04 bit <b7>

Display Power Supply Function Description

Regulator Output Enable/Disable

The boost converter, VBST, will be enabled whenever either ENP *or* ENN is HIGH and the VBST enable bit <b_0> in the ENABLE register is set to '1'. To disable the boost (and effectively VP and VN), ENN and ENP must be LOW, or its enable bit set to '0'.

The negative charge pump, VN, is enabled whenever ENN is HIGH and the VN enable bit <b_1> in the ENABLE register is set to '1'. To disable, ENN must be LOW, or its enable bit set to '0'.

The LDO, VP, is enabled whenever ENP is HIGH and the VP enable Bit <b_2> in the ENABLE register is set to '1'. To disable ENP must be LOW, or its enable bit set to '0'.

All the ENABLE register bits <b_2:b_0> are set to '1' by default.

Note, ENP and ENN are logic level inputs with HIGH/LOW thresholds defined by the V_{IH}/V_{IL} specifications, respectively. These inputs also have 1MΩ (typical) internal pull-down resistance to ground. If the pins are left at high-impedance, they will default to a LOW logic state. Refer to the "LOGIC/DIGITAL" on page 7 of the "Electrical Specifications" table for more information.

VP and VN Headroom Voltage and Output Current

The VP and VN headroom voltage is defined as the difference between the VBST target voltage and maximum of VP and |VN| target voltages.

The headroom voltage must be set high enough so that both the VP LDO and VN negative Charge Pump (CP) can maintain regulation. The VBST voltage must be greater than the absolute value of the VN regulation voltage (i.e., the headroom voltage has to be >0V). Primarily, the minimum headroom voltage is a function of the maximum application load current that the IC will need to support. Fast output current peaks of only a few microseconds should not be considered - those instantaneous current peaks will be supported by the output capacitors and not by the regulator. Equation 4 shows the minimum headroom required depending upon the current.

$$\text{Headroom}(V) > \text{Imax}(A) X 2.7 \quad \text{(EQ. 4)}$$

Note the headroom voltage should not be set overly high, since increasing headroom generally yields lower efficiency performance due to increased conduction losses.

For very low duty cycle where the output voltage of the VBST is very close to the input voltage, VBST starts to track the input voltage with a fixed headroom of ~600mV. This feature avoids the minimum duty cycle limitation from producing increased ripple on VBST (which feeds through to VP/VN) and ensures proper regulation of the VBST, VP and VN regulators.

For most applications, the ISL98608IIH default 400mV headroom voltage setting provides optimal performance for DC output current up to 200mA (maximum).

Negative Charge Pump Operation (VN)

The ISL98608IIH uses a negative charge pump with internal switches to create the VN voltage rail. The charge pump input voltage VBSTCP comes from the boost regulator output, VBST.

Regulation is achieved through a classic voltage mode architecture where an internally compensated integrator output is compared with the voltage ramp to set a duty cycle. The duty cycle controls the amount of time the output capacitor is charged during each switching cycle. The maximum duty cycle is 50%. The charge pump output capacitor (placed on the VN pin) is pumped through internal current source to minimize system noise.

VN and VBST PFM

The ISL98608IIH features light-load Pulse Frequency Modulation (PFM) mode for both the boost regulator and the charge pump, to maximize efficiency at light loads.

The device always uses PWM mode at heavy loading, but will automatically switch to PFM mode at light loads to optimize efficiency. PFM capability is enabled using the respective PFM mode enable/disable register bits.

VBST PFM

In PFM mode, the boost can be configured to either use a fixed peak current or to automatically select the optimal peak current setting. The automatic, or "Auto" mode, is designed to dynamically adjust the peak current to maintain boost output voltage ripple at relatively fixed levels across input voltage, while improving efficiency at low input voltages. This patent pending architecture adjusts the peak current to keep the sum of inductor ramp-up and ramp-down times to a constant value of approximately $1.3*T_{PWM}$. This scheme also gives more consistent ripple part-to-part and keeps PWM/PFM hysteresis defined in a smaller and more optimal band across operating voltages. It is recommended to operate the part in this mode.

The VBST PFM mode features an ultrasonic Audio Band Suppression (ABS) mode, which prevents the switching frequency from falling below 30kHz to avoid audible noise. When the time interval between two consecutive switching cycles in PFM mode is more than 33ms (i.e., 30kHz frequency) the regulator reduces the peak inductor current, to maintain the frequency at 30kHz. If this is not sufficient, the regulator will add low current reverse current cycles.

VN PFM

The charge pump PFM mode works by increasing the minimum pump on-time, and thereby the charge delivered per cycle, when the load is low. This allows increased ripple to be traded off against switching losses.

VP/VN Output Hi-Z Mode

The ISL98608IIH VP and VN regulator can be configured in a Hi-Z mode to prevent any leakage current flowing between VP and VN. Using I^2C register 0x05 <b_6> can be used to disable the pull-down resistors on VP and VN giving a “Hi-Z” state of output.

Power-On/Off Sequence

The boost regulator used to generate VP/VN, VBST, is activated when the VIN input voltage is higher than the UVLO threshold, and either ENP or ENN is high, along with their respective I^2C enable bits. To enable the VBST, Reg 0x05 <b_0> should be 1 (by default this bit is set to 1). The VP output is activated if ENP is high, VBST has completed its soft-start and Reg 0x05 <b_2> is 1 (by default this bit is set to 1). The VN charge pump is activated 2ms after VBST has completed soft-start and the ENN has been pulled high, whichever comes later. To activate the VN regulator, Reg 0x05 <b_1> should also be 1 (by default this bit is set to 1).

Figure 48 shows the power-on sequence for the case when the ENP and ENN all are tied together and VP/VN rail sequencing is enabled in register 0x04 <b_4> by writing “0” and VP soft-start time is 1.2ms where as VN soft-start time is 1.8ms programmed from register 0x05 <b_7> by writing “1”. The VBST soft-starts if the VIN voltage is higher than the UVLO threshold and either ENN or ENP is high. When the VBST soft-start is completed, the VP regulator soft-starts in 1.2ms. The VN power-on occurs 2ms after VBST soft-start completes. The VN soft-start time takes 1.8ms. The 2ms power-on delay between VP and VN can be disabled from register 0x04 <b_4> by writing “1”.

Figure 49 shows the power-on sequence for the case when the ENP and ENN all are tied together and VP/VN rail sequencing is enabled in register 0x04 <b_4> by writing “0” and VP/VN soft-start time is programmed to 0.7ms from register 0x05 <b_7> by writing “1”. The VBST soft-starts if the VIN voltage is higher than the UVLO threshold and either ENN or ENP is high. When the VBST soft-start is completed, the VP regulator soft-starts in 0.7ms. The VN power-on occurs 2ms after VBST soft-start completes. The VN soft-start time takes 0.7ms. The 2ms power-on delay between VP and VN can be disabled from register 0x04 <b_4> by writing “1”.

Figure 50 shows the power-on sequence for the case when the ENP and ENN all are tied together and VP/VN rail sequencing is disabled in register 0x04 <b_4> by writing “1” and VP/VN soft-start time is programmed to 1.2ms from register 0x05 <b_7> by writing “0”. The VBST soft-starts if the VIN voltage is higher than the UVLO threshold and either ENN or ENP is high. When the VBST soft-start is completed, the VP and VN regulator soft-starts in 1.2ms.

Figure 51 shows the power-on sequence for the case when the ENP and ENN all are tied together and VP/VN rail sequencing is disabled in register 0x04 <b_4> by writing “1” and VP/VN soft-start time is programmed to 0.7ms from register 0x05 <b_7> by writing “1”. The VBST soft-starts if the VIN voltage is higher than the UVLO threshold and either ENN or ENP is high. When the VBST soft-start is completed, the VP and VN regulator soft-starts in 0.7ms.

The VP/VN/VBST soft-start times quoted above (VBST = 0.47ms, VP = 1.2ms and VN = 1.2ms or 1.8ms) are valid for the default voltage levels (VSBT = 5.15V, VP = 5V and VN = -5V). These will change with different voltages, as they are set to give a fixed dv/dt.

Figure 52 shows the power-on sequence for the case when the ENP and ENN are controlled by two GPIOs and VP/VN rail sequencing is enabled from register 0x04 <b4> by writing "0". Also, VP soft-start time is programmed to 1.2ms and VN soft-start time is programmed to 1.8ms from register 0x05 <b7> by writing "0".

ENP or ENN going low will shut down VP or VN, respectively. If both ENP and ENN are pulled low, then VP, VN and VBST are all turned off. The VN regulator shuts off when ENN is pulled low. VP and VBST power-off occurs 2ms after the ENP signal goes low (Register 0x05<b_4> = 0), (see Figure 53). If Register 0x05<b_4> = 1, the VP and VN regulators will power off immediately when ENN and ENP are pulled low (see Figure 54).

If VIN falls below UVLO while the IC is active, all active regulators will be turned off at the same time (see Figure 55).

VP AND VN DISCHARGE RESISTOR

The integrated discharge resistors on the VP and VN outputs are 80Ω (typical) and 35Ω (typical), respectively. The VP discharge resistor is enabled for 2ms (by default) following when ENN goes low. If ENP is still high, the VP discharge resistor is disabled 2ms after ENN goes low. The VP discharge resistor will be re-enabled when ENP goes low. If the same output capacitor (value, size, rating) is used for VN and VP, the VN rail will discharge faster than VP if they are both turned off at the same time. This is ideal for applications that require the VN rail to go down before VP at power-off.

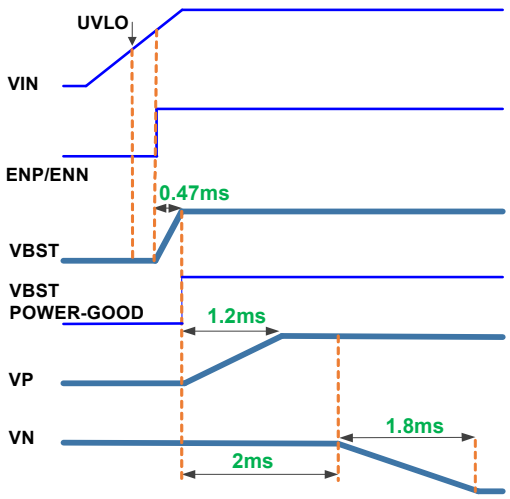


FIGURE 48. POWER-ON SEQUENCE – ACTIVATED BY ONE GPIO FOR ENN AND ENP, REGISTER 0x04 <b_4> = 0 AND 0x05 <b_7> = 0

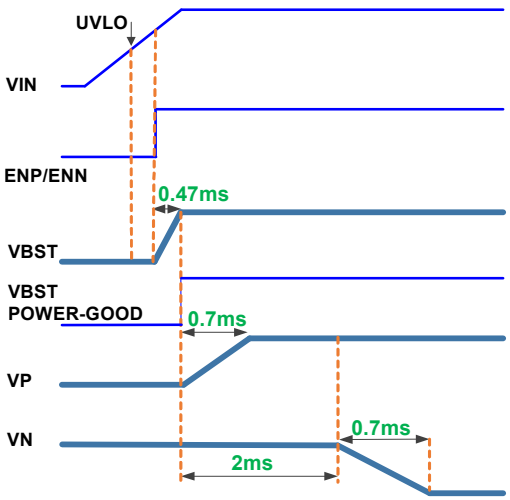


FIGURE 49. POWER-ON SEQUENCE – ACTIVATED BY ONE GPIO FOR ENN AND ENP, REGISTER 0x04 <b_4> = 0 AND 0x05 <b_7> = 1

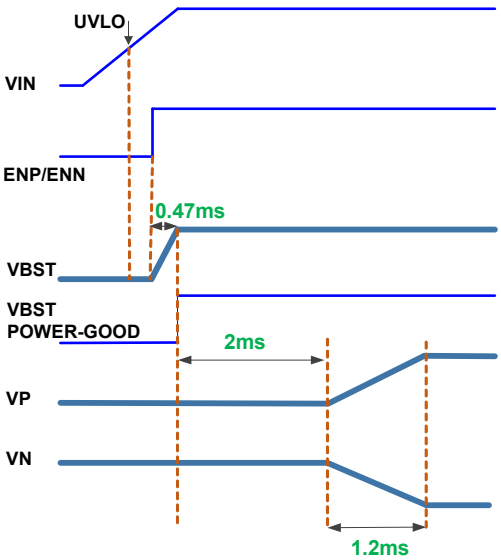


FIGURE 50. POWER-ON SEQUENCE – ACTIVATED BY ONE GPIO FOR ENN AND ENP, REGISTER 0x04 <b_4> = 1 AND 0x05 <b_7> = 0

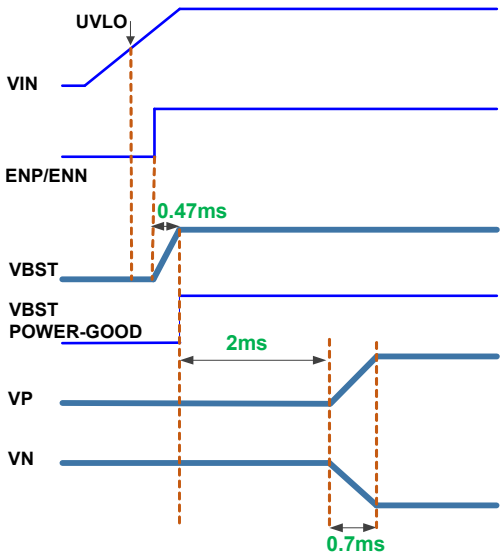


FIGURE 51. POWER-ON SEQUENCE – ACTIVATED BY ONE GPIO FOR ENN AND ENP, REGISTER 0x04 <b_4> = 1 AND 0x05 <b_7> = 1

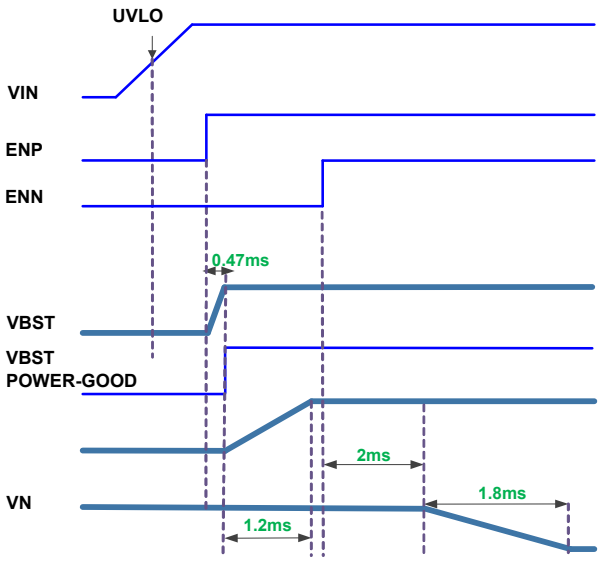


FIGURE 52. POWER-ON SEQUENCE – ACTIVATED BY TWO GPIOs FOR ENN AND ENP, REGISTER 0x04 <b_4> = 0 AND 0x05 <b_7> = 0

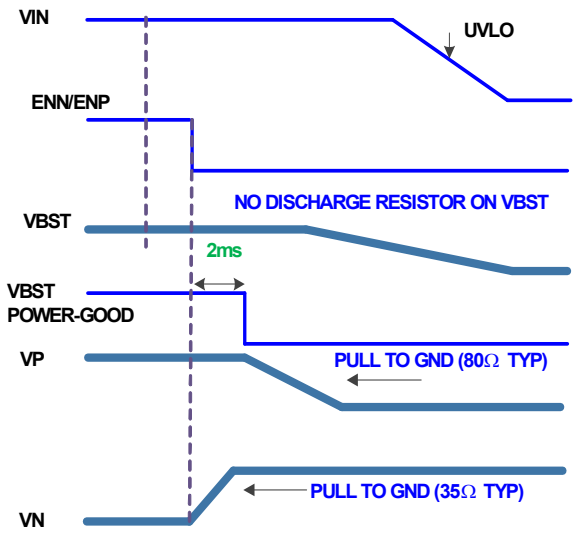


FIGURE 53. POWER-OFF SEQUENCE - ACTIVATED BY TWO GPIOs ENN AND ENP, REGISTER 0x05 <b_4> = 0

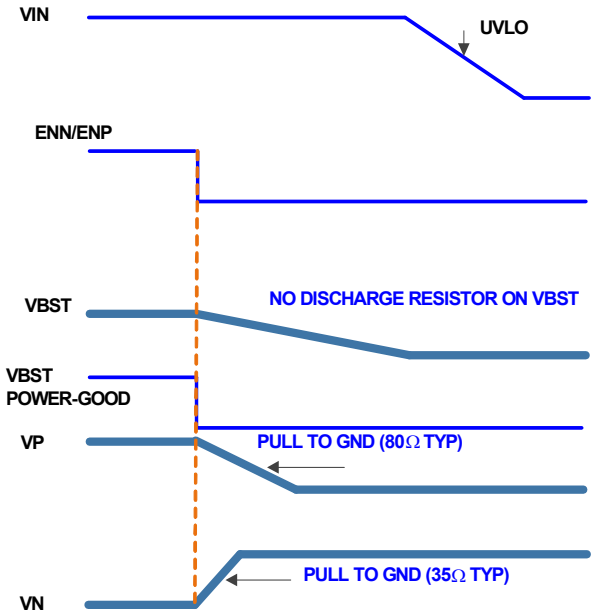


FIGURE 54. POWER-OFF SEQUENCE - ACTIVATED BY TWO GPIOs ENN AND ENP, REGISTER 0x05 <b_4> = 1

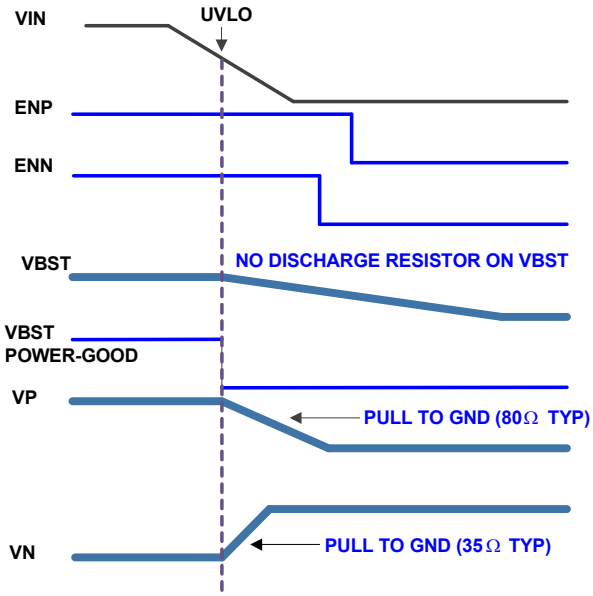


FIGURE 55. POWER-OFF SEQUENCE - ACTIVATED BY VIN FALLING BELOW UVLO

Enable Timing Control Options for VP and VN Regulators

There are several ways to control enable sequencing of the VP and VN regulators: I²C control, and dual or single GPIO control.

I²C CONTROL

By using I²C, the sequencing of the VP and VN regulator can be controlled by writing to register 0x02. Bit <b_1> controls the VN regulator and <b_2> controls the VP regulator. Setting the bits to '1' will enable the regulator and setting to '0' will shut off/disable the regulator. Delaying the writes for setting bit <b_1> and <b_2> (using separate I²C transactions) will delay the turn-on/off sequence of VP and VN accordingly. When using I²C to control the sequencing, ENN and ENP should be pulled low before writing to the I²C register to disable the VP and VN regulators and then ENN and ENP can go high before the I²C is used to enable them.

Figure 56 shows a 14ms delay between when VP and VN turn-on. The 14ms time is an example delay to show the power-on sequencing possibility through I²C. This delay is set between the separate I²C writes to set the enable bits in register 0x02. If both enable bits were set to '1' in the same I²C transaction (same byte) and ENN and ENP are high, then both VP and VN regulators will start power-on sequencing at the same time (when the data is latched at the STOP condition). The VN will come up 2ms after VP if register 0x02<b_6> is low and with VP if high.

Figure 57 shows a 14ms delay between the VP and VN turn-off. The 14ms time is an example delay to show the power-off sequencing possibility using I²C.

Figures 58 (zoom in) and 59 (zoom out) show a typical I²C data transfer to the ENABLE register. In this example, VP and VN regulators are enabled by writing data 0x07 to register address 0x02. The VP regulator will be enabled first after the I²C STOP condition, followed by the VN regulator after the internal 2ms delay.

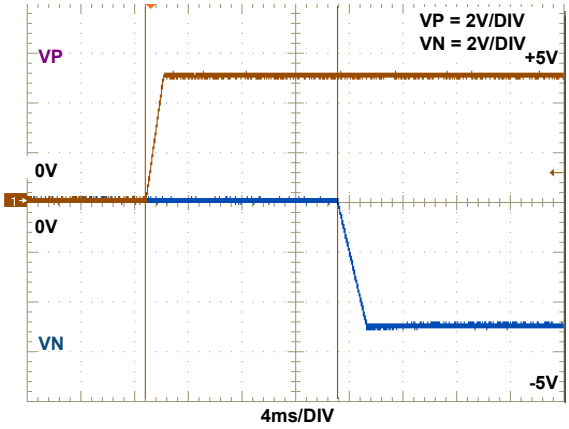


FIGURE 56. ON SEQUENCE, I²C CONTROL

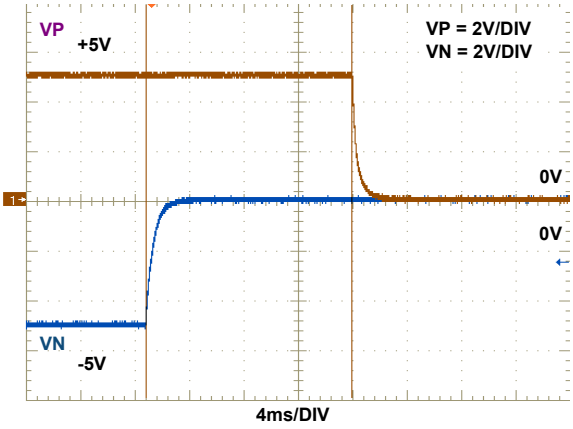


FIGURE 57. OFF SEQUENCE, I²C CONTROL

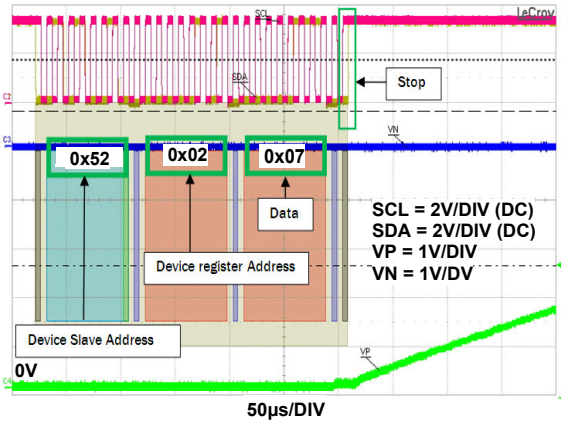


FIGURE 58. I²C SEQUENCE AND VP RESPONSE

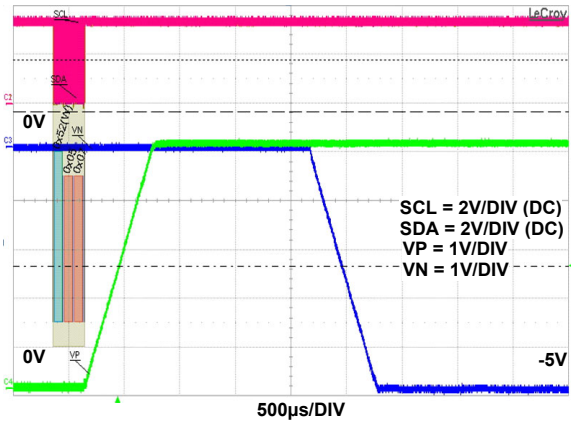


FIGURE 59. I²C SEQUENCE AND VP/VN RESPONSE

SEPARATE ENP AND ENN PINS (2 GPIO CONTROL)

Using two separate GPIO's, and controlling the timing between the ENP and ENN pins, the turn-on/off events can be controlled. The method to control turn-on/off by GPIO is valid when the respective enable bits in the ENABLE register at Register Address 0x02 are set to '1' (default). Thus, this method can be used with no I^2C communication.

Figure 60 shows a 6ms delay (example) between the ENP and ENN rise.

Figure 61 shows a 13ms delay (example) between the ENP and ENN fall.

TIE ENP AND ENN TOGETHER (1 GPIO CONTROL)

There is also an option to sequence the VN and VP regulators if there is only a single GPIO available in the system. The method to control turn-on/off by GPIO is valid when the respective enable bits in the ENABLE register at Register Address 0x02 are set to '1' (default). Therefore, this method can be used with no I^2C communication.

If the ENP and ENN are tied together and both pulled high and register 0x02<b_6> = "0", then there is a default delay sequence in the IC. VP will come up first and after 2ms VN will soft-start. For turn off, VN will power-off first, and VP starts to shut down 2ms after VN starts to power-off.

Figure 62 shows turn-on when the ENN and ENP pins are tied together. There is a 2ms delay between VP and VN turning on.

Figure 63 shows turn-off when the ENN and ENP are tied together.

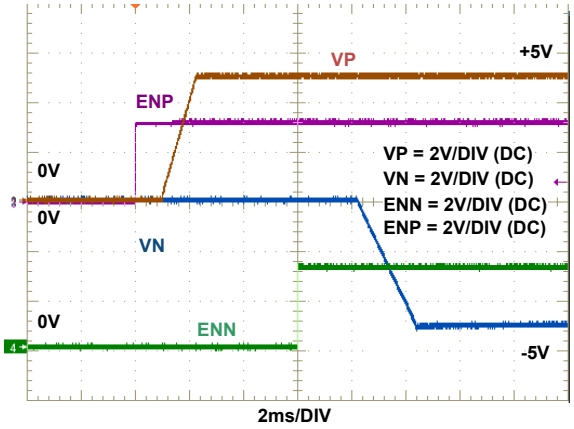


FIGURE 60. ON SEQUENCE, 2 GPIO CONTROL

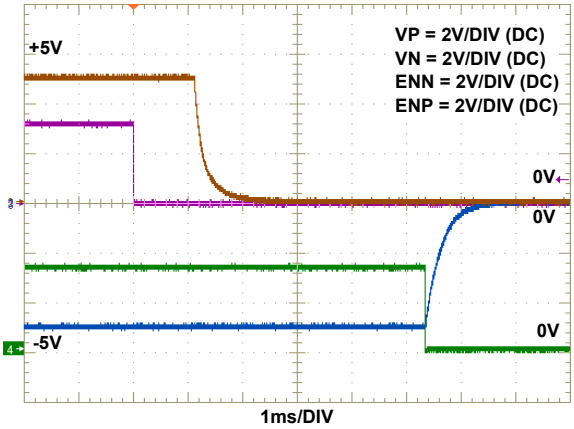


FIGURE 61. OFF SEQUENCE, 2 GPIO CONTROL

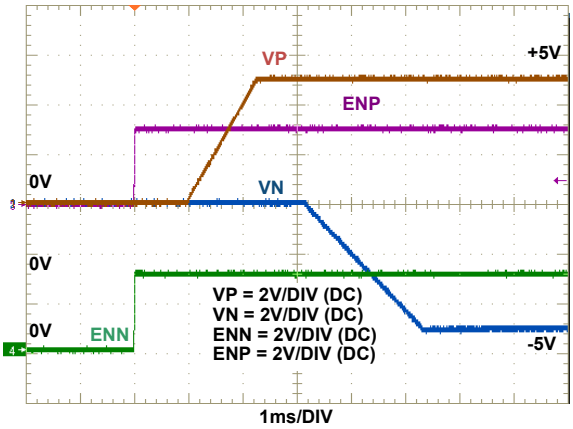


FIGURE 62. ON SEQUENCE, 1 GPIO CONTROL

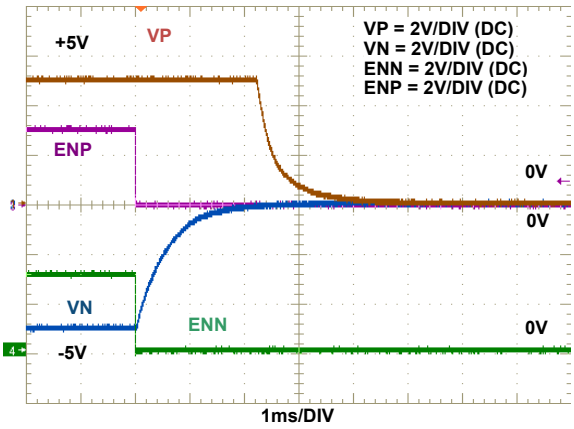


FIGURE 63. OFF SEQUENCE, 1 GPIO CONTROL

Fault Protection and Monitoring

The ISL98608IIH features extensive protections to automatically handle failure conditions and protect the IC and application from damage.

OVERCURRENT PROTECTION (OCP)

The overcurrent protection limits the VBST nMOSFET current on a cycle-by-cycle basis. When the nMOSFET current reaches the current limit threshold, the nMOSFET is turned off for the remainder of that cycle. Overcurrent protection does not disable any of the regulators. Once the fault is removed, the IC will continue with normal operation.

UNDERVOLTAGE LOCKOUT (UVLO)

If the input voltage (V_{IN}) falls below the V_{UVLO_HYS} level of ~2.3V (typical), the VBST, VP and VN regulators will be disabled. All the rails will restart with normal soft-start operation when the V_{IN} input voltage is applied again (rising $V_{IN} > V_{UVLO}$). Refer to the "Electrical Specifications" table on page 6 for the UVLO specifications.

Note, the I^2C registers (logic) are not cleared/reset to default by the falling V_{IN} UVLO. The logic states are retained if V_{IN} remains above 2V (typical). Once V_{IN} falls below 2V, all logic is reset. V_{IN} should fall below 2V (ideally to GND) before power is reapplied to ensure a full power cycle/reset of the device.

OVER-TEMPERATURE PROTECTION (OTP)

The ISL98608IIH has a hysteretic over-temperature protection threshold set at +150°C (typical). If this threshold is reached, the VBST, VP and VN regulators are disabled immediately. As soon as temperature falls by 20°C (typical) then all the regulators automatically restart.

All register bits, except for Bit <b_0> of the FAULT register (Register Address 0x04), remain unaffected during an OTP fault event. When an OTP event occurs, FAULT register bit <b_0> is latched to '1'. This bit is reset/cleared by cycling both ENN and ENP (set LOW, then HIGH) at the same time, or by cycling VIN power. Bit <b_0> can also be reset after it is read twice by I^2C. A single I^2C read will return the bit value (status) and a second read will reset *only* the OTP bit.

Output undervoltage protection is disabled during an OTP event. Since the output voltages decrease during an OTP event because the regulators are disabled, this will not trigger a UVP fault.

UNDERVOLTAGE PROTECTION (UVP)

The ISL98608IIH includes output undervoltage protection. Undervoltage protection disables the regulator whenever the output voltage of VBST or VP falls below 60% of its set/regulated voltage, or the output voltage of VN goes above 60% of its set/regulated voltage, for 100µs or more. If the output voltage exceeds the 60% condition for less than 100µs, no fault will occur.

Depending on which regulator(s) fault, bit(s) <b_3>, <b_2>, or <b_1> in the FAULT register will be latched to '1' for VP, VN and VBST faults, respectively. The bit(s) are reset/cleared by cycling both ENN and ENP (set LOW, then HIGH) at the same time or by cycling VIN power.

Undervoltage protection can be disabled by making selection from register 0x05<b_5>.

Component Selection

The design of the boost converter is simplified by an internal compensation scheme, which allows an easy system design without complicated calculations. Select component values using the following recommendations.

Input Capacitor

It is recommended that a 10µF X5R/X7R or equivalent ceramic capacitor is placed on the VIN input supply to ground.

Inductor

First, determine the minimum inductor saturation current required for the application.

The ISL98608IIH operates in Continuous Conduction Mode (CCM) at higher load current and in Discontinuous Conduction Mode (DCM) at lighter loads. In CCM, we can calculate the peak inductor current using Equations 5 through 9.

Given these parameters:

- Input Voltage = V_{IN}
- Output Voltage = V_O
- Duty Cycle = D
- Switching Frequency = f_{SW}
- $t_{SW} = 1/f_{SW}$

Then the inductor ripple can be calculated as:

$$\Delta I_{P-P} = (V_{IN})*(D)/(L*f_{SW}) \quad \text{(EQ. 5)}$$

Where $D = 1 - (V_{IN}/V_O)$, then rewrite Equation 5:

$$\Delta I_{P-P} = (V_{IN})*(V_O - V_{IN})/(L*f_{SW}*V_O) \quad \text{(EQ. 6)}$$

The average inductor current is equal to the average input current, where I_{IAVG} can be calculated from the efficiency of the converter.

$$I_{IAVG} = (V_O*I_O)/(V_{IN}*\text{Efficiency}) \quad \text{(EQ. 7)}$$

To find the peak inductor current write the expression as:

$$I_{Pk} = \Delta I_{P-P}/2 + I_{IAVG} \quad \text{(EQ. 8)}$$

Substituting Equations 6 and 7 in Equation 8 to calculate I_{Pk}:

$$I_{PK} = 0.5*V_{IN}*(V_O - V_{IN})/(L*f_{SW}*V_O) + (V_O*I_O)/(V_{IN}*EFF) \quad \text{(EQ. 9)}$$

EXAMPLE FOR VBST REGULATOR

Consider the following parameters in the steady state VLED boost regulator operating in CCM mode.

V_{IN} = 2.5V

V_O = 5.3V

I_O = 0.100A

f_{SW} = 1.45MHz

Efficiency = 80%

L = 2.2µH

Substituting previous parameters in Equation 9 gives us:

I_{Pk} = 0.472A

The VBST regulator can be configured to either use a fixed peak current or to automatically select the optimal peak current setting. The automatic mode is designed to dynamically adjust the peak current to maintain boost output voltage ripple at a relatively fixed value across input voltage, while improving efficiency at low input voltages.

In order to avoid the inductor core saturation, the saturation current of the inductor selected should be higher than the greater of the peak inductor current (for CCM) and the peak current in PFM mode and current limit of the regulators. It is recommended to use an inductor that has saturation current rating higher than current limit of the boost regulator.

Auto PFM mode provides maximum efficiency using 2.2µH for the VBST regulator. L = 2.2µH is the optimal value for the VBST regulator.

Table 3 shows the recommended inductors for the VBST boost regulator.

TABLE 3. RECOMMENDED INDUCTORS FOR VBST REGULATOR

INDUCTOR PART NUMBER	INDUCTANCE (µH)	DCR (mΩ)	I_{SAT} (A)	FOOTPRINT SIZE
VLF302510MT-2R2M (TDK)	2.2	70	1.23	3025
DFE252012C (Toko)	2.2	90	2.00	2520
TFM201610G-2R2M (TDK)	2.2	150	1.20	2016

Output Capacitor

The output capacitor supplies current to the load during transient conditions and reduces the ripple voltage at the output. Output ripple voltage consists of two components:

1. The voltage drop due to the inductor ripple current flowing through the ESR of the output capacitor.
2. Charging and discharging of the output capacitor.

For low ESR ceramic capacitors, the output ripple is dominated by the charging and discharging of the output capacitor. The voltage rating of the output capacitor should be greater than the maximum output voltage.

The effective capacitance at the nominal output voltage should be ≥2.2µF for VBST and VP regulators, and ≥4.4µF for VN. It is recommended to use a 10µF X5R 10V or equivalent ceramic output capacitor for both VBST and VP outputs to provide a minimum of 2.2µF effective capacitance. For the VN output, it is recommended to use one or two 10µF X5R 10V or equivalent ceramic output capacitors. Using two VN output capacitors results in <50mV peak-to-peak output voltage ripple with input voltages from 2.5V to 5V.

Table 4 shows the recommended capacitors for various regulators in ISL98608IIH.

Note, capacitors have a voltage coefficient. The effective capacitance will reduce (derate) as the operating voltage/bias increases. Always refer to the manufacturer's derating information to determine effective capacitance for the operating conditions.

TABLE 4. RECOMMENDED OUTPUT CAPACITORS

CAPACITOR PART NUMBER	VALUE (µF)	SIZE	QUANTITY
GRM155R61A106ME11 (Murata)	10	0402	x5: C_{IN}, C_{VBST}, C_{VP}, C_{VN}, C_{CP} x1: C_{VN} (x2 for minimum ripple)
GRM188R61C475KAAJ (Murata)	4.7	0603	x5: C_{IN}, C_{VBST}, C_{VP}, C_{VN}, C_{CP} x1: C_{VN} (x2 for minimum ripple)

General Layout Guidelines

When designing the printed circuit board (PCB) layout for the ISL98608IIH, it is very important to understand the power requirements of the system. Some general best practices should be adhered to in order to create an optimal PCB layout:

1. Careful consideration should be taken with any traces carrying AC signals. AC current loops should be kept as short and tight as possible. The current loop generates a magnetic field, which can couple to another conductor, inducing unwanted voltage. Components should be placed such that current flows through them in a straight line as much as possible. This will help reduce size of loops and reduce the EMI from the PCB.
2. If trace lengths are long, the resistance of the trace increases and can cause some reduction in IC efficiency and can also cause system instability. Traces carrying power should be made wide and short.
3. In discontinuous conduction mode, the direction of the current is interrupted every few cycles. This may result in large di/dt (transient load current). When injected in the ground plane the current may cause voltage drops, which can interfere with sensitive circuitry. The analog ground and power ground of the IC should be connected very close to the IC to mitigate this issue.
4. One plane/layer in the PCB is recommended to be a dedicated ground plane. A large area of metal will have lower resistance, which reduces the return current impedance.

More ground plane area minimizes parasitics and avoids corruption of the ground reference.

5. Low frequency digital signals should be isolated from any high frequency signals generated by switching frequency and harmonics. PCB traces should not cross each other. If they must cross due to the layout restriction, then they must cross perpendicularly to reduce the magnetic field interaction.
6. The amount of copper that should be poured (thickness) depends upon the power requirement of the system. Insufficient copper will increase resistance of the PCB, which will increase heat dissipation.
7. Generally, vias should not be used to route high current paths.
8. While designing the layout of switched controllers, do not use the auto routing function of the PCB layout software. Auto routing connects the nets with the same electrical name and does not account for ideal trace lengths and positioning.

ISL98608IIH Specific Layout Guidelines

1. The input capacitor should be connected to the VIN pin (C1) with the smallest trace possible. This helps reject high frequency disturbances and promotes good regulation of the VBST, VP and VN regulators.
2. The inductor for VBST regulator should be connected between VIN and LXP pin with a short and wide trace to reduce the board parasitics. Careful consideration should be made in selecting the inductor as it may cause electromagnetic interference, which could affect IC functionality. A shielded inductor is recommended.
3. Bump VBSTCP is input to the charge pump regulator. This pin must be connected to VBST on the PCB, so that the boost regulator provides the input voltage supply for the charge pump. The CSP bumps for VBST and VBSTCP are A3 and A4 respectively. These two bumps should be connected/shorted to each other on the PCB with a short and thick trace to avoid parasitic inductance and resistance. A 10µF/10V capacitor should be used on trace connecting bump A3 and A4 to PGND. The distance of the capacitor from the bump A3 and A4 is critical - it should be placed very close to the IC with a short and thick trace.
4. The current return path for VBST boost regulator should be small as possible. The bump A1 is PGND. It is power ground for VBST regulator. A 10µF/10V capacitor should be placed between VBST and PGND.
5. Bump D3 is output of the negative charge pump (VN) and bump D2 is its substrate connection (VSUB). It is highly recommended that D3 and D2 are shorted together with a short and thick trace. It is recommended that 2x10µF/10V capacitors are placed on VN to minimize output ripple. Additionally, it will help minimize noise that may be coupled from the high frequency ripple of the charge pump.
6. Bumps B3 is output of the VP regulator. A 10µF/10V capacitor should be placed between VP and power ground.
7. Bump B4 is charge pump positive connection and bump D4 is charge pump negative connection. A 10µF/10V capacitor should be placed between bump B4 and D4. The capacitor between bump B4 and D4 charges and discharges every cycle and handles high current surges. The capacitor should be placed between CP and CN using short and thick trace.
8. Digital input pins ENN, ENP, SDA and SCL should be isolated from the high di/dt and dv/dt signals. Otherwise, it may cause a glitch on those inputs.
9. I^2C signals, if not used, should be tied to VIN.
10. Analog ground (AGND) and power ground (PGND) of the IC should be connected to each other. It is crucial to connect these two grounds at the location very close to the IC. The regulator should be referenced to the correct ground plane with the short and thick traces. For example, PGND is the power ground for VBST regulator, a capacitor should be placed between VBST and PGND with short and thick trace. All the ground bumps namely PGND, AGND and PGNDCP should be connected with a network of ground plane.
11. One plane/layer in the PCB is recommended to be a dedicated ground plane.
12. The solder pad on the PCB should not be larger than the solder mask opening for the ball pad on the package. The optimal solder joint strength, it is recommended a 1:1 ratio for the two pads.

Figure 64 on page 31 shows the recommended PCB layout for a typical ISL98608IIH application.

ISL98608IIH Layout

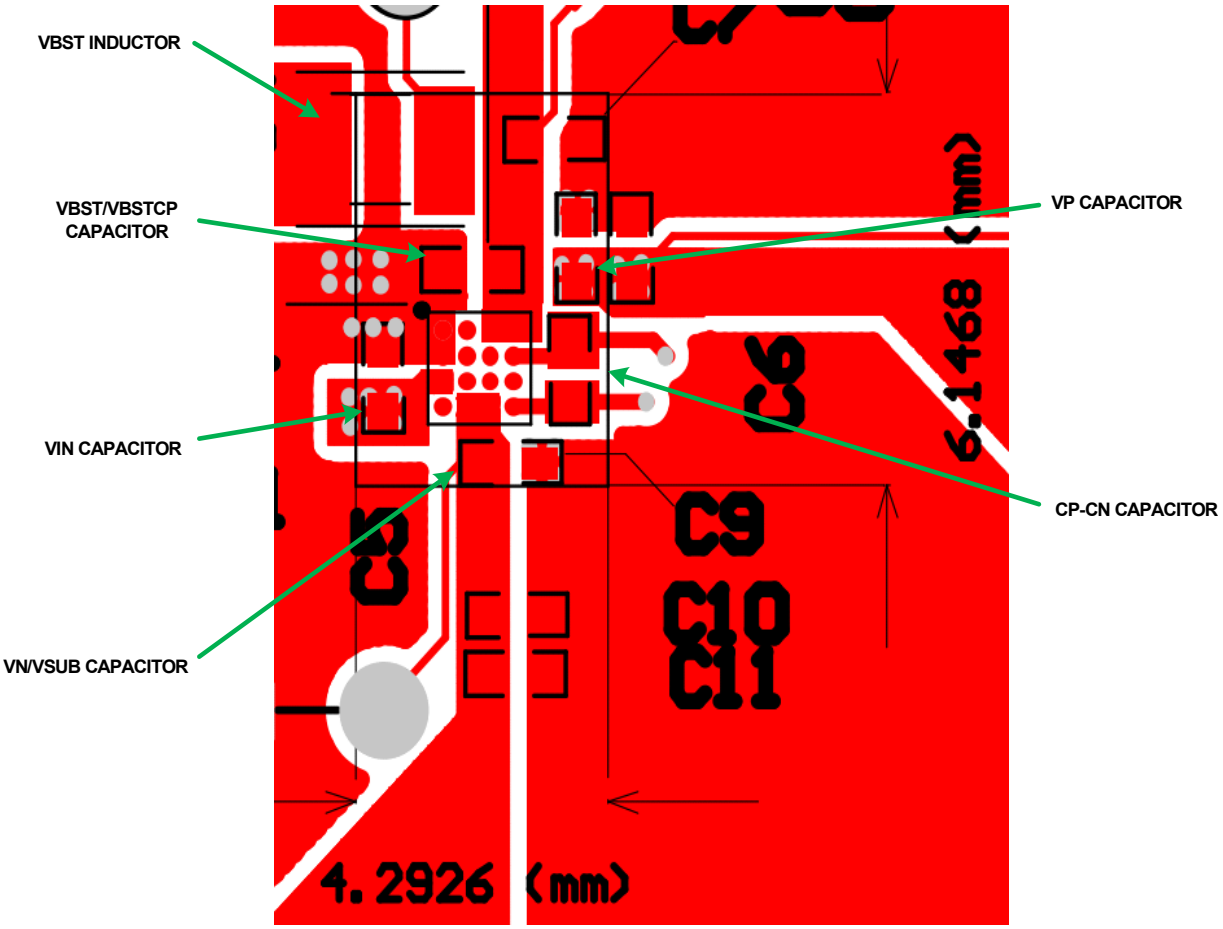


FIGURE 64. ISL98608IIH RECOMMENDED PCB LAYOUT

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
Dec 7, 2021	2.01	Removed references to 200mA max on VP and VN rails. Updated links throughout. Updated Ordering Information table formatting and notes. Removed About Intersil section.
Sep 26, 2017	2.00	Updated default value of Register 0x06 = 0x00 throughout the datasheet In the Electrical Specification table on page, updated bit <b7> for register 0x05 to 0 from 1 Label of LXLED changed to LX in figures 8-13 Eq 1, 2, and 3 have been modified A detailed description of default value of registers 0x06, 0x08 and 0x09 has been added before "VBST CONTROL" section Modified equations in Register 0x06, 0x08 and 0x09 in Register Map Updated POD W4x4.16G from rev 0 to rev 1. Changes since rev 0: Updated Typical Recommended Land Pattern Ball values: -Changed inner measurement from "0.240" to "0.215" -Changed outer measurement from "0.290" to "0.265" Added 4, 5, and 6 note markers. Added Notes 1 and 6. Switched order of Notes 3 and 4. Removed old Note 5.
Dec 23, 2015	1.00	Updated the input voltage range from “2.5V to 5V” to “2.5V to 5.5V” throughout the datasheet. In the “Register Map” on page 21, updated BIT<b0> for Register 0x04 changing from “130°C” to “150°C”.
Apr 1, 2015	0.00	Initial release

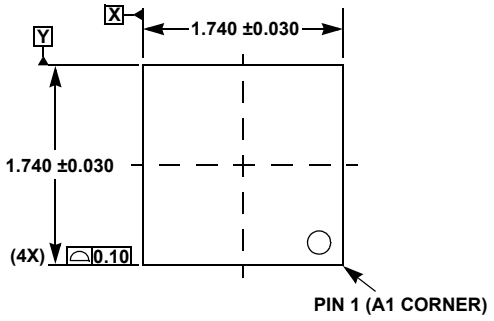
Package Outline Drawing

For the most recent package outline drawing, see W4x4.16G.

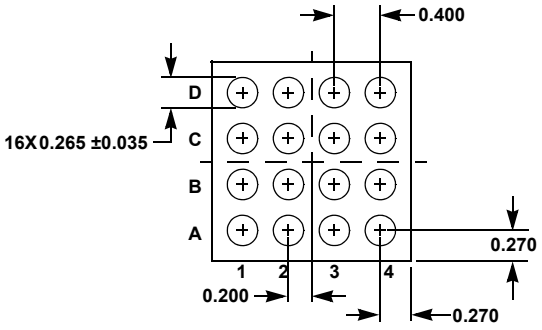
W4x4.16G

16 BALL WLCSP WITH 0.4mm PITCH 4x4 ARRAY (1.740mm x 1.740mm)

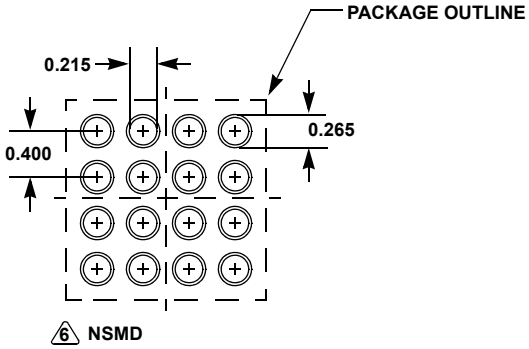
Rev 1, 9/16



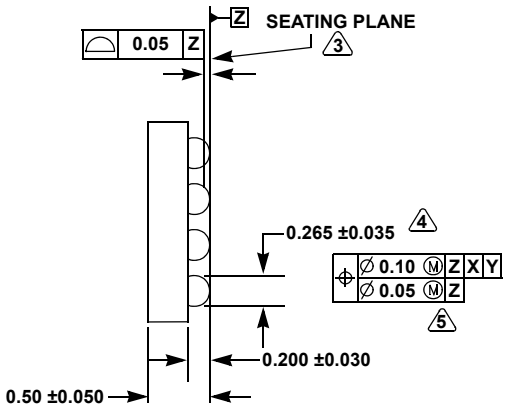
TOP VIEW



BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW

NOTES:

11. All dimensions are in millimeters.
12. Dimensions and tolerances per ASMEY 14.5-1994.
13. Primary datum Z and seating plane are defined by the spherical crowns of the bump.
14. Dimension is measured at the maximum bump diameter parallel to primary datum Z.
15. Bump position designation per JESD 95-1, SPP-010.
16. NSMD refers to non-solder mask defined pad design per techbrief, TB451.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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