DATASHEET

ISL95522

Hybrid Power Boost (HPB) and Narrow VDC (NVDC) Combo Battery Charger with SMBus Interface

The ISL95522 is a highly versatile combination battery charger configurable for operating as either a Hybrid Power Boost (HPB) charger or a Narrow VDC (NVDC) charger, supporting 2-, 3-, or 4-cell batteries. Both configurations allow the battery to work with the adapter to supply the system load when it exceeds the adapter capability, referred to as system Turbo mode. The HPB charger configuration reverse-boosts battery energy to the system bus to help the adapter provide the system power in Turbo mode. The NVDC charger configuration quickly turns on BGATE, which enables the battery to help the adapter provide the system power in Turbo mode.

The ISL95522 uses N-channel MOSFETs (NFETs) for all the switches to achieve the best performance and lowest BOM cost. The internal charge pump can turn on all the NFETs quickly or slowly, depending on the circumstance or need. The ability to quickly turn on NFETs prevents system bus voltage drop when the battery is suddenly removed in Turbo mode or in Battery Learn mode.

The ISL95522 provides many protection features, including a PROCHOT# indicator for system low voltage, adapter overcurrent, battery overcurrent, or overheating, with an array of SMBus programmable parameters for maximum flexibility. It also features a hardware-based adapter-current limit and battery-current limit in addition to SMBus programmable limits.

The ISL95522 provides a high accuracy adapter current monitor, battery current monitor, and system power monitor outputs. To provide maximum flexibility for working with high and low power systems, it provides several configurable current-sense resistor value options to achieve the best trade-off of current sensing accuracy vs power loss.

The ISL95522 uses the Renesas Robust Ripple Regulator (R3™) modulation scheme to provide excellent light-load efficiency and fast dynamic response. The ISL95522 is available in a 32 Ld 4x4mm^2 QFN package.

Features

- Configurable as an HPB charger or NVDC charger
- Compliant with Intel PROCHOT# and PSYS requirements
- Adapter current monitor and battery discharging current monitor
- Uses NFET for all the switches
    - Supports battery removal during Battery Learn mode
    - Actively controlled inrush current to prevent FET damage
- SMBus programmable settings and high accuracy
- Comprehensive protection features include:
    - PROCHOT# indicator for system low voltage, adapter overcurrent, battery overcurrent, or system overheating
    - Hardware-based adapter current and battery current limits
    - Supports sudden battery removal in system Turbo mode
- 16 switching frequency options from 350kHz to 1MHz
- Low quiescent current
- SMBus and auto-increment I^{2}C compatible
- Renesas Robust Ripple Regulator (R3) modulation scheme provides excellent light-load efficiency and fast dynamic response
- 32 Ld 4x4mm^2 QFN package
- Pb-free (RoHS compliant)

Applications

- Devices with rechargeable 2-, 3-, or 4-cell batteries

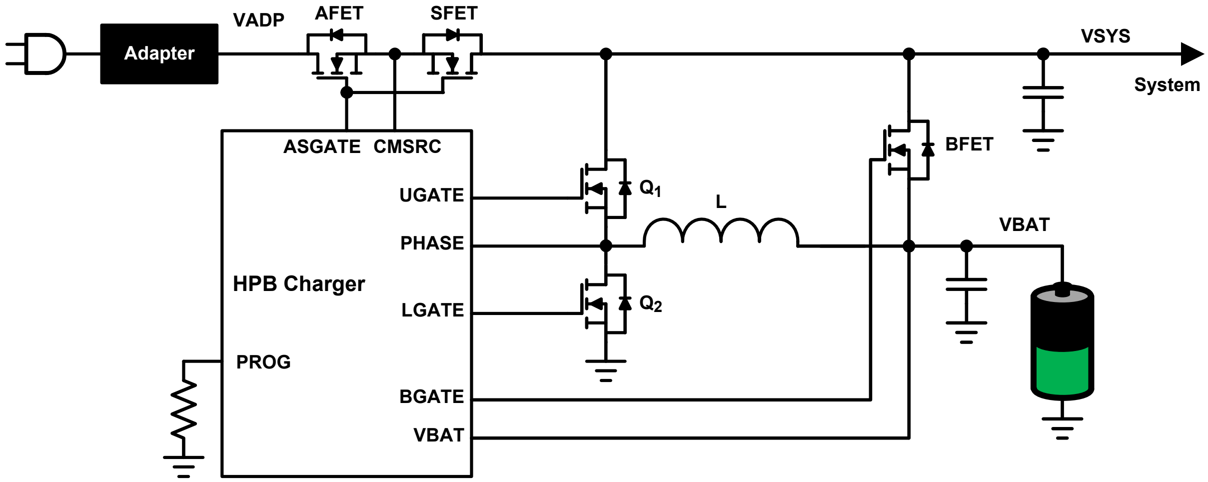


Figure 1. HPB Charger Configuration

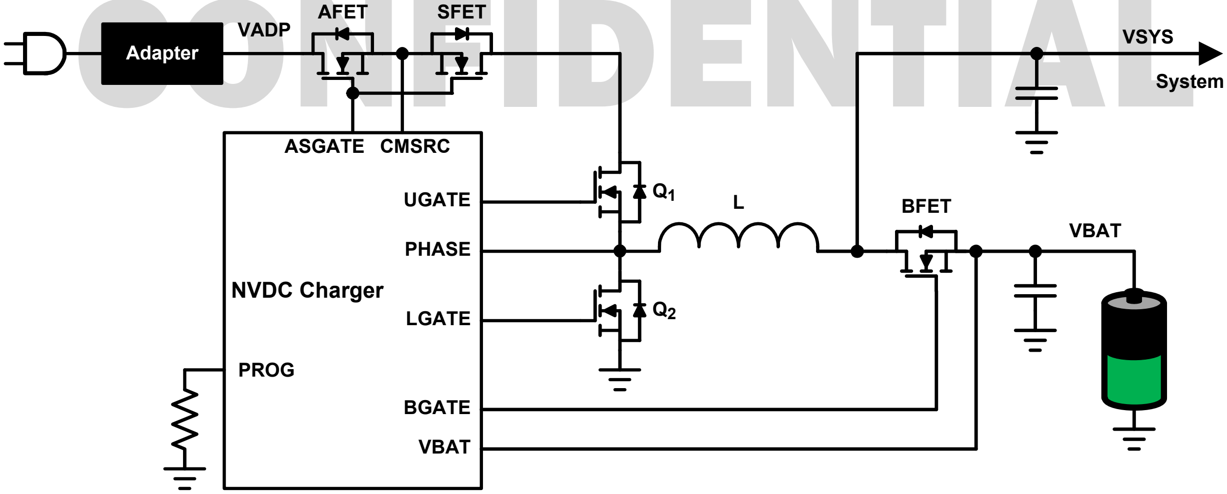


Figure 2. NVDC Charger Configuration

Contents

1. Overview

1.1 Block Diagram

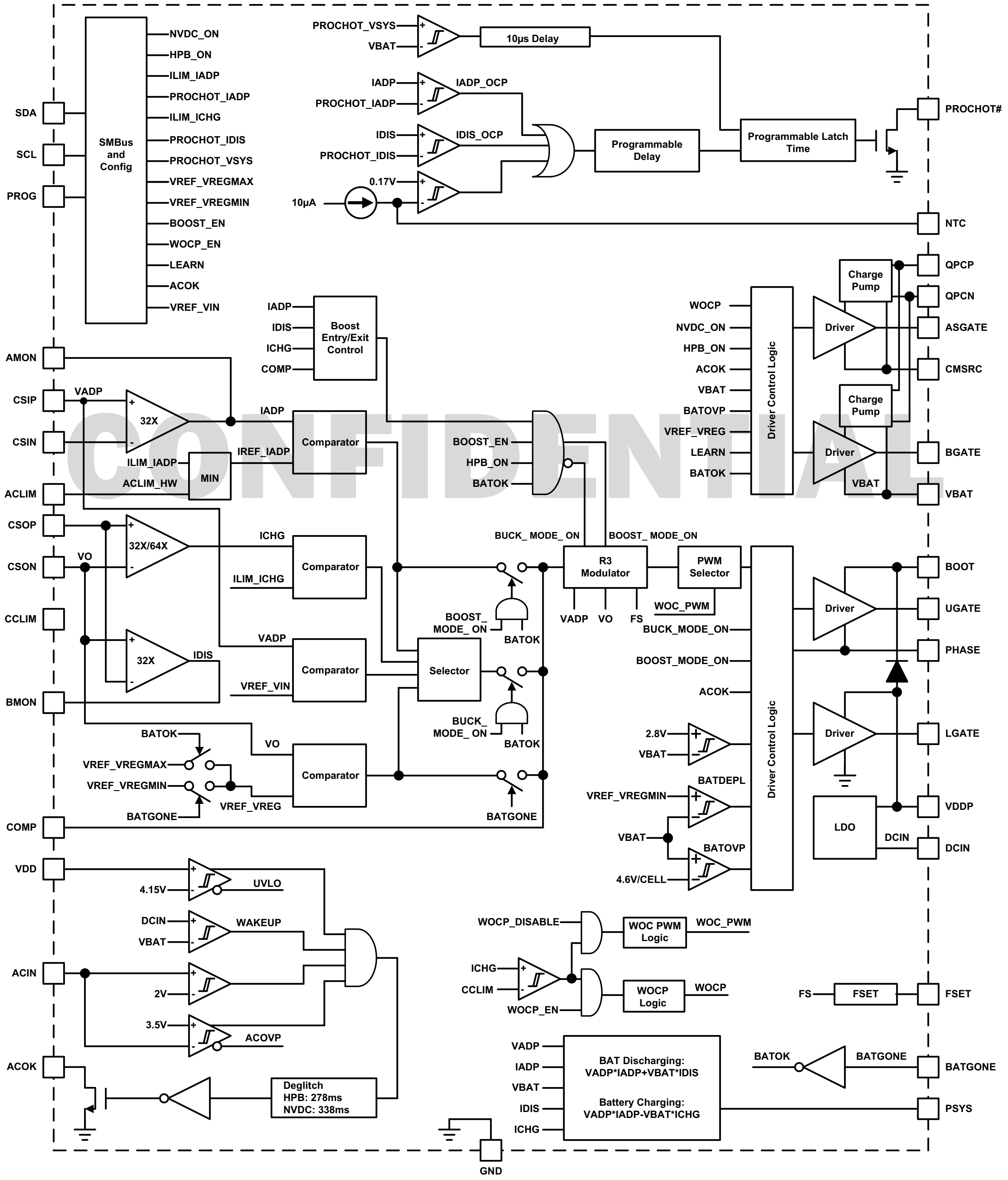


Figure 3. Block Diagram

1.2 Simplified Application Circuits

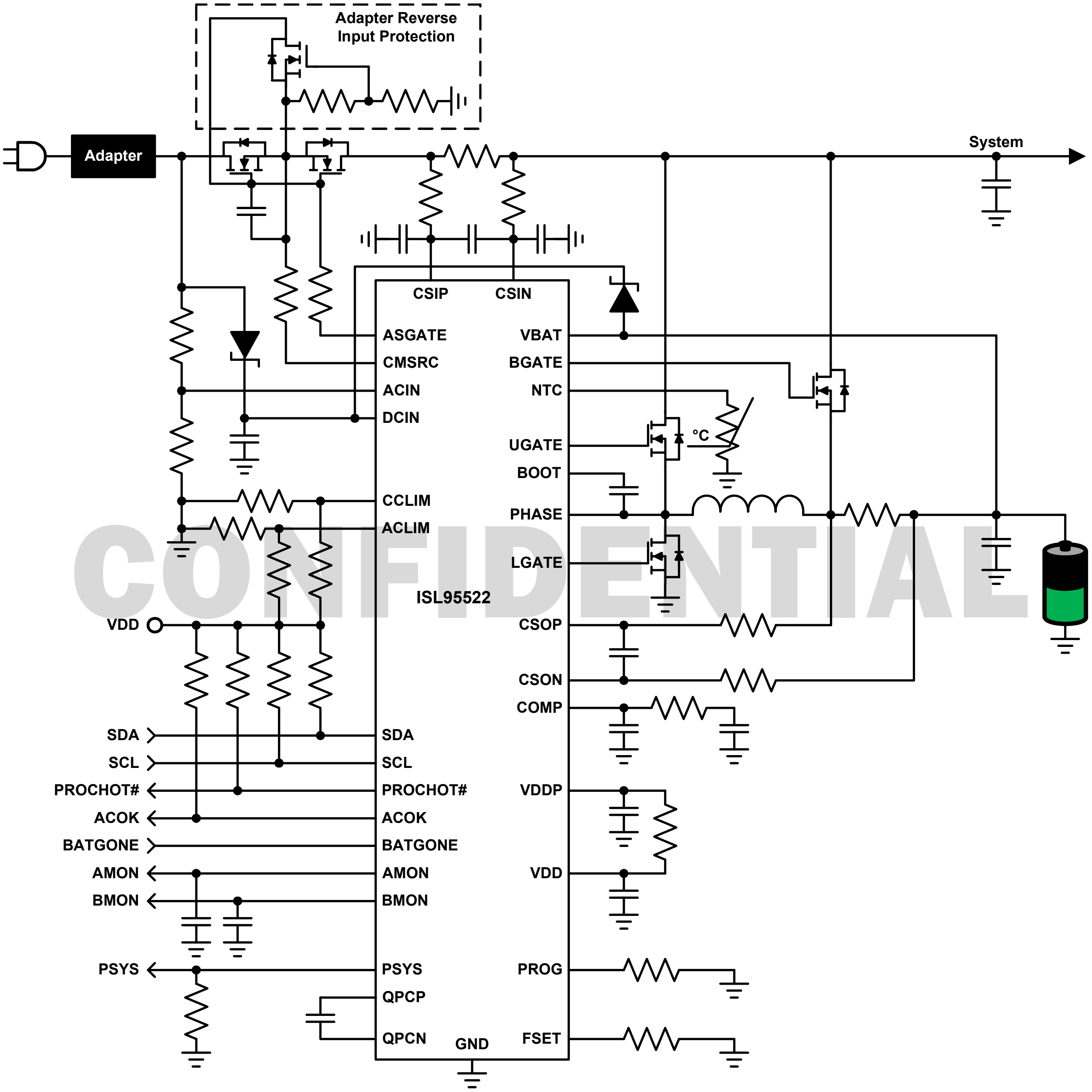


Figure 4. Typical Application Circuit: HPB Charger Configuration with Two NMOS Selectors

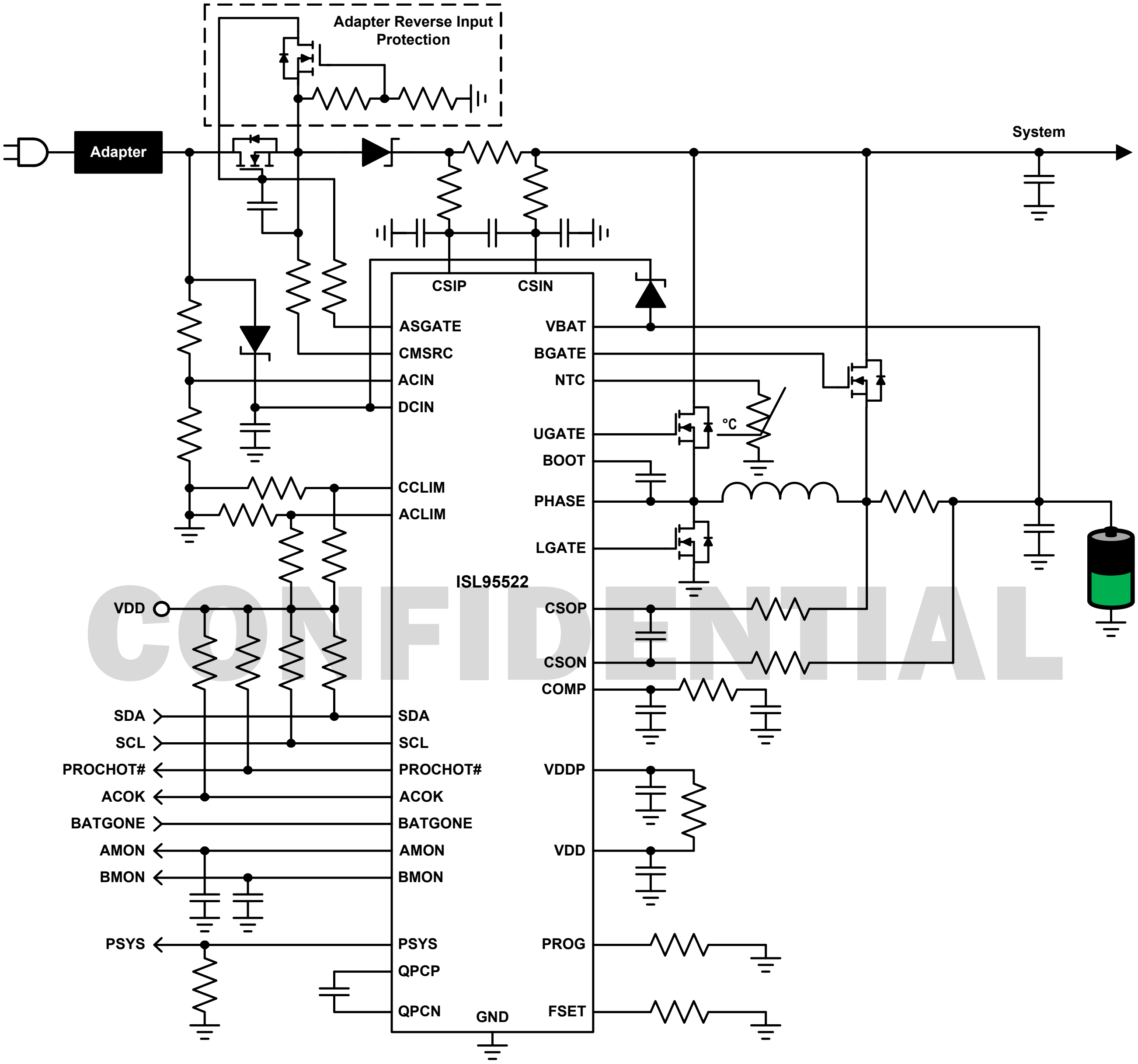


Figure 5. Typical Application Circuit: HPB Charger Configuration with One NMOS Selector and Schottky Diode

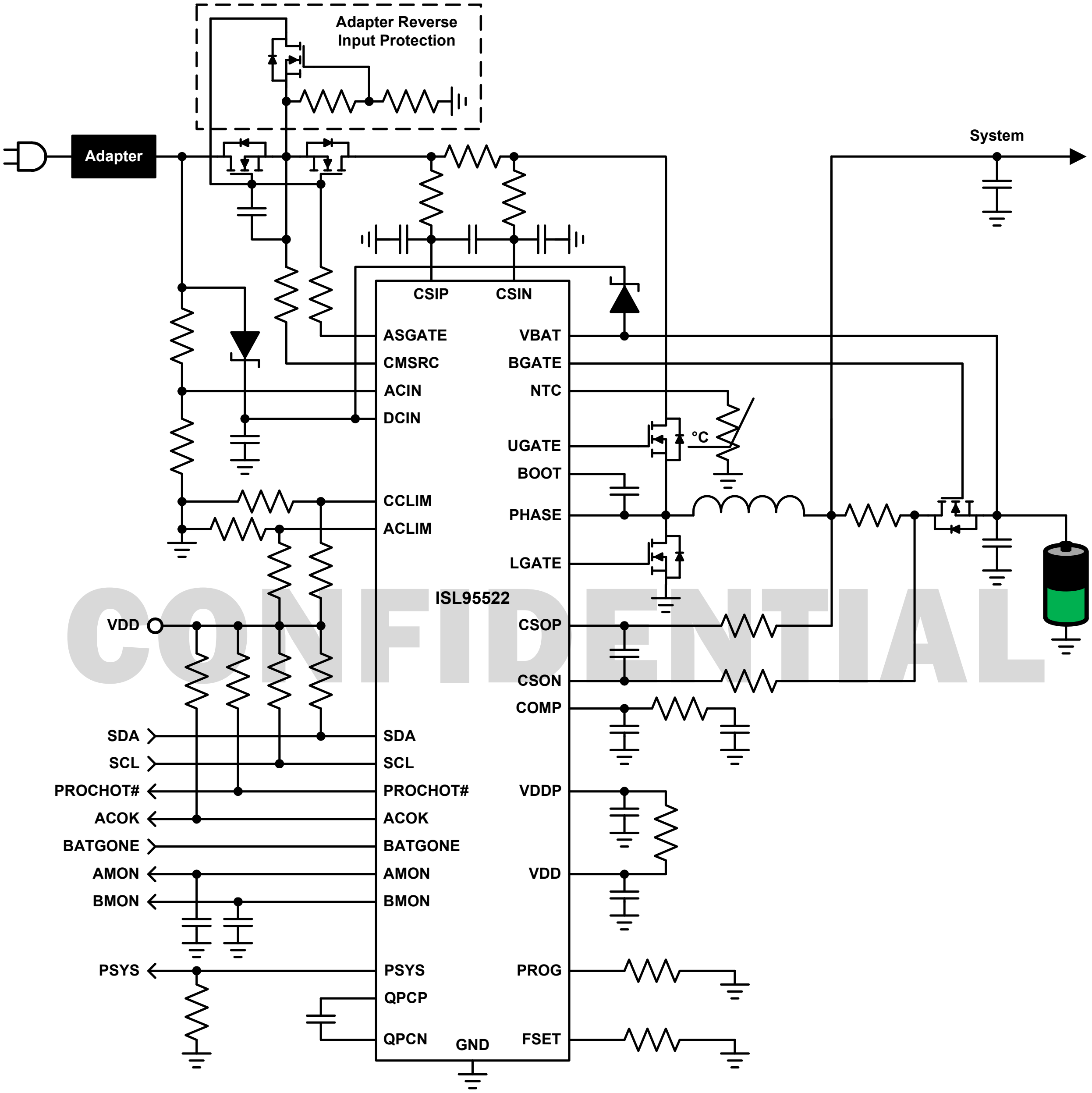


Figure 6. Typical Application Circuit: NVDC Charger Configuration with Two NMOS Selectors

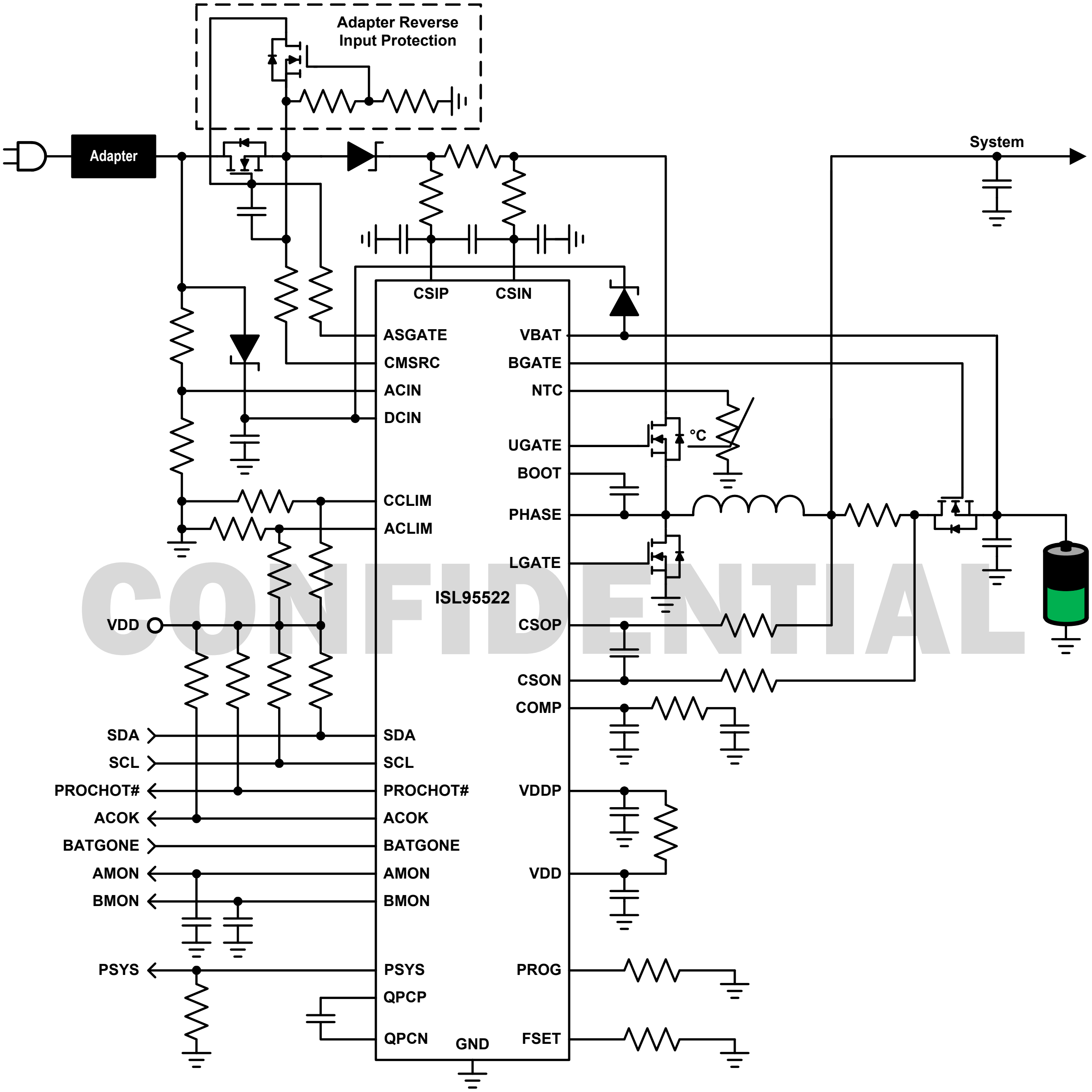


Figure 7. Typical Application Circuit: NVDC Charger Configuration with One NMOS Selector and Schottky Diode

1.3 Ordering Information

Part Number (Notes 2, 3)	Part Marking	Package Description (RoHS Compliant)	Pkg. Dwg. #	Carrier Type (Note 1)	Temp. Range (°C)
ISL95522HRZ	95522H	32 Ld 4x4 QFN	L32.4x4A	Tube	0 to +85
ISL95522HRZ-T				Reel, 6k	
ISL95522IRZ	95522I	32 Ld 4x4 QFN	L32.4x4A	Tube	-40 to +100
ISL95522IRZ-T				Reel, 6k	
ISL95522COMBO-HYBEVZ	HPB Configuration Evaluation Board				
ISL95522COMBONVDCEVZ	NVDC Configuration Evaluation Board				

Notes:

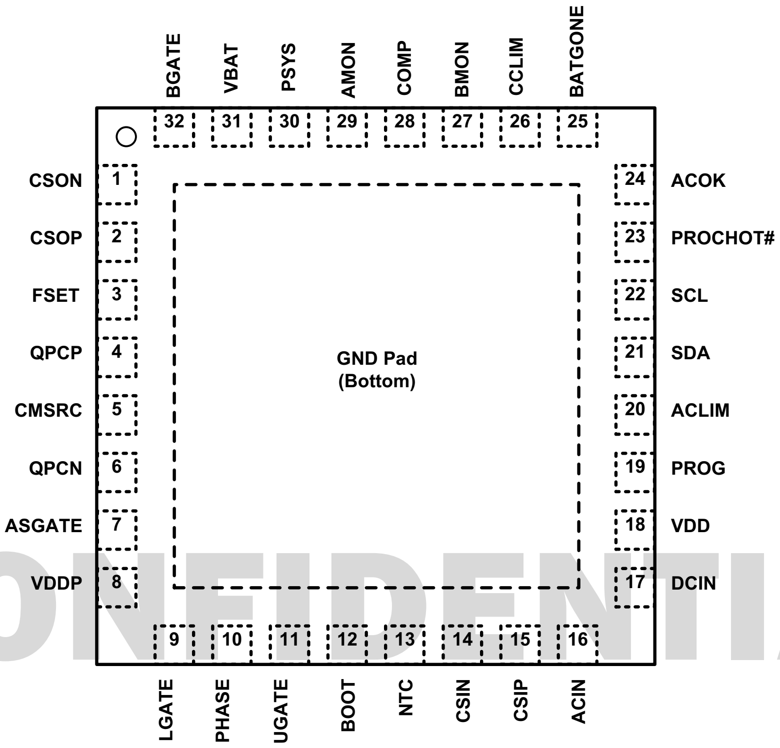
1. See TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
3. For Moisture Sensitivity Level (MSL), see the ISL95522 device page. For more information about MSL, see TB363.

Table 1. Key Differences Between Family of Parts

	ISL95522	ISL95521B	ISL88739
Charger Type	HPB and NVDC combo	HPB and NVDC combo	HPB and NVDC combo
PSYS	Yes	Yes	No
PROCHOT# and NTC	Yes	Yes	Yes
VIN Loop	Yes	No	No

1.4 Pin Configuration

32 Ld 4x4 QFN
Top View



1.5 Pin Descriptions

Pin #	Pin Name	Description
Bottom Pad	GND	Signal common to the IC. Unless otherwise stated, signals are referenced to the GND pin. This pin should also be used as the thermal pad for heat removal.
1	CSON	Battery current sense negative input. Also senses the NVDC charger system voltage.
2	CSOP	Battery current sense positive input.
3	FSET	A resistor from this pin to GND programs the default switching frequency. See Table 20 on page 51 for programming options.
4	QPCP	Internal charge pump positive input. Connect an MLCC capacitor across the QPCP pin and the QPCN pin.
5	CMSRC	Common source node of the two back-to-back ASGATE NFETs.
6	QPCN	Internal charge pump negative input. Connect an MLCC capacitor across the QPCP pin and the QPCN pin.
7	ASGATE	Output of the gate drive for the two back-to-back NFETs.
8	VDDP	Output of the internal 5V output LDO. The ISL95522 uses it as a FET driver power supply. Connect a 2.2µF (10V) MLCC capacitor to GND. The capacitor must have an effective capacitance higher than 0.4µF at 5V and x1.6 effective capacitance at the BOOT pin at 5V.
9	LGATE	Output of the low-side switching FET gate drive. Connect this pin to the gate of the low-side switching FET.
10	PHASE	Current return path for the high-side switching FET gate drive. Connect this pin to the node consisting of the high-side switching FET source, the low-side switching FET drain, and the output inductor.
11	UGATE	Output of the high-side switching FET gate drive. Connect this pin to the gate of the high-side switching FET.

Pin #	Pin Name	Description
12	BOOT	Connect an MLCC capacitor across the BOOT pin and the PHASE pin. The boot capacitor is charged through an internal bootstrap switch connected from the VDDP pin to the BOOT pin, when the PHASE pin drops below VDDP minus the voltage drop across the internal bootstrap switch. Connect a 0.47µF (25V) bootstrap capacitor, which must have an effective capacitance higher than 0.25µF at 5V and x50 effective high-side MOSFET gate capacitance.
13	NTC	10µA current source output. Connect an NTC thermistor network from this pin to GND. If the NTC pin voltage is below 170mV, the ISL95522 pulls PROCHOT# low. In addition to connecting NTC thermistor networks, this NTC pin comparator can be used as a general purpose comparator for the platform.
14	CSIN	Adapter current sense negative input.
15	CSIP	Adapter current sense positive input. Also senses input voltage.
16	ACIN	Adapter voltage sense. The ISL95522 considers the adapter voltage “valid” if the ACIN pin voltage is between 2V and 3.5V. If the ACIN pin voltage exceeds 3.5V, the ISL95522 considers the adapter voltage in overvoltage condition and turns off the ASGATE MOSFETs to isolate the adapter from the system.
17	DCIN	Input of an internal 5V output LDO. Renesas recommends connecting a diode-OR from adapter and battery. The DCIN pin voltage needs to be higher than the VBAT pin voltage for ASGATE to soft-start turn on. Connect a 10Ω DCIN resistor between the DCIN pin and the VADP/VSYS diodes, and connect a 4.7µF (50V) DCIN capacitor to GND. The capacitor must have an effective capacitance higher than 0.4µF at 20V.
18	VDD	5V power supply input for the ISL95522 control circuitry. Connect a 2.2µF (10V) MLCC capacitor to GND. The capacitor must have an effective capacitance higher than 0.4µF at 5V and x1.6 effective capacitance at the BOOT pin at 5V.
19	PROG	A resistor to GND sets the following configurations: • HPB charger or NVDC charger. • Default number of the battery cells in series. • Adapter current sense resistor and battery current sense resistor values. See Table 18 on page 49 for programming options. After POR, pulling the PROG pin to 5V enables Learn mode.
20	ACLIM	The voltage on this pin sets the hardware-based adapter current limit. The lower value of the hardware-set adapter current limit and the SMBus set adapter current limit is the actual limit of the adapter current. The hardware-based adapter current limit also sets the regulated inrush current level for ASGATE MOSFET protection.
21	SDA	SMBus data I/O. Connect to the data line from the host controller or smart battery. Connect a 10kΩ pull-up resistor according to the SMBus specification.
22	SCL	SMBus clock I/O. Connect to the clock line from the host controller or smart battery. Connect a 10kΩ pull-up resistor according to the SMBus specification.
23	PROCHOT#	Open-drain output. Pull low with SMBus programmable debounce time if any of the four conditions occur: • Adapter current reaches PROCHOT_IADP. • Battery discharging current reaches PROCHOT_IDIS. • System bus voltage is below the low system voltage detection threshold (programmable through SMBus). • NTC pin voltage is below 170mV. When asserted, it latches on for a minimum SMBus programmable time before it can be cleared.
24	ACOK	Open-drain output to indicate adapter voltage is ready. Pulled low if the adapter voltage is not ready.
25	BATGONE	Battery presence indicator input pin to the ISL95522. Logic high indicates the battery has been removed. Logic low indicates the battery is present.
26	CCLIM	The voltage on this pin sets the WOCP threshold for the current flowing into the battery.
27	BMON	Battery discharging current monitor. $V_{BMON} = 32 \times (V_{CSON} - V_{CSOP})$. Leave the BMON pin floating if not used.
28	COMP	Error amplifier output. Connect the compensation network externally from COMP to GND.
29	AMON	Adapter current monitor output. $V_{AMON} = 32 \times (V_{CSIP} - V_{CSIN})$. Leave the AMON pin floating if not used.
30	PSYS	System power monitor output. Connect the PSYS pin to GND if not used.
31	VBAT	Current return path for the BGATE gate drive. Also senses battery voltage. Renesas recommends connecting an RC filter at the VBAT pin.
32	BGATE	Output of the gate drive for the NFET connecting the system voltage and the battery. The behavior of the BGATE depends on whether the ISL95522 is in the HPB charger configuration or the NVDC charger configuration.

2. Specifications

2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
CSIP, CSIN, DCIN, CMSRC, QPCN	-0.3	+28	V
VBAT, CSOP, CSON	-0.3	+28	V
ASGATE, BGATE, QPCP	-0.3	+33	V
VDD, VDDP	-0.3	+7	V
CSIP-CSIN, CSOP-CSON	-0.3	+0.3	V
QPCP-QPCN	-0.3	+7	V
UGATE-PHASE	-0.3	+7	V
BOOT Voltage (BOOT)	-0.3	+33	V
BOOT to PHASE Voltage (BOOT-PHASE)	-0.3	+7 (DC)	V
	-0.3	+9 (<10ns)	V
PHASE Voltage (PHASE)	-0.3	+28	V
	-7 (<20ns pulse-width, 10µJ)		V
UGATE Voltage (UGATE)	(PHASE - 0.3) (DC)	BOOT	V
	(PHASE - 5) (<20ns pulse-width, 10µJ)	BOOT	V
LGATE Voltage	-2.5 (<20ns pulse-width, 5µJ)	V_{DDP} + 0.3	V
Open-Drain Outputs, ACOK, PROCHOT#	-0.3	+7	V
All Other Pins	-0.3	(V_{DD} + 0.3)	V
ESD Rating	**Value**		**Unit**
Human Body Model (Tested per JS-001-2017)	2.5		kV
Charged Device Model (Tested per JS-002-2014)	750		V
Latch-Up (Tested per JESD78E; Class 2, Level A)	Class 2, Level A		

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

2.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
32 Ld QFN Package (Notes 4, 5)	41	5

Notes:

4. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with “direct attach” features. See TB379.
5. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature		+150	°C
Maximum Storage Temperature Range	-65	+150	°C
Pb-Free Reflow Profile	see TB493		

2.3 Recommended Operation Conditions

Parameter	Minimum	Maximum	Unit
Ambient Temperature HRZ	0	+85	°C
Ambient Temperature IRZ	-40	+100	°C
Junction Temperature	0	+125	°C

2.4 Electrical Specifications

Operating conditions: V_{DD} = 5V, T_A = 0°C to +85°C or -40°C to +100°C unless otherwise noted. **Boldface limits apply across the operating temperature range, 0°C to +85°C or -40°C to +100°C.**

Parameter	Symbol	Test Conditions	Min (Note 6)	Typ	Max (Note 6)	Unit
Quiescent Current and POR						
Battery Current	$I_{BAT\_BGATE\_OFF}$ NVDC	Adapter present, BGATE off, V_{BAT} = 16.8V, DCIN current does not come from battery, I_BAT = I_VBAT		40	**75**	µA
	$I_{BAT\_BGATE\_ON}$ NVDC	Battery only, BGATE on, V_{BAT} = 16.8V, DCIN current comes from battery, I_BAT = I_PHASE + I_VBAT + I_CSOP + I_CSON + I_DCIN I+ I_CMSRC		130	**190**	µA
	$I_{BAT\_BGATE\_OFF}$ HPB	Adapter present, BGATE off, V_{BAT} = 16.8V, DCIN current does not come from battery, I_BAT = I_PHASE + I_VBAT + I_CSOP + I_CSON + I_CMSRC		43	**75**	µA
	$I_{BAT\_BGATE\_ON}$ HPB	Battery only, BGATE on, V_{BAT} = 16.8V, DCIN current comes from battery, I_BAT = I_PHASE + I_VBAT + I_CSOP + I_CSON + I_DCIN + I_CSIP + I_CSIN + I_CMSRC		130	**190**	µA
Quiescent Current	$I_{DCIN\_STANDBY}$ HPB	VADP = 19.2V, AMON, BMON, PSYS all off		160	**220**	µA
	$I_{DCIN\_NOSW\_1}$ HPB	VADP = 19.2V, no switching, AMON, BMON, PSYS all off		785	**900**	µA
	$I_{DCIN\_NOSW\_2}$ HPB	VADP = 19.2V, no switching, AMON, BMON, PSYS all on		1070	**1250**	µA
	$I_{DCIN\_SW\_H}$ HPB	VADP = 19.2V, charge enabled, AMON, BMON, PSYS all off		1.25	**1.55**	mA
	$I_{DCIN\_SW\_N}$ NVDC	VADP = 19.2V, charge enabled, AMON, BMON, PSYS all off		1.45	**1.75**	mA
VDD Power-On Reset (POR)	POR_{VDD_R}	VDD rising		4.66	**4.75**	V
	POR_{VDD_F}	VDD falling	**4.35**	4.44		mV

Operating conditions: V_{DD} = 5V, T_A = 0°C to +85°C or -40°C to +100°C unless otherwise noted. **Boldface limits apply across the operating temperature range, 0°C to +85°C or -40°C to +100°C. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 6)	Typ	Max (Note 6)	Unit
Charging Voltage Limit						
Maximum Charging Voltage Accuracy	V_{CHG_MAX}	MaxChargeVoltage = 0x41A0H (16.8V) T_A = 0°C to +85°C		16.79		V
			-0.75		**0.75**	%
		MaxChargeVoltage = 0x41A0H (16.8V) T_A = -40°C to +100°C	**-0.85**		**0.85**	%
		MaxChargeVoltage = 0x3140H (12.608V) T_A = 0°C to +85°C		12.6		V
			-0.75		**0.75**	%
		MaxChargeVoltage = 0x3140H (12.608V) T_A = -40°C to +100°C	**-0.85**		**0.85**	%
		MaxChargeVoltage = 0x20D0H (8.4V) T_A = 0°C to +85°C		8.4		V
			-0.75		**0.75**	%
		MaxChargeVoltage = 0x20D0H (8.4V) T_A = -40°C to +100°C	**-0.85**		**0.85**	%
Minimum Charging Voltage Accuracy (NVDC 450mV + MinChargeVoltage register setting)	V_{CHG_MIN}	MinChargeVoltage = 0x2A00H (10.752V) T_A = 0°C to +85°C	**11.1**	11.28	**11.48**	V
		MinChargeVoltage = 0x2A00H (10.752V) T_A = -40°C to +100°C	**11.1**		**11.52**	V
		MinChargeVoltage = 0x2000H (8.192V) T_A = 0°C to +85°C	**8.54**	8.7	**8.9**	V
		MinChargeVoltage = 0x2000H (8.192V) T_A = -40°C to +100°C	**8.54**		**9.3**	V
		MinChargeVoltage = 0x1500H (5.376V) T_A = 0°C to +85°C	**5.72**	5.865	**6.04**	V
		MinChargeVoltage = 0x1500H (5.376V) T_A = -40°C to +100°C	**5.72**		**6.08**	V
Battery Current Limit						
Battery Current Sense Amplifier Input Differential Voltage Range	V_{IBAT_RGE5}	R_{s2} = 5mΩ, charging current (V_{CSOP} - V_{CSON})	**0**		**40.5**	mV
	V_{IBAT_RGE10}	R_{s2} = 10mΩ or R_{s2} = 20mΩ, charging current (V_{CSOP} - V_{CSON})	**0**		**81**	mV
	V_{IBAT_RGED}	Discharging current (V_{CSOP} - V_{CSON})	**-81**		**0**	mV

Operating conditions: V_{DD} = 5V, T_A = 0°C to +85°C or -40°C to +100°C unless otherwise noted. **Boldface limits apply across the operating temperature range, 0°C to +85°C or -40°C to +100°C. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 6)	Typ	Max (Note 6)	Unit
Charging Current Limit R_{s2} = 10mΩ V_{BAT} > 4.5V	I_{CHG_ACC10}	ChargeCurrentLimit = 0x1F20H (7968mA) T_A = 0°C to +85°C		8000		mA
			-2.1	0.4	**3.4**	%
		ChargeCurrentLimit = 0x1F20H (7968mA) T_A = -40°C to +100°C	**-2.2**		**3.5**	%
		ChargeCurrentLimit = 0x0FA0H (4000mA) T_A = 0°C to +85°C		4025		mA
			-2.4	0.6	**3.8**	%
		ChargeCurrentLimit = 0x0FA0H (4000mA) T_A = -40°C to +100°C	**-2.6**		**4**	%
		ChargeCurrentLimit = 0x07E0H (2016mA) T_A = 0°C to +85°C		2030		mA
			-3.6	0.7	**5.4**	%
		ChargeCurrentLimit = 0x07E0H (2016mA) T_A = -40°C to +100°C	**-4.1**		**5.9**	%
		ChargeCurrentLimit = 0x03E0H (992mA) T_A = 0°C to +85°C		1006		mA
			-5	1.4	**7.9**	%
		ChargeCurrentLimit = 0x03E0H (992mA) T_A = -40°C to +100°C	**-6**		**8.9**	%
		ChargeCurrentLimit = 0x0200H (512mA) T_A = 0°C to +85°C		525		mA
			-8.4	2.5	**12.3**	%
		ChargeCurrentLimit = 0x0200H (512mA) T_A = -40°C to +100°C	**-10.4**		**14.3**	%
		ChargeCurrentLimit = 0x0100H (256mA) (not Trickle Charging mode current) T_A = 0°C to +85°C		265		mA
			-19.2	3.5	**24.6**	%
		ChargeCurrentLimit = 0x0100H (256mA) (not Trickle Charging mode current) T_A = -40°C to +100°C	**-23.2**		**28.6**	%

Operating conditions: V_{DD} = 5V, T_A = 0°C to +85°C or -40°C to +100°C unless otherwise noted. **Boldface limits apply across the operating temperature range, 0°C to +85°C or -40°C to +100°C. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 6)	Typ	Max (Note 6)	Unit
Charging Current Limit R_{s2} = 5mΩ V_{BAT} > 4.5V	I_{CHG_ACC5}	ChargeCurrentLimit = 0x1F20H (7968mA) T_A = 0°C to +85°C		8015		mA
			-2.4	0.6	**3.8**	%
		ChargeCurrentLimit = 0x1F20H (7968mA) T_A = -40°C to +100°C	**-2.6**		**4**	%
		ChargeCurrentLimit = 0x0FA0H (4000mA) T_A = 0°C to +85°C		4030		mA
			-3.2	0.8	**4.3**	%
		ChargeCurrentLimit = 0x0FA0H (4000mA) T_A = -40°C to +100°C	**-3.7**		**4.8**	%
		ChargeCurrentLimit = 0x07E0H (2016mA) T_A = 0°C to +85°C		2035		mA
			-5	0.9	**6.3**	%
		ChargeCurrentLimit = 0x07E0H (2016mA) T_A = -40°C to +100°C	**-6**		**7.3**	%
		ChargeCurrentLimit = 0x03E0H (992mA) T_A = 0°C to +85°C		1015		mA
			-8.4	2.3	**11.0**	%
		ChargeCurrentLimit = 0x03E0H (992mA) T_A = -40°C to +100°C	**-10.4**		**13.0**	%
		ChargeCurrentLimit = 0x0200H (512mA) T_A = 0°C to +85°C		535		mA
			-15	4.5	**19.2**	%
		ChargeCurrentLimit = 0x0200H (512mA) T_A = -40°C to +100°C	**-18.9**		**23.2**	%
		ChargeCurrentLimit = 0x0100H (256mA) (not Trickle Charging mode current) T_A = 0°C to +85°C		269		mA
			-34	5.0	**35.0**	%
		ChargeCurrentLimit = 0x0100H (256mA) (not Trickle Charging mode current) T_A = -40°C to +100°C	**-42.0**		**43.0**	%
Trickle Charging Current Limit	$I_{TRKL\_ACC10\_256}$	R_{s2} = 10mΩ, V_{BAT} < MinChargeVoltage T_A = 0°C to +85°C	**210**	265	**315**	mA
		R_{s2} = 10mΩ, V_{BAT} < MinChargeVoltage T_A = -40°C to +100°C	**200**		**320**	mA
	$I_{TRKL\_ACC10\_128}$	R_{s2} = 10mΩ, V_{BAT} < MinChargeVoltage T_A = 0°C to +85°C	**85**	135	**185**	mA
		R_{s2} = 10mΩ, V_{BAT} < MinChargeVoltage T_A = -40°C to +100°C	**75**		**190**	mA
	$I_{TRKL\_ACC5\_256}$	R_{s2} = 5mΩ, V_{BAT} < MinChargeVoltage T_A = 0°C to +85°C	**165**	255	**335**	mA
		R_{s2} = 5mΩ, V_{BAT} < MinChargeVoltage T_A = -40°C to +100°C	**145**		**345**	mA
	$I_{TRKL\_ACC5\_128}$	R_{s2} = 5mΩ, V_{BAT} < MinChargeVoltage T_A = 0°C to +85°C	**32**	120	**213**	mA
		R_{s2} = 5mΩ, V_{BAT} < MinChargeVoltage T_A = -40°C to +100°C	**12**		**220**	mA
V_{BAT} Trickle Charging Threshold	$V_{TRKL\_TH\_R}$	MinChargeVoltage = 4.096V, exit Trickle Charging mode		4.45	**4.6**	V
	$V_{TRKL\_TH\_F}$	MinChargeVoltage = 4.096V, enter Trickle Charging mode	**3.85**	4.05		V

Operating conditions: V_{DD} = 5V, T_A = 0°C to +85°C or -40°C to +100°C unless otherwise noted. **Boldface limits apply across the operating temperature range, 0°C to +85°C or -40°C to +100°C. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 6)	Typ	Max (Note 6)	Unit
Discharging Current PROCHOT# Threshold R_{s2} = 5mΩ	$I_{DIS\_HOT\_TH5}$	DCPROCHOT = 0x2A00H (10752mA) T_A = 0°C to +85°C		10848		mA
			-3.5	0.9	**5.3**	%
		DCPROCHOT = 0x2A00H (10752mA) T_A = -40°C to +100°C	**-3.6**		**5.3**	%
		DCPROCHOT = 0x1500H (5376mA) T_A = 0°C to +85°C		5450		mA
			-6.4	1.4	**9.2**	%
		DCPROCHOT = 0x1500H (5376mA) T_A = -40°C to +100°C	**-6.5**		**9.2**	%
Adapter Current Limit						
Adapter Current Sense Amplifier Input Differential Voltage Range	V_{IADP_RGE}	R_{s1} = 10mΩ or R_{s1} = 20mΩ, adapter current (V_{CSIP} - V_{CSIN})	**0**		**81**	mV
Adapter Current Limit R_{s1} = 10mΩ	I_{ADP_10}	AdapterCurrentLimit = 0x1F20H (8064mA) T_A = 0°C to +85°C		8140		mA
			-0.9	0.9	**2.8**	%
		AdapterCurrentLimit = 0x1F20H (8064mA) T_A = -40°C to +100°C	**-0.9**		**2.9**	%
		AdapterCurrentLimit = 0x1000H (4096mA) T_A = 0°C to +85°C		4150		mA
			-1.1	1.3	**3.7**	%
		AdapterCurrentLimit = 0x1000H (4096mA) T_A = -40°C to +100°C	**-1.1**		**3.9**	%
		AdapterCurrentLimit = 0x0800H (2048mA) T_A = 0°C to +85°C		2085		mA
			-2.3	1.8	**5.7**	%
		AdapterCurrentLimit = 0x0800H (2048mA) T_A = -40°C to +100°C	**-2.3**		**6.2**	%
		AdapterCurrentLimit = 0x0400H (1024mA) T_A = 0°C to +85°C		1060		mA
			-3.5	3.5	**10.5**	%
		AdapterCurrentLimit = 0x0400H (1024mA) T_A = -40°C to +100°C	**-3.5**		**11.5**	%
		AdapterCurrentLimit = 0x0200H (512mA) T_A = 0°C to +85°C		550		mA
			-5.0	7.4	**20.0**	%
		AdapterCurrentLimit = 0x0200H (512mA) T_A = -40°C to +100°C	**-5**		**22**	%
		AdapterCurrentLimit = 0x0100H (256mA) T_A = 0°C to +85°C		295		mA
			-11.0	15.2	**42.0**	%
		AdapterCurrentLimit = 0x0100H (256mA) T_A = -40°C to +100°C	**-11.0**		**48.0**	%
Adapter Current PROCHOT# Threshold R_{s1} = 10mΩ	$I_{ADP\_HOT\_TH10}$	ACPROCHOT = 0x1500H (5376mA)		5389		mA
			-3.50	0.25	**4**	%
		ACPROCHOT = 0x0A80H (2688mA)		2728		mA
			-7.0	1.5	**10.0**	%

Operating conditions: V_{DD} = 5V, T_A = 0°C to +85°C or -40°C to +100°C unless otherwise noted. **Boldface limits apply across the operating temperature range, 0°C to +85°C or -40°C to +100°C. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 6)	Typ	Max (Note 6)	Unit
Monitor						
AMON Accuracy V_{AMON} = 32x (V_{CSIP} - V_{CSIN}) R_{s1} = 10mΩ	V_{AMON}	V_{CSIP} - V_{CSIN} = 80mV T_A = 0°C to +85°C		2544		mV
			-2.5	-0.6	**1.3**	%
		V_{CSIP} - V_{CSIN} = 80mV T_A = -40°C to +100°C	**-2.7**		**1.5**	%
		V_{CSIP} - V_{CSIN} = 40mV T_A = 0°C to +85°C		1269		mV
			-3.50	-0.85	**1.80**	%
		V_{CSIP} - V_{CSIN} = 40mV T_A = -40°C to +100°C	**-3.9**		**2.2**	%
		V_{CSIP} - V_{CSIN} = 20mV T_A = 0°C to +85°C		632		mV
			-6.00	-1.25	**3.50**	%
		V_{CSIP} - V_{CSIN} = 20mV T_A = -40°C to +100°C	**-6.8**		**4.3**	%
		V_{CSIP} - V_{CSIN} = 10mV T_A = 0°C to +85°C		313		mV
			-10.0	-2.2	**6.6**	%
		V_{CSIP} - V_{CSIN} = 10mV T_A = -40°C to +100°C	**-11.6**		**8.2**	%
		V_{CSIP} - V_{CSIN} = 5mV T_A = 0°C to +85°C		154		mV
			-19.50	-3.75	**12.50**	%
		V_{CSIP} - V_{CSIN} = 5mV T_A = -40°C to +100°C	**-22.5**		**15.5**	%
AMON Current Sourcing Capability	$I_{AMON\_MAX\_SR}$	T_A = 0°C to +85°C	**245**	515	**800**	µA
		T_A = -40°C to +100°C	**195**		**850**	µA
AMON Current Sinking Capability	$I_{AMON\_MAX\_SK}$		**12**	22	**32**	µA
BMON Accuracy V_{BMON} = 32 x (V_{CSON} - V_{CSOP}) R_{s2} = 10mΩ	V_{BMON}	V_{CSON} - V_{CSOP} = 80mV T_A = 0°C to +85°C		2562		mV
			-3.70	0.08	**3.70**	%
		V_{CSON} - V_{CSOP} = 80mV T_A = -40°C to +100°C	**-3.70**		**4.10**	%
		V_{CSON} - V_{CSOP} = 40mV T_A = 0°C to +85°C		1284		mV
			-4.2	0.3	**4.7**	%
		V_{CSON} - V_{CSOP} = 40mV T_A = -40°C to +100°C	**-4.2**		**5.1**	%
		V_{CSON} - V_{CSOP} = 20mV T_A = 0°C to +85°C		645		mV
			-5.70	0.75	**7.40**	%
		V_{CSON} - V_{CSOP} = 20mV T_A = -40°C to +100°C	**-5.70**		**7.9**	%
		V_{CSON} - V_{CSOP} = 10mV T_A = 0°C to +85°C		325		mV
			-7.5	1.7	**11.5**	%
		V_{CSON} - V_{CSOP} = 10mV T_A = -40°C to +100°C	**-7.5**		**12.5**	%
BMON Current Sourcing Capability	$I_{BMON\_MAX\_SR}$	T_A = 0°C to +85°C	**120**	285	**460**	µA
		T_A = -40°C to +100°C	**90**		**490**	µA
BMON Current Sinking Capability	$I_{BMON\_MAX\_SK}$		**5.5**	11.4	**17.5**	µA

Operating conditions: V_{DD} = 5V, T_A = 0°C to +85°C or -40°C to +100°C unless otherwise noted. **Boldface limits apply across the operating temperature range, 0°C to +85°C or -40°C to +100°C. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 6)	Typ	Max (Note 6)	Unit
PSYS Output Current R_{s1} = 10mΩ R_{s2} = 10mΩ PSYS Current Gain = 1.12µA/W	I_{PSYS}	V_{CSIP} = 19V, V_{CSIP} - V_{CSIN} = 80mV, V_{BAT} = 12V, V_{CSOP} - V_{CSON} = 0mV T_A = 0°C to +85°C		170		µA
			-8.8	-0.1	**8.6**	%
		V_{CSIP} = 19V, V_{CSIP} - V_{CSIN} = 80mV, V_{BAT} = 12V, V_{CSOP} - V_{CSON} = 0mV T_A = -40°C to +100°C	**-11.1**		**8.6**	%
		V_{CSIP} = 19V, V_{CSIP} - V_{CSIN} = 80mV, V_{BAT} = 12V, V_{CSOP} - V_{CSON} = 20mV T_A = 0°C to +85°C		143.4		µA
			-8.6	0	**8.6**	%
		V_{CSIP} = 19V, V_{CSIP} - V_{CSIN} = 80mV, V_{BAT} = 12V, V_{CSOP} - V_{CSON} = 20mV T_A = -40°C to +100°C	**-10**		**8.6**	%
		V_{CSIP} = 19V, V_{CSIP} - V_{CSIN} = 80mV, V_{BAT} = 12V, V_{CSOP} - V_{CSON} = -20mV T_A = 0°C to +85°C		195.7		µA
			-8.5	-0.7	**7.1**	%
		V_{CSIP} = 19V, V_{CSIP} - V_{CSIN} = 80mV, V_{BAT} = 12V, V_{CSOP} - V_{CSON} = -20mV T_A = -40°C to +100°C	**-13.3**		**7.1**	%
		V_{CSIP} = 0V, V_{CSIP} - V_{CSIN} = 0mV, V_{BAT} = 12V, V_{CSOP} - V_{CSON} = -20mV T_A = 0°C to +85°C		26.4		µA
			-12.8	-1.8	**9.2**	%
		V_{CSIP} = 0V, V_{CSIP} - V_{CSIN} = 0mV, V_{BAT} = 12V, V_{CSOP} - V_{CSON} = -20mV T_A = -40°C to +100°C	**−13.2**		**9.2**	%
Maximum PSYS Output Voltage	V_{PSYS_MAX}	I_{PSYS} = 200µA		2.25		V
NTC Source Current	I_{NTC}	NTC = 1V	**9.71**	10.08	**10.44**	µA
NTC_PROCHOT# Trip Threshold	V_{NTC_TH}	V_{NTC} falling T_A = 0°C to +85°C	**159**	169	**180**	mV
		V_{NTC} falling T_A = -40°C to +100°C	**159**		**181**	mV
NTC_PROCHOT# Hysteresis	V_{NTC_HYS}	T_A = 0°C to +85°C	**18**	27	**36**	mV
		T_A = -40°C to +100°C	**18**		**37**	mV
ACIN/ACOK Comparator						
ACIN Threshold Rising	$V_{ACIN\_TH\_R}$	V_{ACIN} rising T_A = 0°C to +85°C		2.054	**2.083**	V
		V_{ACIN} rising T_A = -40°C to +100°C			**2.088**	V
ACIN Threshold Falling	$V_{ACIN\_TH\_F}$	V_{ACIN} falling T_A = 0°C to +85°C	**2.01**	2.038		V
		V_{ACIN} falling T_A = -40°C to +100°C	**2.005**			V
ACIN OVP Rising	$V_{ACIN\_OVP\_TH\_R}$	V_{ACIN} rising T_A = 0°C to +85°C		3.52	**3.72**	V
		V_{ACIN} rising T_A = -40°C to +100°C			**3.725**	V

Operating conditions: V_{DD} = 5V, T_A = 0°C to +85°C or -40°C to +100°C unless otherwise noted. **Boldface limits apply across the operating temperature range, 0°C to +85°C or -40°C to +100°C. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 6)	Typ	Max (Note 6)	Unit
ACIN OVP Falling	$V_{ACIN\_OVP\_TH\_F}$	V_{ACIN} falling T_A = 0°C to +85°C	**3.30**	3.45		V
		V_{ACIN} falling T_A = -40°C to +100°C	**3.295**			V
ACIN Input Leakage Current	I_{ACIN_LEAK}		**-1**		**1**	µA
ACOK Input Leakage Current	I_{ACOK_LEAK}		**-1**		**1**	µA
ACOK Output Low Current	I_{ACOK}	V_{ACOK} = 0.3V		230		µA
ACLIM, CCLIM						
ACLIM Current Limit		V_{ACLIM} = 2.56V, R_{s1} = 10mΩ T_A = 0°C to +85°C	**7950**	8055	**8155**	mA
		V_{ACLIM} = 2.56V, R_{s1} = 10mΩ T_A = -40°C to +100°C	**7950**		**8165**	mA
		V_{ACLIM} = 1.92V, R_{s1} = 10mΩ T_A = 0°C to +85°C	**5960**	6050	**6140**	mA
		V_{ACLIM} = 1.92V, R_{s1} = 10mΩ T_A = -40°C to +100°C	**5960**		**6150**	mA
		V_{ACLIM} = 1.28V, R_{s1} = 10mΩ T_A = 0°C to +85°C	**3965**	4040	**4115**	mA
		V_{ACLIM} = 1.28V, R_{s1} = 10mΩ T_A = -40°C to +100°C	**3965**		**4125**	mA

Operating conditions: V_{DD} = 5V, T_A = 0°C to +85°C or -40°C to +100°C unless otherwise noted. **Boldface limits apply across the operating temperature range, 0°C to +85°C or -40°C to +100°C. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 6)	Typ	Max (Note 6)	Unit
CCLIM Current Limit		V_{CCLIM} = 2.56V, R_{s1} = 10mΩ, R_{s2} = 5mΩ T_A = 0°C to +85°C	**7865**	8080	**8275**	mA
		V_{CCLIM} = 2.56V, R_{s1} = 10mΩ, R_{s2} = 5mΩ T_A = -40°C to +100°C	**7845**		**8295**	mA
		V_{CCLIM} = 1.92V, R_{s1} = 10mΩ, R_{s2} = 5mΩ T_A = 0°C to +85°C	**5895**	6070	**6225**	mA
		V_{CCLIM} = 1.92V, R_{s1} = 10mΩ, R_{s2} = 5mΩ T_A = -40°C to +100°C	**5885**		**6235**	mA
		V_{CCLIM} = 1.28V, R_{s1} = 10mΩ, R_{s2} = 5mΩ T_A = 0°C to +85°C	**3925**	4060	**4180**	mA
		V_{CCLIM} = 1.28V, R_{s1} = 10mΩ, R_{s2} = 5mΩ T_A = -40°C to +100°C	**3915**		**4190**	mA
		V_{CCLIM} = 2.56V, R_{s1} = 10mΩ, R_{s2} = 10mΩ T_A = 0°C to +85°C	**7845**	8050	**8235**	mA
		V_{CCLIM} = 2.56V, R_{s1} = 10mΩ, R_{s2} = 10mΩ T_A = -40°C to +100°C	**7835**		**8255**	mA
		V_{CCLIM} = 1.92V, R_{s1} = 10mΩ, R_{s2} = 10mΩ T_A = 0°C to +85°C	**5890**	6040	**6180**	mA
		V_{CCLIM} = 1.92V, R_{s1} = 10mΩ, R_{s2} = 10mΩ T_A = -40°C to +100°C	**5885**		**6190**	mA
		V_{CCLIM} = 1.28V, R_{s1} = 10mΩ, R_{s2} = 10mΩ T_A = 0°C to +85°C	**3925**	4030	**4130**	mA
		V_{CCLIM} = 1.28V, R_{s1} = 10mΩ, R_{s2} = 10mΩ T_A = -40°C to +100°C	**3920**		**4140**	mA
		V_{CCLIM} = 2.56V, R_{s1} = 20mΩ, R_{s2} = 20mΩ T_A = 0°C to +85°C	**3925**	4025	**4125**	mA
		V_{CCLIM} = 2.56V, R_{s1} = 20mΩ, R_{s2} = 20mΩ T_A = -40°C to +100°C	**3920**		**4130**	mA
		V_{CCLIM} = 1.92V, R_{s1} = 20mΩ, R_{s2} = 20mΩ T_A = 0°C to +85°C	**2940**	3020	**3095**	mA
		V_{CCLIM} = 1.92V, R_{s1} = 20mΩ, R_{s2} = 20mΩ T_A = -40°C to +100°C	**2935**		**3100**	mA
		V_{CCLIM} = 1.28V, R_{s1} = 20mΩ, R_{s2} = 20mΩ T_A = 0°C to +85°C	**1960**	2015	**2075**	mA
		V_{CCLIM} = 1.28V, R_{s1} = 20mΩ, R_{s2} = 20mΩ T_A = -40°C to +100°C	**1955**		**2080**	mA
PROCHOT#						
PROCHOT# Leakage Current	$I_{PROCHOT\#\_LEAK}$		**-1**		**1**	µA
PROCHOT# Output Low Current	$I_{PROCHOT\#}$	$V_{PROCHOT\#}$ = 0.3V		42		mA

Operating conditions: V_{DD} = 5V, T_A = 0°C to +85°C or -40°C to +100°C unless otherwise noted. **Boldface limits apply across the operating temperature range, 0°C to +85°C or -40°C to +100°C. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 6)	Typ	Max (Note 6)	Unit
Low VSYS PROCHOT# Trip Threshold	$V_{LOW\_VSYS\_HOT}$	Control1 register Bit<9:8> = 00 T_A = 0°C to +85°C	**5.5**	5.64	**5.78**	V
		Control1 register Bit<9:8> = 00 T_A = -40°C to +100°C	**5.49**		**5.785**	V
		Control1 register Bit<9:8> = 01 T_A = 0°C to +85°C	**5.99**	6.13	**6.27**	V
		Control1 register Bit<9:8> = 01 T_A = -40°C to +100°C	**5.98**		**6.275**	V
		Control1 register Bit<9:8> = 10 T_A = 0°C to +85°C	**6.46**	6.61	**6.75**	V
		Control1 register Bit<9:8> = 10 T_A = -40°C to +100°C	**6.45**		**6.755**	V
		Control1 register Bit<9:8> = 11 T_A = 0°C to +85°C	**6.93**	7.08	**7.23**	V
		Control1 register Bit<9:8> = 11 T_A = -40°C to +100°C	**6.92**		**7.235**	V
PROCHOT# Debounce Time		PROCHOT# debounce register Bit<1:0> = 01		102		µs
		PROCHOT# debounce register Bit<1:0> = 10		510		µs
PROCHOT# Duration Time		PROCHOT# duration register Bit<2:0> = 010		15.3		ms
		PROCHOT# duration register Bit<2:0> = 101		1.02		ms
BATGONE Threshold						
BATGONE Threshold Rising	$V_{BATGONE\_TH\_R}$	$V_{BATGONE}$ rising (battery removal)		2.58	**2.75**	V
BATGONE Threshold Falling	$V_{BATGONE\_TH\_F}$	$V_{BATGONE}$ falling (battery insertion)	**1.80**	2.12		V
LDO						
Output Voltage		V_{DCIN} = 6V to 25V, I_VDDP = 1mA T_A = 0°C to +85°C	**4.80**	5.24	**5.75**	V
		V_{DCIN} = 6V to 25V, I_VDDP = 1mA T_A = -40°C to +100°C	**4.75**		**5.80**	V
		V_{DCIN} = 6V, I_VDDP = 30mA T_A = 0°C to +85°C	**4.65**	5.12	**5.65**	V
		V_{DCIN} = 6V, I_VDDP = 30mA T_A = -40°C to +100°C	**4.55**		**5.65**	V
		V_{DCIN} = 25V, I_VDDP = 30mA T_A = 0°C to +85°C	**4.75**	5.22	**5.70**	V
		V_{DCIN} = 25V, I_VDDP = 30mA T_A = -40°C to +100°C	**4.70**		**5.75**	V
Gate Driver						
UGATE Pull-up Resistance (Note 7)	R_{UGPU}	200mA source current		1.0	**1.5**	Ω
UGATE Source Current	I_{UGSRC}	UGATE - PHASE = 2.5V		2.0		A
UGATE Sink Resistance (Note 7)	R_{UGPD}	250mA sink current		1.0	**1.5**	Ω
UGATE Sink Current	I_{UGSNK}	UGATE - PHASE = 2.5V		2.0		A

Operating conditions: V_{DD} = 5V, T_A = 0°C to +85°C or -40°C to +100°C unless otherwise noted. **Boldface limits apply across the operating temperature range, 0°C to +85°C or -40°C to +100°C. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 6)	Typ	Max (Note 6)	Unit
LGATE Pull-up Resistance (Note 7)	R_{LGPU}	250mA source current		1.0	**1.5**	Ω
LGATE Source Current	I_{LGSRC}	LGATE - GND = 2.5V		2.0		A
LGATE Sink Resistance (Note 7)	R_{LGPD}	250mA sink current		0.5	**0.9**	Ω
LGATE Sink Current	I_{LGSNK}	LGATE - GND = 2.5V		4.0		A
UGATE to LGATE Dead Time	t_{UGFLGR}	UGATE falling to LGATE rising, no load		17		ns
LGATE to UGATE Dead Time	t_{LGFUGR}	LGATE falling to UGATE rising, no load		29		ns
ASGATE Pull-Up Resistance	R_{ASGPU}	1mA source current		500		Ω
ASGATE Sink Resistance	R_{ASGPD}	1mA sink current		1300		Ω
BGATE Pull-Up Resistance	R_{BGPU}	1mA source current		500		Ω
BGATE Sink Resistance	R_{BGPD}	1mA sink current		1300		Ω
Bootstrap Switch						
ON-Resistance	R_F			20		Ω
Reverse Leakage	I_R	V_R = 25V		0.2		µA
Amplifiers						
Adapter Current Sense Amplifier Input Offset	V_{ACSNS_OFFSET}			0.4		mV
Battery Charging Current Sense Amplifier Input Offset	$V_{ICHGSNS\_OFFSET}$			0.4		mV
Battery Discharging Current Sense Amplifier Input Offset	$V_{IDISSNS\_OFFSET}$			0.4		mV
Error Amplifier DC Gain	A_{V0_EA}			80		dB
Error Amp Gain-Bandwidth Product	GBW_EA	C_L = 20pF		5		MHz
COMP Lower Clamp	$V_{COMP\_L\_CLP}$			1.24	**1.40**	V
COMP Upper Clamp	$V_{COMP\_U\_CLP}$		**4.90**	4.99		V
Over-Temperature Protection						
Over-Temperature Threshold	T_{OTP_R}	Temperature rising		155		°C
	T_{OTP_F}	Temperature falling		128		°C
SMBus						
SDA/SCL Input Low Voltage					**0.8**	V
SDA/SCL Input High Voltage			**2**			V
SDA/SCL Input Bias Current		SDA, SCL = 0V, 5V	**-1**		**1**	µA
SDA, Output Sink Current (Note 8)		SDA = 0.4V		19		mA
SMBus Frequency	f_{SMB}	(Note 8)	**10**		**400**	kHz
Bus Free Time	t_{BUF}	100kHz, (Note 8)	**4.7**			µs
		400kHz, (Note 8)	**1.3**			µs
Start Condition Hold Time from SCL	t_{HD_STA}	100kHz, (Note 8)	**4**			µs
		400kHz, (Note 8)	**0.6**			µs
Start Condition Setup Time from SCL	t_{SU_STA}	100kHz, (Note 8)	**4.7**			µs
		400kHz, (Note 8)	**0.6**			µs

Operating conditions: V_{DD} = 5V, T_A = 0°C to +85°C or -40°C to +100°C unless otherwise noted. **Boldface limits apply across the operating temperature range, 0°C to +85°C or -40°C to +100°C. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 6)	Typ	Max (Note 6)	Unit
Stop Condition Set-Up Time from SCL	t_{HD_STO}	100kHz, (Note 8)	**4**			μs
		400kHz, (Note 8)	**0.6**			μs
SDA Hold Time from SCL	t_{HD_DAT}	100kHz, (Note 8)	**300**			ns
		400kHz, (Note 8)	**300**			ns
SDA Set-Up Time from SCL	t_{SU_DAT}	100kHz, (Note 8)	**250**			ns
		400kHz, (Note 8)	**100**			ns
SCL Low Period	t_{LOW}	100kHz, (Note 8)	**4.7**			μs
		400kHz, (Note 8)	**1.3**			μs
SCL High Period	t_{HIGH}	100kHz, (Note 8)	**4**			μs
		400kHz, (Note 8)	**0.6**			μs
SDA/SCL Rise Time	t_{RISE}	100kHz, 400pF, maximum load, (Note 8)			**1000**	ns
		400kHz, 400pF, maximum load, (Note 8)			**300**	ns
SDA/SCL Fall Time	t_{FALL}	100kHz, 400pF, maximum load, (Note 8)			**300**	ns
		400kHz, 400pF, maximum load, (Note 8)			**300**	ns
SMBus Inactivity Time-Out (Note 8)		Maximum period without a SMBus write to MaxChargeVoltage or ChargeCurrent register		175		s

Notes:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits are established by characterization and are not production tested.
7. Limits are established by characterization and are not production tested.
8. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.

2.5 Gate Driver Timing Diagram

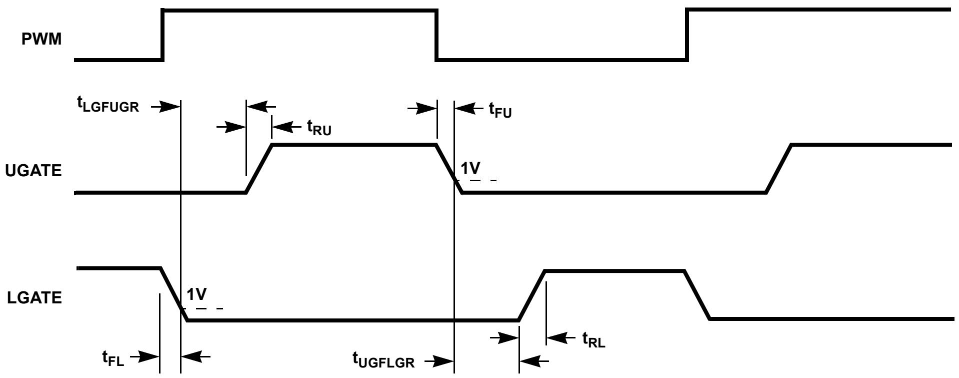


Figure 8. Gate Driver Timing Diagram

3. Typical Performance

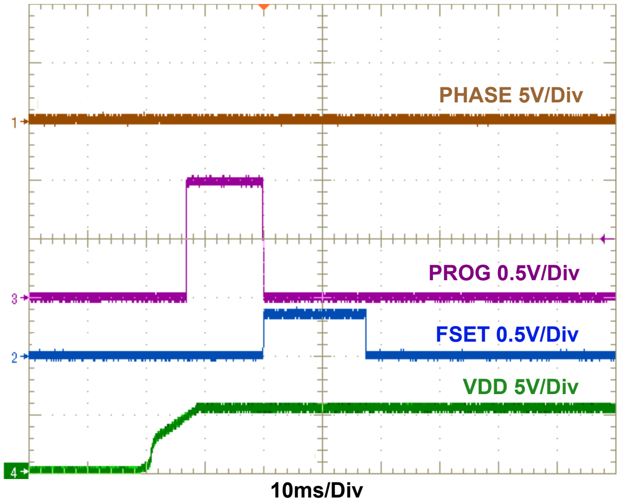


Figure 9. Power-Up, Read Prog, and FSET Resistors

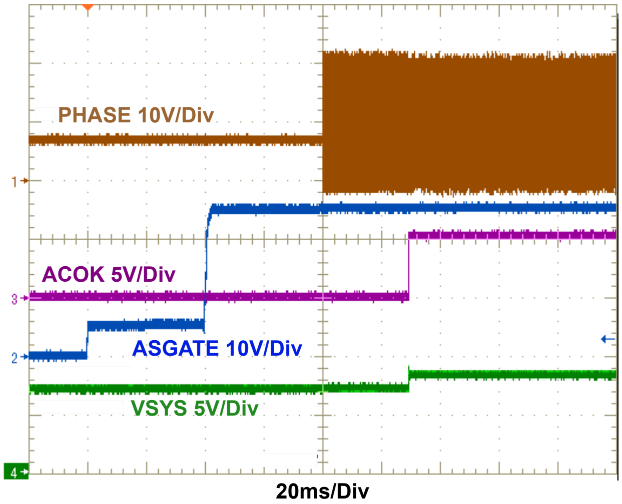


Figure 10. NVDC: Adapter Insertion Start-Up Sequence

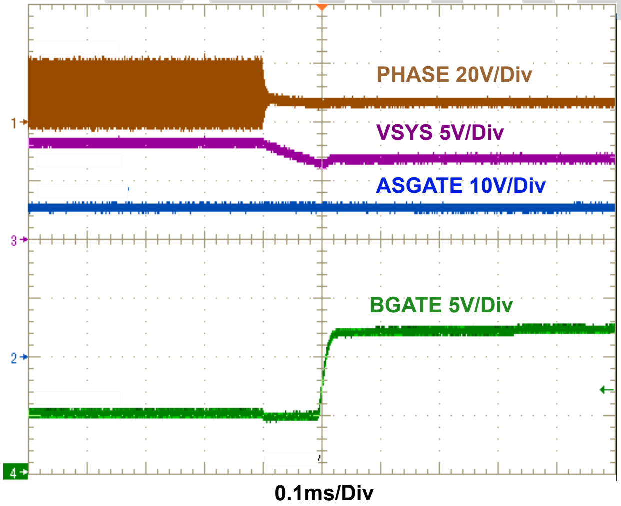


Figure 11. NVDC: Enter Learn Mode

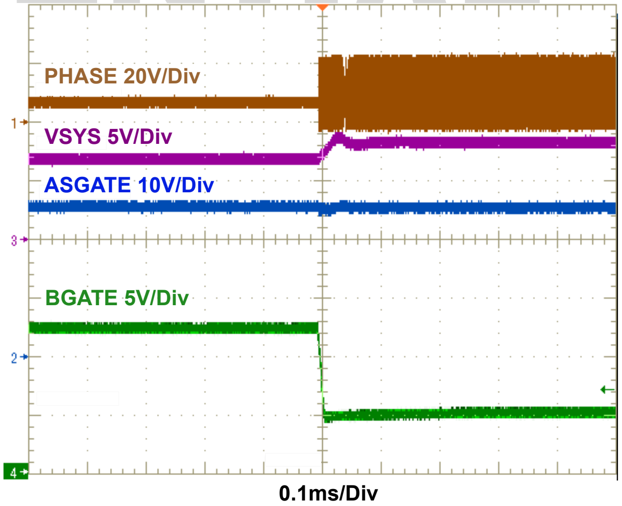


Figure 12. NVDC: Exit Learn Mode

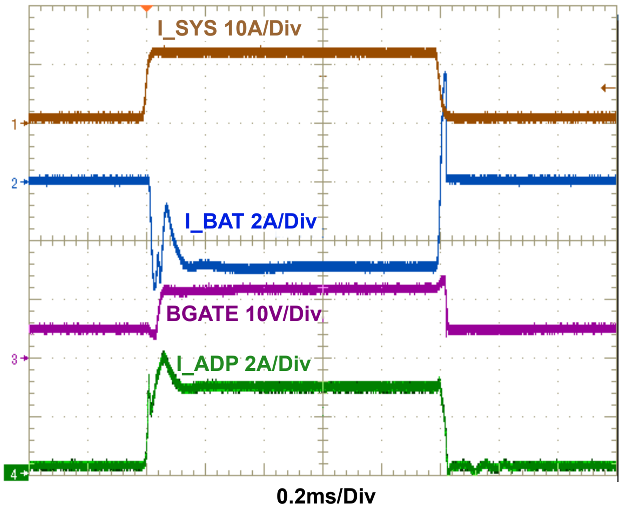


Figure 13. NVDC: System Voltage Regulation Loop and Turbo Mode Transient. VADP = 20V, AdapterCurrentLimit1 = 3.072A, V_{BAT} = 7V, MaxChargeVoltage = 8.192V, 1A to 12A System Load Step

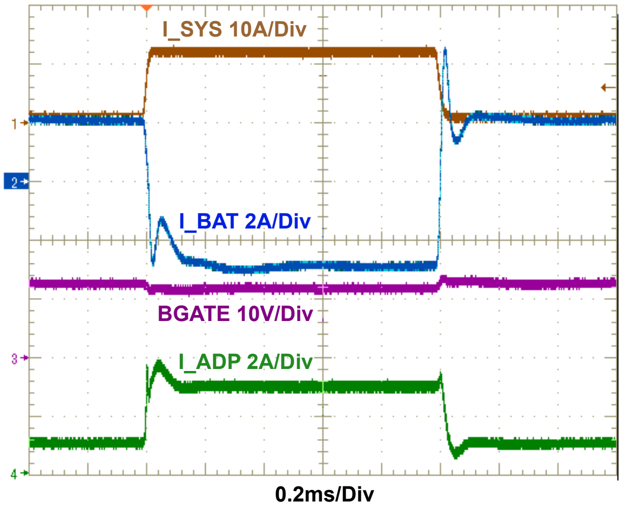


Figure 14. NVDC: Charging Current Limit Loop and Turbo Mode Transition. VADP = 20V, AdapterCurrentLimit1 = 3.072A, V_{BAT} = 7V, MaxChargeVoltage = 8.192V, ChargeCurrent = 2.016A, 1A to 12A System Load Step

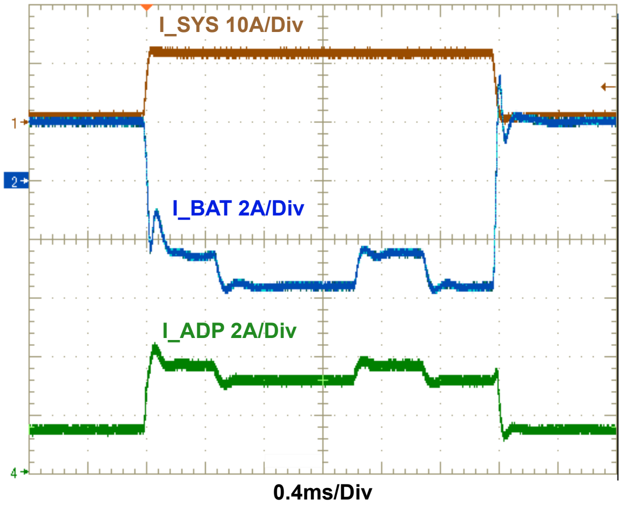


Figure 15. Two Level Adapter Current Limit. VADP = 20V, AdapterCurrentLimit1 = 2.56A, AdapterCurrentLimit2 = 3.072A, T2 = 500µs, T1 = 1ms, V_{BAT} = 7V, MaxChargeVoltage = 8.192V, ChargeCurrent = 2.016A, 1A to 12A System Load Step

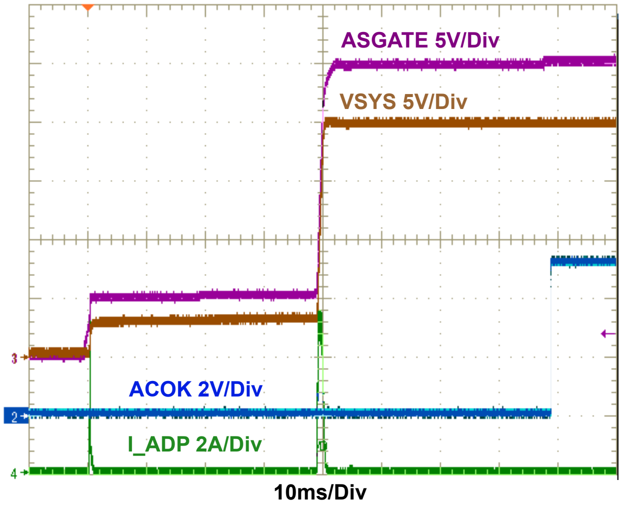


Figure 16. HPB: Adapter Insertion ASGATE Inrush Current Control. No Battery, VADP = 20V, 330µF System Rail Capacitance

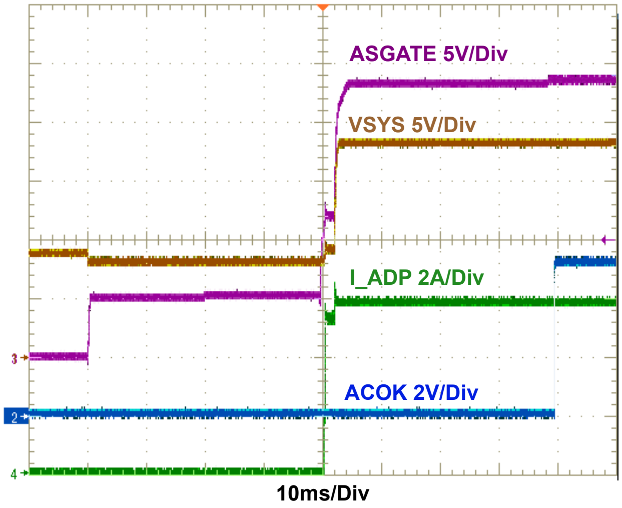


Figure 17. HPB: Adapter Insertion. V_{BAT} = 10V, VADP = 20V, ACLIM Setting = 5A, System Load = 6A

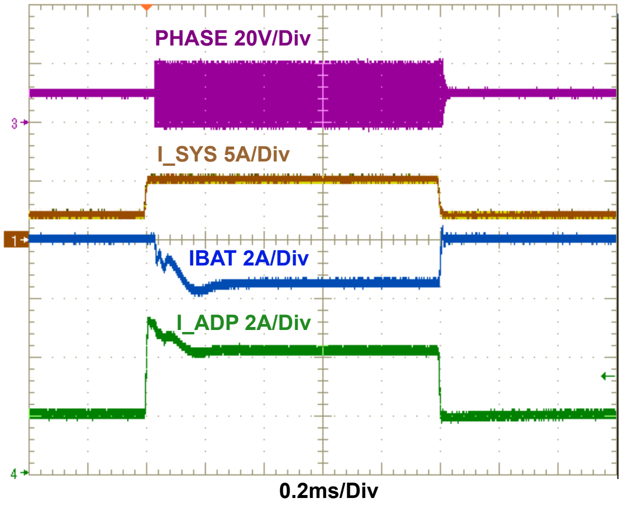


Figure 18. HPB: Charge Disabled, Enter Turbo Mode. VADP = 20V, V_{BAT} = 10V, AdapterCurrentLimit1 = 4.096A, 2A to 5A Load Step

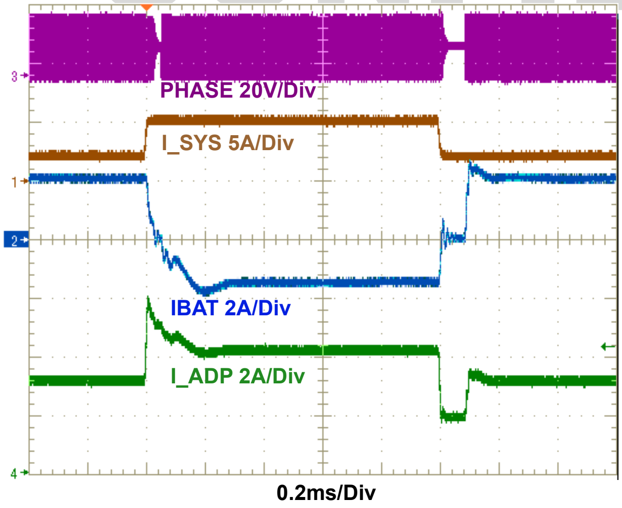


Figure 19. HPB: Charge Enabled, Enter Turbo Mode. VADP = 20V, V_{BAT} = 10V, AdapterCurrentLimit1 = 4.096A, ChargeCurrent = 2.016A, 2A to 5A Load Step

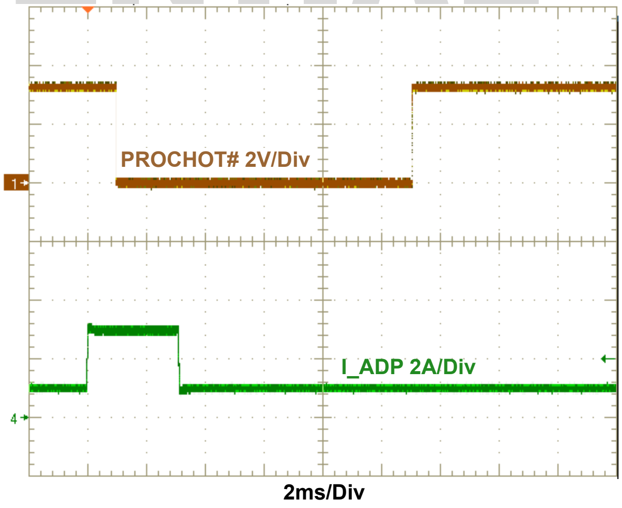


Figure 20. ACPROCHOT# Assertion. ACPROCHOT = 2.048A, PROCHOTDebounce = 1ms, PROCHOTDuration = 10ms

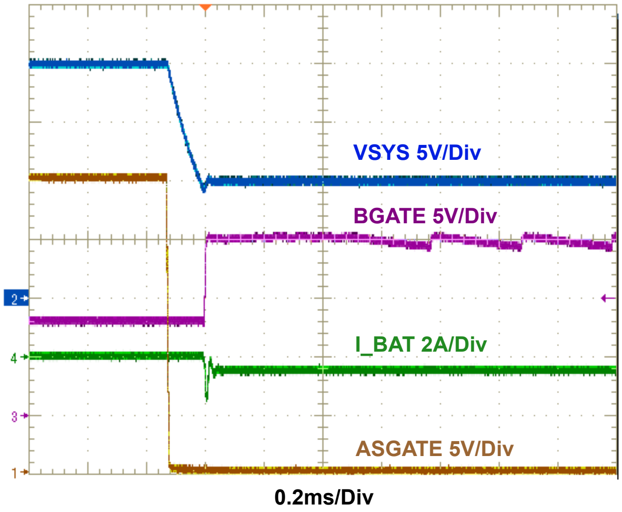


Figure 21. HPB: Enter Learn Mode

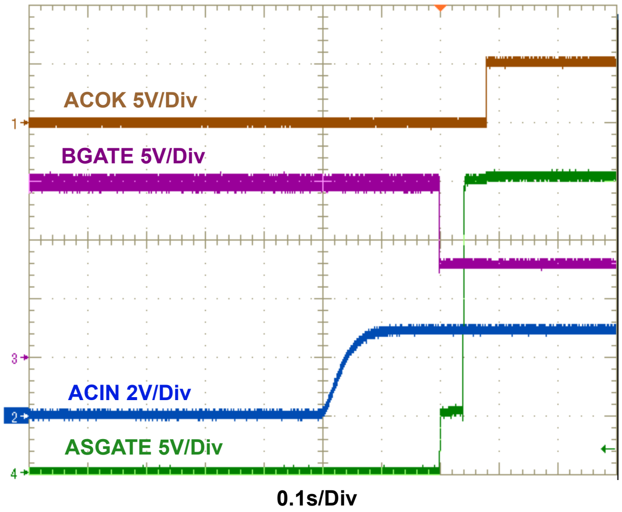


Figure 22. HPB: ASGATE Turning On Delay After Adapter Insertion. VADP = 20V, V_{BAT} = 10V

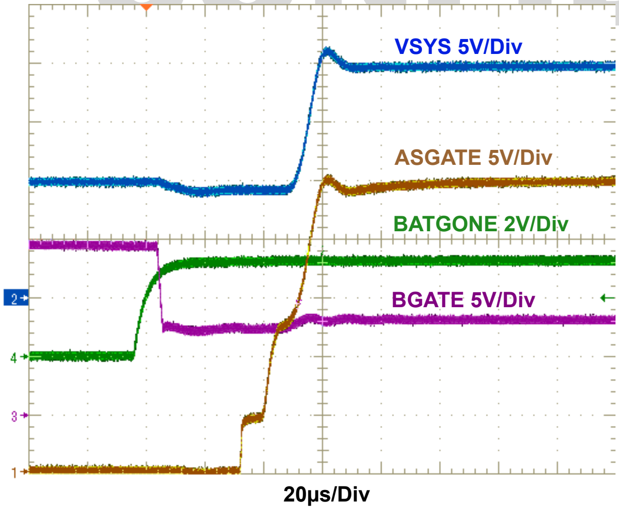


Figure 23. HPB: Battery Sudden Removal in Learn Mode by Pulling BATGONE to High

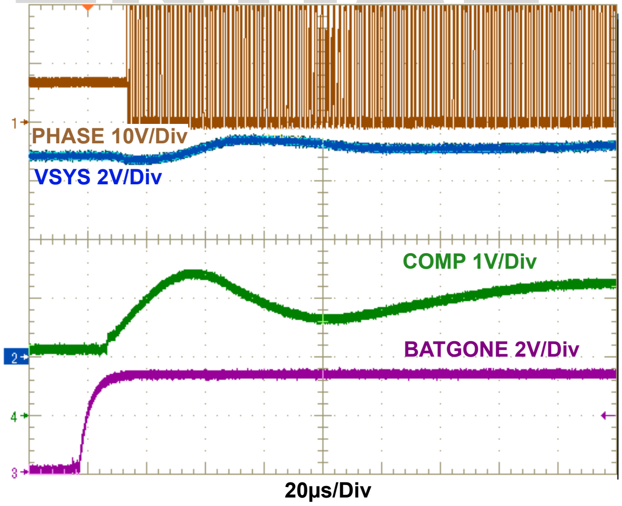


Figure 24. NVDC: Battery Sudden Removal in Learn Mode by Pulling BATGONE to High

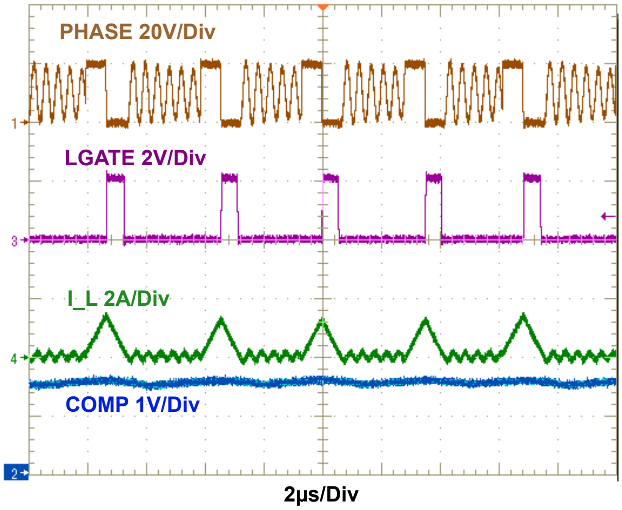


Figure 25. Discontinuous Conduction Mode (DCM) Switching

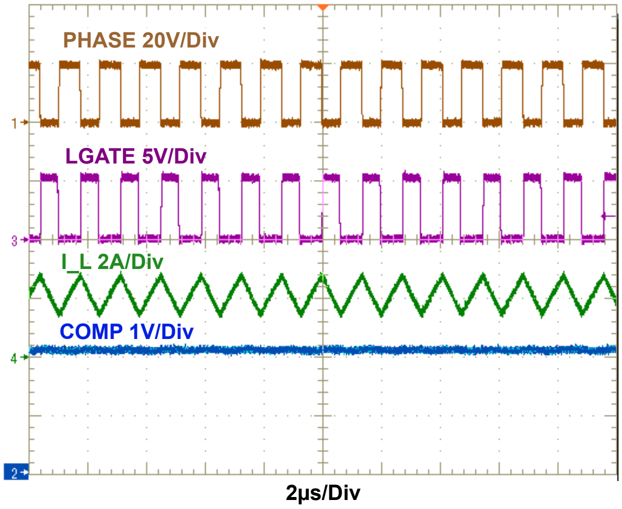


Figure 26. Continuous Conduction Mode (CCM) Switching

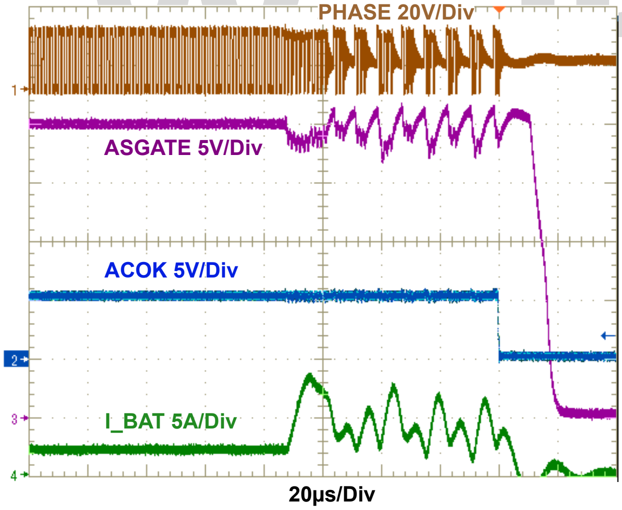


Figure 27. WOCP: Inductor Short During Charging. VADP = 20V, V_{BAT} = 10V, ChargeCurrent = 2A, CCLIM = 2V

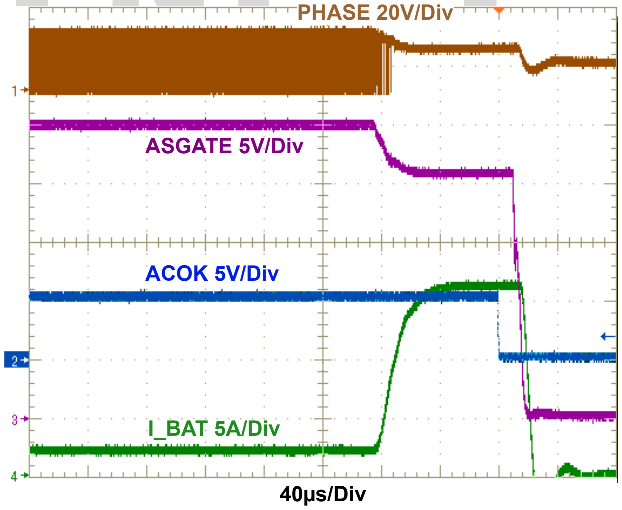


Figure 28. WOCP: High-Side MOSFET Short During Charging. VADP = 20V, V_{BAT} = 10V, ChargeCurrent = 2A, CCLIM = 2V

4. General SMBus Architecture

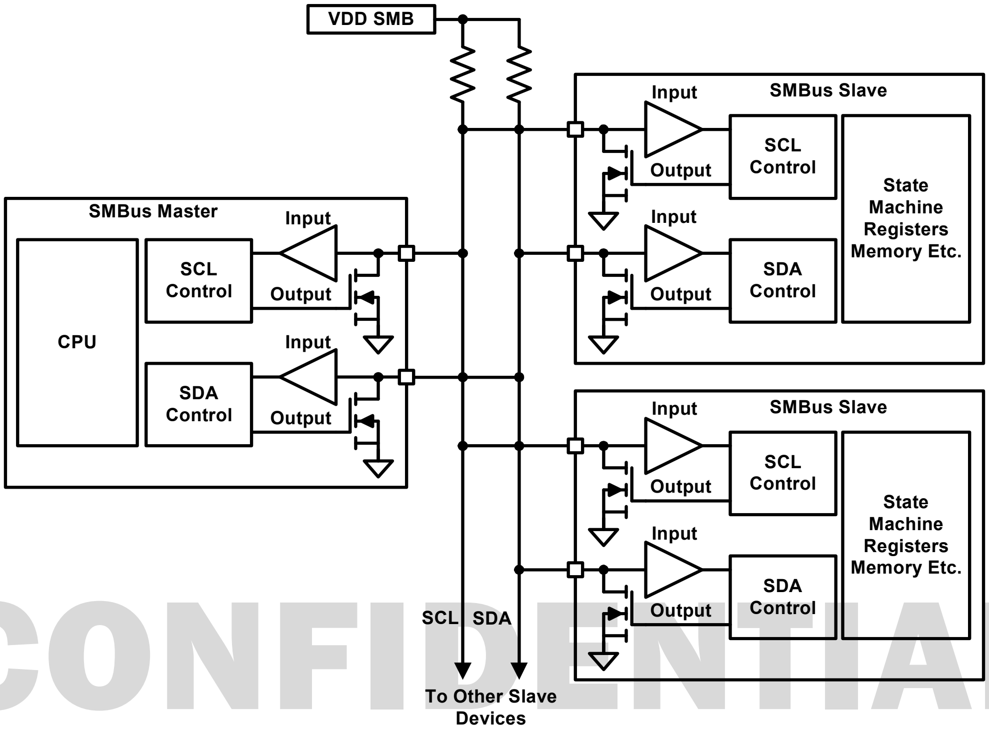


Figure 29. General SMBus Architecture

4.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the SCL, unless generating a START or STOP condition. The HIGH or LOW state of the data line can change only when the clock signal on the SCL line is LOW. See Figure 30.

4.2 Start and Stop Conditions

The START condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. See Figure 31.

The STOP condition is a LOW to HIGH transition on the SDA line while SCL is HIGH. A STOP condition must be sent before each START condition.

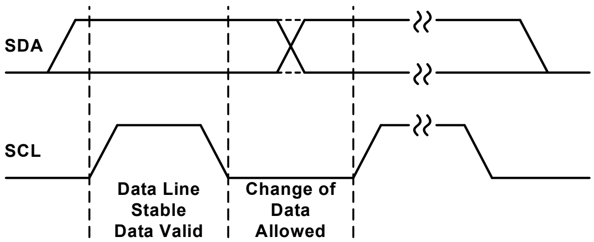


Figure 30. Data Validity

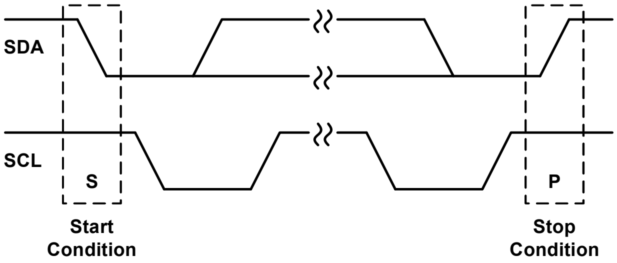


Figure 31. Start and Stop Waveforms

4.3 Acknowledge

Each address and data transmission uses nine-clock pulses. The ninth pulse is the acknowledge bit (ACK). After the start condition, the master sends seven slave address bits and a $R/\overline{W}$ bit during the next eight-clock pulses. During the nine-clock pulse, the device that recognizes its own address holds the data line low to acknowledge (as shown in Figure 32). Both the master and the salve use the ACK bit to acknowledge receipt of register addresses and data.

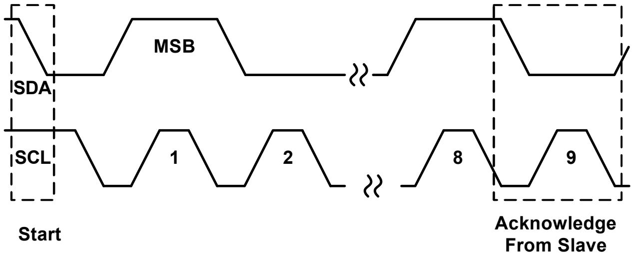


Figure 32. Acknowledge on the SMBus

4.4 SMBus Transactions

All transactions start with a control byte sent from the SMBus master device. The control byte begins with a START condition, followed by seven bits of slave address (0001001 for the ISL95522) and the $R/\overline{W}$ bit. The $R/\overline{W}$ bit is 0 for a WRITE or 1 for a READ. If any slave device on the SMBus bus recognizes its address, it acknowledges by pulling the Serial Data (SDA) line low for the last clock cycle in the control byte. If no slave exists at that address or it is not ready to communicate, the data line is 1, indicating a Not Acknowledge condition.

After the control byte is sent and the ISL95522 acknowledges it, the second byte sent by the master must be a register address byte such as 0x14 for the ChargeCurrent register. The register address byte tells the ISL95522 which register the master writes or reads. See Table 2 on page 33 for more information about the registers. When the ISL95522 receives a register address byte, it responds with an acknowledge.

4.5 Byte Format

Every byte put on the SDA line must be eight bits long and must be followed by an ACK bit. Data is transferred with the Most Significant Bit (MSB) first and the Least Significant Bit (LSB) last. The LO BYTE data is transferred before the HI BYTE data. For example, when writing 0x41A0, 0xA0 is sent first and 0x41 is sent second.

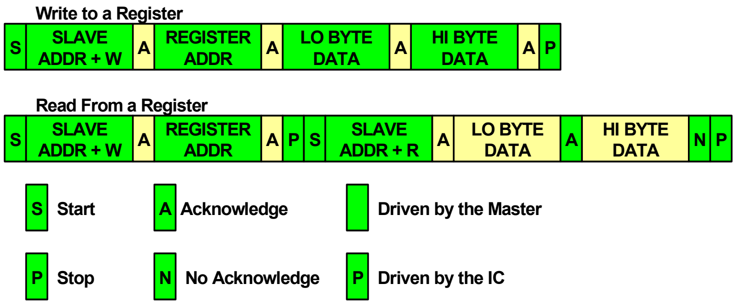


Figure 33. SMBus Read and Write Protocol

4.6 SMBus and I^2C Compatibility

The ISL95522 SMBus minimum input logic high voltage is 2V, so it is compatible with I^2Cs with pull-up power supplies higher than 2V.

The ISL95522 SMBus registers are 16 bits, so it is compatible with 16-bit I^2Cs or 8-bit I^2Cs with auto-increment capabilities.

5. ISL95522 SMBus Commands

The ISL95522 receives control inputs from the SMBus interface after Power-On Reset (POR). The serial interface complies with the System Management Bus Specification, which can be downloaded from www.smbus.org. The ISL95522 uses the SMBus Read Word and Write Word protocols shown in Figure 33 on page 32 to communicate with the host system and a smart battery. The ISL95522 is an SMBus slave device and does not initiate communication on the bus. It responds to the 7-bit address 0b0001001_:

Read address = 0b0001001**1**(0X13H)
Write address = 0b0001001**0**(0X12H)

The data (SDA) and clock (SCL) pins have Schmitt-trigger inputs that can accommodate slow edges. Choose pull-up resistors for SDA and SCL to achieve rise times according to the SMBus specifications.

The ISL95522 allows users to change the SMBus registers to change some functions and options, as shown in Table 2.

The illustration in this datasheet is based on current sensing resistors R_{s1} = 10mΩ and R_{s2} = 10mΩ unless specified otherwise. For other current sensing resistor specifications, see Table 19 on page 50 for more information.

Table 2. Registers Summary (R_{s1} = 10mΩ and R_{s2} = 10mΩ)

Register Names	Register Address	Read/ Write	# of Bits	Description	POR Bit State
ChargeCurrentLimit	0x14H	R/W	8	Bits<12:5> are used. If Bit<0> is interpreted as 1mA, the resolution is 32mA and the POR default value is 0A.	<12:5> 00000000
VIN Voltage	0x40H	R/W	6	Bits<13:8> are used. If Bit<0> is interpreted as 1.68mV, the resolution is 430.08mA and the POR default value is 0V.	<13:8> 000000
AdapterCurrentLimit1	0x3FH	R/W	6	Bits<12:7> are used. If Bit<0> is interpreted as 1mA, the resolution is 128mA and the POR default value is 8.064A.	<12:7> 111111
AdapterCurrentLimit2	0x3BH	R/W	6	Bits<12:7> are used. If Bit<0> is interpreted as 1mA, the resolution is 128mA and the POR default value is 8.064A.	<12:7> 111111
T1	0x37H	R/W	3	Bits<2:0> are used. If 2-level adapter current limit function is enabled and is tripped, T1 configures the effective duration of the AdapterCurrentLimit1 register. The POR default value is 500µs.	<2:0> 110
T2	0x38H	R/W	3	Bits<2:0> are used. If 2-level adapter current limit function is enabled and is tripped, T2 configures the effective duration of the AdapterCurrentLimit2 register. The POR default value is 100µs.	<2:0> 001
MaxChargeVoltage	0x15H	R/W	11	Bits<14:4> are used. If Bit<0> is interpreted as 1mV, the resolution is 16mV. The POR default value is based on PROG pin cell number programming: 2-cell: 8.192V 3-cell: 12.288V 4-cell: 16.4V The MaxChargeVoltage register should always be programmed higher than the MinChargeVoltage register.	

Table 2. Registers Summary (R_{s1} = 10mΩ and R_{s2} = 10mΩ) (Continued)

Register Names	Register Address	Read/ Write	# of Bits	Description	POR Bit State
MinChargeVoltage	0x3EH	R/W	6	Bits<13:8> are used. If Bit<0> is interpreted as 1mV, the resolution is 256mV. The POR default value is based on PROG pin cell number programming: 2-cell: 5.376V 3-cell: 8.064V 4-cell: 10.752V The MinChargeVoltage register should always be programmed lower than the MaxChargeVoltage register.	
PROCHOTDebounce	0x39H	R/W	2	Bits<1:0> are used. Sets the debounce time before asserting the PROCHOT# signal for NTC_PROCHOT#, ACPROCHOT# and DCPROCHOT#. The POR default value is 100µs.	<1:0> 01
PROCHOTDuration	0x3AH	R/W	3	Bits<2:0> are used. Sets the minimum duration of the PROCHOT# signal latch-up when it is asserted. The POR default value is 10ms.	<2:0> 011
ACPROCHOT	0x47H	R/W	6	Bits<12:7> are used. Sets the PROCHOT# threshold for adapter overcurrent conditions. If Bit<0> is interpreted as 1mA, the resolution is 128mA and the POR default value is 6.144A.	<12:7> 110000
DCPROCHOT	0x48H	R/W	6	Sets the PROCHOT# threshold for battery over-discharging current conditions. Bits<12:7> are used. If Bit<0> is interpreted as 1mA, the resolution is 128mA and the POR default value is 4.096A.	<12:7> 100000
Control1	0x3DH	R/W	16	See Control1 register Table 14.	
Control2	0x3CH	R/W	12	See Control2 register Table 15.	
Information1	0x46H	R	8	Various information reported over SMBus. See Information1 register Table 16.	
Information2	0x45H	R/W	8	PROG pin resistor reading result report. Also configures the 20mΩ current sensing resistor option. See Information2 register Table 17.	
ManufacturerID	0xFEH	R		ASCII for “I”.	0x49H
DeviceID	0xFFH	R			0x0AH

5.1 Setting Charging Current Limit

To set the charging current limit, write a 16-bit ChargeCurrentLimit command (0X14H or 0b00010100) using the Write Word protocol shown in Figure 33 on page 32 and the data format shown in Table 3 on page 35.

The ISL95522 limits the charging current by limiting the V_{CSOP} - V_{CSON} voltage. By using the recommended current sense resistor values shown in Table 18 on page 49, the register’s LSB always translates to 1mA of charging current. The ChargeCurrentLimit register accepts any charging current command; however, only the valid register bits are written to the register. Do not set the charging current limit lower than 96mA.

After POR, the ChargeCurrentLimit register is reset to 0x0000H. To set the battery charging current value, write a valid, non-zero number to the ChargeCurrentLimit register. The ChargeCurrentLimit register can be read back to verify its content.

Tables 21 and 22 on page 56 show the conditions to enable fast charging according to the ChargeCurrentLimit register setting for the HPB configuration and the NVDC configuration, respectively.

Table 3. ChargeCurrentLimit Register 0x14H (R_{s1} = 10mΩ and R_{s2} = 10mΩ).
(See Table 19 on page 50 for other configurations)

Bit	Description
<4:0>	Not used
<5>	0 = Adds 0mA of charging current limit. 1 = Adds 32mA of charging current limit.
<6>	0 = Adds 0mA of charging current limit. 1 = Adds 64mA of charging current limit.
<7>	0 = Adds 0mA of charging current limit. 1 = Adds 128mA of charging current limit.
<8>	0 = Adds 0mA of charging current limit. 1 = Adds 256mA of charging current limit.
<9>	0 = Adds 0mA of charging current limit. 1 = Adds 512mA of charging current limit.
<10>	0 = Adds 0mA of charging current limit. 1 = Adds 1024mA of charging current limit.
<11>	0 = Adds 0mA of charging current limit. 1 = Adds 2048mA of charging current limit.
<12>	0 = Adds 0mA of charging current limit. 1 = Adds 4096mA of charging current limit.
<15:13>	Not used

5.2 Setting Input Voltage Register

The input voltage register contains SMBus readable and writable input voltage limit. The default is 0V. This register accepts any current command, but only the valid register bit is written to the register and the maximum value is clamped at 27.095V.

Table 4. Input Voltage Register 0x40H

Bit	Description
<7:0>	Not used
<8>	0 = Adds 0mV of input voltage. 1 = Adds 430.08mV of input voltage.
<9>	0 = Adds 0mV of input voltage. 1 = Adds 860.16mV of input voltage.
<10>	0 = Adds 0mV of input voltage. 1 = Adds 1720.32mV of input voltage.
<11>	0 = Adds 0mV of input voltage. 1 = Adds 3440.64mV of input voltage.
<12>	0 = Adds 0mV of input voltage. 1 = Adds 6881.28mV of input voltage.
<13>	0 = Adds 0mV of input voltage. 1 = Adds 13762.56mV of input voltage.
<15:14>	Not used

5.3 Setting Adapter Current Limit

To set the adapter current limit, write a 16-bit AdapterCurrentLimit1 command (0x3FH or 0b00111111) and/or AdapterCurrentLimit2 command (0x3BH or 0b00111011) using the Write Word protocol shown in Figure 33 on page 32 and the data format shown in Table 5.

The ISL95522 limits the adapter current by limiting the V_{CSIP} - V_{CSIN} voltage. By using the recommended current sense resistor value as Table 18 shows, the register's LSB always translates to 1mA adapter current. Any adapter current limit command is accepted; however, only the valid register bits are written to the AdapterCurrentLimit1 and AdapterCurrentLimit2 registers. The minimum adapter current limit command is 128mA and a 0A command is rejected.

After POR, the AdapterCurrentLimit1 and AdapterCurrentLimit2 register are reset to 0x1F80. The AdapterCurrentLimit1 and AdpaterCurrentLimit2 registers can be read back to verify their content.

To set a second level adapter current limit, write a 16-bit AdapterCurrentLimit2 (0x3BH or 0b00111011) command using the Write Word protocol shown in Figure 33 on page 32 and the data format shown in Table 5.

The AdapterCurrentLimit2 register has the same specification as the AdapterCurrentLimit1 register. See "Two-Level Adapter Current Limit" on page 57 for operation details.

Table 5. AdapterCurrentLimit1 Register 0x3FH and AdapterCurrentLimit2 Register 0x3BH (R_{s1} = 10mΩ and R_{s2} = 10mΩ)

Bit	Description
<6:0>	Not used
<7>	0 = Adds 0mA of adapter current limit. 1 = Adds 128mA of adapter current limit.
<8>	0 = Adds 0mA of adapter current limit. 1 = Adds 256mA of adapter current limit.
<9>	0 = Adds 0mA of adapter current limit. 1 = Adds 512mA of adapter current limit.
<10>	0 = Adds 0mA of adapter current limit. 1= Adds 1024mA of adapter current limit.
<11>	0 = Adds 0mA of adapter current limit. 1 = Adds 2048mA of adapter current limit.
<12>	0 = Adds 0mA of adapter current limit. 1 = Adds 4096mA of adapter current limit.
<15:13>	Not used

5.4 Setting Two-Level Adapter Current Limit Duration

For a two-level adapter current limit, write a 16-bit T1 command (0x37H or 0b00110111) using the Write Word protocol shown in Figure 33 and the data format shown in Table 6 to set the AdapterCurrentLimit1 duration as the adapter current limit. Write a 16-bit T2 command (0x38H or 0b00111000) to set AdapterCurrentLimit2 duration as the adapter current limit. The T1 register and T2 register accept any command; however, only the valid register bits are written. See "Two-Level Adapter Current Limit" on page 57 for detailed operation.

Table 6. T1 Register 0x37H

Bit	Description
<2:0>	000 = 0ms 001 = 20ms 010 = 15ms 011 = 10ms 100 = 5ms 101 = 1ms 110 = 0.5ms 111 = 0.1ms
<15:3>	Not used

Table 7. T2 Register 0x38H

Bit	Description
<2:0>	000 = 15µs 001 = 100µs 010 = 500µs 011 = 1ms 100 = 300µs 101 = 750µs 110 = 3ms 111 = 10ms
<15:3>	Not used

5.5 Setting Maximum Charging Voltage

To set the maximum charging voltage, write a 16-bit MaxChargeVoltage command (0X15H or 0b00010101) using the Write Word protocol shown in Figure 33 on page 32 and the data format shown in Table 8.

The maximum charging voltage range is 7.168V to 18.432V. The MaxChargeVoltage register accepts any voltage command; however, only the valid register bits are written to the register.

The MaxChargeVoltage register sets the battery full charging voltage limit. For the NVDC configuration, the MaxChargeVoltage register setting is also the system bus voltage regulation point when the battery is present but is not in charge. See "NVDC Charger System Voltage Regulation" on page 58 for details.

The CSON pin senses the battery voltage for maximum charging voltage regulation. For the NVDC configuration, the CSON pin is also the system bus voltage regulation sense point.

Table 8. MaxChargeVoltage Register 0x15H

Bit	Description
<3:0>	Not used
<4>	0 = Adds 0mV of charging voltage. 1 = Adds 16mV of charging voltage.
<5>	0 = Adds 0mV of charging voltage. 1 = Adds 32mV of charging voltage.
<6>	0 = Adds 0mV of charging voltage. 1 = Adds 64mV of charging voltage.
<7>	0 = Adds 0mV of charging voltage. 1 = Adds 128mV of charging voltage.
<8>	0 = Adds 0mV of charging voltage. 1 = Adds 256mV of charging voltage.
<9>	0 = Adds 0mV of charging voltage. 1 = Adds 512mV of charging voltage.
<10>	0 = Adds 0mV of charging voltage. 1 = Adds 1024mV of charging voltage.
<11>	0 = Adds 0mV of charging voltage. 1 = Adds 2046mV of charging voltage.
<12>	0 = Adds 0mV of charging voltage. 1 = Adds 4096mV of charging voltage.
<13>	0 = Adds 0mV of charging voltage. 1 = Adds 8192mV of charging voltage.
<14>	0 = Adds 0mV of charging voltage. 1 = Adds 16384mV of charging voltage.
<15>	Not used

5.6 Setting Minimum Charging Voltage

To set the minimum charging voltage, write a 16-bit MinChargeVoltage command (0x3EH or 0b00111110) using the Write Word protocol shown in Figure 33 and the data format shown in Table 9.

The minimum charging voltage range is 2.048V to 16.128V. The MinChargeVoltage register accepts any voltage command; however, only the valid register bits are written to the register. The MinChargeVoltage register value should be set lower than the MaxChargeVoltage register value.

The MinChargeVoltage register sets the battery voltage threshold for entry and exit of the Trickle Charge mode. The VBAT pin senses the battery voltage to compare with the MinChargeVoltage register setting. See "Trickle Charging" on page 58 for details.

For the NVDC configuration, the MinChargeVoltage register setting is also the system voltage regulation point when the battery is not present. The CSON pin is the system voltage regulation sense point. See "NVDC Charger System Voltage Regulation" on page 58 for details.

Table 9. MinChargeVoltage Register 0x3EH

Bit	Description
<7:0>	Not used
<8>	0 = Adds 0mV of charging voltage. 1 = Adds 256mV of charging voltage.
<9>	0 = Adds 0mV of charging voltage. 1 = Adds 512mV of charging voltage.
<10>	0 = Adds 0mV of charging voltage. 1 = Adds 1024mV of charging voltage.
<11>	0 = Adds 0mV of charging voltage. 1 = Adds 2048mV of charging voltage.
<12>	0 = Adds 0mV of charging voltage. 1 = Adds 4096mV of charging voltage.
<13>	0 = Adds 0mV of charging voltage. 1 = Adds 8192mV of charging voltage.
<15:14>	Not used

5.7 Setting PROCHOT# Debounce Time

To set the PROCHOT# signal debounce time before its assertion for ACPROCHOT, DCPROCHOT, and NTC_PROCHOT, write a 16-bit PROCHOT# debounce time (0x39H or 0b00111001) using the Write Word protocol shown in Figure 33 and the data format shown in Table 10. The PROCHOT# Debounce Time register accepts any command; however, only the valid register bits are written.

The low system voltage PROCHOT# has a fixed 10µs debounce time.

Table 10. PROCHOT# Debounce Register 0x39H

Bit	Description
<1:0>	00 = 10µs 01 = 100µs 10 = 500µs 11 = 1ms
<15:2>	Not used

5.8 Setting PROCHOT# Duration

To set the PROCHOT# signal latch-up duration when it is asserted for ACPROCHOT, DCPROCHOT, and NTC_PROCHOT and low system voltage PROCHOT, write a 16-bit PROCHOT# Duration command (0x3AH or 0b01111010) using the Write Word protocol shown in Figure 33 and the data format shown in Table 11. The PROCHOT# Duration register accepts any command; however, only the valid register bits are written.

Table 11. PROCHOT# Duration Register 0x3Ah

Bit	Description
<2:0>	000 = 0ms 001 = 20ms 010 = 15ms 011 = 10ms 100 = 5ms 101 = 1ms 110 = 500µs 111 = 100µs
<15:3>	Not used

5.9 Setting PROCHOT# Threshold for Adapter Overcurrent Condition

To set the PROCHOT# assertion threshold for the adapter overcurrent condition, write a 16-bit ACPROCHOT command (0x47H or 0b01000111) using the Write Word protocol shown in Figure 33 on page 32 and the data format shown in Table 12. By using the recommended current sense resistor value as Table 18 on page 49 shows, the register's LSB always translates to 1mA adapter current. The ACPROCHOT register accepts any command; however, only the valid register bits are written to the register.

After POR, the ACPROCHOT register is reset to 0x1800H. The ACPROCHOT register can be read back to verify its content.

If the adapter current exceeds the ACPROCHOT register setting, the PROCHOT# signal asserts after the debounce time programmed by the PROCHOTDebounce register and latches on for a minimum time programmed by the PROCHOTDuration register.

For HPB configuration, the ACPROCHOT function is disabled when it is in Standby mode because Standby mode turns off the internal comparator reference, which is indicated by Information1 register Bit<8>.

Table 12. ACPROCHOT Register 0x47H (R_{s1} = 10mΩ and R_{s2} = 10mΩ).
(See Table 19 on page 50 for other configurations)

Bit	Description
<6:0>	Not used
<7>	0 = Adds 0mA of ACPROCHOT threshold. 1 = Adds 128mA of ACPROCHOT threshold.
<8>	0 = Adds 0mA of ACPROCHOT threshold. 1 = Adds 256mA of ACPROCHOT threshold.
<9>	0 = Adds 0mA of ACPROCHOT threshold. 1 = Adds 512mA of ACPROCHOT threshold.
<10>	0 = Adds 0mA of ACPROCHOT threshold. 1 = Adds 1024mA of ACPROCHOT threshold.
<11>	0 = Adds 0mA of ACPROCHOT threshold. 1 = Adds 2048mA of ACPROCHOT threshold.
<12>	0 = Adds 0mA of ACPROCHOT threshold. 1 = Adds 4096mA of ACPROCHOT threshold.
<15:13>	Not used

5.10 Setting PROCHOT# Threshold for Battery Over-Discharging Current Condition

To set the PROCHOT# signal assertion threshold for battery over-discharging current condition, write a 16-bit DCPROCHOT command (0x48H or 0b01001000) using the Write Word protocol shown in Figure 33 and the data format shown in Table 13. By using the recommended current sense resistor value as Table 18 on page 49 shows, the register's LSB always translates to 1mA adapter current. The DCPROCHOT register accepts any command; however, only the valid register bits are written to the register.

After POR, the DCPROCHOT register is reset to 0x1000H. The DCPROCHOT register can be read back to verify its content.

If the battery discharging current exceeds the DCPROCHOT register setting, The PROCHOT# signal asserts after the debounce time programmed by the PROCHOTDebounce register and latches on for a minimum time programmed by the PROCHOTDuration register.

In Battery Only mode, the DCPROCHOT function works only when PSYS or NTC is enabled, because enabling PSYS or NTC activates the internal comparator reference. The Information1 register bit<8> indicates whether the internal comparator reference is active.

When the adapter is present, the internal comparator reference is always active unless it is in Standby mode for the HPB configuration.

Table 13. DCPROCHOT Register 0x48H (R_{s1} = 10mΩ and R_{s2} = 10mΩ)
(See Table 19 on page 50 for other configurations)

Bit	Description
<6:0>	Not used
<7>	0 = Adds 0mA of DCPROCHOT threshold. 1 = Adds 128mA of DCPROCHOT threshold.
<8>	0 = Adds 0mA of DCPROCHOT threshold. 1 = Adds 256mA of DCPROCHOT threshold.
<9>	0 = Adds 0mA of DCPROCHOT threshold. 1 = Adds 512mA of DCPROCHOT threshold.
<10>	0 = Adds 0mA of DCPROCHOT threshold. 1 = Adds 1024mA of DCPROCHOT threshold.

Table 13. DCPROCHOT Register 0x48H (R_{s1} = 10mΩ and R_{s2} = 10mΩ)
(See Table 19 on page 50 for other configurations) (Continued)

Bit	Description
<11>	0 = Adds 0mA of DCPROCHOT threshold. 1 = Adds 2048mA of DCPROCHOT threshold.
<12>	0 = Adds 0mA of DCPROCHOT threshold. 1 = Adds 4096mA of DCPROCHOT threshold.
<15:13>	Not used

5.11 Control Registers

To change certain functions or options after POR, write a 16-bit control command to the Control1 register (0x3DH or 0b00111101) or Control2 register (0x3CH or 0b00111100) using the Write Word protocol shown in Figure 33 on page 32 and the data format shown in Tables 14 and 15, respectively.

Table 14. Control1 Register 0x3DH

Bit	Bit Name	Description	POR State
<0>	Standby Mode	1 = The charger enters Standby mode. 0 = The charger exits Standby mode. The Standby mode control bit is valid for the HPB configuration only and is valid only when adapter is present; it has no effect on the NVDC configuration. When the ISL95522 enters Standby mode, it turns off the internal references (indicated by Information1 register Bit<8>) and stops switching to enter a low power consumption mode with minimum quiescent current. If PSYS is already enabled, it cannot enter Standby mode.	0
<1>	Learn Mode	1 = The charger enters Learn mode. 0 = The charger exits Learn mode. The SMBus Learn mode control is valid only when PROG pin is not pulled to 5V after POR.	0
<2>	AMON	1 = Turns on the adapter current monitor AMON function. 0 = Turns off the adapter current monitor AMON function.	0
<3>	BMON	1 = Turns on the battery discharging current monitor BMON function. 0 = Turns off the battery discharging current monitor BMON function. To avoid overdischarging the battery, the BMON function is disabled if the battery voltage is less than 3.5V.	0
<4>	PSYS	1 = Turns on the system power monitor PSYS function. 0 = Turns off the system power monitor PSYS function. The PSYS function does not include the power provided by the battery if the battery voltage is less than 3.5V. If an adapter has already entered Standby mode in HPB configuration, PSYS cannot be turned on.	0

Table 14. Control1 Register 0x3DH (Continued)

Bit	Bit Name	Description	POR State
<5>	Low System Voltage Detection	1 = Turns on the low system voltage detect function. 0 = Turns off the low system voltage detect function. Bit<5> is valid only when the internal comparator reference is active, which is indicated by Information1 register Bit<8>. In Battery Only mode, the low system voltage detection function works only when PSYS or NTC is enabled, because enabling PSYS or NTC activates the internal comparator reference. When an adapter is present, the internal comparator reference is always active unless it is in Standby mode for HPB configuration. In HPB configuration, the ISL95522 senses the system voltage through the CSIP pin. In NVDC configuration, the ISL95522 senses the system voltage through the CSON pin.	0
<6>	NTC	1 = Turns on the NTC function. 0 = Turns off the NTC function. If the NTC pin voltage is less than 170mV when the NTC function is turned on, the PROCHOT# signal asserts after the debounce time programmed by the PROCHOTDebounce register and latches on for a minimum time programmed by the PROCHOTDuration register. For the NTC function to work, the internal reference indicated by Information1 register bit<8> needs to be active. When an adapter is present, the NTC function is always turned on unless it is in Standby mode, then Bit<6> is invalid. In Battery Only mode, Bit<6> can turn the NTC function on or off only when PSYS is turned off; the NTC function is always turned on automatically if PSYS is turned on.	0
<7>	Fast Learn Mode Exit	1 = Fast Learn Mode Exit. 0 = Slow Learn Mode Exit. Fast Learn Mode Exit turns on the ASGATE MOSFETs instantly without going through the ASGATE soft-start turning on procedure when the BATGONE pin voltage goes from logic LOW to HIGH. Slow Learn Mode Exit goes through the ASGATE soft-start turning on procedure 163ms after the BATGONE pin voltage goes from logic LOW to HIGH. The Fast Learn Mode Exit control bit is valid only when the battery is removed during Learn mode and works only for the HPB configuration. It has no effect in the NVDC configuration.	0
<9:8>	Threshold for Low System Voltage Detection	If the Control register Bit<5> = 1, Bits<9:8> program the low system voltage detection threshold. If the system voltage is below this threshold, the PROCHOT# signal asserts after a fixed 10µs debounce time and latches on for a minimum time programmed by the PROCHOTDuration register. 00 = 5.6V threshold 01 = 6.06V threshold 10 = 6.53V threshold 11 = 7V threshold Valid only when Control1 register Bit<5> = 1.	00

Table 14. Control1 Register 0x3DH (Continued)

Bit	Bit Name	Description	POR State
<10>	Turbo/Boost Mode	1 = Disables Turbo/Boost mode. 0 = Enables Turbo/Boost mode.	1
<11>	Charging Current WOCP	1 = Disables charging current way overcurrent protection. 0 = Enables charging current way overcurrent protection.	0
<12>	Enable Charging	0 = Disables charging. 1 = Enables charging.	1
<14:13>	Force the Number of Battery Cells in Series	Bits<14:13> can overwrite the number of battery cells in series that are programmed by the PROG pin. When Bits<14:13> are written, only the POR default MaxChargeVoltage register value and MinChargeVoltage register value changes according to the cell number. The battery 4.6V/cell overvoltage protection threshold also changes according to the cell number. The MaxChargeVoltage register setting should always be smaller than battery overvoltage threshold 4.6V * cell#. If Bits<14:13> are not used, keep their POR code based on the PROG pin cell# setting. 00 = Not available and are ignored if written. 01 = 2-cell 10 = 3-cell 11 = 4-cell	PROG cell#
<15>	SMBus Timeout	The ISL95522 includes a timer to ensure the SMBus master is active and to prevent overcharging the battery. If the adapter is present and if the ISL95522 does not receive a write to the MaxChargeVoltage or ChargeCurrentLimit register within 175s, the ISL95522 terminates charging. If a timeout occurs, writing the MaxChargeVoltage or ChargeCurrentLimit register re-enables charging. 0 = Enable the SMBus timeout function. 1 = Disable the SMBus timeout function.	0

Table 15. Control2 Register 0x3CH

Bit	Bit Name	Description	POR State
<3:0>	Frequency Setting	Overwrite the switching frequency set by the FSET pin. See the default CCM switching frequency programming (Table 20 on page 51) for the correlation. 1111 = 942kHz (equivalent to R_FSET = 0Ω) 1110 = 796kHz 1101 = 693kHz 1100 = 610kHz 1011 = 644kHz 1010 = 583kHz 1001 = 533kHz 1000 = 491kHz 0111 = 487kHz 0110 = 453kHz 0101 = 427kHz 0100 = 400kHz 0011 = 396kHz 0010 = 375kHz 0001 = 356kHz 0000 = Switching frequency set by FSET pin To keep the switching frequency set by the PROG pin resistor, leave Bit<3:0> as is or write code 0000, which sets the same frequency as the PROG pin resistor.	0000

Table 15. Control2 Register 0x3CH (Continued)

Bit	Bit Name	Description	POR State
<4>	Release Adapter Current Limit when No Battery	When there is no battery, Bit<4> enables or releases the adapter current limit for the NVDC configuration. 0 = Enable adapter current limit function. 1 = Release adapter current limit function.	0
<5>	ASGATE Turn-On Delay	0 = Sets the restart ASGATE turn on delay to 1.3s. 1 = Sets the restart ASGATE turn on delay to 163ms. Bit<5> configures the ASGATE restart delay only in a fault condition (adapter OVP and WOCP). In normal operation after the adapter is plugged in, the ASGATE turn on delay is always 163ms, regardless of the Bit<5> setting.	0
<6>	Two-level Adapter Current Limit Function	0 = Disables the two-level adapter current limit function. 1 = Enables the two-level adapter current limit function.	1
<7>	Trickle Charging Current	Bit<7> changes the trickle charging current value. 0 = 256mA trickle charging current 1 = 128mA trickle charging current	1
<8>	Adapter OVP	0 = Enables the adapter OVP function; 1 = Disables the adapter OVP function. If the adapter OVP function is enabled, the ISL95522 turns off ASGATE and pulls down ACOK when ACIN > 3.5V.	0
<9>	PSYS Current Gain	For the “$R_{s1} = 10m\Omega, R_{s2} = 5m\Omega$” and “$R_{s1} = 10m\Omega, R_{s2} = 10m\Omega$” configuration: 0 = 1.12µA/W 1 = 0.285µA/W For the “$R_{s1} = 20m\Omega, R_{s2} = 10m\Omega$” and “$R_{s1} = 20m\Omega, R_{s2} = 20m\Omega$” configuration: 0 = 2.24µA/W 1 = 0.57µA/W	0
<10>	ACLIM Inrush Current Limit Time	0 = Sets the soft-start ACLIM inrush current limit period to 1ms when an adapter is plugged in. 1 = Sets the soft-start ACLIM inrush current limit period to 4ms when an adapter is plugged in.	0
<11>	BGATE Off Timing	Bit<11> is valid for the HPB configuration only. It changes the BGATE FET turn-off timing when an adapter is plugged in. 0 = Turns off the BGATE FET according to battery voltage (see “Soft-Start” on page 51 for details). 1 = Turns off the BGATE FET before turning on ASGATE FETs.	0
<13>	ACLIM Function	Bit<13> configures ACLIM to be functional all the time or only during the ASGATE turn-on procedure to limit the inrush current. 0 = The ACLIM function is on all the time. 1 = The ACLIM function is off after ACOK assertion.	0

Table 15. Control2 Register 0x3CH (Continued)

Bit	Bit Name	Description	POR State
<15, 14, 12>	DCM LGATE Turning Off Timing	Bits<15:14> and Bit<12> adjust the phase comparator offset when the buck switcher is in DCM operation. The LGATE turning off timing is then varied to minimize the MOSFET's body diode conduction time. Bit<15,14,12>: 000 = 0mV 001 = +1mV 010 = +2mV 011 =+3mV 100 = +4mV 101 = +5mV 110 = +6mV 111 = +7mV	000

5.12 Information Registers

To read the information register, write a 16-bit Information1 command (0x46H or 0b01000110) or Information2 command (0x45H or 0b01000101) using the Read Word protocol shown in Figure 33 on page 32 and the data format shown in Tables 16 and 17, respectively.

Table 16. Information1 Register 0x46H

Bit	Bit Name	W/R	Description
<0>	Adapter Present	R	0 = The adapter is not present. 1 = The adapter is present.
<1>	ASGATE On	R	0 = ASGATE is off. 1 = ASGATE is on.
<2>	VBAT<MinChargeVoltage	R	0 = VBAT>MinChargeVoltage. 1 = VBAT<MinChargeVoltage. Valid only when Information1 register Bit<8> = 1.
<3>	VSYS<Low System Voltage Setting	R	0 = VSYS>Low System Voltage Setting programmed by Control1 register Bit<9:8>. 1 = VSYS<Low System Voltage Setting programmed by Control1 register Bit<9:8>. Valid only when Information1 register Bit<8> = 1.
<4>	NTC_PROCHOT#	R	0 = NTC_PROCHOT# not asserted. 1 = NTC_PROCHOT# asserted. Valid only when Information1 register Bit<8> = 1.
<5>	In Trickle Charge Mode	R	0 = Not in Trickle Charge mode. 1 = In Trickle Charge mode. Bit<5> is valid for the NVDC configuration only.
<6>	In Turbo/Boost Mode	R	0 = Not in Turbo/Boost mode. 1 = In Turbo/Boost mode. For the NVDC configuration, if BGATE is already on before entering Turbo mode, BGATE stays on after entering Turbo mode; Bit<6> does not indicate Turbo mode in this case.
<7>	ACPROCHOT	R	0 = ACPROCHOT# is not asserted. 1 = ACPROCHOT# is asserted.

Table 16. Information1 Register 0x46H (Continued)

Bit	Bit Name	W/R	Description
<8>	Reference Active	R	0 = Reference is not active. 1 = Reference is active. When Bit<8> = 1, Information Register Bits <4:2> are valid. When an adapter is present, the internal comparator reference is always active unless it is in Standby mode for the HPB charger configuration. In Battery Only mode, the default internal reference is not active unless PSYS or NTC is enabled.

Table 17. Information2 Register 0x45H

Bit	Bit Name	W/R	Description	POR State
<0> <8>	R_{s1}	W/R	If R_{s1} = 20mΩ (R_{s1} = 20mΩ and R_{s2} = 10mΩ or R_{s1} = 20mΩ and R_{s2} = 20mΩ), both Bit<8> and Bit<0> need to be programmed as 1 to have correct internal current sensing scaling. Bit<8>:<0>: <0>:<0> = R_{s1} = 10mΩ <0>:<1> = R_{s1} = 10mΩ <1>:<0> = R_{s1} = 10mΩ <1>:<1> = R_{s1} = 20mΩ	0:0
<3:1>			Not used. Internally hardwired as <3:1> = 010.	
<5:4>	Cell Number	R	00 = Not available. 01 = 2-cell 10 = 3-cell 11 = 4-cell	
<6>	Current Sensing Resistor	R	0 = "R_{s1}:R_{s2} = 2:1" (R_{s1} = 10mΩ and R_{s2} = 5mΩ or R_{s1} = 20mΩ and R_{s2} = 10mΩ) 1 = "R_{s1}:R_{s2} = 1:1" (R_{s1} = 10mΩ and R_{s2} = 10mΩ or R_{s1} = 20mΩ and R_{s2} = 20mΩ) Together with Bit<8> and Bit<0> R_{s1} setting, it can be calculated that R_{s1} = 10mΩ or R_{s1} = 20mΩ.	
<7>	Charger Configuration	R	0 = HPB charger configuration. 1 = NVDC charger configuration.	
<15:9>			Not used.	

6. Application Information

6.1 R3 Modulator

The ISL95522 uses the Renesas Robust Ripple Regulator (R3) modulation scheme. The R3 modulator combines the best features of fixed frequency PWM and hysteric PWM while eliminating many of their shortcomings. Figure 34 on page 48 shows the R3 modulator circuit and Figure 35 on page 48 shows the operation principles in steady state.

There is a fixed voltage window (VW window) between VW and COMP. The modulator charges the ripple capacitor C_r with a current source equal to $g_m(V_{IN} - V_o)$ during PWM on-time and discharges the ripple capacitor C_r with a current source equal to g_mV_o during PWM off-time, where g_m is a gain factor. The C_r voltage, V_{cr}, therefore emulates the inductor current waveform. The modulator turns off the PWM pulse when V_{cr} reaches VW and turns on the PWM pulse when it reaches COMP.

Because the modulator works with V_{cr}, which is a large amplitude and noise free synthesized signal, it achieves lower phase jitter than conventional hysteretic mode modulators.

Figure 36 on page 48 shows the operation principles during dynamic response. The COMP voltage rises during dynamic response, turning on PWM pulses earlier and more frequently. This operation temporarily allows for higher control loop bandwidth than a conventional fixed frequency PWM modulator at the same steady-state switching frequency.

The R3 modulator can operate in Diode Emulation (DE) mode to increase light-load efficiency. In DE mode, the low-side MOSFET conducts when the current is flowing from source-to-drain and does not allow reverse current, emulating a diode. As shown in Figure 37 on page 48, when LGATE is on, the low-side MOSFET carries current, creating negative voltage on the phase node due to the voltage drop across the ON-resistance. The IC monitors the current by monitoring the phase node voltage. It turns off LGATE when the phase node voltage reaches zero to prevent the inductor current from reversing the direction and creating unnecessary power loss.

If the load current is light enough, as Figure 37 shows, the inductor current reaches and stays at zero before the next phase node pulse and the regulator is in Discontinuous Conduction Mode (DCM). If the load current is heavy enough, the inductor current never reaches 0A and the regulator is in CCM although the controller is in DE mode.

Use Control2 register Bit<15:14> to adjust the LGATE turn-off timing when the inductor current reaches near zero in DCM operation. The default timing purposely turns off LGATE slightly earlier than the inductor current zero crossing. The SMBus bit can adjust the timing more aggressively towards the precise zero-crossing point to minimize the MOSFET’s body diode conduction time for higher efficiency at light load. However, do not turn off LGATE after the inductor current zero crossing; this can feed energy back to the adapter side.

Figure 38 on page 48 shows the operation principle in DE mode at light load. The load gets incrementally lighter in the three cases from top to bottom. The PWM on-time is determined by the VW window size, so it is the same, making the inductor current triangle the same in the three cases. The R3 modulator clamps the ripple capacitor voltage V_{cr} in DE mode to make it mimic the inductor current. The COMP voltage takes longer to reach V_{cr}, which naturally stretches the switching period. The inductor current triangles move farther apart from each other such that the inductor current average value is equal to the load current. The reduced switching frequency helps increase light-load efficiency.

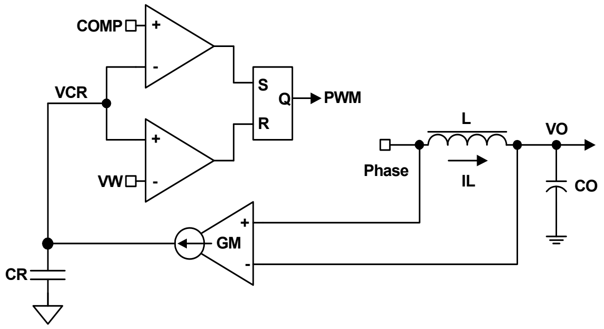


Figure 34. R3 Modulator

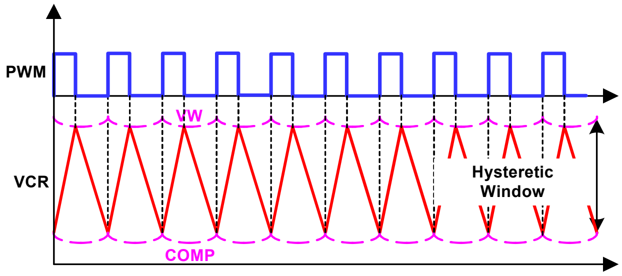


Figure 35. R3 Modulator Operation Principles in Steady State

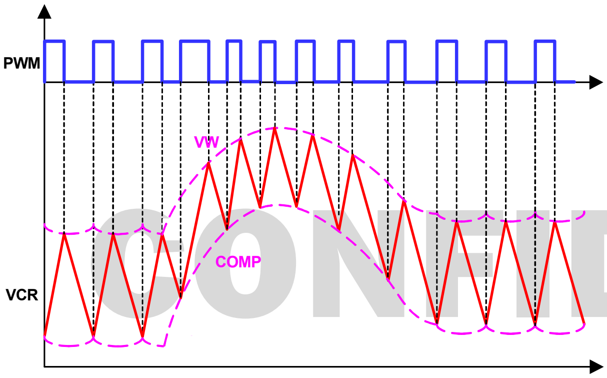


Figure 36. R3 Modulator Operation Principles in Dynamic Response

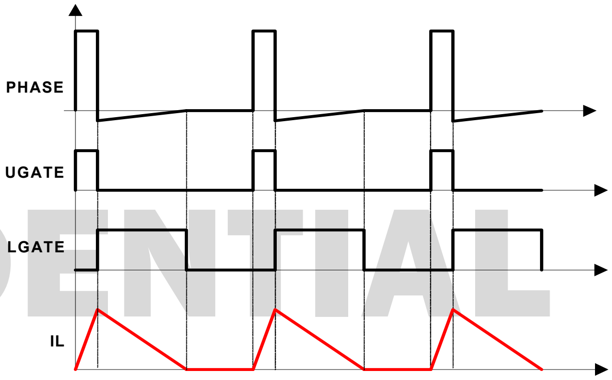


Figure 37. Diode Emulation

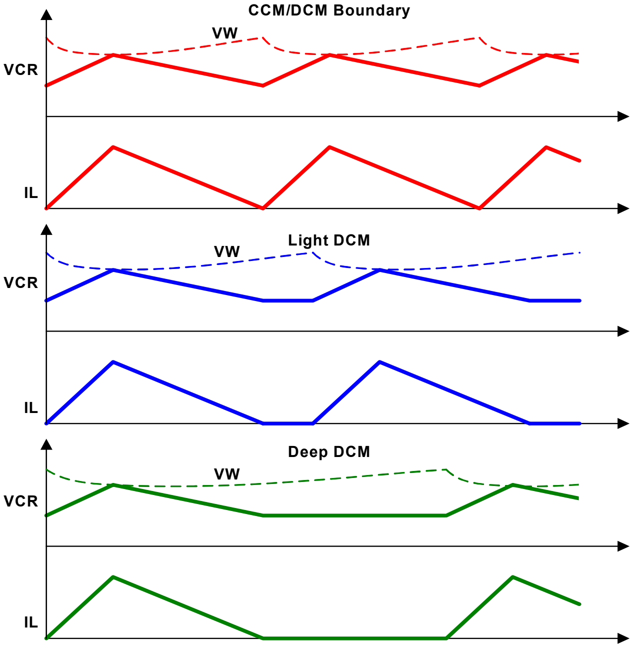


Figure 38. Period Stretching

6.2 Programming Charger Options

Table 18. Prog Pin Programming Options

Prog-GND Resistance (kΩ)	Charger Type	Current Sense Resistor Value	Default Number of Battery Cells in Series
Typ (1% Standard Resistor)			
0	NVDC	R_{s1}:R_{s2} = 2:1 R_{s1} = 10mΩ R_{s2} = 5mΩ or R_{s1} = 20mΩ R_{s2} = 10mΩ	3
22.6			4
38.3			2
69.8		R_{s1}:R_{s2} = 1:1 R_{s1} = 10mΩ R_{s2} = 10mΩ or R_{s1} = 20mΩ R_{s2} = 20mΩ	3
86.6			4
102			2
150	HPB		4
165			2
182			3
215		R_{s1}:R_{s2} = 2:1 R_{s1} = 10mΩ R_{s2} = 5mΩ or R_{s1} = 20mΩ R_{s2} = 10mΩ	4
237			2
255			3

The resistor from the PROG pin to GND programs the configuration of the ISL95522 as an HPB charger or NVDC charger, as well as the default number of battery cells in series and the default values of the adapter and battery current sense resistors R_{s1} and R_{s2}. Table 18 shows the programming options.

Before soft-start and when V_{DD} voltage reaches its POR value, the ISL95522 sources 10µA current out of the PROG pin and reads the PROG pin voltage to determine the resistor value. However, application environmental noise may pollute the PROG pin voltage and cause an incorrect reading. If noise is a concern, connect a capacitor from the PROG pin to GND to provide filtering. The resistor and the capacitor RC time constant should be less than 40µs so the PROG pin voltage can rise to steady state before the ISL95522 reads it.

The ISL95522 can be programmed in two different battery charger configurations.

Figure 1 on page 2 shows the typical application circuit for an HPB charger. In this configuration, the ISL95522 connects the system voltage rail to either the adapter or the battery. When the system is in Turbo mode, which means the system is drawing more power than the adapter's power rating, the ISL95522 operates as a boost converter to reverse-boost the battery energy to the system voltage rail, so the battery works with the adapter to supply the system power.

Figure 6 on page 8 shows the typical application circuit for the NVDC charger. In this configuration, the ISL95522 connects the system voltage rail to either the output of the buck switcher or the battery. In a Turbo event, the ISL95522 turns on the BGATE to discharge the battery so the battery works with the adapter together to supply the system power.

The PROG pin resistor programs the ratio of the current sensing resistor values R_{s1} and R_{s2} as 2:1 or 1:1. Therefore, four sets of R_{s1} and R_{s2} current sensing resistor values can be used, for example:

(1) $R_{s1} = 10m\Omega$, $R_{s2} = 5m\Omega$

(2) $R_{s1} = 10m\Omega$, $R_{s2} = 10m\Omega$

(3) $R_{s1} = 20m\Omega$, $R_{s2} = 10m\Omega$

(4) $R_{s1} = 20m\Omega$, $R_{s2} = 20m\Omega$

If the 20mΩ R_{s1} is used, the SMBus Information2 register Bit<0> and Bit<8> both need to be set as 1 for the appropriate internal current sensing scaling.

Smaller current sense resistor values reduce power loss while larger current sense resistor values give better accuracy.

The PROG pin resistor configures the internal current sense gain automatically for different R_{s1} and R_{s2}, such that the SMBus command remains the same for 20mΩ or 10mΩ R_{s1} and for 10mΩ or 5mΩ R_{s2}. For example, the AdapterCurrentLimit1 register, AdapterCurrentLimit2 register, and the ACPROCHOT register can be programmed with the same SMBus command value, regardless of whether R_{s1} is 20mΩ or 10mΩ, to obtain the same current. The ChargeCurrent register and DCPROCHOT register can be programmed with the same SMBus command value, regardless of whether R_{s2} is 10mΩ or 5mΩ, to obtain the same current. Using any option results in a 1mA/LSB correlation in the SMBus commands.

If the R_{s1} and R_{s2} values are different from the PROG pin programming table, scale the SMBus command accordingly to obtain the correct current.

Upon POR, the ISL95522 uses the default number of cells in series as Table 18 shows and sets the default MaxChargeVoltage register value and default MinChargeVoltage register value accordingly. When SMBus communication is established, the SMBus can program a different number of battery cells in series through SMBus Control1 register Bit<14:13>.

Table 19 shows the adapter current and battery current related settings according to different R_{s1} and R_{s2} options.

Table 19. Current Sensing Resistor Configurations

Current Sensing Resistors		Registers			K_{PSYS} (µA/W)	
		ChargeCurrent	DCPROCHOT	AdapterCurrentLimit1* AdapterCurrentLimit2* ACPROCHOT**	Control2 Bit<9> = 0	Control2 Bit<9> = 1
1	R_{s1} = 10mΩ R_{s2} = 5mΩ	Bit<12:5> Max = 1FE0h, 8.160A Min = 0020h, 32mA Default = 0000h, 0A	Bit<13:8> Max = 3F00h, 16.128A Min = 0100h, 256mA Default = 2000h, 8.192A	Bit<12:7> Max = 1F80h, 8.064A Min = 0080h, 128mA *Default = 1F80h, 8.064A **Default = 1800h, 6.144A	1.12	0.285
2	R_{s1} = 10mΩ R_{s2} = 10mΩ	Bit<12:5> Max = 1FE0h, 8.160A Min = 0020h, 32mA Default = 0000h, 0A	Bit<12:7> Max = 1F80h, 8.064A Min = 0080h, 128mA Default = 1000h, 4.096A	Bit<12:7> Max = 1F80h, 8.064A Min = 0080h, 128mA *Default = 1F80h, 8.064A **Default = 1800h, 6.144A	1.12	0.285
3	R_{s1} = 20mΩ R_{s2} = 10mΩ	Bit<11:4> Max = 0FF0, 4.080A Min = 0010, 16mA Default = 0000h, 0A	Bit<12:7> Max = 1F80h, 8.064A Min = 0080h, 128mA Default = 1000h, 4.096A	Bit<11:6> Max = 0FC0h, 4.032A Min = 0040h, 64mA *Default = 0FC0h, 4.032A **Default = 0C00h, 3.072A	2.24	0.57
4	R_{s1} = 20mΩ R_{s2} = 20mΩ	Bit<11:4> Max = 0FF0, 4.080A Min = 0010, 16mA Default = 0000h, 0A	Bit<11:6> Max = 0FC0h, 4.032A Min = 0040h, 64mA Default = 0800h, 2.048A	Bit<11:6> Max = 0FC0h, 4.032A Min = 0040h, 64mA *Default = 0FC0h, 4.032A **Default = 0C00h, 3.072A	2.24	0.57

6.3 Programming Switching Frequency

Table 20. Default CCM Switching Frequency Options

FSET-GND Resistance (kΩ)	Switching Frequency (kHz)
Typ (1% Standard Resistor)	**Typ (±15%)**
0	942
22.6	796
38.3	693
54.9	610
69.8	644
86.6	583
102	533
118	491
133	487
150	453
165	427
182	400
200	396
215	375
237	356
255	333

The resistor from the FSET pin to GND programs the default CCM switching frequency, as shown in Table 20. Before soft-start, the ISL95522 sources 10µA current out of the FSET pin and reads the FSET pin voltage to determine the resistor value. However, application environmental noise can pollute the FSET pin voltage and cause incorrect readings. If noise is a concern, connect a capacitor from the FSET pin to GND to provide filtering. The resistor and the capacitor RC time constant should be less than 40µs so the FSET pin voltage can rise to steady state before the ISL95522 reads it.

In DE mode, the ISL95522 uses a phase comparator to monitor the PHASE node voltage during low-side switching FET on-time to detect the inductor current zero crossing. The phase comparator needs a minimum on-time of the low-side switching FET for it to recognize inductor current zero crossing. If the low-side switching FET on-time is too short for the phase comparator to successfully recognize the inductor zero crossing, the ISL95522 can lose diode emulation ability. To prevent this, the ISL95522 employs a minimum low-side switching FET on-time. When the intended low-side switching FET on-time is shorter than the minimum value, the ISL95522 stretches the switching period to keep the low-side switching FET on-time at the minimum value, which causes the CCM switching frequency to drop below the set point. This effect is pronounced only in applications using a 4-cell battery and high switching frequency setting.

The switching frequency can be changed through SMBus Control2 register Bit<3:0> after POR. See Table 15 on page 43 for a detailed description.

6.4 Soft-Start

When the DCIN pin voltage is higher than 5V, an internal LDO starts to regulate and output 5V on the VDDP pin, which is the power supply for the gate drives.

The VDD pin is the 5V power supply for the ISL95522 control circuitry. An RC filter is recommended to generate the VDD pin voltage from the VDDP pin voltage. When the VDD pin voltage exceeds its POR, the ISL95522 sources 10µA current out of the PROG pin and reads the pin voltage to determine the PROG resistor value; it then sources 10µA current out of the FSET pin and reads the pin voltage to determine the FSET resistor value. The PROG resistor and the FSET resistor values program the configurations of the ISL95522.

Soft-start begins when the VDD pin voltage exceeds its POR, the ACIN pin voltage exceeds 2V, the DCIN pin voltage is higher than the VBAT pin voltage, and after the 163ms delay.

Note that after the adapter is plugged in, the ASGATE turn-on delay is always 163ms, regardless of the Control2 register Bit<5> setting. Control2 register Bit<5> only sets the ASGATE turn-on delay during restart in a fault condition.

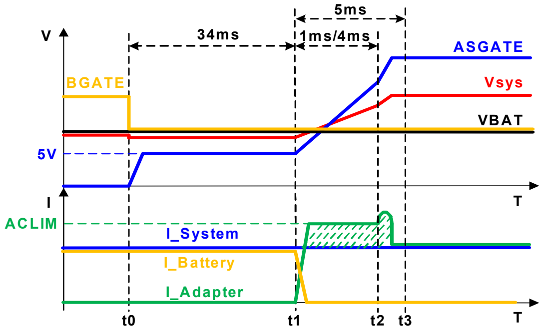


Figure 39. Soft-Start with $V_{BAT} < 4.5V$ or $V_{BAT} > 7V$

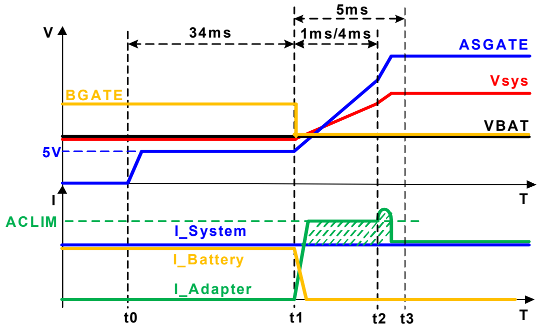


Figure 40. Soft-Start with $4.5V < V_{BAT} < 7V$

In both the HPB charger and the NVDC charger configurations, during soft-start, the ISL95522 limits the adapter current in several steps. Figure 39 shows that at t0, the ISL95522 outputs 20µA current source to charge the ASGATE pin voltage to 5V and then holds the ASGATE pin voltage at 5V for 34ms until t1. From t1 to t2, the ISL95522 limits the adapter current at the value set by the ACLIM pin voltage for the next 1ms (a default 4ms option is available through SMBus Control2 register Bit<10>). From t2 to t3, the ISL95522 outputs 20µA for another 4ms (or 1ms) to fully turn on ASGATE without actively limiting the adapter current. ACOK is asserted high after the ASGATE is fully turned on. The stepped soft-start scheme carefully biases up the system and protects the back-to-back ASGATE FETs against potential damage caused by the inrush current.

Figure 41 shows the HPB configuration without the battery soft-start waveform when the system load is less than the ACLIM-set current level. During t1 through t2, the ISL95522 charges the system bus capacitor with (ACLIM - system load) current and reaches the adapter voltage by t2. There is no inrush current after t2.

Figure 42 shows the HPB configuration without the battery soft-start waveform when the system load is greater than the ACLIM-set current level, which is not a recommended mode of operation. During t2 through t3, the ISL95522 fully turns on the ASGATE and lets the adapter charge the system bus capacitor without current limit.

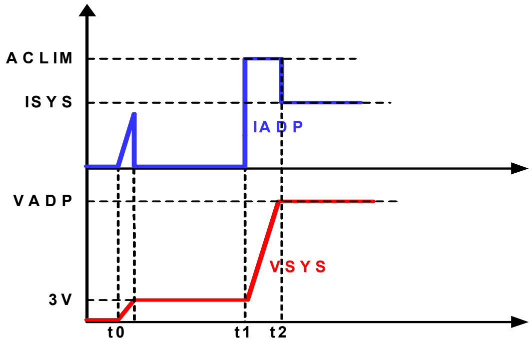


Figure 41. No Battery Soft-Start with I_{SYS} < ACLIM

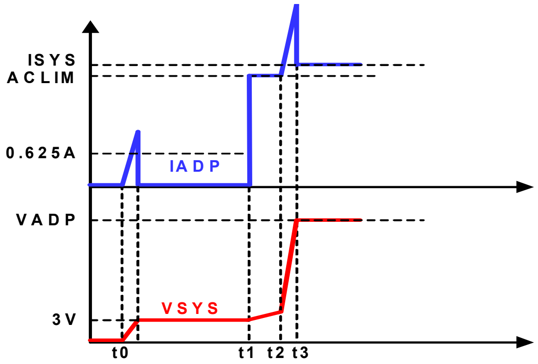


Figure 42. No Battery Soft-Start with I_{SYS} > ACLIM

In the HPB charger configuration, the ISL95522 can determine when to turn off the BGATE MOSFET to prevent system voltage disturbance. The BGATE MOSFET turns off at t0 before ASGATE ramps up if $V_{BAT} < 4.5V$ or $V_{BAT} > 7V$ as shown in Figure 39 and remains on until t2 if $4.5V < V_{BAT} < 7V$ as shown in Figure 40. This scheme prevents the system bus voltage from dropping by the MOSFET body-diode voltage drop caused by the BGATE MOSFET turning off early. This should not pose any danger to the battery. However, if this scheme is not desired, Control2 register Bit<11> can turn off BGATE before ASGATE ramps up regardless of the battery voltage.

the ISL95522 starts the switcher after fully turning on ASGATE in the NVDC charger configuration. If V_{BAT} > 3.5V, the BGATE MOSFET remains on for about 28ms after the buck regulator starts switching to prevent the system bus from dropping by a MOSFET body-diode voltage drop caused by the BGATE MOSFET turning off early. This 28ms switching is called precharging switching. During the 28ms, the current that flows into the battery is controlled at 256mA or 128mA based on the current sensing resistor configuration (see Table 20 on page 51). If V_{BAT} < 3.5V, the BGATE MOSFET does not turn on to avoid charging the depleted battery with a large current. The ACOK signal is asserted high after the precharging switching period.

6.5 Adapter Presence Detection and ACOK

ACOK is an open-drain output pin indicating the presence of the adapter and readiness of the adapter to supply power to the system bus. The ISL95522 actively pulls ACOK low in the absence of the adapter.

Use a voltage divider from the adapter voltage to set the ACIN pin voltage. The ISL95522 monitors the ACIN pin voltage to determine the presence of the adapter. When the ACIN pin voltage exceeds 2V (the DCIN pin voltage is higher than the VBAT pin voltage and ASGATE is fully turned on), the ISL95522 allows the external circuit to pull up the ACOK pin. In the NVDC configuration, the ISL95522 allows the external circuit to pull up the ACOK pin after the precharging switching period.

For the buck converter to work properly to charge the battery, select the ACIN pin voltage divider so that the minimum adapter voltage set by the ACIN pin voltage divider is higher than the maximum battery voltage. There is a 163ms delay between the ACIN pin voltage rising above 2V and ASGATE starting to turn on.

Depending on different operation scenarios, the total deglitch time from the ACIN pin voltage rising above 2V to ACOK asserted high varies. For HPB configuration, this deglitch time is about 278ms with the PROG pin resistor reading and about 247ms without the PROG pin resistor reading. For the NVDC configuration, this deglitch time is about 338ms with the PROG pin resistor reading and about 307ms without the PROG pin resistor reading. These typical numbers can have an 11% variation.

6.6 Adapter Overvoltage Protection

If the ACIN voltage exceeds 3.5V, the ISL95522 determines that an adapter overvoltage condition occurred. It turns off the ASGATE MOSFETs to isolate the adapter from the system and deasserts the ACOK signal by pulling it low.

When the ACIN voltage drops below 3.5V, after the 1.3s or 163ms debounce time set by Control2 register Bit<5>, it goes through the ASGATE soft-start to turn on ASGATE.

The adapter OVP function can be disabled through the SMBus Control2 register Bit<8>.

6.7 Power Source Selection

The ISL95522 automatically selects the adapter and/or the battery as the source for system power.

The BGATE pin drives an NFET that connects/disconnects the battery from the system and the switcher.

The ASGATE pin drives a pair of back-to-back common-source NFETs to connect/disconnect the adapter from the system and the battery.

If the adapter is present, the ISL95522 turns on ASGATE to connect the adapter to the system. In the HPB charger configuration, it also turns off BGATE to disconnect the battery from the system when it turns on ASGATE.

If the adapter is absent, the ISL95522 turns off ASGATE and turns on BGATE to connect the battery to the system. If system bus voltage is higher than the battery voltage, the ISL95522 waits until the system bus voltage decays to battery voltage before turning on BGATE to avoid inrush current into the battery.

6.8 Battery Learn Mode

The ISL95522 supports Battery Learn mode, which is used when supplying the system power from the battery, even when the adapter is plugged in, such as calibration of the battery fuel gauge, hence the name “Battery Learn Mode”. The ISL95522 enters Battery Learn mode when it receives the SMBus Control command (see Table 14 on page 41), or when the PROG pin voltage is externally pulled to 5V after POR. It is not possible to pull up the PROG pin to 5V if the PROG pin to GND resistor value is set to 0Ω. The ISL95522 exits Battery Learn mode when it receives the SMBus control command as Table 14 shows, or when the PROG pin voltage is no longer pulled to 5V.

6.9 HPB Charger Battery Learn Mode Entry/Exit

In the HPB charger configuration Battery Learn mode, the ISL95522 turns off ASGATE and turns on BGATE regardless of whether the adapter is present. The Information1 register Bit<1> indicates ASGATE on or off.

Upon entering Battery Learn mode, the ISL95522 turns on BGATE only when the system bus voltage decays to battery voltage to avoid inrush current from system bus to battery.

The three ways of exiting HPB charger configuration Battery Learn mode are:

- SMBus sends the Battery Learn Mode Exit command
- The PROG pin voltage drops below 5V
- The BATGONE pin voltage goes from logic LOW to HIGH

In cases 1 and 2, after the ASGATE turn-on delay of 163ms, the ISL95522 goes through the soft-start process to turn on ASGATE and turn off BGATE as described in “Soft-Start” on page 51.

In case 3, the ISL95522 uses its maximum gate drive strength to turn on ASGATE quickly to prevent system voltage collapse. This action can be completed within ~35µs after the BATGONE pin voltage level goes to logic high. If the soft-start process is still preferred in this case, use SMBus Control1 register Bit<7> to configure the preference.

6.10 NVDC Charger Battery Learn Mode Entry/Exit

In the NVDC charger configuration Battery Learn mode, the ISL95522 turns on BGATE and keeps ASGATE on but turns off the switcher regardless of whether the adapter is present.

Upon entering Battery Learn mode, the ISL95522 turns on BGATE only when the system bus voltage decays to battery voltage to avoid inrush current from system bus to battery.

The three ways of exiting the NVDC charger configuration Battery Learn mode are the same as for HPB charger configuration Battery Learn mode listed as follows:

- SMBus sends the Battery Learn Mode Exit command
- The PROG pin voltage drops below 5V
- The BATGONE pin voltage goes from logic LOW to HIGH

In all these cases, the ISL95522 resumes switching immediately to supply power to the system bus from the adapter to prevent system voltage collapse.

6.11 Hardware-Based Adapter Current Limit

The ACLIM pin voltage set hardware-based adapter current limit provides an extra level of protection in the unlikely event of an SMBus communication failure.

Equation 1 gives the relationship between the ACLIM pin voltage and the hardware-based adapter current limit, where $V_{ACLIMHW}$ is the ACLIM pin voltage in volts and $I_{ACLIMHW}$ is the hardware-based adapter current limit in amperes.

(EQ. 1)
$$I_{ACLIMHW} = \frac{V_{ACLIMHW}}{32 \times Rs1}$$

Equation 1 is true for all current sensing resistor configurations.

The ISL95522 uses the lower value of the hardware-set adapter current limit and the SMBus programmed adapter current limit as the actual adapter current limit.

The ACLIM pin voltage also sets the ASGATE soft-start current limit level from t2 to t3. The ACLIM current limit function can be disabled through SMBus Control2 register Bit<13> after ACOK assertion, so that the ACLIM pin is used only for the ASGATE soft-start current limit from t2 to t3 as shown in "Soft-Start" on page 51.

6.12 HPB Charger Turbo Mode Support

Turbo mode means that the system draws more power than the adapter's power rating. It prompts the need for the switcher to change from Forward Buck mode of operation to Reverse-Boost mode of operation to reverse the energy flow. Such mode of operation enables the battery to help the adapter provide the required system power. This type of operation has been widely used in many systems, such as "Sun mode" and "Eclipse mode" for bidirectional battery charger/discharger used on satellites with solar panels as the power source acting as the adapter (reference: "A zero voltage switching bidirectional battery charger/discharger for the NASA EOS Satellite", Dan M. Sable, Fred C. Lee and Bo H. Cho, APEC 1992 Conference Proceedings).

In the HPB charger configuration, the ISL95522 normally operates the switcher as a synchronous buck converter with diode emulation. When the buck converter is in light-load condition, it enters DCM operation with reduced switching frequency to increase efficiency. From the description of the R3 modulator operational principle, the COMP pin voltage is lower at lighter loads and can reach the low clamp.

In Turbo mode, the ISL95522 operates the switcher in Reverse-Boost mode to boost energy from the battery to the adapter voltage rail, so the adapter current is limited at the adapter current limit set point while the battery supplies the additional power required by the system.

The Control1 register Bit<10> enables/disables the Turbo/Boost function. See Table 14 on page 41 for details.

The ISL95522 enters Turbo mode when all of the following criteria are met:

- Adapter current is within 80mA of AdapterCurrentLimit1 (or AdapterCurrentLimit2 if two-level adapter current limit function is enabled) register setting
- Battery charging current is less than 150mA
- COMP pin voltage is lower than 1.4V

Meeting these criteria means that the ISL95522 enters Turbo mode precisely only when absolutely necessary. For example, assume the adapter voltage is 20V, the adapter current limit is 4A (80W rating) and the ISL95522 is charging an 8V battery at a 5A rate (40W charging power). If the system load increases from 0W to 79W instantaneously, the adapter current increases from 2A to 5.95A instantaneously, exceeding the 4A current limit level. However, the adapter current loop takes control and decreases the charging current to limit the adapter current at 4A, eventually providing 79W of system power and 1W of battery charging power. In this case, the ISL95522 does not need to enter Turbo mode for the adapter to conserve battery energy. In the same example, if the system load increases from 0W to 81W instantaneously, the adapter current increases from 2A to 6.05A instantaneously, exceeding the 4A current limit level. The adapter current loop takes control and decreases the charging current to limit the adapter current at 4A. Thus, the ISL95522 eventually determines that it needs to enter Turbo mode so the adapter provides 80W and the battery provides 1W to provide 81W to the system.

The interaction of the control loops within the ISL95522, including the adapter current loop, the charging current loop, and the battery full charging voltage loop, determines the timing of the Turbo mode entry. The timing strongly depends on the control loop compensation design and the interaction among the loops. In the previous example, compared with system power instantaneously increasing from 0W to 81W, system power instantaneously increasing from 0W to 160W causes the ISL95522 to enter Turbo mode much faster because the loops drive the circuit parameters to meet the three Turbo mode entry criteria much more quickly when the adapter is more severely overloaded.

The ISL95522 exits Turbo mode when one of the following criteria are met:

- Battery charging current exceeds 150mA (R_{s2} = 10mΩ).
- Adapter current is less than AdapterCurrentLimit register setting and COMP voltage is lower than 1.4V.
- Battery discharging current is less than 140mA (for R_{s2} = 10mΩ) for 140ms.

Table 21 shows the ISL95522 HPB configuration charge function and Turbo/Boost function control truth table.

Table 21. HPB Charger Behavior Truth Table

Turbo/Boost Mode Control Bit	EnableCharging Control Bit	ChargeCurrent Register		
0 = Enable Boost 1 = Disable Boost	**0 = Disable Charging 1 = Enable Charging**	**0 = 0A Command 1 = Non-Zero Valid Command**	**Charge?**	**Boost?**
0	0	0	No	Yes
0	0	1	No	Yes
0	1	0	No	Yes
0	1	1	Yes (Fast charge and trickle charge enabled)	Yes
1	0	0	No	No
1	0	1	No	No
1	1	0	No	No
1	1	1	Yes (Fast charge and trickle charge enabled)	No

Table 22. NVDC Charger Behavior Truth Table

Turbo/Boost Mode Control Bit	EnableCharging Control Bit	ChargeCurrent Register	BGATE On/off	
0 = Enable Turbo 1 = Disable Turbo	**0 = Disable Charging 1 = Enable Charging**	**0 = 0A Command 1 = Non-Zero Valid Command**	**System Load Not In Turbo Mode Range**	**System Load In Turbo Mode Range**
0	0	0	Off	On
0	0	1	Off	On
0	1	0	Off	On
0	1	1	On for fast charge; trickle charge enabled	On
1	0	0	Off	Off
1	0	1	Off	Off
1	1	0	Off	Off
1	1	1	On for fast charge; trickle charge enabled	On

6.13 NVDC Charger Turbo Mode Support

In the NVDC charger configuration and Turbo mode, the ISL95522 turns on the BGATE FET to limit the adapter current at the adapter current limit set point, while the battery supplies the rest of the power required by the system. To turn on BGATE in Turbo mode, the CSON pin voltage needs to be 175mV lower than the VBAT pin voltage. If the ISL95522 detects 150mA charging current or if the battery discharging current is less than 140mA for 140ms, it turns off BGATE to exit Turbo mode. See Table 22 for information about BGATE operation.

If the adapter current reaches the AdapterCurrentLimit1 register set value (or the AdapterCurrentLimit2 register set value, if two-level adapter current limit function is enabled), or the adapter input voltage drops to the Input Voltage

Regulation Reference set by Input Voltage Register 0x40H, the ISL95522 limits the input power by regulating the adapter current at the AdapterCurrentLimit1/2 register set value, or by regulating the adapter voltage at the Input Voltage Regulation Reference point.

6.14 Two-Level Adapter Current Limit

In a real system, a Turbo event usually does not last very long. It is often no longer than milliseconds, a time length during which the adapter can supply current higher than its DC rating. The ISL95522 employs two-level adapter current limit to take full advantage of adapter's surge capability and minimize the power draw from the battery.

Figure 43 shows the two SMBus-programmable adapter current limit levels, AdapterCurrentLimit1 and AdapterCurrentLimit2, as well as the durations t1 and t2. The two-level adapter current limit function is initiated when the adapter current reaches the AdapterCurrentLimit1 register setting. It starts at AdapterCurrentLimit2 for t2 duration, then changes to AdapterCurrentLimit1 for t1 duration before repeating the pattern. These parameters can set adapter current limit with an envelope that allows the adapter to temporarily output surge current without requiring the charger to enter Turbo mode. This operation maximizes battery life.

AdapterCurrentLimit1's register value can be higher or lower than AdapterCurrentLimit2's value.

The two-level adapter current limit function can be enabled and disabled through SMBus Control2 register Bit<6>. When the two-level adapter current limit function is disabled, only AdapterCurrentLimit1's value is used as the adapter current limit and AdapterCurrentLimit2's value is ignored.

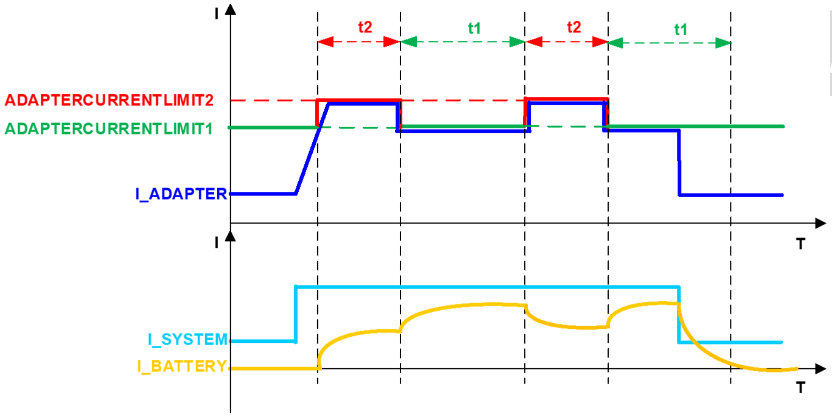


Figure 43. Two-Level Adapter Current Limit

6.15 Current Monitor

The ISL95522 provides an adapter current monitor through the AMON pin and a battery discharging current monitor through the BMON pin. The AMON pin voltage is 32x the (V_{CSIP}-V_{CSIN}) voltage and the BMON pin voltage is 32x the (V_{CSON}-V_{CSOP}) voltage.

The AMON and BMON functions can be enabled or disabled through SMBus Control1 register Bit<2> and Bit<3> respectively, as Table 14 on page 41 shows.

6.16 PSYS Monitor

The ISL95522 PSYS pin provides a measure of the instantaneous power consumption of the entire platform. The PSYS pin outputs a current source described by Equation 2.

(EQ. 2)
$$I_{PSYS} = K_{PSYS} \times (V_{ADP} \times I_{ADP} + V_{BAT} \times I_{BAT})$$

K_{PSYS} is based on the current sensing resistors R_{s1} and R_{s2} configurations and is selectable through SMBus Control2 register Bit<9>. See Table 19 for details. V_{ADP} is the adapter voltage in volts, I_{ADP} is the adapter current in Amperes, V_{BAT} is the battery voltage, and I_{BAT} is the battery discharging current. When the battery is discharging, I_{BAT} is a positive value; when the battery is charging, I_{BAT} is a negative value. The battery voltage V_{BAT} is detected through the CSON pin to maximize the power monitor accuracy in NVDC configuration Trickle Charge mode.

The PSYS information includes the power loss of the charger circuit and the actual power delivered to the system. Resistor R_{PSYS} connected between the PSYS pin and GND converts the PSYS information from current to voltage.

The PSYS function can be enabled or disabled through SMBus Control1 register Bit<4> as shown in Table 14.

6.17 Charger Timeout

The ISL95522 includes a timer to ensure the SMBus master is active and to prevent overcharging the battery. The ISL95522 terminates charging if the charger has not received a write to the MaxChargeVoltage or ChargeCurrent register within 175s. If a time-out occurs, MaxChargeVoltage or ChargeCurrent register must be written to re-enable charging.

The ISL95522 allows you to disable the charger timeout function through SMBus Control1 register Bit<15> as Table 14 shows.

6.18 Trickle Charging

The ISL95522 supports trickle charge to an overly discharged battery. It can activate the trickle charge function when the battery voltage is lower than the MinChargeVoltage setting. The VBAT pin is the battery voltage sense point for Trickle Charge mode.

To enable trickle charge, set the EnableCharging control bit to ‘1’ and set the ChargeCurrent register to a valid non-zero value. To disable trickle charge, either set the EnableCharging control bit to ‘0’ or set the ChargeCurrent register to ‘0’. Table 21 on page 56 shows the condition to enable HPB configuration Trickle Charge mode. Table 22 shows the condition to enable the NVDC configuration Trickle Charge mode.

The trickle charging current can be programmed to be 256mA or 128mA through SMBus Control2 register Bit<7> as shown in Table 15 on page 43.

In the HPB charger configuration, the ISL95522 charges the battery at 256mA or 128mA in Trickle Charge mode.

In the NVDC charger configuration Trickle Charge mode, the ISL95522 regulates the system voltage at 450mV above the MinChargeVoltage register value. An independent control loop regulates BGATE FET gate voltage to regulate the battery charging current at 256mA or 128mA.

When the battery voltage is charged to 175mV above MinChargeVoltage register value, the ISL95522 enters Fast Charging mode by limiting the charging current at the ChargeCurrentLimit register setting.

The ISL95522 CSON pin sinks about 20µA current and the CSOP pin sinks about 35µA current to provide the bias power for the battery current sensing amplifier. If there is a resistor series in CSON pin, the voltage drop on this resistor creates a small offset so that the actual battery charging current becomes slightly smaller. If there is a resistor series in the CSOP pin, the voltage drop on this resistor creates a small offset so that the actual battery charging current becomes slightly larger. These two resistors can be used to slightly tweak the actual battery charging current.

6.19 NVDC Charger System Voltage Regulation

If the battery is absent, the ISL95522 regulates the system bus voltage at the higher value of 7.168V and the MinChargeVoltage register setting.

If the battery is present but BGATE is turned off, the ISL95522 regulates the system bus voltage at the higher value of 7.168V and the MaxChargeVoltage register setting.

The CSON pin senses the system bus voltage.

When the battery is absent, the ISL95522 does not limit the adapter current if the system power draw causes the adapter current to exceed the adapter current limit. This function prevents system voltage collapse and can be enabled or disabled through SMBus Control2 register Bit<4>.

6.20 Charging Current WOCP

The ISL95522 provides Way-Overcurrent Protection (WOCP) for the current flowing into the battery against the high-side MOSFET short and inductor short scenarios. It employs the CCLIM pin to set the WOCP threshold. The ISL95522 monitors the CSOP-CSON voltage and compares it with the WOCP threshold. When the WOC comparator is tripped, it either terminates the PWM switching pulse or turns off ASGATE and deasserts ACOK. This is configurable through SMBus Control1 register Bit<11>.

If the WOC comparator is tripped when the WOCP function is enabled through Control1 register Bit<11>, the ISL95522 counts once within every 20µs. Whenever the ISL95522 counts to seven times in 656ms, it turns off ASGATE and deasserts ACOK immediately. After the 1.3s or 163ms debounce time set by Control2 register Bit<5>, it goes through the ASGATE soft-start to retry.

When the WOCP function is disabled through Control1 register Bit<11>, as long as the WOC comparator is tripped within every 20µs, it terminates the PWM switching pulse immediately for the remainder of the 20µs.

The CCLIM pin voltage sets the charging current WOCP threshold. Equations 3 and 4 give the relationship between the CCLIM pin voltage and the WOCP threshold, where $V_{CCLIMHW}$ is the CCLIM pin voltage in volts and I_{WOCP} is the WOCP threshold in amperes.

(EQ. 3)
$$I_{WOCP} = 1.23 \times \frac{V_{CCLIMHW}}{64 \times R_{s2}}$$

Equation 3 is true for R_{s1}: R_{s2} = 2:1 (R_{s1} = 10mΩ and R_{s2} = 5mΩ or R_{s1} = 20mΩ and R_{s2} = 10mΩ).

(EQ. 4)
$$I_{WOCP} = \frac{V_{CCLIMHW}}{32 \times R_{s2}}$$

Equation 4 is true for R_{s1}: R_{s2} = 1:1 (R_{s1} = 10mΩ and R_{s2} = 10mΩ or R_{s1} = 20mΩ and R_{s2} = 20mΩ).

The WOC comparator monitors the peak current crossing the battery current sensing resistor R_{s2}, so the WOCP threshold needs to be set at least half of the inductor ripple current higher than the SMBus-programmed charging current command to avoid false tripping in normal charging.

For the WOCP function to work properly, it needs to connect an RC filter from the CSON pin to ground to increase the overcurrent detection sensitivity. This RC filter time constant should be selected carefully and cannot be too large, otherwise the WOCP can be falsely tripped by the current overshoot flowing into the battery when the ISL95522 exits Turbo mode after system bus load release. Meanwhile, the WOCP threshold should be set high enough to avoid the false trip by the current overshoot flowing into the battery.

The current spike flowing into the battery can cause a voltage spike at the battery connector due to the battery current path impedance. For the NVDC charger, pay attention to this voltage spike at the VBAT pin to avoid tripping the battery 4.6V/cell OVP function, otherwise the BGATE FET turns off due to the battery OVP so that the current flowing on R_{s2} is gone. Renesas recommends adding an RC filter at VBAT in this scenario.

6.21 Over-Temperature Protection

The ISL95522 turns off the internal LDO for self-protection when the junction temperature exceeds +155°C. The internal LDO stays off until the junction temperature falls below +128°C.

In the HPB charger configuration, the ISL95522 puts the charger in Standby mode after declaring over-temperature protection.

In the NVDC charger configuration, the ISL95522 stops switching after declaring over-temperature protection.

When the temperature falls below +128°C, the ISL95522 enables the internal LDO and resumes operation.

6.22 Battery Overvoltage Protection

The battery overvoltage protection function prevents the battery from being overcharged.

In the HPB charger configuration, the ISL95522 stops switching if the battery voltage is higher than the MaxChargeVoltage register setting. If the battery voltage is higher than 4.6V/cell, it stops charging.

In the NVDC charger configuration, the ISL95522 stops switching if the system bus voltage is higher than the MaxChargeVoltage register value; if the battery voltage is higher than 4.6V/cell, it turns off BGATE to stop charging.

The MaxChargeVoltage register setting should be less than 4.6V/cell.

6.23 System Bus Short-Circuit Detection

If the ACIN pin is pulled below 2V by the system bus excessive current or short-circuit, the ISL95522 turns off ASGATE to isolate the adapter from the system bus. When the ACIN pin voltage rises above 2V again and after 163ms delay, ASGATE turns on again with soft-start.

Figure 44 shows how an external circuit can detect the system bus short-circuit. If the system bus is short-circuited, the ACIN pin is pulled below 2V by diode D_1, so ASGATE cannot turn on. While in normal operation, ASGATE can still turn on when the system bus is charged up above 2V through D_1.

In normal operation, to charge up the system bus above 2V through D_1 quickly, the ACIN pin voltage divider resistor values need to be small, which in sequence causes a larger constant power consumption on the ACIN pin voltage divider resistors. Two optional circuits shown in Figure 44 can be dedicated to charge up the system bus. Renesas recommends using circuit Option 1 for HPB configuration and circuit Option 2 for NVDC configuration.

For circuit Option 2, the R_3 and R_4 voltage divider voltage (for example, the Q_1 gate voltage) needs to be 2V higher than the Q_1 gate source threshold voltage, so that Q_1 can be turned on and the system bus can be charged up above 2V through R_2 and Q_1. Meanwhile, the R_3 and R_4 voltage divider voltage needs to be less than the final system bus voltage so that Q_1 can be turned off in normal operation to avoid the leakage current through Q_1. D_3 can be used to block the leakage current from the system bus to the adapter side through the Q_1 body diode in Battery Only mode.

Note that leakage current through R_1 and D_2 occurs in circuit Option 1 when the adapter voltage is higher than the system bus voltage, such as in Learn mode in the NVDC configuration.

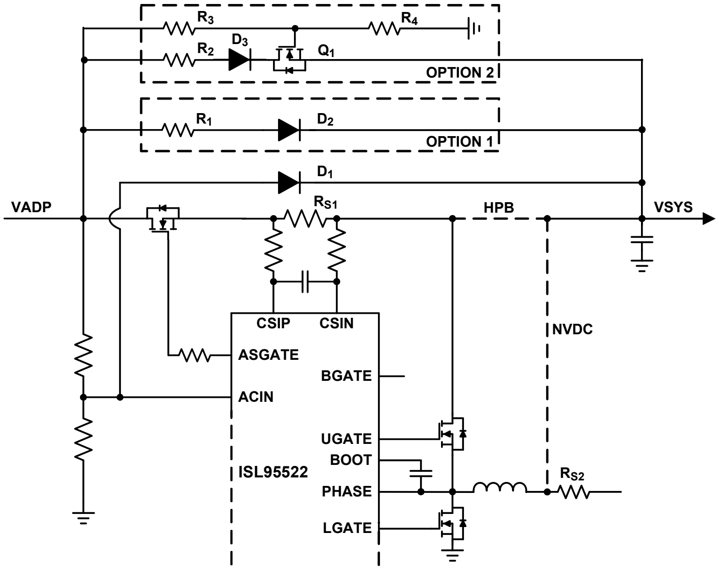


Figure 44. External System Bus Short Detection Circuit

6.24 Adapter Input Filter

The adapter cable parasitic inductance and capacitance can cause some voltage ring or overshoot spike at the adapter connector node when the adapter is hot plugged in. This voltage spike can damage the ASGATE MOSFET or the ISL95522 pins connecting to the adapter connector node. One low cost solution is to add an RC snubber circuit at the adapter connector node to clamp the voltage spike as shown in Figure 45. A practical value of the RC snubber is 2.2Ω to 2.2µF, while the appropriate values and power rating should be carefully characterized based on the actual design. Do not add a pure capacitor at the adapter connector node, which can cause an even larger voltage spike due to the adapter cable or the adapter current path parasitic inductance.

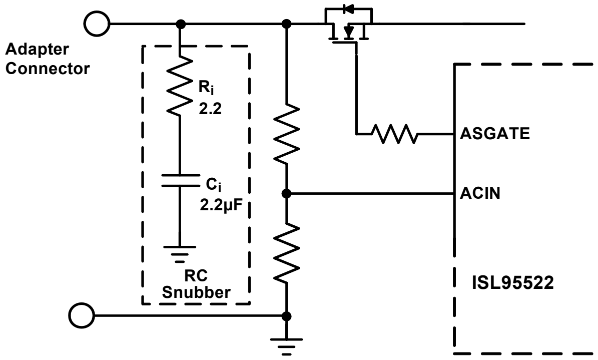


Figure 45. Adapter Input RC Snubber Circuit

6.25 Test with e-Load Constant Voltage Mode

An electronic load in Constant Voltage mode (e-Load in CV mode) is often used to emulate a battery in testing a battery charger. However, an e-Load in CV mode does not accurately emulate the characteristics of a real battery, particularly the ESR. Such discrepancy can result in a much more exaggerated output voltage switching ripple observed by the battery charger and present inaccurate test results. Renesas recommends adding a capacitor, such as 680µF, at the terminal of the e-Load to better match the impedance of a real battery, so that the test result better represents that with a real battery. As a precaution for potentially testing with an e-load with large ESR, Renesas recommends adding an RC filter at the VBAT pin to smooth the switching ripple observed by the ISL95522. The recommended range of the RC time constant is 200µs to 1ms.

7. General Application Information

This design guide provides a high-level explanation of the steps necessary to design a single-phase power converter. It is assumed that the reader is familiar with many of the basic skills and techniques referenced in the following section. In addition to this guide, Renesas provides complete reference designs that include schematics, bills of materials, and example board layouts.

7.1 Select the LC Output Filter

The duty cycle of an ideal buck converter in CCM is a function of the input and the output voltage. This relationship is written by Equation 5:

(EQ. 5)
$$D = \frac{V_{OUT}}{V_{IN}}$$

The output inductor peak-to-peak ripple current is written by Equation 6:

(EQ. 6)
$$I_{P\text{-}P} = \frac{V_{OUT} \cdot (1 - D)}{f_{SW} \cdot L}$$

A typical step-down DC/DC converter has an $I_{P\text{-}P}$ of 20% to 40% of the maximum DC output load current for a practical design. The value of $I_{P\text{-}P}$ is selected based upon several criteria such as MOSFET switching loss, inductor core loss, and the resistive loss of the inductor winding.

The DC copper loss of the inductor can be estimated by Equation 7:

(EQ. 7)
$$P_{COPPER} = I_{LOAD}^{2} \cdot DCR$$

where I_{LOAD} is the converter output DC current.

The copper loss can be significant, so pay attention to the DCR selection. Another factor to consider when choosing the inductor is its saturation characteristics at elevated temperatures. A saturated inductor can destroy circuit components.

A DC/DC buck regulator must have output capacitance C_O into which ripple current $I_{P\text{-}P}$ can flow. Current $I_{P\text{-}P}$ develops a corresponding ripple voltage $V_{P\text{-}P}$ across $C_{O,}$ which is the sum of the voltage drop across the capacitor ESR and of the voltage change stemming from charge moved in and out of the capacitor.

These two voltages are written by Equation 8 and Equation 9:

(EQ. 8)
$$\Delta V_{ESR} = I_{P\text{-}P} \cdot ESR$$

(EQ. 9)
$$\Delta V_C = \frac{I_{P\text{-}P}}{8 \cdot C_O \cdot f_{SW}}$$

If the output of the converter has to support a load with high pulsating current, several capacitors need to be paralleled to reduce the total ESR until the required $V_{P\text{-}P}$ is achieved. The inductance of the capacitor can cause a brief voltage dip if the load transient has an extremely high slew rate. Low inductance capacitors should be considered in this case. A capacitor dissipates heat as a function of RMS current and frequency. Be sure that $I_{P\text{-}P}$ is shared by a sufficient quantity of paralleled capacitors so that they operate below the maximum rated RMS current at f_{SW}. Note that the rated value of a capacitor can fade as much as 50% as the DC voltage across it increases.

7.2 Select the Input Capacitor

The important parameters for the input capacitance are the voltage rating and the RMS current rating. For reliable operation, select capacitors with voltage and current ratings above the maximum input voltage and that are capable of supplying the RMS current required by the switching circuit. Their voltage rating should be at least 1.25x greater than the maximum input voltage, while a voltage rating of 1.5x is a preferred rating. Figure 46 on page 63 is a graph of the input capacitor RMS ripple current, normalized relative to output load current, as a function of duty cycle and is adjusted for converter efficiency. The normalized RMS ripple current calculation is written as Equation 10:

$$I_{C_{IN}(RMS,NORMALIZED)} = \frac{I_{MAX} \cdot \sqrt{D \cdot (1 - D) + \frac{D \cdot k^2}{12}}}{I_{MAX}} \quad \text{(EQ. 10)}$$

where:

- I_{MAX} is the maximum continuous I_{LOAD} of the converter
- k is a multiplier (0 to 1) corresponding to the inductor peak-to-peak ripple amplitude expressed as a percentage of I_{MAX} (0% to 100%)
- D is the duty cycle that is adjusted to take into account the efficiency of the converter, which is written as Equation 11:

$$D = \frac{V_{OUT}}{V_{IN} \cdot EFF} \quad \text{(EQ. 11)}$$

In addition to the capacitance, some low ESL ceramic capacitance is recommended to decouple between the drain of the high-side MOSFET and the source of the low-side MOSFET.

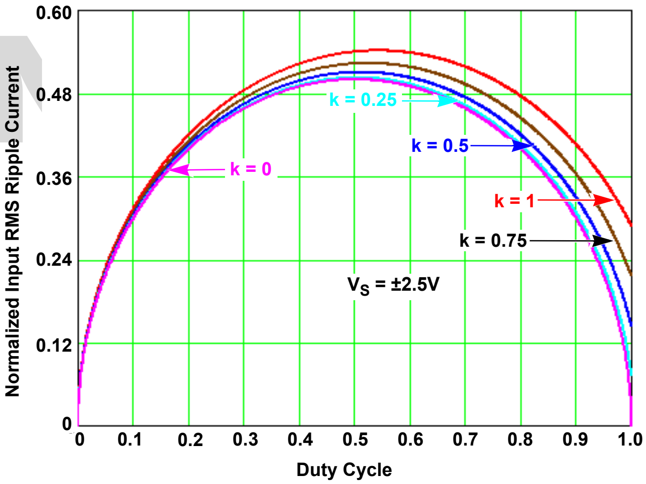


Figure 46. Normalized RMS Input Current at EFF = 1

7.3 Select the Switching Power MOSFET

Typically, MOSFETs cannot tolerate even brief excursions beyond their maximum drain-to-source voltage ratings. The MOSFETs used in the power stage of the converter should have a maximum VDS rating that exceeds the sum of the upper voltage tolerance of the input power source and the voltage spike that occurs when the MOSFET switches off.

Several power MOSFETs optimized for DC/DC converter applications are readily available. The preferred high-side MOSFET emphasizes low gate charge so that the device spends the least amount of time dissipating power in the linear region. Unlike the low-side MOSFET, which has the drain-to-source voltage clamped by its body diode during turn off, the high-side MOSFET turns off with a VDS of approximately V_{IN}-V_{OUT}, plus the spike across it. The preferred low-side MOSFET emphasizes low $r_{DS(ON)}$ when fully saturated to minimize conduction loss. Note that this is an optimal configuration of MOSFET selection for low duty cycle applications (D < 50%). For higher output, low input voltage solutions, a more balanced MOSFET selection for high-side and low-side devices may be warranted.

The Low-Side (LS) MOSFET's power loss can be assumed to be conductive only and is written as Equation 12:

(EQ. 12) $$P_{CON\_LS} \approx I_{LOAD}^{2} \cdot r_{DS(ON)\_LS} \cdot (1 - D)$$

The High-Side (HS) MOSFET's conduction loss is written by Equation 13:

(EQ. 13) $$P_{CON\_HS} = I_{LOAD}^{2} \cdot r_{DS(ON)\_HS} \cdot D$$

The HS MOSFET's switching loss is written as Equation 14:

(EQ. 14) $$P_{SW\_HS} = \frac{V_{IN} \cdot I_{VALLEY} \cdot t_{ON} \cdot f_{SW}}{2} + \frac{V_{IN} \cdot I_{PEAK} \cdot t_{OFF} \cdot f_{SW}}{2}$$

where:

- I_{VALLEY} is the difference of the DC component of the inductor current minus 1/2 of the inductor ripple current
- I_{PEAK} is the sum of the DC component of the inductor current plus 1/2 of the inductor ripple current
- t_{ON} is the time required to drive the device into saturation
- t_{OFF} is the time required to drive the device into cut-off

Renesas recommends using a 2.2µF (10V) VDD/VDDP capacitor, which has an effective capacitance higher than 0.4µF at 5V and x1.6 effective cap at the BOOT pin at 5V.

7.4 Select the Bootstrap Capacitor

The selection of the bootstrap capacitor is written by Equation 15:

(EQ. 15) $$C_{BOOT} = \frac{Q_g}{\Delta V_{BOOT}}$$

where:

- Q_g is the total gate charge required to turn on the HS MOSFET
- ΔV_{BOOT}, is the maximum allowed voltage decay across the boot capacitor each time the HS MOSFET is switched on

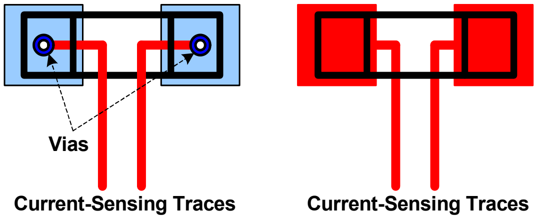
As an example, suppose the HS MOSFET has a total gate charge Q_g, of 25nC at VGS = 5V and a ΔV_{BOOT} of 200mV. The calculated bootstrap capacitance is 0.125µF; for a comfortable margin, select a capacitor that is double the calculated capacitance. In this example, 0.22µF will suffice. Use an X7R or X5R ceramic capacitor.

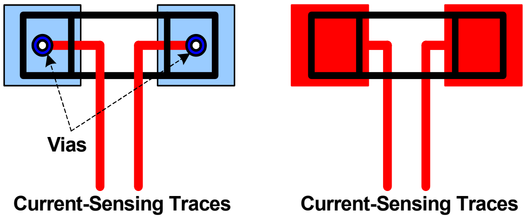
Renesas recommends using a bootstrap capacitor of 0.47µF (25V), which has an effective capacitance higher than 0.25µF at 5V and x50 effective high-side MOSFET gate capacitance.

7.5 Select the DCIN Filter

An RC filter is connected at the DCIN pin. Renesas recommends connecting a 10Ω DCIN resistor between the DCIN pin and the VADP/VSYS diodes, and connecting a 4.7µF (50V) DCIN capacitor to GND, which has an effective capacitance higher than 0.4µF at 20V.

8. Layout Guidelines

Pin #	Symbol	Layout Guidelines
Bottom Pad	GND	Connect this ground pad to the ground plane through the low impedance path. Renesas recommends using at least five vias to connect to the ground planes in the PCB to ensure sufficient thermal dissipation directly under the IC.
1	CSON	Run two dedicated traces with sufficient width in parallel (close to each other to minimize the loop area) from the two terminals of the battery current sensing resistor to the IC. Place the differential-mode and common-mode RC filter components in the general proximity of the controller. Route the current sensing traces through vias to connect the center of the pads; or route the traces into the pads from the inside of the current sensing resistor. The following drawings show the two preferred ways of routing current sensing traces. 
2	CSOP	
3	FSET	Place the FSET programming resistor in the general proximity of the controller.
4	QPCP	Place the charge pump flying capacitor in the general proximity of the controller. Route traces with sufficient width.
5	CMSRC	Run these two traces in parallel fashion with sufficient width.
6	QPCN	Place the charge pump flying capacitor in the general proximity of the controller. Route traces with sufficient width.
7	ASGATE	Run these two traces in parallel fashion with sufficient width.
8	VDDP	Place the decoupling capacitor in the general proximity of the controller.
9	LGATE	Run LGATE trace in parallel with UGATE and PHASE traces on the same PCB layer. Use sufficient width. Avoid any sensitive analog signal trace from crossing over or getting close.
10	PHASE	Run these two traces in parallel fashion with sufficient width. Avoid any sensitive analog signal trace from crossing over or getting close. Renesas recommends routing the PHASE trace to the high-side MOSFET source pin instead of general copper. Place the IC close to the switching MOSFET's gate terminals and keep the gate drive signal traces short for a clean MOSFET drive. The IC can be placed on the opposite side of the switching MOSFETs. Place the input capacitors as close as possible to the switching high-side MOSFET drain and the low-side MOSFET source and use shortest PCB trace connection. Place these capacitors on the same PCB layer as the MOSFETs. Do not place the capacitors on different layers and use vias to make the connection. Place the inductor input terminal to the switching high-side MOSFET drain and low-side MOSFET source terminal as close as possible. Minimize this phase node area to lower the electrical and magnetic field radiation but make this phase node area large enough to carry the current. Place the inductor and the switching MOSFETs on the same layer of the PCB.
11	UGATE	
12	BOOT	Place the bootstrap capacitor in the general proximity of the controller. Use a sufficiently wide trace. Avoid any sensitive analog signal trace from crossing over or getting close.
13	NTC	Place the resistor series with the NTC thermistor in the general proximity of the controller. Place the NTC thermistor at the point where the temperature is to be monitored. Note: if the NTC thermistor is too close to the switching components, it can couple the switching noise to the NTC pin.

Pin #	Symbol	Layout Guidelines
14	CSIN	Place the battery current sensing resistor immediately next to the inductor output. Run two dedicated traces with sufficient width in parallel (close to each other to minimize the loop area) from the two terminals of the adapter current sensing resistor to the IC. Place the differential-mode and common-mode RC filter components in the general proximity of the controller. Route the current sensing traces through vias to connect the center of the pads; or route the traces into the pads from the inside of the current sensing resistor. The following drawings show the two preferred ways of routing current sensing traces. 
15	CSIP	
16	ACIN	Place the voltage divider resistors and the optional decoupling capacitor in the general proximity of the controller.
17	DCIN	Place the OR diodes and the RC filter in the general proximity of the controller.
18	VDD	Place the RC filter from the VDDP pin in the general proximity of the controller.
19	PROG	Place the PROG programming resistor in the general proximity of the controller.
20	ACLIM	Place the ACLIM voltage divider resistors in the general proximity of the controller.
21	SDA	No special consideration.
22	SCL	
23	PROCHOT#	
24	ACOK	
25	BATGONE	Place the 100kΩ resistor series in the BATGONE signal trace and the optional decoupling capacitor in the general proximity of the controller.
26	CCLIM	Place the CCLIM voltage divider resistors in the general proximity of the controller.
27	BMON	No special consideration. Place the optional RC filter in the general proximity of the controller.
28	COMP	Place the compensation components in the general proximity of the controller.
29	AMON	No special consideration. Place the optional RC filter in the general proximity of the controller.
30	PSYS	No special consideration.
31	VBAT	Place the RC filter in the general proximity of the controller. Run a dedicated trace from the battery positive connection point to the IC. In HPB configuration, separate this trace with the trace connecting the CSON pin.
32	BGATE	Use sufficient width trace from the IC to the BGATE MOSFET gate.

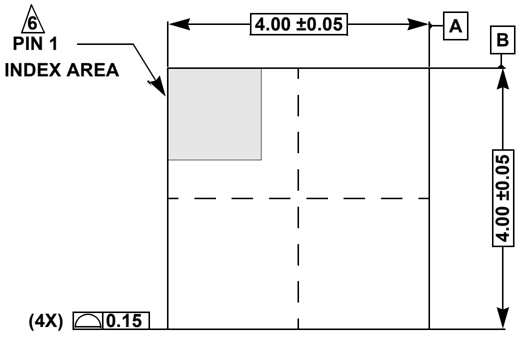
9. Revision History

Date	Revision	Description
Jul 14, 2023	2.01	Removed related literature section. Updated the ordering information table.
Jul 9, 2019	2.00	Updated links throughout. Corrected tech brief reference in Note 3. Updated the VDDP, BOOT, VDD, and DCIN pin descriptions. Updated second sentence in the SMBus Transactions section on page 32 by changing “1001100” to “0001001”. Added the last paragraph in the Select the Switching Power MOSFET and Select the Bootstrap Capacitor sections on page 64. Added the Select the DCIN Filter section on page 64.
Jun 21, 2018	1.00	Changed θ_{JA} from 39 to 41 and θ_{JC} from 3 to 5 on page 13. Updated Figure 15 on page 27. Fixed a typo in Figure 23 on page 29.
May 17, 2018	0.00	Initial release.

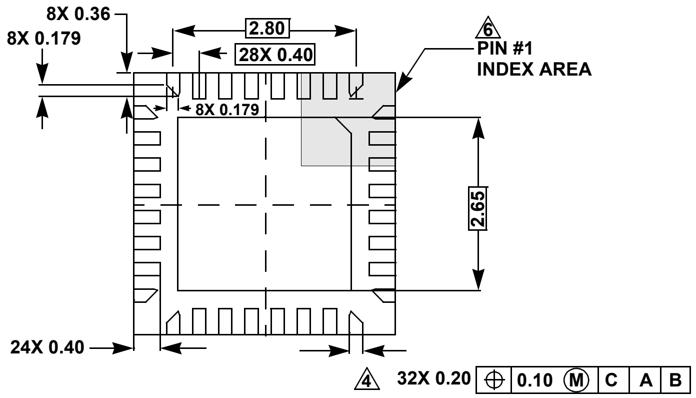
10. Package Outline Drawing

For the most recent package outline drawing, see L32.4x4A.

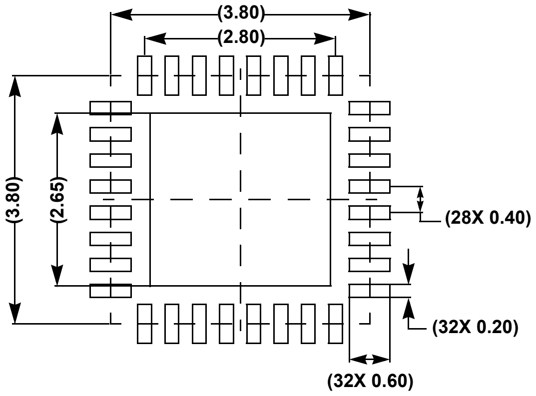
L32.4x4A
32 Lead Quad Flat No-Lead Plastic Package
Rev 5, 2/16



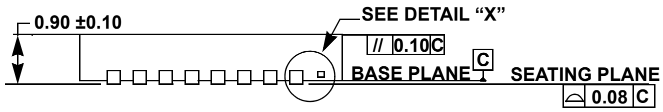
TOP VIEW



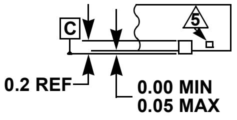
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ±0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.25mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

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