ISL9238

Buck-Boost Narrow VDC Battery Charger with SMBus Interface and USB OTG

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The ISL9238 is a buck-boost Narrow Output Voltage DC (NVDC) charger. The ISL9238 provides the NVDC charging, system bus regulation and protection features for tablet, Ultrabook, notebook, power bank, and any USB-C interface platform. The advanced Renesas R3™ Technology provides high light-load efficiency and fast transient response.

In Charging mode, the ISL9238 takes input power from a wide range of DC power sources (such as conventional AC/DC charger adapters, USB PD ports, and travel adapters) and safely charges battery packs with up to 4-series cell Li-ion batteries.

As a NVDC topology charger, it also regulates the system output to a narrow DC range for stable system bus voltage. The system power can be provided from the adapter, battery, or a combination of both. The ISL9238 can operate with only a battery, only an adapter, or both connected. For Intel IMVP8 compliant systems the ISL9238 includes System Power monitor (PSYS) functionality, which provides an analog signal representing total platform power. The PSYS output connects to a wide range of IMVP8 core regulators to provide an IMVP8 compliant power domain function.

The ISL9238 supports reverse buck, boost, or buck-boost operation to input port from 2- to 4-cell batteries.

The ISL9238 has serial communication using SMBus/I^2C that allows programming of many critical parameters to deliver a customized solution.

Related Literature

For a full list of related documents, visit our website:

- ISL9238 device page

Features

- Buck-boost NVDC charger for 1-, 2-, 3-, or 4-cell Li-ion batteries
- Input voltage range 3.2V to 23.4V (no dead zone)
- System output voltage 2.4V to 18.304V
- Autonomous charging option (automatic end of charging)
- System power monitor PSYS output, IMVP compliant
- Up to 1MHz switching frequency
- Adapter current and battery current monitor (AMON/BMON)
- PROCHOT# open-drain output, IMVP compliant
- Allows trickle charging of depleted battery
- Ideal diode control in Turbo mode
- Reverse buck, boost, and buck-boost operation from battery
- Two-level adapter current limit available
- Battery Ship mode option
- SMBus and auto-increment I^2C compatible
- 4x4 32 Ld TQFN package

Applications

- 1 to 4-cell tablet, Ultrabook, notebook, power bank, and any USB-C interface portable device requiring batteries

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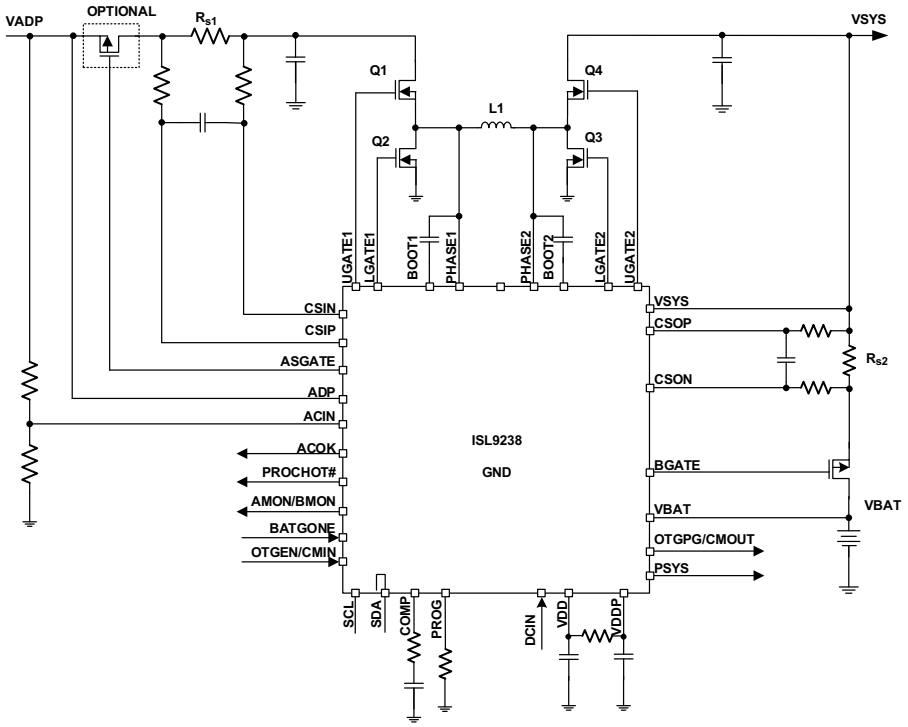

FIGURE 1. TYPICAL APPLICATION CIRCUIT

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Ordering Information

PART NUMBER (Notes 2, 3)	PART MARKING	TEMP. RANGE (°C)	TAPE AND REEL (UNITS) (Note 1)	PACKAGE (RoHS COMPLIANT)	PKG. DWG. #
ISL9238HRTZ	9238H	-10 to +100	-	32 Ld 4x4 TQFN	L32.4x4D
ISL9238HRTZ-T	9238H	-10 to +100	6k	32 Ld 4x4 TQFN	L32.4x4D
ISL9238HRTZ-TK	9238H	-10 to +100	1k	32 Ld 4x4 TQFN	L32.4x4D
ISL9238HRTZ-T7A	9238H	-10 to +100	250	32 Ld 4x4 TQFN	L32.4x4D
ISL9238IRTZ	9238I	-40 to +100	-	32 Ld 4x4 TQFN	L32.4x4D
ISL9238IRTZ-T	9238I	-40 to +100	6k	32 Ld 4x4 TQFN	L32.4x4D
ISL9238EVAL1Z	Evaluation Board				

NOTES:

1. See TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
3. For Moisture Sensitivity Level (MSL), see the ISL9238 device page. For more information about MSL, see TB363.

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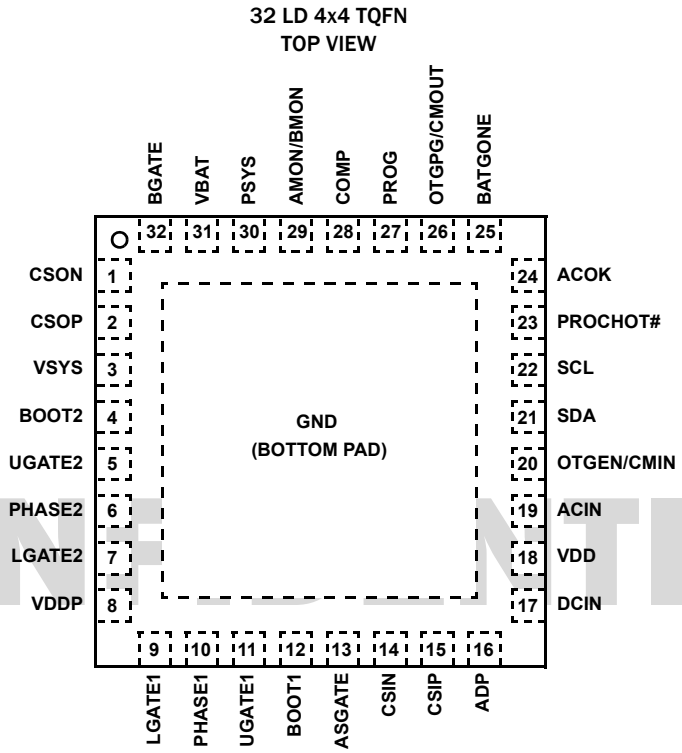
TABLE 1. KEY DIFFERENCES BETWEEN FAMILY OF PARTS

PART NUMBER	I^2C READ ADDRESS	I^2C WRITE ADDRESS
ISL9238	0b00010011 (0x13H)	0b00010010 (0x12H)
ISL9238A	0b00011011 (0x1BH)	0b00011010 (0x1AH)

Pin Configuration



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Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
BOTTOM PAD	GND	Signal common to the IC. Unless otherwise stated, signals are referenced to the GND pin. It should also be used as the thermal pad for heat dissipation.
1	CSON	Battery current sense “–” input. Connect to the battery current resistor negative input. Place a ceramic capacitor between CSOP to CSON to provide Differential mode filtering.
2	CSOP	Battery current sense “+” input. Connect to the battery current resistor positive input. Place a ceramic capacitor between CSOP to CSON to provide Differential mode filtering.
3	VSYS	Provides feedback voltage for MaxSystemVoltage regulation.
4	BOOT2	High-side MOSFET Q4 gate driver supply. Connect an MLCC capacitor across the BOOT2 and PHASE2 pins. The boot capacitor is charged through an internal boot diode connected from the VDDP to BOOT2 pins when the PHASE2 pin drops below VDDP minus the voltage drop across the internal boot diode. Connect a 0.47µF (25V) bootstrap capacitor, which must have an effective capacitance higher than 0.25µF at 5V and x50 effective high-side MOSFET gate capacitance.
5	UGATE2	High-side MOSFET Q4 gate drive.
6	PHASE2	Current return path for the high-side MOSFET Q4 gate drive. Connect this pin to the node consisting of the high-side MOSFET Q4 source, the low-side MOSFET Q3 drain and the one terminal of the inductor.
7	LGATE2	Low-side MOSFET Q3 gate drive.
8	VDDP	Power supply for the gate drivers. Connect to the VDD pin through a 4.7Ω resistor and connect a 2.2µF (10V) MLCC capacitor to GND. The capacitor must have an effective capacitance higher than 0.4µF at 5V and x1.6 effective capacitance at the BOOT1/BOOT2 pins at 5V.
9	LGATE1	Low-side MOSFET Q2 gate drive.
10	PHASE1	Current return path for the high-side MOSFET Q1 gate drive. Connect this pin to the node consisting of the high-side MOSFET Q1 source, the low-side MOSFET Q2 drain and the input terminal of the inductor.
11	UGATE1	High-side MOSFET Q1 gate drive.

Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
12	BOOT1	High-side MOSFET Q1 gate driver supply. Connect an MLCC capacitor across the BOOT1 and PHASE1 pins. The boot capacitor is charged through an internal boot diode connected from the VDDP to BOOT1 pins when the PHASE1 pin drops below VDDP minus the voltage drop across the internal boot diode. Connect a 0.47µF (25V) bootstrap capacitor, which must have an effective capacitance higher than 0.25µF at 5V and x50 effective high-side MOSFET gate capacitance.
13	ASGATE	Gate drive output to the P-channel adapter FET. The use of ASGATE FETs is optional. If the ASGATE pin is not used, leave it floating. When ASGATE turns on, it is clamped 10V below the ADP pin voltage.
14	CSIN	Adapter current sense "-" input.
15	CSIP	Adapter current sense "+" input. The modulator also uses this for sensing input voltage in forward mode and output voltage in reverse mode.
16	ADP	Adapter input. Senses adapter voltage. When adapter voltage is higher than 3.2V, AGATE is turned on. ADP pin is also one of the two internal low power LDO inputs.
17	DCIN	Internal LDO input that provides power to the IC. Connect a diode OR from adapter and system outputs. Bypass this pin with an MLCC capacitor. Connect a 10Ω DCIN resistor between the DCIN pin and the VADP/VSYS diodes, and connect a 4.7µF (50V) DCIN capacitor to GND. The capacitor must have an effective capacitance higher than 0.4µF at 20V.
18	VDD	Internal LDO output that provides the bias power for the internal analog and digital circuit. Connect a 2.2µF (10V) MLCC capacitor to GND. The capacitor must have an effective capacitance higher than 0.4µF at 5V and x1.6 effective capacitance at the BOOT1/BOOT2 pins at 5V. If VDD is pulled below 2V for more than 1ms, the ISL9238 resets all the SMBus register values to their defaults.
19	ACIN	Adapter voltage sense. Use a resistor divider externally to detect adapter voltage. The adapter voltage is valid if the ACIN pin voltage is greater than 0.8V.
20	OTGEN/ CMIN	OTG function enable pin or stand-alone comparator input pin. Pull high to enable OTG function. The OTG function is enabled when the control register is written to select OTG mode and when the battery voltage is above 5.2V. When OTG function is not selected, this pin is the general purpose stand-alone comparator input.
21	SDA	SMBus data I/O. Connect to the data line from the host controller or smart battery. Connect a 10k pull-up resistor according to SMBus specifications.
22	SCL	SMBus clock I/O. Connect to the clock line from the host controller or smart battery. Connect a 10k pull-up resistor according to SMBus specifications.
23	PROCHOT#	Open-drain output. Pulled low when ACHOT, DCHOT or Low_VSYS is detected. IMVP8 compliant. SMBus command to pull low with OTGCURRENT, BAGONE, ACOK, and general purpose comparator (see Table 15 on page 27).
24	ACOK	Adapter presence indicator output to indicate the adapter is ready.
25	BATGONE	Input pin to the IC. Logic high on this pin indicates the battery has been removed. Logic low on this pin indicates the battery is present. BATGONE pin logic high forces the BGATE FET to turn off in any circumstances.
26	OTGPG/ CMOUT	Open-drain output. OTG function output power-good indicator or the stand-alone comparator output. When OTG function is enabled, low if OTG output voltage is not within regulation window. When OTG function is not used, it is the general purpose comparator output.
27	PROG	A resistor from PROG pin to GND sets the following configurations: 1. Default number of the battery cells in series: 1-, 2-, 3-, or 4-cell. 2. Default switching frequency 733kHz or 1MHz. 3. Default adapter current limit value 0.476A or 1.5A. 4. Autonomous Charging mode enable or disable See Table 23 for programming options.
28	COMP	Error amplifier output. Connect a compensation network externally from COMP to GND.
29	AMON/ BMON	Adapter current, OTG output current, battery charging current, or battery discharging current monitor output. $V_{AMON} = 18x(V_{CSIP}-V_{CSIN})$ for adapter current monitor $V_{OTGCMON} = 18x(V_{CSIN}-V_{CSIP})$ for OTG output current monitor $V_{BMON_DISCHARGING} = 18x(V_{CSON}-V_{CSOP})$ for battery discharging current monitor $V_{BMON_CHARGING} = 36x(V_{CSOP}-V_{CSON})$ for battery charging current monitor
30	PSYS	Current source output that indicates the whole platform power consumption. PSYS gain = 1.44µA/W (default) or 0.723µA/W
31	VBAT	Battery voltage sensing. Used for trickle charging detection and Ideal Diode mode control. Connect to a >1µF ceramic capacitor from VBAT pin to GND. VBAT pin is also one of the two internal low power LDO inputs.

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Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
32	BGATE	Gate drive output to the P-channel FET connecting the system and the battery. This pin can go high to disconnect the battery, low to connect the battery or operate in a Linear mode to regulate trickle charge current during trickle charge. When BGATE turns on, it is clamped 10V below VSYS pin voltage.

Block Diagram

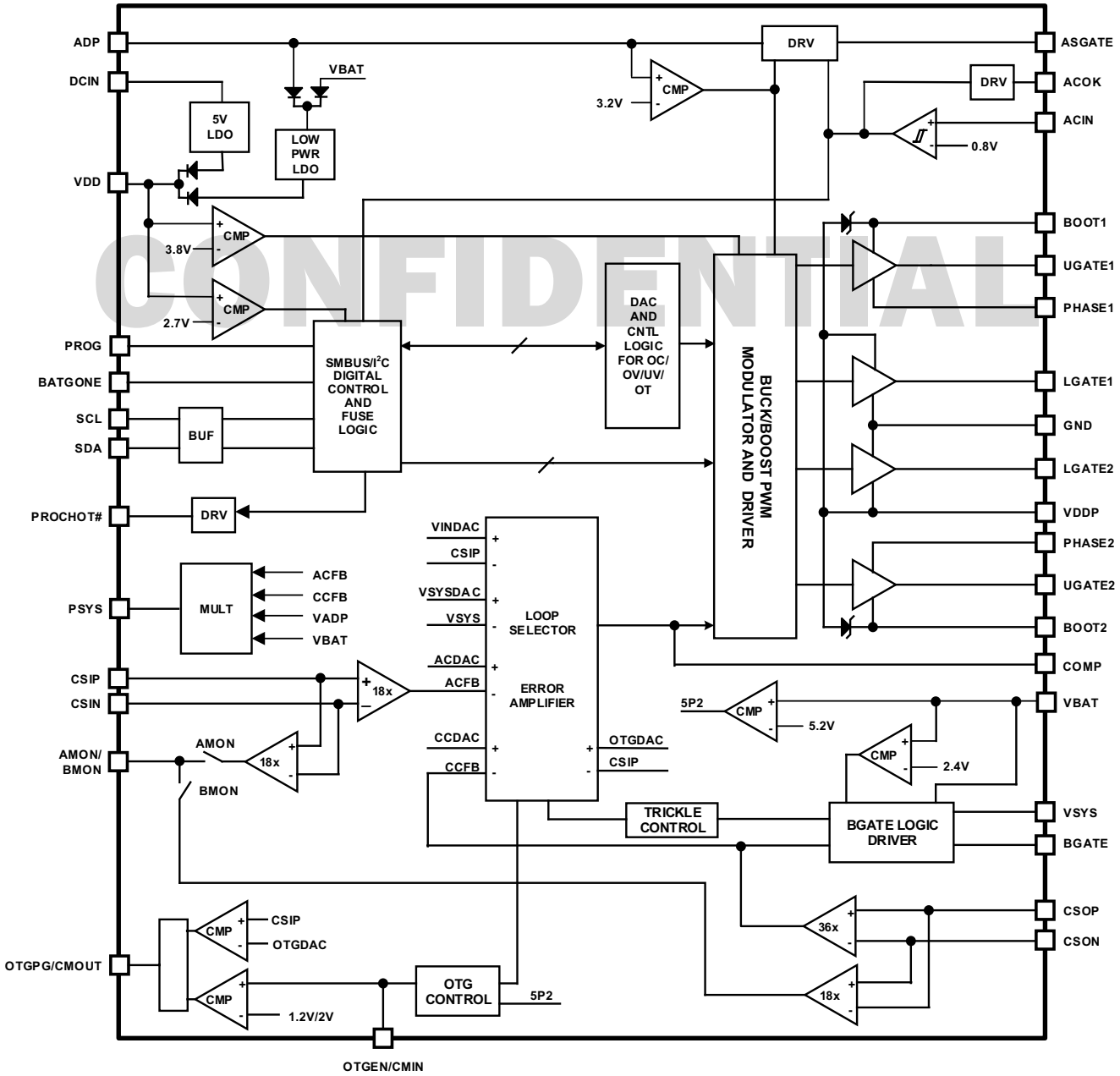

FIGURE 2. BLOCK DIAGRAM

Simplified Application Circuit

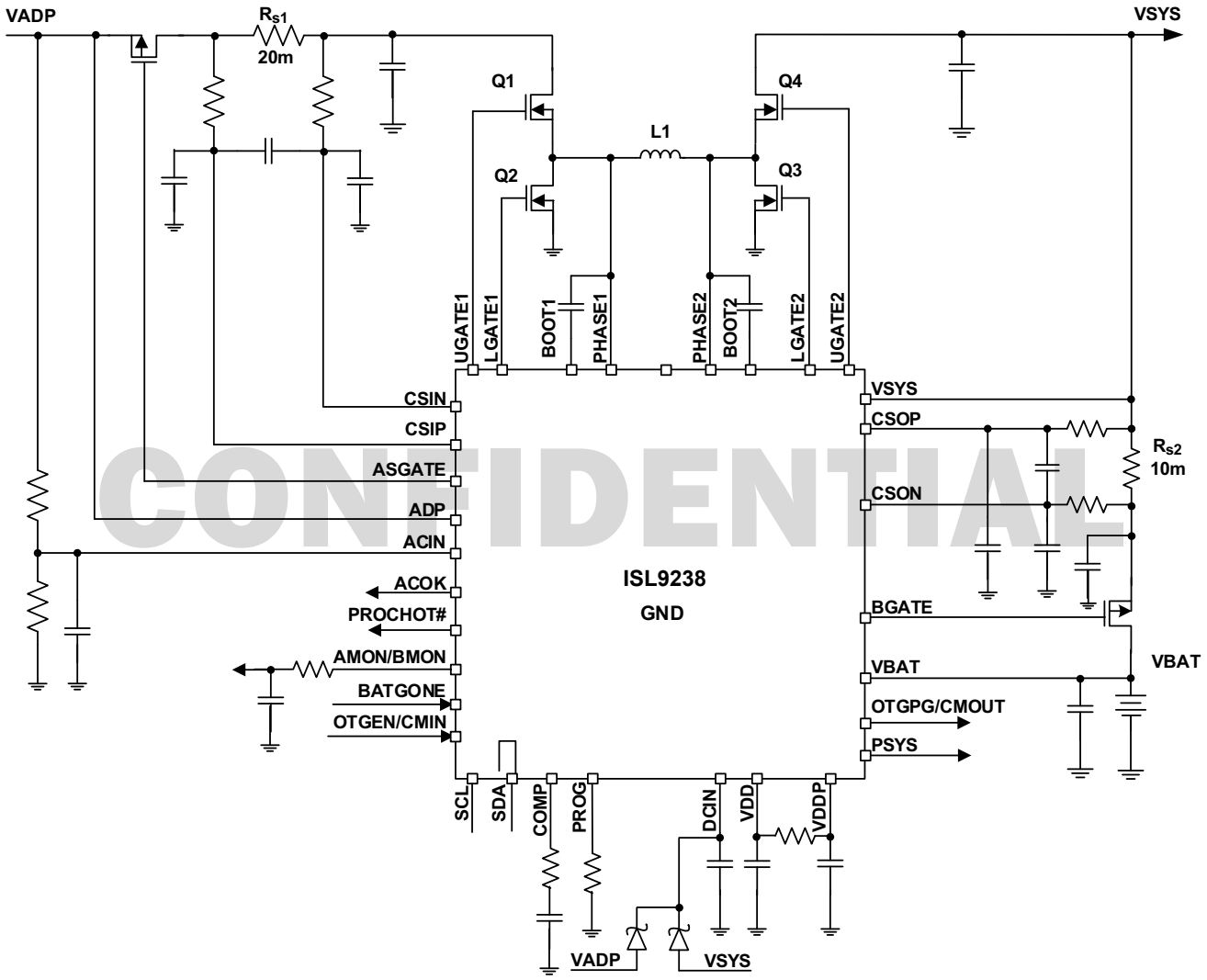

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FIGURE 3. SIMPLIFIED APPLICATION DIAGRAM

Absolute Maximum Ratings

CSIP, CSIN, DCIN, ADP, ASGATE . . . . . -0.3V to +28V
PHASE1 . . . . . (GND - 0.3V) to +28V
PHASE1 . . . . . GND-2V(<20ns) to +28V
BOOT1, UGATE1 . . . . . (GND - 0.3V) to +33V
PHASE2 . . . . . (GND - 0.3V) to +24V
PHASE2 . . . . . GND - 2V(<20ns) to +24V
BOOT2, UGATE2 . . . . . (GND - 0.3V) to +29V
LGATE1, LGATE2. . . . . (GND - 0.3V) to +6.5V
LGATE1, LGATE2. . . . . GND - 2V(<20ns) to +6.5V
VBAT, VSYS, CSOP, CSON, BGATE . . . . . -0.3V to +24V
VDD, VDDP. . . . . -0.3V to +6.5V
COMP . . . . . -0.3V to +6.5V
AMON/BMON, PSYS. . . . . -0.3V to +6.5V
OTGEN, BATGONE. . . . . -0.3V to +6.5V
ACIN, ACOK, PROCHOT#, OTGPG . . . . . -0.3V to +6.5V
CLK, DAT . . . . . -0.3V to +6.5V
BOOT1-PHASE1, BOOT2-PHASE2. . . . . -0.3V to +6.5V
CSIP-CSIN, CSOP-CSON . . . . . -0.3V to +0.3V
VDD. 70mA
ACIN, SDA, SCL, DCIN, ACOK. 2mA
ESD Rating
Human Body Model (Tested per JESD22-A114E). 2kV
Machine Model (Tested per JESD22-A115-A). 200V
Charged Device Model (Tested per JESD22-C101A) 1kV
Latch-Up (Tested per JESD-78B; Class 2, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
32 Ld TQFN Package (Notes 4, 5)	37	2

Ambient Temperature Range (T_A) . . . . . -10°C to +100°C
Junction Temperature Range (T_J). . . . . -10°C to +125°C
Storage Temperature Range (T_S). . . . . -65°C to +175°C
Pb-Free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

Ambient Temperature
HRTZ . . . . . -10°C to +100°C
IRTZ . . . . . -40°C to +100°C
Junction Temperature . . . . . -10°C to +125°C
Adapter voltage . . . . . +4V to +23V

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CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with "direct attach" features. See TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Operating conditions: ADP = CSIP = CSIN = 5V and 20V, V_{SYS} = V_{BAT} = CSOP = CSON = 8V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -10°C to +125°C unless otherwise specified.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
UVLO/ACOK						
VADP UVLO Rising	VADP_UVLO_r		**3.1**	3.3	**3.5**	V
VADP UVLO Hysteresis	VADP_UVLO_h			600		mV
V_{BAT} UVLO Rising	VBAT_UVLO_r		**2.30**	2.45	**2.65**	V
V_{BAT} UVLO Hysteresis	VBAT_UVLO_h			400		mV
V_{BAT} 5P2V Rising	VBAT_5P2_r		**5.05**	5.20	**5.65**	V
V_{BAT} 5P2V Hysteresis	VBAT_5P2_h			490		mV
V_{DD} 2P7 POR Falling, SMBus and BGATE/BMON Active Threshold	VDD_2P7_f		**2.50**	2.70	**2.9**	V
V_{DD} 2P7 POR Hysteresis	VDD_2P7_h			150		mV
V_{DD} 3P8 POR Rising, Modulator and Gate Driver Active	VDD_3P8_r		**3.6**	3.8	**3.9**	V
V_{DD} 3P8 POR Hysteresis	VDD_3P8_h			150		mV
ACIN Rising	ACIN_r		**0.775**	0.800	**0.825**	V
ACIN Hysteresis	ACIN_h			50		mV

Electrical Specifications Operating conditions: ADP = CSIP = CSIN = 5V and 20V, V_{SYS} = V_{BAT} = CSOP = CSON = 8V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -10°C to +125°C unless otherwise specified. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
LINEAR REGULATOR						
V_{DD} Output Voltage	VDD	6V < V_{DCIN} < 23V, no load	**4.5**	5.0	**5.5**	V
V_{DD} Dropout Voltage	VDD_dp	30mA, V_{DCIN} = 4V		85		mV
V_{DD} Overcurrent Threshold	VDD_OC	HRTZ	**80**	115	**150**	mA
V_{DD} Overcurrent Threshold		IRTZ	**75**	115	**150**	mA
Battery Current	I_{BAT1}	Battery only, BGATE on, PSYS OFF, BMON OFF, V_{BAT} = 16.8V, DCIN current comes from battery, I_{BAT} = I_{VBAT} + I_{CSOP} + I_{CSON} + I_{DCIN} + I_{VSYS}		24	**50**	µA
	I_{BAT2}	Battery only, BGATE on, PSYS OFF, BMON ON, V_{BAT} = 16.8V, DCIN current comes from battery, I_{BAT} = I_{VBAT} + I_{CSOP} + I_{CSON} + I_{DCIN} + I_{VSYS}		74		µA
	I_{BAT3}	Battery only, BGATE on, PSYS ON, BMON OFF, V_{BAT} = 16.8V, DCIN current comes from battery, I_{BAT} = I_{VBAT} + I_{CSOP} + I_{CSON} + I_{DCIN} + I_{VSYS}		905	**1055**	µA
ADAPTER CURRENT REGULATION, R_{s1} = 20mΩ						
Adapter Current Accuracy		CSIP-CSIN = 80mV		4		A
			-2		**2**	%
		CSIP-CSIN = 40mV		2		A
			-2.5		**2.5**	%
		CSIP-CSIN = 10mV		0.5		A
			-10		**10**	%
Adapter Current PROCHOT# Threshold R_{s1} = 20mΩ	$I_{ADP_HOT_TH10}$	ACProchot = 0x1580H (5504mA)		5504		mA
			-1.5		**1.5**	%
		ACProchot = 0x0A80H (2688mA)		2688		mA
			-3.0		**3.0**	%
		ACProchot = 0x0400H (1024mA)		1024		mA
			-6.0		**6.0**	%
SYSTEM VOLTAGE REGULATION						
Maximum System Voltage Accuracy	HRTZ	MaxSystemVoltage for 1-cell (4.2V)	**-0.75**		**0.75**	%
		MaxSystemVoltage for 1-cell (8.4V)	**-0.6**		**0.6**	%
		MaxSystemVoltage for 3-cell and 4-cell (12.6V and 16.8V)	**-0.5**		**0.5**	%
	IRTZ	MaxSystemVoltage for 1-cell (4.2V)	**-0.85**		**0.85**	%
		MaxSystemVoltage for 1-cell (8.4V)	**-0.7**		**0.7**	%
		MaxSystemVoltage for 3-cell and 4-cell (12.6V and 16.8V)	**0.55**		**0.50**	%
Minimum System Voltage Accuracy			**-3**		**3**	%
Input Voltage Regulation Accuracy		4.096V	**3.98**		**4.22**	%

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Electrical Specifications Operating conditions: ADP = CSIP = CSIN = 5V and 20V, V_{SYS} = V_{BAT} = CSOP = CSON = 8V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -10°C to +125°C unless otherwise specified. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
CHARGE CURRENT REGULATION, R_{s2} = 10mΩ (LIMITS APPLY ACROSS TEMPERATURE RANGE OF 0°C TO +85°C)						
Charge Current Accuracy		CSOP-CSON = 60mV		6.03		A
			-2		**2**	%
		CSOP-CSON = 20mV		2.01		A
			-4		**4**	%
		CSOP-CSON = 10mV		1.005		A
			-5		**6**	%
		CSOP-CSON = 5mV		0.501		A
			-10		**12**	%
BGATE CLAMP						
VSYS-VBGATE ON		Charging enabled	**6.80**	8.30	**9.16**	V
VSYS-VBGATE OFF		Charging disabled		0		V
ASGATE CLAMP						
VADP-VASGATE ON				12		V
VSYS-VBGATE OFF				0		V
TRICKLE CHARGING CURRENT REGULATION, R_{s2} = 10mΩ (LIMITS APPLY ACROSS TEMPERATURE RANGE OF 0°C TO +85°C)						
Trickle Charge Current Accuracy		Trickle, 512mA	**410**	512	**614**	mA
		Trickle, 256mA	**205**	256	**334**	mA
		Trickle, 128mA	**77**	128	**192**	mA
		Trickle, 64mA	**16**	64	**128**	mA
Fast Charge to Trickle Charge Threshold		V_{SYS} - V_{BGATE}	**4.23**	5.18	**5.97**	V
Trickle Charge to Fast Charge Threshold Hysteresis		V_{SYS} - V_{BGATE}	**55**	130	**210**	mV
Fast Charge to Trickle Charge BGATE Threshold		V_{SYS} > 7V, V_{FB} >> V_{REF}		1.15		V
Trickle Charge to Fast Charge BGATE Threshold Hysteresis		V_{SYS} > 7V, V_{FB} >> V_{REF}		50		mV
IDEAL DIODE MODE						
Entering Ideal Diode Mode VSYS Voltage Threshold		BGATE off, VSYS falling V_{VBAT} - V_{VSYS}	**100**	150	**200**	mV
Exiting Ideal Diode Mode Battery Discharging Current Threshold		R_{s2} = 10mΩ	**110**	200	**290**	mA
Exiting Ideal Diode Mode Battery Charging Current Threshold		R_{s2} = 10mΩ	**50**	130	**200**	mA
BGATE Source		VSYS - BGATE = 2V, charging disabled	**4**	6	**10**	mA
BGATE Sink		BGATE - GND = 2V, charging enabled	**20**	30	**40**	µA
BGATE Sink		BGATE - GND = 2V, in Ideal Diode mode		6		µA
AMON/BMON						
INPUT CURRENT SENSE AMPLIFIER, R_{s1} = 20mΩ						
CSIP/CSIN Input Voltage Range	$V_{CSIP/N}$		**4**		**23**	V/V
AMON Gain				17.97		V/V
AMON Accuracy V_{AMON} = 17.9 * (CSIP - CSIN)		V_{CSIP} - V_{CSIN} = 100mV (5A), CSIP = 5V - 20V	**-2**		**2**	%
		V_{CSIP} - V_{CSIN} = 20mV (1A), CSIP = 5V - 20V	**-5**		**5**	%
		V_{CSIP} - V_{CSIN} = 10mV (0.5A), CSIP = 5V - 20V	**-10**		**10**	%
		V_{CSIP} - V_{CSIN} = 2mV (0.1A), CSIP = 5V - 20V	**-40**		**40**	%

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Electrical Specifications Operating conditions: ADP = CSIP = CSIN = 5V and 20V, V_{SYS} = V_{BAT} = CSOP = CSON = 8V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -10°C to +125°C unless otherwise specified. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
Reverse AMON Gain				17.9		V/V
AMON Accuracy V_{AMON} = 17.9 * (CSIN - CSIP)		V_{CSIN} - V_{CSIP} = 80mV (4A), CSIP = 4V - 22V	**-2.5**		**2.5**	%
		V_{CSIN} - V_{CSIP} = 20mV (1A), CSIP = 4V - 22V	**-6.5**		**4.5**	%
		V_{CSIN} - V_{CSIP} = 10mV (0.5A), CSIP = 4V - 22V	**-12**		**9**	%
		V_{CSIN} - V_{CSIP} = 5.12mV (0.256A), CSIP = 4V - 22V	**-25**		**25**	%
AMON Minimum Output Voltage		V_{CSIP} - V_{CSIN} = 0V			**30**	mV
DISCHARGE CURRENT SENSE AMPLIFIER, R_{S2} = 10mΩ						
BMON Gain (Battery Discharging)				17.78		V/V
BMON Accuracy V_{BMON} = 17.9 * (V_{CSON} - V_{CSOP})		V_{CSON} - V_{CSOP} = 100mV (10A), V_{CSON} = 8V	**-2**		**2**	%
		V_{CSON} - V_{CSOP} = 20mV (2A), V_{CSON} = 8V	**-7.0**	-1.5	**3.0**	%
		V_{CSON} - V_{CSOP} = 10mV (1A), V_{CSON} = 8V	**-10.5**	-2.5	**5.5**	%
		V_{CSON} - V_{CSOP} = 6mV (0.6A), V_{CSON} = 8V	**-17**	-4	**12**	%
BMON Gain (Battery Charging)		Limits apply across temperature range of 0°C to +85°C		35.7		V/V
BMON Accuracy V_{BMON} = 35.7* (V_{CSON} - V_{CSOP})		V_{CSOP} - V_{CSON} = 60mV (6A), V_{CSON} = 8V	**-3**		**3**	%
		V_{CSOP} - V_{CSON} = 40mV (4A), V_{CSON} = 8V	**-4**		**4**	%
		V_{CSOP} - V_{CSON} = 10mV (1A), V_{CSON} = 8V	**-10**		**10**	%
		V_{CSOP} - V_{CSON} = 5mV (0.5A), V_{CSON} = 8V	**-25**		**25**	%
BMON Minimum Output Voltage		V_{CSOP} - V_{CSON} = 0V			**30**	mV
Discharging Current PROCHOT# Threshold, R_{S2} = 10mΩ	$I_{DIS_HOT_TH}$	DCProchot = 2.048A	**1.77**	2.08	**2.39**	A
Discharging Current PROCHOT# Threshold, Battery Only, R_{S2} = 10mΩ	$I_{DIS_HOT_TH}$	DCProchot = 12A	**10.8**	13.5	**17**	A
		DCProchot = 6A	**5.35**	6.5	**8**	A
AMON/BMON Source Resistance		(Note 7)			**5**	Ω
AMON/BMON Sink Resistance		(Note 7)			**5**	Ω
BATGONE AND OTGEN						
High-Level Input Voltage			**0.9**			V
Low-Level Input Voltage					**0.4**	V
Input Leakage Current		$V_{BATGONE}$ = 3.3V, 5V; V_{OTGEN} = 3.3V, 5V			**1**	µA
PROCHOT#						
PROCHOT# Debounce Time		PROCHOT# Debounce register Bit<1:0> = 11	**0.85**	1	**1.15**	ms
		PROCHOT# Debounce register Bit<1:0> = 10	**425**	500	**575**	µs
PROCHOT# Duration Time		PROCHOT# Duration register Bit<2:0> = 011	**8.5**	10	**11.5**	ms
		PROCHOT# Duration register Bit<2:0> = 001	**17**	20	**23**	ms
Low VSYS PROCHOT# Trip Threshold	$V_{LOW_VSYS_HOT}$	Control1 register Bit<1:0> = 00	**5.8**	6.0	**6.2**	V
		Control1 register Bit<1:0> = 01	**6.1**	6.3	**6.5**	V
		Control1 register Bit<1:0> = 10	**6.4**	6.6	**6.8**	V
		Control1 register Bit<1:0> = 11	**6.7**	6.9	**7.1**	V
PSYS (Notes 7, 8)						
PSYS Output Current R_{S1} = 20mΩ R_{S2} = 10mΩ I_{PSYS}= 1.493 x Power + 1.43µA	I_{PSYS} Control3 Bit<9> = 1	V_{CSIP} = 19V, $V_{CSIP-CSIN}$ = 80mV, V_{BAT} = 12V, $V_{CSOP-CSON}$ = 10mV	**-5**		**5**	%
		V_{CSIP} = 19V, $V_{CSIP-CSIN}$ = 80mV, V_{BAT} = 12V, $V_{CSOP-CSON}$ = -10mV	**-5.3**		**5.3**	%
	I_{PSYS} Control3 Bit<9> = 0	V_{CSIP} = 19V, $V_{CSIP-CSIN}$ = 0mV, V_{BAT} = 8.4V, $V_{CSOP-CSON}$ = 20mV	**-7**		**7**	%
Maximum PSYS Output Voltage	V_{PSYS_MAX}		**4**			V

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Electrical Specifications Operating conditions: ADP = CSIP = CSIN = 5V and 20V, V_{SYS} = V_{BAT} = CSOP = CSON = 8V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -10°C to +125°C unless otherwise specified. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
OTG						
OTG Voltage		OTGVoltage register = 5.12V	**4.95**	5.03	**5.12**	V
OTG Current (5V to 12V)		OTGCurrent register = 512mA	**435**	512	**589**	mA
		OTGCurrent register = 1024mA	**922**	1024	**1126**	mA
		OTGCurrent register = 4096mA	**3975**	4096	**4240**	mA
GENERAL PURPOSE COMPARATOR						
General Purpose Comparator Rising Threshold		Reference = 1.2V	**1.15**	1.2	**1.25**	V
		Reference = 2V	**1.95**	2	**2.05**	V
General Purpose Comparator Hysteresis		Reference = 1.2V	**30**	60	**90**	mV
		Reference = 2V	**30**	60	**90**	mV
PROTECTION (Note 9)						
VSYS Overvoltage Rising Threshold		MaxSystemVoltage register value = 8.4V	**8.95**	9.15	**9.35**	V
VSYS Overvoltage Hysteresis			**250**	400	**550**	mV
Adapter Way Overcurrent Rising Threshold		R_{S1} = 20mΩ and VCSIP range 5V to 20V	**7.5**	16	**25**	A
Battery Discharge Way Overcurrent Rising Threshold		R_{S2} = 10mΩ and VCSOP range 4V to 16V	**10**	21	**33**	A
Over-Temperature Threshold (Note 7)			**140**	150	**160**	°C
Adapter Overvoltage Rising Threshold			**22.5**	23.4	**24**	V
Adapter Overvoltage Hysteresis			**150**	350	**500**	mV
OTG Undervoltage Falling Threshold		OTG voltage = 5.004V	**3.45**	3.80	**4.25**	V
OTG Overvoltage Rising Threshold		OTG voltage = 5.004V	**5.8**	6.2	**6.6**	V
OSCILLATOR						
Oscillator Frequency. Digital Core Only			**0.85**	1	**1.15**	MHz
Digital Debounce Time Accuracy (Note 7)			**-15**		**15**	%
MISCELLANEOUS						
Switching Frequency Accuracy		COMP >1.7V and not in period stretching	**-15**		**15**	%
Battery Learn Mode Auto-Exit Threshold		MinSystemVoltage = 5.376V Control1 register Bit<13> = 1	**5.05**	5.35	**5.7**	V
Battery Learn Mode Auto-Exit Hysteresis (Note 7)			**180**	330	**480**	mV
SMBus						
SDA/SCL Input Low Voltage		3.3V			**0.8**	V
SDA/SCL Input High Voltage		3.3V	**2**			V
SDA/SCL Input Bias Current		3.3V			**1**	µA
SDA, Output Sink Current		SDA = 0.4V, on	**4**			mA
SMBus Frequency	f_{SMB}		**10**		**400**	kHz
GATE DRIVER						
UGATE1 Pull-Up Resistance	$UG1_{RPU}$	100mA source current		800	**1200**	mΩ
UGATE1 Source Current	$UG1_{SRC}$	UGATE1 - PHASE1 = 2.5V	**1.3**	2		A
UGATE1 Pull-Down Resistance	$UG1_{RPD}$	100mA sink current		350	**475**	mΩ
UGATE1 Sink Current	$UG1_{SNK}$	UGATE1 - PHASE1 = 2.5V	**1.9**	2.8		A
LGATE1 Pull-Up Resistance	$LG1_{RPU}$	100mA source current		800	**1200**	mΩ
LGATE1 Source Current	$LG1_{SRC}$	LGATE1 - GND = 2.5V	**1.3**	2		A
LGATE1 Pull-Down Resistance	$LG1_{RPD}$	100mA sink current		300	**450**	mΩ

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Electrical Specifications

Operating conditions: ADP = CSIP = CSIN = 5V and 20V, V_{SYS} = V_{BAT} = CSOP = CSON = 8V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -10°C to +125°C unless otherwise specified. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
LGATE1 Sink Current	$LG1_{SNK}$	LGATE1 - GND = 2.5V	**2.3**	3.5		A
LGATE2 Pull-Up Resistance	$LG2_{RPU}$	100mA source current		800	**1200**	mΩ
LGATE2 Source Current	$LG2_{SRC}$	LGATE2 - GND = 2.5V	**1.3**	2		A
LGATE2 Pull-Down Resistance	$LG2_{RPD}$	100mA sink current		300	**450**	mΩ
LGATE2 Sink Current	$LG2_{SNK}$	LGATE2 - GND = 2.5V	**2.3**	3.5		A
UGATE2 Pull-Up Resistance	$UG2_{RPU}$	100mA source current		800	**1200**	mΩ
UGATE2 Source Current	$UG2_{SRC}$	UGATE2 - PHASE2 = 2.5V	**1.3**	2		A
UGATE2 Pull-Down Resistance	$UG2_{RPD}$	100mA sink current		300	**450**	mΩ
UGATE2 Sink Current	$UG2_{SNK}$	UGATE2 - PHASE2 = 2.5V	**2.3**	3.5		A
UGATE1 to LGATE1 Dead Time	$t_{UG1LG1DEAD}$		**10**	20	**40**	ns
LGATE1 to UGATE1 Dead Time	$t_{LG1UG1DEAD}$		**10**	20	**40**	ns
LGATE2 to UGATE2 Dead Time	$t_{LG2UG2DEAD}$		**10**	20	**40**	ns
UGATE2 to LGATE2 Dead Time	$t_{UG2LG2DEAD}$		**10**	20	**40**	ns

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SMBus Timing Specifications (Note 7)

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
SMBus Frequency	F_{SMB}		**10**		**400**	kHz
Bus Free Time	t_{BUF}		**4.7**			µs
Start Condition Hold Time from SCL	$t_{HD:STA}$		**4**			µs
Start Condition Setup Time from SCL	$t_{SU:STA}$		**4.7**			µs
Stop Condition Setup Time from SCL	$t_{SU:STO}$		**4**			µs
SDA Hold Time from SCL	$t_{HD:DAT}$		**300**			ns
SDA Setup Time from SCL	$t_{SU:DAT}$		**250**			ns
SCL Low Period	t_{LOW}		**4.7**			µs
SCL High Period	t_{HIGH}		**4**			µs
SMBus Inactivity Timeout		Maximum charging period without a SMBus Write to MaxSystemVoltage or ChargeCurrent register		175		s

NOTES:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
7. Limits established by characterization and are not production tested.
8. For more information about PSYS, see "PSYS Monitor" on page 36.
9. For more information about Way Overcurrent Protection, see "Way Overcurrent Protection (WOCP)" on page 38.

Gate Driver Timing Diagram

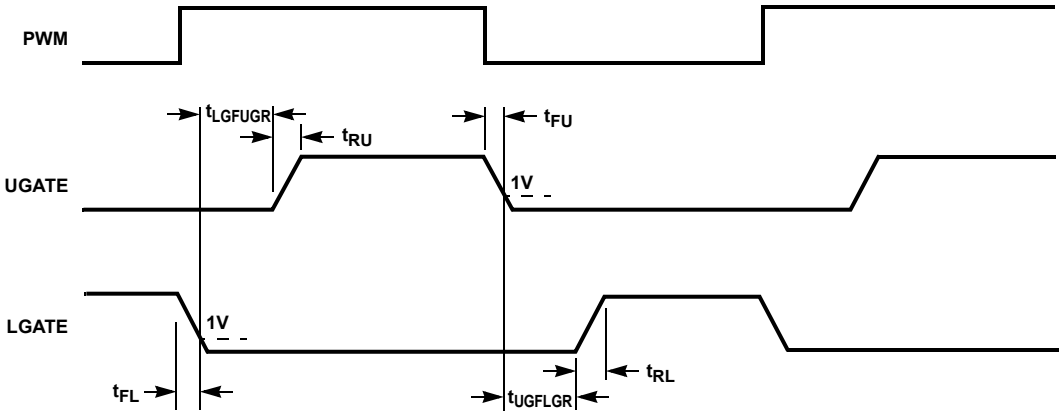

FIGURE 4. GATE DRIVER TIMING DIAGRAM

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Typical Performance

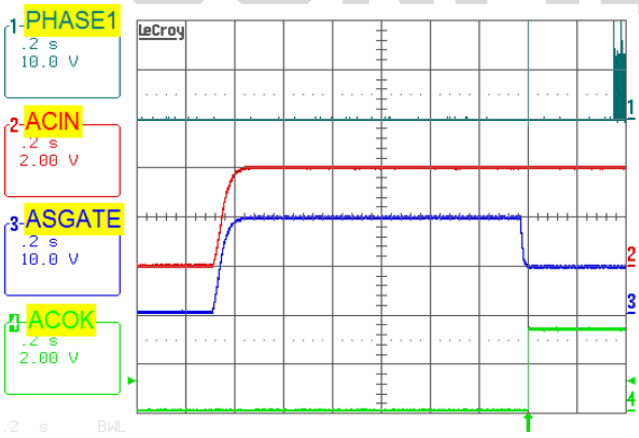

FIGURE 5. ADAPTER INSERTION, V_{ADP} = 20V, V_{BAT} = 11V, CHARGECURRENT = 0A

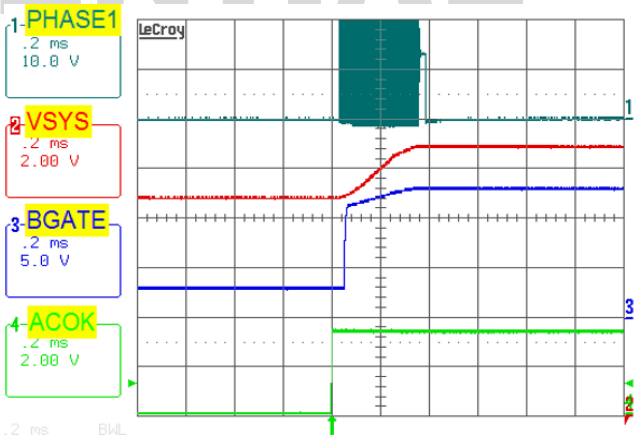

FIGURE 6. ADAPTER INSERTION, V_{ADP} = 20V, V_{BAT} = 11V, CHARGECURRENT = 0A (Figure 5 ZOOM IN)

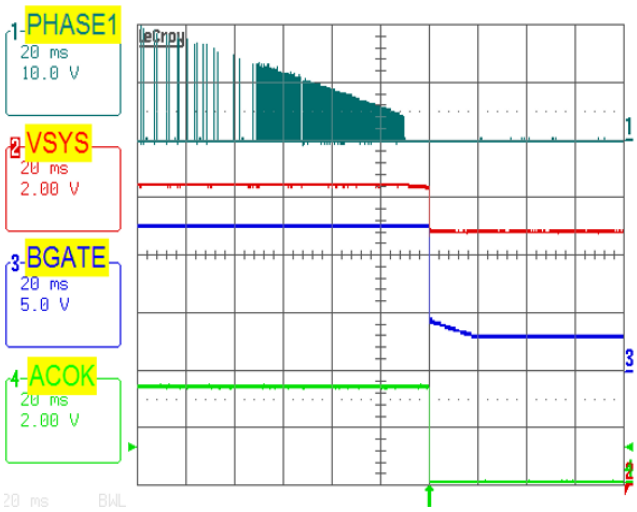

FIGURE 7. ADAPTER REMOVAL, V_{ADP} = 20V, V_{BAT} = 11V, CHARGECURRENT = 0A

Typical Performance (Continued)

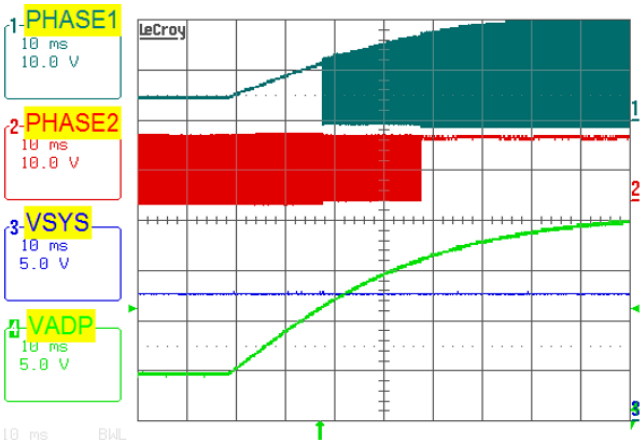

FIGURE 8. ADAPTER VOLTAGE RAMPS UP, BOOST -> BUCK-BOOST -> BUCK OPERATION MODE TRANSITION

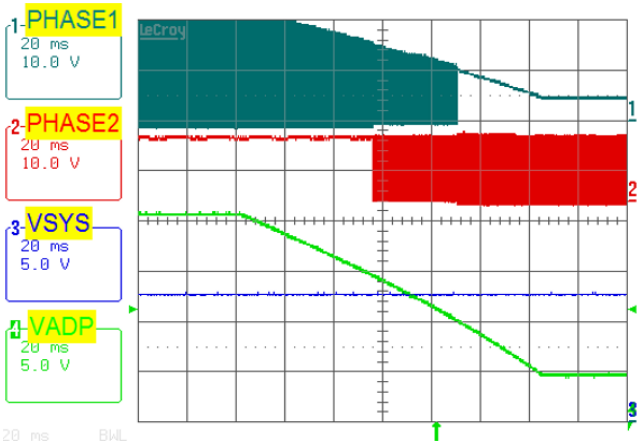

FIGURE 9. ADAPTER VOLTAGE RAMPS DOWN, BUCK -> BUCK-BOOST -> BOOST OPERATION MODE TRANSITION

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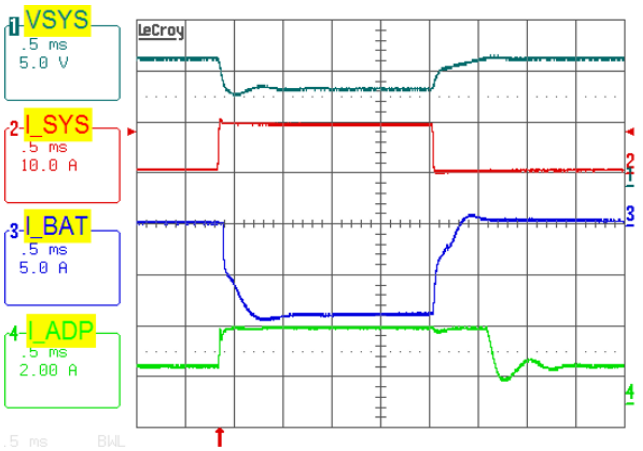

FIGURE 10. BOOST MODE, OUTPUT VOLTAGE LOOP TO ADAPTER CURRENT LOOP TRANSITION. V_{ADP} = 5V, MAXSYSTEMVOLTAGE = 12.576V, V_{BAT} = 11V, SYSTEM LOAD 0.5A TO 10A STEP, ADAPTERCURRENTLIMIT = 3A, CHARGECURRENT = 0A

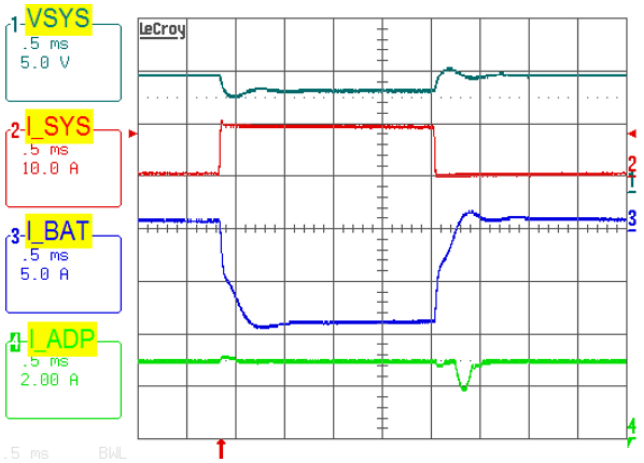

FIGURE 11. BOOST MODE, CHARGING CURRENT LOOP TO ADAPTER CURRENT LOOP TRANSITION. V_{ADP} = 5V, MAXSYSTEMVOLTAGE = 12.5766V, V_{BAT} = 11V, SYSTEM LOAD 0.5A TO 10A STEP, ADAPTERCURRENTLIMIT = 3A, CHARGECURRENT = 1A

Typical Performance (Continued)

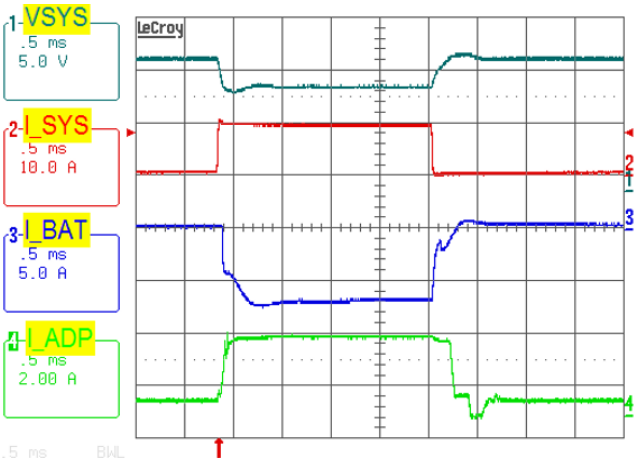

FIGURE 12. BUCK-BOOST MODE, OUTPUT VOLTAGE LOOP TO ADAPTER CURRENT LOOP TRANSITION. V_{ADP} = 12V, MAXSYSTEMVOLTAGE = 12.576V, V_{BAT} = 11V, SYSTEM LOAD 1A TO 10A STEP, ADAPTERCURRENTLIMIT = 3A, CHARGECURRENT = 0A

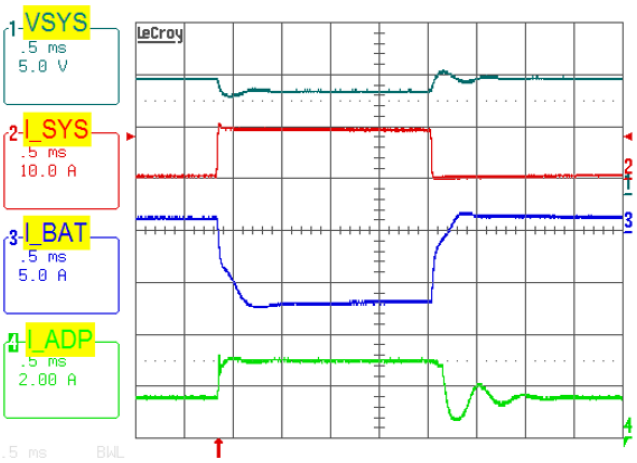

FIGURE 13. BUCK-BOOST MODE, CHARGING CURRENT LOOP TO ADAPTER CURRENT LOOP TRANSITION. V_{ADP} = 12V, MAXSYSTEMVOLTAGE = 12.576V, V_{BAT} = 11V, SYSTEM LOAD 1A TO 10A STEP, ADAPTERCURRENTLIMIT = 3A, CHARGECURRENT = 1A

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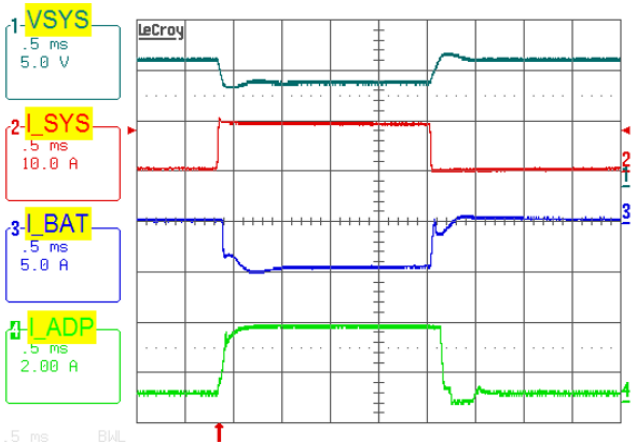

FIGURE 14. BUCK MODE, OUTPUT VOLTAGE LOOP TO ADAPTER CURRENT LOOP TRANSITION. V_{ADP} = 20V, MAXSYSTEMVOLTAGE = 12.576V, V_{BAT} = 11V, SYSTEM LOAD 2A TO 10A STEP, ADAPTERCURRENTLIMIT = 3A, CHARGECURRENT = 0A

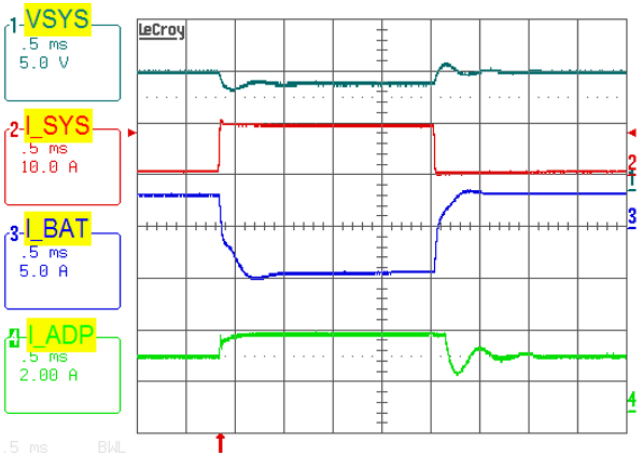

FIGURE 15. BUCK MODE, CHARGING CURRENT LOOP TO ADAPTER CURRENT LOOP TRANSITION. V_{ADP} = 20V, MAXSYSTEMVOLTAGE = 12.576V, V_{BAT} = 11V, SYSTEM LOAD 2A TO 10A STEP, ADAPTERCURRENTLIMIT = 3A, CHARGECURRENT = 3A

Typical Performance (Continued)

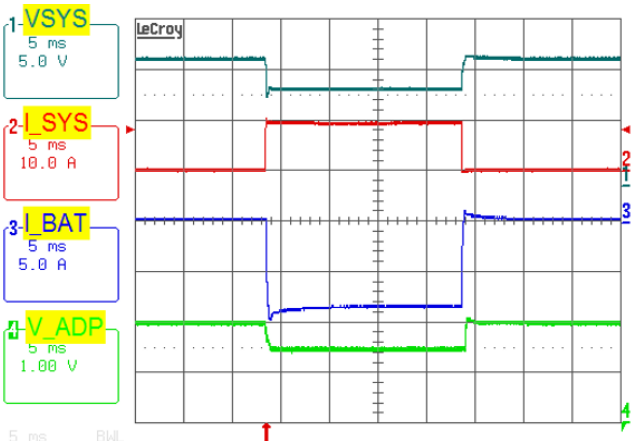

FIGURE 16. BOOST MODE, OUTPUT VOLTAGE LOOP TO INPUT VOLTAGE LOOP TRANSITION. V_{ADP} = 5.004V, MAXSYSTEMVOLTAGE = 12.576V, V_{BAT} = 11V, VINDAC = 4.437V, SYSTEM LOAD 0A TO 10A STEP, CHARGECURRENT = 0A

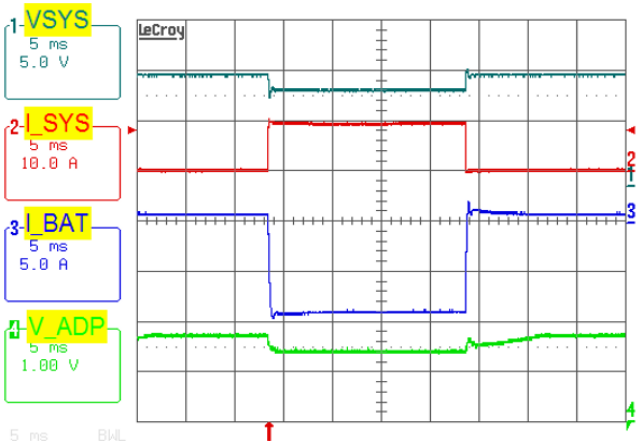

FIGURE 17. BOOST MODE, CHARGING CURRENT LOOP TO INPUT VOLTAGE LOOP TRANSITION. V_{ADP} = 5.004V, MAXSYSTEMVOLTAGE = 12.576V, V_{BAT} = 11V, VINDAC = 4.437V, SYSTEM LOAD 0A TO 10A STEP, CHARGECURRENT = 0.5A

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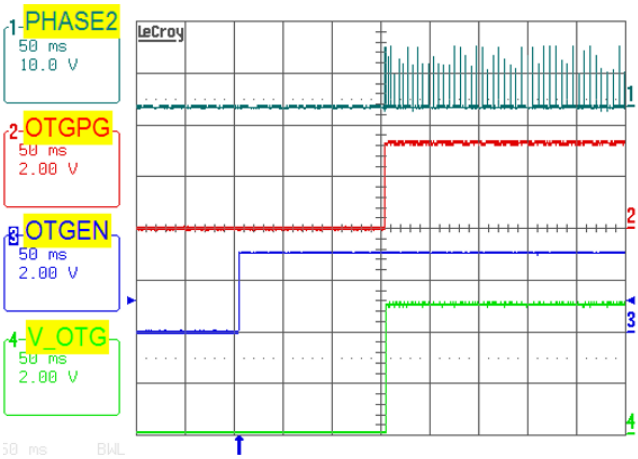

FIGURE 18. OTG MODE ENABLE, OTG ENABLE 150ms DEBOUNCE TIME

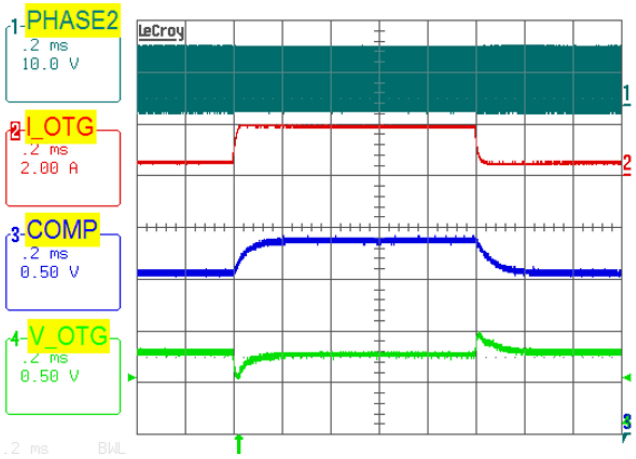

FIGURE 19. OTG MODE 0.5A TO 2A TRANSIENT LOAD, OTG VOLTAGE = 5.12V

General SMBus Architecture

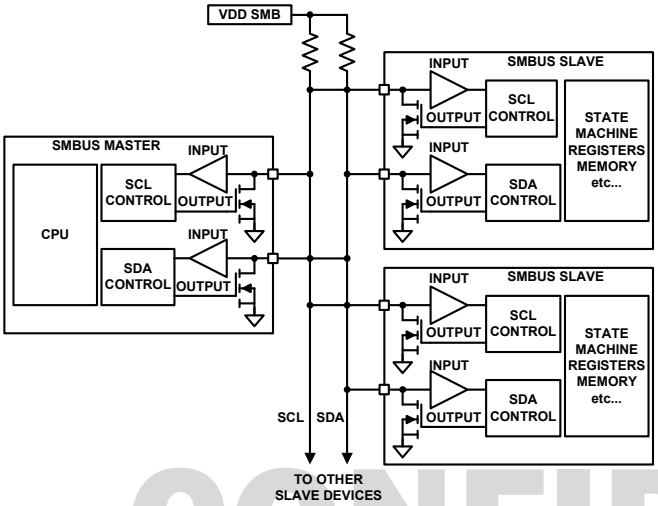

FIGURE 20. GENERAL SMBus ARCHITECTURE

Data Validity

The data on the SDA line must be stable during the HIGH period of the SCL, unless generating a START or STOP condition. The HIGH or LOW state of the data line can change only when the clock signal on the SCL line is LOW. See Figure 21.

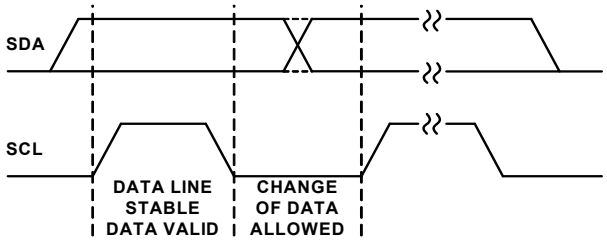

FIGURE 21. DATA VALIDITY

START and STOP Conditions

In Figure 22 the START condition is a HIGH to LOW transition of the SDA line while SCL is HIGH.

The STOP condition is a LOW to HIGH transition on the SDA line while SCL is HIGH. A STOP condition must be sent before each START condition.

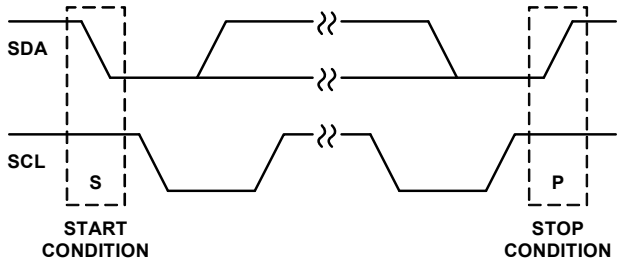

FIGURE 22. START AND STOP WAVEFORMS

Acknowledge

Each address and data transmission uses nine clock pulses. The ninth pulse is the Acknowledge bit (ACK). After the start condition, the master sends seven slave address bits and a R/$\overline{W}$ bit during the next eight clock pulses. During the ninth clock pulse, the device that recognizes its own address holds the data line low to acknowledge (see Figure 23). The ACK bit is also used by both the master and the slave to acknowledge receipt of register addresses and data.

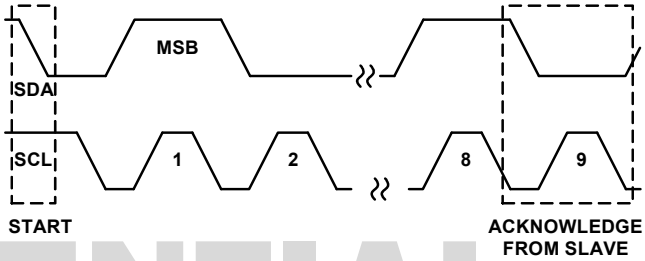

FIGURE 23. ACKNOWLEDGE ON THE SMBus

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SMBus Transactions

All transactions start with a control byte sent from the SMBus master device. The control byte begins with a Start condition, followed by 7 bits of slave address (0001001) and the R/$\overline{W}$ bit. The R/$\overline{W}$ bit is 0 for a WRITE or 1 for a READ. If any slave device on the SMBus bus recognizes its address, it acknowledges by pulling the Serial Data (SDA) line low for the last clock cycle in the control byte. If no slave exists at that address or it is not ready to communicate, the data line will be 1, indicating a not acknowledge condition.

When the control byte is sent and the ISL9238 acknowledges it, the second byte sent by the master must be a register address byte such as 0x14 for the ChargeCurrent register. The register address byte tells the ISL9238 which register the master will write or read. See Table 2 on page 19 for details about the registers. When the ISL9238 receives a register address byte, it responds with an acknowledge.

Byte Format

Every byte put on the SDA line must be 8 bits long and must be followed by an ACK bit. Data is transferred with the Most Significant Bit (MSB) first and the Least Significant Bit (LSB) last. The LO BYTE data is transferred before the HI BYTE data. For example, when writing 0x41A0, 0xA0 is written first and 0x41 is written second.

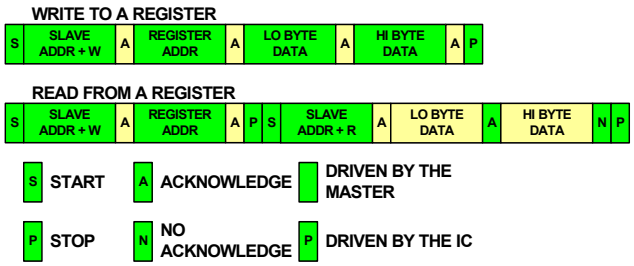

FIGURE 24. SMBus READ AND WRITE PROTOCOL

SMBus and I²C Compatibility

The ISL9238 SMBus minimum input logic high voltage is 2V, so it is compatible with I²C with higher than 2V pull-up power supply.

The ISL9238 SMBus registers are 16 bits, so it is compatible with a 16-bit I²C or an 8-bit I²C with auto-increment capability.

ISL9238 SMBus Commands

The ISL9238 receives control inputs from the SMBus interface after Power-On Reset (POR). The serial interface complies with the System Management Bus Specification, which can be downloaded from www.smbus.org. The ISL9238 uses the SMBus Read-word and Write-word protocols (see Figure 24) to communicate with the host system and a smart battery. The ISL9238 is an SMBus slave device and does not initiate communication on the bus. It responds to the 7-bit address 0b0001001_ as follows:

Read and Write address for ISL9238 is:

Read address = 0b00010011 (0X13H)/0b00011011 (0X1BH)

Write address = 0b00010010 (0X12H)/0b00011010 (0X1AH)

The data (SDA) and clock (SCL) pins have Schmitt-trigger inputs that can accommodate slow edges. Choose pull-up resistors for SDA and SCL to achieve rise times according to the SMBus specifications.

The examples in this datasheet are based on current-sensing resistors R_{S1} = 20mΩ and R_{S2} = 10mΩ unless otherwise specified.

TABLE 2. REGISTER SUMMARY

REGISTER NAMES	REGISTER ADDRESS	READ/ WRITE	NUMBER OF BITS	DESCRIPTION	DEFAULT
ChargeCurrentLimit	0x14	R/W	11	[12:2]11-bit, LSB size 4mA, total range 6080mA with 10mΩ R_{S2}	0A
MaxSystemVoltage	0x15	R/W	12	[14:3]12-bit, LSB size 8mV, total range 18.304V	4.192V for 1-cell
					8.384V for 2-cell
					12.576V for 3-cell
					16.768V for 4-cell
T1 and T2	0x38	R/W	6	Configure two-level adapter current limit duration	0x000h
Control0	0x39	R/W	16	Configure various charger options	0x0000h
Information1	0x3A	R	16	Indicate various charger status	0x0000h
AdapterCurrentLimit2	0x3B	R/W	11	[12:2]11-bit, LSB size 4mA, total range 6080mA with 20mΩ R_{S1}	1500mA
Control1	0x3C	R/W	16	Configure various charger options	0x0000h
Control2	0x3D	R/W	16	Configure various charger options	0x0000h
MinSystemVoltage	0x3E	R/W	6	[13:8]6-bit, LSB size 256mV, total range 13.824V	2.56V for 1-cell
					5.12V for 2-cell
					7.68V for 3-cell
					10.24V for 4-cell
AdapterCurrentLimit1	0x3F	R/W	11	[12:2]11-bit, LSB size 4mA, total range 6080mA with 20mΩ R_{S1}	Set by PROG pin
Revision ID	0x44	R	8	Revision ID register - Read only 0x01 - Rev1 0x02 - Rev2 0x06 - Rev3	N/A
ACProchot#	0x47	R/W	6	[12:7] adapter current PROCHOT# threshold Default 3.072A, 128mA resolution for 20mΩ R_{S1}.	3.072A
DCProchot#	0x48	R/W	6	[13:8] Battery discharging current PROCHOT# threshold Default 4.096A, 256mA resolution for 10mΩ R_{S2}.	4.096A
OTG Voltage	0x49	R/W	12	[14:3] 12-bit, LSB size 12mV, total range 27.456V OTG mode voltage reference	5.004V
OTG Current	0x4A	R/W	6	[12:7] 6-bit, LSB size 128mAV, total range 4.096A OTG mode maximum current limit	0.512A
V_{IN} Voltage	0x4B	R/W	6	[13:8] 6-bit, LSB size 341.3mV, total range 18.432mV V_{IN} loop voltage reference	4.096V
Control3	0x4C	R/W	16	Configure various charger options	0x0000h
Information2	0x4D	R	16	Indicate various charger status	0x0000h
Control4	0x4E	R/W	8	[7:0] 8-bit, Configure various charger options	0x0000h

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TABLE 2. REGISTER SUMMARY (Continued)

REGISTER NAMES	REGISTER ADDRESS	READ/ WRITE	NUMBER OF BITS	DESCRIPTION	DEFAULT
Manufacturer ID	0xFE	R	8	Manufacturer's ID register – 0x49 - Read only	0x0049h
Device ID	0xFF	R	8	Device ID register - 0x0C- Read only	0x000Ch

Setting Charging Current Limit

To set the charging current limit, write a 16-bit ChargeCurrentLimit command (0x14H or 0b00010100) using the Write-word protocol shown in Figure 24 on page 18 and the data format shown in Table 3 for a 10mΩ R_{S2} or Table 4 for a 5mΩ R_{S2}.

The ISL9238 limits the charging current by limiting the CSOP - CSON voltage. By using the recommended current sense resistor values R_{S1} = 20mΩ and R_{S2} = 10mΩ, the register's LSB always translates to 4mA of charging current. The ChargeCurrentLimit register accepts any charging current command, but only the valid register bits are written to the register and the maximum values is clamped at 6080mA for R_{S2} = 10mΩ.

After POR, the ChargeCurrentLimit register is reset to 0x0000H. To set the battery charging current value, write a non-zero number to the ChargeCurrentLimit register. The ChargeCurrentLimit register can be read back to verify its content.

Table 24 shows the conditions to enable fast charging according to the ChargeCurrentLimit register setting.

TABLE 3. ChargeCurrentLimit REGISTER 0x14H (11-BIT, 4mA STEP, 10mΩ SENSE RESISTOR, x36)

BIT	DESCRIPTION
<1:0>	Not used
<2>	0 = Add 0mA of charge current limit. 1 = Add 4mA of charge current limit.
<3>	0 = Add 0mA of charge current limit. 1 = Add 8mA of charge current limit.
<4>	0 = Add 0mA of charge current limit. 1 = Add 16mA of charge current limit.
<5>	0 = Add 0mA of charge current limit. 1 = Add 32mA of charge current limit.
<6>	0 = Add 0mA of charge current limit. 1 = Add 64mA of charge current limit.
<7>	0 = Add 0mA of charge current limit. 1 = Add 128mA of charge current limit.
<8>	0 = Add 0mA of charge current limit. 1 = Add 256mA of charge current limit.
<9>	0 = Add 0mA of charge current limit. 1 = Add 512mA of charge current limit.
<10>	0 = Add 0mA of charge current limit. 1 = Add 1024mA of charge current limit.
<11>	0 = Add 0mA of charge current limit. 1 = Add 2048mA of charge current limit.
<12>	0 = Add 0mA of charge current limit. 1 = Add 4096mA of charge current limit.
<13:15>	Not used
Maximum	<12:2> = 10111110000 6080mA

TABLE 4. ChargeCurrentLimit REGISTER 0x14H (11-BIT, 8mA STEP, 5mΩ SENSE RESISTOR, x36)

BIT	DESCRIPTION
<1:0>	Not used
<2>	0 = Add 0mA of charge current limit. 1 = Add 8mA of charge current limit.
<3>	0 = Add 0mA of charge current limit. 1 = Add 16mA of charge current limit.
<4>	0 = Add 0mA of charge current limit. 1 = Add 32mA of charge current limit.
<5>	0 = Add 0mA of charge current limit. 1 = Add 64mA of charge current limit.
<6>	0 = Add 0mA of charge current limit. 1 = Add 128mA of charge current limit.
<7>	0 = Add 0mA of charge current limit. 1 = Add 256mA of charge current limit.
<8>	0 = Add 0mA of charge current limit. 1 = Add 512mA of charge current limit.
<9>	0 = Add 0mA of charge current limit. 1 = Add 1024mA of charge current limit.
<10>	0 = Add 0mA of charge current limit. 1 = Add 2048mA of charge current limit.
<11>	0 = Add 0mA of charge current limit. 1 = Add 4096mA of charge current limit.
<12>	0 = Add 0mA of charge current limit. 1 = Add 8192mA of charge current limit.
<13:15>	Not used
Maximum	<12:2> = 10111110000 12160mA

Setting Adapter Current Limit

To set the adapter current limit, write a 16-bit AdapterCurrentLimit1 command (0x3FH or 0b00111111) and/or AdapterCurrentLimit2 command (0x3BH or 0b00111011) using the Write-word protocol shown in Figure 24 on page 18 and the data format shown in Table 5 on page 21 for a 20mΩ R_{S1} or Table 6 on page 21 for a 10mΩ R_{S1}.

The ISL9238 limits the adapter current by limiting the CSIP - CSIN voltage. By using the recommended current sense resistor values, the register's LSB always translates to 4mA of adapter current. Any adapter current limit command is accepted but only the valid register bits are written to the AdapterCurrentLimit1 and AdapterCurrentLimit2 registers. The maximum value is clamped at 6080mA for R_{S1} = 20mΩ.

After adapter POR, the AdapterCurrentLimit1 register is reset to the value programmed through the PROG pin resistor. The AdapterCurrentLimit2 register is set to its default value of 1.5A or keeps the value that is written to it previously if battery is present first. The AdapterCurrentLimit1 and AdapterCurrentLimit2 registers can be read back to verify their content.

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To set a second level adapter current limit, write a 16-bit AdapterCurrentLimit2 (0x3BH or 0b00111011) command using the Write-word protocol shown in Figure 24 and the data format as shown in Table 5 for a 20mΩ R_{S1} or Table 6 for a 10mΩ R_{S1}.

The AdapterCurrentLimit2 register has the same specification as the AdapterCurrentLimit1 register. See "Two-Level Adapter Current Limit" on page 35 for detailed operation.

TABLE 5. AdapterCurrentLimit1 REGISTER 0x3FH AND AdapterCurrentLimit2 REGISTER 0x3BH (11-BIT, 4mA STEP, 20mΩ SENSE RESISTOR, x18)

BIT	DESCRIPTION
<1:0>	Not used
<2>	0 = Add 0mA of adapter current limit. 1 = Add 4mA of adapter current limit.
<3>	0 = Add 0mA of adapter current limit. 1 = Add 8mA of adapter current limit.
<4>	0 = Add 0mA of adapter current limit. 1 = Add 16mA of adapter current limit.
<5>	0 = Add 0mA of adapter current limit. 1 = Add 32mA of adapter current limit.
<6>	0 = Add 0mA of adapter current limit. 1 = Add 64mA of adapter current limit.
<7>	0 = Add 0mA of adapter current limit. 1 = Add 128mA of adapter current limit.
<8>	0 = Add 0mA of adapter current limit. 1 = Add 256mA of adapter current limit.
<9>	0 = Add 0mA of adapter current limit. 1 = Add 512mA of adapter current limit.
<10>	0 = Add 0mA of adapter current limit. 1 = Add 1024mA of adapter current limit.
<11>	0 = Add 0mA of adapter current limit. 1 = Add 2048mA of adapter current limit.
<12>	0 = Add 0mA of adapter current limit. 1 = Add 4096mA of adapter current limit.
<13:15>	Not used
Maximum	<12:4> = 10111110000 6080mA

TABLE 6. AdapterCurrentLimit1 REGISTER 0x3FH AND AdapterCurrentLimit2 REGISTER 0x3BH (11-BIT, 8mA STEP, 10mΩ SENSE RESISTOR, x18)

BIT	DESCRIPTION
<1:0>	Not used.
<2>	0 = Add 0mA of adapter current limit. 1 = Add 8mA of adapter current limit.
<3>	0 = Add 0mA of adapter current limit. 1 = Add 16mA of adapter current limit.
<4>	0 = Add 0mA of adapter current limit. 1 = Add 32mA of adapter current limit.
<5>	0 = Add 0mA of adapter current limit. 1 = Add 64mA of adapter current limit.
<6>	0 = Add 0mA of adapter current limit. 1 = Add 128mA of adapter current limit.

TABLE 6. AdapterCurrentLimit1 REGISTER 0x3FH AND AdapterCurrentLimit2 REGISTER 0x3BH (11-BIT, 8mA STEP, 10mΩ SENSE RESISTOR, x18) (Continued)

BIT	DESCRIPTION
<7>	0 = Add 0mA of adapter current limit. 1 = Add 256mA of adapter current limit.
<8>	0 = Add 0mA of adapter current limit. 1 = Add 512mA of adapter current limit.
<9>	0 = Add 0mA of adapter current limit. 1 = Add 1024mA of adapter current limit.
<10>	0 = Add 0mA of adapter current limit. 1 = Add 2048mA of adapter current limit.
<11>	0 = Add 0mA of adapter current limit. 1 = Add 4096mA of adapter current limit.
<12>	0 = Add 0mA of adapter current limit. 1 = Add 8192mA of adapter current limit.
<13:15>	Not used
Maximum	<12:4> = 10111110000 12160mA

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SETTING TWO-LEVEL ADAPTER CURRENT LIMIT DURATION

For a two-level adapter current limit, write a 16-bit T1 and T2 command (0x38H or 0b00111000) using the Write-word protocol shown in Figure 24 and the data format shown in Table 5 or Table 6 to set the AdapterCurrentLimit1 duration t1. Write a 16-bit T2 command (0x38H or 0b00111000) to set AdapterCurrentLimit2 duration t2. The T1 and T2 registers accept any command, but only the valid register bits are written. See "Two-Level Adapter Current Limit" on page 35 for detailed operation information.

TABLE 7. T1 AND T2 REGISTER 0x38H

BIT	DESCRIPTION
<2:0> T1	000 = 10ms (default) 001 = 20ms 010 = 15ms 011 = 5ms 100 = 1ms 101 = 0.5ms 110 = 0.1ms 111 = 0ms
<7:3>	Not used
<10:8> T2	000 = 10µs (default) 001 = 100µs 010 = 500µs 011 = 1ms 100 = 300µs 101 = 750µs 110 = 2ms 111 = 10ms
<15:11>	Not used

Setting Maximum Charging Voltage or System Regulating Voltage

To set the maximum charging voltage or the system regulating voltage, write a 16-bit MaxSystemVoltage command (0x15H or 0b00010101) using the Write-word protocol shown in Figure 24 on page 18 and the data format shown in Table 8.

The maximum system voltage range is 8mV to 18.304V. The MaxSystemVoltage register accepts any voltage command but only the valid register bits are written to the register and the maximum values is clamped at 18.304V. The ISL9238 accepts a 0V command, but the register value does not change.

The MaxSystemVoltage register sets the battery full charging voltage limit. The MaxSystemVoltage register setting also is the system bus voltage regulation point when battery is absent or battery is present but is not in Charging mode. See "System Voltage Regulation" on page 36 for details.

The VSYS pin senses the battery voltage for maximum charging voltage regulation. The VSYS pin is also the system bus voltage regulation sense point.

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TABLE 8. MaxSystemVoltage REGISTER 0x15H (8mV STEP)

BIT	DESCRIPTION
<2:0>	Not used
<3>	0 = Add 0mV of charge voltage. 1 = Add 8mV of charge voltage.
<4>	0 = Add 0mV of charge voltage. 1 = Add 16mV of charge voltage.
<5>	0 = Add 0mV of charge voltage. 1 = Add 32mV of charge voltage.
<6>	0 = Add 0mV of charge voltage. 1 = Add 64mV of charge voltage.
<7>	0 = Add 0mV of charge voltage. 1 = Add 128mV of charge voltage.
<8>	0 = Add 0mV of charge voltage. 1 = Add 256mV of charge voltage.
<9>	0 = Add 0mV of charge voltage. 1 = Add 512mV of charge voltage.
<10>	0 = Add 0mV of charge voltage. 1 = Add 1024mV of charge voltage.
<11>	0 = Add 0mV of charge voltage. 1 = Add 2046mV of charge voltage.
<12>	0 = Add 0mV of charge voltage. 1 = Add 4096mV of charge voltage.
<13>	0 = Add 0mV of charge voltage. 1 = Add 8192mV of charge voltage.
<14>	0 = Add 0mV of charge voltage. 1 = Add 16384mV of charge voltage.
<15>	Not used
Maximum	18304mV

Setting Minimum System Voltage

To set the minimum system voltage, write a 16-bit MinSystemVoltage command (0x3EH or 0b00111110) using the Write-word protocol shown in Figure 24 on page 18 and the data format as shown in Table 9.

The minimum system voltage range is 256mV to 13.824V. The MinSystemVoltage register accepts any voltage command, but only the valid register bits are written to the register. The MinSystemVoltage register value should be set lower than the MaxSystemVoltage register value and the maximum value is clamped at 13.824V.

The MinSystemVoltage register sets the battery voltage threshold for entry and exit of the Trickle Charging mode and for entry and exit of the Learn mode. The VBAT pin senses the battery voltage to compare with the MinSystemVoltage register setting. See "Trickle Charging" on page 36 and "Battery Learn Mode" on page 35 for details.

The MinSystemVoltage register setting also is the system voltage regulation point when the device is in Trickle Charging mode. The CSON pin is the system voltage regulation sense point in Trickle Charging mode. See "System Voltage Regulation" on page 36" for details.

TABLE 9. MinSystemVoltage REGISTER 0x3EH

BIT	DESCRIPTION
<7:0>	Not used
<8>	0 = Add 0mV of charge voltage. 1 = Add 256mV of charge voltage.
<9>	0 = Add 0mV of charge voltage. 1 = Add 512mV of charge voltage.
<10>	0 = Add 0mV of charge voltage. 1 = Add 1024mV of charge voltage.
<11>	0 = Add 0mV of charge voltage. 1 = Add 2046mV of charge voltage.
<12>	0 = Add 0mV of charge voltage. 1 = Add 4096mV of charge voltage.
<13>	0 = Add 0mV of charge voltage. 1 = Add 8192mV of charge voltage.
<15:14>	Not used
Maximum	13824mV

Setting PROCHOT# Threshold for Adapter Overcurrent Condition

To set the PROCHOT# assertion threshold for adapter overcurrent conditions, write a 16-bit ACProchot# command (0x47H or 0b01000111) using the Write-word protocol shown in Table 24 on page 18 and the data format shown in Table 10 on page 23. By using the recommended current sense resistor values, the register's LSB always translates to 128mA of adapter current. The ACProchot# register accepts any current command but only the valid register bits are written to the register and the maximum value is clamped at 6400mA for R_{S1} = 20mΩ.

After POR, the ACProchot# register is reset to 0x0C00H. The ACProchot# register can be read back to verify its content.

If the adapter current exceeds the ACProchot# register setting, PROCHOT# signal asserts after the debounce time programmed by the Control2 register Bit<10:9> and latches on for a minimum time programmed by Control2 register Bit<8:6>.

TABLE 10. ACProchot# REGISTER 0x47H (20mΩ SENSING RESISTOR, 128mA STEP, x18 GAIN)

BIT	DESCRIPTION
<6:0>	Not used
<7>	0 = Add 0mA of ACProchot# threshold. 1 = Add 128mA of ACProchot# threshold.
<8>	0 = Add 0mA of ACProchot# threshold. 1 = Add 256mA of ACProchot# threshold.
<9>	0 = Add 0mA of ACProchot# threshold. 1 = Add 512mA of ACProchot# threshold.
<10>	0 = Add 0mA of ACProchot# threshold. 1 = Add 1024mA of ACProchot# threshold.
<11>	0 = Add 0mA of ACProchot# threshold. 1 = Add 2048mA of ACProchot# threshold.
<12>	0 = Add 0mA of ACProchot# threshold. 1 = Add 4096mA of ACProchot# threshold.
<15:13>	Not used
Maximum	<12:7> = 110010, 6400mA

Setting PROCHOT# Threshold for Battery Over Discharging Current Condition

To set the PROCHOT# signal assertion threshold for battery over discharging current conditions, write a 16-bit DCProchot# command (0x48H or 0b01001000) using the Write-word protocol shown in Figure 24 on page 18 and the data format shown in Table 11. By using the recommended current sense resistor values, the register's LSB always translates to 256mA of adapter current. The DCProchot# register accepts any current command, but only the valid register bits are written to the register and the maximum values is clamped at 12.8A for R_{S2} = 10mΩ.

After POR, the DCProchot# register is reset to 0x1000H. The DCProchot# register can be read back to verify its content.

If the battery discharging current exceeds the DCProchot# register setting, the PROCHOT# signal asserts after the debounce time programmed by the Control2 register Bit<10:9> and latches on for a minimum time programmed by Control2 register Bit<8:6>.

In battery only and Low Power mode, the DCProchot# threshold is set by Control0 register Bit<4:3>.

In battery only mode, the DCProchot# function works only when PSYS is enabled, because enabling PSYS activates the internal comparator reference. The Information register Bit<15> indicates whether the internal comparator reference is active. When the adapter is present, the internal comparator reference is always active.

TABLE 11. DCPROCHOT# REGISTER 0x48H (10mΩ SENSING RESISTOR, 256mA STEP, x18 GAIN)

BIT	DESCRIPTION
<7:0>	Not used
<8>	0 = Add 0mA of DCProchot# threshold. 1 = Add 256mA of DCProchot# threshold.
<9>	0 = Add 0mA of DCProchot# threshold. 1 = Add 512mA of DCProchot# threshold.
<10>	0 = Add 0mA of DCProchot# threshold. 1 = Add 1024mA of DCProchot# threshold.
<11>	0 = Add 0mA of DCProchot# threshold. 1 = Add 2048mA of DCProchot# threshold.
<12>	0 = Add 0mA of DCProchot# threshold. 1 = Add 4096mA of DCProchot# threshold.
<13>	0 = Add 0mA of DCProchot# threshold. 1 = Add 8192mA of DCProchot# threshold.
<15:14>	Not used.
Maximum	<13:8> = 110010, 12800mA

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Setting PROCHOT# Debounce Time and Duration Time

Control2 register Bit<10:9> configures the PROCHOT# signal debounce time before its assertion for ACProchot# and DCProchot#. The low system voltage PROCHOT# has a fixed debounce time of 10µs.

Control2 register Bit<8:6> configures the minimum duration of PROCHOT# signal when asserted.

Control Registers

The Control0, Control1, Control2, Control3, and Control4 registers configure the operation of the ISL9238. To change certain functions or options after POR, write an 8-bit control command to Control0 register (0x39H or 0b00111001) or a 16-bit control command to Control1 register (0x3CH or 0b00111100) or Control2 register (0x3DH or 0b00111101) or Control3 register (0x4CH or 0b00111100) or Control4 register (0x4EH or 0b00111101) using the Write-word protocol shown in Figure 24 on page 18 and the data format shown in Tables 12, 13, 14, and 15 on page 15, respectively.

TABLE 12. CONTROL0 REGISTER 0x39H

<table>
<tr><th>BIT</th><th>BIT NAME</th><th>DESCRIPTION</th></tr>
<tr><td><15:13></td><td>Forward Buck and Buck-Boost Phase Comparator Threshold Offset</td><td>Bit<15:13> adjusts the phase comparator threshold offset for forward buck and buck-boost
<table>
<tr><th>REV1</th><th>REV2</th></tr>
<tr><td>000 = 0mV</td><td>000 = 0mV</td></tr>
<tr><td>001 = 0.5mV</td><td>001 = 1mV</td></tr>
<tr><td>010 = 1mV</td><td>010 = 2mV</td></tr>
<tr><td>011 = 1.5mV</td><td>011 = 3mV</td></tr>
<tr><td>100 = -2mV</td><td>100 = -4mV</td></tr>
<tr><td>101 = -1.5mV</td><td>101 = -3mV</td></tr>
<tr><td>110 = -1mV</td><td>110 = -2mV</td></tr>
<tr><td>111 = -0.5mV</td><td>111 = -1mV</td></tr>
</table></td></tr>
<tr><td><12:10></td><td>Forward and Reverse Boost Phase Comparator Threshold Offset</td><td>Bit<12:10> adjusts the phase comparator threshold offset for forward and reverse boost
000 = 0mV
001 = 0.5mV
010 = 1mV
011 = 1.5mV
100 = -2mV
101 = -1.5mV
110 = -1mV
111 = -0.5mV</td></tr>
<tr><td><9,8,0></td><td>Reverse Buck and Buck-Boost Phase Comparator Threshold Offset</td><td>Bit<9,8,0> adjusts phase comparator threshold offset for forward and reverse boost
<table>
<tr><th>REV1</th><th>REV2</th></tr>
<tr><td>000 = 0mV</td><td>000 = 0mV</td></tr>
<tr><td>001 = 0.5mV</td><td>001 = 1mV</td></tr>
<tr><td>010 = 1mV</td><td>010 = 2mV</td></tr>
<tr><td>011 = 1.5mV</td><td>011 = 3mV</td></tr>
<tr><td>100 = -2mV</td><td>100 = -4mV</td></tr>
<tr><td>101 = -1.5mV</td><td>101 = -3mV</td></tr>
<tr><td>110 = -1mV</td><td>110 = -2mV</td></tr>
<tr><td>111 = -0.5mV</td><td>111 = -1mV</td></tr>
</table></td></tr>
<tr><td><7></td><td>SMBus Timeout</td><td>The ISL9238 includes a timer to insure the SMBus master is active and to prevent overcharging the battery. If the adapter is present and if the ISL9238 does not receive a write to the MaxChargeVoltage or ChargeCurrentLimit register within 175s, ISL9238 terminates charging. If a timeout occurs, writing the MaxChargeVoltage or ChargeCurrentLimit register re-enables charging.
0 = Enable the SMBus timeout function.
1 = Disable the SMBus timeout function.</td></tr>
<tr><td><6:5></td><td>High-Side FET Short Detection Threshold</td><td>Bit<6:5> configures the high-side FET short detection PHASE node voltage threshold during low-side FET turning on.
00 = 400mV (default)
01 = 500mV
10 = 600mV
11 = 800mV</td></tr>
</table>

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TABLE 12. CONTROL0 REGISTER 0x39H (Continued)

BIT	BIT NAME	DESCRIPTION
<4:3>	DCProchot# Threshold in Battery Only Low Power Mode	Bit<4:3> only configures the battery discharging current DCProchot# threshold in battery only Low Power mode indicated by the Information1 register 0x3A Bit<15>. If PSYS is enabled, the battery discharge current DCProchot# threshold is set by the DCProchot# register 0x48 setting. Bit<4:3> | R_{s2} = 10mΩ (A) | R_{s2} = 20mΩ (A) | R_{s2} = 5mΩ (A) 00 | 12 (Default) | 6 | 24 01 | 10 | 5 | 20 10 | 8 | 4 | 16 11 | 6 | 3 | 12
<2>	Input Voltage Regulation Loop	Bit<2> disables or enables the input voltage regulation loop. 0 = Enable (default) 1 = Disable
<1>		Not used

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TABLE 13. CONTROL1 REGISTER 0x3CH

BIT	BIT NAME	DESCRIPTION
<15:14>	General Purpose Comparator Assertion Debounce Time	Bit<15:14> configures the general purpose comparator assertion debounce time. 00 = 2µs (default) 01 = 12µs 10 = 2ms 11 = 5s
<13>	Exit Learn Mode Option	Bit<13> provides the option to Exit Learn mode when the battery voltage is lower than the MinSystemVoltage register setting. 0 = Stay in Learn mode even if V_{BAT} < MinSystemVoltage register setting (default) 1 = Exit Learn mode if V_{BAT} < MinSystemVoltage register setting
<12>	Learn Mode	Bit<12> enables or disables the Battery Learn mode. 0 = Disable (default) 1 = Enable To enter Learn mode, BATGONE pin needs to be low, that is, battery must be present.
<11>	OTG Function	Bit<11> enables or disables OTG function. 0 = Disable (default) 1 = Enable
<10>	Audio Filter	Bit<10> enables or disables the audio filter function. 0 = Disable (default) 1 = Enable
<9:8>	Switching Frequency	Bit<9:8> configures the switching frequency and overrides the switching frequency set by PROG pin. 00 = Switching frequency set by PROG pin (default) 01 = 839kHz 10 = 723kHz 11 = 635kHz To keep the switching frequency set by PROG pin resistor, leave Bit<9:8> as it is or write code 00, which sets the same frequency as the PROG pin resistor does.
<7>		Not used, When writing, write 0
<6>	Turbo	Bit<6> enables or disables Turbo mode. When the turbo function is enabled, the BGATE FET turns on in Turbo mode. See Table 24 on page 35 for the BGATE ON/OFF truth table. 0 = Enable (default) 1 = Disable
<5>	AMON/BMON Function	Bit<5> enables or disables the current monitor function AMON and BMON. 0 = Enable AMON/BMON (default) 1 = Disable AMON/BMON Bit<5> is only valid in battery only mode. When adapter is present, AMON/BMON is automatically enabled and Bit<5> becomes invalid.

TABLE 13. CONTROL1 REGISTER 0x3CH (Continued)

BIT	BIT NAME	DESCRIPTION
<4>	AMON or BMON	Bit<4> selects AMON or BMON as the output of AMON/BMON pin. 0 = AMON (default) 1 = BMON
<3>	PSYS	Bit<3> enables or disables the system power monitor PSYS function. 0 = Disable (default) 1 = Enable
<2>	VSYS	Bit<2> enables or disables the buck-boost charger switching VSYS output. When disabled, the ISL9238 stops switching and forces the BGATE FET on. 0 = Enable (default) 1 = Disable
<1:0>	Low_VSYS_Prochot# Reference	Bit<1:0> configures the Low_VSYS_Prochot# assertion threshold. 00 = 6.0V (default) 01 = 6.3V 10 = 6.6V 11 = 6.9V For 1-cell configuration, the Low_VSYS_Prochot# assertion threshold is fixed 2.4V.

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TABLE 14. CONTROL2 REGISTER 0x3DH

BIT	BIT NAME	DESCRIPTION
<15:14>	Trickle Charging Current	Bit<15:14> configures the charging current in Trickle Charging mode. 00 = 256mA (default) 01 = 128mA 10 = 64mA 11 = 512mA
<13>	OTG Function Enable Debounce Time	Bit<13> configures the OTG function debounce time from when the ISL9238 receives the OTG enable command. 0 = 1.3s (default) 1 = 150ms
<12>	Two-Level Adapter Current Limit Function	Bit<12> enables or disables the two-level adapter current limit function. 0 = Disable (default) 1 = Enable
<11>	Adapter Insertion to Switching Debounce	Bit<11> configures the debounce time from adapter insertion to ACOK asserted high. 0 = 1.3s (default) 1 = 150ms After V_{DD} POR, for the first time adapter plugged in, the ASGATE turn-on delay is always 150ms, regardless of the Bit<11> setting. This bit only sets the ASGATE turn-on delay after ASGATE turns off at least one-time when V_{DD} is above it POR value and Bit<11> default is 0 for 1.3s.
<10:9>	PROCHOT# Debounce	Bit<10:9> configures the PROCHOT# debounce time before its assertion for ACProchot# and DCProchot#. 00: 7µs (default) 01: 100µs 10: 500µs 11: 1ms The Low_VSYS_Prochot# has fixed 10µs debounce time.
<8:6>	PROCHOT# Duration	Bit<8:6> configures the minimum duration of PROCHOT# signal when asserted. 000 = 10ms (default) 001 = 20ms 010 = 15ms 011 = 5ms 100 = 1ms 101 = 500µs 110 = 100µs 111 = 0s
<5>	ASGATE in OTG Mode	Bit<5> turns on or off the ASGATE FET in OTG mode. 0 = Turn ON ASGATE in OTG mode (default) 1 = Turn OFF ASGATE in OTG mode

TABLE 14. CONTROL2 REGISTER 0x3DH (Continued)

BIT	BIT NAME	DESCRIPTION
<4>	CMIN Reference	Bit<4> configures the general purpose comparator reference voltage. 0 = 1.2V (default) 1 = 2V
<3>	General Purpose Comparator	Bit<3> enables or disabled the general purpose comparator. 0 = Enable (default) 1 = Disable
<2>	CMOUT Polarity	Bit<2> configures the general purpose comparator output polarity when asserted. The comparator reference voltage is connected at the inverting input node. 0 = CMOUT is High when CMIN is higher than the reference (default) 1 = CMOUT is Low when CMIN is higher than the reference
<1>	WOCP Function	Bit<1> enables or disables the WOC (Way Overcurrent) fault protection function. 0 = Enable WOCP (default) 1 = Disable WOCP
<0>	Battery OVP Function	Bit<0> enables or disables the Battery OV (Overvoltage) fault protection function. 0 = Disable Battery OVP (default) 1 = Enable Battery OVP

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TABLE 15. CONTROL3 REGISTER 0x4CH

BIT	BIT NAME	DESCRIPTION
<15>	Reread PROG Pin Resistor	Bit<15> reread PROG pin resistor or not. 0 = Reread PROG pin resistor 1 = Do not reread PROG pin resistor
<14>	Reload ACLIM When Adapter Is Plugged In	Bit<14> reload the AdapterCurrentLimit1 register set by PROG pin resistor. 0 = Reload AdapterCurrentLimit1 register 1 = Do not reload
<13>	Autonomous Charging Termination Time	Bit<13> configures autonomous charging termination time. 0 = 20ms 1 = 200ms
<12:11>	Charger Timeout	Bit<12:11> configures SMBus charger timeout time. 00 = 175s (default) 01 = 87.5s 10 = 43.75s 11 = 5s
<10>	BGATE OFF	Bit<10> enables or disables Battery Ship mode. 0 = Idle 1 = Force BGATE MOSFET OFF (enable Battery Ship mode)
<9>	PSYS Gain	Bit<9> configures the system power monitor PSYS output gain. 0 = 1.44µA/W (default) 1 = 0.723µA/W
<8>	Exit IDM Timer	Bit<8> configures the Ideal Diode mode exit timer when the battery discharge current is less than 300mA. 0 = 40ms (default) 1 = 80ms
<7>	Autonomous Charging Mode	Bit<7> enables Autonomous Charging mode. 0 = Enable Autonomous Charging mode 1 = Battery charging current control through SMBus
<6>	AC and CC Feedback Gain	Bit<6> configures AC and CC feedback gain for high current. 0 = Idle 1 = x0.5
<5>	Input Current Limit Loop	Bit<5> disables the input current limit loop. 0 = Enable input current limit loop 1 = Disable input current limit loop
<4>	Input Current Limit Loop when BATGONE = 1	Bit<4> disables the input current limit loop when BATGONE = 1. 0 = Enable ACLIM when BATGONE = 1 1 = Disable ACLIM when BATGONE = 1

TABLE 15. CONTROL3 REGISTER 0x4CH (Continued)

BIT	BIT NAME	DESCRIPTION
<3>	AMON/BMON Direction	Bit<3> configures AMON/BMON direction. 0 = Adapter current monitor/battery charging current monitor 1 = OTG output current monitor/battery discharging current monitor
<2>	Digital Reset	Bit<2> resets all SMBus register values to the POR default values. 0 = Idle 1 = Reset
<1>	Buck-Boost Switching Period	Bit<1> configures the switching period in Buck-Boost mode 0 = x1 1 = x2 (half switching frequency)
<0>	OTG Start-Up Delay	Bit<0> shorts the OTG start-up time 0 = Idle 1 = Short OTG start-up time from 150ms to 1ms when Control2 register Bit<13> = 1 for 150ms

TABLE 16. CONTROL4 REGISTER 0x4EH

BIT	BIT NAME	DESCRIPTION
<15:8>		Not used
<7>	OTGCURRENT PROCHOT#	Bit<6> enables or disables trigger PROCHOT# with OTGCURRENT 0 = Disable 1 = Enable
<6>	BATGONE PROCHOT#	Bit<6> enables or disables trigger PROCHOT# with BATGONE 0 = Disable 1 = Enable
<5>	ACOK PROCHOT#	Bit<6> enables or disables trigger PROCHOT# with ACOK 0 = Disable 1 = Enable
<4>	Comparator PROCHOT#	Bit<6> enables or disables trigger PROCHOT# with General Purpose Comparator rising. 0 = Disable 1 = Enable
<3:2>	ACOK falling or BATGONE Rising Debounce	Bit<3:2> configures the debounce time from ACOK falling or BATGONE rising to PROCHOT# trip. 00 = 2µs 01 = 25µs 10 = 125µs 11 = 250µs
<1>	PROCHOT# Clear	Bit<1> clears PROCHOT#. 0 = Idle 1 = Clear PROCHOT#
<0>	PROCHOT# Latch	Bit<0> manually resets PROCHOT#. 0 = PROCHOT# signal auto-clear 1 = Hold PROCHOT# low when tripped

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OTG Voltage Register

The OTG voltage register contains the SMBus readable and writable OTG mode output regulation voltage reference. The default is 5.004V. This register accepts any voltage command but only the valid register bits are written to the register and the maximum value is clamped at 27.456V.

TABLE 17. OTGVOLTAGE REGISTER 0x49H

BIT	DESCRIPTION
<2:0>	Not used
<3>	0 = Add 0mV of OTG voltage 1 = Add 12mV of OTG voltage
<4>	0 = Add 0mV of OTG voltage 1 = Add 24mV of OTG voltage
<5>	0 = Add 0mV of OTG voltage 1 = Add 48mV of OTG voltage
<6>	0 = Add 0mV of OTG voltage 1 = Add 96mV of OTG voltage
<7>	0 = Add 0mV of OTG voltage 1 = Add 192mV of OTG voltage
<8>	0 = Add 0mV of OTG voltage 1 = Add 384mV of OTG voltage
<9>	0 = Add 0mV of OTG voltage 1 = Add 768mV of OTG voltage
<10>	0 = Add 0mV of OTG voltage 1 = Add 1536mV of OTG voltage
<11>	0 = Add 0mV of OTG voltage 1 = Add 3072mV of OTG voltage
<12>	0 = Add 0mV of OTG voltage 1 = Add 6144mV of OTG voltage
<13>	0 = Add 0mV of OTG voltage 1 = Add 12288mV of OTG voltage
<14>	0 = Add 0mV of OTG voltage 1 = Add 24576mV of OTG voltage
<15>	Not used
Maximum	27456mV

OTG Current Register

The OTG current register contains the SMBus readable and writable OTG current limit. The default is 512mA. This register accepts any current command but only the valid register bits are written to the register and the maximum values is clamped at 4096mA for R_{S1} = 20mΩ.

TABLE 18. OTGCURRENT 0x4AH

BIT	DESCRIPTION
<6:0>	Not used
<7>	0 = Add 0mA of OTG current 1 = Add 128mA of OTG current
<8>	0 = Add 0mA of OTG current 1 = Add 256mA of OTG current
<9>	0 = Add 0mV of OTG current 1 = Add 512mA of OTG current
<10>	0 = Add 0mV of OTG current 1 = Add 1024mA of OTG current
<11>	0 = Add 0mV of OTG current 1 = Add 2048mA of OTG current
<12>	0 = Add 0mV of OTG current 1 = Add 4096mA of OTG current
<15:13>	Not used
Maximum	4096mA

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Input Voltage Register

The input voltage register contains the SMBus readable and writable input voltage limit. The default is 4.096V. This register accepts any current command but only the valid register bits are written to the register and the maximum values is clamped at 18.432V.

TABLE 19. INPUT VOLTAGE REGISTER 0x4BH

BIT	DESCRIPTION
<7:0>	Not used
<8>	0 = Add 0mV of Input voltage 1 = Add 341.3mV of Input voltage
<9>	0 = Add 0mA of Input voltage 1 = Add 682.6mV of Input voltage
<10>	0 = Add 0mV of Input voltage 1 = Add 1365.3mV of Input voltage
<11>	0 = Add 0mV of Input voltage 1 = Add 2730.6mV of Input voltage
<12>	0 = Add 0mV of Input voltage 1 = Add 5461.3mV of Input voltage
<13>	0 = Add 0mV of Input voltage 1 = Add 10922.6mV of Input voltage
<15:14>	Not used
Maximum	18432mV

Information Register

The information register contains SMBus readable information about manufacturing and Operating modes. Table 21 identifies the bit locations of the information available.

TABLE 20. INFORMATION1 REGISTER 0x3AH

BIT	DESCRIPTION
<3:0>	Not used
<4>	Bit<4> indicates whether the Trickle Charging mode is active. 0 = Trickle Charging mode is not active 1 = Trickle Charging mode is active
<9:5>	Not used
<10>	Bit<10> indicates whether the Low_VSYS_Prochot# is tripped. 0 = Low_VSYS Prochot# is not tripped 1 = Low_VSYS Prochot# is tripped
<11>	Bit<11> indicates whether DCProchot# is tripped. 0 = DCProchot# is not tripped 1 = DCProchot# is tripped
<12>	Bit<12> indicates whether ACProchot#/OTGCURRENTProchot# is tripped. 0 = ACProchot#/OTGCURRENTProchot# is not tripped 1 = ACProchot#/OTGCURRENTProchot# is tripped
<14:13>	Bit<14:13> indicates the active control loop. 00 = MaxSystemVoltage control loop is active 01 = Charging current loop is active 10 = Adapter current limit loop is active 11 = Input voltage loop is active
<15>	Bit<15> indicates whether the internal reference circuit is active. Bit<15> = 0 indicates that ISL9238 is in Low Power mode. 0 = Reference is not active 1 = Reference is active

TABLE 21. INFORMATION2 REGISTER 0x4DH

BIT	DESCRIPTION
<4:0>	Program Resister read out. # of battery cells Switching Frequency Adapter current Limit
<7:5>	Bit<7:5> indicates the ISL9238 is in operation mode. 001 = Boost Mode 010 = Buck Mode 011 = Buck-Boost Mode 101 = OTG Boost Mode 110 = OTG Buck Mode 111 = OTG Buck-Boost Mode
<11:8>	Bit<11:8> indicates the ISL9238 state machine status. 0000 = OFF 0001 = BATTERY 0010 = ADAPTER 0011 = ACOK 0100 = VSYS 0101 = CHARGE 0110 = ENOTG 0111 = OTG 1000 = ENLDO5 1001 = Not Applicable 1010 = TRIM/ENCHREF 1011 = ACHRG 1100 = CAL 1101 = AGON/AGONTG 1110 = WAIT/PSYS 1111 = ADPPSYS
<12>	Bit<10> indicates the BATGONE pin status 0 = Battery is present 1 = No battery
<13>	Bit<11> indicates the general purpose comparator output after debounce time. 0 = Comparator output is low 1 = Comparator output is high
<14>	Bit<12> indicates the ACOK pin status. 0 = No adapter 1 = Adapter is present
<15>	Not used

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Application Information

R3 Modulator

The ISL9238 uses the R3 (Robust Ripple Regulator) modulation scheme. The R3 modulator combines the best features of fixed frequency PWM and hysteretic PWM while eliminating many of their shortcomings. Figure 25 conceptually shows the R3 modulator circuit and Figure 26 shows the operation principles in steady state.

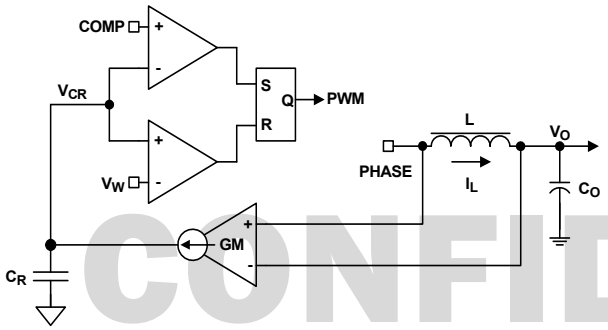

FIGURE 25. R3 MODULATOR

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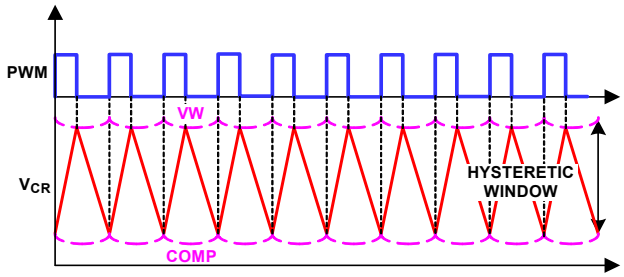

FIGURE 26. R3 MODULATOR OPERATION PRINCIPLES IN STEADY STATE

A fixed voltage window (VW window) between VW and COMP. The modulator charges the ripple capacitor C_R with a current source equal to $g_m(V_{IN}-V_O)$ during PWM on-time and discharges the ripple capacitor C_R with a current source equal to g_mV_O, during PWM off-time, where g_m is a gain factor. The C_r voltage V_{CR} therefore emulates the inductor current waveform. The modulator turns off the PWM pulse when V_{CR} reaches VW and turns on the PWM pulse when it reaches COMP.

Because the modulator works with V_{cr}, which is large amplitude and noise free synthesized signal, it achieves lower phase jitter than conventional hysteretic mode modulator.

Figure 27 shows the operation principles during dynamic response. The COMP voltage rises during dynamic response, turning on PWM pulses earlier and more frequently temporarily, which allows for higher control loop bandwidth than conventional fixed frequency PWM modulator at the same steady state switching frequency.

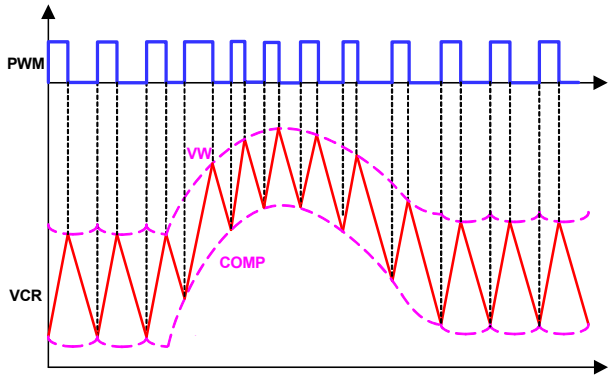

FIGURE 27. R3 MODULATOR OPERATION PRINCIPLES IN DYNAMIC RESPONSE

The R3 modulator can operate in Diode Emulation (DE) mode to increase light-load efficiency. In DE mode the low-side MOSFET conducts when the current is flowing from source-to-drain and does not allow reverse current, emulating a diode. As shown in Figure 28, when LGATE is on, the low-side MOSFET carries current, creating negative voltage on the phase node due to the voltage drop across the ON-resistance. The IC monitors the current by monitoring the phase node voltage. It turns off LGATE when the phase node voltage reaches zero to prevent the inductor current from reversing the direction and creating unnecessary power loss.

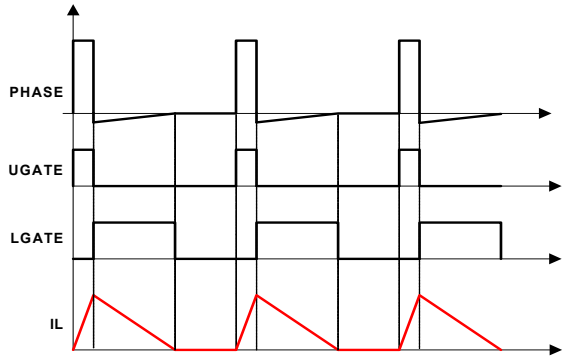

FIGURE 28. DIODE EMULATION

If the load current is light enough, as Figure 28 shows, the inductor current reaches and stays at zero before the next phase node pulse and the regulator is in Discontinuous Conduction Mode (DCM). If the load current is heavy enough, the inductor current never reaches 0A and the regulator is in CCM although the controller is in DE mode.

Figure 29 shows the operation principle in DE mode at light load. The load gets incrementally lighter in the three cases from top to bottom. The PWM on-time is determined by the VW window size; therefore is the same, making the inductor current triangle the same in the three cases. The R3 modulator clamps the ripple capacitor voltage V_{CR} in DE mode to make it mimic the inductor current. The COMP voltage takes longer to reach V_{CR}, naturally stretching the switching period. The inductor current triangles move further apart from each other, so that the inductor current average value is equal to the load current. The reduced switching frequency helps increase light-load efficiency.

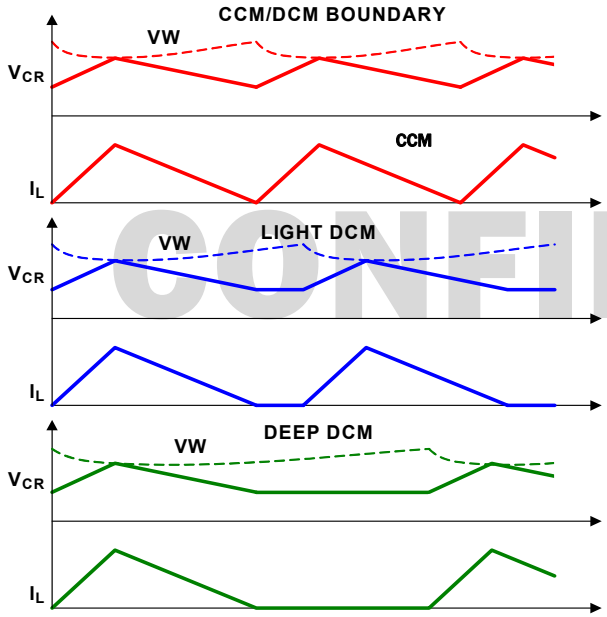

FIGURE 29. PERIOD STRETCHING

ISL9238 Buck-Boost Charger with USB OTG

The ISL9238 buck-boost charger drives an external N-channel MOSFET bridge comprised of two transistor pairs as shown in Figure 30. The first pair, Q1 and Q2, is a buck arrangement with the transistor center tap connected to an inductor "input" as is the case with a buck converter. The second transistor pair, Q3 and Q4, is a boost arrangement with the transistor center tap connected to the same inductor's "output" as is the case with a boost converter. This arrangement supports bucking from a voltage input higher than the battery and boosting from a voltage input lower than the battery.

In Buck mode, Q1 and Q2 turn on and off alternatively, while Q3 remains off and Q4 remains on.

In Boost mode, Q3 and Q4 turn on and off alternatively, while Q1 remains on and Q2 remains off.

In Buck-Boost mode, Q1 and Q3 turn on at the same time, Q3 turns off and Q4 turns on, Q1 turns off and Q2 turns on and after Q2 and Q4 turn off at the same time and Q1 and Q3 turn on again.

In OTG Buck mode, Q3 and Q4 turn on and off alternatively, while Q2 remains off and Q1 remains on.

In OTG Boost mode, Q1 and Q2 turn on and off alternatively, while Q4 remains on and Q3 remains off.

In OTG Buck-Boost mode, Q4 and Q2 turn on at the same time, Q2 turns off and Q1 turns on, Q4 turns off and Q3 turns on and after Q3 and Q1 turn off at the same time and Q4 and Q2 turn on again.

In OTG mode the output sensing point is the CSIP pin.

TABLE 22. OPERATION MODE

MODE	Q1	Q2	Q3	Q4
Buck	Control FET	Sync. FET	OFF	ON
Boost	ON	OFF	Control FET	Sync. FET
Buck-Boost	Control FET	Sync. FET	Control FET	Sync. FET
OTG Buck	ON	OFF	Sync. FET	Control FET
OTG Boost	Sync. FET	Control FET	OFF	ON
OTG Buck-Boost	Sync. FET	Control FET	Sync. FET	Control FET

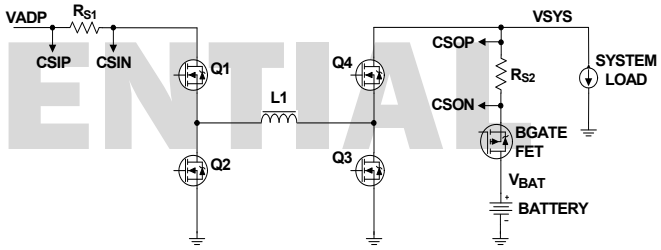

FIGURE 30. BUCK-BOOST CHARGER TOPOLOGY

The ISL9238 optimizes the Operation mode transition algorithm by considering the input and output voltage ratio and the load condition. When adapter voltage V_{ADP} is rising and is higher than 94% of the system bus voltage VSYS, the ISL9238 transitions from Boost mode to Buck-Boost mode; if V_{ADP} is higher than 120% of VSYS, the ISL9238 forcedly transitions from Buck-Boost mode to Buck mode at any circumstance. At heavier load, the mode transition point changes accordingly to accommodate the duty cycle change due to the power loss on the charger circuit.

When the adapter voltage V_{ADP} is falling and is lower than 106% the system bus voltage VSYS, ISL9238 transitions from Buck mode to Buck-Boost mode; if V_{ADP} is lower than 80% of VSYS, ISL9238 transitions from Buck-Boost mode to Boost mode.

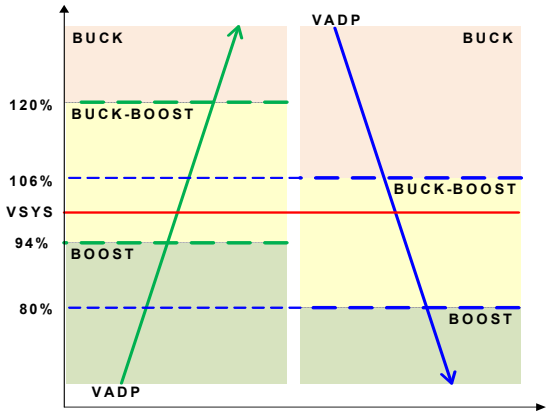

FIGURE 31. OPERATION MODE

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When the OTG function is enabled with the SMBus command and OTGEN pin, and if battery voltage V_{BAT} is higher than 5.2V, the ISL9238 operates in the OTG mode, there is one digital bit to control ASGATE. OTG mode is not available for 1-cell battery systems.

The ISL9238 connects the system voltage rail to either the output of the buck-boost switcher or the battery. In Turbo event, the ISL9238 turns on the BGATE FET to discharge the battery so the battery works with the adapter together to supply the system power.

Soft-Start

The ISL9238 includes a low power LDO with nominal 5V output, which input is OR-ed from VBAT and ADP pins. The ISL9238 also includes a high power LDO with nominal 5V output, which input is from DCIN pin connected to the adapter and the system bus through an external OR-ing diode circuit. Both LDO outputs are tied to the VDD pin to provide the bias power and gate drive power for the ISL9238. The VDDP pin is the ISL9238 gate drive power supply input. Use an R-C filter to generate the VDDP pin voltage from the VDD pin voltage.

When V_{DD} >2.7V, the ISL9238 digital block is activated and the SMBus register is ready to communicate with the master controller.

When VADP >3.2V, after 1.3s or 150ms debounce time set by Control2 register Bit<11> (after V_{DD} POR, for the first time adapter plugged in, the ASGATE turn on delay is always 150ms), ASGATE starts turning on with 10µA sink current. During the 1.3s or 150ms debounce time, ISL9238 uses the Renesas technique to check if the input bus is short or not; if CSIP <2V or ACIN <0.8V, the ASGATE does not turn on. The soft-start scheme carefully biases up the input capacitors and protect the back-to-back ASGATE FETs against potential damage caused by the inrush current.

Use a voltage divider from the adapter voltage to set the ACIN pin voltage. The ISL9238 monitors the ACIN pin voltage to determine the presence of the adapter. When V_{DD} >3.8V, the ACIN pin voltage exceeds 0.8V and ASGATE is fully turned on, the ISL9238 allows the external circuit to pull up the ACOK pin. When ACOK is asserted, ISL9238 start switching.

The ACOK is an open-drain output pin indicating the presence of the adapter and readiness of the adapter to supply power to the system bus. The ISL9238 actively pulls ACOK low in the absence of the adapter.

Before ASGATE turns ON, the ISL9238 sources 10µA of current out of the PROG pin and read the pin voltage to determine the PROG resistor value. The PROG resistor programs the configurations of the ISL9238.

In Battery Only mode, the ISL9238 enters Low Power mode if only battery is present. V_{DD} is 5V from the low power LDO to minimize the power consumption. V_{DD} becomes 5V when it exits the Low Power mode such as when PSYS is enabled.

Programming Charger Option

The resistor from the PROG pin to GND programs the configuration of the ISL9238 for the default number of battery cells in series, the default switching frequency, the default AdapterCurrentLimit1 register value and autonomous charging function. AdapterCurrentLimit2 register default value is 1.5A. Table 23 shows the programming options.

TABLE 23. PROG PIN PROGRAMMING OPTIONS

PROG-GND RESISTANCE (kΩ)			CELL #	DEFAULT SWITCHING FREQUENCY	AUTONOMOUS CHARGING	DEFAULT ACLimit1 Reg (A)
MIN	TYP 1%	MAX				
	0		1	733kHz	No	0.476
8.3	8.45	8.6		733kHz	No	1.5
14.5	14.7	14.9		1MHz	No	1.5
20.7	21.0	21.3		1MHz	No	0.476
27.7	28.0	28.3		733kHz	Yes	0.476
35.3	35.7	36.1		733kHz	Yes	1.5
42.7	43.2	43.7	2	733kHz	Yes	1.5
51.7	52.3	52.9		733kHz	Yes	0.476
61.2	61.9	62.6		1MHz	No	0.476
70.6	71.5	72.4		1MHz	No	1.5
81.5	82.5	83.5		733kHz	No	1.5
92.0	93.1	94.2		733kHz	No	0.476
104	105	106	3	733kHz	No	0.476
116	118	120		733kHz	No	1.5
131	133	135		1MHz	No	1.5
145	147	149		1MHz	No	0.476
160	162	164		733kHz	Yes	0.476
176	178	180		733kHz	Yes	1.5
194	196	198	4	733kHz	Yes	1.5
212	215	218		733kHz	Yes	0.476
234	237	240		1MHz	No	0.476
258	261	264		1MHz	No	1.5
284	287	290		733kHz	No	1.5
312	316	320		733kHz	No	0.476
344	348	352	1	733kHz	No	0.476

The ISL9238 uses the default number of cells in series as Table 23 shows and sets the default MaxSystemVoltage register value and default MinSystemVoltage register value accordingly.

The switching frequency can be changed through SMBus Control1 register Bit<9:8> after POR. See the SMBus Control1 register programming table on page 25 for detailed description.

Before ASGATE turns on, the ISL9238 sources 10µA current out of the PROG pin and reads the PROG pin voltage to determine the resistor value. However, application environmental noise may pollute the PROG pin voltage and cause incorrect reading. If noise is a concern, it is recommended to connect a capacitor from the PROG pin to GND to provide filtering. The resistor and the capacitor

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RC time constant should be less than 40µs so the PROG pin voltage can rise to steady state before the ISL9238 reads it.

If ISL9238 is powered up from the battery, it does not read the PROG resistor unless PSYS is enabled through SMBus Control1 register Bit<3>. In Battery Only mode, whenever PSYS is enabled, the ISL9238 reads the PROG pin resistor and resets the configuration to the default.

Whenever the adapter is plugged in, ISL9238 resets the AdapterCurrentLimit1 register to the default by reading the PROG pin resistor if it is not read before or by loading the previous reading result.

If PSYS is not enabled, the ISL9238 resets the MaxSystemVoltage and MinSystemVoltage registers to their default values according to the PROG pin cell number setting. If PSYS is enabled, the ISL9238 keeps the values in these two registers.

By default, the adapter current-sensing resistor R_{S1} is 20mΩ and battery current-sensing resistor R_{S2} is 10mΩ. Using this R_{S1} = 20mΩ and R_{S2} = 10mΩ option would result in 4mA/LSB correlation in the SMBus current commands.

If R_{S1} and R_{S2} values are different from this R_{S1} = 20mΩ and R_{S2} = 10mΩ option, the SMBus command needs to be scaled accordingly to obtain the correct current. Smaller current sense resistor values reduce the power loss while larger current sense resistor values give better accuracy.

If different current-sensing resistors are used, the R_{S1}:R_{S2} ratio should be kept as 2:1, the PSYS output can be scaled accordingly to reflect the total system power correctly.

The illustration in this datasheet is based on current-sensing resistors R_{S1} = 20mΩ and R_{S2} = 10mΩ unless otherwise specified.

Autonomous Charging Mode

This mode can be enabled/disabled by programming charging option resistor or SMBus Control3 register Bit<7>. When Autonomous Charging mode is enabled, this mode can be also disabled by writing to the SMBus ChargingCurrentLimit or MaxSystemVoltage commands.

The ISL9238 enters Autonomous Charging mode when the battery voltage is lower than MaxSystemVoltage -200mV per cell for 1ms debounce time and BGATE MOSFET is on.

In Autonomous Charging mode, the ISL9238 starts to charge the battery with 2A (with R_{S2} = 10mΩ), the PROCHOT# pin (Autonomous Charging mode indication pin) is pulled down to GND, and the 175s charging timeout timer is disabled. The ISL9238 exits from Autonomous Charging mode when the battery charging current is less than 200mA (with R_{S2} = 10mΩ) for 20ms or 200ms in CV loop. This autonomous charging termination time can be set by Control3 register Bit<13>. The ISL9238 re-enters Autonomous Charging mode when the battery voltage is discharged below MaxSystemVoltage - 200mV per cell. When ISL9238 stays in Autonomous Charging mode for 12hrs, which means the battery charging current is higher than 200mA and the battery can not be charged to MaxSystemVoltage for 12hrs, the ISL9238 stops charging the battery and exits Autonomous Charging mode.

Battery Ship Mode

When Control3 register Bit <10> is 1, BGATE MOSFET stays off for Battery Ship mode.

DE Operation

In DE operation mode, the ISL9238 uses a phase comparator to monitor the PHASE node voltage during the low-side switching FET on-time to detect the inductor current zero crossing. The phase comparator needs a minimum on-time of the low-side switching FET for it to recognize the inductor current zero crossing. If the low-side switching FET on-time is too short for the phase comparator to successfully recognize the inductor zero crossing, the ISL9238 may lose diode emulation ability. To prevent this, the ISL9238 uses a minimum low-side switching FET on-time. When the intended low-side switching FET on-time is shorter than the minimum value, the ISL9238 stretches the switching period to keep the low-side switching FET on-time at the minimum value, which causes the CCM switching frequency to drop below the set point.

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Power Source Selection

The ISL9238 automatically selects the adapter and/or the battery as the source for system power.

The BGATE pin drives a P-channel MOSFET gate that connects/disconnects the battery from the system and the switcher.

The ASGATE pin drives a pair of back-to-back common source PFETs to connect/disconnect the adapter from the system and the battery.

Use of the ASGATE pin is optional.

When the battery voltage, V_{BAT}, is higher than 2.4V and the adapter voltage V_{ADP} is less than 3.2V, the ISL9238 operates in Battery Only mode. During Battery Only mode, the ISL9238 turns on the BGATE FET to connect the battery to the system. In Battery Only mode, the ISL9238 consumes very low power, less than 20µA. The battery discharging current monitor BMON can be turned on during this mode to monitor the battery discharging current. If the battery voltage V_{BAT} is higher than 5.2V, the system power monitor PSYS function can also be turned on to monitor system power.

In Battery Only mode, the USB OTG function can be enabled when the battery voltage V_{BAT} is higher than 5.2V, see "USB OTG (On the Go)" on page 37 for details.

When the adapter voltage, V_{ADP}, is more than 3.2V, the ISL9238 turns on ASGATE. If VDD is higher than 3.8V, the ISL9238 enters Forward Buck, Forward Boost, or Forward Buck-Boost mode depending upon the adapter and system voltage VSYS duty cycle ratio. The system bus voltage is regulated at the voltage set on the MaxSystemVoltage register. If the charge current register is programmed (non-zero), the ISL9238 charges the battery either in Trickle Charging mode or Fast Charging mode, as long as BATGONE is low.

Battery Learn Mode

This mode of operation is used when it is desired to supply the system power from the battery even when the adapter is plugged in, such as calibration of the battery fuel gauge, hence the name “Battery Learn mode”.

The ISL9238 enters Battery Learn mode when it receives the SMBus Control command.

Upon entering Battery Learn mode, the ISL9238 turns on the BGATE FET.

In Battery Learn mode, the ISL9238 turns on BGATE, keeps ASGATE on but turns off the buck-boost switcher regardless of whether the adapter is present.

The three ways of exiting Battery Learn mode are:

- Receive Battery Learn mode exit command through SMBus.
- Battery voltage is less than MinSystemVoltage register setting (according to Control1 register Bit<12> setting).
- BATGONE pin voltage goes from logic LOW to HIGH.

In all these cases, the ISL9238 resumes switching immediately to supply power to the system bus from the adapter to prevent system voltage collapse.

Turbo Mode Support

Turbo mode refers to scenarios in which the system draws more power than the adapter’s power rating.

If the adapter current reaches the AdapterCurrentLimit1 register set value (or AdapterCurrentLimit2 register set value, if two-level adapter current limit function is enabled), or the adapter input voltage drops to the Input Voltage Regulation Reference set by the Control0 register 0x39H Bit<2>, the ISL9238 limits the input power by regulating the adapter current at AdapterCurrentLimit1/2 register set value, or by regulating the adapter voltage at the Input Voltage Regulation Reference point.

In Turbo mode, the system bus voltage VSYS drops automatically or the charging current drops automatically to limit the adapter input power. If the VSYS pin voltage is 150mV lower than the VBAT pin voltage, the BGATE FET turns on, so that the battery supplies the rest of the power required by the system.

If the ISL9238 detects 150mA charging current or if the battery discharging current is less than 200mA for longer than 40ms or 80ms, it turns off BGATE to exit Turbo mode. The Turbo mode exit timer can be configured through Control3 register 0x4C Bit<8>. See Table 24 for BGATE control logic.

TABLE 24. BGATE ON/OFF TRUTH TABLE

TURBO (CONTROL BIT)	CHARGECURRENT REGISTER	BGATE ON/OFF	
0 = ENABLE 1 = DISABLE	0 = ZERO 1 = NONZERO	SYSTEM LOAD NOT IN TURBO MODE RANGE	SYSTEM LOAD IN TURBO MODE RANGE
0	0	OFF	ON
0	1	ON for fast charge; Trickle charge is enabled	ON
1	0	OFF	OFF
1	1	ON for fast charge; Trickle charge is enabled	ON

Two-Level Adapter Current Limit

In a real system, Turbo event usually does not last very long. It is often no longer than milliseconds, a time length during which the adapter can supply current higher than its DC rating. The ISL9238 uses a two-level adapter current limit to fully take advantage of adapter’s surge capability and minimize the power drawn from the battery.

Figure 32 shows the two SMBus programmable adapter current limit levels, AdapterCurrentLimit1 and AdapterCurrentLimit2, as well as the durations t1 and t2. The two-level adapter current limit function is initiated when the adapter current is less than 100mA lower than the AdapterCurrentLimit1 register setting and it starts at AdapterCurrentLimit2 for t2 duration, then changes to AdapterCurrentLimit1 for t1 duration before repeating the pattern. These parameters can set the adapter current limit with an envelope that allows the adapter to temporarily output surge current without requiring the charger to enter Turbo mode. This operation maximizes battery life.

The AdapterCurrentLimit1 register value can be higher or lower than the AdapterCurrentLimit2 value.

The two-level adapter current limit function can be enabled and disabled through SMBus Control2 register Bit<12>. When the two-level adapter current limit function is disabled, only the AdapterCurrentLimit1 value is used as the adapter current limit. The AdapterCurrentLimit2 value is ignored.

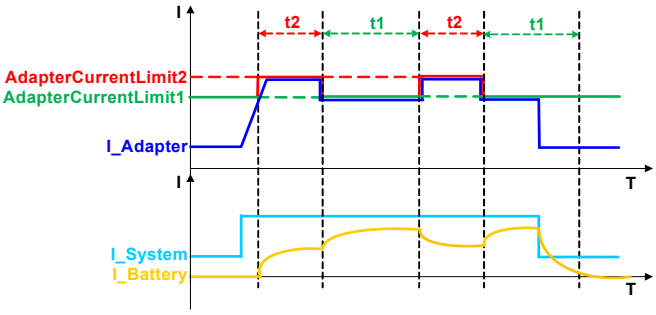

FIGURE 32. TWO-LEVEL ADAPTER CURRENT LIMIT

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Current Monitor

The ISL9238 provides an adapter current monitor/OTG current monitor or a battery charging current monitor/battery discharging current monitor through the AMON/BMON pin. The AMON output voltage is 18x (CSIP-CSIN) and 18x (CSIN-CSIP) voltage and the BMON output voltage is 18x (CSON-CSOP) and 36x (CSOP-CSON) voltage.

AMON and BMON functionality can be enabled or disabled through SMBus Control1 register Bit<5>, AMON or BMON can be selected through SMBus Control1 register Bit<4> and AMON/BMON direction can be configured through SMBus Control3 register Bit<3> as Table 13 on page 25 shows.

PSYS Monitor

The ISL9238 PSYS pin measures the instantaneous power consumption of the entire platform. The PSYS pin outputs a current source described by Equation 1.

$$I_{PSYS} = K_{PSYS} \times (V_{ADP} \times I_{ADP} + V_{BAT} \times I_{BAT}) \quad \text{(EQ. 1)}$$

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K_{PSYS} is based on current-sensing resistor R_{s1} = 20mΩ and R_{s2} = 10mΩ. V_{ADP} is the adapter voltage in V, I_{ADP} is the adapter current in A, V_{BAT} is the battery voltage and I_{BAT} is the battery discharging current. When the battery is discharging, I_{BAT} is a positive value; when the battery is being charged, I_{BAT} is a negative value. The battery voltage V_{BAT} is detected through CSON pin to maximize the power monitor accuracy in NVDC configuration Trickle Charge mode.

The R_{s1} to R_{s2} ratio must be 2:1 for a valid power calculation to occur. If the resistance values are higher (or lower) than the suggested values mentioned previously, K_{PSYS} is proportionally higher (or lower). As an example, if R_{s1} = 10mΩ and R_{s2} = 5mΩ, the output current is half that above for the same power. If the PSYS information is not needed, any R_{s1}:R_{s2} ratio is acceptable.

The PSYS gain can be configured through SMBus Control3 register Bit<9>. The default PSYS gain is set to 1.44µA/W and a 0.723µA/W PSYS gain option is available.

The PSYS information includes the power loss of the charger circuit and the actual power delivered to the system. The resistor R_{PSYS} connected between the PSYS pin and GND converts the PSYS information from current to voltage.

PSYS accuracy limits and a typical accuracy scan are shown in Figure 33.

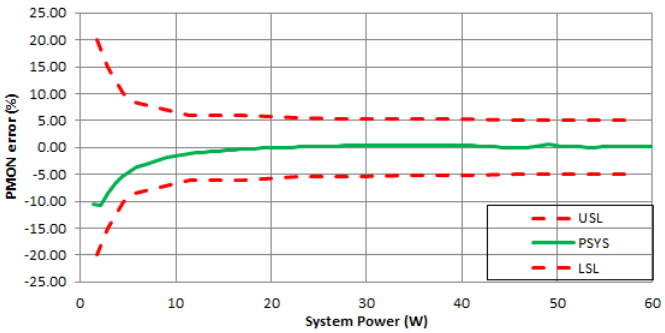

FIGURE 33. PSYS ACCURACY AND LIMITS

The PSYS function can be enabled or disabled through SMBus Control1 register Bit<3> as shown in Table 13 on page 25.

In Battery Only mode, the PSYS function cannot work if the battery voltage is less than 5.2V.

Trickle Charging

The ISL9238 supports trickle charging to an overly discharged battery. It can activate the trickle charging function when the battery voltage is lower than MinSystemVoltage setting. The VBAT pin is the battery voltage sense point for Trickle Charge mode.

To enable Trickle Charging, set the ChargeCurrent register to a non-zero value. To disable trickle charging, set the ChargeCurrent register to 0. See Table 24 on page 35 for trickle charging control logic.

The trickle charging current can be programmed to be 512mA, 256mA, 128mA or 64mA through SMBus Control2 register Bit<15:14> in Table 14 on page 26.

In Trickle Charging mode, the ISL9238 regulates the trickle charging current through the buck-boost switcher. Another independent control loop controls the BGATE FET so that the system voltage is maintained at the voltage set in the MinSystemVoltage register. The VSYS pin is the system voltage sensing point in Trickle Charging mode.

When the battery voltage is charged the MinSystemVoltage register value, the ISL9238 enters Fast Charging mode by limiting the charging current at the ChargeCurrentLimit register setting.

System Voltage Regulation

If the battery is absent, or if a battery is present but BGATE is turned off, the ISL9238 regulates the system bus voltage at the MaxSystemVoltage register setting. The VSYS pin senses the system bus voltage.

Charger Timeout

The ISL9238 includes a timer to insure the SMBus master is active and to prevent overcharging the battery. The ISL9238 terminates charging by turning off BGATE FET if the charger has not received a write command to the MaxSystemVoltage or ChargeCurrent register within 175s (SMBus Control3 register Bit<12:11> = 00). Charger timeout time can be configured through SMBus Control3 register Bit<12:11>. When the charging is terminated by the timeout, the ChargeCurrent register retains its value instead of resetting to zero. If a timeout occurs, MaxSystemVoltage or ChargeCurrent register must be written to re-enable charging.

The ISL9238 allows you to disable the charger timeout function through the SMBus Control0 register Bit<7> as Table 12 on page 24 shows.

USB OTG (On the Go)

When the OTG function is enabled with SMBus command and OTGEN pin and if battery voltage V_{BAT} is higher than 5.2V, the ISL9238 operates in the Reverse Buck, Reverse Boost, or Reverse Buck-Boost mode.

When ISL9238 receives the command to enable the OTG function, it starts switching after the 1.3s or 150ms debounce time set by Control2 register Bit<13>. When the OTG output voltage reaches the OTG output voltage set by register 0x49 Bit<14:3>, OTG power-good (OTGPG) asserts to High. Moreover, Control2 register Bit<5> can turn the ASGATE FET off to cut off the OTG output.

Before OTG mode starts switching, the CSIP pin voltage needs to drop below the OTG output overvoltage protection threshold (OTGVDAV + 100mV) first.

The default OTG output voltage is programmable up to 20V. The OTG Voltage register 0x49H can configure the OTG output voltage.

The default OTG output current is limited at 512mA through R_{S1}. The OTGCurrent register 0x4AH can adjust the OTG output current limit.

The ISL9238 includes the OTG output undervoltage and overvoltage protection functions. The UVP threshold is OTG output voltage -1.2V and the OVP threshold is OTG output voltage +1.2V.

When UV is detected, the ISL9238 stops switching and turns off ASGATE and deassert OTGPG after 32ms and after 1.3s or 150ms debounce time set by Control2 register Bit<13>, it resumes switching.

When OV is detected, the ISL9238 stops switching and deasserts OTGPG. It resumes switching after 100µs when OTG voltage drops below the OTG OV threshold.

BATGONE needs to be low to enable OTG mode. OTG mode is not available for 1-cell battery systems.

Stand-Alone Comparator

The ISL9238 includes a general purpose stand-alone comparator. The OTGEN/CMIN pin is the comparator input. The internal comparator reference is connected to the inverting input of the comparator and can be configured as 1.2V or 2V through SMBus Control2 register Bit<4>. The comparator output is the OTGPG/CMOUT pin and the output polarity can be configured through SMBus register bit when the comparator is tripped.

When Control2 register Bit<2> = 0 for normal comparator output polarity, if CMIN > Reference, CMOUT = High; if CMIN < Reference, CMOUT = Low.

When Control2 register Bit<2> = 1 for inversed comparator output polarity, if CMIN > Reference, CMOUT = Low; if CMIN < Reference, CMOUT = High.

In Battery Only mode, the stand-alone comparator is disabled unless PSYS is enabled through SMBus Control1 register Bit<3> to enable the internal reference, which is indicated through Information1 register Bit<15>.

Table 25 shows the OTG mode and the stand-alone comparator truth table.

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TABLE 25. OTG AND COMPARATOR TRUTH TABLE

				DESCRIPTION
Control1 Register 0x3C	Control2 Register 0x3D	PIN-20	PIN-26	
Bit<11> OTG Function Enable/Disable	Bit<3> Comparator Enable/Disable	OTGEN/CMIN	OTGPG/CMOUT	
0	0	Comparator Input Pin CMIN	Comparator Output Pin CMOUT	OTG function is disabled. Comparator is enabled.
0	1	X	X	Both OTG function and comparator are disabled.
1	0	Comparator Input Pin CMIN	Comparator Output Pin CMOUT	Both OTG function and comparator are enabled. OTG function is enabled when V_{BAT} > 5.2V and Control1 register Bit<11> = 1 without OTG power-good pin indication. While the Information1 register 0x3A Bit<6:5> = 11 indicates it is in OTG mode.
1	1	OTG Enable Input Pin OTGEN	OTG Power-Good Indication Pin OTGPG	Comparator is disabled. OTG function is enabled when V_{BAT} > 5.2V and ENOTG pin = High and Control1 register Bit<11> = 1

Adapter Overvoltage Protection

If the ADP pin voltage exceeds 23.4V for more than 10µs, an adapter overvoltage condition has occurred. The ISL9238 turns off the ASGATE MOSFETs to isolate the adapter from the system, deasserts the ACOK signal by pulling it low, and stops switching. BGATE turns on for the battery to support the system load. When ADP voltage drops below 23.04V from more than 100µs, it starts to turn on ASGATE and starts switching.

Battery Overvoltage Protection

If the VBAT pin voltage is higher than battery overvoltage threshold (Vbov) + MaxSystemVoltage for 1ms, it declares the battery overvoltage and stops switching. Battery overvoltage threshold are 4% of MaxSystemVoltage for the 1-cell battery setting and 2% of MaxSystemVoltage in 2-, 3-, and 4-cells setting. It resumes switching with 1ms debounce time when VBAT pin voltage drops 0.5xVbov + MaxSystemVoltage. The ISL9238 allows you to disable the battery overvoltage protection function through SMBus Control2 register Bit<0>.

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System Overvoltage Protection

The ISL9238 provides system rail overvoltage protection. If the system voltage VSYS is 800mV higher than MaxSystemVoltage register set value, it declares the system overvoltage and stops switching. It resumes switching without the 1.3s or 150ms debounce when VSYS drops 300mV below the system overvoltage threshold.

Way Overcurrent Protection (WOCP)

In the case that the system bus is shorted, either a MOSFET short or an inductor short, the input current could be high. The ISL9238 includes input overcurrent protection to turn off the ASGATE and stop switching.

The ISL9238 provides adapter current and battery discharging current WOCP (Way Overcurrent Protection) against MOSFET shorts, system bus shorts, and inductor shorts. The ISL9238 monitors the CSIP - CSIN voltage and CSON - VSYS voltage, compares them with the WOCP thresholds of 16A for adapter current and 21A for battery discharge current.

When the WOC comparator is tripped, the ISL9238 counts one time within each 10µs. Whenever the ISL9238 counts WOC seven times in 50ms, it turns off ASGATE, deasserts ACOK, and stops switching immediately. After the 1.3s or 150ms debounce time set by Control2 register Bit<11>, it goes through the start-up sequence to retry.

The WOCP function can be disabled through Control2 register Bit<1>.

Over-Temperature Protection

The ISL9238 stops switching for self protection when the junction temperature exceeds +140°C.

When the temperature falls below +120°C and after 100µs delay, the ISL9238 starts switching.

Switching Power MOSFET Gate Capacitance

The ISL9238 includes an internal 5V LDO output at the VDD pin, which can provide the switching MOSFET gate driver power through the VDDP pin with an RC filter. The 5V LDO output overcurrent protection threshold is 100mA, nominal. When selecting the switching power MOSFET, the MOSFET gate capacitance should be considered carefully to avoid overloading the 5V LDO, especially in Buck-Boost mode when four MOSFETs are switching at the same time. For one MOSFET, the gate drive current can be estimated by Equation 2:

$$I_{driver} = Q_g \bullet f_{SW} \quad \text{(EQ. 2)}$$

where:

- Q_g is the total gate charge, which can be found in the MOSFET datasheet
- f_{SW} is switching frequency

Adapter Input Filter

The adapter cable parasitic inductance and capacitance can cause some voltage ringing or an overshoot spike at the adapter connector node when the adapter is hot plugged in. This voltage spike can damage the ASGATE MOSFET or the ISL9238 pins connecting to the adapter connector node. One low cost solution is to add an RC snubber circuit at the adapter connector node to clamp the voltage spike shown in Figure 34. A practical value of the RC snubber is 2.2Ω to 2.2µF while the appropriate values and power rating should be carefully characterized based on the actual design. Meanwhile, it is not recommended to add a pure capacitor at the adapter connector node, which can cause an even bigger voltage spike due to the adapter cable or the adapter current path parasitic inductance.

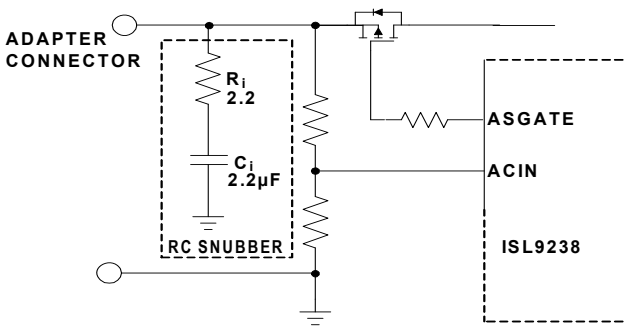

FIGURE 34. ADAPTER INPUT RC SNUBBER CIRCUIT

General Application Information

This design guide is intended to provide a high-level explanation of the steps necessary to design a single-phase power converter. It is assumed that the reader is familiar with many of the basic skills and techniques referenced in the following section. In addition to this guide, complete reference designs that include schematics, bill of materials, and example board layouts are provided.

Selecting the LC Output Filter

The duty cycle of an ideal buck converter in CCM is a function of the input and the output voltage. This relationship is written by Equation 3:

$$D = \frac{V_{OUT}}{V_{IN}} \quad \text{(EQ. 3)}$$

The output inductor peak-to-peak ripple current is written by Equation 4:

$$I_{P-P} = \frac{V_{OUT} \cdot (1 - D)}{f_{SW} \cdot L} \quad \text{(EQ. 4)}$$

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A typical step-down DC/DC converter has an I_{P-P} of 20% to 40% of the maximum DC output load current for a practical design. The value of I_{P-P} is selected based upon several criteria such as MOSFET switching loss, inductor core loss and the resistive loss of the inductor winding.

The DC copper loss of the inductor can be estimated by Equation 5:

$$P_{COPPER} = I_{LOAD}^{2} \cdot DCR \quad \text{(EQ. 5)}$$

where I_{LOAD} is the converter output DC current.

The copper loss can be significant so attention has to be given to the DCR selection. Another factor to consider when choosing the inductor is its saturation characteristics at elevated temperatures. A saturated inductor can destroy circuit components.

A DC/DC buck regulator must have output capacitance C_O into which ripple current I_{P-P} can flow. Current I_{P-P} develops a corresponding ripple voltage V_{P-P} across C_O, which is the sum of the voltage drop across the capacitor ESR and of the voltage change stemming from charge moved in and out of the capacitor. These two voltages are written by Equations 6 and 7:

$$\Delta V_{ESR} = I_{P-P} \cdot ESR \quad \text{(EQ. 6)}$$

$$V_C = \frac{I_{P-P}}{8 \cdot C_O \cdot f_{SW}} \quad \text{(EQ. 7)}$$

If the output of the converter has to support a load with high pulsating current, several capacitors need to be paralleled to reduce the total ESR until the required V_{P-P} is achieved. The inductance of the capacitor can cause a brief voltage dip if the load transient has an extremely high slew rate. Low inductance capacitors should be considered in this scenario. A capacitor dissipates heat as a function of RMS current and frequency. Be sure that I_{P-P} is shared by a sufficient quantity of paralleled capacitors so that they operate below the maximum rated RMS current at f_{SW}. Take into account that the rated value of a capacitor can fade as much as 50% as the DC voltage across it increases.

Selecting the Input Capacitor

The important parameters for the input capacitance are the voltage rating and the RMS current rating. For reliable operation, select capacitors with voltage and current ratings above the maximum input voltage and that are capable of supplying the RMS current required by the switching circuit. Their voltage rating should be at least 1.25x greater than the maximum input voltage, while a voltage rating of 1.5x is a preferred rating. Figure 35 is a graph of the input capacitor RMS ripple current, normalized relative to output load current, as a function of duty cycle and is adjusted for converter efficiency. The normalized RMS ripple current calculation is written as Equation 8:

$$I_{C_{IN}(RMS,NORMALIZED)} = \frac{I_{MAX} \cdot \sqrt{D \cdot (1 - D) + \frac{D \cdot k^2}{12}}}{I_{MAX}} \quad \text{(EQ. 8)}$$

where:

- I_{MAX} is the maximum continuous I_{LOAD} of the converter
- k is a multiplier (0 to 1) corresponding to the inductor peak-to peak ripple amplitude expressed as a ratio of I_{MAX} (0 to 1)
- D is the duty cycle that is adjusted to take into account the efficiency of the converter, which is written as Equation 9:

$$D = \frac{V_{OUT}}{V_{IN} \cdot EFF} \quad \text{(EQ. 9)}$$

In addition to the capacitance, some low ESL ceramic capacitance is recommended to decouple between the drain of the high-side MOSFET and the source of the low-side MOSFET.

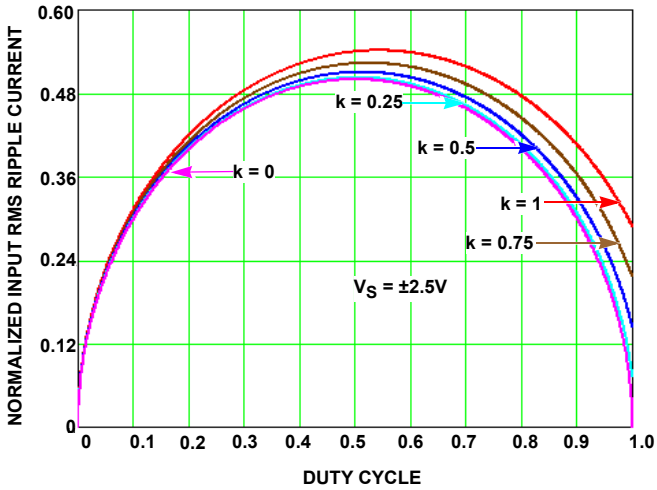

FIGURE 35. NORMALIZED RMS INPUT CURRENT AT EFF = 1

Selecting the Switching Power MOSFET

Typically, a MOSFET cannot tolerate even brief excursions beyond its maximum drain-to-source voltage rating. The MOSFETs used in the power stage of the converter should have a maximum VDS rating that exceeds the sum of the upper voltage tolerance of the input power source and the voltage spike that occurs when the MOSFET switches off.

Several power MOSFETs optimized for DC/DC converter applications are readily available. The preferred high-side MOSFET emphasizes low gate charge so that the device spends the least amount of time dissipating power in the linear region. Unlike the low-side MOSFET, which has the drain-to-source voltage clamped by its body diode during turn off, the High-Side (HS) MOSFET turns off with a VDS of approximately VIN - VOUT, plus the spike across it. The preferred Low-Side (LS) MOSFET emphasizes low $r_{DS(ON)}$ when fully saturated to minimize conduction loss. Note that this is an optimal configuration of MOSFET selection for low duty cycle applications (D < 50%). For higher output, low input voltage solutions, a more balanced MOSFET selection for HS and LS devices may be warranted.

The LS MOSFET's power loss can be assumed to be conductive only and is written as Equation 10:

$$P_{CON_LS} \approx I_{LOAD}^{2} \cdot r_{DS(ON)_LS} \cdot (1 - D) \quad \text{(EQ. 10)}$$

The HS MOSFET's conduction loss is written by Equation 11:

$$P_{CON_HS} = I_{LOAD}^{2} \cdot r_{DS(ON)_HS} \cdot D \quad \text{(EQ. 11)}$$

The HS MOSFET's switching loss is written as Equation 12:

$$P_{SW_HS} = \frac{V_{IN} \cdot I_{VALLEY} \cdot t_{SWON} \cdot f_{SW}}{2} + \frac{V_{IN} \cdot I_{PEAK} \cdot t_{SWOFF} \cdot f_{SW}}{2} \quad \text{(EQ. 12)}$$

where:

- I_{VALLEY} is the difference of the DC component of the inductor current minus 1/2 of the inductor ripple current
- I_{PEAK} is the sum of the DC component of the inductor current plus 1/2 of the inductor ripple current
- $t_{SW(ON)}$ is the time required to drive the device into saturation
- $t_{SW(OFF)}$ is the time required to drive the device into cut-off

Renesas recommends using a 2.2µF (10V) VDD/VDDP capacitor, which has an effective capacitance higher than 0.4µF at 5V and x1.6 effective capacitance at the BOOT1/BOOT2 pins at 5V.

Selecting the Bootstrap Capacitor

The selection of the bootstrap capacitor is written by Equation 13:

$$C_{BOOT} = \frac{Q_g}{\Delta V_{BOOT}} \quad \text{(EQ. 13)}$$

where:

- Q_g is the total gate charge required to turn on the HS MOSFET
- ΔV_{BOOT}, is the maximum allowed voltage decay across the boot capacitor each time the HS MOSFET is switched on.

As an example, suppose the HS MOSFET has a total gate charge Q_g, of 25nC at V_{GS} = 5V and a ΔV_{BOOT} of 200mV. The calculated bootstrap capacitance is 0.125µF; for a comfortable margin, select a capacitor that is double the calculated capacitance. In this example, 0.22µF will suffice. Use an X7R or X5R ceramic capacitor.

Renesas recommends using a bootstrap capacitor of 0.47µF (25V), which has an effective capacitance higher than 0.25µF at 5V and x50 effective high-side MOSFET gate capacitance.

DCIN Filter

An RC filter is connected at the DCIN pin. Renesas recommends connecting a 10Ω DCIN resistor between the DCIN pin and the VADP/VSYS diodes, and connecting a 4.7µF (50V) DCIN capacitor to GND that has an effective capacitance higher than 0.4µF at 20V.

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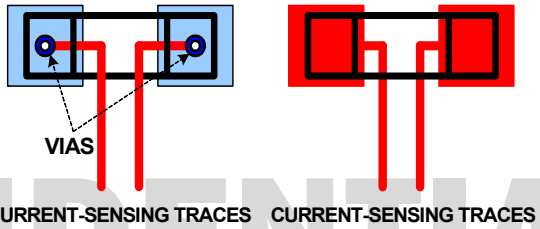
Layout

PIN NUMBER	PIN NAME	LAYOUT GUIDELINES
BOTTOM PAD	GND	Connect this ground pad to the ground plane through a low impedance path. Renesas recommends using at least five vias to connect to the ground planes in the PCB to ensure sufficient thermal dissipation directly under the IC.
1	CSON	Run two dedicated trace with sufficient width in parallel (close to each other to minimize the loop area) from the two terminals of the battery current-sensing resistor to the IC. Place the differential mode and common-mode RC filter components in the general proximity of the controller. Route the current-sensing traces through vias to connect the center of the pads; or route the traces into the pads from the inside of the current-sensing resistor. The following drawings show the two preferred ways of routing current-sensing traces. 
2	CSOP	
3	VSYS	Signal pin that provides feedback for the system bus voltage. Place the optional RC filter in the general proximity of the controller. Run a dedicated trace from system bus to the pin and do not route near the switching traces. Do not share the same trace with the signal routing to the DCIN pin OR diodes.
4	BOOT2	Switching pin. Place the bootstrap capacitor in the general proximity of the controller. Use decent wide trace. Avoid any sensitive analog signal trace from crossing over or getting close.
5	UGATE2	Run these two traces in parallel fashion with sufficient width. Avoid any sensitive analog signal trace from crossing over or getting close. Recommend routing the PHASE2 trace to high-side MOSFET source pin instead of general copper. Place the IC close to the switching MOSFETs gate terminals and keep the gate drive signal traces short for a clean MOSFET drive. The IC can be placed on the opposite side of the switching MOSFETs. Place the output capacitors as close as possible to the switching high-side MOSFET drain and the low-side MOSFET source; and use shortest PCB trace connection. Place these capacitors on the same PCB layer with the MOSFETs instead of on different layers and using vias to make the connection. Place the inductor terminal to the switching high-side MOSFET drain and low-side MOSFET source terminal as close as possible. Minimize this phase node area to lower the electrical and magnetic field radiation, but make this phase node area large enough to carry the current. Place the inductor and the switching MOSFETs on the same layer of the PCB.
6	PHASE2	
7	LGATE2	Switching pin. Run the LGATE2 trace in parallel with the UGATE2 and PHASE2 traces on the same PCB layer. Use sufficient width. Avoid any sensitive analog signal trace from crossing over or getting close.
8	VDDP	Place the decoupling capacitor in the general proximity of the controller. Run the trace connecting to VDD pin with sufficient width.
9	LGATE1	Switching pin. Run the LGATE1 trace in parallel with the UGATE1 and PHASE1 traces on the same PCB layer. Use sufficient width. Avoid any sensitive analog signal trace from crossing over or getting close.
10	PHASE1	Run these two traces in parallel fashion with sufficient width. Avoid any sensitive analog signal trace from crossing over or getting close. Recommend routing the PHASE1 trace to high-side MOSFET source pin instead of general copper. Place the IC close to the switching MOSFETs gate terminals and keep the gate drive signal traces short for a clean MOSFET drive. The IC can be placed on the opposite side of the switching MOSFETs. Place the input capacitors as close as possible to the switching high-side MOSFET drain and the low-side MOSFET source; and use shortest PCB trace connection. Place these capacitors on the same PCB layer with the MOSFETs instead of on different layers and using vias to make the connection. Place the inductor terminal to the switching high-side MOSFET drain and low-side MOSFET source terminal as close as possible. Minimize this phase node area to lower the electrical and magnetic field radiation but make this phase node area large enough to carry the current. Place the inductor and the switching MOSFETs on the same layer of the PCB.
11	UGATE1	

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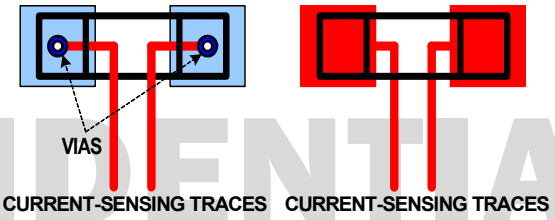
Layout (Continued)

PIN NUMBER	PIN NAME	LAYOUT GUIDELINES
12	BOOT1	Switching pin. Place the bootstrap capacitor in the general proximity of the controller. Use decent wide trace. Avoid any sensitive analog signal trace from crossing over or getting close.
13	ASGATE	Run this trace with sufficient width parallel to the ADP pin trace.
14	CSIN	Run two dedicated traces with sufficient width in parallel (close to each other to minimize the loop area) from the two terminals of the adapter current-sensing resistor to the IC. Place the Differential mode and common-mode RC filter components in the general proximity of the controller. Route the current-sensing traces through vias to connect the center of the pads; or route the traces into the pads from the inside of the current-sensing resistor. The following drawings show the two preferred ways of routing current-sensing traces. 
15	CSIP	
16	ADP	Run this trace with sufficient width parallel to the ASGATE pin trace.
17	DCIN	Place the OR diodes and the RC filter in the general proximity of the controller. Run the VADP trace and VSYS trace to the OR diodes with sufficient width.
18	VDD	Place the RC filter connecting with VDDP pin in the general proximity of the controller. Run the trace connecting to VDDP pin with sufficient width.
19	ACIN	Place the voltage divider resistors and the optional decoupling capacitor in the general proximity of the controller.
20	OTGEN/CMIN	No special consideration.
21	SDA	Digital pins. No special consideration. Run the SDA and SCL traces in parallel.
22	SCL	
23	PROCHOT#	Digital pin, open-drain output. No special consideration.
24	ACOK	Digital pin, open-drain output. No special consideration.
25	BATGONE	Digital pin. Place the 100kΩ resistor series in the BATGONE signal trace and the optional decoupling capacitor in the general proximity of the controller.
26	OTGPG/CMOUT	Digital pin, open-drain output. No special consideration.
27	PROG	Signal pin. Place the PROG programming resistor in the general proximity of the controller.
28	COMP	Place the compensation components in the general proximity of the controller. Avoid any switching signal from crossing over or getting close.
29	AMON/BMON	No special consideration. Place the optional RC filter in the general proximity of the controller.
30	PSYS	Signal pin, current source output. No special consideration.
31	VBAT	Place the optional RC filter in the general proximity of the controller. Run a dedicated trace from the battery positive connection point to the IC.
32	BGATE	Use sufficient width trace from the IC to the BGATE MOSFET gate. Place the capacitor from BGATE to ground close to the MOSFET.

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Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warranted. Please visit our website to make sure that you have the latest revision.

DATE	REVISION	CHANGE
Jul 19, 2019	FN8877.9	Updated pin descriptions for CSOP, CSON, BOOT2, VDDP, BOOT1, DCIN, and VDD. Changed VSYS - CSON to CSON-VSYS in the second paragraph in the Way Overcurrent Protection section on page 38. Added the last sentence to the Selecting the Switching Power MOSFET and Selecting the Bootstrap Capacitor sections on page 40. Added the DCIN Filter section on page 40.
May 13, 2019	FN8877.8	Abs Max table, CSIP-CSIN, CSOP-CSON, changed voltages from: -0.5V to +0.5V to: -0.3V to +0.3V. Updated disclaimer.
Aug 8, 2018	FN8877.7	Page 39, WOCP section. Two changes: 1. Changed WOCP currents to match new EC table values of 16A adapter and 21A battery. 2.Changed “CSON - CSOP” to “VSYS - CSON”
May 31, 2018	FN8877.6	Updated Ordering Information table by removing Notes 2 and 3, updated Note 1, and added tape and reel information to table. Removed PSYS Output Current specification (last row only). Removed Adapter Way Overcurrent Hysteresis specification. Removed Battery Discharge Way Overcurrent Hysteresis specification. Updated Adapter Way Overcurrent Rising Threshold test conditions, changed the typical value from “12” to “16”, and changed the maximum value from “18” to “25”. Updated Battery Discharge Way Overcurrent Rising Threshold test conditions, changed the typical value from “20” to “21”, and changed the maximum value from “32” to “33”. Added Notes 8 and 9 along with applicable cross-referencing. Updated Table 2 added 0x06 information to the Revision ID description. Removed About Intersil section and updated the disclaimer.
Nov 29, 2017	FN8877.5	Added Way Overcurrent Protection (WOCP) function to datasheet.
Oct 4, 2017	FN8877.4	Removed Way Overcurrent Protection (WOCP) function from datasheet. Made bit 1 on page 28 to “Not used”.
Sep 7, 2017	FN8877.3	Removed ISL9238A part due to non-applicable changes to this datasheet. Updated Table 2 on page 19 added Revision ID. Updated Table 12 on page 24. Updated About Intersil section.
Nov 9, 2016	FN8877.2	Remove the ISL9238AIRTZ parts from Ordering Information table. Updated POD L32.4x4D. Changes: Added 0.035 Nominal value to standoff height
Sep 7, 2016	FN8877.1	Increased HBM ESD from 1.5kV to 2kV. Updated Applications and 1st paragraph to include more broad applications.
Aug 31, 2016	FN8877.0	Initial Release

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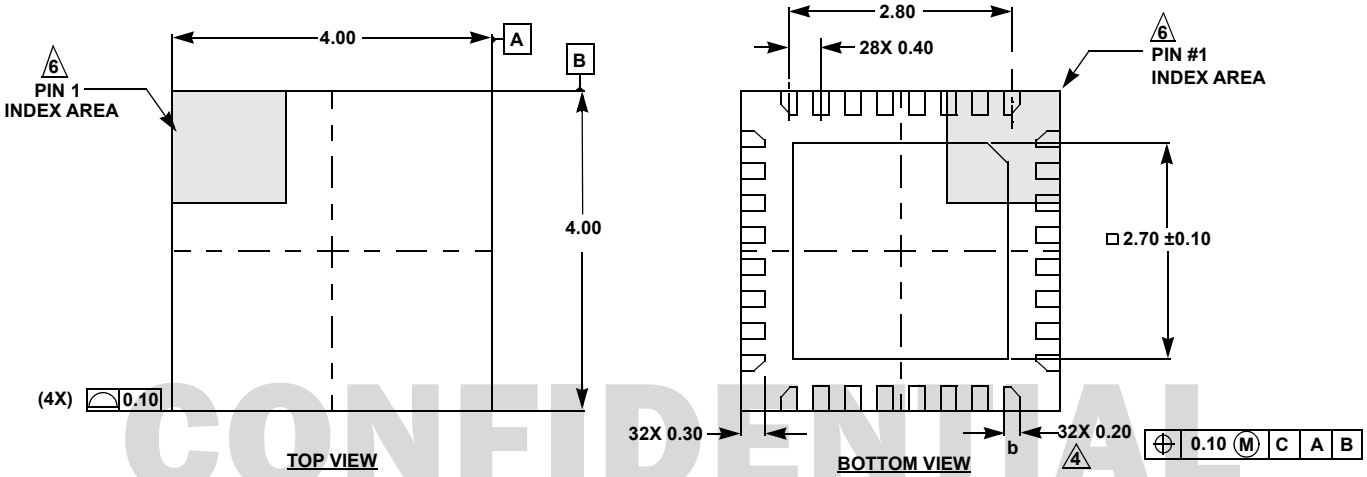
Package Outline Drawing

For the most recent package outline drawing, see L32.4x4D.

L32.4x4D

32 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE

Rev 2, 10/16



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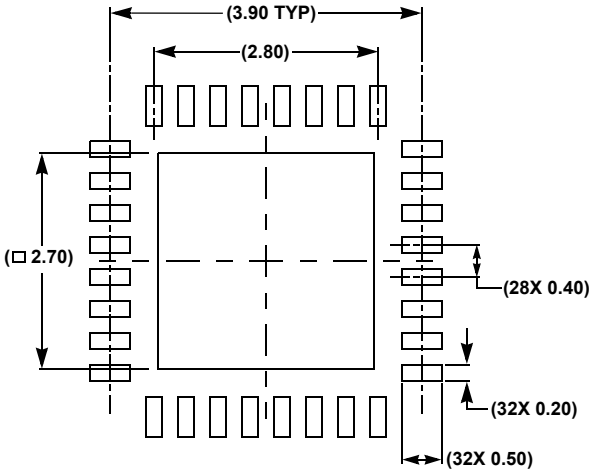
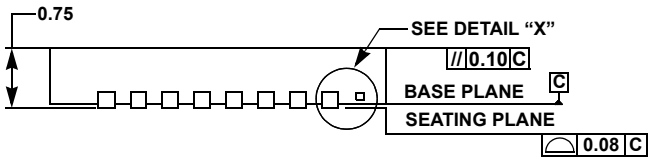
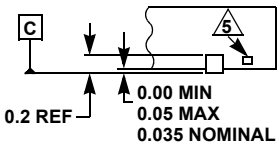


TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ±0.05.
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.25mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

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