ISL81806

80V Dual Synchronous Buck Controller Optimized to Drive E-mode GaN FET

The ISL81806 is a dual synchronous buck controller that generates two independent outputs or one output with two interleaved phases for a wide variety of applications in industrial and general-purpose segments. With wide input and output voltage ranges, the controller is suitable for telecommunication, data center, and computing applications.

The ISL81806 provides a gate driver voltage of 5.3V. With its small dead time setting, it is a perfect controller for the E-mode GaN FET devices.

The ISL81806 uses peak current mode control with phase interleaving for the two outputs. Each output has a voltage regulator, current monitor, and average current regulator to provide independent average voltage and current control. The internal Phase-Locked Loop (PLL) oscillator assures an accurate frequency setting from 100kHz to 2MHz, and the oscillator can be synchronized to an external clock signal for frequency synchronization and phase interleave paralleling applications. This PLL circuit can output a phase-shift-programmable clock signal that is used for multi-phase cascade synchronization with the required interleaving phase shift.

The ISL81806 features programmable soft-start and accurate threshold enable functions along with a power-good indicator to simplify power supply rail sequencing. It also provides full protection features such as OVP, UVP, OTP, and average and a peak current limit on both outputs to ensure high reliability.

The IC is available in a space-conscious 32 Ld 5mmx5mm TQFN package. The package uses an EPAD to improve thermal performance and noise immunity. The full feature design with low pin count makes the ISL81806 an ideal solution for a simple power supply design with a fast time to market.

Features

- Wide input voltage range: 4.5V to 80V
- Wide output voltage range: 0.8V to 76V
- Gate drive voltage: 5.3V
- Four FET drivers
- Dual interleaved outputs or single output with interleaved dual-phase operation
- Programmable frequency: 100kHz to 2MHz
- Constant output voltage and output current feedback loop control
- Light-load efficiency enhancement
  - Low ripple diode emulation and burst mode operation
- Programmable soft-start
- Supports startup into pre-biased rails
- Supports current sharing with cascade phase interleaving
- External clock sync
- Clock out with accurate phase angle controlled by PLL or frequency dithering
- PGOOD indicator
- Output current monitor
- Selectable mode between PWM/DE/Burst
- Accurate EN/UVLO threshold: ±2%
- Low shutdown current: 5µA
- Complete protection: OCP (pulse by pulse and optional hiccup or constant current mode), OVP, OTP, and UVP

Applications

- Telecommunication
- Server and data center
- Automotive electronics
- Industrial equipment
- Power system

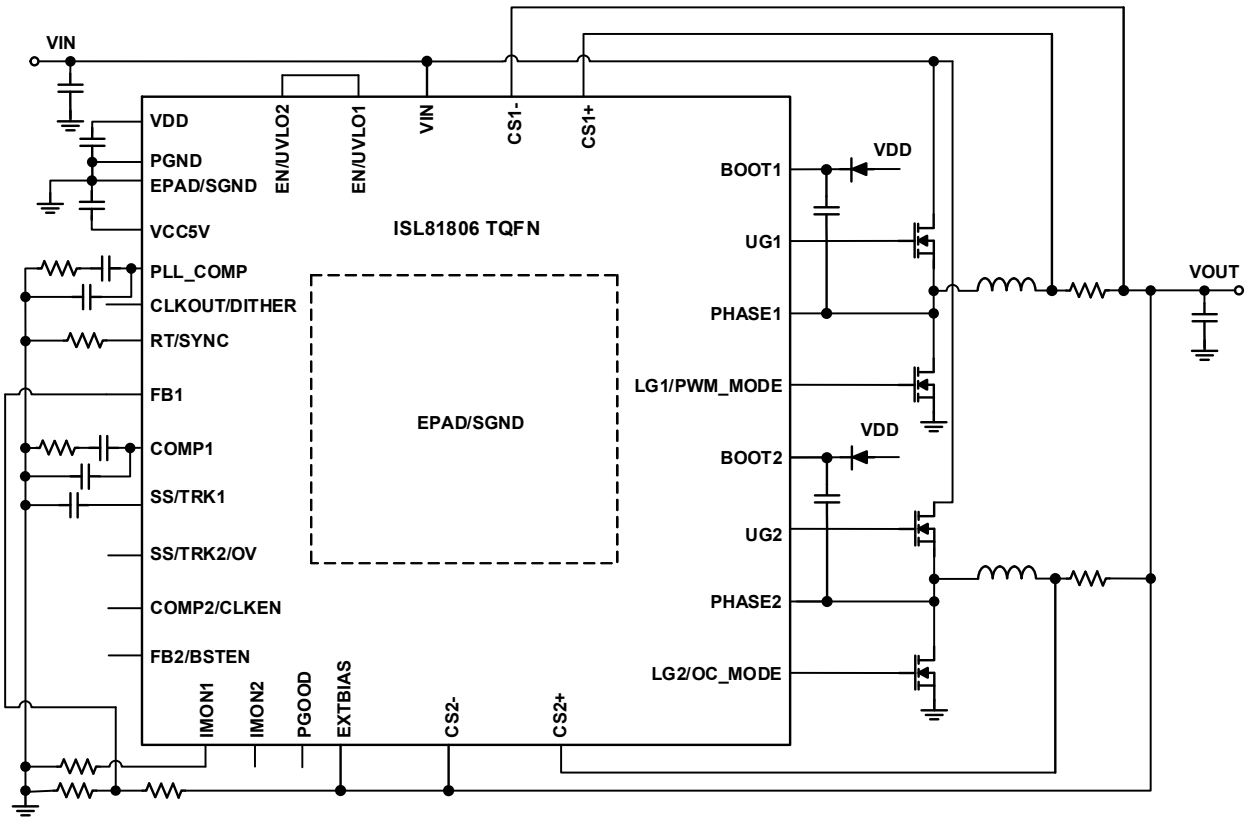


Figure 1. Typical Application Diagram

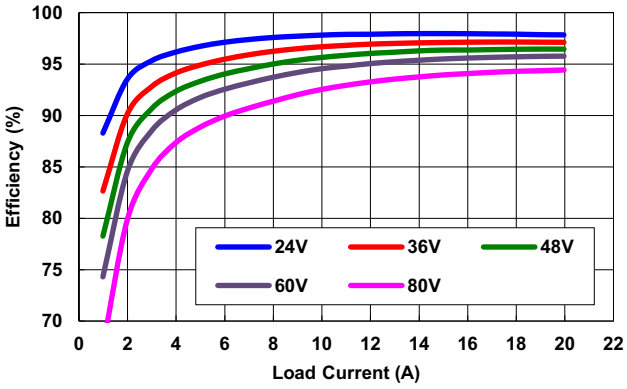


Figure 2. Efficiency (V_{OUT} = 12V, f_{SW} = 500kHz, PWM Mode)

Contents

1. Overview

1.1 Typical Application Schematics

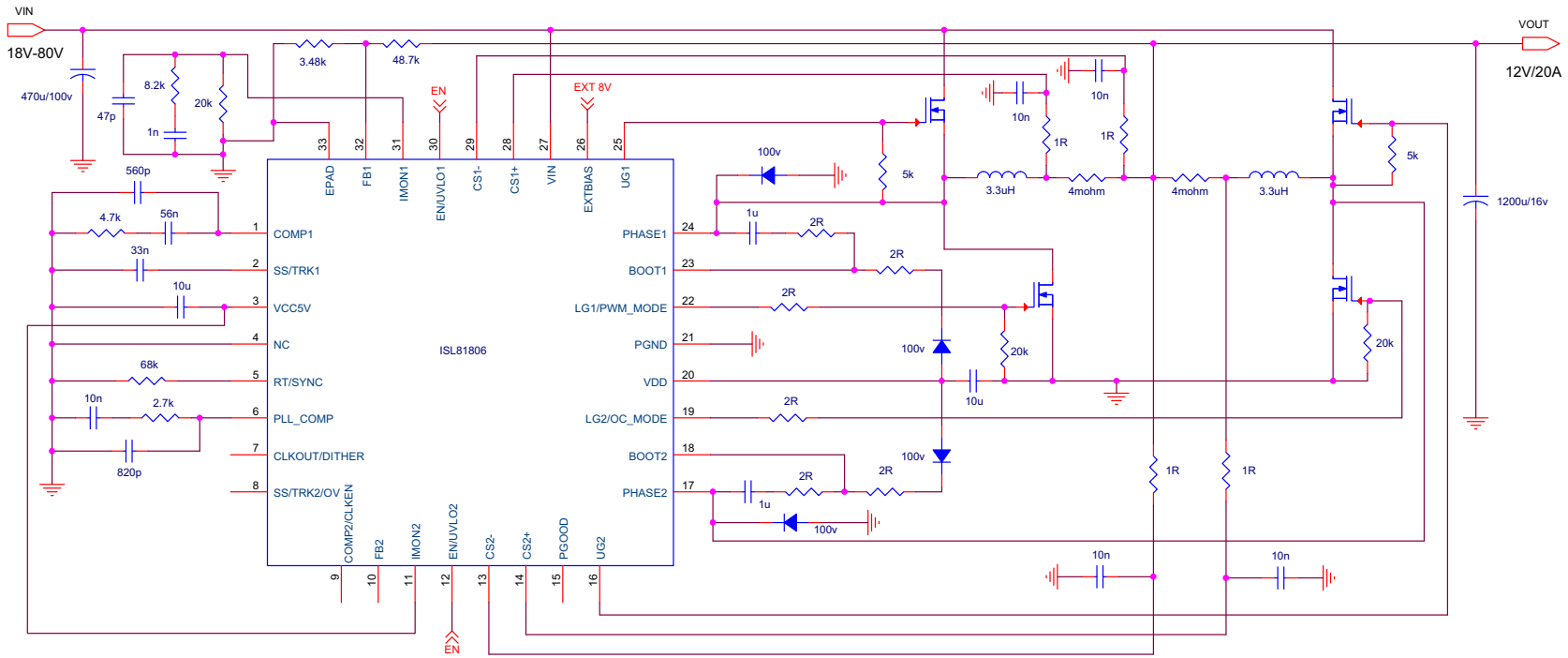


Figure 3. V_{IN} = 18V to 80V, V_{OUT} = 12V, I_{OUT} = 20A Typical Circuit

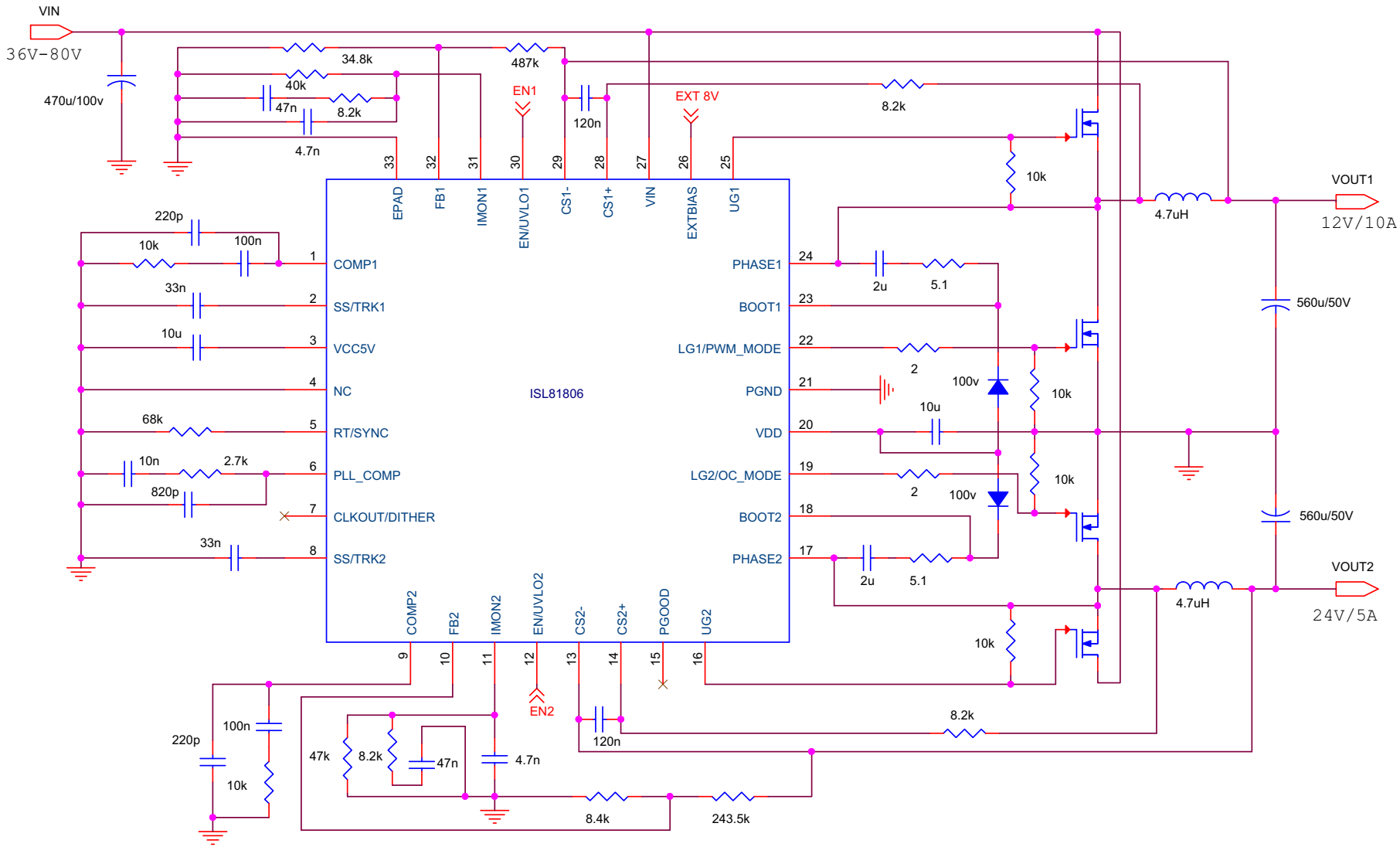


Figure 4. V_{IN} = 36V to 80V, V_{OUT1} = 12V, V_{OUT2} = 24V Typical Circuit

1.2 Block Diagram

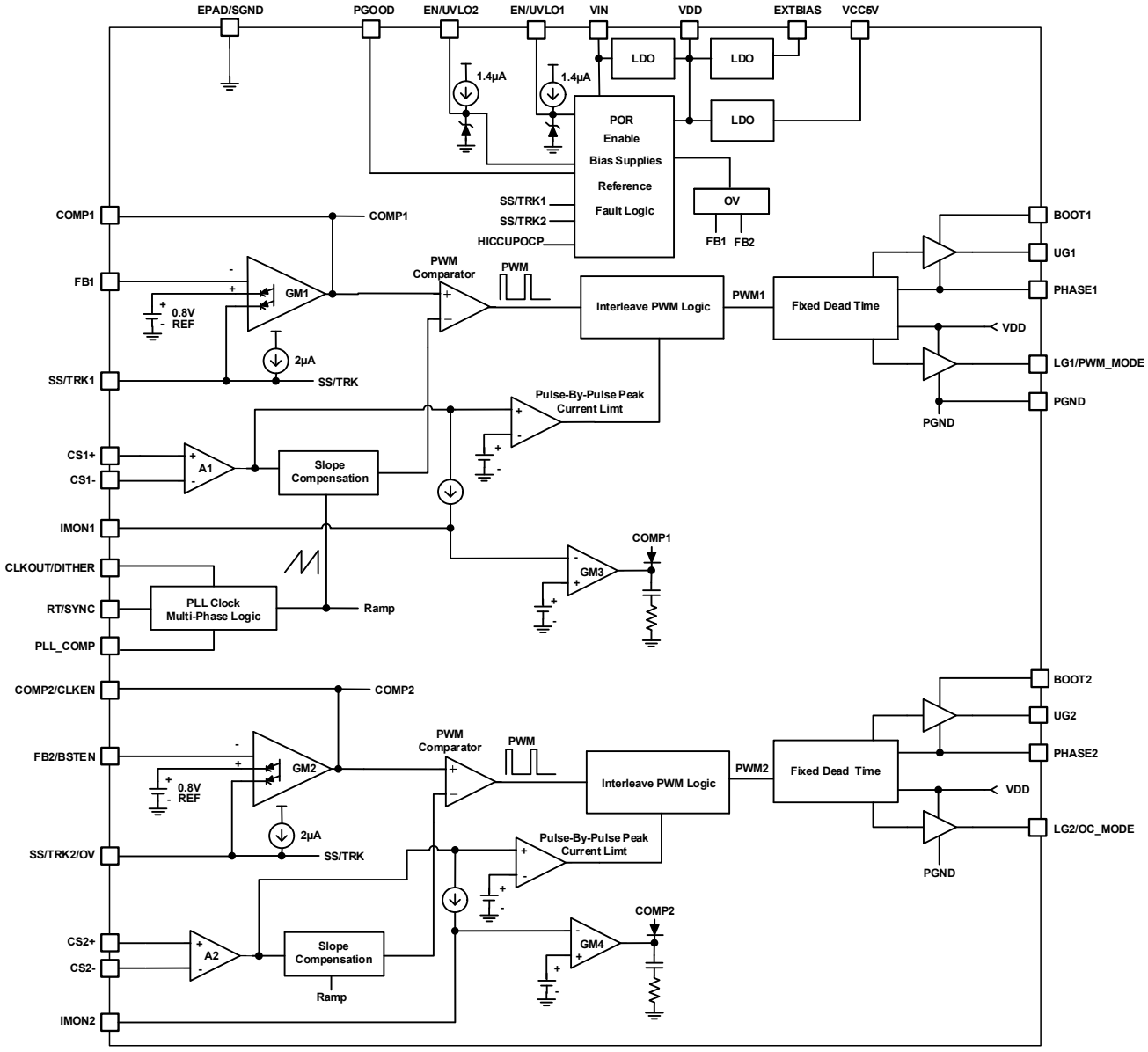
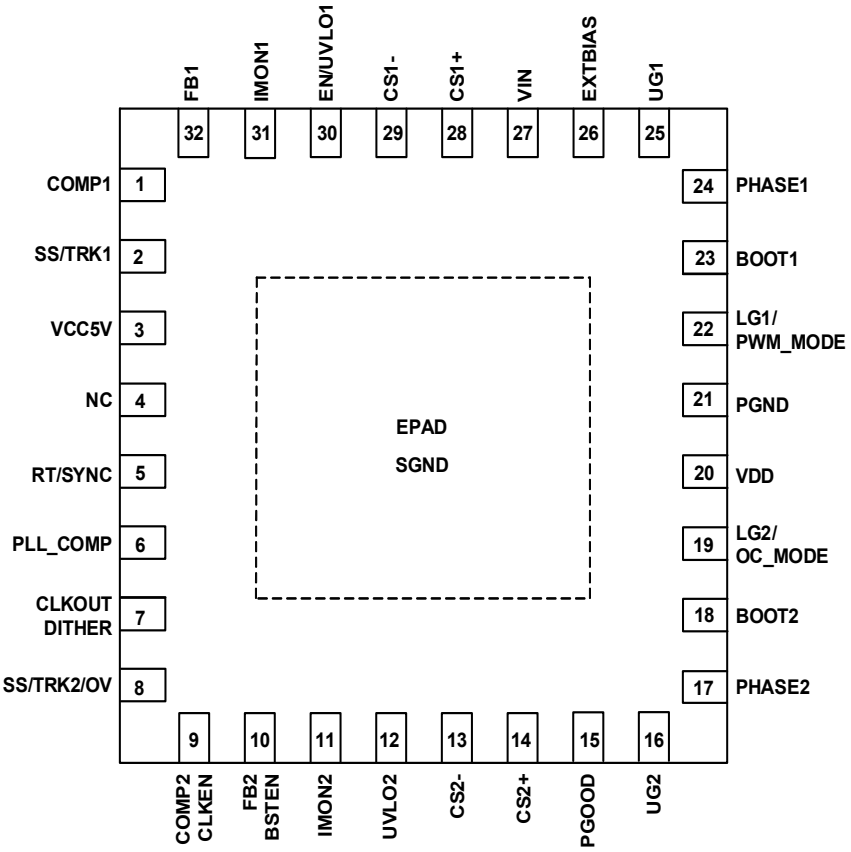


Figure 5. Block Diagram

2. Pin Information

2.1 Pin Assignments



Top View

2.2 Pin Descriptions

Pin #	Pin Name	Function
1	COMP1	Channel 1 voltage error GM amplifier output. It sets the reference of the inner current loop. The feedback compensation network is connected between the COMP1 and SGND pins. When the COMP1 pin is pulled below 1.1V, the PWM duty cycle reduces to 0%. In dual-phase application, COMP2 is disconnected from Pin 9 and internally connected to this pin.
2	SS/TRK1	Channel 1 soft-start or track control pin. When used for soft-start control, a soft-start capacitor is connected from this pin to ground. A regulated 2µA current source charges up the soft-start capacitor. The value of the soft-start capacitor sets the output voltage ramp. When used for tracking control, an external supply rail is configured as the master, and the output voltage of the master supply is applied to this pin using a resistor divider. The output voltage tracks the master supply voltage. In dual-phase applications, SS/TRK2 is disconnected from Pin 8 and internally connected to this pin.
3	VCC5V	The output of the internal 5V linear regulator. This output supplies bias for the IC. The VCC5V pin must always be decoupled to SGND ground with a minimum 4.7µF ceramic capacitor placed close to the pin.
4	NC	No connection

Pin #	Pin Name	Function
5	RT/SYNC	A resistor from this pin to ground adjusts the default switching frequency from 100kHz to 2MHz. The default switching frequency of the PWM controller is determined by the resistor R_T as shown in Equation 1. **(EQ. 1)** $R_T = \left(\frac{34.7}{f_{SW}} - 4.78\right) \cdot k\Omega$ where f_{SW} is the switching frequency in MHz. When this pin is open or tied to VCC5V, f_{SW} is set to 120kHz. When this pin is tied to GND, f_{SW} is set to 575kHz. When an external clock signal is applied to this pin, the internal frequency is synchronized to the external clock frequency.
6	PLL_COMP	Compensation pin for the internal PLL circuit. A compensation network shown in Figure 34 is required. R_{PLL}(2.7kΩ), C_{PLL1} (10nF), and C_{PLL2} (820pF) are recommended.
7	CLKOUT/DITHER	Dual function pin. When there is no capacitor connected to this pin, it provides a clock signal to synchronize the other ISL81806(s). The phase shift of the clock signal is set by the IMON2 and EN/UVLO2 pin voltage. When a capacitor is connected to this pin, the clock out function is disabled and the frequency dither function is enabled before the soft-start. The capacitor is charged by an 8µA and discharged by a 10µA current source. As the voltage on the pin ramps up and down the oscillator frequency is modulated between -15% and +15% of the nominal frequency set by the RT resistor. In the external sync mode, the frequency dither function is disabled.
8	SS/TRK2/OV	Channel 2 soft-start or track control pin. When used for soft-start control, a soft-start capacitor is connected from this pin to ground. A regulated 2µA current source charges up the soft-start capacitor. The value of the soft-start capacitor sets the output voltage ramp. When used for tracking control, an external supply rail is configured as the master, and the output voltage of the master supply is applied to this pin using a resistor divider. The output voltage tracks the master supply voltage. In dual-phase applications, the internal SS/TRK2 signal is disconnected from this pin and internally connected to the SS/TRK1 pin. In this configuration, the OVP trip signal is connected to this pin for multi-phase operation. In multi-chip parallel applications, connect this pin of each chip together to synchronize OVP operation.
9	COMP2/CLKEN	Channel 2 voltage error GM amplifier output. This pin sets the reference of the inner current loop. The feedback compensation network is connected between this and the SGND pins. When the COMP2 pin is pulled below 1.1V, the PWM duty cycle reduces to 0%. In dual-phase applications, the internal COMP2 signal is disconnected from this pin and internally connected to the COMP1 pin. In this configuration, the PFM OFF mode trip signal is connected to this pin for multi-phase operation. In multi-chip parallel applications, connect this pin from each chip together to synchronize the PFM OFF state.
10	FB2/BSTEN	Channel 2 output voltage feedback input pin. Connect FB2 to a resistive voltage divider from the output to SGND to adjust the output voltage. The FB2 pin voltage is regulated to the internal 0.8V reference. In dual-phase applications, the internal FB2 signal is disconnected from this pin and internally connected to the FB1 pin. In this configuration, the burst enable signal is connected to this pin for multi-phase operation. In multi-chip parallel applications, connect this pin of each chip together to synchronize the Burst operation.

Pin #	Pin Name	Function
11	IMON2	Channel 2 output current monitor. The current from this pin is proportional to the differential voltage between the CS2+ and CS2- pins. Connect a resistor and capacitor network between this pin and SGND to make the pin voltage proportional to the average output current. When the pin voltage reaches 1.2V, the internal average current limit loop reduces the output voltage to keep the output current constant when the constant current OCP mode is set or the converter shuts down when hiccup OCP mode is set. In DE Burst mode, when this pin voltage is less than 815mV, the controller runs in Burst mode. When FB2 voltage is lower than 0.78V, the controller exits Burst mode. When a higher resistance on this pin sets its voltage higher than 815mV at no-load condition, the controller runs in DE mode with no burst operation. When the IMON2 pin voltage is higher than 3V, the IC is set for single output dual-phase mode, and the original IMON2 current monitor function pin is disconnected from the IMON2 pin and internally connected to the IMON1 pin. Table 1 shows the CLKOUT phase settings with different EN/UVLO2 pin connections and the IMON2 pin voltage.
12	EN/UVLO2	This pin provides both an enable/disable function for the IC and an accurate UVLO function for Channel 2. The channel output is disabled when the pin is pulled to ground. When the voltage on the pin reaches 1.3V, the VDD and VCC5V LDOs become active. When the voltage on the pin reaches 1.8V, the Channel 2 PWM modulator is enabled. When the pin is floating, it is enabled by default by an internal pull-up. Pulling both EN/UVLO1 and EN/UVLO2 lower than 0.9V disables the internal LDOs to achieve a low standby current. An internal Zener is connected between this pin and ground. The maximum sink current for this Zener is 100µA.
13	CS2-	Channel 2 output current sense signal negative input pin.
14	CS2+	Channel 2 output current sense signal positive input pin.
15	PGOOD	The power-good open-drain logic output that indicates the status of Channel 1 output voltage. This pin is pulled down when Channel 1 output is not within ±11% of the nominal voltage or EN1 pin is pulled LOW.
16	UG2	High-side FET gate driver output controlled by the Channel 2 PWM signal.
17	PHASE2	Phase node connection of Channel 2 buck converter. This pin is connected to the junction of the upper FET source, filter inductor, and the lower FET drain of the converter.
18	BOOT2	Bootstrap pin that provides bias for the Channel 2 high-side driver. The positive terminal of the bootstrap capacitor connects to this pin. Connect a bootstrap diode between this pin and VDD to create the bias for the high-side driver. When the BOOT2 to PHASE2 voltage drops to 3.9V at no switching condition, a minimum on-time pulse is issued to turn on LG2 to refresh the bootstrap capacitor and maintain the high-side driver bias voltage.
19	LG2/ OC_MODE	Low-side FET gate driver output controlled by the Channel 2 PWM signal and OCP mode set pin. The OCP mode is set by a resistor connected from the pin to ground during the initialization period before soft-start. During the initialization period, the pin sources 10µA of current to set the voltage on the pin. If the pin voltage is less than 0.3V, OCP is set to Constant Current mode. If the pin voltage is greater than 0.3V, OCP is set to Hiccup mode.
20	VDD	The output of the internal 5.3V linear regulator supplied by either VIN or EXTBIAS. This output supplies bias for the IC low-side drivers and the boot circuitries for the high-side drivers. The VDD pin must always be decoupled to PGND ground with a minimum 4.7µF ceramic capacitor placed close to the pin.
21	PGND	Power ground connection. This pin should be connected to the sources of the lower FET and the (-) terminals of the external input capacitors.
22	LG1/ PWM_MODE	Low-side FET gate driver output controlled by the Channel 1 PWM signal and PWM mode set pin. The PWM mode is set by a resistor connected from the pin to ground during the initialization period before soft-start. During the initialization period, the pin sources a 10µA of current to set the voltage on the pin. If the pin voltage is less than 0.3V, the converter is set to Forced PWM mode. If the pin voltage is higher than 0.3V, the converter is set to Diode Emulation (DE) Burst mode.

Pin #	Pin Name	Function
23	BOOT1	Bootstrap pin that provides bias for the Channel 1 high-side driver. The positive terminal of the bootstrap capacitor connects to this pin. Connect a bootstrap diode between this pin and VDD to create the bias for the high-side driver. When the BOOT1 to PHASE1 voltage drops to 3.9V at no switching condition, a minimum on-time pulse is issued to turn on LG1 to refresh the bootstrap capacitor and maintain the high-side driver bias voltage.
24	PHASE1	Phase node connection of the Channel 1 buck converter. This pin is connected to the junction of the upper FET source, filter inductor, and lower FET drain of the converter.
25	UG1	High-side FET gate driver output controlled by the Channel 1 PWM signal.
26	EXTBIAS	External bias input for the optional VDD LDO. There is an internal switch to disconnect the VIN LDO when EXTBIAS voltage is higher than 4.8V. Decouple this pin to ground with a 10µF capacitor when it is in use, otherwise tie this pin to ground. DO NOT float this pin.
27	VIN	This pin should be tied to the input rail. It provides power to the internal LDO for VDD. Decouple this pin with a small ceramic capacitor (0.1µF to 1µF) to ground.
28	CS1+	Channel 1 output current sense signal positive input pin.
29	CS1-	Channel 1 output current sense signal negative input pin.
30	EN/ UVLO1	This pin provides both an enable/disable function for the IC and an accurate UVLO function for Channel 1. The channel output is disabled when the pin is pulled to ground. When the voltage on the pin reaches 1.3V, the VDD and VCC5V LDOs become active. When the voltage on the pin reaches 1.8V, the Channel 1 PWM modulator is enabled. When the pin is floating, it is enabled by default by an internal pull-up. Pulling both EN/UVLO1 and EN/UVLO2 lower than 0.9V disables the internal LDOs to achieve a low standby current. An internal Zener is connected between this pin and ground, the maximum sink current for this Zener is 100µA.
31	IMON1	Channel 1 output current monitor. The current from this pin is proportional to the differential voltage between the CS1+ and CS1- pins. Connect a resistor and capacitor network between this pin and SGND to make the pin voltage proportional to the average output current. When the pin voltage reaches 1.2V, the internal average current limit loop reduces the output voltage to keep the output current constant when constant current OCP mode is set or the converter shuts down when the Hiccup OCP mode is set. In DE Burst mode, when this pin voltage is less than 815mV, the controller runs in Burst mode. When FB1 voltage is lower than 0.78V, the controller exits Burst mode. When a higher resistance on this pin sets its voltage higher than 815mV at no-load condition, the controller runs in DE mode with no burst operation. In dual-phase parallel operation mode, the resistor connected between IMON1 and GND should be between 17k and 24k.
32	FB1	Channel 1 output voltage feedback input pin. Connect FB1 to a resistive voltage divider from the output to SGND to adjust the output voltage. The FB1 pin voltage is regulated to the internal 0.8V reference. In dual-phase applications, FB2 is disconnected from Pin 10 and internally connected to this pin.
-	EPAD SGND	EPAD at ground potential. EPAD is connected to SGND internally. However, Renesas recommends soldering it directly to the ground plane for better thermal performance and noise immunity. This is the small-signal ground common to all control circuitry. Renesas recommends routing this pin separately from the high current ground (PGND). Tie SGND and PGND together if there is one solid ground plane with no noisy currents around the chip. All voltage levels are measured with respect to this pin.

3. Specifications

3.1 Absolute Maximum Ratings

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
VCC5V, EN/UVLO1, EN/UVLO2	-0.3	+5.9	V
VDD to GND	-0.3	+9	V
EXTBIAS to GND	-0.3	+40	V
VIN	-0.3	+85	V
CS1+, CS1-, CS2+, CS2- to GND	-0.3	+85	V
BOOT1, 2/UG1, 2 to PHASE1, 2	-0.3	+12	V
PHASE1, 2 to GND	-5 (<20ns)/-0.3 (DC)	+85	V
FB1, FB2, SS/TRK1, SS/TRK2, COMP1, COMP2, RT/SYNC, PLL_COMP, CLKOUT/DITHER, BSTEN, CLKEN, OV, PGOOD, IMON1, IMON2 to GND	-0.3	VCC5V + 0.3	V
LG1/PWM_MODE, LG2/OC_MODE to GND	-0.3	V_{DD} + 0.3	V
CS1+ to CS1- and CS2+ to CS2-	-0.3	+0.3	V
VCC5V, VDD Short-Circuit to GND Duration	1		s
ESD Ratings	**Value**		**Unit**
Human Body Model (Tested per JS-001-2017)	2		kV
Charge Device Model (Tested per JS-002-2018)	1		kV
Latch-Up (Tested per JESD78E; Class II, Level A, +125°C (T_J))	100		mA

3.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)[1]	θ_{JC} (°C/W)[2]
32 Ld TQFN Package	29	1

1. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
2. For θ_{JC}, the case temperature location is the center of the exposed metal pad on the package underside.

Parameter	Minimum	Maximum	Unit
Junction Temperature	-55	+150	°C
Operating Temperature	-40	+125	°C
Storage Temperature Range	-65	+150	°C
Pb-Free Reflow Profile	see TB493		

3.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Temperature	-40	+125	°C
VIN to GND	4.5	80	V
VCC5V, EN/UVLO1, EN/UVLO2 to GND	0	5.4	V
VDD to GND	0	5.6	V
EXTBIAS to GND	0	36	V

3.4 Electrical Specifications

Recommended operating conditions unless otherwise noted. See the Block Diagram and Overview. V_{IN} = 4.5V to 80V, or V_{DD} = 5.3V ±10%, C_VCC5V = 4.7µF, T_A = -40°C to +125°C, Typical values are at T_A = +25°C, unless otherwise specified.
Boldface limits apply across the operating temperature range, -40°C to +125°C.

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
V_{IN} Supply						
Input Voltage Range	V_{IN}		**4.5**		**80.0**	V
V_{IN} Supply Current						
Shutdown Current[2]	I_{VINQ}	EN1 = EN2 = 0V, PGOOD is floating		5.5	**10.0**	µA
Operating Current[3]	I_{VINOP}	PGOOD is floating		5.5	**7.0**	mA
		PGOOD is floating, EXTBIAS=12V		50		µA
VCC5V Supply						
Internal LDO Output Voltage	V_{CC5V}	V_{IN} = 8V, I_L = 0mA	**4.7**	5.1	**5.4**	V
		V_{IN} = 80V, I_L = 0mA	**4.7**	5.1	**5.4**	V
		V_{IN} = 4.5V, I_L = 5mA	**3.85**	4.4		V
		V_{IN} > 5.6V, I_L = 10mA	**4.65**	5.1		V
Maximum Supply Current of Internal LDO	I_{VCC_MAX}	V_{VCC5V} = 0V, V_{IN} = 8V		120		mA
V_{DD} Supply						
Internal LDO Output Voltage	V_{DD}	V_{IN} = 12V, EXTBIAS = 0V, I_L = 0mA	**5.0**	5.35	**5.6**	V
		V_{IN} = 80V, EXTBIAS = 0V, I_L = 0mA	**5.0**	5.35	**5.6**	V
		V_{IN} = 4.5V, EXTBIAS = 12V, I_L = 0mA	**5.0**	5.35	**5.6**	V
		V_{IN} = 80V, EXTBIAS = 12V, I_L = 0mA	**5.0**	5.35	**5.6**	V
		V_{IN} = 4.5V, EXTBIAS = 0V, I_L = 30mA	**3.9**	4.3		V
		V_{IN} = 4.5V, EXTBIAS = 7.8V, I_L = 30mA	**4.8**	5.25		V
		V_{IN} > 8.6V, EXTBIAS = 0V, I_L = 75mA	**4.8**	5.25		V
		V_{IN} = 4.5V, EXTBIAS > 9.0V, I_L = 75mA	**4.8**	5.2		V
Maximum Supply Current of Internal LDO	I_{VDD_MAX}	V_{VDD} = 0V, EXTBIAS = 0V, V_{IN} = 12V		120		mA
		V_{VDD} = 4.5V, EXTBIAS = 12V, V_{IN} = 4.5V		140		mA

Recommended operating conditions unless otherwise noted. See the Block Diagram and Overview. V_{IN} = 4.5V to 80V, or V_{DD} = 5.3V ±10%, C_VCC5V = 4.7µF, T_A = -40°C to +125°C, Typical values are at T_A = +25°C, unless otherwise specified.
Boldface limits apply across the operating temperature range, -40°C to +125°C. (Cont.)

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
EXTBIAS Supply						
Switch Over Threshold Voltage, Rising	V_{EXT_THR}	EXTBIAS voltage	**4.5**	4.8	**5.1**	V
Switch Over Threshold Voltage, Falling	V_{EXT_THF}	EXTBIAS voltage	**4.25**	4.45	**4.7**	V
V_{IN} UVLO						
V_{IN} Rising UVLO Threshold	$V_{UVLOTHR}$	V_{IN} voltage, 0mA on VCC5V and VDD		3.5		V
V_{IN} Falling UVLO Threshold	$V_{UVLOTHF}$	V_{IN} voltage, 0mA on VCC5V and VDD		3.3		V
VCC5V Power-On Reset						
VCC5V Rising POR Threshold	V_{PORTHR}	VCC5V voltage, 0mA on VCC5V and VDD	**3.7**	4.0	**4.3**	V
VCC5V Falling POR Threshold	V_{PORTHF}	VCC5V voltage, 0mA on VCC5V and VDD	**3.30**	3.55	**3.75**	V
EN/UVLO Threshold						
EN1 Rise Threshold	V_{EN1SS_THR}	V_{IN} > 5.6V	**0.75**	1.05	**1.30**	V
EN1 Fall Threshold	V_{EN1SS_THF}	V_{IN} > 5.6V	**0.60**	0.90	**1.10**	V
EN1 Hysteresis	V_{EN1SS_HYST}	V_{IN} > 5.6V	**70**	150	**300**	mV
UVLO1 Rise Threshold	V_{UVLO1_THR}	V_{IN} > 5.6V	**1.77**	1.80	**1.83**	V
UVLO1 Hysteresis Current	I_{UVLO1_HYST}	V_{IN} = 12V, EN/UVLO = 1.815V	**2.5**	4.4	**6.0**	µA
EN2 Rise Threshold	V_{EN2SS_THR}	V_{IN} > 5.6V	**0.75**	1.05	**1.30**	V
EN2 Fall Threshold	V_{EN2SS_THF}	V_{IN} > 5.6V	**0.60**	0.90	**1.10**	V
EN2 Hysteresis	V_{EN2SS_HYST}	V_{IN} > 5.6V	**70**	150	**300**	mV
UVLO2 Rise Threshold	V_{UVLO2_THR}	V_{IN} > 5.6V	**1.77**	1.80	**1.83**	V
UVLO2 Hysteresis Current	I_{UVLO2_HYST}	V_{IN} = 12V, EN/UVLO = 1.815V	**2.5**	4.4	**6.0**	µA
Soft-Start Current						
SS/TRK1 Soft-Start Charge Current	I_{SS1}	SS/TRK1 = 0V		2.00		µA
SS/TRK2 Soft-Start Charge Current	I_{SS2}	SS/TRK2 = 0V		2.00		µA
Default Internal Minimum Soft-Starting						
Default Internal Output Ramping Time1	t_{SS1_MIN}	SS/TRK1 open		1.7		ms
Default Internal Output Ramping Time2	t_{SS2_MIN}	SS/TRK2 open		1.7		ms
Power-Good Monitors						
PGOOD Upper Threshold	V_{PGOV}		**107**	109	**112**	%
PGOOD Lower Threshold	V_{PGUV}		**87**	90	**92**	%
PGOOD Low Level Voltage	V_{PGLOW}	I_SINK = 2mA			**0.35**	V
PGOOD Leakage Current	I_{PGLKG}	PGOOD = 5V		0	**150**	nA

Recommended operating conditions unless otherwise noted. See the Block Diagram and Overview. V_{IN} = 4.5V to 80V, or V_{DD} = 5.3V ±10%, C_VCC5V = 4.7µF, T_A = -40°C to +125°C, Typical values are at T_A = +25°C, unless otherwise specified.
Boldface limits apply across the operating temperature range, -40°C to +125°C. (Cont.)

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
PGOOD Timing						
V_{OUT} Rising Threshold to PGOOD Rising[4]	t_{PGR}			1.1	**5**	ms
V_{OUT} Falling Threshold to PGOOD Falling	t_{PGF}			80		µs
Reference Section						
Internal Voltage Loop Reference Voltage	V_{REFV}			0.800		V
Reference Voltage Accuracy		T_A = 0°C to +85°C	-0.75		+0.75	%
		T_A = -40°C to +125°C	**-1.00**		**+1.00**	%
Internal Current Loop Reference Voltage	V_{REFI}			1.200		V
Reference Voltage Accuracy		T_A = 0°C to +85°C	-0.75		+0.75	%
		T_A = -40°C to +125°C	**-1.00**		**+1.00**	%
PWM Controller Error Amplifiers						
FB_1 Pin Bias Current	$I_{FBOUTLKG1}$		**-50**	0	**+50**	nA
FB_1 Error Amp GM	Gm1			1.75		mS
FB_1 Error Amp Voltage Gain	AV1			82		dB
FB_1 Error Amp Gain-BW Product	GBW1			8		MHz
FB_1 Error Amp Output Current Capability				300		µA
FB_2 Pin Bias Current	$I_{FBOUTLKG2}$		**-50**	0	**+50**	nA
FB_2 Error Amp GM	Gm2			1.75		mS
FB_2 Error Amp Voltage Gain	AV2			82		dB
FB_2 Error Amp Gain-BW Product	GBW2			8		MHz
FB_2 Error Amp Output Current Capability				300		µA
COMP1 Max High Voltage	V_{COMP1_HIGH}	FB1 = 0V		4.7		V
COMP1 Min Low Voltage	V_{COMP1_LOW}	FB1 = 1V		0.01		V
COMP2 Max High Voltage	V_{COMP2_HIGH}	FB2 = 0V		4.7		V
COMP2 Min Low Voltage	V_{COMP2_LOW}	FB2 = 1V		0.01		V
PWM Regulator						
PWM1 Minimum Off-Time	t_{OFF_MIN1}			160		ns
PWM1 Minimum On-Time	t_{ON_MIN1}			120		ns
PWM2 Minimum Off-Time	t_{OFF_MIN2}			160		ns
PWM2 Minimum On-Time	t_{ON_MIN2}			120		ns
PWM1 Peak-to-Peak Sawtooth Amplitude	DV_{RAMP1}	V_{IN} = V_{OUT1} = 12V, f_{SW} = 300kHz		1		V

Recommended operating conditions unless otherwise noted. See the Block Diagram and Overview. V_{IN} = 4.5V to 80V, or V_{DD} = 5.3V ±10%, C_VCC5V = 4.7µF, T_A = -40°C to +125°C, Typical values are at T_A = +25°C, unless otherwise specified.
Boldface limits apply across the operating temperature range, -40°C to +125°C. (Cont.)

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
PWM2 Peak-to-Peak Sawtooth Amplitude	DV_{RAMP2}	V_{IN} = V_{OUT2} = 12V, f_{SW} = 300kHz		1		V
PWM1 Ramp Offset	$V_{ROFFSET1}$		**0.9**	1.1	**1.25**	V
PWM2 Ramp Offset	$V_{ROFFSET2}$		**0.9**	1.1	**1.25**	V
Current Sense, Current Monitors, and Average Current Loop						
Current Sense1 Differential Voltage Range	V_{CS1+} - V_{CS1-}		**-80**		**+150**	mV
Current Sense1 Common-Mode Voltage Range	$CMIR_{CS1}$		**0**		**80**	V
CS1+ Bias Current		CS1+ = CS1- = 12V			**3**	µA
CS1- Bias Current		CS1+ = CS1- = 12V			**400**	µA
IMON1 Offset Current	$I_{CS1OFFSET}$	CS1+ = CS1- = 12V	**17.0**	19.5	**21.5**	µA
Current Sense1 Voltage to IMON1 Current Source Gain	Gm_{CS1}	12V common-mode voltage applied to CS1± pins, 0 to 40mV differential voltage	**165**	200	**235**	µS
IMON1 Error Amp GM	Gm3			12		µS
IMON1 Error Amp Voltage Gain	AV3			72		dB
IMON1 Active Range[5]	V_{IMON1_ACT}	VCC5V = 5V	**0**		**4.3**	V
IMON1 Logic High Threshold[5]	V_{IMON1_H}	VCC5V = 5V			**4.7**	V
IMON1 Error Amp Gain-BW Product	GBW3			5		MHz
Current Sense2 Differential Voltage Range	V_{CS2+} - V_{CS2-}		**-80**		**+150**	mV
Current Sense2 Common-Mode Voltage Range	$CMIR_{CS2}$		**0**		**80**	V
CS2+ Bias Current		CS2+ = CS2- = 12V			**3**	µA
CS2- Bias Current		CS2+ = CS2- = 12V			**400**	µA
IMON2 Offset Current	$I_{CS2OFFSET}$	CS2+ = CS2- = 12V	**17.0**	19	**21**	µA
IMON2 Current		CS2+ = 12V. CS2- = 11.96V	**25**	27.5	**28.5**	µA
Current Sense2 Voltage to IMON2 Current Source Gain	Gm_{CS2}	12V common-mode voltage applied to CS2± pins, 0mV to 40mV differential voltage	**165**	205	**235**	µS
IMON2 Error Amp GM	Gm4			12		µS
IMON2 Error Amp Voltage Gain	AV4			72		dB
IMON2 Error Amp Gain-BW Product	GBW4			5		MHz

Recommended operating conditions unless otherwise noted. See the Block Diagram and Overview. V_{IN} = 4.5V to 80V, or V_{DD} = 5.3V ±10%, C_VCC5V = 4.7µF, T_A = -40°C to +125°C, Typical values are at T_A = +25°C, unless otherwise specified.
Boldface limits apply across the operating temperature range, -40°C to +125°C. (Cont.)

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Switching Frequency and Synchronization						
Switching Frequency	f_{SW}	R_T = 144kΩ	**220**	245	**265**	kHz
		R_T = 72kΩ	**420**	450	**485**	kHz
		R_T Open or to VCC5V	**90**	120	**145**	kHz
		R_T = 0V	**470**	575	**650**	kHz
RT Voltage	V_{RT}	R_T = 72kΩ		560		mV
SYNC Synchronization Range	f_{SYNC}		**140**		**2000**	kHz
SYNC Input Logic High	V_{SYNCH}		**3.2**			V
SYNC Input Logic Low	V_{SYNCL}				**0.5**	V
Clock Output and Frequency Dither						
CLKOUT Output High	V_{CLKH}	I_{SOURCE} = 1mA, VCC5V = 5V	**4.55**			V
CLKOUT Output Low	V_{CLKL}	I_{SINK} = 1mA			**0.3**	V
CLKOUT Frequency	f_{CLK}	R_T = 72kΩ	**420**	450	**485**	kHz
Dither Mode Setting Current Source	$I_{DITHER\_MODE\_SO}$			12		µA
Dither Mode Setting Threshold Low	$V_{DITHER\_MODE\_L}$		**0.26**			V
Dither Mode Setting Threshold High	$V_{DITHER\_MODE\_H}$				**0.34**	V
Dither Source Current	$I_{DITHERSO}$			8		µA
Dither Sink Current	$I_{DITHERSI}$			10		µA
Dither High Threshold Voltage	$V_{DITHERH}$			2.2		V
Dither Low Threshold Voltage	$V_{DITHERL}$			1.05		V
Diode Emulation Mode Detection						
LG1/PWM_MODE Current Source	$I_{MODELG1}$		**7.5**	10	**13.0**	µA
LG1/PWM_MODE Threshold Low	$V_{MODETHL}$		**0.26**			V
LG1/PWM_MODE Threshold High	$V_{MODETHH}$				**0.34**	V
PWM1 Diode Emulation Phase Threshold[6]	V_{CROSS1}	V_{IN} = 12V		0		mV
PWM2 Diode Emulation Phase Threshold[7]	V_{CROSS2}	V_{IN} = 12V		0		mV
Diode Emulation Burst Mode						
PWM1 Burst Mode Enter Threshold	$V_{IMON1BSTEN}$	IMON1 pin voltage	**0.78**	0.815	**0.845**	V
PWM1 Burst Mode Peak Current Limit Input Shunt Set Point	$V_{BST-CS1}$	V_{CS1+} - V_{CS1-}, 12V common-mode voltage applied to CS1± pins		27		mV
PWM1 Burst Mode Peak FB1 Voltage Limit Set Point	$V_{BST-VFB1-UTH}$			0.81		V
PWM1 Burst Mode Exit FB1 Voltage Set Point	$V_{BST-VFB1-LTH}$			0.78		V

Recommended operating conditions unless otherwise noted. See the Block Diagram and Overview. V_{IN} = 4.5V to 80V, or V_{DD} = 5.3V ±10%, C_VCC5V = 4.7µF, T_A = -40°C to +125°C, Typical values are at T_A = +25°C, unless otherwise specified.
Boldface limits apply across the operating temperature range, -40°C to +125°C. (Cont.)

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
PWM2 Burst Mode Enter Threshold	$V_{IMON2BSTEN}$	IMON2 pin voltage	**0.78**	0.815	**0.845**	V
PWM2 Burst Mode Peak Current Limit Input Shunt Set Point	$V_{BST-CS2}$	V_{CS2+} - V_{CS2-}, 12V common-mode voltage applied to CS2± pins		27		mV
PWM2 Burst Mode Peak FB1 Voltage Limit Set Point	$V_{BST-VFB2-UTH}$			0.81		V
PWM2 Burst Mode Exit FB1 Voltage Set Point	$V_{BST-VFB2-LTH}$			0.78		V
BSTEN Output Logic High	$V_{BSTEN-OH}$	No load, VCC5V = 5V		4.9		V
BSTEN Output Logic Low	$V_{BSTEN-OL}$	Pull-up resistance 100kΩ		0.1		V
BSTEN Input Logic High[5]	$V_{BSTEN-IH}$		**3.2**			V
BSTEN Input Logic Low[5]	$V_{BSTEN-IL}$				**1**	V
CLKEN Output Logic High	$V_{CLKEN-OH}$	No load, VCC5V = 5V		4.9		V
CLKEN Output Logic Low	$V_{CLKEN-OL}$	Pull-up resistance 100kΩ		0.1		V
CLKEN Input Logic High[5]	$V_{CLKEN-IH}$		**3.2**			V
CLKEN Input Logic Low[5]	$V_{CLKEN-IL}$				**1**	V
PWM Gate Drivers						
Driver 1, 2 BOOT Refresh Trip Voltage	$V_{BOOTRF1,2}$	BOOT voltage - PHASE voltage	**3.4**	3.9	**4.5**	V
Driver 1, 2 Source and Upper Sink Current	$I_{GSRC1,2}$			1100		mA
Driver 1, 2 Lower Sink Current	$I_{GSNK1,2}$			1400		mA
Driver 1, 2 Upper Drive Pull-Up	$R_{UG\_UP1,2}$			2		Ω
Driver 1, 2 Upper Drive Pull-Down	$R_{UG\_DN1,2}$			1.8		Ω
Driver 1, 2 Lower Drive Pull-Up	$R_{LG\_UP1,2}$			3		Ω
Driver 1, 2 Lower Drive Pull-Down	R_{LG_DN}			2		Ω
Driver 1, 2 Upper Drive Rise Time	t_{GR_UP}	C_{OUT} = 1000pF		15		ns
Driver 1, 2 Upper Drive Fall Time	t_{GF_UP}	C_{OUT} = 1000pF		15		ns
Driver 1, 2 Lower Drive Rise Time	t_{GR_DN}	C_{OUT} = 1000pF		13		ns
Driver 1, 2 Lower Drive Fall Time	t_{GF_DN}	C_{OUT} = 1000pF		13		ns
Driver 1, 2 Dead Time	t_{D_LU}	C_{OUT} = 1000pF, LG falling edge 1V to UG rising edge 1V		15		ns
Driver1, 2 Dead Time	t_{D_UL}	C_{OUT} = 1000pF, UG falling edge 1V to LG rising edge 1V		20		ns
Overvoltage Protection						
Output OVP Threshold	V_{OVTH_OUT}		**112**	114	**116**	%
OV Pin Output Logic High	V_{OV-OH}	Load resistance 100k, VCC5V = 5V		4.9		V
OV Pin Output Logic Low	V_{OV-OL}	No load		0.1		V
OV Pin Input Logic High[5]	V_{OV-IH}		**3.2**			V
OV Pin Input Logic Low[5]	V_{OV-IL}				**1**	V

Recommended operating conditions unless otherwise noted. See the Block Diagram and Overview. V_{IN} = 4.5V to 80V, or V_{DD} = 5.3V ±10%, C_VCC5V = 4.7µF, T_A = -40°C to +125°C, Typical values are at T_A = +25°C, unless otherwise specified.
Boldface limits apply across the operating temperature range, -40°C to +125°C. (Cont.)

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Overcurrent Protection						
LG2/OC_MODE Current Source	$I_{MODELG2}$		**7.5**	10.5	**13.0**	µA
LG2/OC_MODE Threshold Low	$V_{MODETHLOC}$		**0.26**			V
LG2/OC_MODE Threshold High	$V_{MODETHHOC}$				**0.34**	V
Pulse-by-Pulse Peak Current Limit Input Shunt Set Point1	$V_{OCSET-CS1}$	V_{CS1+} - V_{CS1-}, 12V common-mode voltage applied to CS1± pins	**68**	82	**96**	mV
Hiccup Peak Current Limit Input Shunt Set Point1	$V_{OCSET-CS1-HIC}$	V_{CS1+} - V_{CS1-}		98		mV
Pulse-by-Pulse Negative Peak Current Limit Output Shunt Set Point1	$V_{OCSET-CS1}$	V_{CS1+} - V_{CS1-}, 12V common-mode voltage applied to CS1± pins		-60		mV
Output Constant and Hiccup Current Limit Set Point1	$V_{IMON1CC}$	IMON1 Pin Voltage	**1.18**	1.2	**1.22**	V
Output Constant and Hiccup Current Limit Set Point at CS1± Input	V_{AVOCP_CS1}	V_{CS1+} - V_{CS1-}, 12V common-mode applied to CS1± pins, R_{IMON1} = 40.2k, T_J = -40°C to +125°C	**44**	51	**63**	mV
		V_{CS1+} - V_{CS1-}, 12V common-mode applied to CS1± pins, R_{IMON1} = 40.2k, T_J = -40°C to +85°C	**44**	51	**60**	mV
Pulse-by-Pulse Peak Current Limit Input Shunt Set Point2	$V_{OCSET-CS2}$	V_{CS2+} - V_{CS2-}, 12V common-mode voltage applied to CS2± pins	**68**	82	**96**	mV
Hiccup Peak Current Limit Input Shunt Set Point2	$V_{OCSET-CS2-HIC}$	V_{CS2+} - V_{CS2-}		98		mV
Pulse-by-Pulse Negative Peak Current Limit Output Shunt Set Point2	$V_{OCSET-CS2}$	V_{CS2+} - V_{CS2-}, 12V common-mode voltage applied to CS2± pins		-60		mV
Output Constant and Hiccup Current Limit Set Point2	$V_{IMON2CC}$	IMON2 pin voltage	**1.18**	1.2	**1.22**	V
Output Constant and Hiccup Current Limit Set Point at CS2± Input	V_{AVOCP_CS2}	V_{CS2+} - V_{CS2-}, 12V common-mode applied to CS2± pins, R_{IMON2} = 40.2k, T_J = -40°C to +125°C	**44**	51	**63**	mV
		V_{CS2+} - V_{CS2-}, 12V common-mode applied to CS2± pins, R_{IMON2} = 40.2k, T_J = -40°C to +85°C	44	51	60	mV
Hiccup OCP Off-Time	t_{HICC_OFF}			55		ms
Over-Temperature						
Over-Temperature Shutdown	T_{OT-TH}			160		°C
Over-Temperature Hysteresis	T_{OT-HYS}			15		°C

1. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
2. This is the total shutdown current with V_{IN} = 5.6V and 80V.
3. Operating current is the supply current consumed when the device is active but not switching. It does not include gate drive current.
4. When soft-start time is less than 4.5ms, t_{PGR} increases. With internal soft-start (the fastest soft-start time), t^{PGR} increases close to its max limit 5ms.

5. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.
6. Threshold voltage at the PHASE1 pin for turning off the buck bottom FET during DE mode.
7. Threshold voltage at the PHASE2 pin for turning off the buck bottom FET during DE mode.

4. Typical Performance Graphs

Oscilloscope plots are taken using the ISL81806EVAL1Z evaluation board

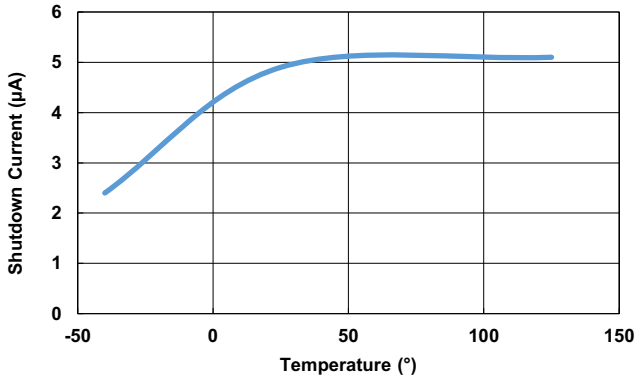


Figure 6. Shutdown Current vs Temperature

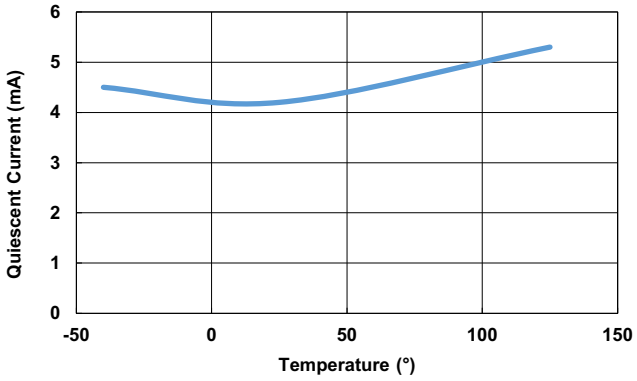


Figure 7. Quiescent Current vs Temperature

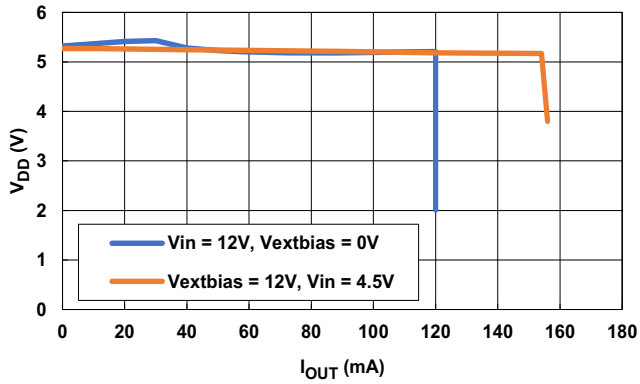


Figure 8. V_{DD} Load Regulation at 12V Input

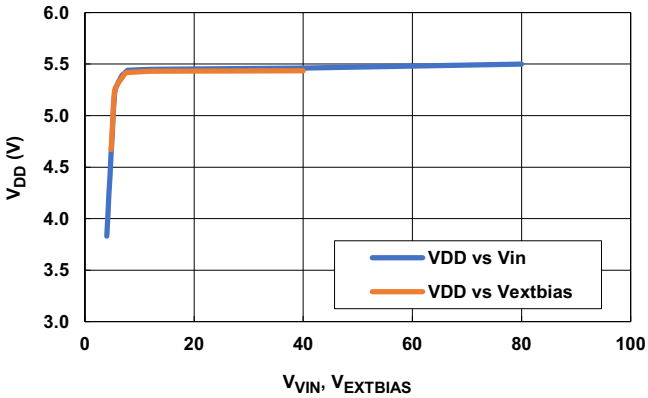


Figure 9. V_{DD} Line Regulation at 20mA Load

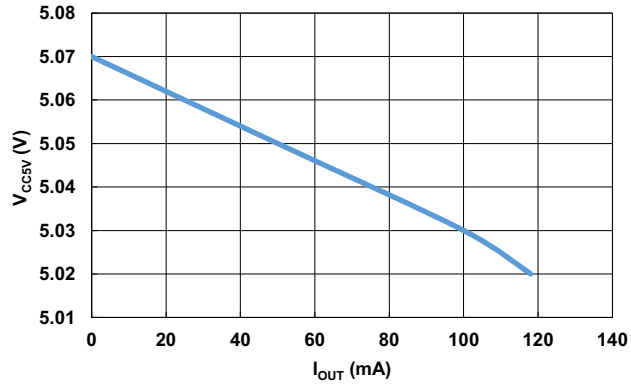


Figure 10. V_{CC5V} Load Regulation at $12V_{IN}$

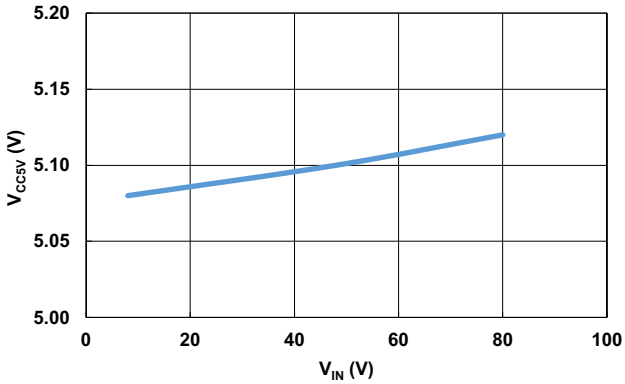


Figure 11. V_{CC5V} Line Regulation at 20mA Load

Oscilloscope plots are taken using the ISL81806EVAL1Z evaluation board (Cont.)

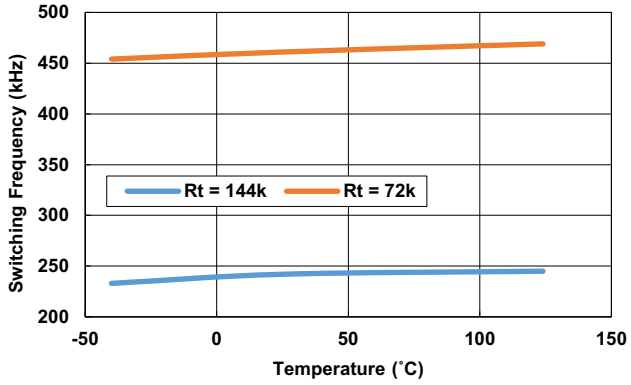


Figure 12. Switching Frequency vs Temperature

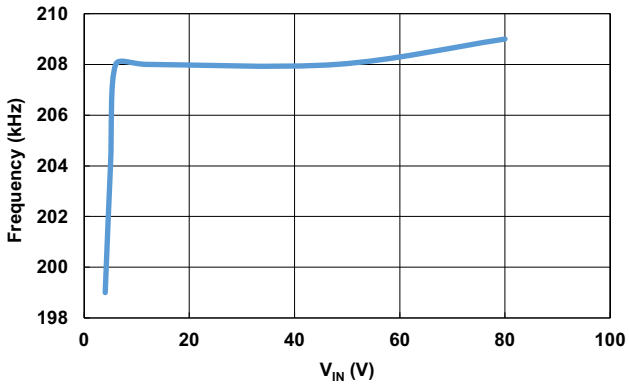


Figure 13. Switching Frequency vs V_{IN}, R_T = 169k

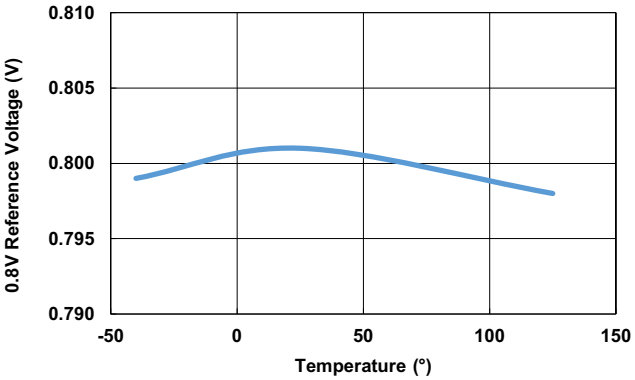


Figure 14. 0.8V Reference Voltage vs Temperature

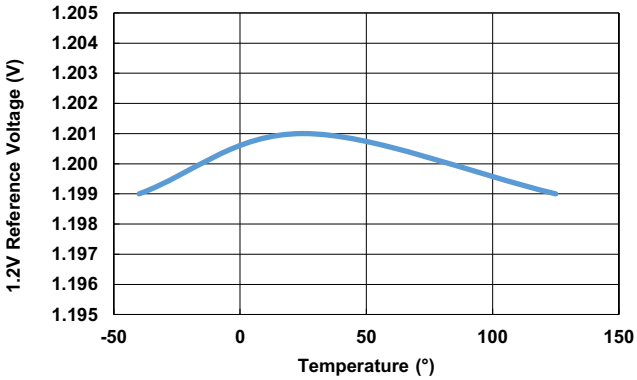


Figure 15. 1.2V Reference Voltage vs Temperature

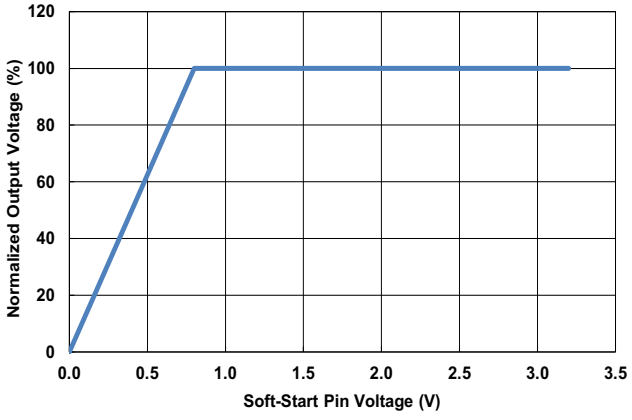


Figure 16. Normalized Output Voltage vs Voltage on Soft-Start Pin

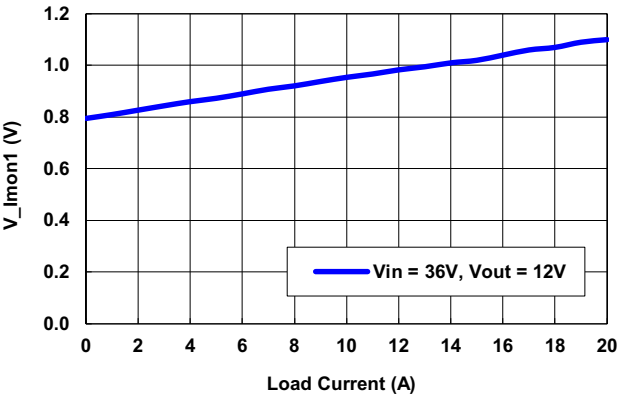


Figure 17. Dual-Phase Output Current I_{OUT} (DC) vs IMON1 Pin Voltage, R_{S_out} = 4mΩ, R_{IMON1} = 20k

Oscilloscope plots are taken using the ISL81806EVAL1Z evaluation board (Cont.)

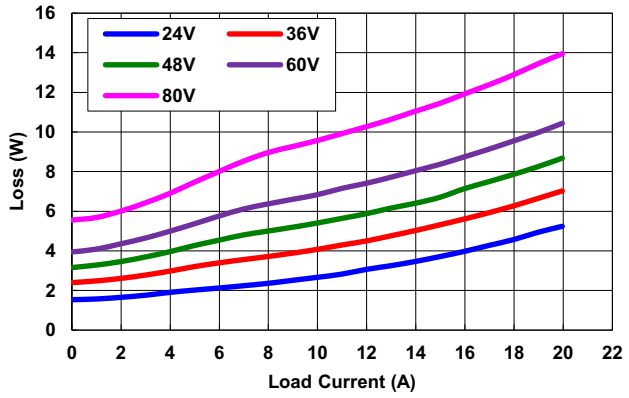


Figure 18. V_{OUT} = 12V CCM Mode Power Loss

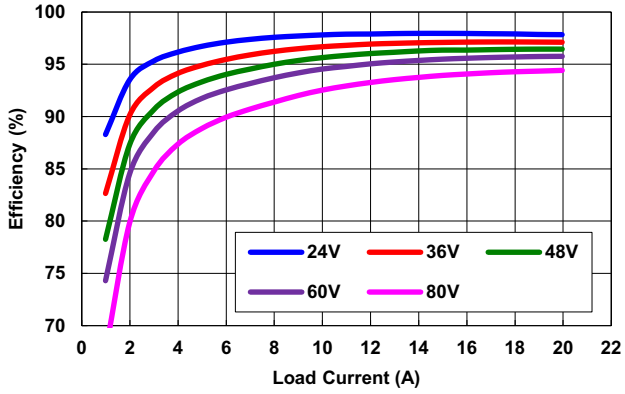


Figure 19. V_{OUT} = 12V CCM Mode Efficiency

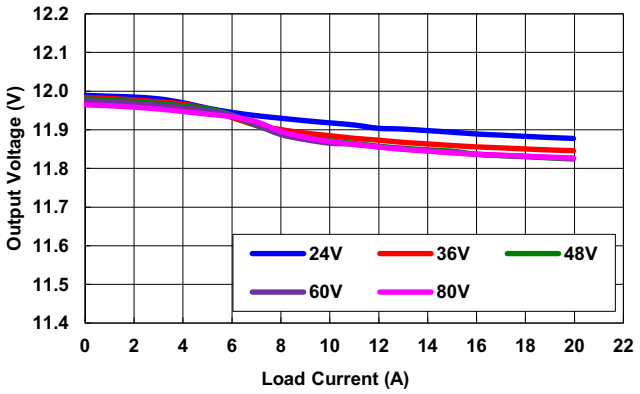


Figure 20. CCM V_{OUT} = 12V Load Regulation at 25°C

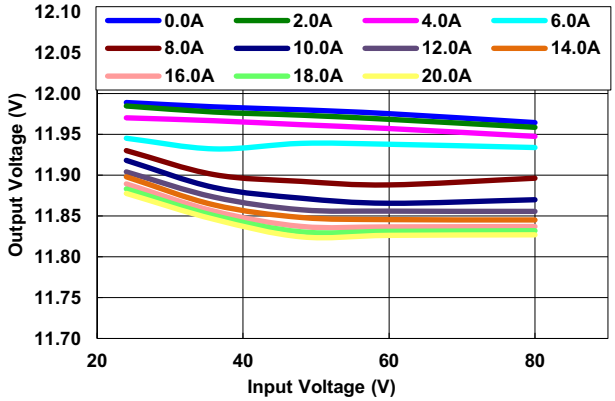


Figure 21. CCM Line Regulation at 25°C

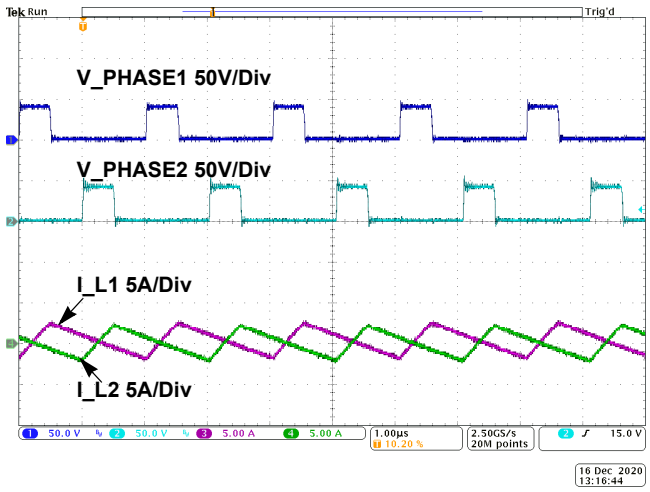


Figure 22. Dual-Phase Waveforms, V_{IN} = 48V, I_{OUT} = 0A, CCM Mode

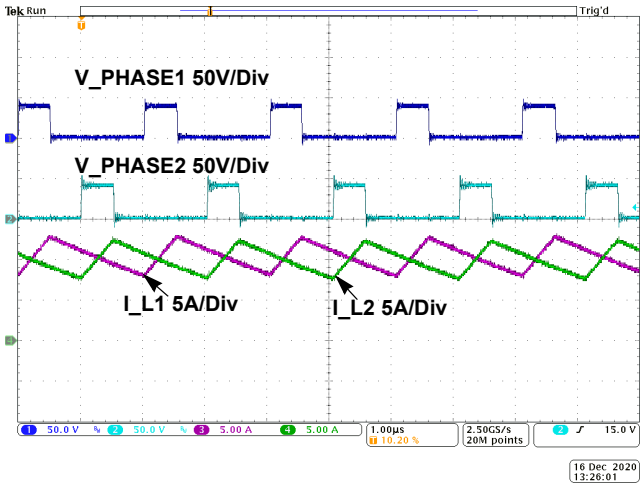


Figure 23. Dual-Phase Waveforms, V_{IN} = 48V, I_{OUT} = 20A, CCM Mode

Oscilloscope plots are taken using the ISL81806EVAL1Z evaluation board (Cont.)

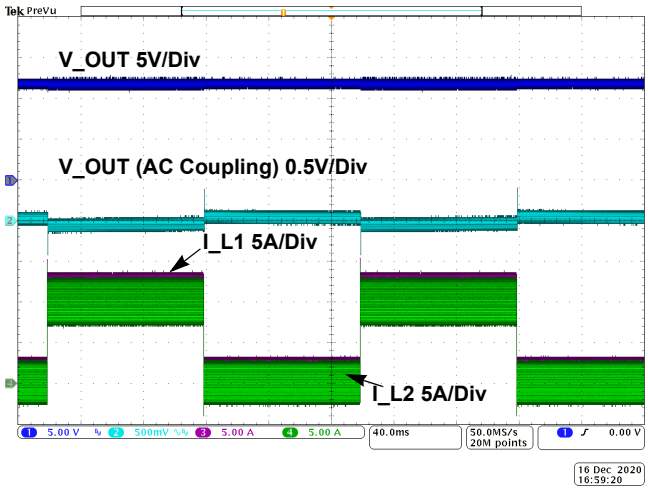


Figure 24. Dual-Phase Waveforms, V_{IN} = 48V, I_{OUT} = 0A-20A Dynamic, CCM Mode

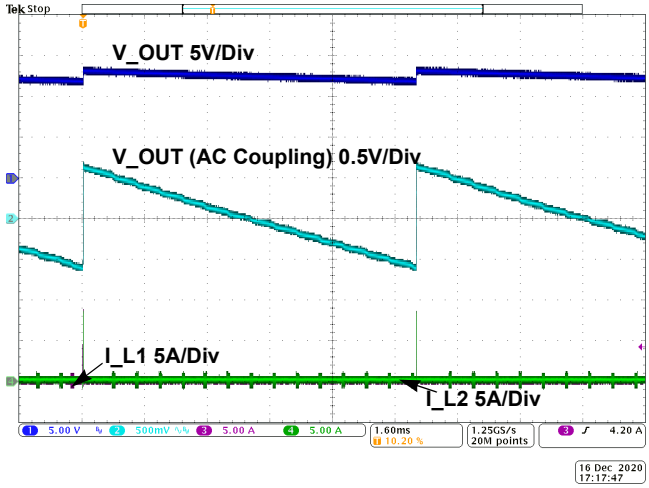


Figure 25. Dual-Phase Waveforms, Burst Mode Waveforms, V_{IN} = 48V, I_{OUT} = 0A

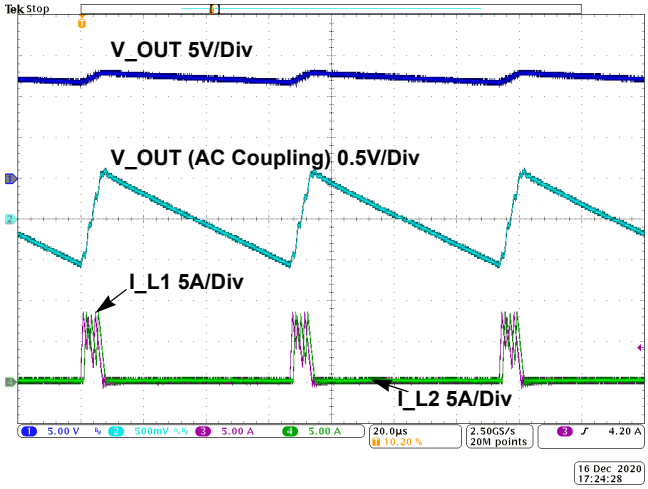


Figure 26. Dual-Phase Burst Mode V_{IN} = 48V, I_{OUT} = 1A

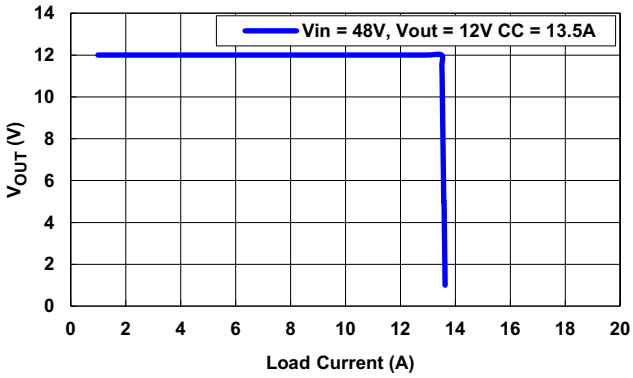


Figure 27. Constant Voltage (CV) and Constant Current (CC) Operation

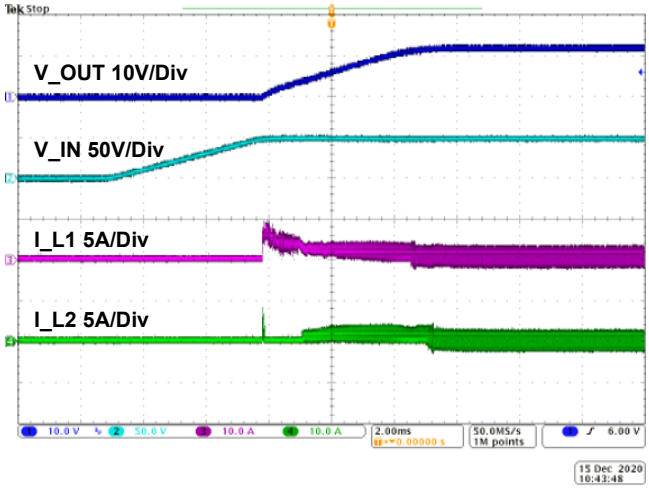


Figure 28. Dual-Phase Waveforms, Start-Up Waveform, V_{IN} = 48V I_O = 0A, CCM

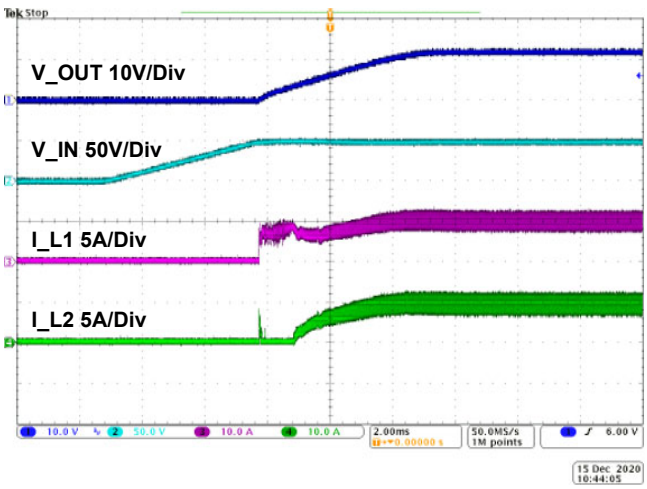


Figure 29. Dual-Phase Waveforms, Start-Up Waveform, V_{IN} = 48V I_O = 20A, CCM

5. Functional Description

5.1 General Description

The ISL81806 implements dual-buck, dual-phase, and multi-phase controls with a PWM controller, internal drivers, references, protection circuits, current and voltage control inputs, PLL clock and sync control logic, and current monitor outputs. See Figure 5.

The ISL81806 is a peak-current mode controller. The two channels can independently control their outputs and maintain a 180° phase shift between the two PWM outputs. The controller integrates two control loops to regulate V_{OUT} and average maximum I_{OUT} in each buck channel.

The driver and protection circuits are also integrated into each buck channel to simplify the end design.

The part has an independent enable/disable pin for each buck channel that provides a flexible power-up sequencing and a simple V_{IN} UVP implementation. Each buck channel has soft-start control. The soft-start time is programmable by adjusting the soft-start capacitor on the SS/TRK pin.

5.2 Internal 5.3V Linear Regulator (VDD), Ext. Bias Supply (EXTBIAS), and 5V Linear Regulator (VCC5V)

The ISL81806 provides two input pins, VIN and EXTBIAS, and two internal LDOs for the VDD gate driver supply. A third LDO generates VCC5V from VDD. VCC5V provides power to all internal functional circuits other than the gate drivers. Bypass the output (VDD) of the linear regulator with a 10µF capacitor to the power ground. Also, bypass the third linear regulator output (VCC5V) with a 10µF capacitor to the signal ground. VCC5V is monitored by a power-on-reset circuit, which disables all regulators when VCC5V falls below 3.5V.

Both LDOs from VIN and EXTBIAS can source over 75mA for VDD to power the gate drivers. When driving large FETs at a high switching frequency, little or no regulator current may be available for external loads. The LDO from VDD to VCC5V can also source over 75mA to supply the IC internal circuit. Although the current consumed by the internal circuit is low, the current supplied by VCC5V to the external loads is limited by VDD. For example, a single large FET with 15nC total gate charge requires 15nC x 300kHz = 4.5mA (15nC x 600kHz = 9mA).

Also, at higher input voltages with larger FETs, the power dissipation across the internal 5.3V LDO increases. Excessive power dissipation across this regulator must be avoided to prevent junction temperature rise. Thermal protection is triggered if the die temperature increases above +160°C because of excessive power dissipation.

When large FETs or high input voltages are used, an external 6V bias voltage can be applied to the EXTBIAS pin to alleviate excessive power dissipation. When the voltage at the EXTBIAS pin is higher than typical 4.8V, the LDO from EXTBIAS activates and the LDO from VIN is disconnected. The recommended maximum voltage at the EXTBIAS pin is 36V. For applications with V_{OUT} significantly lower than V_{IN}, EXTBIAS is usually back biased by V_{OUT} to reduce the LDO power loss. An external UVLO circuit might be necessary to ensure smooth soft-starting. When back biased from V_{OUT}, Renesas recommends adding a 10µF capacitor on the EXTBIAS pin and using a diode to connect the EXTBIAS pin to V_{OUT} to prevent the EXTBIAS pin voltage from being pulled low because of a V_{OUT} short-circuit condition.

The two VDD LDOs have an overcurrent limit for short-circuit protection. The VIN to VDD LDO current limit is set to a typical value of 120mA. The EXTBIAS to VDD LDO current limit is set to a typical 140mA.

5.3 Enable (EN/UVLO) and Soft-Start Operation

ISL81806 provides an enable pin to each of the two buck channels, EN/UVLO1 and EN/UVLO2. Pulling the pin high or low can enable or disable the corresponding output. When the voltage of either of the two pins is higher than 1.3V, the three LDOs are enabled. After the VCC5V reaches the POR threshold, the controller is powered up to initialize its internal circuit. When EN/UVLO1 or EN/UVLO2 is higher than the 1.8V accurate Undervoltage Lockout (UVLO) threshold, the soft-start circuitry of the corresponding channel becomes active. An internal 2µA current source begins charging up the soft-start capacitor connected from the corresponding soft-start pin

SS/TRK1 or SS/TRK2/OV to GND. The voltage error amplifier reference voltage is clamped to the voltage on the SS/TRK1 or SS/TRK2/OV pin. Therefore, the corresponding output voltage rises from 0V to regulation as the soft-start pin voltage rises from 0V to 0.8V. Charging of the soft-start capacitor continues until the voltage on the soft-start pin reaches 3V. The soft-start pin can also be used for tracking.

The soft-start time is set by the value of the soft-start capacitor connected from the soft-start pin to GND. Inrush current during start-up is alleviated by adjusting the soft-start time.

The typical soft-start time is set according to Equation 2:

(EQ. 2) $$t_{SS} = 0.8V\left(\frac{C_{SS}}{2\mu A}\right)$$

When the soft-start time set by external C_{SS} or tracking is less than 1.7ms, an internal soft-start circuit of 1.7ms takes over the soft-start.

In dual-phase applications, the internal SS/TRK2 signal is disconnected from SS/TRK2/OV pin and internally connected to SS/TRK1 pin. The V_{OUT} soft-start is controlled by the SS/TRK1 pin with a doubled charge current of 4µA. Therefore, the external C_{SS} capacitor needs to be doubled to achieve the same soft-start time.

PGOOD toggles high when the Channel 1 output voltage is in regulation.

Pulling both EN/UVLO1 and EN/UVLO2 pins lower than the EN falling threshold V_{ENSS_THF} typical 0.9V disables the PWM output and internal LDOs to achieve low standby current. The SS/TRK1 and SS/TRK2/OV are also discharged to GND by an internal MOSFET with 70Ω $r_{DS(ON)}$ in each of the buck channels. For applications with more than a 1µF capacitor on the soft-start pin, Renesas recommends adding a 100Ω to 1kΩ resistor in series with the capacitor to share the power loss during the discharge.

With the use of the accurate UVLO threshold, an accurate V_{IN} Undervoltage Protection (UVP) feature is implemented by feeding the V_{IN} into the EN/UVLO pin using a voltage divider (R_{UV1} and R_{UV2}) shown in Figure 30.

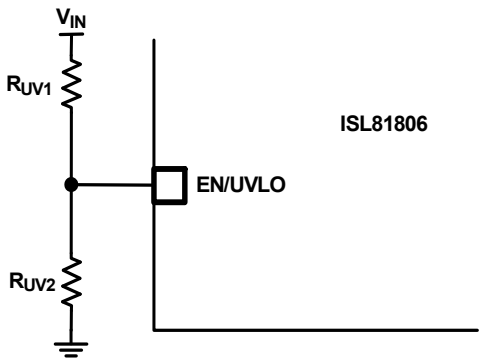


Figure 30. V_{IN} Undervoltage Protection

The V_{IN} UVP rising threshold is calculated using Equation 3.

(EQ. 3) $$V_{UVRISE} = \frac{V_{UVLO\_THR}(R_{UV1} + R_{UV2}) - 1.4x10^{-6}\ R_{UV1}R_{UV2}}{R_{UV2}}$$

where V_{UVLO_THR} is the EN/UVLO pin UVLO rising threshold, typically 1.8V.

The V_{IN} UVP falling threshold is calculated using Equation 4:

(EQ. 4) $$V_{UVFALL} = \frac{V_{UVLO\_THR}(R_{UV1} + R_{UV2}) - I_{UVLO\_HYST}\ R_{UV1}R_{UV2}}{R_{UV2}}$$

where I_{UVLO_HYST} is the UVLO hysteresis current, typically 3.4µA.

5.4 Tracking Operation

Each of the two ISL81806 buck outputs can track an external supply. To implement tracking, connect a resistive divider between the external supply output and ground. Connect the center point of the divider to the SS/TRK (SS/TRK1 for Channel 1 and dual-phase or SS/TRK2/OV for Channel 2) pin of the corresponding buck channel. The resistive divider ratio sets the ramping ratio between the two voltage rails. To implement coincident tracking, set the tracking resistive divider ratio the same as the output-resistive divider given by Equation 5. Ensure that the voltage at SS/TRK is greater than 0.8V when the master rail reaches regulation.

To minimize the impact of the 2µA soft-start current on the tracking function, Renesas recommends using resistors less than 10kΩ for the tracking resistive divider.

When the SS/TRK pin voltage is pulled down to less than 0.3V by the external tracking source, the pre-bias startup DE mode function is enabled again. The output voltage can not be pulled down if the load current is not high enough.

When Overcurrent Protection (OCP) is triggered, the internal minimum soft-start time circuit determines the 55ms OCP soft-start hiccup off-time.

5.5 Control Loops

The ISL81806 integrates two identical buck controllers that provide two output voltages below the input voltage or one output voltage using two phases. Peak current mode PWM control algorithm is used in the two controllers. The Renesas proprietary control architecture uses a current sense resistor in series with the inductor to sense the inductor current (see Figure 1 and Figure 5). By using an RC network, the inductor current signal can also be derived from the inductor voltage using DCR sensing. The inductor current is controlled by the voltage on the COMP pin, which is the lowest output of the error amplifiers Gm1 and Gm3 for Channel 1 or Gm2 and Gm4 for Channel 2. As the simplest example, when the output is regulated to a constant voltage, the FB1 or FB2 pin receives the output feedback signal, which is compared to the internal reference by Gm1 or Gm2. Lower output voltage creates higher COMP voltage, which leads to a higher PWM duty cycle to deliver more current to the output. Conversely, higher output voltage creates lower COMP voltage, which leads to a lower PWM duty cycle to reduce the current delivered to the output.

The ISL81806 has four error amplifiers (Gm1-4), which can control Channel 1 output voltage (Gm1) and current (Gm3), and Channel 2 output voltage (Gm2) and current (Gm4). In this architecture, both channels can provide constant voltage and constant current output.

5.5.1 Output Voltage Regulation Loop

The ISL81806 provides a precision 0.8V internal reference voltage to set the output voltage. Based on this internal reference, the output voltage is set from 0.8V up to a level determined by the feedback voltage divider, as shown in Figure 31.

A resistive divider from the output to ground sets the output voltage. Connect the center point of the divider to the FB pin. The output voltage value is determined by Equation 5.

(EQ. 5) $$V_{OUT} = 0.8V\left(\frac{R_{FBO1} + R_{FBO2}}{R_{FBO2}}\right)$$

where R_{FBO1} is the top resistor of the feedback divider network and R_{FBO2} is the bottom resistor connected from FB to ground, shown in Figure 31.

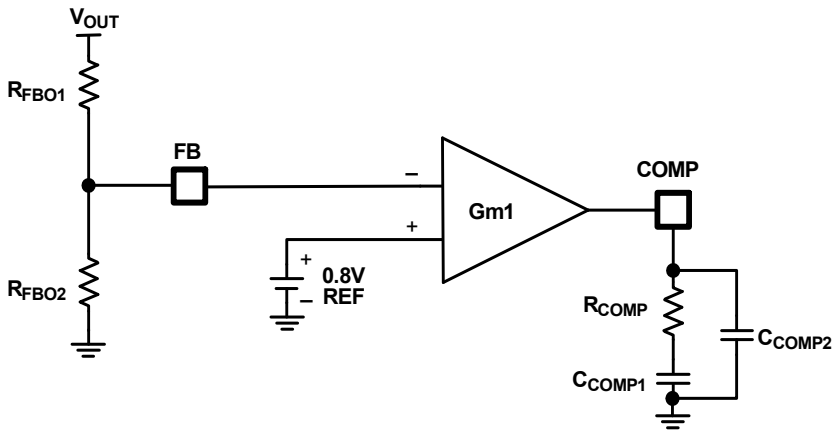


Figure 31. Output Voltage Regulator

As shown in Figure 31, the R_{COMP}, C_{COMP1}, and C_{COMP2} network connected to the Gm1 regulator output COMP pin is needed to compensate the loop for stable operation. The loop stability can be affected by many different factors such as V_{IN}, V_{OUT}, load current, switching frequency, inductor value, output capacitance, and the compensation network on COMP pin. For most applications, 47nF is a good value for C_{COMP1}. A larger C_{COMP1} makes the loop more stable by giving a larger phase margin, but the loop bandwidth is lower. C_{COMP2} is typically 1/10th to 1/30th of C_{COMP1} to filter high-frequency noise. A good starting value for C_{COMP2} is 2.2nF. A good starting value for R_{COMP} is 4.7k. Lower R_{COMP} improves stability but slows the loop response. Optimize the final compensation network with a bench test.

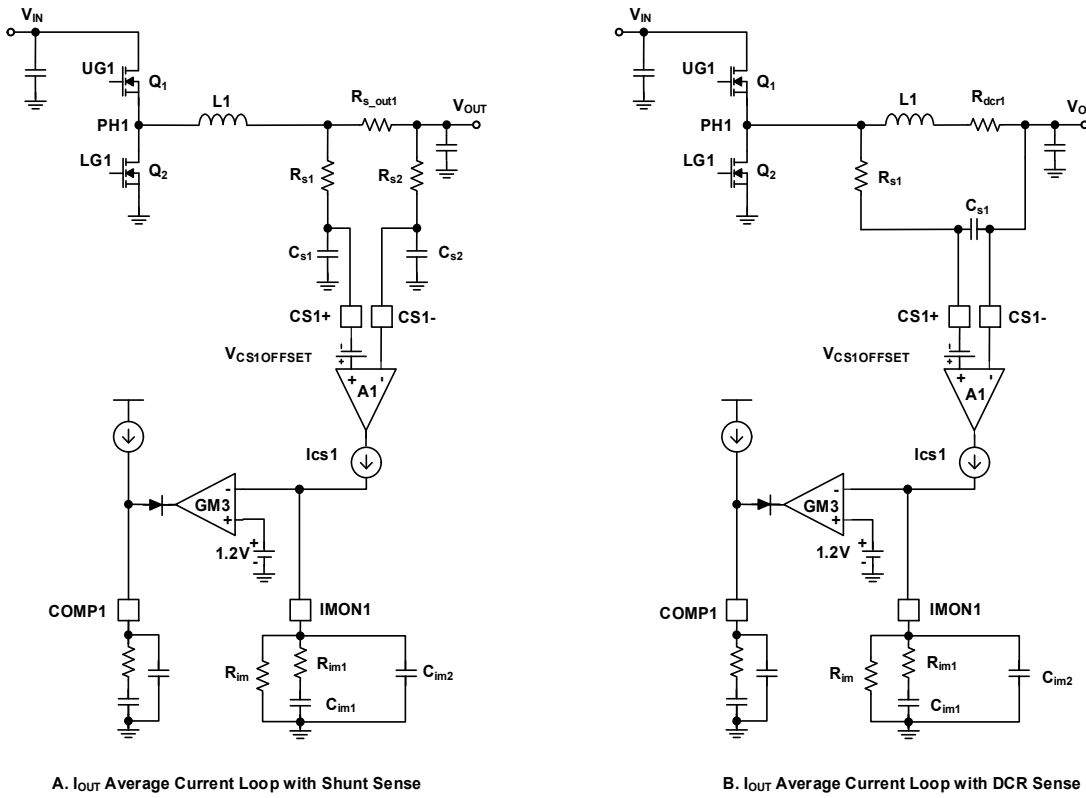
5.5.2 Output Average Current Monitoring and Regulation Loops

The ISL81806 has two current-sense amplifiers (A1 and A2) that monitor the output current of both channels. Figure 32 A shows the ISL81806 Channel 1 current shunt sense and monitor circuit, which is identical to Channel 2. The voltage signal on the current sense resistor R_{S_OUT1} is sent to the differential input of CS1+/CS1-, after the RC filters R_{S1}/C_{S1} and R_{S2}/C_{S2}. Renesas recommends using a 1Ω value for R_{S1} and R_{S2}, and a 10nF value for C_{S1} and C_{S2} to effectively damp the switching noise without significantly delaying the current signal or introducing too much error by the op-amp bias current. The A1 amplifier converts the current sense voltage signal to the current signal I_{CS1}.

(EQ. 6) $$I_{CS1} = [(I_{OUT1})R_{S\_OUT1} + V_{CS1OFFSET}]Gm_{CS1}$$

where

- I_{OUT1} is the Channel 1 inductor current
- $V_{CS1OFFSET}$ is the A1 input offset voltage
- Gm_{CS1} is the gain of A1, typical 200µS
- $V_{CS1OFFSET}$ Gm_{CS1} = $I_{CS1OFFSET}$. The typical value of $I_{CS1OFFSET}$ is 20µA.



A. I_{OUT} Average Current Loop with Shunt Sense

B. I_{OUT} Average Current Loop with DCR Sense

Figure 32. Output Average Current Monitoring and Regulation Loops

By connecting resistor R_{IM} on the IMON1 pin, the I_{CS1} current signal is transferred to a voltage signal. The RC network on the IMON1 pin (R_{IM1}, C_{IM1}, and C_{IM2}) is needed to remove the AC content in the I_{CS1} signal and ensure stable loop operation. The average voltage at the IMON1 pin is regulated to 1.2V by Gm3 for constant current control.

In dual-phase application, the internal IMON2 signal is disconnected from the IMON2 pin and internally connected to the IMON1 pin. The $I_{CS1OFFSET}$ is a doubled current 40µA.

The output constant current loop setpoint I_{OUTCC1} is calculated using Equation 7. See V_{AVOCP_CS1} in the Electrical Specifications table to estimate the setpoint tolerance.

(EQ. 7) $$I_{OUTCC1} = \frac{1.2 - I_{CS1OFFSET} \times R_{IM}}{R_{IM} \times R_{S\_OUT1} \times Gm_{CS1}}$$

Similar to the voltage control loop, the average current loop stability can be affected by many different factors such as V_{IN}, V_{OUT}, switching frequency, inductor value, output and input capacitance, and the RC network on the IMON1 pin. Because of the AC content in I_{CS1}, a larger C_{IM1} is needed. Larger C_{IM1} can also make the loop more stable by giving a larger phase margin, but the loop bandwidth is lower. For most applications, 47nF is a good value for C_{IM1}. C_{IM2} is typically 1/10th to 1/30th of C_{IM1} to filter high-frequency noise. R_{IM1} is needed to boost the phase margin. A good starting value for R_{IM1} is 5k. Optimize the final compensation network with iSim simulation and bench testing.

Figure 32 B shows the ISL81806 Channel 1 inductor DCR current sense and monitor circuit. Rdcr1 plays the same role as R_{S_OUT1} in the shunt current sense circuit. Renesas recommends keeping Rs1 x Cs1 = L1/Rdcr1. To minimize the error caused by the A1 input bias current, Renesas recommends keeping Rs1 less than 10k.

5.6 Light-Load Efficiency Enhancement

Set each of the two ISL81806 channels to DE and Burst mode to improve light-load efficiency. The LG1/PWM_MODE pin sets the DE or PWM mode operation in the initialization period before soft-start. During the initialization period, a typical 10µA current source $I_{MODELG1}$ from the LG1/PWM_MODE pin creates a voltage drop on the resistor R_{LG1} connected between the LG1/PWM_MODE pin and GND. When the voltage is lower than the typical 0.3V, PWM mode is set; otherwise, DE mode is set. **Note:** DE or PWM mode can only be selected during the initialization period and cannot be changed after initialization is complete.

To set for DE mode operation, select R_{LG1} to meet:

(EQ. 8) $$R_{LG1} x I_{MODELG1} > 0.34V$$

Note: This equation is accurate only when there is no pre-bias voltage on the VOUT for a GaN FET application. With a GaN FET application, there is an approximately 1MΩ resistance between the drain and the gate. The pre-bias voltage on the VOUT supplies to the gate through this 1MΩ resistor. The equation needs to be corrected by this factor. Most importantly, the gate voltage must be kept lower than the minimum gate threshold voltage of the GaN FET, which is typically 0.8V to avoid GaN FET damage in the initial stage. The voltage of LG1 should be higher than 0.3V during the initialization period. At the same time, the LG1 voltage should be lower than Vth of the GaN FET to avoid the GaN FET turning on.

When DE mode is set, the Channel 1 and 2 buck sync FET driven by LG1 and LG2 are all running in DE mode. The inductor current is not allowed to reverse (discontinuous operation) depending on the zero-cross detection reference level V_{CROSS1} for Channel 1 and V_{CROSS2} for Channel 2 sync FET. At light-load conditions, the converter goes into diode emulation. When the load current is less than the level set by $V_{IMON1BSTEN}$ or $V_{IMON2BSTEN}$ typical 815mV on the IMON1 or IMON2 pin, Channel 1 or 2 enters Burst mode. Equation 9 sets the Burst mode operation enter condition for Channel 1 as an example (see Figure 32). The same equation also applies to Channel 2.

(EQ. 9) $$R_{IM} x (I_{CS1OFFSET} + I_{OUT1} x R_{S\_OUT1} x Gm_{CS1}) < V_{IMON1BSTEN}$$

where:

- $I_{CS1OFFSET}$ is the output current sense op amp internal offset current, typical 20µA
- Gm_{CS1} is the output current sense op amp Gm, typical 200µS.

When the part enters Burst mode, the BSTEN pin goes low. To avoid any enter/exit chattering, add a 4-10MΩ resistor between the BSTEN and IMON1 or IMON2 pins to further expand the hysteresis.

In Burst mode, an internal window comparator takes control of the output voltage. The comparator monitors the FB1 or FB2 pin voltage for Channel 1 or 2. When the FB1 or FB2 pin voltage is higher than 0.81V, Channel 1 or 2 enters Low Power Off mode. Some unneeded internal circuits are powered off to further reduce power dissipation. When the FB1 or FB2 pin voltage drops to 0.8V, Channel 1 or 2 wakes up and runs in a fixed level peak current mode. The fixed level peak current is set by the level that the input current sense amplifier input voltage reaches $V_{BST-CS1}$ or $V_{BST-CS2}$ for Channel 1 or 2, typical 27mV. The output voltage increases in the wake-up period. When the output reaches 0.81V again, the controller enters Low Power Off mode again. When the load current increases, the Low Power Off mode period decreases. When the off-mode period disappears and the load current further increases, the output voltage drops. When the FB1 or FB2 pin voltage drops to 0.78V, Channel 1 or 2 exits Burst mode and runs in normal DE PWM mode. The voltage error amplifier takes control of the output voltage regulation.

In Low Power Off mode, the CLKEN pin goes low.

The DE and Burst mode operations also apply to dual-phase and multi-phase applications. By connecting the BSTEN and CLKEN pins in a multiple chip parallel system, the Burst mode enter/exit and burst on/off control are all synchronized.

Because V_{OUT} is controlled by a window comparator in Burst mode, a higher than normal low-frequency voltage ripple appears on V_{OUT}, which can generate audible noise if the inductor and output capacitors are not chosen properly. To avoid these drawbacks, disable the Burst mode by choosing a bigger R_{IM} to set the IMON1 pin voltage higher than 815mV at no load condition, shown in Equation 10 for Channel 1. Channel 1 runs in DE mode only. Pulse Skipping mode can also be implemented to lower the light-load power loss with a much lower output voltage ripple as V_{OUT1} is always controlled by the regulator Gm1. The same approach also applies to Channel 2 and dual-phase operation.

(EQ. 10) $R_{IM} x I_{CS1OFFSET} > V_{IMON1BSTEN}$

5.7 Pre-Biased Power-Up

Each of the two ISL81806 channels can soft-start with a pre-biased output by running in forced DE mode during soft-start. The output voltage is not pulled down during pre-biased start-up. The PWM mode is not active until the soft-start ramp reaches 90% of the output voltage set point times the feedback resistive divider ratio. Forced DE mode is set again when the SS/TRK pin voltage is pulled to less than 0.3V by either an internal or external circuit.

The overvoltage protection function is still operating during soft-start in DE mode.

5.8 Frequency Selection

Switching frequency selection is a trade-off between efficiency and component size. Low switching frequency improves efficiency by reducing FET switching loss. To meet the output ripple and load transient requirements, operation at a low switching frequency requires larger inductance and output capacitance. The switching frequency of the ISL81806 is set by a resistor connected from the RT/SYNC pin to GND according to Equation 1.

The frequency setting curve shown in Figure 33 assists in selecting the correct value for R_T.

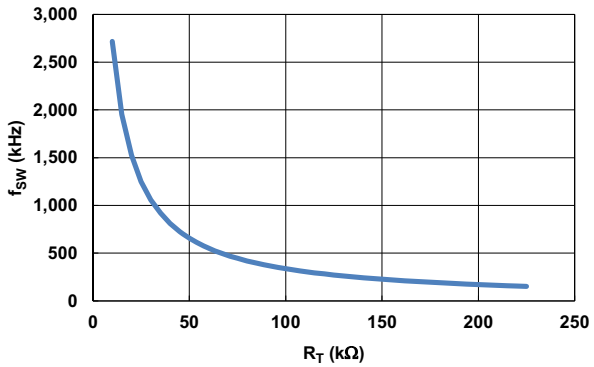


Figure 33. R_T vs Switching Frequency f_{SW}

5.9 Phase Lock Loop (PLL)

The ISL81806 integrates a high-performance PLL. The PLL ensures a wide range of accurate clock frequency and phase settings. It also makes the internal clock easily synchronized to an external clock with a frequency either lower or higher than the internal setting.

As shown in Figure 34, an external compensation network of R_{PLL}, C_{PLL1}, and C_{PLL2} is needed to connect to the PLL_COMP pin to ensure PLL stable operation. Renesas recommends choosing 2.7kΩ for R_{PLL}, 10nF for C_{PLL1}, and 820pF for C_{PLL2}. With the recommended compensation network, the PLL stability is ensured in the full clock frequency range of 100kHz to 2MHz.

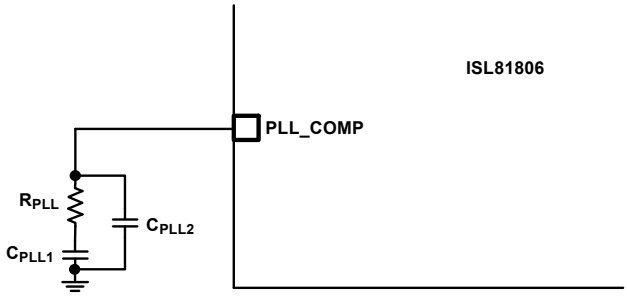


Figure 34. PLL Compensation Network

5.10 Frequency Synchronization, Multi-Phase Operation and Dithering

The RT/SYNC pin can synchronize the ISL81806 to an external clock or the CLKOUT/DITHER pin of another ISL81806. When the RT/SYNC pin is connected to the CLKOUT/DITHER pin of another ISL81806, the two controllers operate in cascade synchronization with phase interleaving.

When the RT/SYNC pin is connected to an external clock, the ISL81806 synchronizes to this external clock frequency. The frequency set by the R_T resistor can be either lower or higher than, or equal to the external clock frequency.

The CLKOUT/DITHER pin outputs a clock signal with approximately 300ns pulse width. The signal frequency is the same as the frequency set by the resistor from the RT pin to ground or the external sync clock. The signal rising edge phase angle to the rising edge of the internal clock or the external clock to the RT/SYNC pin can be set by the EN/UVLO2 pin connection and the voltage applied to the IMON2 pin. The phase interleaving can be implemented by the cascade connecting of the upstream chip CLKOUT/DITHER pin to the downstream chip RT/SYNC pin in a parallel system. Table 1 shows the CLKOUT/DITHER phase settings with a different EN/UVLO2 pin connection and IMON2 pin voltage.

Table 1. CLKOUT and Channel 2 Phase Shift vs EN/UVLO2 and IMON2 Voltage

CLKOUT Phase Shift (°)[1]	Channel 2 Phase Shift (°)[2]	IMON2 Voltage (V)	EN/UVLO2
90	180	0-4.3	Tie to EN/UVLO1
60	180	4.7-5	Tie to EN/UVLO1
240	120	3-5	Tie to SGND

1. CLKOUT Phase Shift: CLKOUT rising edge delay after UG1 rising edge.
2. Channel 2 Phase Shift: UG2 rising edge delay after UG1 rising edge.

When the IMON2 pin is actively used as the Channel 2 current monitor, the pin max voltage is 1.2V. The ISL81806 is running in a dual-output application.

When the IMON2 pin is tied to 5V or externally forced to higher than 3V, the ISL81806 is configured for a dual-phase application. The IMON2 pin internal Channel 2 current signal is connected to the IMON1 pin. The IMON1 pin monitors the sum of the Channel 1 and 2 current. The internal current sharing circuit is also enabled.

Meanwhile, the SS/TRK2/OV pin internal SS/TRK2 signal is disconnected from the SS/TRK2/OV pin and connected to the SS/TRK1 pin. The SS/TRK2/OV pin is connected to the OVP signal, which is pulled high by a MOSFET with about 4.5k $r_{DS(ON)}$ when an output overvoltage fault is triggered. The COMP2/CLKEN pin internal COMP2 signal is disconnected from the COMP2/CLKEN pin and connected to the COMP1 pin. The COMP2/CLKEN pin is connected to the CLKEN signal, which is pulled low by a MOSFET with about 4.5k $r_{DS(ON)}$ during burst mode off time. The FB2/BSTEN pin internal FB2 signal is disconnected from the FB2/BSTEN pin and connected to the FB1 pin. The FB2/BSTEN pin is connected to the BSTEN signal, which is pulled low by a MOSFET with about 4.5k $r_{DS(ON)}$ when the controller enters burst mode.

In multi-chip cascade parallel operation, the CLKOUT/DITHER pin of the upstream chip is connected to the RT/SYNC pin of the downstream chip. The FB1, COMP1, IMON1, EN/UVLO1, SS/TRK1, FB2/BSTEN, COMP2/CLKEN, and SS/TRK2/OV pins of all the paralleled chips are tied together to implement current sharing, synchronized start-up, burst mode operation, and OVP protection.

The CLKOUT/DITHER pin provides a dual-function option. When a capacitor C_{DITHER} is connected on the CLKOUT/DITHER pin, the internal circuit disables the CLKOUT function and enables the DITHER function. When the CLKOUT/DITHER pin voltage is lower than 1.05V, a typical 8µA current source $I_{DITHERSO}$ charges the capacitor on the pin. When the capacitor voltage is charged to more than 2.2V, a typical 10µA current source $I_{DITHERSI}$ discharges the capacitor on the pin. A sawtooth voltage waveform shown in Figure 35 is generated on the CLKOUT/DITHER pin. The internal clock frequency is modulated by the sawtooth voltage on the CLKOUT/DITHER pin. The clock frequency dither range is set to typically ±15% of the frequency set by the resistor on the RT/SYNC pin. The dither function is lost when the chip is synchronized to an external clock.

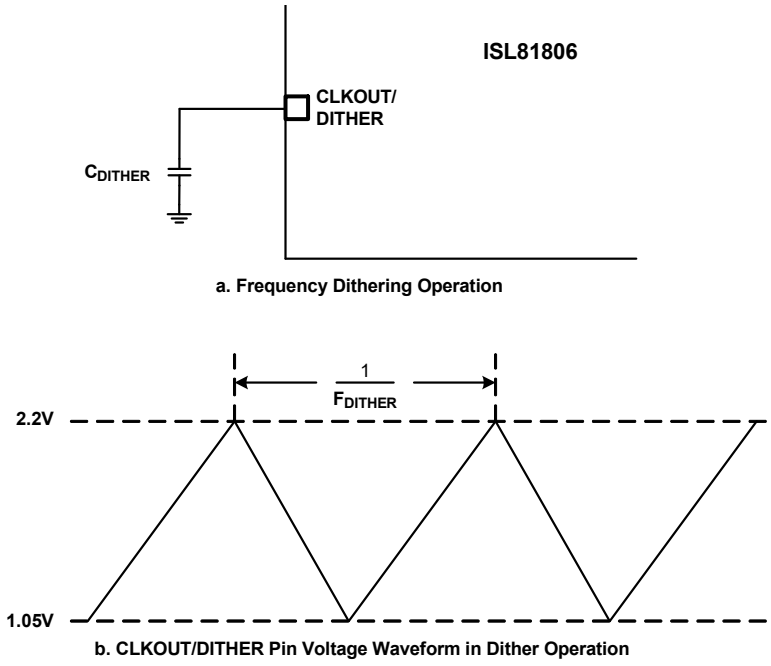


Figure 35. Frequency Dithering Operation

The dither frequency F_{DITHER} is calculated using Equation 11. Renesas recommends setting C_{DITHER} between 10nF and 1µF. With C_{DITHER} too low, the part may not be able to set to Dither mode. With a higher C_{DITHER}, the discharge power loss at disable, or power off is higher, leading to higher thermal stress to the internal discharge circuit. To avoid a low-frequency ripple on V_{OUT}, lower the dither frequency to less than 1/10 of the loop bandwidth.

(EQ. 11) $$F_{DITHER} = \frac{3.865x10e(-6)}{C_{DITHER}}$$

5.11 Parallel Operation Current Sharing

When ISL81806 is set to a dual-phase application, the internal Renesas proprietary instant active current sharing circuit assures the accurate current sharing between the two phases in steady-state and start-up or load transient conditions. Because the current signal from IMON1 is the sum of the two phases, reduce the resistor between the IMON1 pin and GND to half of the value in a single-phase application. To assure proper parallel operation, Renesas recommends selecting between 17k and 24k resistance for the resistor between the IMON1 pin and GND. The RC network is added on the IMON1 pin to filter the ripple noise in the inductor currents and improve the control loop stability.

Multiple ISL81806 controlled buck converters can be paralleled to each other in cascade as described in Frequency Synchronization, Multi-Phase Operation and Dithering. The currents in the paralleled converters can be shared by connecting the IMON1 pin of each controller to enable the internal Renesas proprietary instant active current sharing circuit. The 4-phase ISL81806 controlled buck converter is shown in Figure 36. To minimize the input current and output voltage ripple, the CLKOUT phase delay of the first ISL81806 controller is programmed to 90° for a perfect phase interleaving.

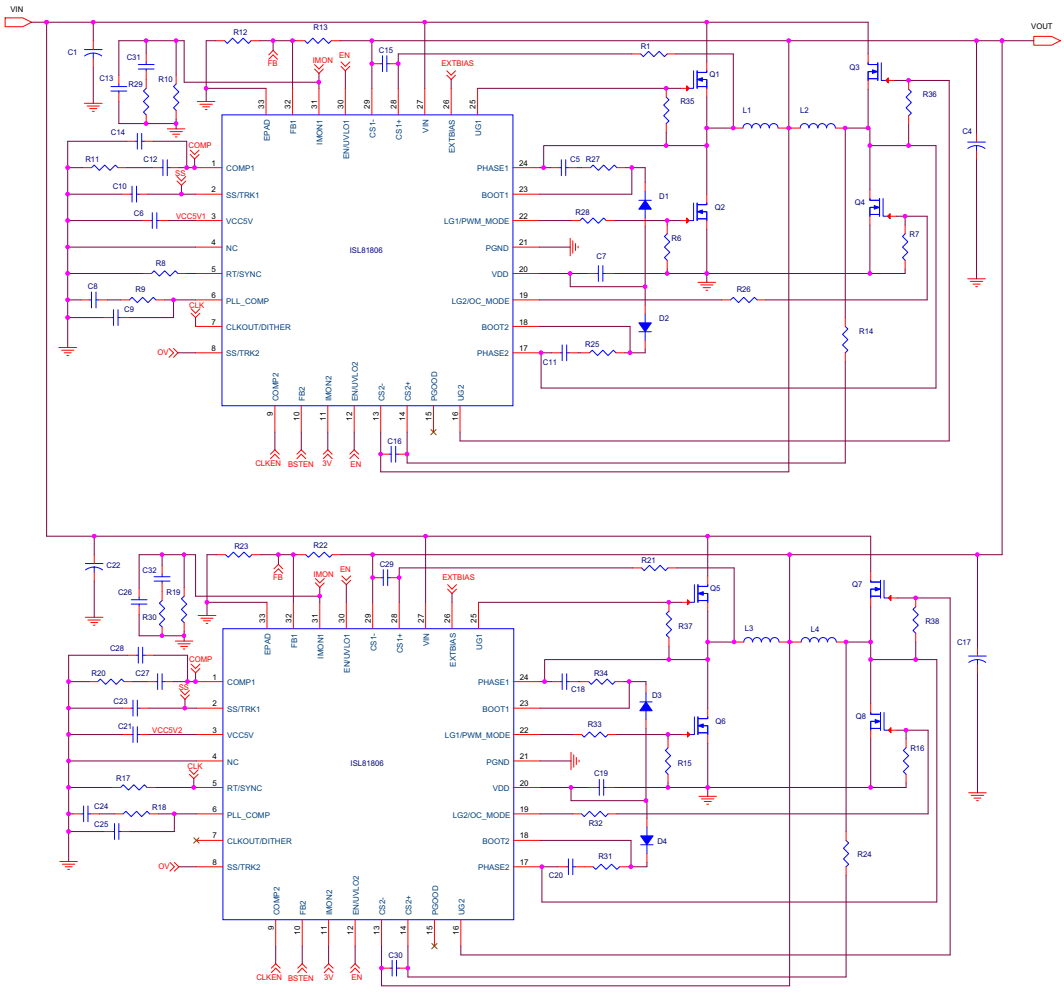


Figure 36. ISL81806 Multi-Phase Current Sharing Circuit

Figure 36 shows the connections between the two paralleled converters.

5.12 Gate Drivers

The ISL81806 integrates two almost identical high voltage driver pairs to drive both buck FET pairs. Each driver pair consists of a gate control logic circuit, a low-side driver, a level shifter, and a high-side driver.

The ISL81806 incorporates a fixed dead time for the drivers. It provides approximately 20ns dead time between the switching of the upper and lower FETs.

The low-side gate driver is supplied from VDD and provides a 1.4A peak sink and 1.1A peak source current. The high-side gate driver can also deliver peak 1.4A sink and 1.1A source current. Gate-drive voltage for the upper FET is generated by a flying capacitor boot circuit. A boot capacitor connected from the BOOT pin to the PHASE node provides power to the high-side FET driver. As shown in Figure 37, the boot capacitor is charged up to VDD by an external Schottky diode during low-side FET on-time (phase node low). To limit the peak current in the Schottky diode, place an external resistor between the BOOT pin and the boot capacitor. This small series resistor also damps any oscillations caused by the resonant tank of the parasitic inductances in the traces of the board and the input capacitance of the FET.

At start-up, the low-side FET turns on first and forces PHASE to ground to charge the BOOT capacitor to 5.3V if the diode voltage drop is ignored. After the low-side FET turns off, the high-side FET is turned on by closing an internal switch between BOOT and UGATE. This provides the necessary gate-to-source voltage to turn on the upper FET, an action that boosts the 5.3V gate drive signal above V_{IN}. The current required to drive the upper FET is drawn from the internal 5.3V regulator supplied from either VIN or EXTBIAS pin.

The BOOT to PHASE voltage is monitored internally. When the voltage drops to 3.9V at no switching condition, a minimum off-time pulse is issued to turn off the high-side FET and turn on the low-side FET to refresh the bootstrap capacitor and maintain the upper driver bias voltage.

To optimize EMI performance or reduce phase node ringing, place a small resistor between the BOOT pin to the positive terminal of the bootstrap capacitor.

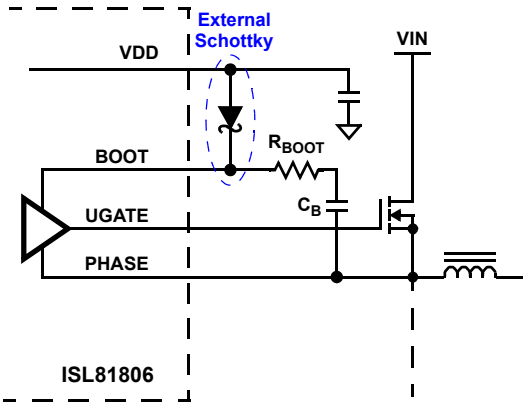


Figure 37. Upper Gate Driver Circuit

5.13 Power-Good Indicator

The power-good pin can monitor the status of the Channel 1 output voltage. PGOOD is true (open-drain) 1.1ms after the FB1 pin is within ±11% of the reference voltage. The pin is pulled down when Channel 1 output is not within ±11% of the nominal voltage or EN1 pin is pulled LOW.

There is no extra delay when the PGOOD pin is pulled LOW.

6. Protection Circuits

The converter output and input are monitored and protected against overload, overvoltage, and undervoltage conditions.

6.1 Input Undervoltage Lockout (UVLO)

The ISL81806 includes input UVLO protection, which keeps the device in a reset condition until a proper operating voltage is applied. UVLO protection shuts down the ISL81806 if the input voltage drops below 3.2V. The controller is disabled when UVLO is asserted. When UVLO is asserted, Power-Good (PGOOD) is valid and is de-asserted.

6.2 VCC5V Power-On Reset (POR)

The ISL81806 sets its VCC5V POR rising threshold at 4V and the falling threshold at 3.5V when supplied by V_{IN}. EXTBIAS can only be applied after VCC5V reaches its POR rising threshold.

6.3 Overcurrent Protection (OCP)

6.3.1 Output Average Overcurrent Protection

As described in Output Average Current Monitoring and Regulation Loops, the ISL81806 can regulate the output current of both channels with close loop control. This provides a constant current type of overcurrent protection for both channels. It can be set to a hiccup type of protection by selecting a different value of the resistor connected between LG2/OC_MODE and GND.

The output constant or hiccup average OCP set point and I_{OUTCC} are calculated using Equation 7 in Output Average Current Monitoring and Regulation Loops.

The average OCP mode is set by a resistor connected from the LG2/OC_MODE pin to ground during the initiation stage before soft-start. During the initiation stage, the LG2/OC_MODE pin sources out a typical 10µA current $I_{MODELG2}$ to set the voltage on the pin. If the pin voltage is less than typical 0.3V, the OCP is set to Constant Current-mode. Otherwise, the OCP is set to hiccup mode.

Note: The LG2 setting is also calculated by Equation 8 by replacing the RLG1 and IMODELG1 with RLG2 and IMODELG2. This equation is accurate only when there is no pre-bias voltage on the VOUT for a GaN FET application. With a GaN FET application, there is an approximately 1MΩ resistance between the drain and the gate. The pre-bias voltage on the VOUT supplies to the gate through this 1MΩ resistor. The equation needs to be corrected by this factor. Most importantly, the gate voltage must be kept lower than the minimum gate threshold voltage of the GaN FET, which is typically 0.8V to avoid GaN FET damage in the initial stage. The voltage of the LG2 should be higher than 0.3V during the initialization period. At the same time, the LG2 voltage should be lower than Vth of the GaN FET to avoid the GaN FET turning on.

In hiccup OCP mode, after the average current is higher than the setpoint for 32 consecutive switching cycles, the converter turns off for 55ms before a restart is issued.

6.3.2 First Level Pulse-by-Pulse Peak Current Limit

As shown in Figure 32 in Output Average Current Monitoring and Regulation Loops as an example, the inductor peak current is sensed by the shunt resistor R_{S_OUT1} and amplifier A1 for Channel 1. For both Channel 1 and 2, when the voltage drops on R_{S_OUT} and reaches the set point $V_{OCSET-CS}$ typical 82mV, the high-side FET is turned off. The first level peak current limit set point I_{OCPP1} is calculated using Equation 12.

(EQ. 12) $$I_{OCPP1} = \frac{V_{OCSET-CS}}{R_{S\_OUT1}}$$

6.3.3 Second Level Hiccup Peak Current Protection

To avoid any false trip in peak current-mode operation, a minimum on or blanking time is set to the PWM signal. The first level pulse-by-pulse current limit circuit cannot further reduce the PWM duty cycle in the minimum on-time. For both Channel 1 and 2, the ISL81806 integrates a second-level hiccup type of peak current protection. When the voltage drops on R_{S_OUT} and reaches the set point $V_{OCSET\text{-}CS\text{-}HIC}$ (typical 98mV), the converter turns off by turning off all switches for 55ms before a restart is issued. The second level peak current protection setpoint I_{OCPP2} is calculated using Equation 13.

(EQ. 13) $$I_{OCPP2} = \frac{V_{OCSET\text{-}CS\text{-}HIC}}{R_{S\_OUT1}}$$

6.3.4 Pulse-by-Pulse Negative Peak Current Limit

In cases of OVP protection, the inductor current becomes negative. For the Channel 1 example, the negative current is sensed by the shunt resistor R_{S_OUT1} and amplifier A1 as shown in Figure 32. For both channel 1 and 2, when the voltage drops on R_{S_OUT} and reaches the set point $V_{OCSET\text{-}ISEN}$ (typical -60mV), the low-side FET is turned off and the high-side FET is turned on. The negative peak current limit set point (I_{OCPPN}) is calculated using Equation 14.

(EQ. 14) $$I_{OCPPN} = \frac{V_{OCSET\text{-}ISEN}}{R_{S\_OUT1}}$$

6.4 Overvoltage Protection (OVP)

The overvoltage set point is set at 114% of the nominal output voltage set by the feedback resistors. In the case of an overvoltage event, the IC attempts to bring the output voltage back into regulation by keeping the high-side FET turned off and low-side FET turned on. If the OV condition continues, the inductor current goes negative to trip the negative peak current limit. The converter reverses direction to transfer energy from the output end to the input end. Input voltage is pushed high if the input source impedance is not low enough. The IC can be damaged if the input voltage goes higher than its maximum limit. If the overvoltage condition is corrected and the output voltage drops to the nominal voltage, the controller resumes normal PWM switching. The OV pin is pulled high when output OVP trips.

6.5 Over-Temperature Protection (OTP)

The ISL81806 incorporates an over-temperature protection circuit that shuts the IC down when a die temperature of +160°C is reached. Normal operation resumes when the die temperature drops below +145°C through the initiation of a full soft-start cycle. During the OTP shutdown, the IC consumes only 100µA current. When the controller is disabled, thermal protection is inactive. This helps achieve a low shutdown current of 5µA.

7. Layout Guidelines

Careful attention to layout requirements is necessary for the successful implementation of an ISL81806 based DC/DC converter. The ISL81806 switches at a high frequency, so the switching times are short. At these switching frequencies, even the shortest trace has significant impedance. Also, the peak gate drive current rises significantly in an extremely short time. The transition speed of the current from one device to another causes voltage spikes across the interconnecting impedances and parasitic circuit elements. These voltage spikes can degrade efficiency, generate EMI, and increase device voltage stress and ringing. Careful component selection and proper Printed Circuit Board (PCB) layout minimize the magnitude of these voltage spikes.

The three sets of critical components in a DC/DC converter using the ISL81806 are:

- Controller
- Switching power components
- Small signal components

The switching power components are the most critical from a layout point of view because they switch a large amount of energy, which tends to generate a large amount of noise. The critical small signal components are those connected to sensitive nodes or those supplying critical bias currents. A multilayer PCB is recommended.

7.1 Layout Considerations

- Place the input capacitors, buck FETs, inductor, and output capacitor first. Isolate these power components on dedicated areas of the board with their ground terminals adjacent to one another. Place the input and output high frequency decoupling ceramic capacitors close to the FETs.
- If signal components and the IC are placed in a separate area to the power train, use full ground planes in the internal layers with shared SGND and PGND to simplify the layout design. Otherwise, use separate ground planes for the power ground and the small-signal ground. Connect the SGND and PGND close to the IC. DO NOT connect them anywhere else.
- Keep the loop formed by the input capacitor, the buck top FET, and the buck bottom FET as small as possible.
- Keep the current paths from the input capacitor to the buck FETs, the power inductor, and the output capacitor as short as possible with maximum allowable trace widths.
- Place the PWM controller IC close to the lower FETs. The FETs gate drive connections should be short and wide. Place the IC over a quiet ground area. Avoid switching ground loop currents in this area.
- Place the VDD bypass capacitor close to the VDD pin of the IC and connect its ground end to the PGND pin. Connect the PGND pin to the ground plane using a via. Do not directly connect the PGND pin to the SGND EPAD.
- Place the gate drive components (BOOT diodes and BOOT capacitors) together near the controller IC.
- Use copper-filled polygons or wide short traces to connect the junction of the upper FET, lower FET, and output inductor. Also, keep the PHASE nodes connection to the IC short. DO NOT oversize the copper islands for the PHASE nodes. Because the phase nodes are subjected to high dv/dt voltages, the stray capacitor formed between these islands and the surrounding circuitry tends to couple switching noise.
- Route all high-speed switching nodes away from the control circuitry.
- Create a separate small analog ground plane near the IC. Connect the SGND pin to this plane. Connect all small-signal grounding paths including feedback resistors, current monitoring resistors and capacitors, soft-starting capacitors, loop compensation capacitors and resistors, and EN pull-down resistors to this SGND plane.
- Use a pair of traces with a minimum loop for the input or output current sensing connection.
- Ensure the feedback connection to the output capacitor is short and direct.

7.2 General EPAD Design Considerations

Figure 38 shows how to use vias to remove heat from the IC.

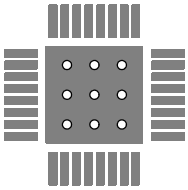


Figure 38. PCB Via Pattern

Fill the thermal pad area with vias. A typical via array fills the thermal pad footprint so that their centers are three times the radius apart from each other. Keep the vias small but not so small that their inside diameter prevents solder wicking through during reflow.

Connect all vias to the ground plane. The vias must have low thermal resistance for efficient heat transfer. Ensure a complete connection of the plated through hole to each plane.

8. Component Selection Guideline

8.1 Power FET Considerations

The FETs are chosen for optimum efficiency given the potentially wide input voltage range and output power requirement. Select these FETs based on $r_{DS(ON)}$, gate supply requirements, and thermal management considerations.

The maximum operating voltage of the FET is decided by the maximum V_{IN} voltage. Choose the FETs based on their maximum operating voltage with enough margin for safe operation.

The power dissipation of the FET is based on conduction loss and switching loss. The power loss of the upper and lower FETs are calculated using Equation 15 and Equation 16. The conduction losses are the main source of power dissipation for the lower FET. Only the upper FET has significant switching losses because the lower device turns on and off into near zero voltage. The equations assume linear voltage-current transitions and do not model power loss because of the reverse recovery of the lower FET body diode.

(EQ. 15) $$P_{UPPER} = \frac{(I_{OUT}^{2})(r_{DS(ON)})(V_{OUT})}{V_{IN}} + \frac{(I_{OUT})(V_{IN})(t_{SW})(f_{SW})}{2}$$

(EQ. 16) $$P_{LOWER} = \frac{(I_{OUT}^{2})(r_{DS(ON)})(V_{IN} - V_{OUT})}{V_{IN}}$$

A large gate-charge increases the switching time, t_{SW}, which increases the switching losses of the buck upper FETs. Ensure that all four FETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal resistance specifications.

8.2 Inductor Selection

The inductor is selected to meet the output voltage ripple requirements. The inductor value determines the ripple current and the ripple voltage of the converter is a function of the ripple current and the output capacitor(s) ESR. The ripple voltage expression is given in the capacitor selection section and the ripple current is approximated by Equation 17.

(EQ. 17) $$\Delta I_{LBuck} = \frac{(V_{IN} - V_{OUT})(V_{OUT})}{(f_{SW})(L)(V_{IN})}$$

The ripple current ratio is usually 30% to 70% of the inductor average current at the full output load condition.

8.3 Output Capacitor Selection

In general, select the output capacitors to meet the dynamic regulation requirements including ripple voltage and load transients. The selection of output capacitors is also dependent on the inductor, so some inductor analysis is required to select the output capacitors.

One of the parameters limiting the response of the converter to a load transient is the time required for the inductor current to slew to its new level. The ISL81806 provides either a 0% or maximum duty cycle in response to a load transient.

The response time is the time interval required to slew the inductor current from an initial current value to the load current level. During this interval, the difference between the inductor current and the transient current level must be supplied by the output capacitor(s). The output capacitance is minimized if faster loop compensation is used. Also, if the load transient rise time is slower than the inductor response time, it reduces the requirement on the output capacitor.

The maximum capacitor value required to provide the full, rising step, transient load current during the response time of the inductor is shown in Equation 18:

(EQ. 18) $$C_{OUT} = \frac{(L)(I_{TRAN})^2}{2(V_{IN} - V_{OUT})(DV_{OUT})}$$

where:

- C_{OUT} is the output capacitor(s) required
- L is the inductor, I_{TRAN} is the transient load current step
- V_{IN} is the input voltage
- V_{OUT} is output voltage
- DV_{OUT} is the drop-in output voltage allowed during the load transient

High-frequency capacitors initially supply the transient current and slow the load rate of change seen by the bulk capacitors. The bulk filter capacitor values are determined by the Equivalent Series Resistance (ESR) and voltage rating requirements in addition to actual capacitance requirements.

The output voltage ripple is because of the inductor ripple current and the ESR of the output capacitors as defined by Equation 19:

(EQ. 19) $$V_{RIPPLE} = \Delta I_L(ESR)$$

where ΔI_{LBuck} is calculated in Equation 17.

Place high-frequency decoupling capacitors as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load circuitry for specific decoupling requirements.

Use only specialized low-ESR capacitors intended for switching regulator applications for the bulk capacitors. In most cases, multiple small case electrolytic capacitors perform better than a single large case capacitor.

The stability requirement on the selection of the output capacitor is that the ESR zero (f_Z) is between 2kHz and 60kHz. The ESR zero can help increase the phase margin of the control loop.

This requirement is shown in Equation 20:

(EQ. 20) $$C_{OUT} = \frac{1}{2\pi(ESR)(f_Z)}$$

In conclusion, the output capacitors must meet the following criteria:

- They must have enough bulk capacitance to sustain the output voltage during a load transient while the output inductor current is slewing to the value of the load transient.
- The ESR must be sufficiently low to meet the desired output voltage ripple because of the supplied ripple current.
- Place the ESR zero in a large range to provide additional phase margin.

8.4 Input Capacitor Selection

The important parameters for the input capacitor(s) are the voltage rating and the RMS current rating. For reliable operation, select input capacitors with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and 1.5 times is a conservative guideline. The AC RMS input current varies with the load giving in Equation 21:

(EQ. 21) $$I_{RMS} = \sqrt{DC - DC^2} \times I_{OUT}$$

where DC is duty cycle.

The maximum RMS current supplied by the input capacitance occurs at V_{IN} = 2 X V_{OUT}, DC = 50% as shown in Equation 22:

(EQ. 22) $$I_{RMS} = \frac{1}{2} \times I_{OUT}$$

Use a mix of input bypass capacitors to control the voltage ripple across the FETs. Use ceramic capacitors for the high-frequency decoupling and bulk capacitors to supply the RMS current. Place small ceramic capacitors close to the FETs to suppress the voltage induced in the parasitic circuit impedances.

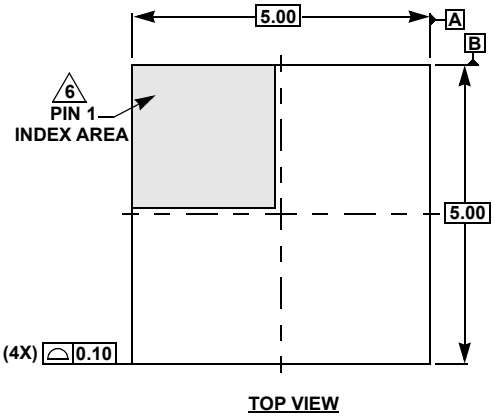
Note: Solid tantalum capacitors can be used but use caution regarding the capacitor surge current rating. These capacitors must be capable of handling the surge current at power-up.

9. Package Outline Drawing

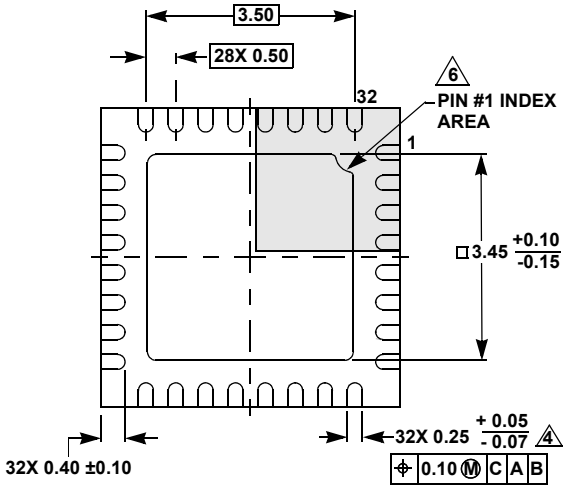
For the most recent package outline drawing, see L32.5x5A.

L32.5x5A

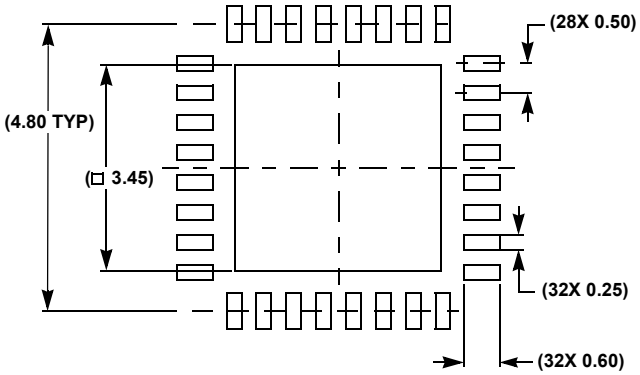
32 Lead Thin Quad Flat No-Lead Plastic Package
Rev 1, 5/17



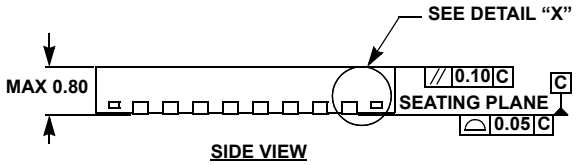
TOP VIEW



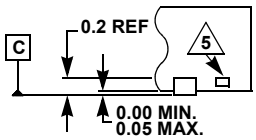
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for reference only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ±0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

10. Ordering Information

Part Number[1][2]	Part Marking	Package Description (RoHS Compliant)	Pkg. Dwg. #	Carrier Type[3]	Temp. Range
ISL81806FRTZ-T	81806 FRTZ	32 Ld 5x5 TQFN	L32.5x5A	Reel, 3k	-40 to +125°C
ISL81806EVAL1Z	Dual-Phase Evaluation Board for TQFN				

1. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. For Moisture Sensitivity Level (MSL), see the ISL81806 device page. For more information about MSL, see TB363.
3. See TB347 for details about reel specifications.

Table 2. Key Differences Between Family of Parts

Part Number	VDD (V)	Dead Time	Maximum Switching Frequency (MHz)	Gate Source Current (A)	Gate Sink Current (A)
ISL81802	8	Adaptive	1	2	3
ISL81806	5.3	Fixed	2	1.1	1.4

11. Revision History

Rev.	Date	Description
1.01	Jan 28, 2022	Updated IMON1 and IMON2 pin descriptions. Removed PWM1/2 Burst Mode Exit Threshold specifications. Updated PWM1/2 Peak-to-Peak Sawtooth Amplitude typical values from 1.5V to 1V. Updated the Light-Load Efficiency Enhancement section. Updated the tape and reel quantity from 6k to 3k and removed ISL81806FRTZ-T7A in the ordering information table.
1.00	Sep 28, 2021	Initial release

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(Rev.1.0 Mar 2020)

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