ISL75054M

Radiation Tolerant Ultra Low Noise 1A LDO

Description

The ISL75054M is a radiation tolerant low dropout linear regulator with ultra-low noise and high PSRR intended for ADC, RF, and other noise sensitive applications. The device has an operating supply voltage range of 2.7V to 30V and an output voltage range of 0.5V to V_{IN} - V_{DO}. Built-in protection includes V_{IN} - V_{OUT} foldback current limiting, externally programmable current limit, and over-temperature protection. The ISL75054M features excellent noise performance and PSRR for radiation tolerant LDOs, with ultra-low RMS noise of 3.9µV_{RMS} from 10Hz to 100kHz and ultrahigh PSRR of 104dB at 120Hz.

The ISL75054M is fabricated on a Silicon-On Insulator (SOI) process which makes it latch-up free.The ISL75054M is offered in a 16 lead heatsink thin shrink small outline package (HTSSOP) and operates across the full military temperature range of -55°C to +125°C.

Applications

Power Supplies for:

- ADC/DAC Reference, High Speed/Precision Data Converters
- RF PLLs, VCOs, Mixers, LNAs, PAs
- Low Noise Instrumentation Amplifier

Features

- Qualified to Renesas Rad Tolerant Screening and QCI Flow (R34TB0004EU)
- Ultra-low RMS noise: 3.9µV_{RMS} from 10Hz-100kHz
- Ultra-low spot noise: 11.5nV/√Hz at 10kHz
- Ultrahigh PSRR
  - 104dB at 120Hz, 71dB at 10kHz, 39dB at 100kHz, 28dB at 1MHz, and 27dB at 10MHz
- Input voltage range (V_{IN}): 2.7V to 30V
- Output voltage range (V_{OUT}): 0.5V to V_{IN} -V_{DO}
- Low dropout voltage (V_{DO}): 379mV
  - I_{OUT} = 1A, V_{IN} = 3.3V, R_{SET} = 33kΩ
- Output voltage set using a single resistor
- Programmable current limit with V_{IN} - V_{OUT} foldback current limiting
- TID Radiation Lot Acceptance Testing (RLAT) (LDR: ≤10mrad(Si)/s)
  - ISL75054M30VZ: 30krad(Si)
  - ISL75054M50VZ: 50krad(Si)
- SEE Characterization
  - No DSEE for V_{IN} = 32V at 46MeV•cm^2/mg
  - SEFI <2.5µm^2 at 46MeV•cm^2/mg
  - V_{OUT} SET <2% at 46MeV•cm^2/mg

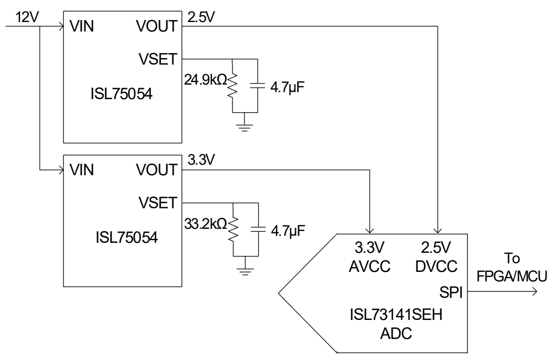


Figure 1. Typical Application

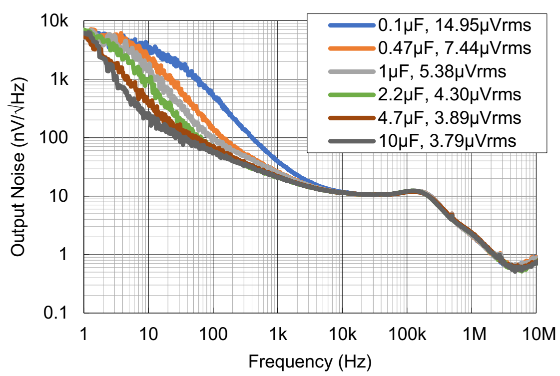


Figure 2. Noise Spectral Density vs C_{SET} Capacitor V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} = 1A (RMS noise 10Hz to 100kHz)

Contents

1. Overview

1.1 Typical Application Schematic

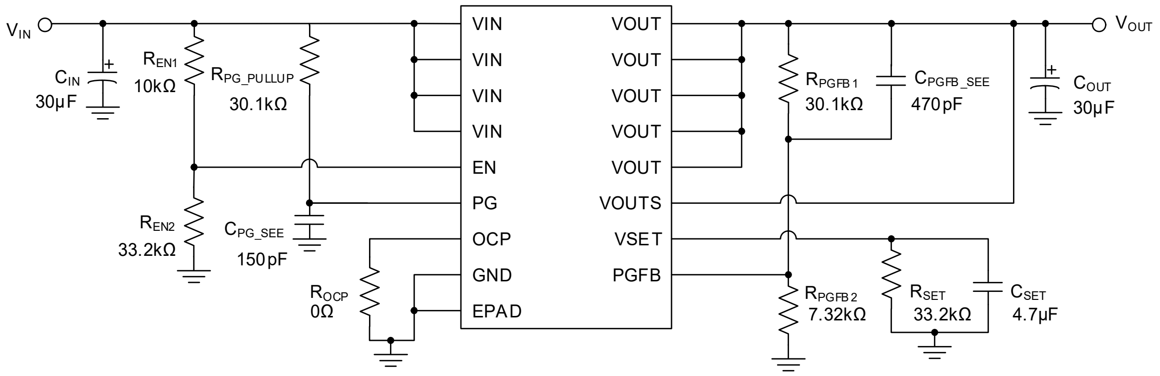


Figure 3. Plastic HTTSOP Typical Application for 3.3V Output

1.2 Block Diagram

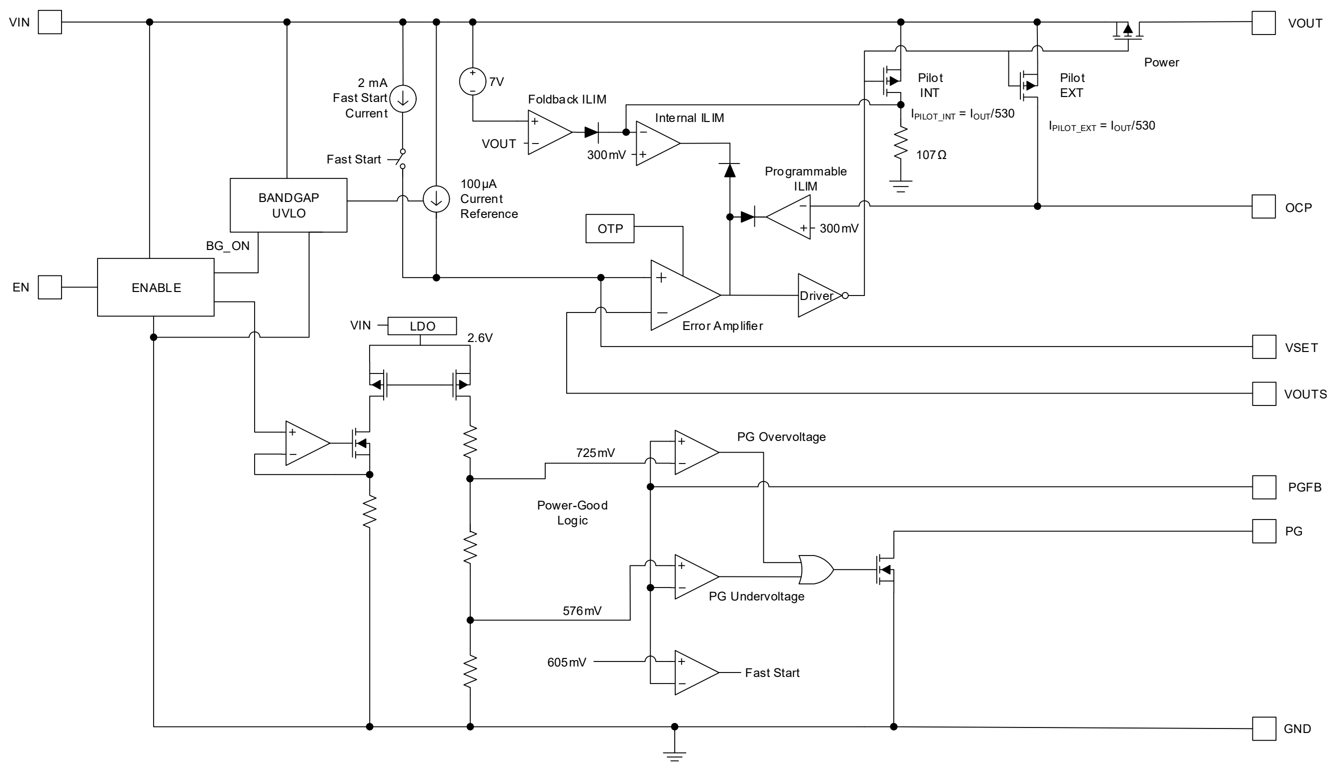


Figure 4. Functional Block Diagram

2. Pin Information

2.1 Pin Assignments

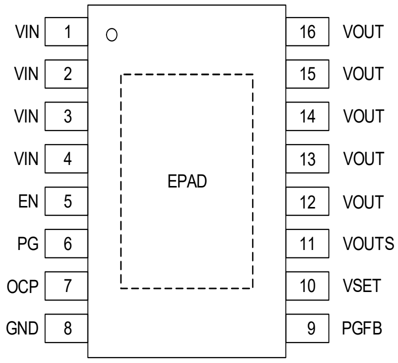
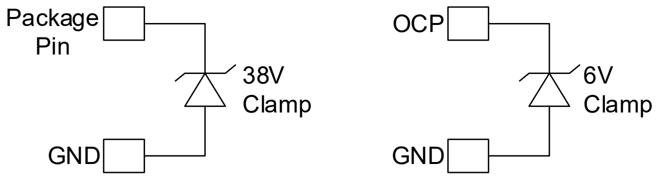


Figure 5. Pin Assignment - Top View

2.2 Pin Descriptions

Pin Number	Pin Name	ESD Circuit	Description
1	VIN	1	Input supply pins. VIN range is from 2.7V to 30V. This pin requires sufficient input capacitance from VIN to GND. 30µF is recommended and should be placed close to the device pins.
2	VIN	1	
3	VIN	1	
4	VIN	1	
5	EN	1	Enable pin. When set above 1.14V nominally, the device is enabled.
6	PG	1	Power-Good output. The output is open-drain logic, connect a pull-up resistor to a logic supply or VIN. For SEE mitigation, connect a 150pF capacitor from PG to GND. PG stays low and fast start-up functionality is disabled by connecting PGFB to VIN.
7	OCP	2	Overcurrent protection. OCP allows the current limit to be programmed with an external resistor, R_{OCP}, between a typical range of 0.2A to 1.4A. Connect OCP directly to GND to set the maximum current limit. *Note*: The OCP pin sources a 530:1 ratio of the current out of VOUT. Refer to Overcurrent Protection for more details.
8	GND	-	Ground pin. Connect to the PCB GND plane.
9	PGFB	1	Power-good feedback. To enable fast start-up functionality and power-good detection, connect an external resistor divider from VOUT so that 665mV is provided to PGFB at the nominal output voltage. For SEE mitigation, connect a 470pF capacitor from VOUT to PGFB. Connect PGFB to VIN to disable fast start-up and PG functions when not required.
10	VSET	1	Output voltage set. VSET sources a precision 100µA current that flows through the external R_{SET} resistor to GND. VSET sets the soft-start output voltage ramp rate through an external capacitor, C_{SET}, to GND. C_{SET} also provides filtering to internal device noise. Renesas recommends selecting C_{SET} between 0.47µF and 10µF. Refer to Output Voltage for more information about setting the output voltage and VSET Capacitance: Noise and Soft-Start for more information about configuring the soft-start time.
11	VOUTS	1	Output voltage sense. VOUTS is the inverting input to the error amplifier. Connect VOUTS directly to the output capacitor.
12	VOUT	1	Output voltage pins. A capacitance is required from VOUT to GND, 30µF is recommended. VOUT is set through a resistor from the VSET pin to GND and can range from 0.5V to V_{IN} - V_{DO}.
13	VOUT	1	
14	VOUT	1	
15	VOUT	1	
16	VOUT	1	

Pin Number	Pin Name	ESD Circuit	Description
-	EPAD	-	The EPAD functions as a heatsink. Connect to PCB GND to tie the die substrate to the GND pin.



Circuit 1 Circuit 2

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
VIN	GND - 0.3	+35	V
EN, PG, PGFB, VSET, VOUTS, VOUT	GND - 0.3	+35	V
VOUTS - VSET	- 0.3	+0.3	V
VIN[1]	GND - 0.3	+32	V
OCP	GND - 0.3	+6.5	V
Junction Temperature	-55	+150	°C
Storage Temperature	-65	+150	°C
Human Body Model (Tested per MIL-STD-883 TM3015.7)	-	1.5	kV
Charged Device Model (Tested per JS-002-2022)	-	1.25	kV
Latch-Up (Tested per JESD-78E; Class 2, Level A) at 125°C	-	±100	mA

1. Tested under a heavy ion environment at LET = 46MeV•cm^2/mg at 125°C. Refer to Single-Event Effects Testing for more information regarding test setup.

3.2 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
VIN	2.7	30	V
VSET, VOUTS, VOUT	0.5	V_{IN}-V_{DO}	V
EN, PG, PGFB	0	30	V
Ambient Temperature	-55	125	°C

3.3 Outgas Testing

Specification (Tested per ASTM E595, 1.5)	Value	Unit
Total Mass Lost[1]	0.04	%
Collected Volatile Condensible Material[1]	<0.01	%
Water Vapor Recovered	0.03	%

1. Outgassing results meet NASA requirements of total mass loss <1% and collected volatile condensible material <0.1%.

3.4 Thermal Information

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	16 Ld HTSSOP Package	θ_{JA}[1]	Junction to ambient	33	°C/W
		θ_{JC}[2]	Junction to case	2.5	

1. θ_{JA} is measured in free air with the component mounted with solder on a high-effective thermal conductivity test board with direct attach features in free air. See TB379.
2. For θ_{JC}, the case temperature location is taken at the center of the exposed metal pad on the package bottom.

3.5 Electrical Specifications

Default test conditions unless otherwise specified: V_{IN} = V_{OUT} + 0.5V or 2.7V, whichever is greater unless otherwise noted. Maximum I_{OUT} is defined as 1A for V_{IN}-V_{OUT} <= 2.2V, 100mA for 2.2V < V_{IN}-V_{OUT} ≤ 15V, 60mA for 15V < V_{IN}-V_{OUT} ≤ 29.4V, 50mA for V_{IN}-V_{OUT} > 29.4V. Typical values are at T_J = +25°C. **Boldface limits apply across the operating temperature range, -55°C to +125°C by characterization with production testing at +25°C; over a total ionizing dose of 30krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL75054M30VZ); or over a total ionizing dose of 50krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL75054M50VZ).**

Parameter	Test Conditions	Temp.	Min	Typ[1]	Max	Unit
Power Supply						
Input Voltage Range	-	-55 to +125°C	**2.7**	-	**30**	V
Input Supply UVLO Rising	EN = 2.25V	-55 to +125°C	**2.3**	2.58	**2.7**	V
Input Supply UVLO Falling	EN = 2.25V	-55 to +125°C	**2.2**	2.4	**2.5**	V
Input Supply UVLO Hysteresis	-	-55 to +125°C	-	0.18	**0.3**	V
Output Current	-	-55 to +125°C	-	-	**1**	A
Operating Supply Current	I_{OUT} = 0A; V_{OUT} = 0.9V; V_{IN} = 2.7V	-55 to +125°C	-	1.7	**2.5**	mA
	I_{OUT} = 0A; V_{OUT} = 0.9V, V_{IN} = 30V	-55 to +125°C	-	6.9	**8.5**	mA
	I_{OUT} = 0A; V_{OUT} = 29V, V_{IN} = 30V	-55 to +125°C	-	2.3	**3.5**	mA
	I_{OUT} = 0A; V_{OUT} = 0.5V; V_{IN} = 2.7V	-55 to +125°C	-	1.6	**2.5**	mA
	I_{OUT} = 0A; V_{OUT} = 0.5V; V_{IN} = 30V	-55 to +125°C	-	6.9	**8.5**	mA
	I_{OUT} = 0A; V_{IN}-V_{OUT} = V_{DO}	-55 to +125°C	-	2.2	**3.5**	mA
Shutdown Current	EN = 0V; V_{IN} = 6V	-55 to +125°C	-	198	**350**	µA
	EN = 0V; V_{IN} = 30V	-55 to +125°C	**-**	320	**450**	µA
V_{SET} Current	V_{IN} = 2.7V to 30V; V_{OUT} = 0.9V to V_{IN} -V_{DO}; I_{OUT} = 1A, or 50mA for V_{IN}-V_{OUT} > 2.2V	-55°C	98.5	100	101.5	µA
		+25°C	98.5	100	101.5	µA
		+125°C	98.5	100	101.5	µA
		+25°C (Post Rad)	98.5	100	101.5	µA
	V_{IN} = 2.7V to 30V; V_{OUT} = 0.5V; I_{OUT} = 1A, or 50mA for V_{IN}-V_{OUT} > 2.2V	-55°C	98.5	100.8	104	µA
		+25°C	98.5	100.8	104	µA
		+125°C	98.5	100.8	106.5	µA
		+25°C (Post Rad)	98.5	100.8	104	µA
V_{SET} Fast Start Current	V_{PGFB} = 560mV; V_{IN} = 2.7V; V_{SET} = 0.9V	-55 to +125°C	**1.5**	2	**2.4**	mA
Output						
Output Voltage Range	V_{IN} = 2.7V to 30V	-55 to +125°C	**0.5**	-	**VIN - VDO**	V

Default test conditions unless otherwise specified: V_{IN} = V_{OUT} + 0.5V or 2.7V, whichever is greater unless otherwise noted. Maximum I_{OUT} is defined as 1A for V_{IN}-V_{OUT} <= 2.2V, 100mA for 2.2V < V_{IN}-V_{OUT} ≤ 15V, 60mA for 15V < V_{IN}-V_{OUT} ≤ 29.4V, 50mA for V_{IN}-V_{OUT} > 29.4V. Typical values are at T_J = +25°C. **Boldface limits apply across the operating temperature range, -55°C to +125°C by characterization with production testing at +25°C; over a total ionizing dose of 30krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL75054M30VZ); or over a total ionizing dose of 50krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL75054M50VZ). (Cont.)**

Parameter	Test Conditions	Temp.	Min	Typ[1]	Max	Unit
Output Offset Voltage	V_{IN} = 2.7V to 30V; V_{OUT} = 0.9V to V_{IN} -V_{DO}; I_{OUT} = 0mA	-55°C	-	1.75	6	mV
		+25°C	-	1.75	6	mV
		+125°C	-	1.75	6	mV
		+25°C (Post Rad)	-	1.75	6	mV
	V_{IN} = 2.7V to 30V; V_{OUT} = 0.9V to V_{IN} -V_{DO}; Maximum I_{OUT}	-55°C	-	2.4	8	mV
		+25°C	-	2.4	8	mV
		+125°C	-	2.4	8	mV
		+25°C (Post Rad)	-	2.4	8	mV
	V_{IN} = 2.7V to 30V; V_{OUT} = 0.5V; I_{OUT} = 0mA	-55°C	-	5	18	mV
		+25°C	-	5	18	mV
		+125°C	-	5	18	mV
		+25°C (Post Rad)	-	5	18	mV
	V_{IN} = 2.7V to 30V; V_{OUT} = 0.5V; Maximum I_{OUT}	-55°C	-	6.7	20	mV
		+25°C	-	6.7	20	mV
		+125°C	-	6.7	20	mV
		+25°C (Post Rad)	-	6.7	20	mV
Line Regulation, $\Delta V_{OS}/\Delta V_{IN}$	V_{OUT} = 0.9V	-55 to +125°C	**-20**	-1.1	**5**	µV/V
	V_{OUT} = 0.5V	-55 to +125°C	**-45**	-5	**15**	µV/V
Line Regulation, $\Delta I_{SET}/\Delta V_{IN}$	V_{OUT} = 0.9V	-55 to +125°C	**-10**	1.2	**10**	nA/V
	V_{OUT} = 0.5V	-55 to +125°C	**-5**	7.8	**20**	nA/V
Load Regulation, ΔV_{OUT}	V_{IN} = 2.7V; V_{OUT} = 0.9V; I_{OUT} = 0mA to 1A	-55 to +125°C	**-3**	-1	**0**	mV
	V_{IN} = 2.7V; V_{OUT} = 0.5V; I_{OUT} = 0mA to 1A	-55 to +125°C	**-5**	-2.2	**0**	mV
	V_{IN} = 16V, V_{OUT} = 15V; I_{OUT} = 0mA to 1A	-55 to +125°C	**-3**	-1.1	**0**	mV
	V_{IN} = 30V; V_{OUT} = 29V; I_{OUT} = 0mA to 1A	-55 to +125°C	**-3**	-1.1	**0**	mV

Default test conditions unless otherwise specified: V_{IN} = V_{OUT} + 0.5V or 2.7V, whichever is greater unless otherwise noted. Maximum I_{OUT} is defined as 1A for V_{IN}-V_{OUT} <= 2.2V, 100mA for 2.2V < V_{IN}-V_{OUT} ≤ 15V, 60mA for 15V < V_{IN}-V_{OUT} ≤ 29.4V, 50mA for V_{IN}-V_{OUT} > 29.4V. Typical values are at T_J = +25°C. **Boldface limits apply across the operating temperature range, -55°C to +125°C by characterization with production testing at +25°C; over a total ionizing dose of 30krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL75054M30VZ); or over a total ionizing dose of 50krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL75054M50VZ). (Cont.)**

Parameter	Test Conditions	Temp.	Min	Typ[1]	Max	Unit
Dropout Voltage, V_{DO}	V_{IN} - V_{OUT} for V_{IN} = 3.3V; R_{SET} = 33kΩ; I_{OUT} = 1mA	-55°C	300	370	500	mV
		+25°C	300	370	500	mV
		+125°C	300	370	500	mV
		+25°C (Post Rad)	300	370	500	mV
	V_{IN} - V_{OUT} for V_{IN} = 3.3V; R_{SET} = 33kΩ; I_{OUT} = 500mA	-55°C	300	380	500	mV
		+25°C	300	380	500	mV
		+125°C	300	380	500	mV
		+25°C (Post Rad)	300	380	500	mV
	V_{IN} - V_{OUT} for V_{IN} = 3.3V; R_{SET} = 33kΩ; I_{OUT} = 1A	-55°C	300	387	500	mV
		+25°C	300	387	500	mV
		+125°C	300	387	500	mV
		+25°C (Post Rad)	300	387	500	mV
Programmable Current Limit	V_{IN} = 2.7V to 5.5V; R_{OCP} = 750Ω	-55 to +125°C	**0.15**	0.2	**0.25**	A
	V_{IN} = 2.7V to 5.5V; R_{OCP} = 150Ω	-55 to +125°C	**0.8**	1	**1.2**	A
Internal Current Limit	V_{IN} = 2.7V; V_{OUT} = 0V; OCP = 0V	-55 to +125°C	**1.2**	1.4	**1.6**	A
	V_{IN} = 30V; V_{OUT} = 0V; OCP = 0V; V_{IN} - V_{OUT} foldback limiting	-55 to +125°C	**0.1**	0.32	**0.8**	A
OCP Pin Current	V_{IN} = 2.7V; V_{OUT} = 0.9V; I_{OUT} = 100mA	-55 to +125°C	**140**	190	**250**	µA
	V_{IN} = 2.7V; V_{OUT} = 0.9V; I_{OUT} = 1A	-55 to +125°C	**1.5**	1.85	**2.5**	mA
	V_{IN} = 30V; V_{OUT} = 28.7V; I_{OUT} = 100mA	-55 to +125°C	**140**	193	**250**	µA
	V_{IN} = 30V; V_{OUT} = 28.7V; I_{OUT} = 1A	-55 to +125°C	**1.5**	1.87	**2.5**	mA
Start-Up Time	V_{IN} = 5V; R_{SET} = 33kΩ; C_{SET} = 100nF; I_{OUT} = 500mA; Fast Start-Up Disabled; V_{OUT} rise from 10% to 90%	-55 to +125°C	**6**	7.9	**11**	ms
	V_{IN} = 5V; R_{SET} = 33kΩ; C_{SET} = 0.47µF; I_{OUT} = 500mA; Fast Start-Up Disabled; V_{OUT} rise from 10% to 90%	-55 to +125°C	**32**	36	**48**	ms
	V_{IN} = 5V; R_{SET} = 33kΩ; C_{SET} = 4.7µF; I_{OUT} = 500mA; Fast Start-Up Disabled; V_{OUT} rise from 10% to 90%	-55 to +125°C	**320**	379	**480**	ms
	V_{IN} = 5V; R_{SET} = 33kΩ; C_{SET} = 4.7µF; I_{OUT} = 500mA; Fast Start-Up Enabled; V_{OUT} rise from 10% to 90%	-55 to +125°C	**4**	5.8	**9**	ms
Thermal Shutdown	Rising	-	-	165	-	°C
Thermal Shutdown Hysteresis	-	-	-	20	-	°C

Default test conditions unless otherwise specified: V_{IN} = V_{OUT} + 0.5V or 2.7V, whichever is greater unless otherwise noted. Maximum I_{OUT} is defined as 1A for V_{IN}-V_{OUT} <= 2.2V, 100mA for 2.2V < V_{IN}-V_{OUT} ≤ 15V, 60mA for 15V < V_{IN}-V_{OUT} ≤ 29.4V, 50mA for V_{IN}-V_{OUT} > 29.4V. Typical values are at T_J = +25°C. **Boldface limits apply across the operating temperature range, -55°C to +125°C by characterization with production testing at +25°C; over a total ionizing dose of 30krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL75054M30VZ); or over a total ionizing dose of 50krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL75054M50VZ). (Cont.)**

Parameter	Test Conditions	Temp.	Min	Typ[1]	Max	Unit
Noise						
Noise Spectral Density (V_{IN} = 5V; V_{OUT} = 3.3V)	V_{IN} = 5V; V_{OUT} = 3.3V; I_{OUT} = 1A; Frequency = 10Hz; C_{OUT} = 30µF; C_{SET} = 4.7µF	+25°C	-	350	-	nV/√Hz
	V_{IN} = 5V; V_{OUT} = 3.3V; I_{OUT} = 1A; Frequency = 100Hz; C_{OUT} = 30µF; C_{SET} = 4.7µF	+25°C	-	65	-	nV/√Hz
	V_{IN} = 5V; V_{OUT} = 3.3V; I_{OUT} = 1A; Frequency = 1kHz; C_{OUT} = 30µF; C_{SET} = 4.7µF	+25°C	-	22.5	-	nV/√Hz
	V_{IN} = 5V; V_{OUT} = 3.3V; I_{OUT} = 1A; Frequency = 10kHz; C_{OUT} = 30µF; C_{SET} = 4.7µF	+25°C	-	11.5	-	nV/√Hz
Output RMS Noise (V_{IN} = 5V; V_{OUT} = 3.3V)	V_{IN} = 5V; V_{OUT} = 3.3V; I_{OUT} = 1A; Frequency = 10Hz to 100kHz; C_{OUT} = 30µF; C_{SET} = 4.7µF	+25°C	-	3.9	-	$µV_{RMS}$
	V_{IN} = 5V; V_{OUT} = 3.3V; I_{OUT} = 1A; Frequency = 10Hz to 100kHz; C_{OUT} = 30µF; C_{SET} = 2.2µF	+25°C	-	4.3	-	$µV_{RMS}$
	V_{IN} = 5V; V_{OUT} = 3.3V; I_{OUT} = 1A; Frequency = 10Hz to 100kHz; C_{OUT} = 30µF; C_{SET} = 1µF	+25°C	-	5.4	-	$µV_{RMS}$
	V_{IN} = 5V; V_{OUT} = 3.3V; I_{OUT} = 1A; Frequency = 10Hz to 100kHz; C_{OUT} = 30µF; C_{SET} = 0.47µF	+25°C	-	7.4	-	$µV_{RMS}$
PSRR						
PSRR	V_{IN} - V_{OUT} = 2V; I_{OUT} = 1A; V_{RIPPLE} = 150mV_{P-P}; Frequency = 120Hz; C_{OUT} = 30µF; C_{SET} = 4.7µF	+25°C	-	103.6	-	dB
	V_{IN} - V_{OUT} = 2V; I_{OUT} = 1A; V_{RIPPLE} = 150mV_{P-P}; Frequency = 10kHz; C_{OUT} = 30µF; C_{SET} = 4.7µF	+25°C	-	71.1	-	dB
	V_{IN} - V_{OUT} = 2V; I_{OUT} = 1A; V_{RIPPLE} = 150mV_{P-P}; Frequency = 100kHz; C_{OUT} = 30µF; C_{SET} = 4.7µF	+25°C	-	39.1	-	dB
	V_{IN} - V_{OUT} = 2V; I_{OUT} = 1A; V_{RIPPLE} = 150mV_{P-P}; Frequency = 1MHz; C_{OUT} = 30µF; C_{SET} = 4.7µF	+25°C	-	28.4	-	dB
	V_{IN} - V_{OUT} = 2V; I_{OUT} = 1A; V_{RIPPLE} = 150mV_{P-P}; Frequency = 10MHz; C_{OUT} = 30µF; C_{SET} = 4.7µF	+25°C	-	27.1	-	dB
EN Input Pin						
EN Input Rising Threshold	V_{IN} = 6V	-55 to +125°C	**1.06**	1.14	**1.2**	V
EN Threshold Hysteresis	-	-55 to +125°C	-	0.14	**0.3**	V
EN Leakage	V_{IN} = 30V; EN = 30V	-55 to +125°C	-	0.2	-	µA
PG Output Pin						
PG Trip UV Rising	V_{IN} = 2.7V to 30V; V_{OUT} ≥ 0.9V	-55 to +125°C	**580**	605	**625**	mV
PG UV Hysteresis	V_{IN} = 2.7V to 30V; V_{OUT} ≥ 0.9V	-55 to +125°C	-	29	**90**	mV
PG Trip OV Rising	V_{IN} = 2.7V to 30V; V_{OUT} ≥ 0.9V	-55 to +125°C	**690**	725	**750**	mV
PG OV Hysteresis	V_{IN} = 2.7V to 30V; V_{OUT} ≥ 0.9V	-55 to +125°C	-	27	**90**	mV
PG Falling Delay; UV Warning	V_{IN} = 2.7V to 30V; V_{OUT} ≥ 0.9V; R_{PULLUP} = 100kΩ to 5V; Time from PGFB = 0.5V to PG falling	-55 to +125°C	**290**	329	**390**	ns

Default test conditions unless otherwise specified: V_{IN} = V_{OUT} + 0.5V or 2.7V, whichever is greater unless otherwise noted. Maximum I_{OUT} is defined as 1A for V_{IN}-V_{OUT} <= 2.2V, 100mA for 2.2V < V_{IN}-V_{OUT} ≤ 15V, 60mA for 15V < V_{IN}-V_{OUT} ≤ 29.4V, 50mA for V_{IN}-V_{OUT} > 29.4V. Typical values are at T_J = +25°C. **Boldface limits apply across the operating temperature range, -55°C to +125°C by characterization with production testing at +25°C; over a total ionizing dose of 30krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL75054M30VZ); or over a total ionizing dose of 50krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL75054M50VZ). (Cont.)**

Parameter	Test Conditions	Temp.	Min	Typ[1]	Max	Unit
PG Rising Delay; UV Recovery	V_{IN} = 2.7V to 30V; V_{OUT} ≥ 0.9V; R_{PULLUP} = 100kΩ to 5V; C_{PG} = 50pF; Time from PGFB = 0.65V to PG = 0.5V	-55 to +125°C	**0.7**	0.8	**0.9**	µs
PG Rising Delay; OV Recovery	V_{IN} = 2.7V to 30V; V_{OUT} ≥ 0.9V; R_{PULLUP} = 100kΩ to 5V; C_{PG} = 50pF; Time from PGFB = 0.65V to PG = 0.5V	-55 to +125°C	**0.65**	0.75	**0.9**	µs
PG Falling Delay; OV Warning	V_{IN} = 2.7V to 30V; V_{OUT} ≥ 0.9V; R_{PULLUP} = 100kΩ to 5V; Time from PGFB = 0.8V to PG falling	-55 to +125°C	**280**	338	**390**	ns
PG VOL	I_{PG} = 1mA; V_{IN} = 2.7V; V_{OUT} ≥ 0.9V	-55 to +125°C	-	196	**350**	mV
PG Leakage	V_{IN} = 30V; V_{PG} = 30V	-55 to +125°C	-	0.01	**1**	µA

1. Typical values are at 25°C and are not guaranteed.

4. Typical Performance Curves

V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} = 1A, C_{SET} = 4.7µF, C_{OUT} = 2x 15µF Tantalum + 2x 0.1µF Ceramic, T_A = 25°C unless otherwise stated. RMS noise for 10Hz to 100kHz bandwidth.

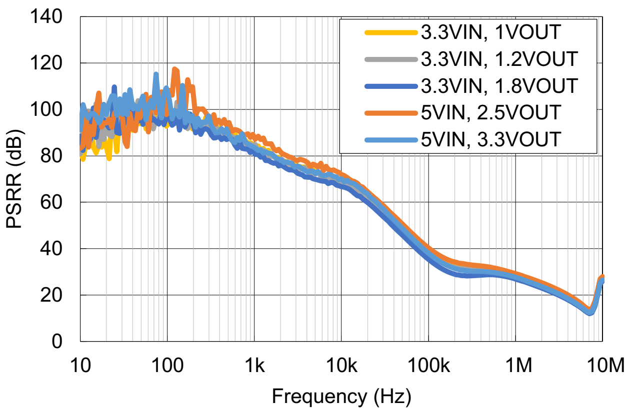


Figure 6. PSRR for Common V_{IN} to V_{OUT} Configurations

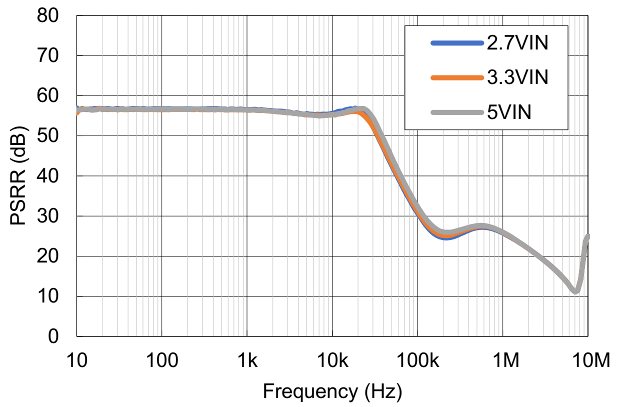


Figure 7. PSRR vs Input Voltage (V_{OUT} = V_{IN} - 0.8V)

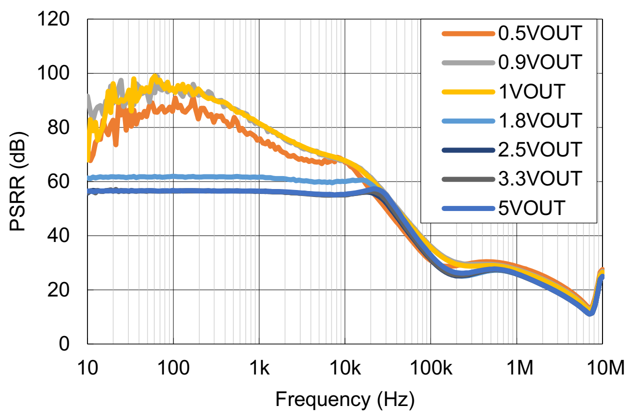


Figure 8. PSRR vs Output Voltage
(V_{IN} = V_{OUT} + 0.8V or 2.7V, whichever is greater)

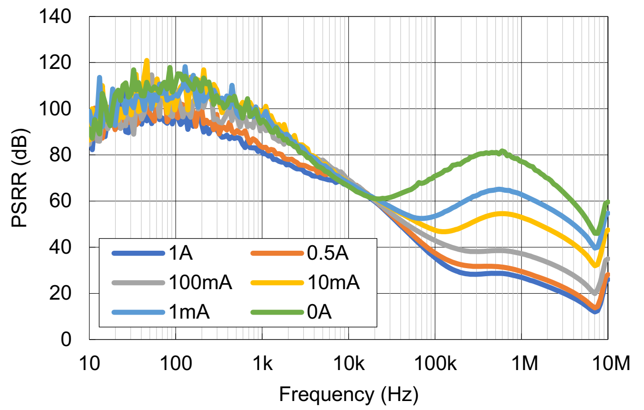


Figure 9. PSRR vs Output Current
(V_{IN} = 3.3V, V_{OUT} = 1.8V)

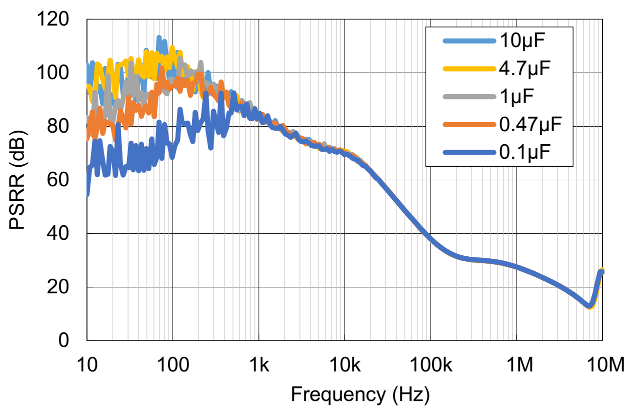


Figure 10. PSRR vs C_{SET}

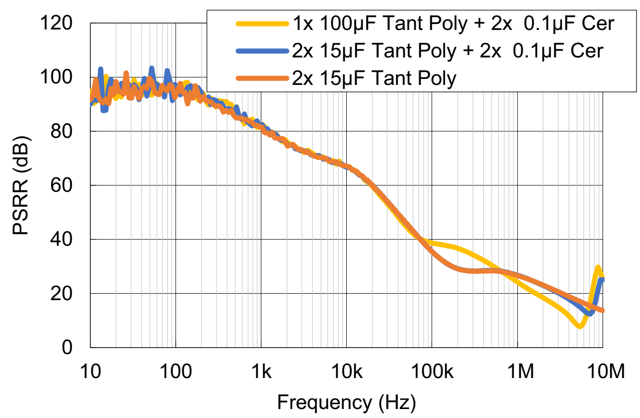


Figure 11. PSRR vs Output Capacitance
(V_{IN} = 3.3V, V_{OUT} = 1.8V)

V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} = 1A, C_{SET} = 4.7µF, C_{OUT} = 2x 15µF Tantalum + 2x 0.1µF Ceramic, T_A = 25°C unless otherwise stated. RMS noise for 10Hz to 100kHz bandwidth. (Cont.)

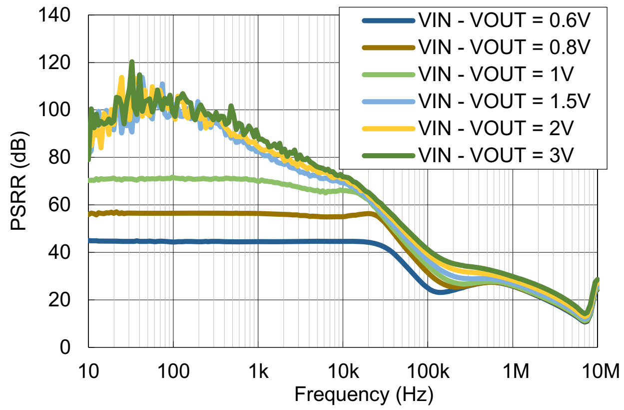


Figure 12. PSRR vs V_{IN} - V_{OUT}

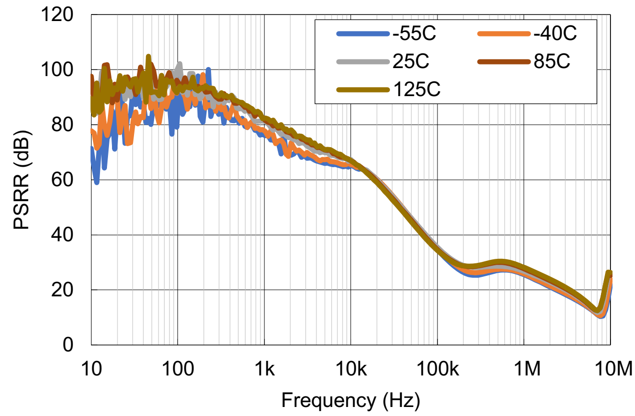


Figure 13. PSRR vs Temperature (V_{IN} = 3.3V, V_{OUT} = 1.8V)

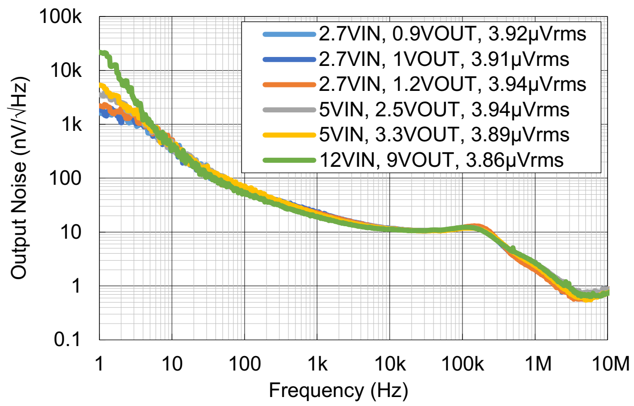


Figure 14. Output Noise for Common V_{IN} to V_{OUT} Configurations

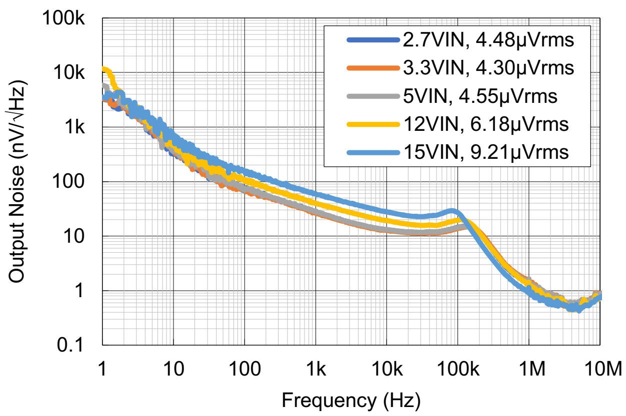


Figure 15. Output Noise vs Input Voltage (V_{OUT} = V_{IN} - 0.8V)

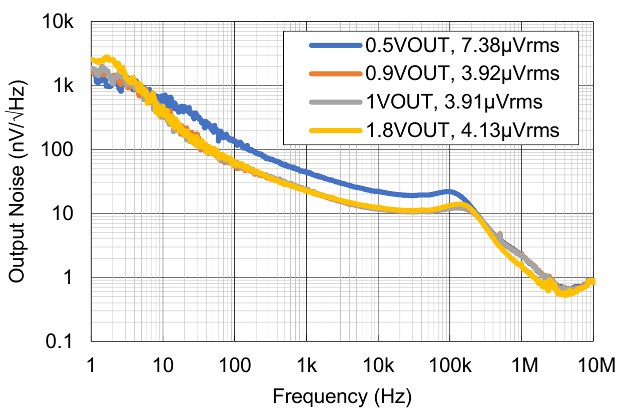


Figure 16. Output Noise vs Output Voltage (V_{IN} = 2.7V)

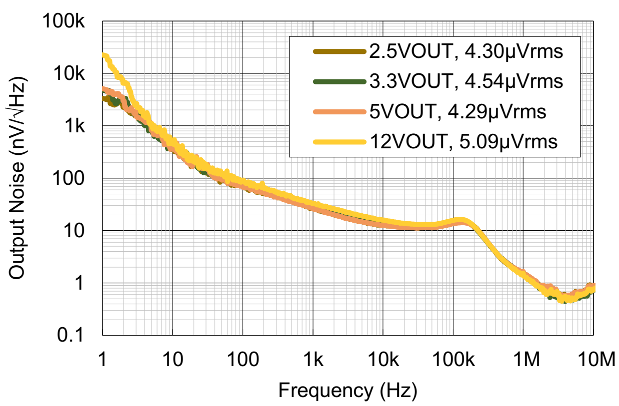


Figure 17. Output Noise vs Output Voltage (V_{IN} = V_{OUT} + 0.8V)

V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} = 1A, C_{SET} = 4.7µF, C_{OUT} = 2x 15µF Tantalum + 2x 0.1µF Ceramic, T_A = 25°C unless otherwise stated. RMS noise for 10Hz to 100kHz bandwidth. (Cont.)

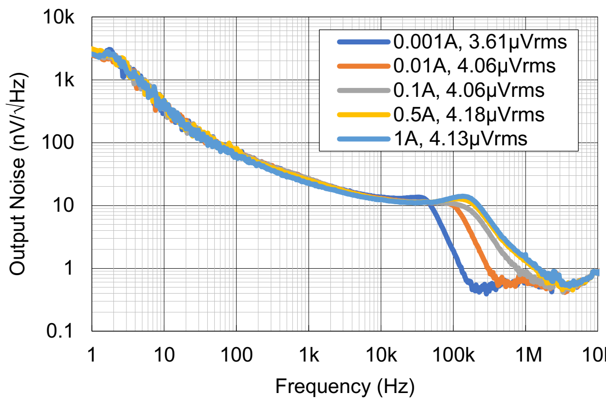


Figure 18. Output Noise vs Output Current (V_{IN} = 2.7V, V_{OUT} = 1.8V)

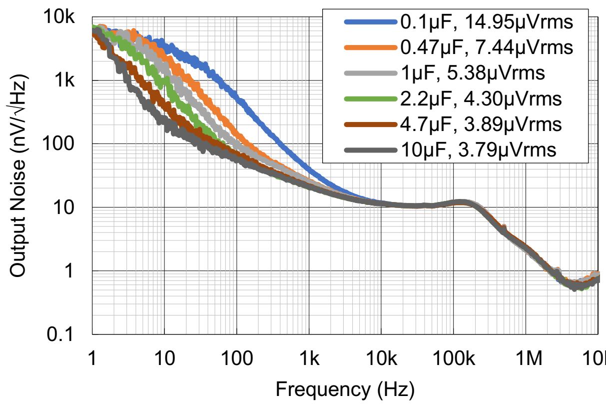


Figure 19. Output Noise vs C_{SET}

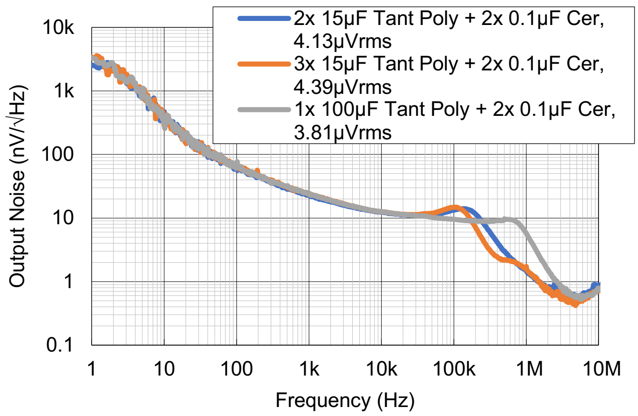


Figure 20. Output Noise vs Output Capacitance (2.7V, V_{OUT} = 1.8V)

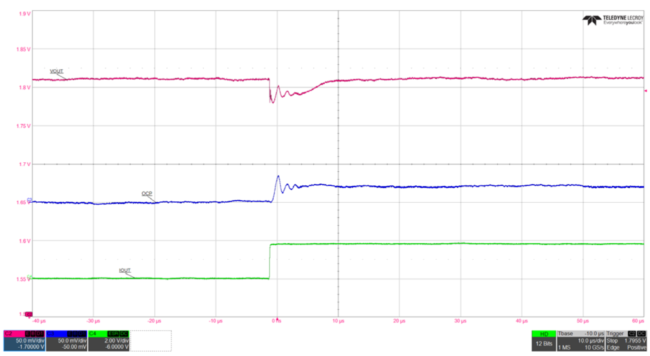


Figure 21. Load Transient (V_{OUT} = 1.8V, I_{OUT} = 1mA to 1A, V_{IN} = 3.3V, Slew Rate = 8A/µs, R_{OCP} = 10.5Ω)

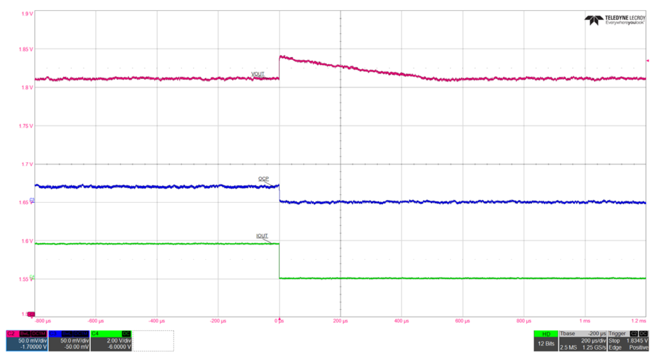


Figure 22. Load Transient (V_{OUT} = 1.8V, I_{OUT} = 1A to 1mA, V_{IN} = 3.3V, Slew Rate = 8.1A/µs, R_{OCP} = 10.5Ω)

V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} = 1A, C_{SET} = 4.7µF, C_{OUT} = 2x 15µF Tantalum + 2x 0.1µF Ceramic, T_A = 25°C unless otherwise stated. RMS noise for 10Hz to 100kHz bandwidth. (Cont.)

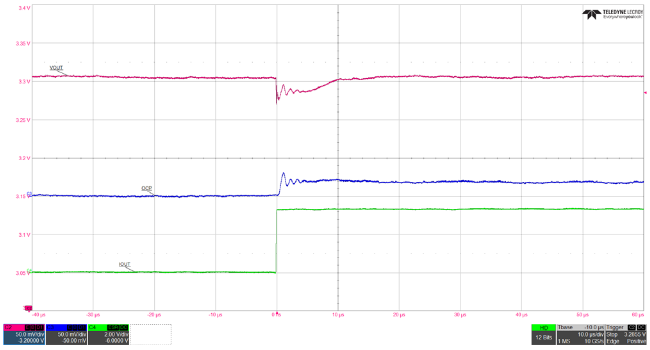


Figure 23. Load Transient (V_{OUT} = 3.3V, I_{OUT} = 1mA to 1A, V_{IN} = 5V, Slew Rate = 10.3A/µs, R_{OCP} = 10.5Ω)

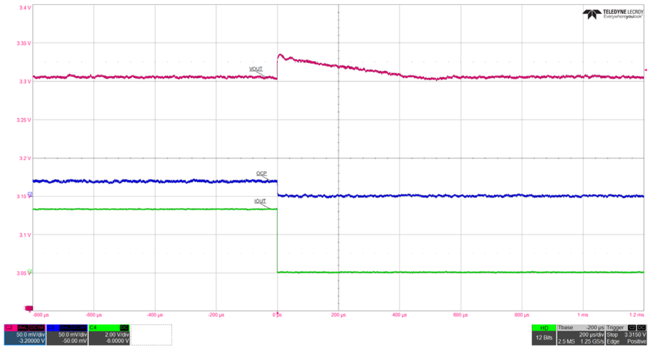


Figure 24. Load Transient (V_{OUT} = 3.3V, I_{OUT} = 1A to 1mA (V_{IN} = 5V, Slew Rate = 6.4A/µs, R_{OCP} = 10.5Ω)

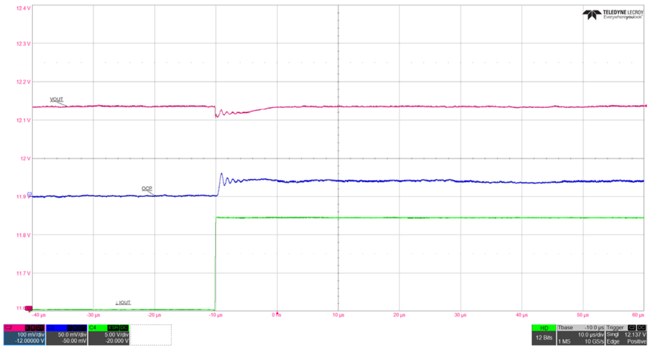


Figure 25. Load Transient (V_{OUT} = 12V, I_{OUT} = 1mA to 1A, V_{IN} = 15V, Slew Rate = 8.1A/µs, R_{OCP} = 10.5Ω)

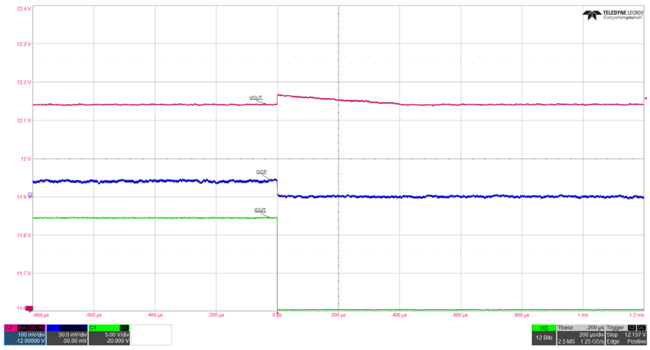


Figure 26. Load Transient (V_{OUT} = 12V, I_{OUT} = 1A to 1mA, V_{IN} = 15V, Slew Rate = 3.7A/µs, R_{OCP} = 10.5Ω)

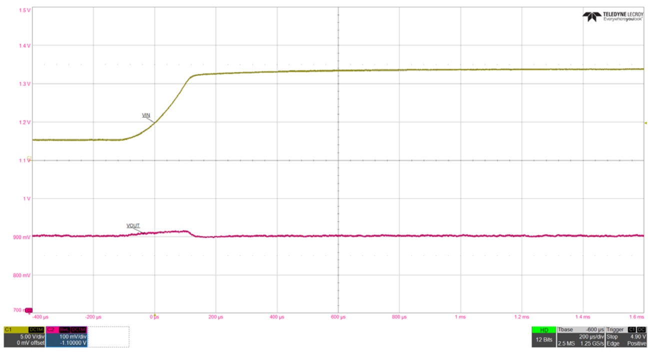


Figure 27. Line Transient (V_{OUT} = 0.9V, V_{IN} = 2.7V to 12V, I_{OUT} = 0A, Slew rate = 41.5V/ms)

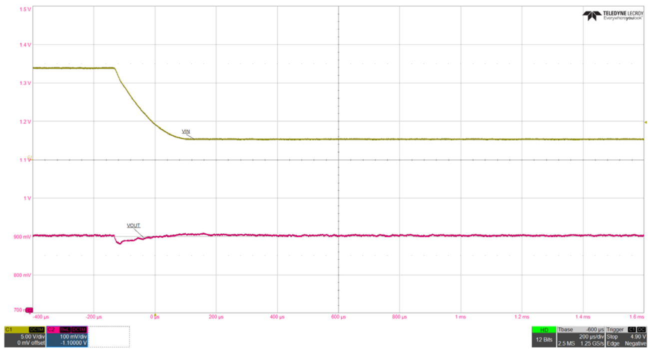


Figure 28. Line Transient (V_{OUT} = 0.9V, V_{IN} = 12V to 2.7V, I_{OUT} = 0A, Slew Rate = 46.5V/ms)

V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} = 1A, C_{SET} = 4.7μF, C_{OUT} = 2x 15μF Tantalum + 2x 0.1μF Ceramic, T_A = 25°C unless otherwise stated. RMS noise for 10Hz to 100kHz bandwidth. (Cont.)

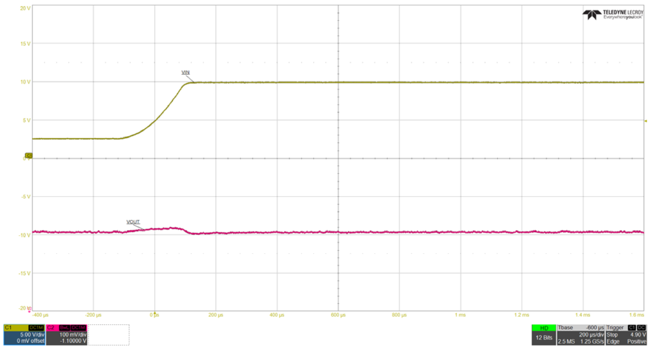


Figure 29. Line Transient (V_{OUT} = 0.9V, V_{IN} = 2.7V to 12V, I_{OUT} = 1A, Slew Rate = 36.5V/ms)

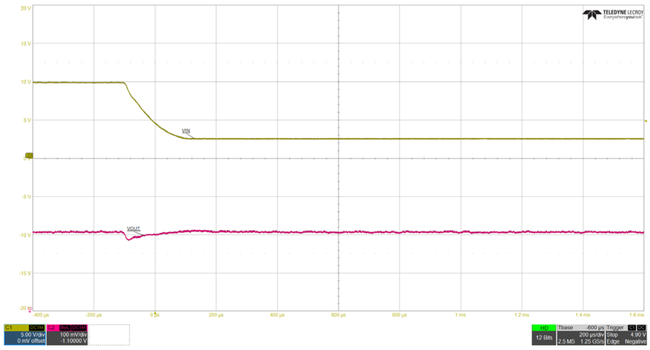


Figure 30. Line Transient (V_{OUT} = 0.9V, V_{IN} = 12V to 2.7V, I_{OUT} = 1A, Slew Rate = 36.5V/ms)

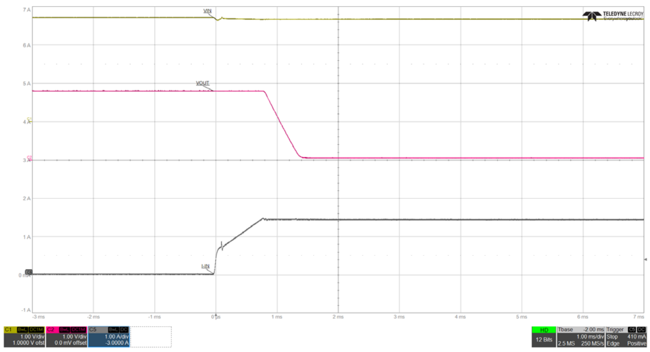


Figure 31. Current Limit Response (V_{IN} = 3.3V, V_{OUT} = 1.8V, I_{OUT} = 0A to 1.5A, R_{OCP} = 0Ω)

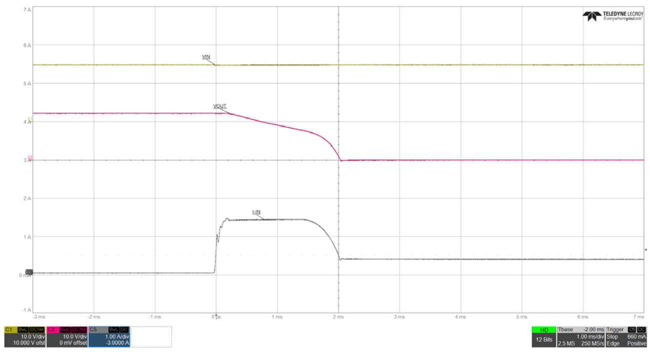


Figure 32. Current Limit Response (V_{IN} = 15V, V_{OUT} = 12, I_{OUT} = 0A to 1.5A, R_{OCP} = 0Ω)

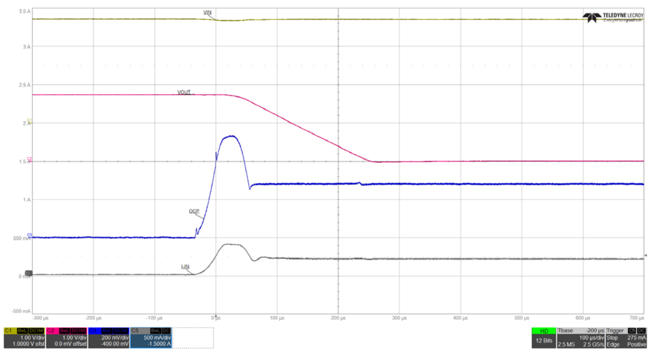


Figure 33. Current Limit Response (V_{OUT} = 1.8V, I_{OUT} = 0A to 1.5A, R_{OCP} = 750Ω

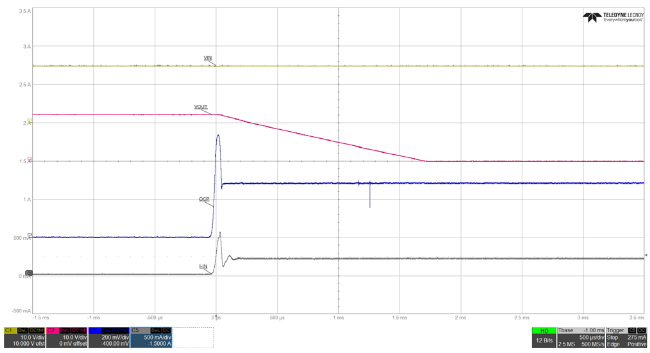


Figure 34. Current Limit Response (V_{OUT} = 12, I_{OUT} = 0A to 1.5A, R_{OCP} = 750Ω

V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} = 1A, C_{SET} = 4.7µF, C_{OUT} = 2x 15µF Tantalum + 2x 0.1µF Ceramic, T_A = 25°C unless otherwise stated. RMS noise for 10Hz to 100kHz bandwidth. (Cont.)

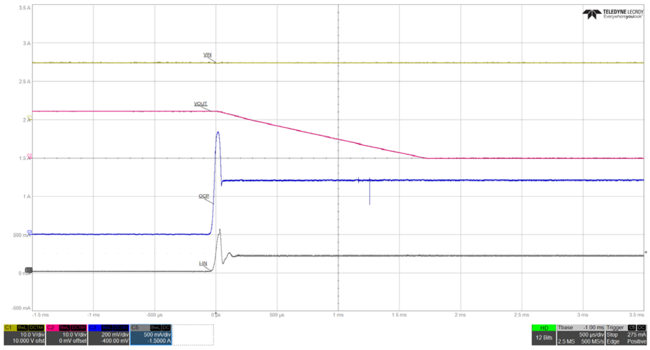


Figure 35. Foldback Current Limit Response (V_{IN} = 20V, V_{OUT} = 1.8V, I_{OUT} = 0A to 1.5A, R_{OCP} = 0Ω)

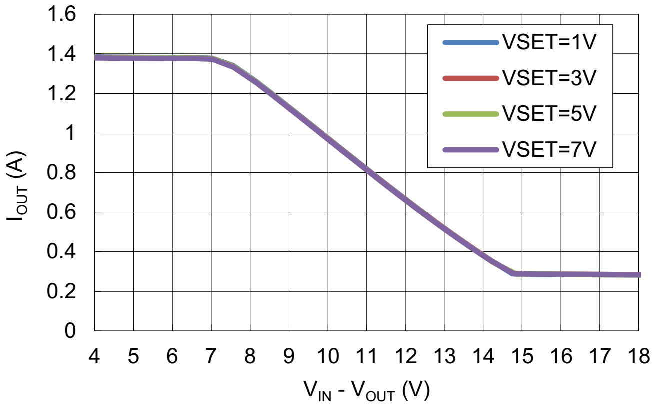


Figure 36. Foldback Current Limit (I_{OUT} vs V_{IN}-V_{OUT}, V_{OUT} = 0.9V)

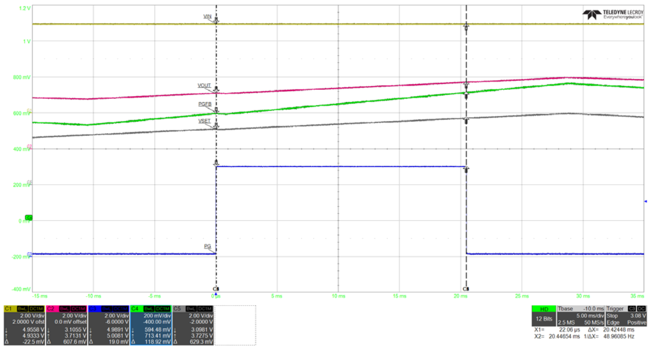


Figure 37. OV Warning/UV Recovery (PGFB Rising, I_{OUT} = 0A)

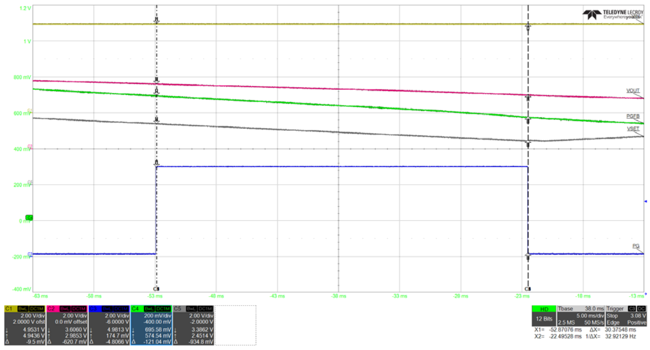


Figure 38. OV Recovery/UV Warning (PGFB Falling, I_{OUT} = 0A)

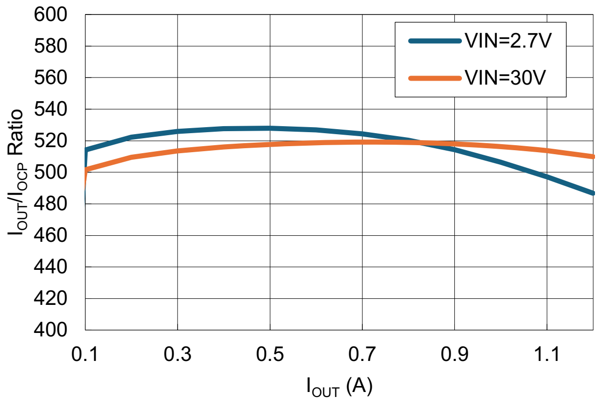


Figure 39. OCP Current Ratio (I_{OUT}/I_{OCP}Ratio vs I_{OUT}, V_{OUT} = V_{IN} - 0.5V)

V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} = 1A, C_{SET} = 4.7µF, C_{OUT} = 2x 15µF Tantalum + 2x 0.1µF Ceramic, T_A = 25°C unless otherwise stated. RMS noise for 10Hz to 100kHz bandwidth. (Cont.)

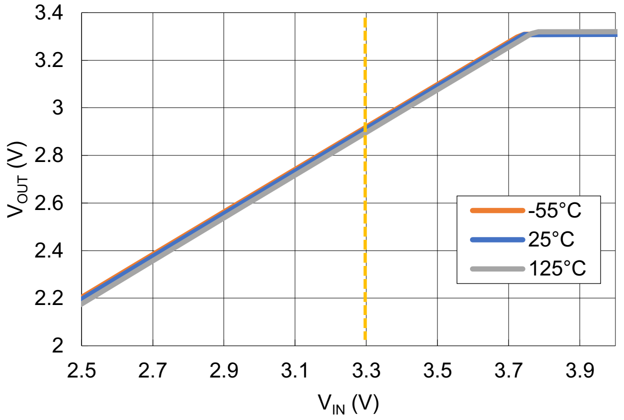


Figure 40. Dropout (I_{OUT} = 1A, R_{SET} = 33.2kΩ)

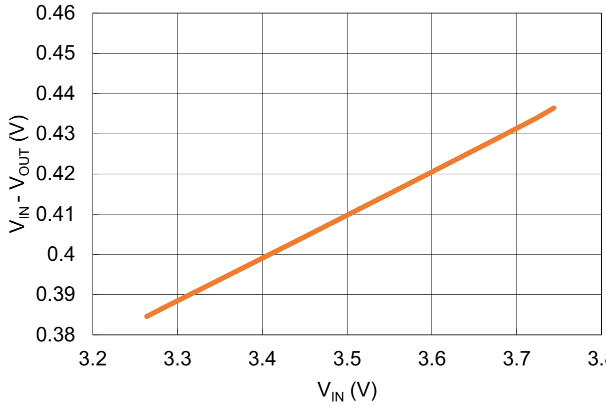


Figure 41. Dropout Variation vs V_{IN} (I_{OUT} = 1A, R_{SET} = 33.2kΩ)

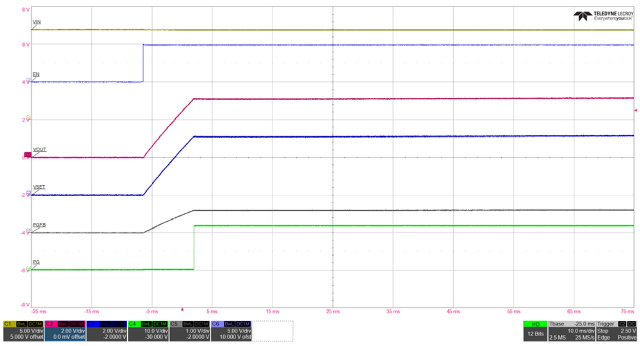


Figure 42. Startup by EN (V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 1A, C_{SET} = 4.7µF, Fast Start Enabled)

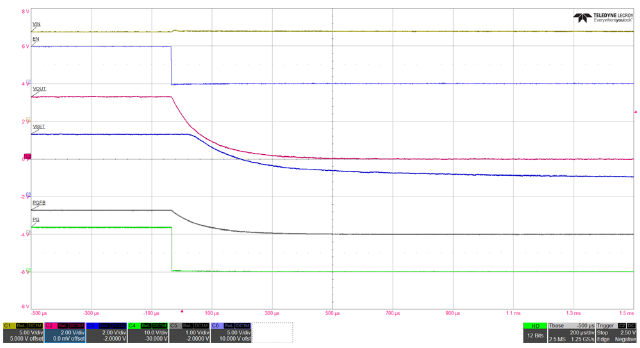


Figure 43. Shutdown by EN (V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 1A, C_{SET} = 4.7µF, Fast Start Enabled)

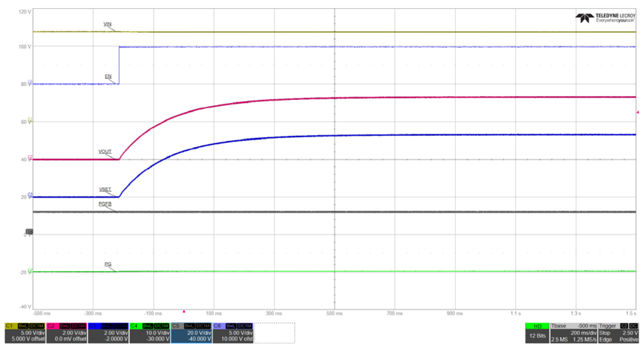


Figure 44. Startup by EN (V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 1A, C_{SET} = 4.7µF, Fast Start Disabled)

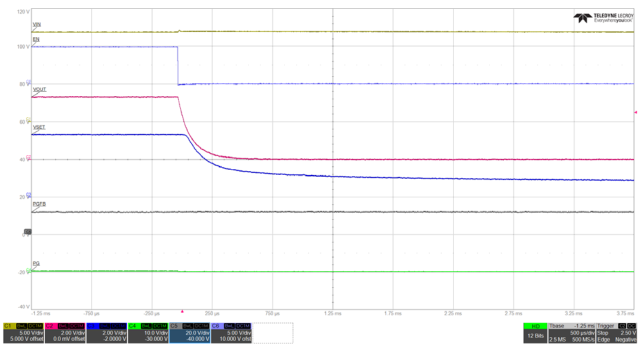


Figure 45. Shutdown by EN (V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 1A, C_{SET} = 4.7µF, Fast Start Disabled)

V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} = 1A, C_{SET} = 4.7µF, C_{OUT} = 2x 15µF Tantalum + 2x 0.1µF Ceramic, T_A = 25°C unless otherwise stated. RMS noise for 10Hz to 100kHz bandwidth. (Cont.)

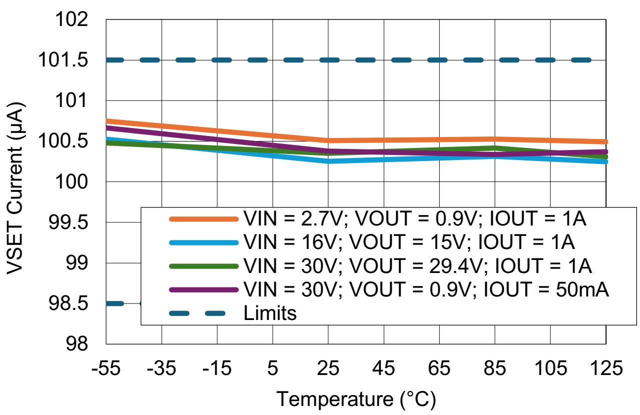


Figure 46. VSET Current, V_{OUT} = 0.9V to V_{IN}-V_{DO}

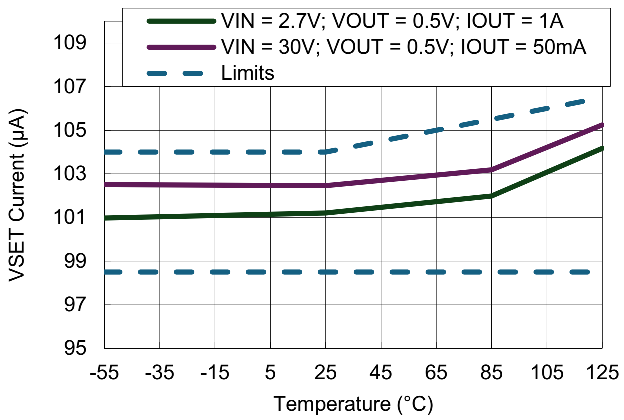


Figure 47. VSET Current, V_{OUT} = 0.5V

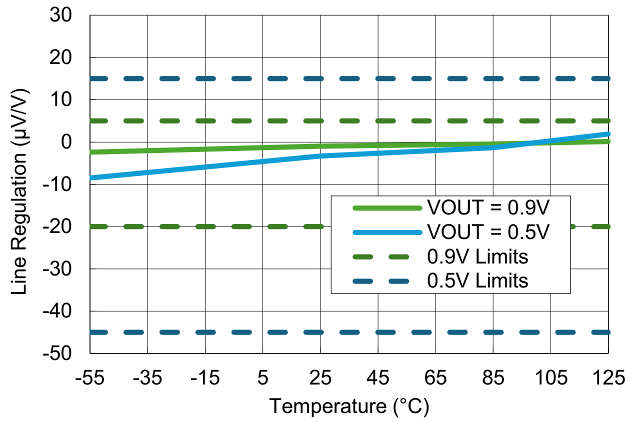


Figure 48. Line Regulation, $\Delta V_{OS}/\Delta V_{IN}$

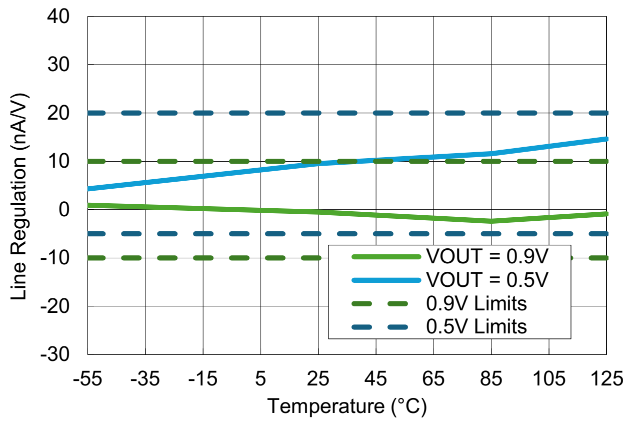


Figure 49. Line Regulation, $\Delta I_{SET}/\Delta V_{IN}$

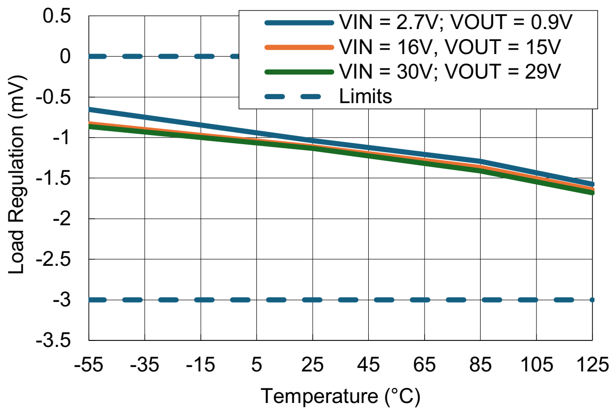


Figure 50. Load Regulation, ΔV_{OUT}

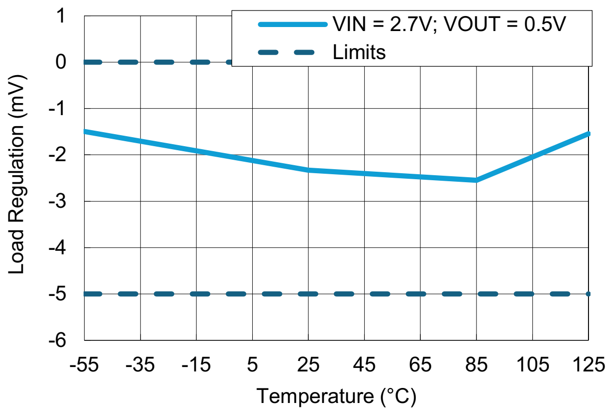


Figure 51. Load Regulation, ΔV_{OUT}, V_{OUT} = 0.5V

V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} = 1A, C_{SET} = 4.7µF, C_{OUT} = 2x 15µF Tantalum + 2x 0.1µF Ceramic, T_A = 25°C unless otherwise stated. RMS noise for 10Hz to 100kHz bandwidth. (Cont.)

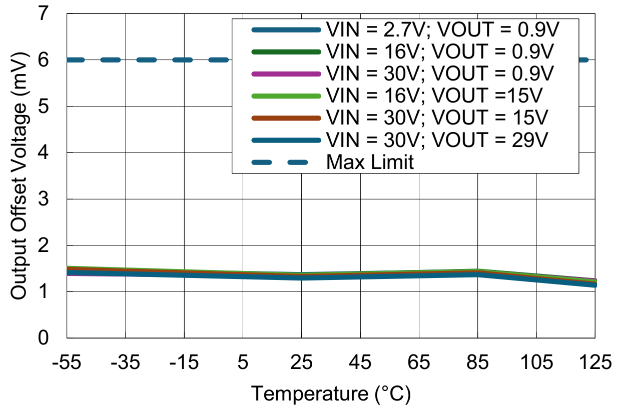


Figure 52. Output Offset Voltage, No Load

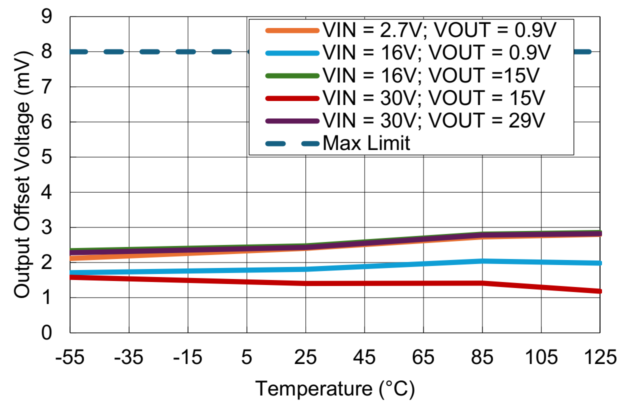


Figure 53. Output Offset Voltage, Max I_{OUT}

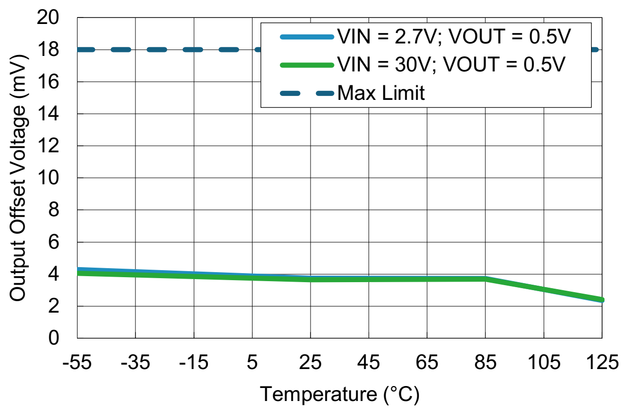


Figure 54. Output Offset Voltage, 0.5V, No Load

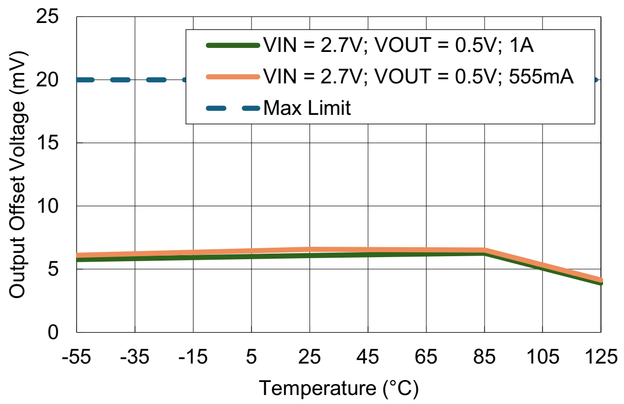


Figure 55. Output Offset Voltage 0.5V

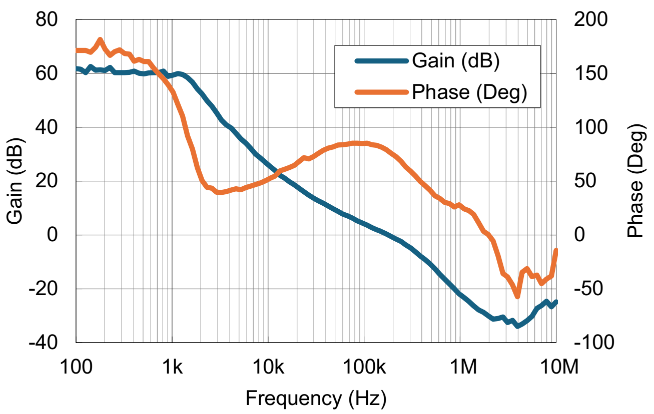


Figure 56. Bode Plot (I_{OUT} = 30mA, C_{OUT} = 1× 33µF Tantalum + 2× 0.1µF Ceramic)

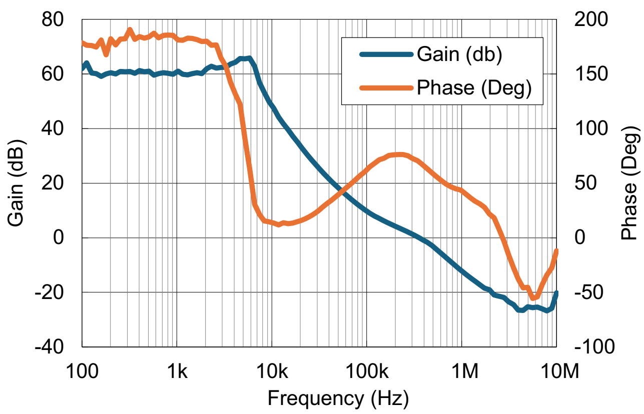


Figure 57. Bode Plot (I_{OUT} = 1A, C_{OUT} = 1×33µF Tantalum + 2× 0.1µF Ceramic)

5. Functional Description

5.1 Overview

The ISL75054M is a radiation tolerant low dropout linear regulator with ultra-low noise, and high PSRR for use in ADC, RF, and other noise sensitive applications. The linear regulator has an operating supply voltage range of 2.7V to 30V and an output voltage range of 0.5V to V_{IN} - V_{DO}. The ISL75054M features excellent noise performance and PSRR for radiation tolerant LDOs, with ultra-low RMS noise of 3.9µV_{RMS} from 10Hz to 100kHz and ultra-high PSRR of 103.6dB at 120Hz. Additionally, excellent regulation over line, load, temperature, and radiation is made possible through a precision current source and high performance voltage buffer. Built-in protections includes V_{IN} - V_{OUT} foldback current limiting, externally programmable current limit, and over-temperature protection. Additional features include enable functionality, fast start-up capability, soft-start control, and power-good. The ISL75054M is designed to draw a small quiescent current (typically 1.7mA for 2.7V input) and features a small footprint with minimal external components required.

5.2 Precision Current Reference Architecture

A 100µA precision current reference is sourced out of VSET, which is tied to the non-inverting input of a high performance unity gain voltage buffer used as the error amplifier. This current flows through a resistor between VSET and GND, resulting in a voltage generated on VSET equal to the product of the resistance and current. Through this configuration, regardless of programmed output voltage, the error amplifier always operates with unity gain. In a traditional LDO, a resistor divider scales down V_{OUT} to be compared with an internal voltage reference to set the output regulation voltage. This amplifies the regulator noise and degrades frequency response and PSRR. In the precision current reference architecture, this is no longer the case, meaning noise, PSRR, and frequency response are no longer dependent on output voltage as in traditional voltage reference LDOs where the inverting input to the error amplifier is a resistor divided version of V_{OUT}. The rail-to-rail error amplifier and current reference allow for a wide output voltage range from 0.5V to V_{IN}-V_{DO}.

5.3 Power-Good and Fast Start-Up

The PG pin is an open-drain output that asserts when PGFB is within a specified voltage range. VOUT is scaled down and sensed through a resistor divider from VOUT to PGFB. PG goes low when the voltage on PGFB falls below a typical value of 576mV or rises above a typical value of 725mV, providing both overvoltage and undervoltage monitoring. Refer to the Electrical Specifications table for PGFB rising and falling threshold specifications.

PGFB is also used to enable fast start-up operation. When voltage on PGFB is less than 605mV, fast start-up is enabled. While in fast start-up mode, a 2mA current source is connected to the VSET pin, in addition to the 100µA current source. The higher current source increases the charge rate of the external capacitor on VSET, decreasing start-up time.

PG and fast startup are independent functions. For output voltages below 0.7V, fast start-up is not possible and power-good functionality is always disabled.

5.4 Low Noise, High PSRR Performance

Output noise is the measure of intrinsic noise that the linear regulator generates internally. Typical sources of noise in linear regulators include the voltage reference, error amplifier, and the feedback resistor divider network used for output voltage sensing. The ISL75054M achieves excellent noise performance by eliminating the voltage reference and feedback resistor network. These circuits are replaced with a 100µA precision current reference and resistor tied from VSET to GND to set the output voltage. Output voltage is sensed directly from VOUT by the VOUTS pin, which is tied to the error amplifier inverting input. Total noise is therefore a product of the current source noise, R_{SET}, and error amplifier.

PSRR is the measure of how much attenuation a linear regulator provides to extrinsic noise from supply input to output. Two circuits are responsible for total PSRR on the ISL75054M; the error amplifier and the precision current source. The precision current source uses a capacitor across the resistor from VSET to GND to provide a low impedance and reject variations in the reference voltage due to input variation. Larger C_{SET} values improve PSRR and transient performance at the cost of increased start-up time. The error amplifier provides maximum PSRR by operating in unity gain configuration rather than using some of the gain with a feedback resistor divider. Additional PCB layout techniques are used to prevent magnetic fields from AC currents coupling through from the input to the output. Refer to Layout Guidelines for more details.

6. Applications Information

6.1 Input Capacitance and Stability

The ISL75054M requires a minimum of 30µF capacitance on VIN for stability and to prevent input supply droop. Additionally, ESR should be kept below 200mΩ to reduce input supply droop during transients.

6.2 Output Capacitance and Stability

To ensure stable operation, select a suitable output capacitance and equivalent series resistance (ESR) combination. Renesas recommends using an output capacitance of 30µF or greater and ESR in the range of 20mΩ to 50mΩ to maintain greater than 60° of phase margin across load. A single 33µF Tantalum capacitor is suitable. Typically, low ESR, ceramic capacitors alone, are not sufficient to compensate the LDO. If the ESR is too low, a resistor can be added between the output and ceramic output capacitor to intentionally increase the ESR. When selecting this resistor size, ensure that it can handle the AC currents expected on the output. Ceramic capacitors of 0.1µF or lower can be placed near the point of load for high frequency filtering and should not be considered in the above recommendation for total output capacitance and ESR. Figure 58 shows the stable operating region across load current, capacitance, and ESR at 25°C. Validate stability through Bode plot and load transient analysis in the end application.

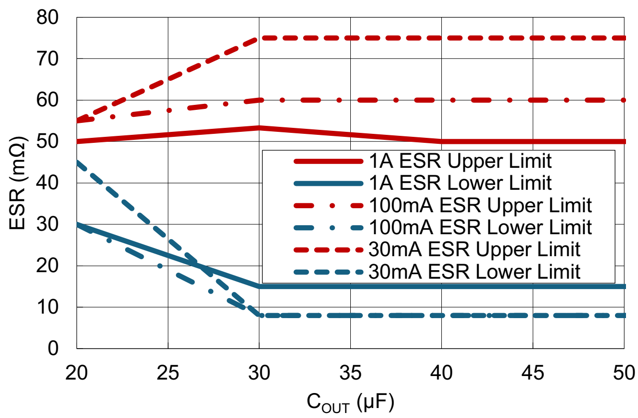


Figure 58. Recommended COUT and ESR Range for >60° Phase Margin

Bode plots in Figure 56 and Figure 57 were generated using a single 33µF Tantalum output capacitor. Use capacitor datasheets or vendor-provided simulation tools to determine the effective ESR near the expected gain crossover frequency. When selecting ceramic output capacitors, consider capacitance derating at the expected output voltage.

6.3 Input UVLO and Enable Threshold

The EN pin enables and disables the ISL75054M. Adjustable input UVLO can be implemented through a resistor divider from VIN to EN. When the EN voltage is below the EN Input Threshold, the device is in Shutdown mode. In this mode the output is disabled and the device draws minimal input current. When EN voltage is above the typical

EN Input Threshold of 1.14V, the device is enabled and the output is active. Use Equation 1 to calculate the UVLO threshold based on the upper enable resistor, R_{EN1}, and lower enable resistor, R_{EN2}.

(EQ. 1) $$V_{EN} = \frac{(EN_{Rising\ Threshold}) \times (R_{EN1} + R_{EN2})}{R_{EN2}}$$

In addition to the EN pin, VIN features a UVLO of 2.7V typical. This restricts device operation to input voltages above 2.7V.

6.4 Output Voltage

Output voltage is set through a 100µA (typical) precision current source flowing out of VSET, which is tied to the error amplifier non-inverting input. A resistor, R_{SET}, connected from VSET to GND generates a voltage reference to the error amplifier as shown in Figure 59.

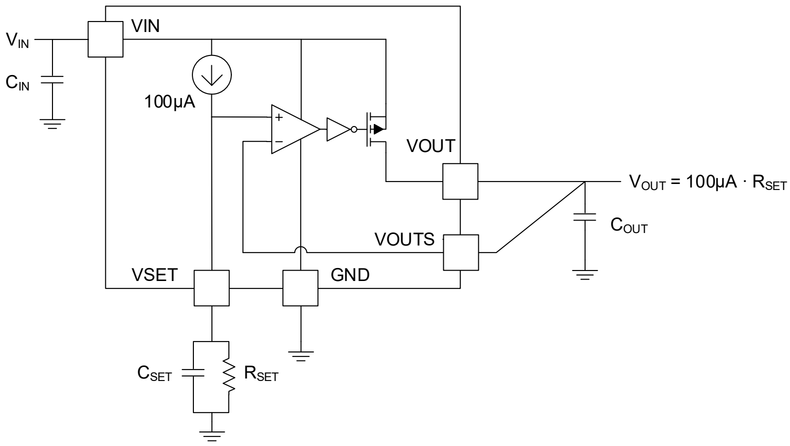


Figure 59. Functional Block for Output Regulation

The reference voltage on the VSET pin is used to set the output voltage. The voltage generated on this pin is a product of the 100µA precision current source and the R_{SET} value. Use Equation 2 to find the exact R_{SET} value for the required V_{OUT}, where I_{SET} = 100µA.

(EQ. 2) $$R_{SET} = \frac{V_{OUT}}{I_{SET}}$$

A 0.1% or better resistor is recommended for R_{SET}. Overall accuracy is a product of the error amplifier (EA) offset, error in the 100µA current source, and R_{SET} resistor accuracy; therefore, minimizing resistor error is important to ensure highest accuracy performance.

Table 1 shows common output voltages and their corresponding resistor values.

Table 1. R_{SET} Values for Common Output Voltages

VOUT	0.1% Resistor for R_{SET}
0.5V	4.99kΩ
0.9V	9.09kΩ
1V	10.0kΩ
1.2V	12.0kΩ
1.5V	15.0kΩ
2.5V	24.9kΩ
3.3V	33.2kΩ

Table 1. R_{SET} Values for Common Output Voltages (Cont.)

VOUT	0.1% Resistor for R_{SET}
5V	49.9kΩ
12V	120.0kΩ
15V	150.0kΩ
18V	180.0kΩ
24V	240.0kΩ

6.4.1 Output Voltage Set by External Voltage Source

The VSET pin can be driven using an external voltage source, under the condition that the external source is capable of sinking 100µA of current during operation (and 2.1mA if power-good and fast start functionality is required). If a precision voltage source is connected to VSET, errors in VOUT from the reference current and R_{SET} tolerances can be eliminated but are replaced by the errors in the voltage source.

IMPORTANT: VOUT directly follows VEXT, so there is no soft start. If soft start is required, an RC filter between VEXT and VSET is recommended.

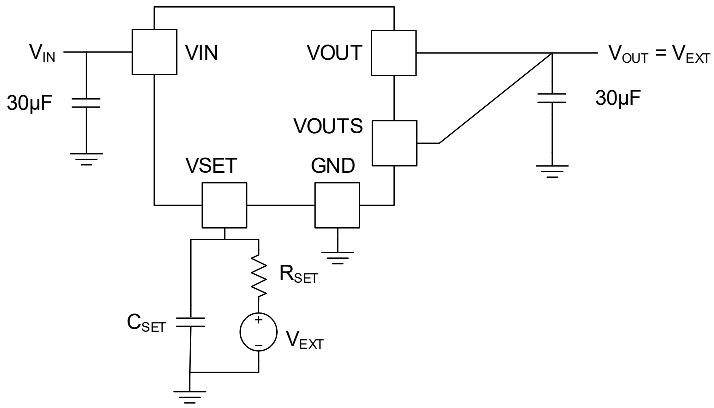


Figure 60. Simplified Schematic for Externally Set Output Voltage

6.5 VSET Capacitance: Noise and Soft-Start

A capacitor, C_{SET}, from VSET to GND has the dual function of both reducing output noise and setting the soft-start time. Renesas recommends using a C_{SET} capacitor between 0.47µF and 10µF. A larger C_{SET} capacitor results in lower noise. However, because of the RC time constant from the C_{SET} capacitor and the R_{SET} resistor, a larger C_{SET} results in a longer start-up time. Refer to Figure 6 through Figure 20 in the Typical Performance Curves to view the measured impact of C_{SET} on PSRR and Output Noise.

Soft start is addressed through fast start-up circuitry that increases the current on the VSET by activating a 2mA current source in addition to the 100µA current source until the voltage on PGFB is >605mV. Renesas recommends selecting the PGFB divider so that the PG UV Rising Threshold is reached when VOUT reaches 90% of the nominal output voltage. After the 2mA current source is disabled, the 100µA current reference sets the final output voltage regulation point on VSET.

When fast start-up circuitry is active, the start-up time can be approximated by a linear relationship between I_{SET} and C_{SET}. The start-up time for VOUT rising to the target output voltage set by the PGFB divider can be estimated by Equation 3:

(EQ. 3)
$$t_{fast-start} = \frac{C_{SET}}{I_{SET}} \times \text{PG UV Rising} \times \frac{R_{PGFB1} + R_{PGFB2}}{R_{PGFB2}}$$

Refer to Power-Good and Fast Start-Up for more information.

When fast start is disabled, start-up time is dependent on the time constant formed by R_{SET} and C_{SET}. Time to start-up to 90% of the target output voltage can be calculated by Equation 4 when Fast Start is disabled.

(EQ. 4) $$t_{startup} = R_{SET} \times C_{SET} \times (\ln[R_{SET} \times I_{SET}] - \ln[R_{SET} \times I_{SET} - (0.9 \times R_{SET} \times I_{SET})])$$

6.6 Power-Good, PGFB, and Fast Start

Power-good and fast start-up functionality are configured through a resistor divider between VOUT, PGFB, and GND. Renesas recommends selecting the PGFB divider for a voltage of 665mV, or approximately halfway between the UV and OV thresholds. However, because there is a range for which the PG circuitry considers good, the output voltage where PG is asserted can be adjusted depending on the resistor values chosen. See the Electrical Specifications table for more information on PGFB thresholds.

The PG pin is an open-drain output and requires a pull-up resistor to VIN. Renesas recommends selecting the pull-up resistor so that 1mA current (nominally) flows into PG when the part is in operation and PG is held low. Larger resistor values result in increased SEE sensitivity. Additionally, Renesas recommends placing a 470nF cap between PGFB and VOUT and a 150nF cap from PG to GND for further SEE mitigation.

Internally, PGFB is connected to a pair of comparators to allow for both overvoltage (OV) and undervoltage (UV) detection to be indicated on PG. The voltage on PGFB is referenced against 576mV for the UV comparator and 725mV for the OV comparator.

Additionally, the outputs of both of the UV and OV comparators are connected to an OR gate which drives the gate of the PG pin NMOS pull-down device. When the voltage on the PGFB pin is between 576mV and 725mV, the OR gate outputs a logic LOW signal, forcing the PG pin to be pulled HIGH through the external pull-up resistor. When the voltage on the PGFB pin is either above 725mV or below 576mV, the OR gate outputs a logic HIGH signal. The logic HIGH signal turns on the FET, pulling the PG pin low and indicating a UV or OV condition.

PGFB can also control fast start-up. When the voltage on PGFB is below 605mV, the comparator outputs a logic HIGH signal, enabling the fast start current source. When the voltage on PGFB is above 605mV, the comparator outputs a logic LOW signal, disabling the fast start current source. A switch connects a 2mA current source to the VSET pin, allowing the output voltage to quickly rise when the voltage on PGFB is below 605mV. This is useful for applications where a large VSET capacitor (C_{SET}) is required. Startup time is significantly reduced because the VSET capacitor is being charged with a 2mA current in addition to the 100µA current until the LDO output reaches the threshold set by the PGFB resistor divider, which is recommended to be 90% of the target VOUT.

If power-good and fast start-up are not used, tie the PGFB pin directly to VIN and float PG, as shown in Figure 61**.**

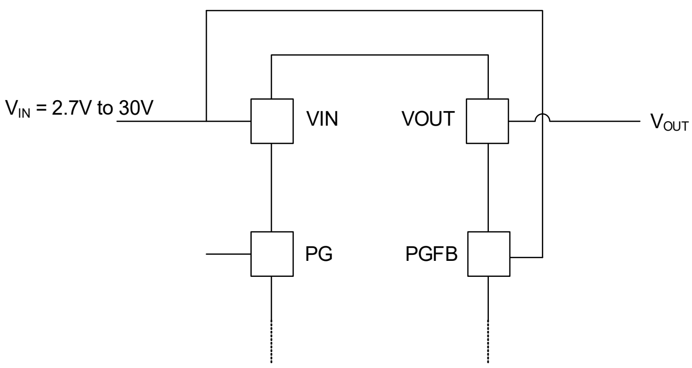


Figure 61. Simplified Schematic for PG and Fast Start-up Disabled

6.7 Overcurrent Protection

The ISL75054M features both externally programmable and internally set overcurrent protection that can be configured through the OCP pin. The external overcurrent limit is resistor programmable through a resistor, R_{OCP}, connected from OCP to GND. When the external current limit is not used, connect the OCP pin to GND. In this configuration, the internal current limit of 1.4A (typical) is active. Both internal and external OCP use a brick-wall current limit.

The current limit has a 150A×Ω scaling factor, so the value for R_{OCP} can be calculated based on the required current limit using Equation 5.

(EQ. 5) $$R_{OCP} = \frac{150A \times \Omega}{I_{OUT(Limit)}}$$

For example, with an R_{OCP} of 150Ω, the maximum output current is limited to 1A (typical). With an R_{OCP} of 750Ω, the maximum output current is limited to 200mA (typical).

Additionally, the ISL75054M features internal V_{IN}-V_{OUT} foldback current limiting. When V_{IN}-V_{OUT} is less than 7V, foldback current limiting is not active. As V_{IN}-V_{OUT} increases, the foldback current limit decreases. Refer to Figure 35 in the Typical Performance Curves section. The current limit for the ISL75054M is the lowest of the three current limits: programmed current limit, internal current limit, or foldback current limit.

Output current monitoring can also be implemented using the OCP pin. The OCP pin sources a current, I_{OCP}, that is approximately 1/530 of the output current. The relationship between output current, I_{OUT}, and I_{OCP} is shown in Equation 6.

(EQ. 6) $$I_{OCP} = \frac{I_{OUT}}{530}$$

Figure 39 in the Typical Application Curves shows the relationship between output current and the ratio between I_{OUT}/I_{OCP}.

6.8 Over-Temperature Protection

The ISL75054M features integrated thermal protection. When the internal temperature reaches 165°C (typical), the LDO output is disabled. After the internal temperature falls below 145°C (typical), the device resumes normal operation.

To determine the expected temperature rise of the device, first calculate power dissipation using Equation 7.

(EQ. 7) $$P_{DISS} = (VIN - VOUT) \times IOUT$$

Using the power dissipation, maximum expected ambient temperature, and maximum junction temperature calculate the required thermal impedance to meet the worst case operating conditions.

(EQ. 8) $$\theta_{JAmax} = \frac{(T_{Jmax} - T_{Amax})}{P_{DISS}}$$

To avoid thermal shutdown, ensure the specified θ_{JA} is less than the calculated θ_{JAmax}. The θ_{JA} value used must take into account copper area, airflow, and use of heatsinks in a given system.

7. PCB Layout

7.1 Layout Guidelines

PCB layout is critical for optimizing low noise, high PSRR LDO performance. See Figure 62 and Figure 63 for a recommended layout.

To maximize PSRR, careful consideration should be used on the placement of the input caps and routing of the VIN plane to avoid coupling signals from the input to the output. AC voltages on the input create AC currents (and magnetic fields) with the low impedance provided by the input capacitors. These magnetic fields impress themselves on other nearby loops the way two windings of a transformer transfer signals to each other. Magnetic coupling requires a consideration of distance, shielding, and loop orientation when designing a board. In the following layout example, the input plane (top layer) is routed directly above the return GND plane (layer 2). By routing these traces directly overlapping, EMF generated by AC voltages flows in opposite directions and is minimized. The GND return from the input caps should not tie directly to the larger GND plane at the device, but instead tie to the GND plane at the input supply GND terminal.

VOUTS and the connection to the upper resistor of the PGFB divider should be Kelvin connected to the required regulation point at the point of load.

Avoid routing sensitive signals such as VOUTS and VSET near noise generating sources to prevent unwanted noise coupling to the output of the LDO.

Tie the exposed thermal pad to a large GND plane to maximize dissipation of heat generated by the IC.

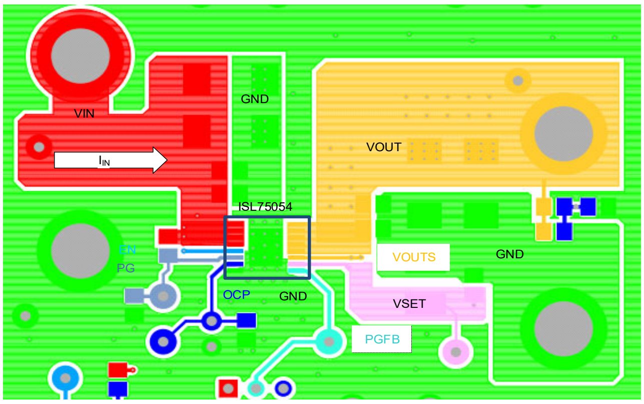


Figure 62. Recommended Layout: Top Layer

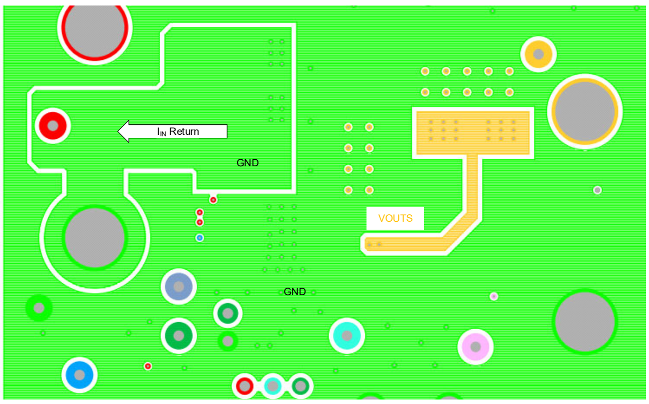


Figure 63. Recommended Layout: Layer 2

8. Radiation Tolerance

The ISL75054M is a radiation tolerant device for commercial space applications, Low Earth Orbits (LEO) applications, high altitude avionics, launch vehicles, and other harsh environments. This device's response to Total Ionizing Dose (TID) radiation effects and Single Event Effects (SEE) has been measured, characterized, and reported in the following sections. The ISL75054M30VZ is radiation lot acceptance tested (RLAT) to 30krad(Si) and the ISL75054M50VZ is RLAT to 50krad(Si).

8.1 Total Ionizing Dose (TID) Testing

8.1.1 Introduction

Total dose testing of the ISL75054M proceeded in accordance with the guidelines of MIL-STD-883 Test Method 1019. The experimental matrix consisted of 16 samples irradiated under bias and 16 samples irradiated with all pins grounded (unbiased). Three control units were used. Figure 64 shows the bias configuration. The wafers were drawn from wafer lot F6X120. All samples were packaged in the production 16-Ld HTSSOP plastic package.

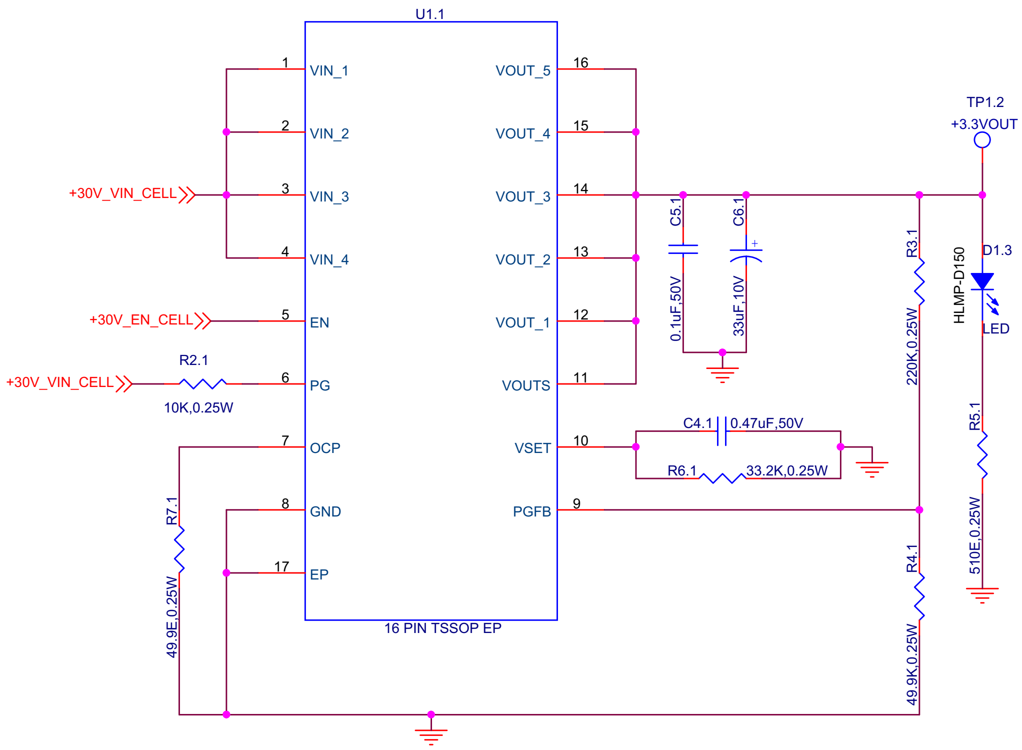


Figure 64. TID Testing Bias Configuration

Samples were irradiated at a low dose rate (LDR) of 0.01rad(Si)/s using a Hopewell Designs N40 vault-type LDR irradiation located in the Palm Bay, Florida, Renesas Facility. A PbAl box was used to shield the test fixture and devices against low energy, secondary gamma radiation. All electrical testing was performed outside the irradiator using the production Automated Test Equipment (ATE) with data logging at each downpoint. Downpoint electrical testing was performed at room temperature. The planned irradiation downpoints were 0krad(Si), 10krad(Si), 30krad(Si), and 50krad(Si).

8.1.2 Results

Table 2 summarizes the attributes data.

Table 2. Attributes Data

Dose Rate (rad(Si)/s)	Condition	Sample Size	Downpoint	Pass[1]	Fail
0.01	Biased (Figure 64)	16	Pre-irradiation	16	0
			10krad(Si)	16	0
			30krad(Si)	16	0
			50krad(Si)	16	0
0.01	Grounded	16	Pre-irradiation	16	0
			10krad(Si)	16	0
			30krad(Si)	16	0
			50krad(Si)	16	0

1. A Pass indicates a device that passes all the datasheet specification limits.

The plots in Figure 65 through Figure 89 show data for key parameters at all downpoints. The plots show the sample size average as a function of the total dose for each irradiation condition. All parts showed excellent stability over irradiation.

8.1.3 Typical Radiation Performance

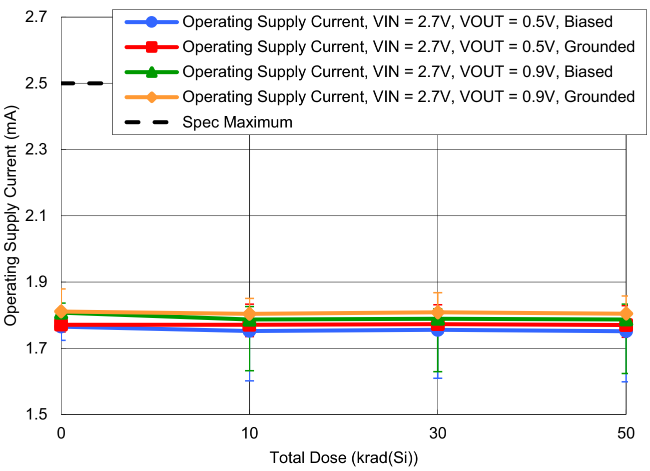


Figure 65. Operating Supply Current with V_{IN} = 2.7V vs TID

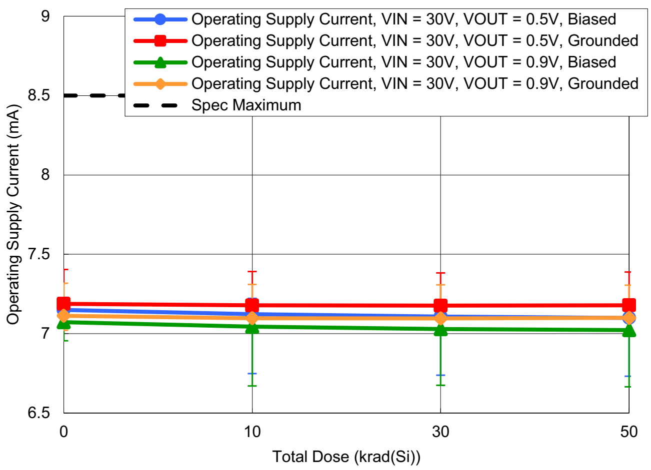


Figure 66. Operating Supply Current with V_{IN} = 30V vs TID

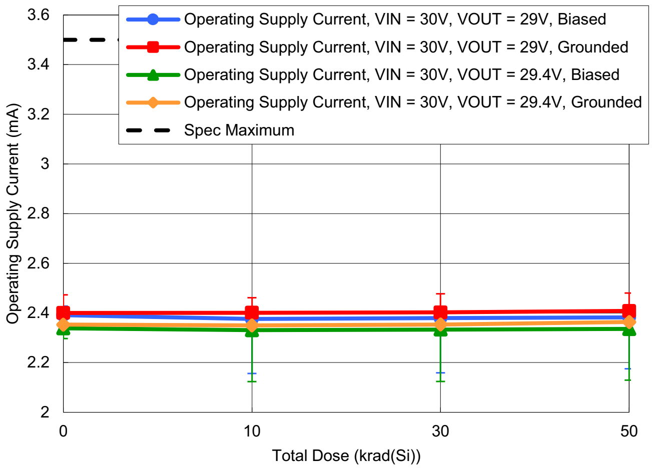


Figure 67. Operating Supply Current with V_{IN} = 30V vs TID

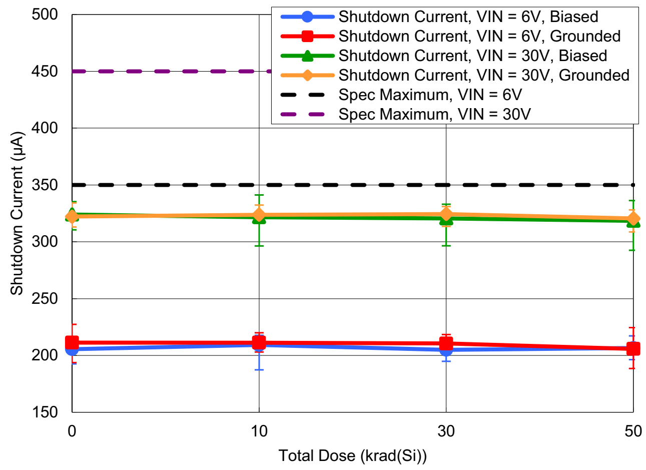


Figure 68. Shutdown Current vs TID

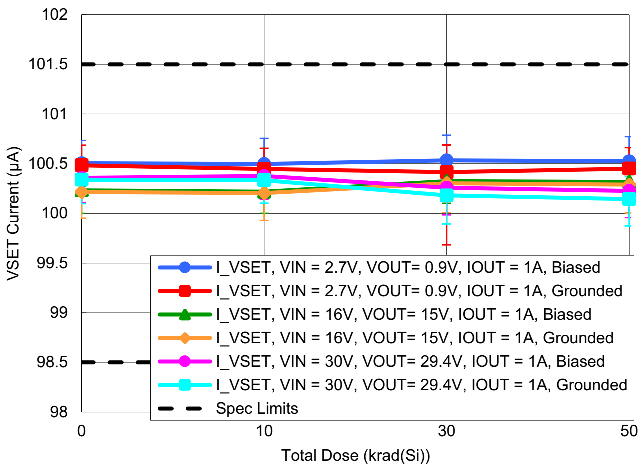


Figure 69. VSET Current with I_{OUT} = 1A vs TID

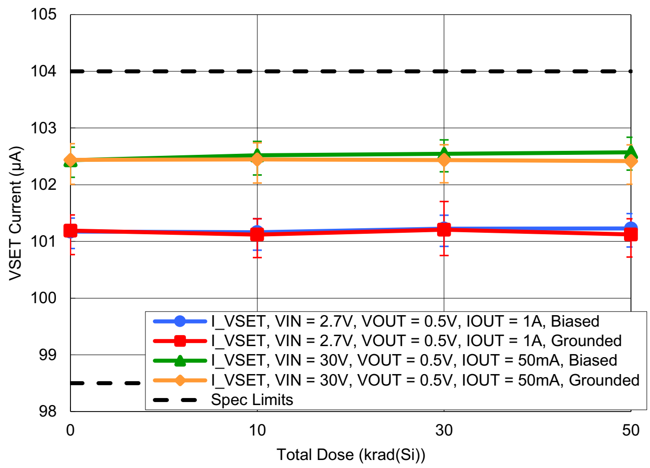


Figure 70. VSET Current with V_{OUT} = 0.5V and I_{OUT} = 1A or 50mA vs TID

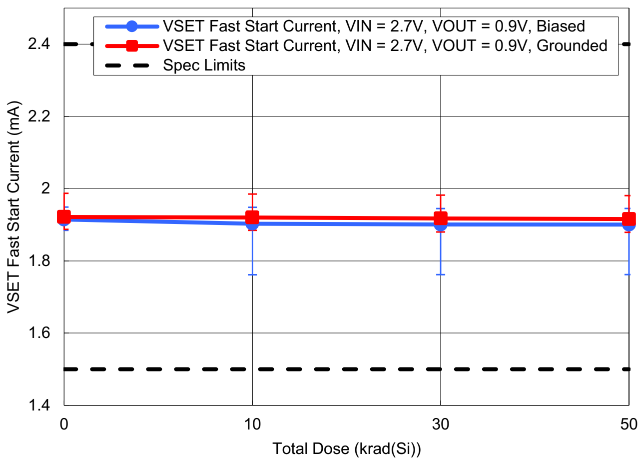


Figure 71. VSET Fast Start Current vs TID

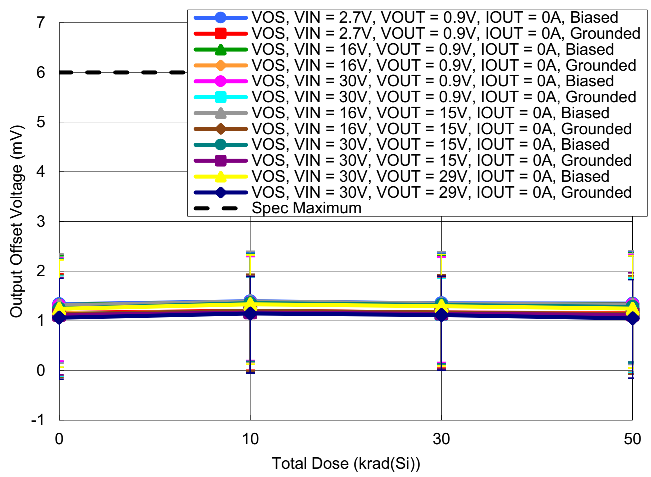


Figure 72. Output Offset Voltage with I_{OUT} = 0A vs TID

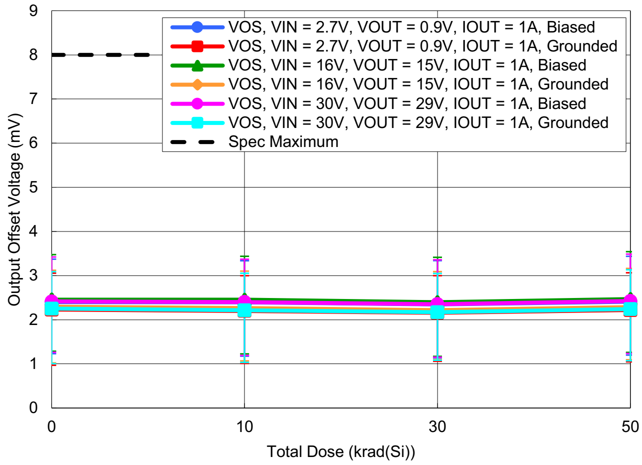


Figure 73. Output Offset Voltage with I_{OUT} = 1A vs TID

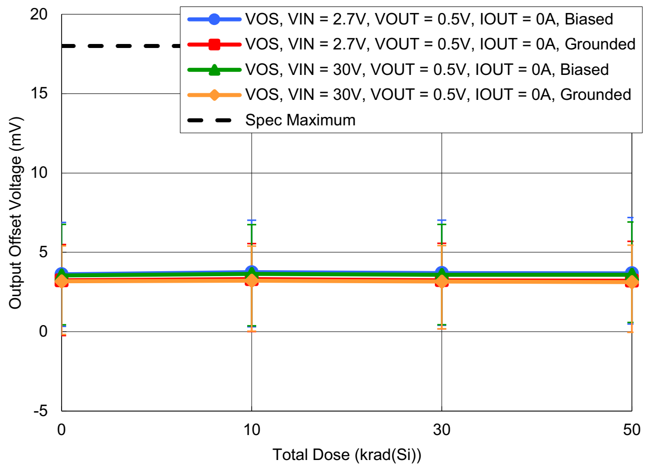


Figure 74. Output Offset Voltage with V_{OUT} = 0.5V and I_{OUT} = 0A vs TID

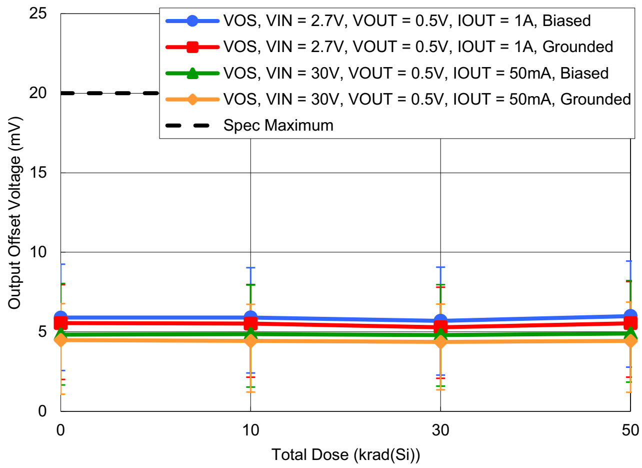


Figure 75. Output Offset Voltage with V_{OUT} = 0.5V and I_{OUT} = Maximum vs TID

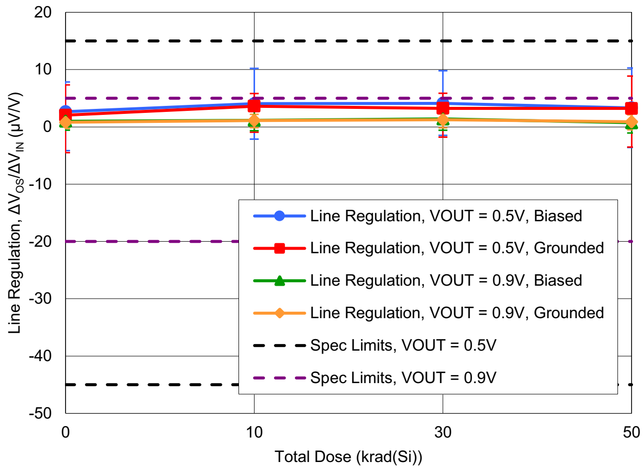


Figure 76. Line Regulation, $\Delta V_{OS}/\Delta V_{IN}$ vs TID

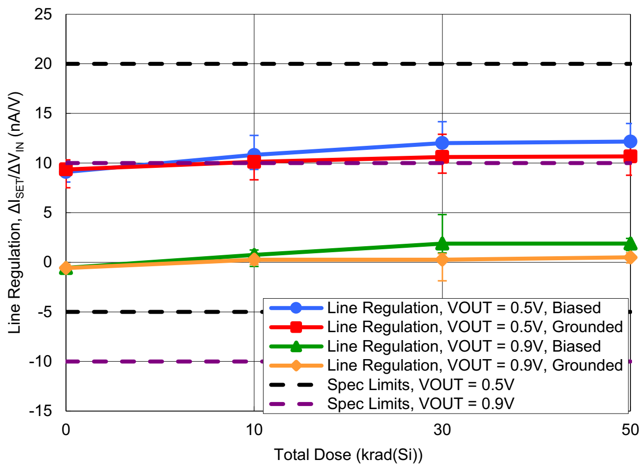


Figure 77. Line Regulation, $\Delta I_{SET}/\Delta V_{IN}$ vs TID

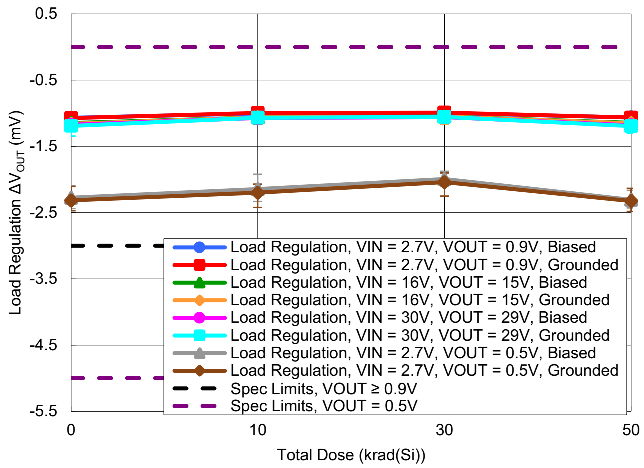


Figure 78. Load Regulation ΔV_{OUT} vs TID

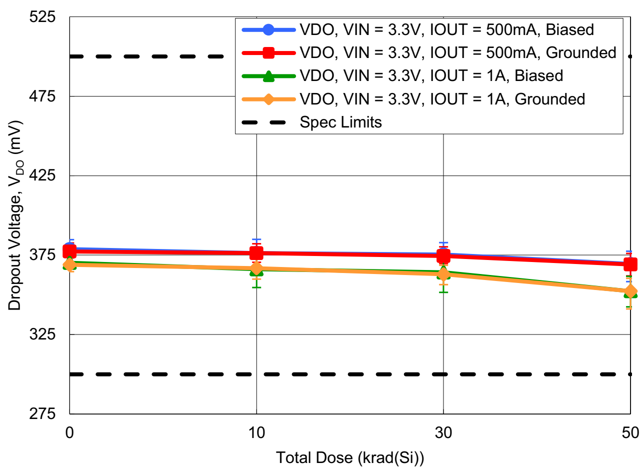


Figure 79. Dropout Voltage, V_{DO} vs TID

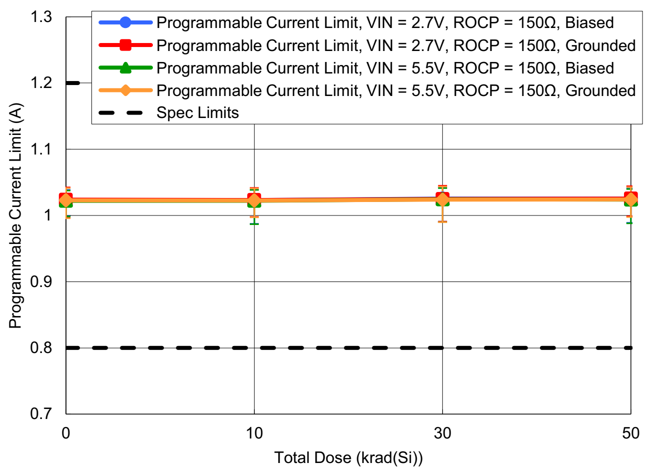


Figure 80. Programmable Current Limit with R_{OCP} = 150Ω vs TID

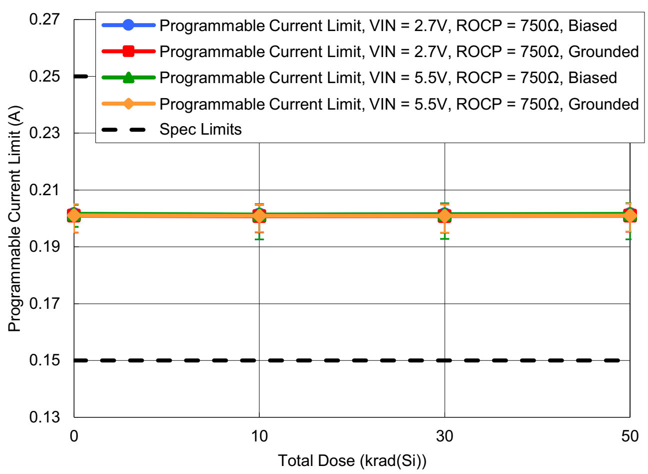


Figure 81. Programmable Current Limit with R_{OCP} = 750Ω vs TID

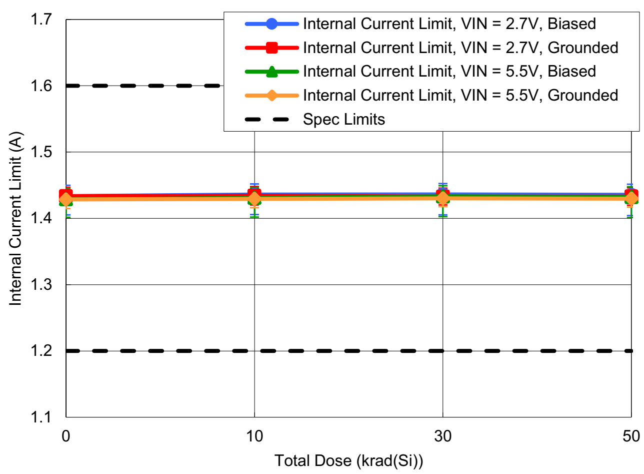


Figure 82. Internal Current Limit with V_{IN} = 2.7V or 5.5V vs TID

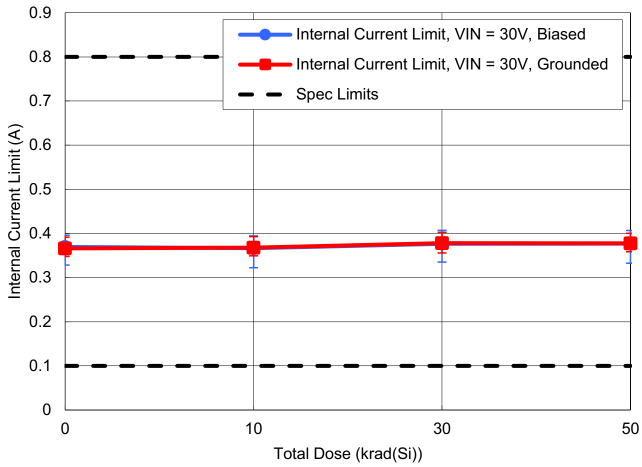


Figure 83. Internal Current Limit with V_{IN} = 30V vs TID

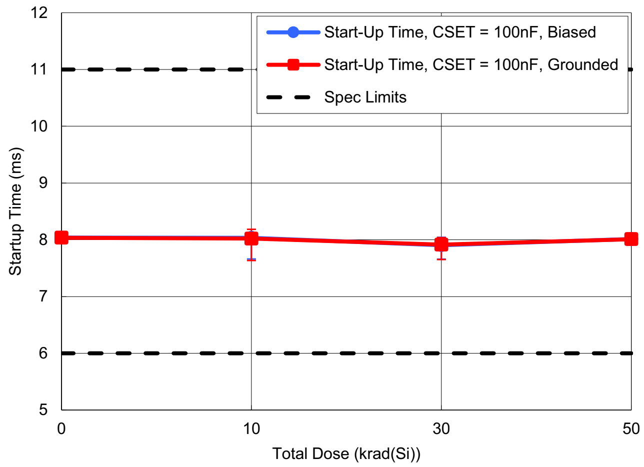


Figure 84. Startup Time with CSET = 100nF vs TID

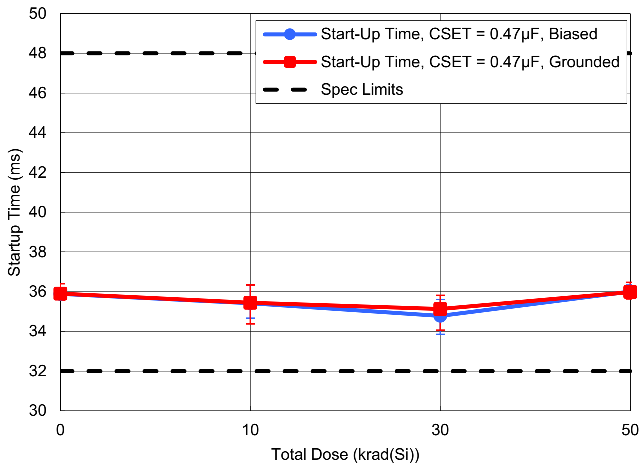


Figure 85. Startup Time with CSET = 0.47µF vs TID

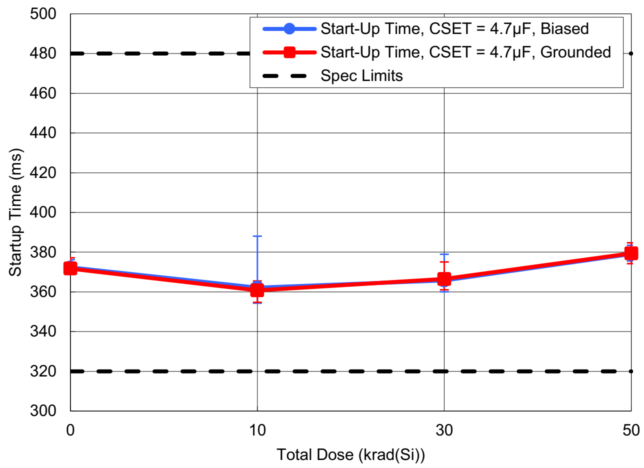


Figure 86. Startup Time with CSET = 4.7µF vs TID

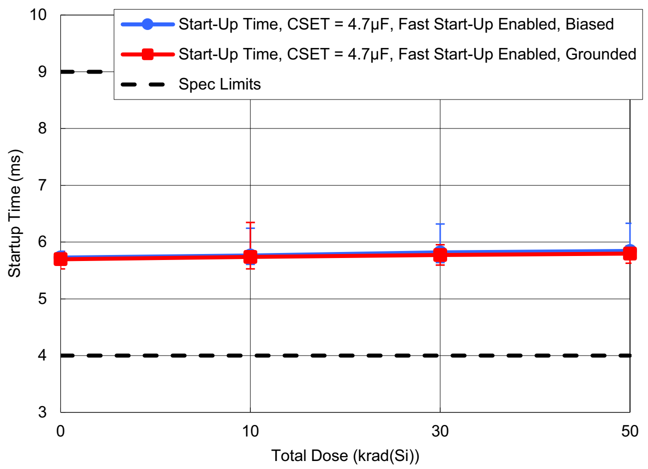


Figure 87. Startup Time with CSET = 4.7µF and Fast Startup Enabled vs TID

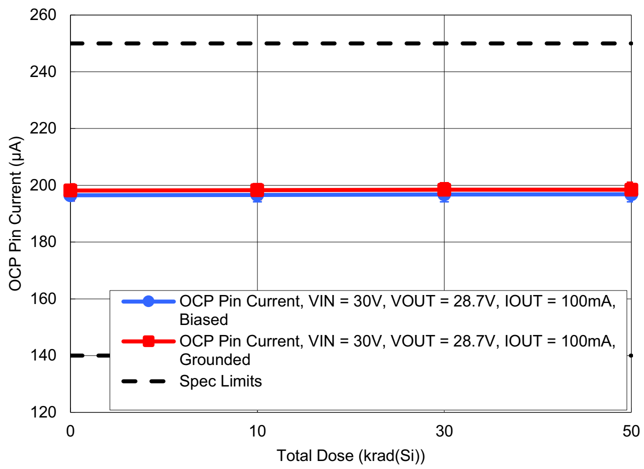


Figure 88. OCP Pin Current with I_{OUT} = 100mA vs TID

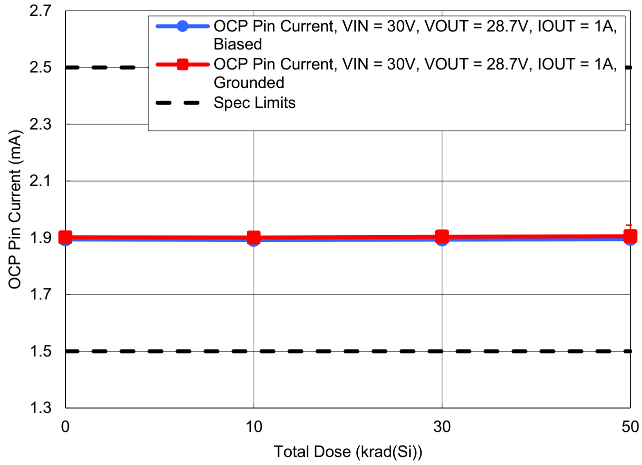


Figure 89. OCP Pin Current with I_{OUT} = 1A vs TID

8.1.4 Conclusion

ATE characterization testing showed no rejects to the datasheet limits at all downpoints. Variables data for selected parameters are presented in Figure 65 through Figure 89. No differences between biased and unbiased irradiation were noted and the part is not considered bias sensitive.

8.2 Single-Event Effects Testing

8.2.1 Introduction

The intense proton and heavy ion environment encountered in space applications can cause a variety of Single-Event Effects (SEE) in electronic circuitry, including Single Event Upset (SEU), Single Event Transient (SET), Single Event Functional Interrupt (SEFI), Single Event Gate Rupture (SEGR), and Single Event Burnout (SEB). SEE can lead to system-level performance issues, including disruption, degradation, and destruction. Individual electronic components should be characterized for predictable and reliable space system operation to determine their SEE response. This section discusses the results of SEE testing on the ISL75054M low noise LDO.

8.2.2 Test Facility

SEE testing was performed at the Texas A&M University (TAMU) Radiation Effects Facility of the Cyclotron Institute heavy ion facility. The facility is coupled to a K500 super-conducting cyclotron that can generate a wide range of particle beams with the various energy, flux, and fluence levels needed for advanced radiation testing. The Devices Under Test (DUTs) were in air at 40mm from the Aramica window for the ion beam. SET testing was performed on October 17, 2024 with normal incidence silver ions for an LET of 45.8MeV·cm^2/mg at the surface of the device. The LET of the ions in the active silicon layer ranged from 48.1MeV·cm^2/mg to 50.5MeV·cm^2/mg. The range to the Bragg peak was 67.6µm.

8.2.3 Destructive Single Event Effects (DSEE) Results

DSEE testing was performed to determine the maximum input supply voltage (V_{IN}) free from DSEEs at a die temperature of 125°C. The test board was laid out such that two parts could be irradiated simultaneously. During each test run, the DUTs were exposed to a fluence of 1E7ions/cm^2. Testing was conducted in two sections, one with EN high and one with EN grounded.

For DSEE testing with EN high, I_{OUT} was set to 1.1A. V_{IN} was initially set to 26V and V_{OUT} was initially set to 25V. The values of V_{IN} and V_{OUT} were simultaneously increased by 1V following each run until a DSEE was observed or V_{IN} reached 32V and V_{OUT} reached 31V. Figure 90 shows the test schematic used for DSEE testing. To increase VIN and VOUT without making a board modification between runs V_{OUT} was set using an external power supply connected to V_{SET}. Due to this, PG and fast start functionalities were disabled, however their circuit blocks were still on and had the opportunities to exhibit DSEEs. A device was considered to have exhibited a DSEE if the output voltage at no load deviated by ±1%, the current on V_{IN} or PG at no load deviated by ±5%, or there was a loss of functionality.

DSEE testing was also performed with EN grounded to apply the maximum stress to the pass transistor as blocking mode is the worst-case condition for MOSFETs. For this testing, V_{OUT} was tied to ground and there was no load. The voltage on V_{IN} was increased by 1V following each run until a DSEE was observed or V_{IN} reached 32V. A device was considered to have exhibited a DSEE if the current on V_{IN} deviated by ±10%.

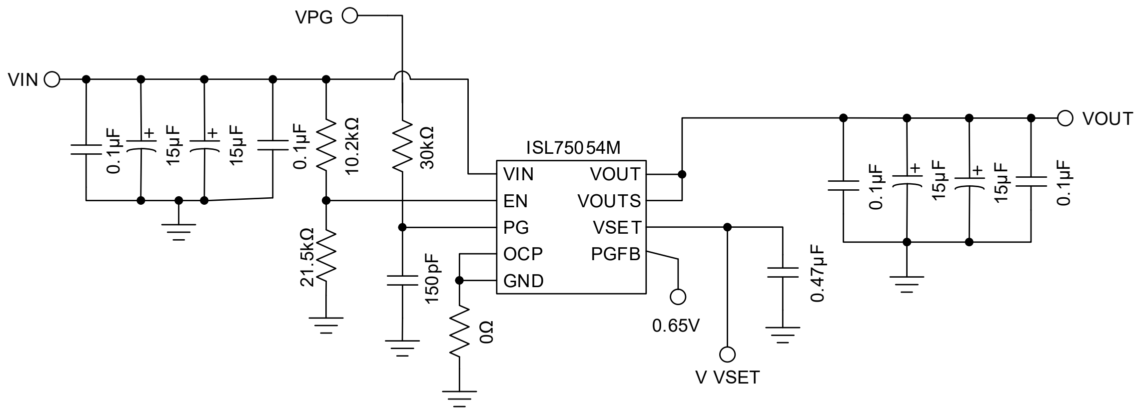


Figure 90. DSEE Test Schematic

All devices passed testing at each electrical condition. Therefore, DSEE testing indicates that the ISL75054M is insensitive to SEB when biased with a maximum of V_{IN} = 32V, V_{PG} = 32V, and I_{OUT} = 1.1A at 125°C regardless of whether EN is high or low at 45.8MeV·cm^2/mg.

8.2.4 SET Results

Figure 91 shows the test schematic used for SET testing. V_{OUT} was set using the R_{SET} resistor, and PG and fast-start were enabled. The voltage on PG was pulled up to 5V and PGFB was set using a voltage divider. A low pass filter of 30kΩ and 150pF was applied to PG and a 470pF capacitor was connected from VOUT to PGFB for SEE mitigation. The test board was laid out such that two parts could be irradiated simultaneously. During each test run, the DUTs were exposed to a fluence of 1E7ions/cm^2.

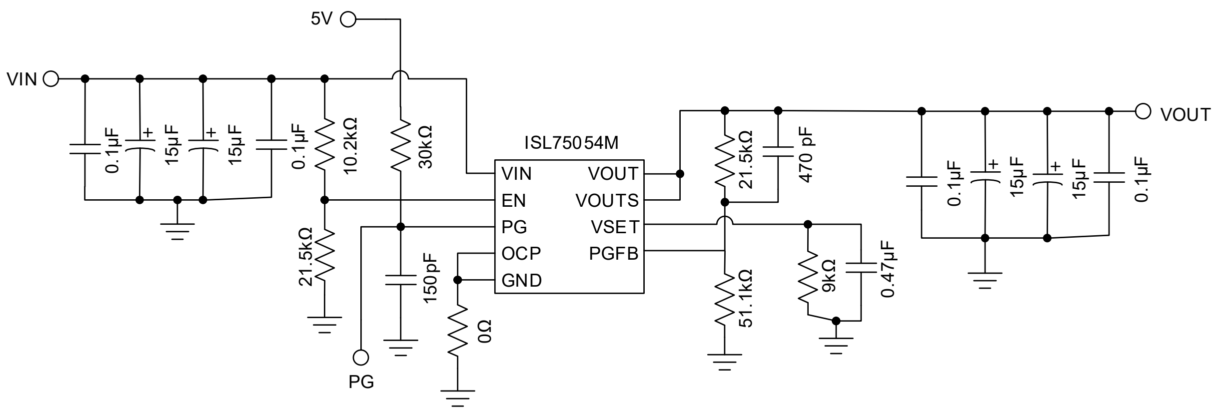


Figure 91. SET Test Schematic

For SET testing, devices were tested under three different test conditions as given in Table 3 at an ambient temperature of 25°C. Devices were monitored for V_{OUT} SETs, PG SETs, and SEFIs. A device exhibited a V_{OUT} SET when V_{OUT} deviated beyond ±2% of its operating value. A device exhibited a PG SET when PG pulled low but the device did not lose V_{OUT} regulation and there was no hold time on PG. The device exhibited a SEFI when PG pulled low and there was a loss of V_{OUT} regulation. The device then would restart and spontaneously recover with a normal fast-start. V_{OUT} SETs were captured with a trigger set to capture events in which V_{OUT} deviated beyond ±2% of its nominal value. PG SETs and SEFIs were captured with a trigger set to capture events in which PG dropped by 0.5V.

Table 3. SET Test Conditions

Test Condition	Number of Devices Tested	V_{IN} (V)	V_{OUT} (V)	I_{OUT} (mA)
#1	4	2.7	0.9	1000
#2	4	5	0.9	440
#3	4	27	0.9	69

The results of SET testing for the ISL75054M are summarized in Table 4. The ISL75054M did not exhibit V_{OUT} SETs, PG SETs, or SEFIs at 45.8MeV·cm^2/mg.

Table 4. SET Test Summary at 45.8MeV·cm^2/mg

Test Condition	# of DUTs	Total Fluence (ions/cm^2)	# of VOUT SETs	VOUT SET σ (µm^2)	# of PG SETs	PG SET σ (µm^2)	# of SEFIs	SEFI σ (µm^2)
#1	4	4.0E7	0	2.5	0	2.5	0	2.5
#2	4	4.0E7	0	2.5	0	2.5	0	2.5
#3	4	4.0E7	0	2.5	0	2.5	0	2.5

8.2.5 Conclusion

The ISL75054M was found to be free of DSEE when operated with a maximum of V_{IN} = 32V, V_{PG} = 32V, and I_{OUT} = 1.1A at 125°C regardless of whether EN is high or low at 45.8MeV·cm^2/mg.

The ISL75054M did not exhibit any V_{OUT} SETs, PG SETs, or SEFIs when tested at 45.8MeV·cm^2/mg. Therefore, the ISL75054M has excellent radiation performance for radiation tolerant applications.

9. Package Outline Drawing

The package outline drawing is located at the end of this document and is accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

10. Ordering Information

Part Number[1]	Part Marking	Radiation Lot Acceptance Testing (Total Ionizing Dose)	Package Description[2] (RoHS Compliant)	Package Drawing	MSL Rating[3]	Carrier Type[4]	Temp Range
ISL75054M30VZ	75054 MVZ	LDR to 30krad(Si)	16 Ld HTSSOP	M16.173C	1	Tray	-55 to +125°C
ISL75054M30VZ-T						Reel, 2.5k	
ISL75054M30VZ-T7A						Reel, 250	
ISL75054M50VZ	75054 MVZ	LDR to 50krad(Si)	16 Ld HTSSOP	M16.173C	1	Tray	-55 to +125°C
ISL75054M50VZ-T						Reel, 2.5k	
ISL75054M50VZ-T7A						Reel, 250	
ISL75054MVZEVAL1Z	Evaluation Board for HTSSOP package						
ISL75054MVZDEMO1Z	Demonstration Board for HTSSOP package						

1. These Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu-Ag plate-e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. For the Pb-Free Reflow Profile, see TB493.
3. For more information about MSL, see TB363.
4. See TB347 for details about reel specifications.

11. Revision History

Rev.	Date	Description
1.01	Feb 5, 2026	▪ Updated Abs Max section (split out first row). ▪ Updated the test conditions for the Start-Up Time specs. ▪ Removed duplicate noise figure. ▪ Updated the Foldback Current Limit figure. ▪ Added over-temperature curves. ▪ Updated Bode Plot Curves. ▪ Corrected Equation 4. ▪ Updated the Output Capacitance and Stability section. ▪ Updated Figures 53 and 54.
1.00	Apr 21, 2025	Initial release

A. ECAD Design Information

This information supports the development of the PCB ECAD model for this device. It is intended to be used by PCB designers.

A.1 Part Number Indexing

Orderable Part Number	Number of Pins	Package Type	Package Code/POD Number
ISL75054M30VZ	16	HTSSOP	M16.173C
ISL75054M30VZ-T	16	HTSSOP	M16.173C
ISL75054M30VZ-T7A	16	HTSSOP	M16.173C
ISL75054M50VZ	16	HTSSOP	M16.173C
ISL75054M50VZ-T	16	HTSSOP	M16.173C
ISL75054M50VZ-T7A	16	HTSSOP	M16.173C

A.2 Symbol Pin Information

A.2.1 16-HTSSOP

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
1	VIN	Power	-
2	VIN	Power	-
3	VIN	Power	-
4	VIN	Power	-
5	EN	Input	-
6	PG	Output	-
7	OCP	Input	-
8	GND	Power	-
9	PGFB	Input	-
10	VSET	Output	-
11	VOUTS	Input	-
12	VOUT	Output	-
13	VOUT	Output	-
14	VOUT	Output	-
15	VOUT	Output	-
16	VOUT	Output	-
EPAD17	GND	Power	-

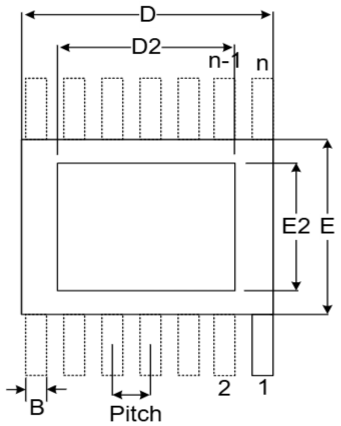
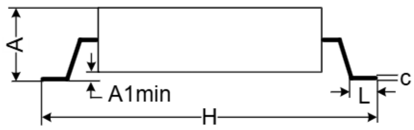
A.3 Symbol Parameters

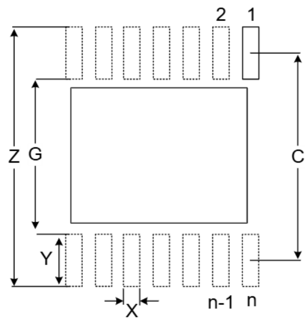
Orderable Part Number	Qualification	Radiation Qualification	LDR	Mounting Type	RoHS	Number of Outputs	Min Operating Temperature	Max Operating Temperature	Min Input Voltage	Max Input Voltage	Output Current
ISL75054M30VZ	Space	Radiation Tolerant	30 krad(Si)	SMD	Compliant	1	-55 °C	125 °C	2.7 V	30 V	1 A
ISL75054M30VZ-T	Space	Radiation Tolerant	30 krad(Si)	SMD	Compliant	1	-55 °C	125 °C	2.7 V	30 V	1 A
ISL75054M30VZ-T7A	Space	Radiation Tolerant	30 krad(Si)	SMD	Compliant	1	-55 °C	125 °C	2.7 V	30 V	1 A
ISL75054M50VZ	Space	Radiation Tolerant	50 krad(Si)	SMD	Compliant	1	-55 °C	125 °C	2.7 V	30 V	1 A
ISL75054M50VZ-T	Space	Radiation Tolerant	50 krad(Si)	SMD	Compliant	1	-55 °C	125 °C	2.7 V	30 V	1 A
ISL75054M50VZ-T7A	Space	Radiation Tolerant	50 krad(Si)	SMD	Compliant	1	-55 °C	125 °C	2.7 V	30 V	1 A

A.4 Footprint Design Information

A.4.1 16-HTSSOP

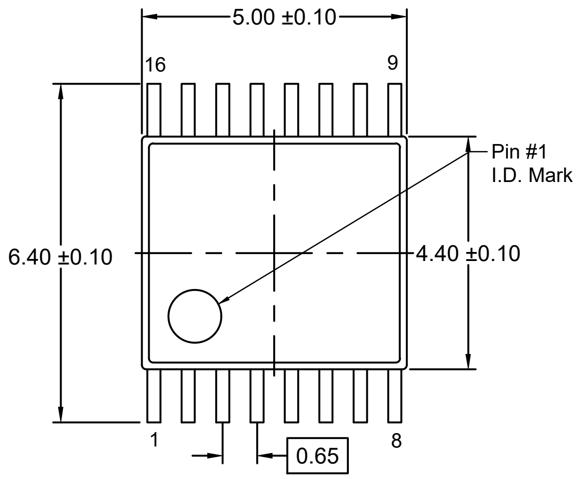
IPC Footprint Type	Package Code/ POD Number	Number of Pins
SOP	M16.173C/HV0016AB	16

Description	Dimension	Value (mm)	Diagram
Minimum body span (pin1 side)	Dmin	4.9	 Bottom View
Maximum body span (pin1 side)	Dmax	5.1	
Minimum body span	Emin	4.3	
Maximum body span	Emax	4.5	
Minimum Lead Width	Bmin	0.19	
Maximum Lead Width	Bmax	0.3	
Total number of pin positions (including absent pins)	PinCount	16	
Distance between the center of any two adjacent pins	Pitch	0.65	
Minimum thermal pad size (pin1 side)	D2min	3.5	
Maximum thermal pad size (pin1 side)	D2max	3.7	
Minimum thermal pad size	E2min	2.9	
Maximum thermal pad size	E2max	3.1	
Minimum lead span	Hmin	6.3	 Side View
Maximum lead span	Hmax	6.5	
Minimum Lead Length	Lmin	0.45	
Maximum Lead Length	Lmax	0.75	
Maximum Height	Amax	1.2	
Minimum Standoff Height	A1min	0.05	
Minimum Lead Thickness	cmin	0.09	
Maximum Lead Thickness	cmax	0.20	

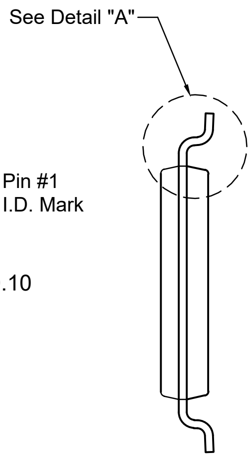
Recommended Land Pattern			
Description	**Dimension**	**Value (mm)**	**Diagram**
Distance between left pad toe to right pad toe.	Z	7.0	 PCB Top View
Distance between left pad heel to right pad heel.	G	4.6	
Row spacing. Distance between pad centers	C	5.8	
Pad Width	X	0.33	
Pad Length	Y	1.20	

Package Outline Drawing

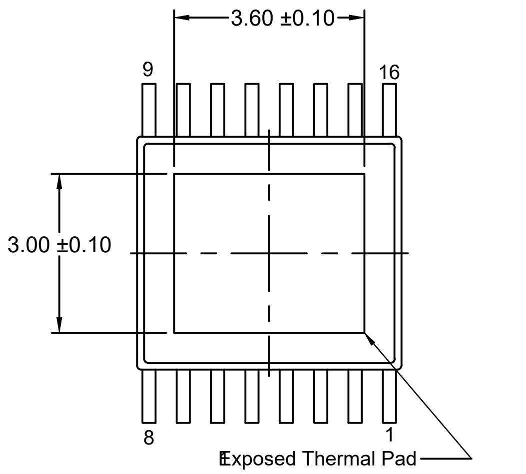
M16.173C
HV0016AB
16-HTSSOP 5.0 x 4.4 x 1.2 mm Body, 0.65 mm Pitch Epad 3.6 X 3.0 mm
Rev01, Date Created: Apr 2, 2025



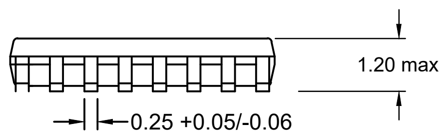
Top View



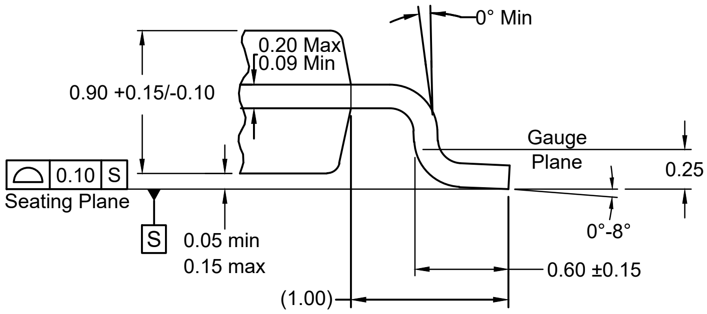
End View



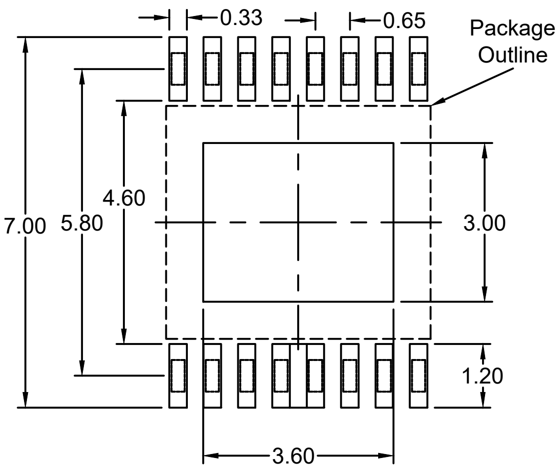
Bottom View



Side View



Detail "A"



Typical Recommended Land Pattern

Notes:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Foot length is measured at gauge plane 0.25 mm above seating plane.

Corporate Headquarters

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Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.