ISL73033SLHM

Radiation Hardened Driver-GaN Power Stage with 100V GaN FET

The ISL73033SLHM is a radiation hardened Driver-GaN power stage with a 4.5V gate driver and a 100V, 7.5mΩ enhancement-mode Gallium Nitride (GaN) FET in one package. The device simplifies the PCB layout by integrating a driver plus GaN FET in one package and is designed for isolated topologies and boost type configurations. The driver operates with a supply voltage from 4.5V to 13.2V and has both inverting (INB) and non-inverting (IN) inputs to satisfy requirements for inverting and non-inverting gate drives with a single device.

The ISL73033SLHM has a 4.5V gate drive voltage (V_{DRV}) generated using an internal regulator that prevents the gate voltage from exceeding the maximum gate-source rating of enhancement-mode GaN FETs. The gate drive voltage also features Undervoltage Lockout (UVLO) protection that ignores the inputs (IN/INB) and keeps the GaN FET in an OFF state whenever V_{DRV} is below the UVLO threshold.

The ISL73033SLHM inputs can withstand voltages up to 14.7V regardless of the V_{DD} voltage, allowing the inputs to be connected directly to most PWM controllers.

The ISL73033SLHM is offered in an 81 ball 8x8mm Ball Grid Array (BGA) package.

Features

- Production testing and qualification follow the standard AS6294/1
- 100V, 7.5mΩ eGaN FET with integrated 4.5V gate driver
- Wide driver bias range of 4.5V to 13.2V
- Up to 16.5V logic inputs (regardless of V_{DD} level)
  - Inverting and non-inverting inputs
- Integrated driver optimized for enhancement-mode GaN FETs
  - Internal 4.5V regulated gate drive voltage
- Full military temperature range operation
  - T_A = -55°C to +125°C
  - T_J = -55°C to +150°C
- Radiation hardness assurance (lot-by-lot)
  - Low dose rate (0.01rad(Si)/s): 75krad(Si)
- SEE hardness for Driver (see the SEE test report)
  - No SEB/L LET_{TH}, V_{DD} = 16.5V: 86MeV•cm^2/mg
  - No SET, LET_{TH}, V_{DD} = 13.2V: 86MeV•cm^2/mg
- SEE hardness for GaN FET (see the SEE test report)
  - No SEB/L LET_{TH}, V_{DS} = 100V: 86MeV•cm^2/mg

Applications

- Flyback and forward converters
- Boost and PFC converters
- Secondary synchronous FET drivers

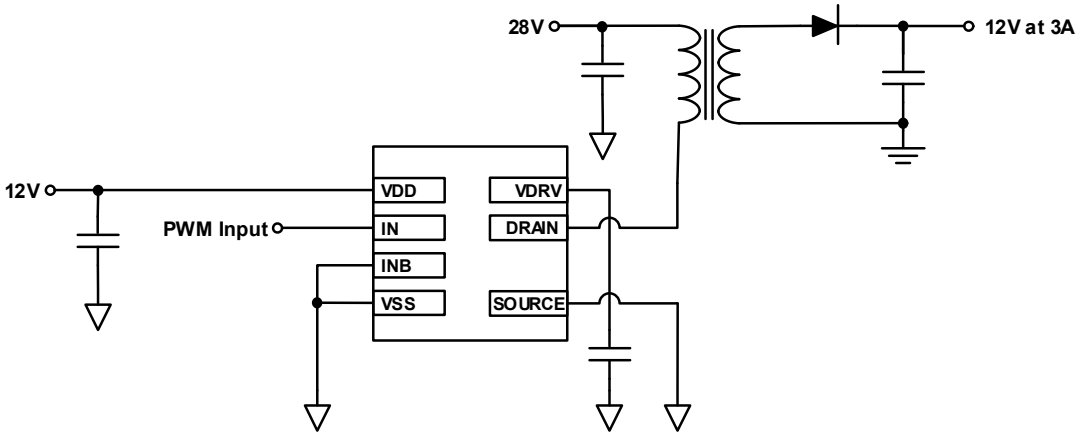


Figure 1. Typical Application: Flyback Power Supply

Contents

1. Overview

1.1 Block Diagram

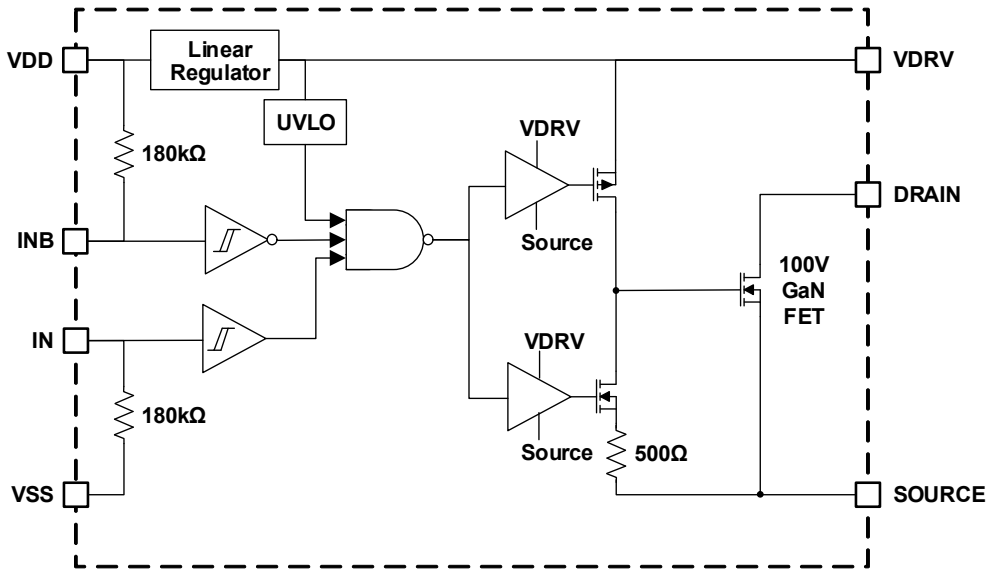
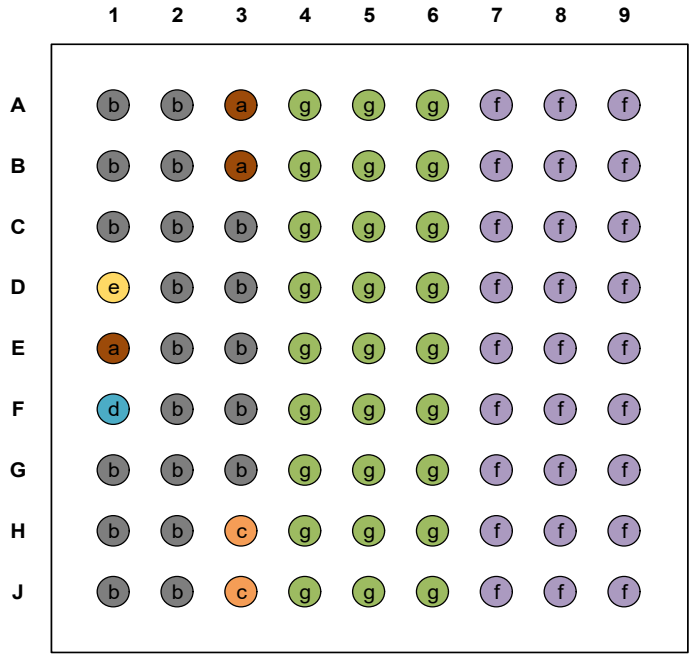


Figure 2. Functional Block Diagram

2. Pin Information

2.1 Pin Assignments



Legend:

Brown (a):	VDD	Yellow (e):	INB
Grey (b):	VSS	Purple (f):	DRAIN
Orange (c):	VDRV	Green (g):	SOURCE
Blue (d):	IN		

Top View

2.2 Pin Descriptions

Pin Name	ESD Circuit	Description
VDD	2	Supply for the internal linear regulator. Bypass VDD to VSS using at least a 4.7µF ceramic capacitor.
VSS	-	Ground reference for the logic circuitry. Internally shorted to Source.
VDRV	1	Gate drive voltage generated by the internal linear regulator. Bypass VDRV to SOURCE using at least a 4.7µF ceramic capacitor. See Applications Information for more details.
IN	2	Non-inverting TTL/CMOS input pin that controls the gate of the GaN FET. When using this device in an inverting application, tie this pin to VDD. The IN pin has a 180kΩ internal pull-down resistor to VSS.
INB	2	Inverting TTL/CMOS input pin that controls the gate of the GaN FET. When using this device in a non-inverting application, tie this pin to VSS. The INB pin has a 180kΩ internal pull-up resistor to VDD.
DRAIN	-	Drain connection for the GaN FET
SOURCE	-	Source connection for the GaN FET

ESD Circuits:

Circuit 1 Circuit 2

3. Specifications

3.1 Absolute Maximum Ratings

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
V_{DD} [1]	-0.3	+16.5	V
IN, INB[1]	-0.3	+16.5	V
VDRV	-0.3	+6.5	V
VDRV[1]	-0.3	+6.2	V
V_{DS} Drain to Source Voltage[1]		100	
ESD Rating	**Value**		**Unit**
Human Body Model (Tested per MIL-STD-883 TM3015)	1.75		kV
Charged Device Model (Tested per JS-002-2014)	2.0		kV

1. Tested in a heavy ion environment at LET = 86MeV•cm^2/mg at +125°C (TC) for SEB.

3.2 Outgas Testing

Specification (Tested per ASTM E595, 1.5)	Value	Unit
Total Mass Lost[1]	0.09	%
Collected Volatile Condensible Material[1]	<0.01	%
Water Vapor Recovered	0.03	%

1. Outgassing results meet NASA requirements of total mass loss <1% and collected volatile condensible material of <0.1%.

3.3 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)[1]	θ_{JC} (°C/W)[2]
81 Ball 8x8mm BGA Package	22.6	5.5

1. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features including vias to buried source and drain planes. See TB379.
2. For θ_{JC}, the case temperature location is the bottom of the ball at the center of the package underside.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature		+150	°C
Maximum Storage Temperature Range	-65	+150	°C
Pb-Free Reflow Profile	See TB493		

3.4 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Case Operating Temperature Range	-55	+125	°C
V_{DD}	4.5	13.2	V
IN, INB	0	13.2	V
V_{DS} Voltage		80	V
I_D (T_C = +25°C)[1]		36	A
I_D (T_C = +105°C)[2]		20	A

1. T_J = +150°C. Current is limited by die constraints.
2. T_J = +150°C. Current is limited by package constraints.

3.5 Electrical Specifications

Unless otherwise noted, V_{DD} = 4.5V, 13.2V, V_{DS} = 80V, V_{SS} = SOURCE = 0V, C_{VDRV} = 4.7µF, V_{IH} = 5.0V, V_{IL} = 0V. **Boldface limits apply across the operating temperature range, -55°C to +125°C or over a total ionizing dose of 75krad(Si) with exposure at an LDR of <10mrad(Si)/s.**

Parameter	Symbol	Test Conditions	Min[1]	Typ[2]	Max[1]	Unit
Power Supply						
Quiescent Supply Current	I_{DDQ}	V_{DD} = 4.5V, IN = 0V, INB = V_{DD}		1.4	**2.5**	mA
		V_{DD} = 13.2V, IN = 0V, INB = V_{DD}		1.5	**2.5**	mA
Operating Supply Current	I_{DDO}	V_{DD} = 4.5V, f_{PWM} = 500kHz		6.8	**16**	mA
		V_{DD} = 13.2V, f_{PWM} = 500kHz		7.3	**18**	mA
Gate Drive Voltage						
Output Voltage	V_{DRV}	V_{DD} = 4.5V, 25mA load on VDRV	**4.34**	4.44		V
		V_{DD} = 13.2V, 25mA load on VDRV	**4.39**	4.57	**4.71**	V
Current Limit of V_{DRV}	I_{LIM}	V_{DD} = 4.5V, 13.2V	**100**	150	**210**	mA
Undervoltage Lockout (UVLO) on V_{DRV}						
UVLO Rising Threshold	V_{RDRV}		**3.79**	3.96	**4.12**	V
UVLO Falling Threshold	V_{FDRV}		**3.50**	3.70	**3.90**	V
UVLO Hysteresis	V_{HDRV}		**150**	238	**375**	mV
Input Pins IN and INB						
High Level Threshold	V_{IH}			1.7	**2.0**	V
Low Level Threshold	V_{IL}		**1.0**	1.4		V
Input Hysteresis	V_{IHYS}		**150**	290	**400**	mV
Pull-Up/Down Resistor	$R_{INU/D}$	IN to V_{SS}, INB to V_{DD}	**125**	180	**275**	kΩ
Input Leakage Current	$I_{IN/INB}$	IN = 0V; INB = 13.2V	**-1**		**1**	µA
Output Static Characteristics						
Drain-to-Source Breakdown Voltage	BV_{DSS}	V_{IN} = 0V, V_{INB} = 0V, I_D = 1.2mA	**100**			V
Drain-to-Source Leakage Current	I_{DSS}	V_{IN} = 0V, V_{INB} = 0V, V_{DS} = 80V, V_{GS} = 0V		0.1	**1.1**	mA

Unless otherwise noted, V_{DD} = 4.5V, 13.2V, V_{DS} = 80V, V_{SS} = SOURCE = 0V, C_{VDRV} = 4.7µF, V_{IH} = 5.0V, V_{IL} = 0V. **Boldface limits apply across the operating temperature range, -55°C to +125°C or over a total ionizing dose of 75krad(Si) with exposure at an LDR of <10mrad(Si)/s. (Continued)**

Parameter	Symbol	Test Conditions	Min[1]	Typ[2]	Max[1]	Unit
Drain-to-Source On-Resistance	$r_{DS(ON)}$	V_{IN} = 5V, V_{INB} = 0V, I_D = 25A, T_A = 25°C, -55°C		7.5	11	mΩ
		V_{IN} = 5V, V_{INB} = 0V, I_D = 20A, T_A = 125°C, Post Rad, Post Burn-in		9.5	17	mΩ
Source-to-Drain Forward Voltage	V_{SD}	V_{IN} = 0V, V_{INB} = 0V, I_S = 0.5A, T_A = 25°C, -55°C	0.7	1.8	3.0	V
	V_{SD}	V_{IN} = 0V, V_{INB} = 0V, I_S = 0.5A, T_A = 125°C, Post Rad, Post Burn-in		2.3	3.2	V
Output Dynamic Characteristics						
Output Capacitance	C_{OSS}	V_{DS} = 50V, V_{IN} = 0V, V_{INB} = 0V		960		pF
Output Charge	Q_{OSS}	V_{DS} = 50V, V_{IN} = 0V, V_{INB} = 0V		71		nC
Timing Characteristics						
Turn-ON Propagation Delay	t_{DON-IN}	I_D = 12.5A, T_A = -55°C, Figure 3	26	37	52	ns
		I_D = 12.5A, T_A = +25°C, Figure 3	32	42	58	ns
		I_D = 12.5A, T_A = +125°C, Figure 3	35	50	64	ns
Turn-OFF Propagation Delay	$t_{DOFF-IN}$	I_D = 12.5A, T_A = -55°C, Figure 3	26	39	52	ns
		I_D = 12.5A, T_A = +25°C, Figure 3	32	44	58	ns
		I_D = 12.5A, T_A = +125°C, Figure 3	35	51	64	ns
Propagation Delay Matching	t_{DM-IN}	$\lvert t_{DON} - t_{DOFF} \rvert$		3	**8**	ns
Turn-ON Propagation Delay	$t_{DON-INB}$	I_D = 12.5A, T_A = -55°C, Figure 3	26	40	52	ns
		I_D = 12.5A, T_A = +25°C, Figure 3	32	45	58	ns
		I_D = 12.5A, T_A = +125°C, Figure 3	35	53	64	ns
Turn-OFF Propagation Delay	$t_{DOFF-INB}$	I_D = 12.5A, T_A = -55°C, Figure 3	26	39	52	ns
		I_D = 12.5A, T_A = +25°C, Figure 3	32	44	58	ns
		I_D = 12.5A, T_A = +125°C, Figure 3	35	52	64	ns
Propagation Delay Matching	t_{DM-INB}	$\lvert t_{DON} - t_{DOFF} \rvert$		3	**8**	ns
Rise Time (10% to 90%)	t_{RISE}			3.5	**11.5**	ns
Fall Time (90% to 10%)	t_{FALL}			5.0	**11.5**	ns

1. Parameters with MIN and/or MAX limits are 100% tested at -55°C, +25°C, and +125°C, unless otherwise specified.
2. Typical values shown are not guaranteed.

3.6 Timing Diagram

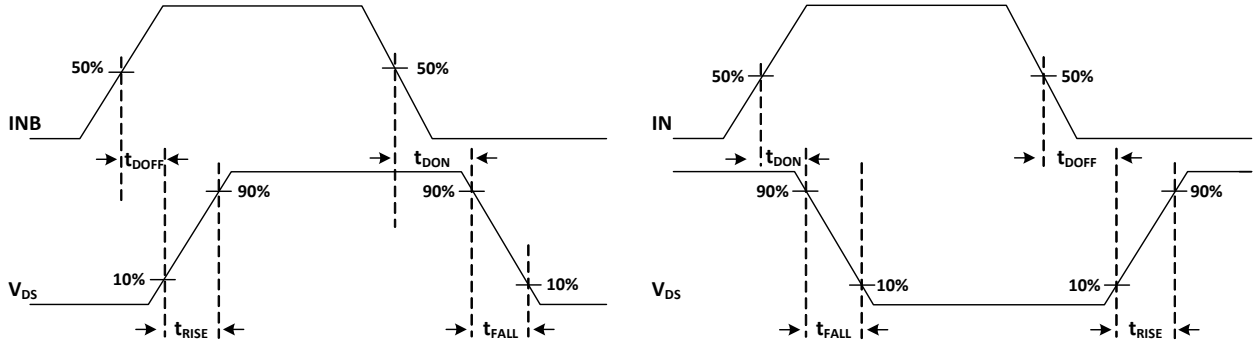


Figure 3. Timing Diagram for Propagation Delay

4. Typical Performance Graphs

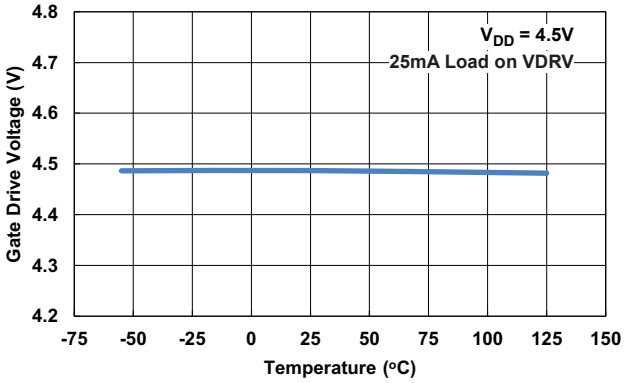


Figure 4. V_{DRV} vs Temperature

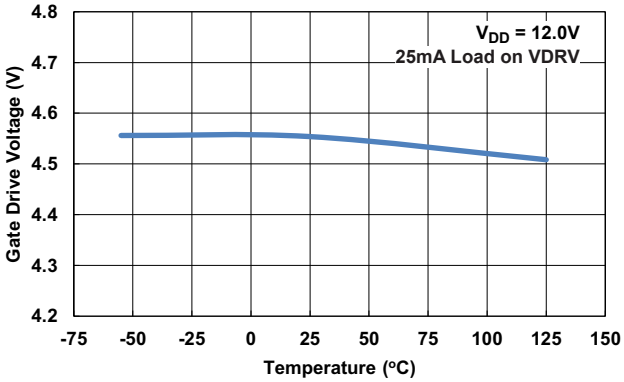


Figure 5. V_{DRV} vs Temperature

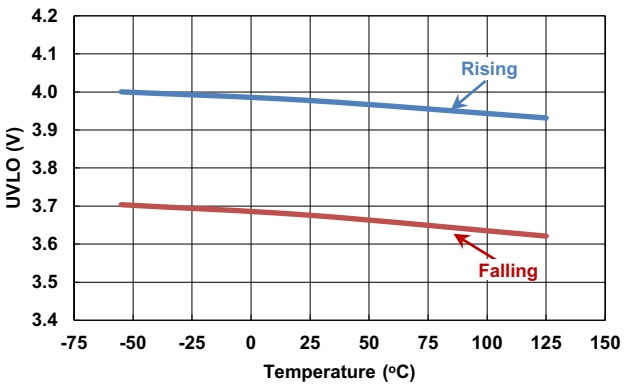


Figure 6. V_{DRV} Undervoltage Lockout Threshold

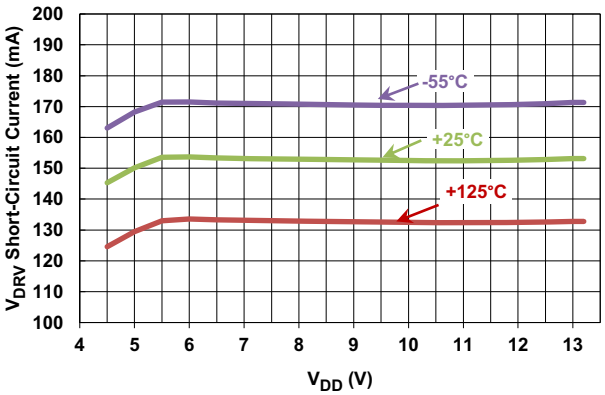


Figure 7. V_{DRV} Short-Circuit Current vs Temperature

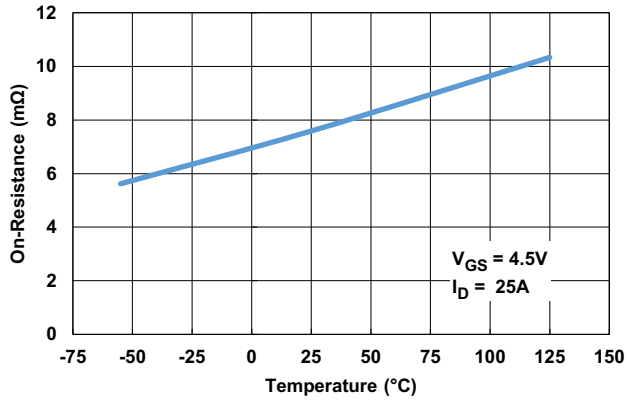


Figure 8. Drain-to-Source $r_{DS(ON)}$ vs Temperature

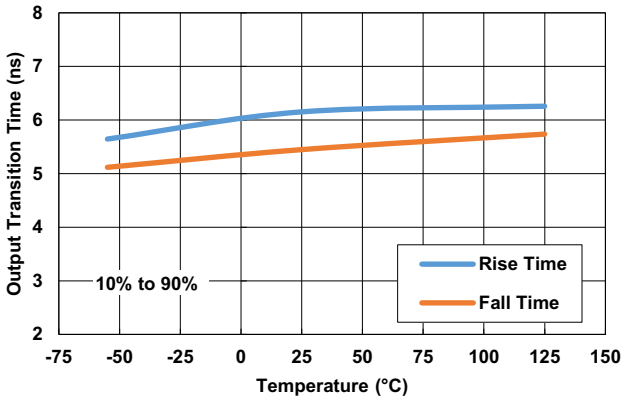


Figure 9. Output Transition Times vs Temperarture

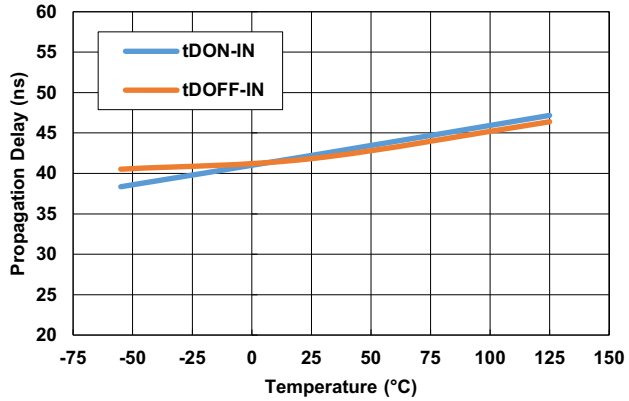


Figure 10. Input Propagation Delay vs Temperature

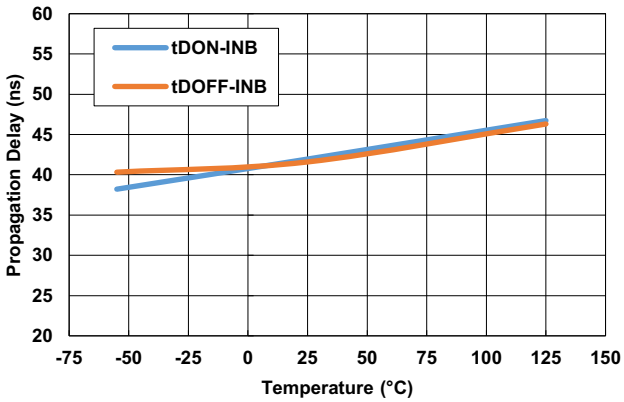


Figure 11. Input Bar Propagation Delay vs Temperature

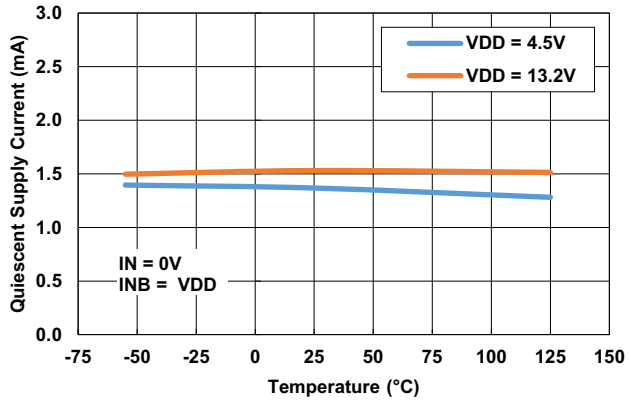


Figure 12. V_{DD} Quiescent Supply Current vs Temperature

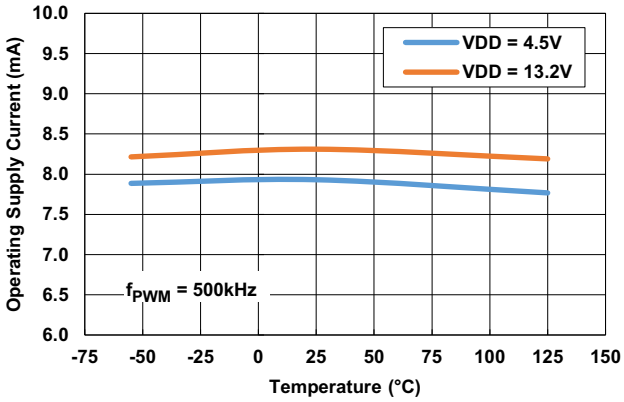


Figure 13. V_{DD} Operating Supply Current vs Temperature

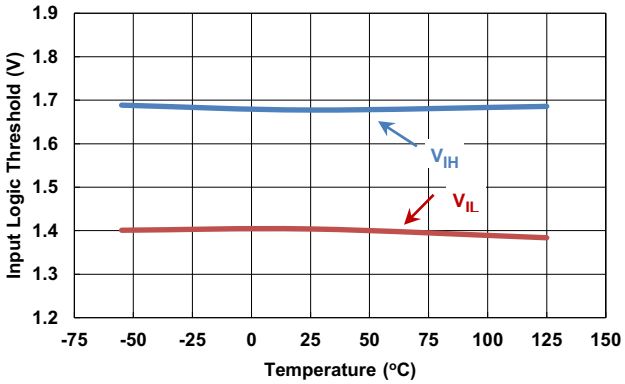


Figure 14. Input Logic Threshold vs Temperature

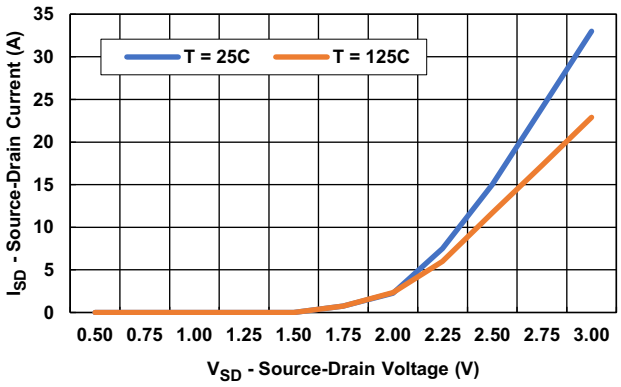


Figure 15. Reverse Drain-Source Characteristic; V_{GS} = 0V

5. Applications Information

5.1 Functional Overview

The ISL73033SLHM is a single channel high-speed low-side driver with a 100V enhanced mode GaN FET designed for boost, isolated power supplies and Synchronous Rectifier (SR) applications.

The ISL73033SLHM offers a wide operating supply range of 4.5V to 13.2V. The gate drive voltage is generated from an internal linear regulator to keep the gate-source voltage below the absolute maximum level of 6V for the GaN FET. The input stage can handle inputs to the 13.2V independent of V_{DD} and offers both inverting and non-inverting inputs. The typical propagation delay of 42ns enables high switching frequency operation.

5.2 Undervoltage Lockout

The VDD pin accepts a recommended supply voltage range of 4.5V to 13.2V and is the input to the internal linear regulator. VDRV is the output of the regulator and is equal to 4.5V. VDRV provides the bias for all internal circuitry and the gate drive voltage for the output stage.

A UVLO circuitry monitors the voltage on VDRV and prevents unexpected glitches when VDD is being turned on or turned off. When VDRV < ~1V, an internal 500Ω pull-down resistor helps keep the V_{GS} close to ground. When ~1.2V < VDRV < UV, the gate is driven low while ignoring the logic inputs. This low state has the same current sinking capacity as during normal operation, which ensures that the driven FETs are held off even if there is a switching voltage on the drains that can inject charge into the gates from the Miller capacitance.

When VDRV > UVLO, the output responds to the logic inputs following the next rising edge on IN or falling edge on INB. In the non-inverting operation (PWM signal applied to the IN pin), the output is in phase with the input. In the inverting operation (PWM signal applied to the INB pin), the output is out of phase with the input.

For the negative transition of VDD through the UV lockout voltage, the gate is held low when V_{DRV} < ~3.7V, regardless of the input logic states.

5.3 Input Stage

The ISL73033SLHM input thresholds are based on a TTL and CMOS compatible input threshold logic that is independent of the supply voltage. With typical high threshold = 1.7V and typical low threshold = 1.4V, the logic level thresholds can be conveniently driven with PWM control signals derived from 3.3V and 5V power controllers.

The ISL73033SLHM offers both inverting and non-inverting inputs. The state of the output pin is dependent on the bias on both input pins. Table 1 summarizes the inputs to output relation.

Table 1. Truth Table

IN	INB	V_{GS} (V)
0	0	0.0
0	1	0.0
1	0	4.5
1	1	0.0

As a protection mechanism, if any of the input pins are left in a floating condition, the gate of the GaN FET is held in a low state. This is achieved using an internal 180kΩ pull-up resistor on the INB pin to VDD and an internal 180kΩ pull-down resistor on the IN pin to VSS. For proper operation in non-inverting applications, connect INB to VSS. For proper operation in inverting applications, connect IN to VDD.

5.4 Enable Function

An enable or disable function can be easily implemented in the ISL73033SLHM using the unused input pin. The following guidelines describe how to implement the enable and disable functions:

- In a non-inverting configuration, the INB pin can be used to implement the enable and disable functions. The GaN FET driver is enabled when INB is biased low, acting as an active-low enable pin
- In an inverting configuration, the IN pin can be used to implement the enable and disable functions. The GaN FET driver is enabled when IN is biased high, acting as an active-high enable pin

The layout of the package facilitates the input pull-up and pull-down by placing VDD and VSS balls next to the inputs.

5.5 Power Dissipation of the Driver

The total power dissipation of the ISL73033SLHM is a combination of the power losses in the gate driver circuitry and the power losses of the GaN FET.

The power dissipation of the gate driver is dominated by the losses associated with the gate charge of the driven FETs and the switching frequency. The internal bias current also contributes to the total dissipation but is usually not significant compared to the gate charge losses.

For example, the included GaN FET has a total gate charge of 8nC (typical) when V_{DS} = 50V and V_{GS} = 4.5V. This is the charge that a driver must source to turn on the GaN FET and must sink to turn off the GaN FET. Use Equation 1 to calculate the power dissipation of the driver.

(EQ. 1)
$$PD_{driver} = Q_g \bullet freq \bullet V_{GS} + I_{DD}(freq) \bullet V_{DD} + \frac{V_{GS}}{r_{PD}} \bullet V_{DD} \bullet D$$

where:

- freq = switching frequency
- V_{GS} = V_{DRV} bias of the ISL73033SLHM, 4.5V
- Q_g = Gate charge for V_{GS}

- I_{DD}(freq) = Bias current at the switching frequency
- r_{PD} = Internal 500Ω pull-down resistance
- D = Duty cycle that gate drive is equal to V_{DRV} during one switching cycle.

The power dissipation of the GaN FET includes the conduction, switching, dead time, and output capacitance C_{OSS} related losses. Use Equation 2 to calculate the power dissipation of the GaN FET.

(EQ. 2) $$PD_{FET} = Pcond + Psw + Poss + Pdt$$

- $Pcond = I_{DRAIN}^2 \cdot r_{DS(ON)} \cdot (t_{ON}/t_{period})$
- $Psw = 0.5 \cdot V_{SD} \cdot I_{DRAIN} \cdot (t_{RISE} + t_{FALL}) \cdot freq$
- $P_{OSS} = 0.5 \cdot C_{OSS} \cdot V_{IN}^2 \cdot freq$
- $Pdt = V_{SD} \cdot I_{DRAIN} \cdot (Tdt_{ON} + Tdt_{OFF})$

where:

- $r_{DS(ON)}$ = GaN FET ON-resistance
- V_{SD} = GaN FET off source-drain forward conduction
- t_{ON}/t_{PERIOD} = GaN FET on duty cycle
- t_{RISE} is the drain voltage rise time from 0V to Vin
- t_{FALL} is the drain voltage fall time from Vin to 0V
- V_{IN} is the FET off drain voltage
- C_{OSS} is FET output capacitance
- Tdt_{ON} is the dead time before the FET turns on for a synchronous application
- Tdt_{OFF} is the dead time after the FET turns off for a synchronous application

The total power dissipation of the ISL73033SLHM is the sum of Equation 1 and Equation 2.

(EQ. 3) $$PD_{TOTAL} = PD_{driver} + PD_{FET}$$

5.6 Layout Guidelines

The ISL73033SLHM BGA package ball assignment is placed to allow for a simplified layout and optimizing performance. The following are the layout guidelines for external component placement and Printed Circuit Board (PCB) routing.

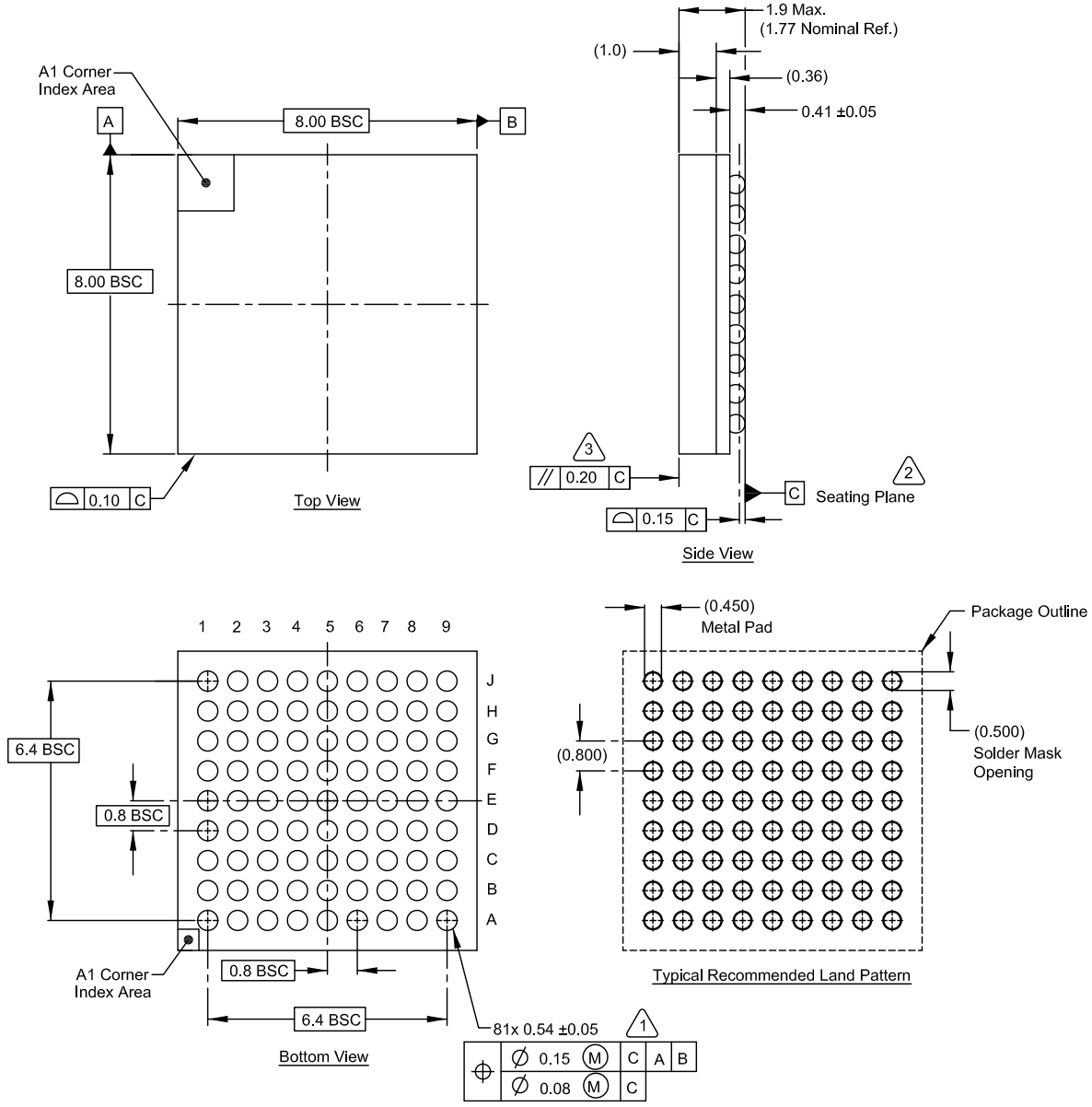
- Place a 4.7µF or larger X7R rated ceramic capacitor near the VDD and VSS balls.
- Place a 4.7µF or larger X7R rated ceramic capacitor near the VDRV and SOURCE balls.
- If using a non-inverting configuration, the INB ball is co-located next to the VSS balls for connecting INB to VSS. If using an inverting configuration, the IN ball is co-located next to the VDD ball for connecting IN to VDD.
- For the 100V GaN FET, connect the DRAIN close to the rectifier path to minimize parasitic inductance that may cause ringing or overshoot during switching and potentially exceed the drain-to-source voltage of the GaN FET.
- The DRAIN and SOURCE balls are the thermal dissipation path. Allow adequate areas of PCB copper to these balls on the top layer to carry away heat. Renesas also recommends using a conductively filled via underneath the balls to additional PCB layers to help carry heat away from the package.

6. Package Outline Drawing

For the most recent package outline drawing, see V81.8x8.

V81.8x8

81 Ball Plastic Ball Grid Array Package
Rev 0, 10/18



Notes:

1. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
2. Datum C (seating plane) is defined by the spherical crowns of the solder balls.
3. Parallelism measurement shall exclude any effect of the mark on the top surface of the package.
4. All dimensions and tolerances conform to ASME Y14.5M.
5. Units: mm

7. Ordering Information

Part Number[1][2]	Part Marking	Radiation Hardness (Total Ionizing Dose)	Package Description (RoHS Compliant)	Pkg. Dwg #	Carrier Type	Temp. Range
ISL73033SLHMKZ	ISL73033 SLHMKZ	LDR to 75krad(Si)	81 Ball BGA	V81.8x8	Tray	-55 to +125°C
ISL73033SLHMKZ/PROTO[3]	73033SLH /PROTO	N/A			Tray	
ISL73033SLHEV1Z[4]	Evaluation Board					

1. These Pb-free BGA packaged products employ special Pb-free material sets; molding compounds/die attach materials and SnAgCu - e6 solder ball terminals, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free BGA packaged products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. For Moisture Sensitivity Level (MSL), see the ISL73033SLHM device page. For more information about MSL, see TB363.
3. The /PROTO device is not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. This part is intended for engineering evaluation purposes only. The /PROTO part meets the electrical limits and conditions across temperature specified in this datasheet. This part type does not come with a Certificate of Conformance.
4. Evaluation board uses the /PROTO parts. The /PROTO parts are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity.

8. Revision History

Rev.	Date	Description
4.0	Jul 30, 2021	Updated Block Diagram. Updated pin descriptions for the IN and INB Pins. Updated Figures 8, 9, 12, and 13. Updated Input Stage section changed 300kΩ to 180kΩ. Updated Equation 1.
3.0	May 25, 2021	Updated Maximum spec for the recommended ID current at T_C = +25C from 45A to 36A. Added Note 1 in the Recommended Operating Conditions table. Added Figure 15. Updated the Power Dissipation of the Driver section. Reformatted the Ordering Information table.
2.0	Mar 24, 2021	Applied new template. Updated first features bullet. Updated base part number from ISL73033SLH to ISL73033SLHM throughout document.
1.0	Dec 18, 2020	Initial release

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