ISL73006SLH

Radiation Hardened 18V, 1A Point-of-Load Regulator

The ISL73006SLH is a radiation hardened Point-of-Load (POL) buck regulator that provides up to 1A of output current capability with an input voltage ranging from 3V to 18V. The device uses constant frequency peak current mode control architecture for fast loop transient response. The device uses internal compensationor an external Type-II compensation to optimize performance and stabilize the loop. The ISL73006SLH has an internally configured switching frequency of 500kHz. .

The ISL73006SLH integrates high-side (P-channel) and low-side (N-channel) power FETs. There are options for external or internal compensation and slope control that can be implemented with a minimum of external components reducing the BOM count and design complexity.

The ISL73006SLH includes a comprehensive suite of operational features and protections, including preset undervoltage, overvoltage, overcurrent protections, power-good, soft-start, and over-temperature.

The ISL73006SLH operates across the temperature range of -55°C to +125°C and is available in a 10-lead ceramic dual in-line flat package (CDFP) and die form.

Features

- Qualified to Renesas Rad Hard QML-V Equivalent Screening and QCI Flow (R34TB0001EU)
  - All screening and QCI is in accordance with MIL-PRF-38535 Class-V
- Input Bias Voltage
  - 3V to 18V
- Internal or external loop compensation
- 1% reference voltage over-temperature and radiation
- Positive and negative overcurrent, over/undervoltage, and over-temperature protections
- High 500kHz efficiency ~95% from 0.4A to 1A
- Adjustable slope compensation
- TID Rad Hard Assurance (RHA) wafer-by-wafer testing
  - LDR (0.01rad(Si)/s): 75krad(Si)
- SEE Characterization
  - No DSEE for V_{IN} = 16.5 and 86MeV•cm^2/mg
  - SEFI <10µm^2 at 86MeV•cm^2/mg
  - SET <2.5% on V_{OUT} at 86MeV•cm^2/mg

Applications

- Low Power Auxiliary Rails for FPGAs, DSPs, CPUs, and ASICs

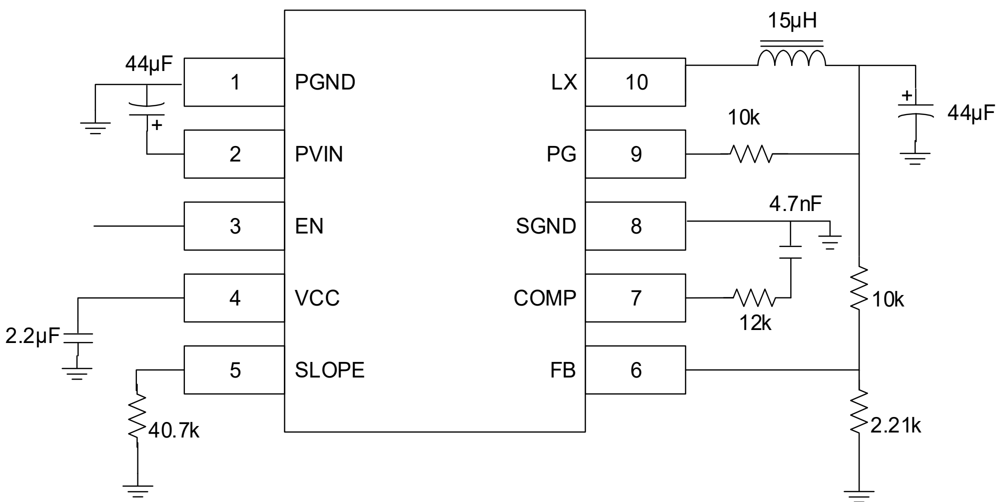


Figure 1. External Compensation Application Diagram for 12V to 3.3V

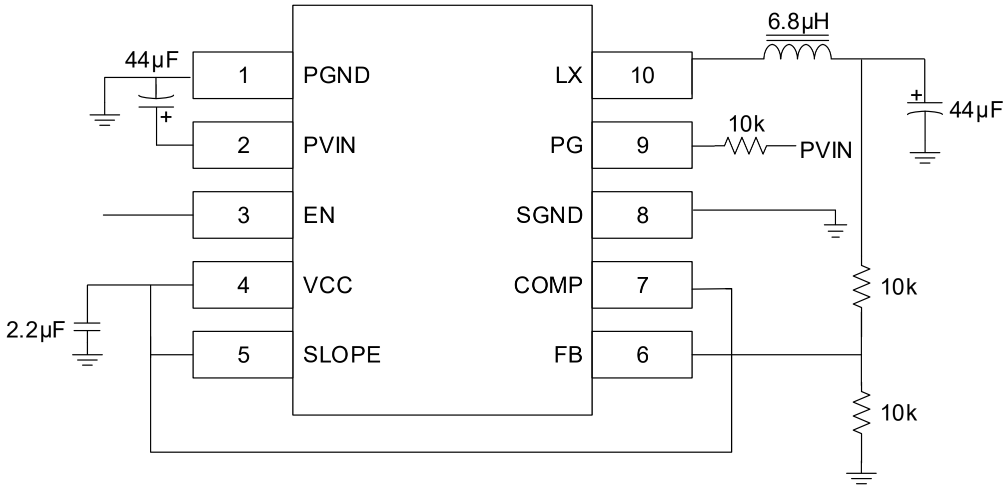


Figure 2. Internal Compensation Application Diagram for 5V to 1.2V

Contents

1. Overview

1.1 Block Diagram

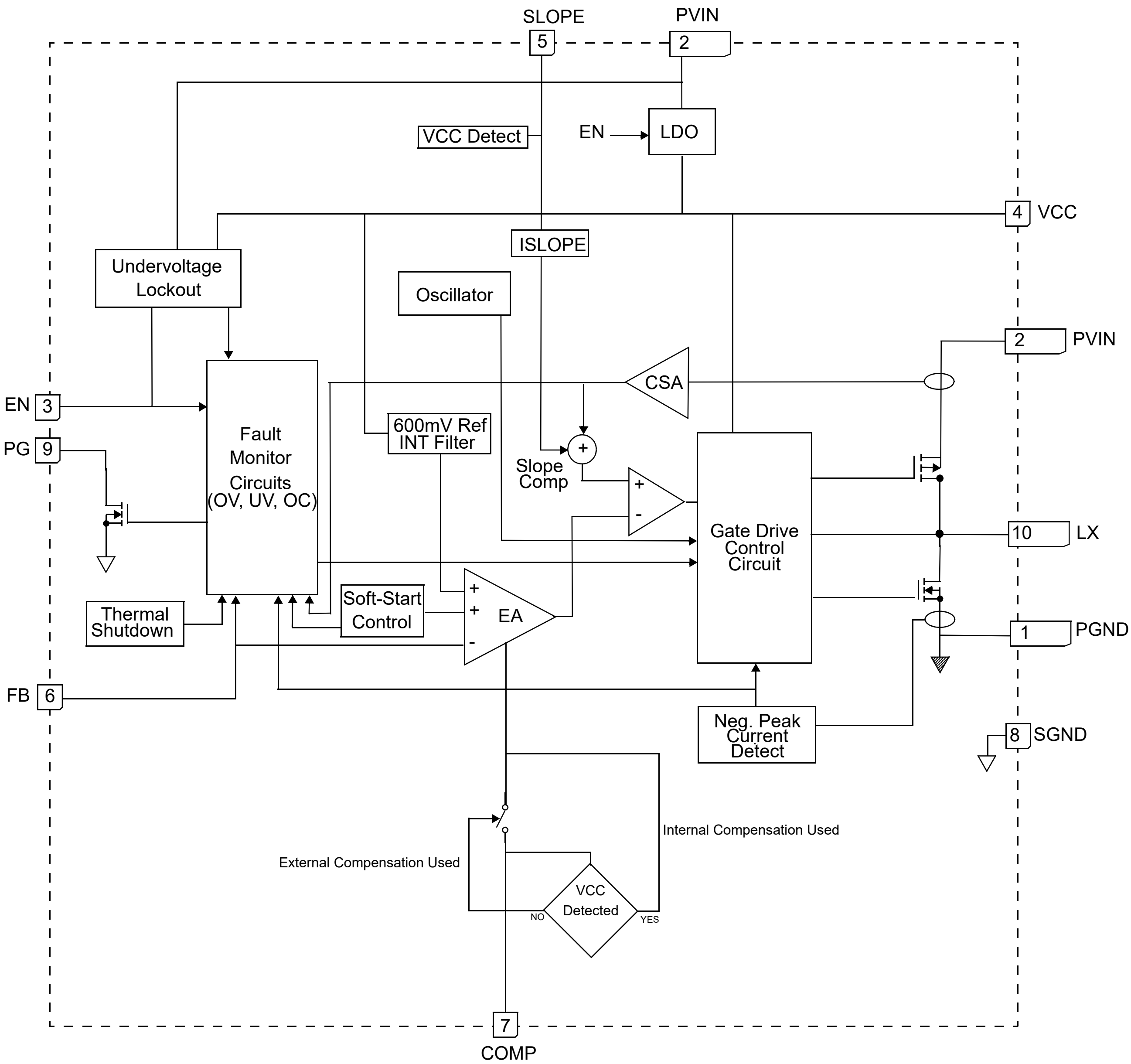


Figure 3. Block Diagram

2. Pin Information

2.1 Pin Assignments

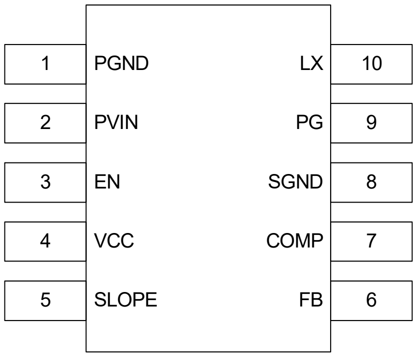


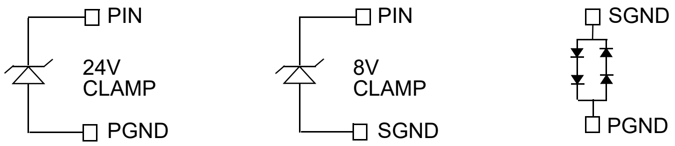
Figure 4. Pin Assignments - Top View

2.2 Pin Descriptions

Pin Number	Pin Name	ESD Circuit	Description
1	PGND	3	Power-ground connection. Ground return for the low-side power MOSFET
2	PVIN	1	Power Input. Supplies the power switches of the buck converter.
3	EN	2	Enable input. This input is a comparator-type input with a rising threshold of 1.2V. Bypass this pin to the PCB ground plane with a 10nF ceramic capacitor to mitigate SEE. This pin can be tied to a maximum of 5V.
4	VCC	2	Linear regulator output from PVIN to provide an internal bias supply rail of up to 5V. Bypass this pin to the PCB ground plane with a 2.2µF ceramic or low ESR Tantalum capacitor for stability, SEE, and noise mitigation. VCC is not intended to bias external circuits
5	SLOPE	2	Slope Compensation. Connect a resistor from this pin to GND to externally set the slope compensation. This pin is a current source of 12µA into the external resistor. Connect the SLOPE pin to VCC to use the default internal slope compensation voltage of 1.2V. If not connected to VCC, add a 1nF capacitor from this pin to ground for SEE mitigation.
6	FB	2	Error Amplifier inverting input. Connect a resistor divider from VOUT to GND with the midpoint driving the FB pin.
7	COMP	2	Error Amplifier output. The external compensation network is connected from this pin to GND. Tie this pin to VCC to use the internal Error Amplifier compensation setup.

Pin Number	Pin Name	ESD Circuit	Description
8	SGND	3	Signal ground. The ground is associated with the internal control circuitry. Connect this pin directly to the PCB ground plane at a single point. Pin 8 is connected to the thermal flash on the package bottom and lid seal ring.
9	PG	1	Power-good output. The pin is an open-drain logic output pulled to SGND when the output is outside of the PGOOD range. The pin can be pulled to any voltage up to the PVIN abs maximum limit. Renesas recommends using a nominal 1kΩ to 10kΩ pull-up resistor. Bypass this pin to the PCB ground plane with a 100pF capacitor for SEE mitigation.
10	LX	N.A.	Switch node connection. Connect this pin to the output filter inductor. Internally, this pin is connected to the common node of the synchronous MOSFET power switches.

ESD Circuits



Circuit 1 Circuit 2 Circuit 3

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
PVIN	PGND - 0.3	+20	V
PVIN[1]	PGND + 3.0	PGND + 16.5	V
SGND	PGND - 0.1	PGND + 0.1	V
FB, COMP, SLOPE	PGND - 0.3	VCC + 0.3	V
EN	PGND - 0.3	5.3	V
PG	PGND - 0.3	PVIN	V
Peak Output Current	-	Overcurrent Protected	A
LX DC Output Current	-	1.13	A
Maximum Junction Temperature	-	+150	°C
Maximum Storage Temperature Range	-65	+150	°C
Human Body Model (Tested per MIL-PRF-883 3015.7)	-	2.5	kV
Charged Device Model (Tested per JS-002-2022)	-	1	kV
Latch-Up (Tested per JESD78E; Class 2, Level A)	-	±100	mA

1. LET = 86MeV•cm^2/mg at 125°C (T_C)

3.2 Thermal Information

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	10 Ld CDFP Package	θ_{JA}[1]	Junction to ambient	31	°C/W
		θ_{JC}[2]	Junction to case	6	°C/W

1. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.

2. For θ_{JC}, the case temperature location is the center of the metallization on the package underside.

3.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Input Voltage (PVIN)	PGND + 3.0	+18	V
Output Current	0	1	A
External R_{SLOPE} Resistor	25	100	kΩ
Ambient Temperature	-55	+125	°C
Junction Temperature	-55	+150	°C
Output Voltage	0.6	Limited by min on/off timing constraints & f_{SW}	V

3.4 Electrical Specifications

Unless otherwise noted, PVIN = 3V and 18V; PGND = SGND = 0V; LX = Open Circuit; PGOOD is pulled up to PVIN with a 10k resistor; I_{OUT} = 0A; $T_J = T_A$, $r_{DS(ON)}$ is pulse tested. **Boldface limits apply across the operating temperature range, -55°C to +125°C by production testing; over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s.**

Parameter	Symbol	Test Conditions	Temp. (°C)	Min	Typ[1]	Max	Unit
Input Power Supply							
Rising Undervoltage Lockout	V_{PVIN_UVLO}	EN = 2.25V	-55 to +125	-	2.86	**2.95**	V
Falling Undervoltage Lockout		EN = 2.25V	-55 to +125	**2.7**	2.78	-	V
Operating Supply Current	I_{PVIN_OPER}	PVIN = 3V, EN = 2.25V, no load	-55 to +125	**2**	-	**6**	mA
		PVIN = 12V, EN = 2.25V, no load	-55 to +125	**5**	-	**12**	mA
		PVIN = 18V, EN = 2.25V, no load	-55 to +125	**5**	-	**12.5**	mA
Stand-by Supply Current	I_{PVIN_SB}	PVIN = 3V, EN = 1V	-55 to +125	**1.05**	1.31	1.5	mA
		PVIN =18V, EN = 1V	-55 to +125	**1**	1.22	**1.4**	
Shutdown Supply Current	I_{PVIN_SD}	PVIN = 3V, EN = 0V	-55 to +125	**5**	19	**30**	µA
		PVIN = 18V, EN = 0V	-55 to +125	**75**	111	**190**	
Output Regulation							
Feedback Voltage Accuracy[2]	V_{FB}	VFB (including Error Amplifier V_{IO} to SGND)	-55	593.5	597	600	mV
			+25	596	600	603	
			+125	596	600	603	
			+25 (Post Rad)	596	601	603.5	
FB Leakage Current[2]	I_{FB}	PVIN = 12V, V_{FB} = 0.6V	-55	-20	0.492	20	nA
			+25	-20	0.49	20	
			+125	-20	1.767	20	
			+25 (Post Rad)	-20	0.49	20	
Output Voltage Tolerance Over Input Voltage Range	LNREG	PVIN = 3V, 18V using servo loop	-55 to +125	**-0.11**	0.039	**0.25**	%
Protection Features							
Positive Peak Current Limit[3]	$I_{IPLIMIT1}$	PVIN = 3.2V	-55 to +125	**1.5**	2	**2.6**	A
		PVIN ≥ 5V	-55 to +125	**1.4**	1.9	**2.4**	
	$I_{IPLIMIT2}$	PVIN = 18	-55 to +125	**1.7**	2.2	**2.6**	
Negative Peak Current Limit[3]	$-I_{IPLIMIT}$	-	+25	-2.0	-1.6	-1.3	A
			-55 to +125	**-2.0**	-1.7	**-1.3**	
Thermal Shutdown[4]	$Therm_{SD}$	Die Rising Temperature Threshold	-	-	161	-	°C
Thermal Reset[4]	$Therm_{SD}$	Die Falling Temperature Threshold	-	-	148	-	°C

Unless otherwise noted, PVIN = 3V and 18V; PGND = SGND = 0V; LX = Open Circuit; PGOOD is pulled up to PVIN with a 10k resistor; I_{OUT} = 0A; T_J = T_A, $r_{DS(ON)}$ is pulse tested. **Boldface limits apply across the operating temperature range, -55°C to +125°C by production testing; over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s. (Cont.)**

Parameter	Symbol	Test Conditions	Temp. (°C)	Min	Typ[1]	Max	Unit
Thermal Shutdown Hysteresis[4]	$Therm_{SDHYS}$	-	-	-	-	20	°C
Compensation							
Internal Error Amplifier Output Transconductance [4]	$EA_{transcon1}$	Internal Compensation Configuration R_{COMP} = 1MΩ, C_{COMP} = 50pF	+25	-	0.022	-	mA/V
Internal Error Amplifier Zero [4]	EA_{fz}	f_z = gm_integrater/(2pi(R2/R1)Ccomp)	+25	-	4.1	-	kHz
Internal Error Amplifier Gain-Bandwidth Product[4]	EA_{GBP1}	-	+25	-	33	-	MHz
Internal Error Amplifier DC Gain[4]	EA_{AV1}	1Hz	+25	55.3	82	-	dB
			+125	58.5	82	-	dB
External Error Amplifier Transconductance	$EA_{transcon2}$	PVIN = 5V, delta COMP current/delta FB Voltage (10mV)	-55	0.93	1.057	1.18	mA/V
			+25	0.82	0.923	1.02	mA/V
			+125	0.68	0.768	0.87	mA/V
External Error Amplifier DC Gain[4]	EA_{AV2}	1Hz	+25	66	80	-	dB
External Error Amplifier Gain-Bandwidth Product[4]	EA_{GBP2}	-	+25	15	-	-	MHz
Oscillator/Slope Generator							
Switching Frequency	f_{SW}	V_{SLOPE} = 1.2V	-55 to +125	**450**	500	**550**	kHz
SLOPE Pin Current Source	I_{SLOPE}	-	-55 to +125	**10.5**	12	**13.5**	µA
Internal SLOPE Ramp Rate	t_{SLOPE}	(V_{COMP} at 80%DC - V_{COMP} at 20%DC)/ (t_{MIN_ON}at80%DC - t_{MIN_ON} at 20%DC)	-55 to +125	**0.1**	0.13	**0.16**	V/µs
Enable							
Rising Enable Voltage Threshold	EN_{VIH}	Enable Rising to LX Switching	-55 to +125	**1.18**	1.21	**1.3**	V
Falling Enable Voltage Threshold	EN_{VIL}	Enable Falling to LX Stops Switching	-55 to +125	**0.96**	1	**1.06**	V
Enable Voltage LX Hysteresis	EN_{VIHhys}	Enable Rising to LX Switching - Enable Falling to LX Stop switching	-55 to +125	**20**	200	**410**	mV
Standby Enable Voltage	SB_EN_{VIH}	Enable Rising to VCC Enabled	-55 to +125	**0.45**	0.76	**1**	V

Unless otherwise noted, PVIN = 3V and 18V; PGND = SGND = 0V; LX = Open Circuit; PGOOD is pulled up to PVIN with a 10k resistor; I_{OUT} = 0A; T_J = T_A, $r_{DS(ON)}$ is pulse tested. **Boldface limits apply across the operating temperature range, -55°C to +125°C by production testing; over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s. (Cont.)**

Parameter	Symbol	Test Conditions	Temp. (°C)	Min	Typ[1]	Max	Unit
Shutdown Enable Voltage	SB_EN_{VIL}	Enable Falling to VCC Disabled	-55 to +125	**0.3**	0.68	**0.9**	V
Enable Hysteresis Voltage	EN_{HYS}	Enable Rising to LX Switching - EN Falling to VCC Disable	-55 to +125	**20**	80	**175**	mV
Low Enable Current	EN_{IIL}	Enable = 0V	-55 to +125	**-20**	0.426	**20**	nA
High Enable Current	EN_{IIH}	Enable = 5V	-55 to +125	**1.7**	2.4	**3.1**	µA
Enable (EN) Pull-Down Resistance	R_{EN}	PVIN = 12V	-55 to +125	**1.7**	2.3	**2.9**	MΩ
VCC							
VCC Output Voltage	$VOUT_{3V,0mA}$	PVIN = 3V, I_{OUT} = 0mA	-55 to +125	**2.96**	2.99	**3**	V
	$VOUT_{3V,10mA}$	PVIN = 3V, I_{OUT} = 10mA	-55 to +125	**2.93**	2.97	**2.98**	
	$VOUT_{5.5V,0mA}$	PVIN = 5.5V, I_{OUT} = 0mA	-55 to +125	**4.83**	4.95	**5**	
	$VOUT_{5.5V,10mA}$	PVIN = 5.5V, I_{OUT} = 10mA	-55 to +125	**4.82**	4.94	**5**	
VCC Foldback Current	I_{CC_SC}	PVIN = 18V, V_{CC} = 0V, EN = 1.6V	-55 to +125	**40**	72	**90**	mA
VCC Overcurrent Limit	I_{CC_CL}	PVIN = 18V, V_{CC} = 4.3V, EN = 1.6V	-55 to +125	**75**	98	**130**	mA
Power-Good							
Output Overvoltage Error Threshold	OVPG	PVIN = 5V, FB as a % of V_{REF}	-55 to +125	**106.25**	107.1	**108.25**	%
Output Undervoltage Error Threshold	UVPG	PVIN = 5V, FB as a % of V_{REF}	-55 to +125	**92.7**	92.3	**94.7**	%
Output Overvoltage Fault	OVflt	PVIN = 5V, FB as a % of V_{REF}	-55 to +125	**113.5**	115	**117.25**	%
Output Undervoltage Fault	UVflt	PVIN = 5V, FB as a % of V_{REF}	-55 to +125	**82.5**	85	**87**	%
Low Current Drive	PG_I_{OL}	PVIN = 3V, PG = 0.4V, EN = 0V	-55 to +125	**11**	22	**35**	mA
Low V_{OUT}	PG_V_{OL}	PVIN = 18V, FB = 0V, EN = 0V, IPG = 10mA	-55 to +125	**-**	0.15	**0.27**	V
Leakage	I_{LKGPG}	PVIN = PG = 18V	-55 to +125	**-**	-	**1**	µA
Power Good Rising Delay	$t_{SSPGdlyr}$	PVIN = 5.5V From EN edge to PG high	-55 to +125	**6.6**	7.4	**8.4**	ms
Rising Edge Delay	t_{PGdlyr}	Return to regulation to PG response	-55 to +125	**1.9**	3	**4.2**	µs
Falling Edge Delay	t_{PGdlyf}	Out of regulation to PG response	-55 to +125	**3.5**	4.3	**5**	µs

Unless otherwise noted, PVIN = 3V and 18V; PGND = SGND = 0V; LX = Open Circuit; PGOOD is pulled up to PVIN with a 10k resistor; I_{OUT} = 0A; T_J = T_A, $r_{DS(ON)}$ is pulse tested. **Boldface limits apply across the operating temperature range, -55°C to +125°C by production testing; over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s. (Cont.)**

Parameter	Symbol	Test Conditions	Temp. (°C)	Min	Typ[1]	Max	Unit
Phase							
Minimum LX On-Time[5]	t_{MIN_ON}	PVIN = 12V, Forced Min On-Time by COMP bias, No Load	-55 to +125	-	230	**280**	ns
Minimum LX Off-Time[5]	t_{MIN_OFF}	PVIN = 12V, Forced Min Off-Time by COMP bias, No Load	-55 to +125	-	171	**210**	ns
CDFP Upper FET $r_{DS(ON)}$[2][3]	$-55UPR_{DSON\_3}$	PVIN = 3.0V, I_{OUT} = 200mA	-55	235	280	320	mΩ
	$-55UPR_{DSON\_5}$	PVIN = 5.5V, I_{OUT} = 200mA		190	236	275	
	$25UPR_{DSON\_3}$	PVIN = 3.0V, I_{OUT} = 200mA	+25	320	370	410	
	$25UPR_{DSON\_5}$	PVIN = 5.5V, I_{OUT} = 200mA		255	305	360	
	$125UPR_{DSON\_3}$	PVIN = 3.0V, I_{OUT} = 200mA	+125	435	495	550	
	$125UPR_{DSON\_5}$	PVIN = 5.5V, I_{OUT} = 200mA		350	405	460	
Post Rad CDFP Upper FET $r_{DS(ON)}$[2][3]	$25UPR_{DSON\_3}$	PVIN = 3.0V, I_{OUT} = 200mA	+25 (Post Rad)	320	-	440	mΩ
	$25UPR_{DSON\_5}$	PVIN = 5.5V, I_{OUT} = 200mA		255	-	390	
CDFP Lower FET $r_{DS(ON)}$[2][3]	$-55LWR_{DSON\_3}$	PVIN = 3.0V, I_{OUT} = 200mA	-55	105	139	175	mΩ
	$-55LWR_{DSON\_5}$	PVIN = 5.5V, I_{OUT} = 200mA		100	122	150	
	$25LWR_{DSON\_3}$	PVIN = 3.0V, I_{OUT} = 200mA	+25	165	203	240	
	$25LWR_{DSON\_5}$	PVIN = 5.5V, I_{OUT} = 200mA		155	178	205	
	$125LWR_{DSON\_3}$	PVIN = 3.0V, I_{OUT} = 200mA	+125	270	312	350	
	$125LWR_{DSON\_5}$	PVIN = 5.5V, I_{OUT} = 200mA		240	274	310	
Post Rad CDFP Lower FET $r_{DS(ON)}$[2][3]	$25LWR_{DSON\_3}$	PVIN = 3.0V, I_{OUT} = 200mA	+25 (Post Rad)	165	-	240	mΩ
	$25LWR_{DSON\_5}$	PVIN = 5.5V, I_{OUT} = 200mA		155	-	205	
DIE Upper FET $r_{DS(ON)}$[3]	$25DUPR_{DSON\_3}$	PVIN = 3.0V, I_{OUT} = 200mA	+25	290	309	355	mΩ
	$25DUPR_{DSON\_5}$	PVIN = 5.5V, I_{OUT} = 200mA		225	244	300	
DIE Lower FET $r_{DS(ON)}$[3]	$25DLWR_{DSON\_3}$	PVIN = 3.0V, I_{OUT} = 200mA		140	159	190	mΩ
	$25DLWR_{DSON\_5}$	PVIN = 5.5V, I_{OUT} = 200mA		120	134	160	

1. Typical values are at 25°C and are not guaranteed.
2. Typical values shown are at stated temperature and are not guaranteed.
3. Parameter tested in a Test Mode not available to user.
4. Limits established by characterization and/or design analysis and are not production tested.
5. The operating envelope may be reduced by Minimum On-Time and Minimum Off Time constraints.

3.5 Operation Burn-In Deltas

Unless otherwise noted, PVIN = 12V and 18V; PGND = SGND = 0V; LX = Open Circuit; PGOOD is pulled up to PVIN with a 10k resistor; I_{OUT} = 0A; T_J = T_A = 25°C.

Parameter[1]	Symbol	Test Conditions	Min	Max	Unit
Operating Supply Current	I_{PVIN_OPER}	PVIN = 18V, EN = 5V, 500kHz, no load	-2	+2	mA
Shutdown Supply Current	I_{PVIN_SD}	PVIN = 18V, EN = 0V	-25	+25	µA
Reference Voltage Tolerance	V_{FB}	PVIN = 18V, V_{FB} (including Error Amplifier V_{IO} to SGND)	-2.35	+2.35	mV
Positive Peak Current Limit	$I_{IPLIMIT1}$	PVIN = 12	-0.5	+0.5	A
Switching Frequency	f_{SW5}	PVIN = 12	-10	+10	kHz
V_{CC} Output Voltage	$VOUT_{5.5V,10mA}$	PVIN = 5.5V, I_{OUT} = 10mA	-0.015	+0.015	V
SLOPE Pin Current Source	I_{SLOPE}	PVIN = 12	-0.2	+0.2	µA

1. This data table shows the delta limits of critical parameters after 2000hrs of HTOL at 135°C.

4. Typical Performance Curves

T_A = Room ambient, unless otherwise noted

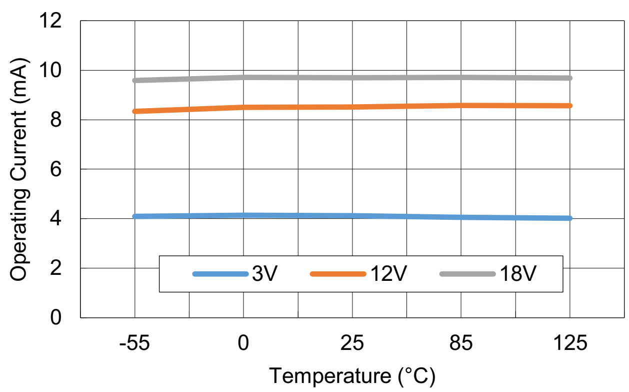


Figure 5. Operating Supply Current vs Temperature

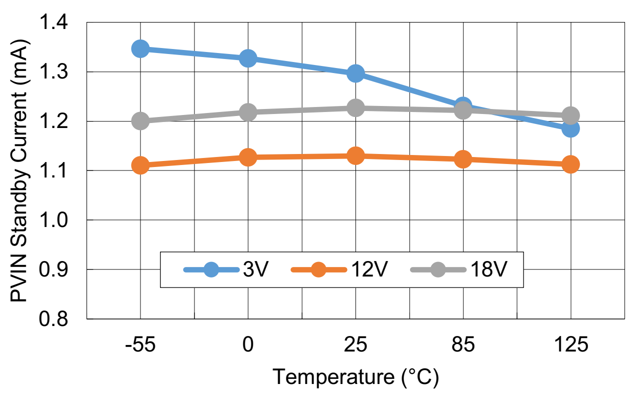


Figure 6. Standby Current vs Temperature

T_A = Room ambient, unless otherwise noted (Cont.)

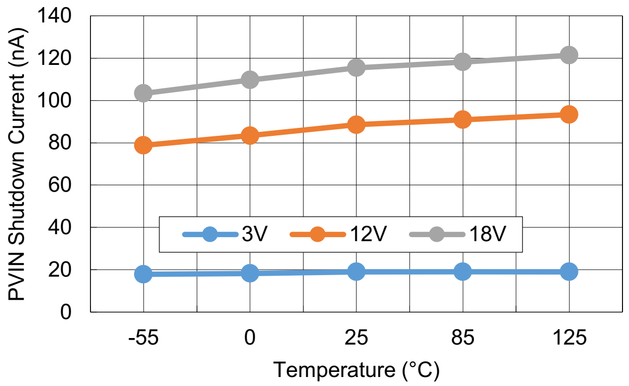


Figure 7. Shutdown Current vs Temperature

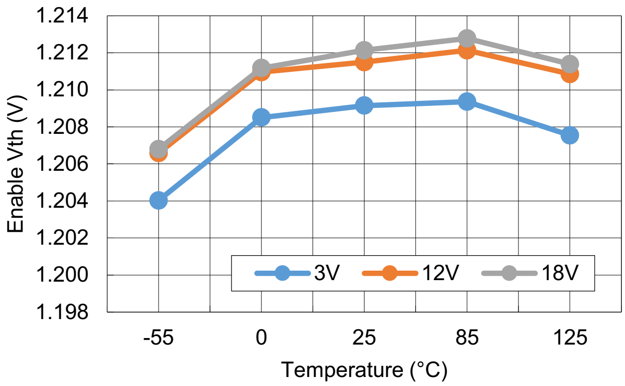


Figure 8. Enable Threshold to LX Switching vs Temperature

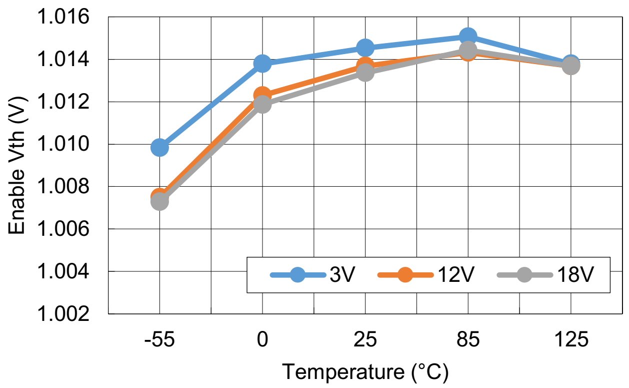


Figure 9. Enable Threshold to LX Stop vs Temperature

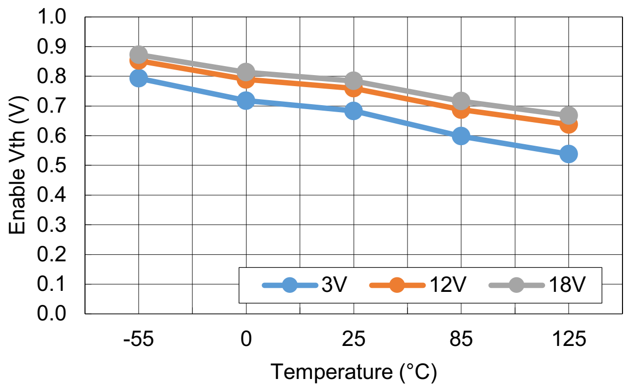


Figure 10. Enable Threshold to VCC ON vs Temperature

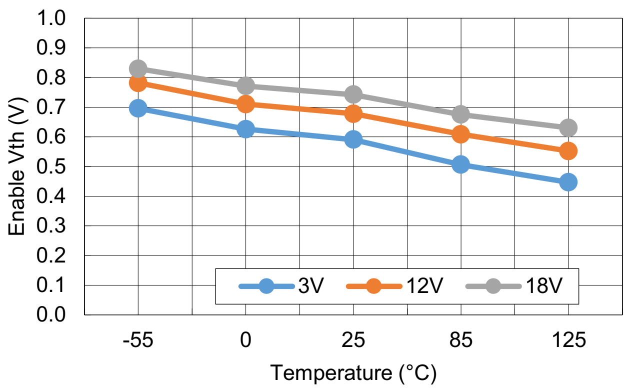


Figure 11. Enable Threshold to VCC OFF vs Temperature

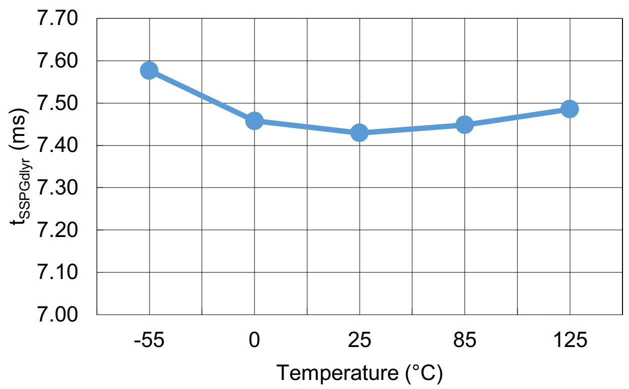


Figure 12. Enable to PGOOD Soft-Start vs Temperature

T_A = Room ambient, unless otherwise noted (Cont.)

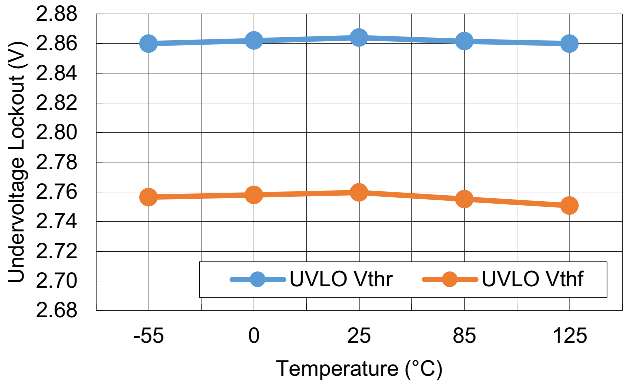


Figure 13. Undervoltage Lockout vs Temperature

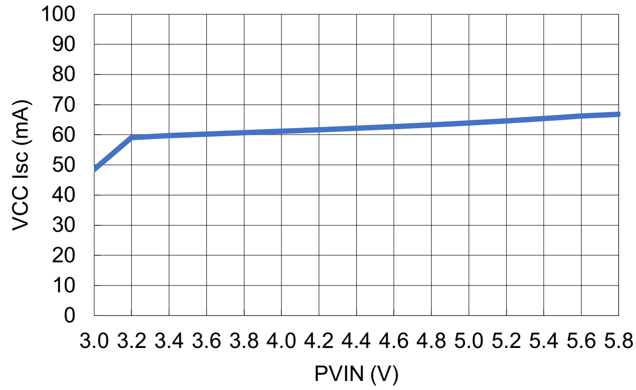


Figure 14. VCC Isc vs PVIN

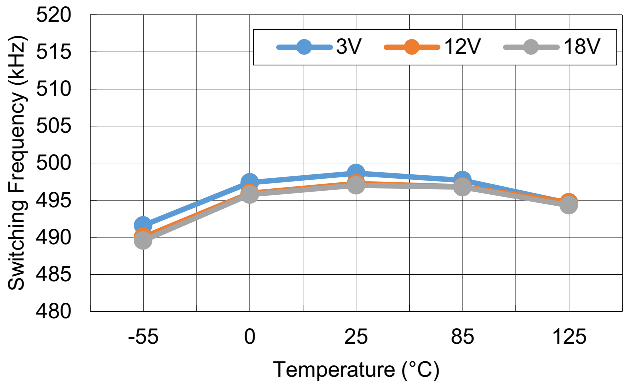


Figure 15. Switching Frequency vs Temperature

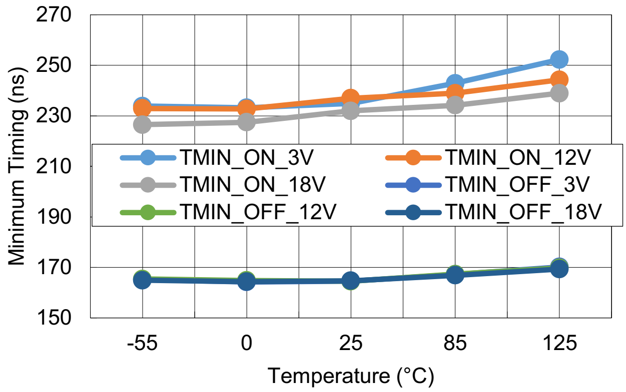


Figure 16. Minimum ON/OFF-Time vs Temperature

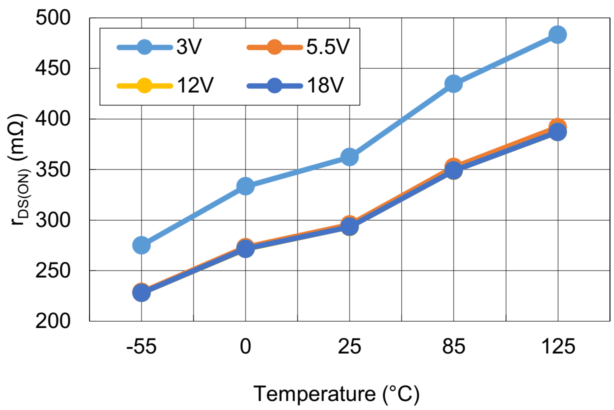


Figure 17. Upper FET $r_{DS(ON)}$ vs Temperature

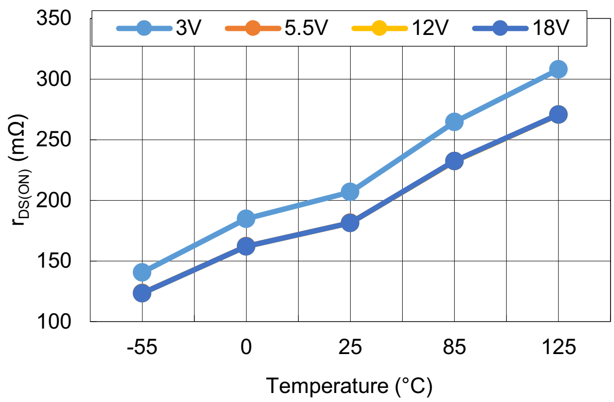


Figure 18. Lower FET $r_{DS(ON)}$ vs Temperature

T_A = Room ambient, unless otherwise noted (Cont.)

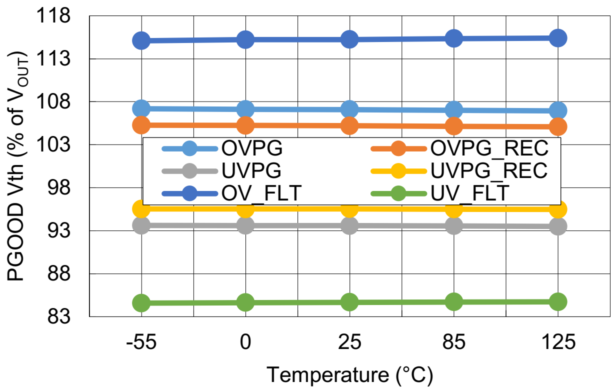


Figure 19. PGOOD Vth vs Temperature

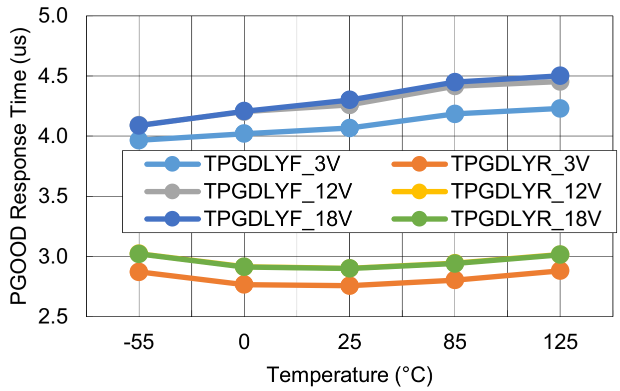


Figure 20. PGOOD Response Time vs Temperature

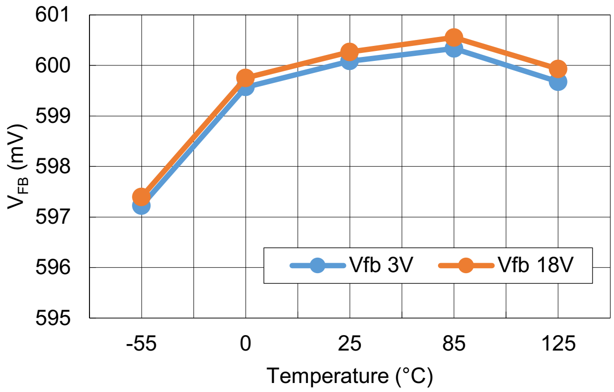


Figure 21. FB Voltage vs Temperature

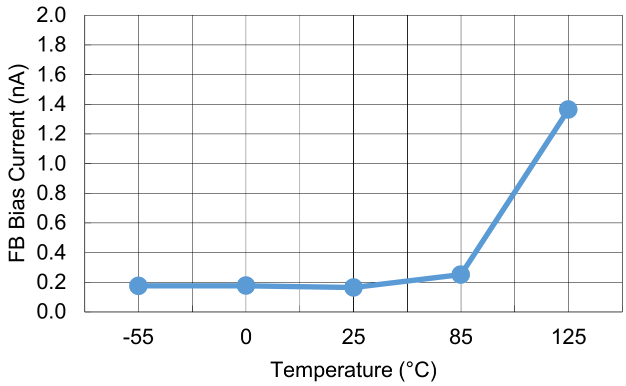


Figure 22. FB Bias Current vs Temperature

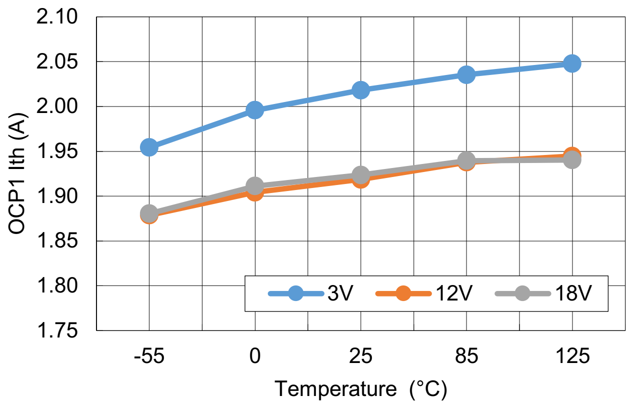


Figure 23. Operating Overcurrent Protection vs Temperature

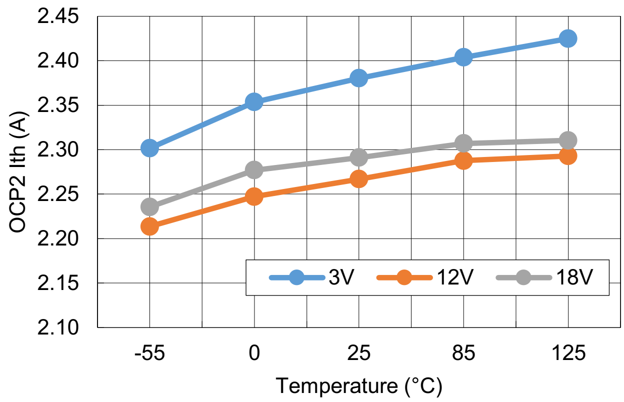


Figure 24. Additional Current Protection During Soft-Start vs Temperature

T_A = Room ambient, unless otherwise noted (Cont.)

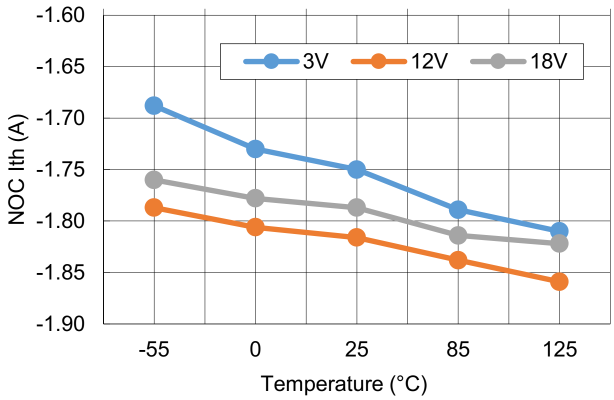


Figure 25. Negative Overcurrent Protection vs Temperature

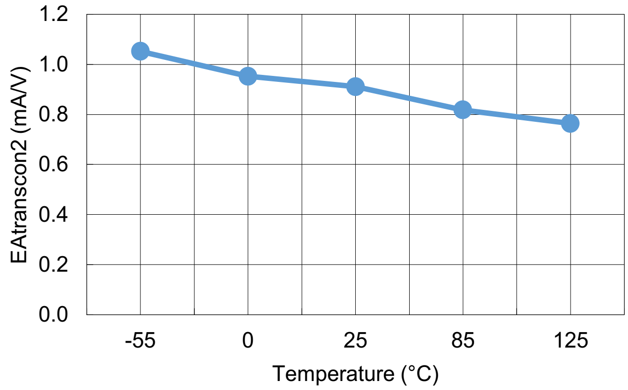


Figure 26. External Error Amp Transconductance vs Temperature

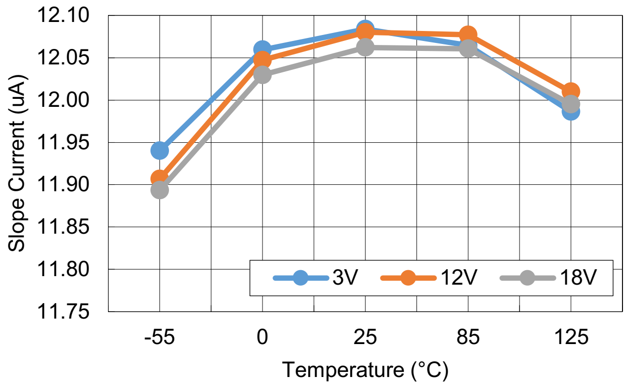


Figure 27. SLOPE Current vs Temperature

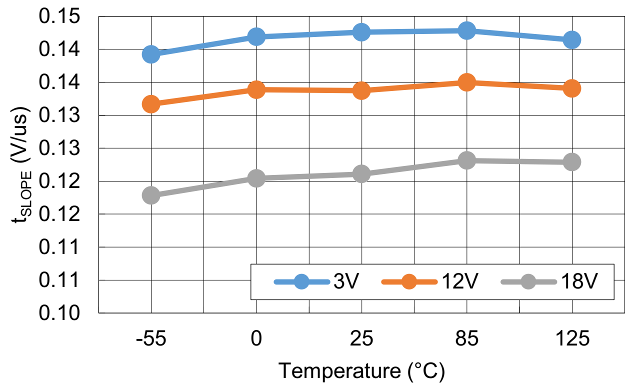


Figure 28. Slope Ramp Rate vs Temperature

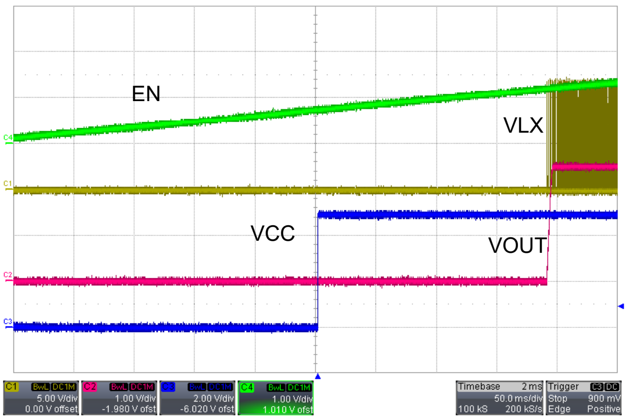


Figure 29. ENABLE to VCC to LX and VOUT Turn-On

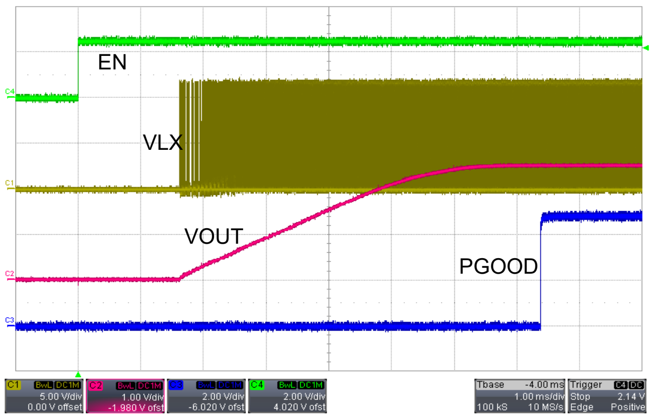


Figure 30. ENABLE to LX and VOUT to PGOOD

T_A = Room ambient, unless otherwise noted (Cont.)

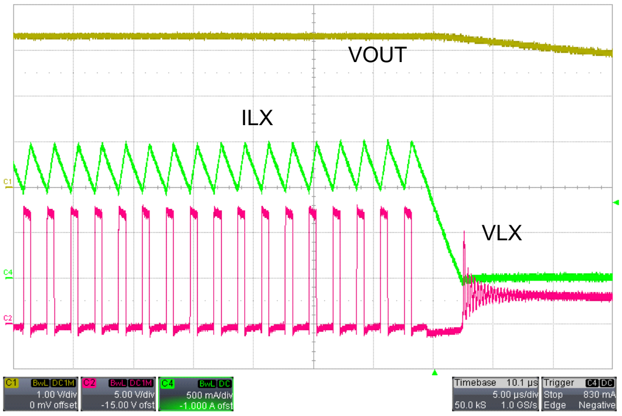


Figure 31. Overcurrent Protection Function

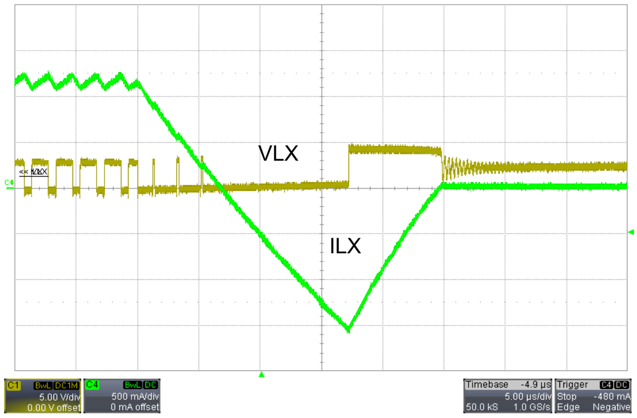


Figure 32. Negative Overcurrent Protection Function

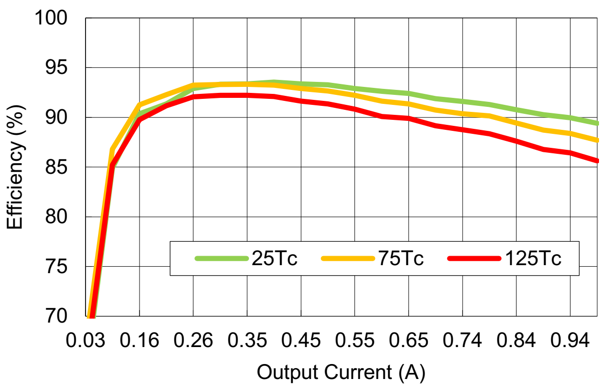


Figure 33. Efficiency 5V_{IN} to 2.5V_{OUT} vs Case Temp

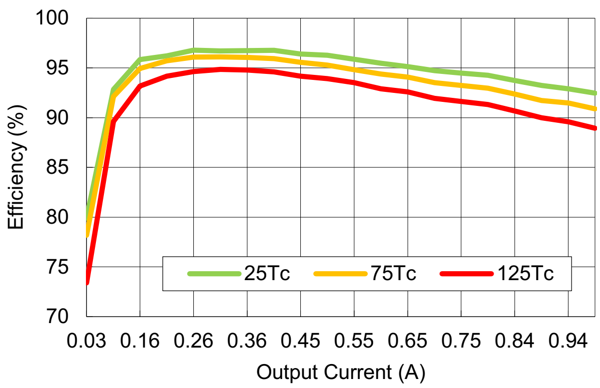


Figure 34. Efficiency 5V_{IN} to 3.3V_{OUT} vs Case Temp

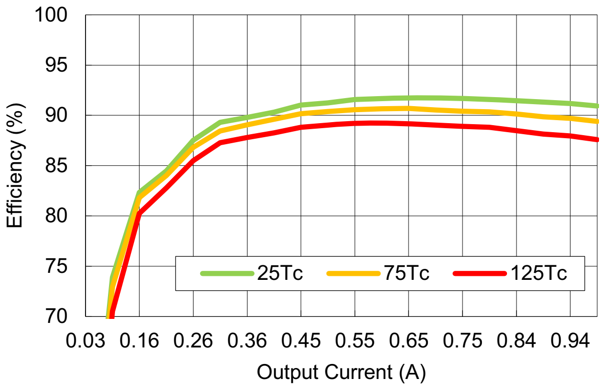


Figure 35. Efficiency 12V_{IN} to 3.3V_{OUT} vs Case Temp

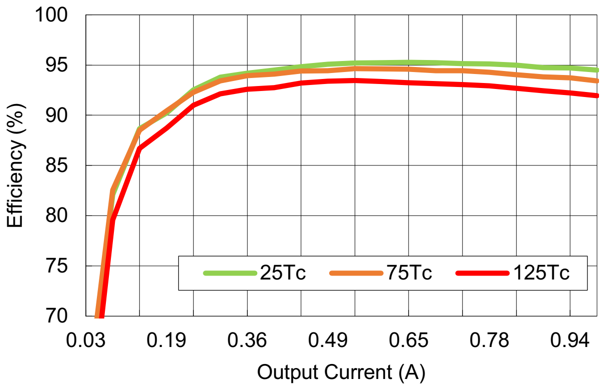


Figure 36. Efficiency 12V_{IN} to 5V_{OUT} vs Case Temp

T_A = Room ambient, unless otherwise noted (Cont.)

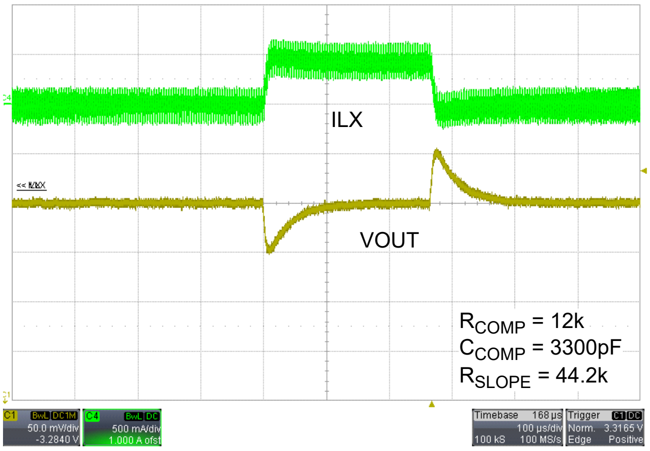


Figure 37. External Comp Current Transient
$12V_{IN}$, $3.3V_{OUT}$, I_{OUT} Step = 0.45A

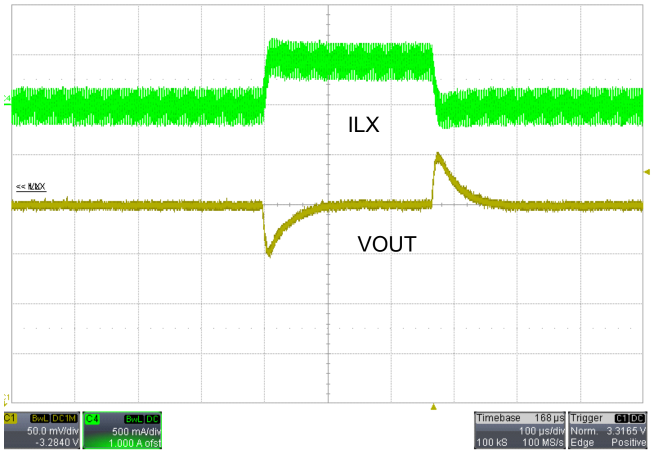


Figure 38. Internal Comp Current Transient
$12V_{IN}$, $3.3V_{OUT}$, I_{OUT} Step = 0.45A

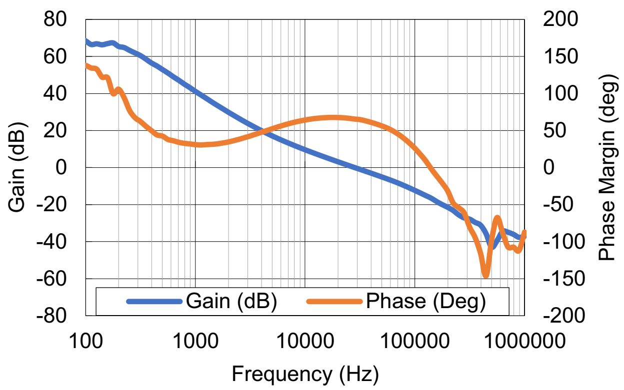


Figure 39. External Comp Gain/Phase BODE Plot,
$12V_{IN}$, $3.3V_{OUT}$
(R_{COMP} = 12k, C_{COMP} = 3300pF, R_{SLOPE} = 44.2k)

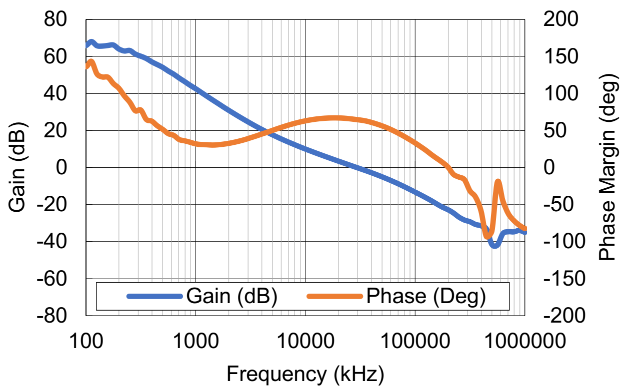


Figure 40. Internal Comp Gain/Phase BODE Plot,
$12V_{IN}$, $3.3V_{OUT}$

5. Theory of Operation

5.1 Description of Features

The ISL73006SLH is a Radiation Hardened by design buck converter using constant frequency peak current mode control architecture for fast loop transient response with a 3V to 18V input voltage regulating down to a minimum 0.6V output voltage adjusted using external resistors. The ISL73006SLH is capable of ~95% efficiency from 0.4A to the 1A maximum output rated current.

The ISL73006SLH can be configured such that the loop and slope compensations can either be defaulted to internal attributes by tying pins to the VCC or be adjusted externally with passive components to meet particular design requirements and performance optimization. These features can be mixed externally or internally when implemented. This flexibility allows for a basic functional configuration with a minimal BOM or an optimized configuration for the POL task.

5.2 Output Voltage Setting

Use Equation 1 to calculate the required regulated output voltage. For greater voltage accuracy, Renesas recommends using 0.1% feedback resistors.

(EQ. 1)

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_2}{R_1}\right)$$

- V_{OUT} is the required regulated output voltage.
- V_{REF} is the internal reference voltage on the VFB+ pin, which is 0.6V (typical).
- R_1 is the bottom resistor in the feedback divider.
- R_2 is the top resistor in the feedback divider.

5.3 Internal Configuration Summary Description

The ISL73006SLH loop and slope compensations can be configured entirely internally or partially internally with either of the adjustable attributes. The corresponding COMP and SLOPE pins are connected to VCC to configure each of these internally. Tying COMP to VCC configures an internal compensation optimized for <2% transient response for the 0.5A current step.

Internal compensation has the additional benefit of significantly reducing Single Event Transients (SET) compared to external compensation.Tying SLOPE to VCC selects the internal slope compensation with 250mV/T slew rate ($T = 1/f_{SW}$).

5.4 External Configuration Summary Description

You can individually configure the ISL73006SLH loop and slope compensation externally.

After you choose the external loop compensation, connect a Type II compensation network between the COMP pin and the neighboring SGND pin.

You can select the external slope compensation by tying a resistor from the SLOPE pin to ground. The SLOPE pin forces 12µA of current into the R_{SLOPE} resistor ($25k\Omega \le R_{SLOPE} \le 100k\Omega$), which sets the voltage reference for the internal slope. A 100kΩ resistor sets a maximum 250mV/T compensation slew rate, while a 25kΩ resistor sets a minimum 62.5mV/T slew rate.

5.5 Time Constraints on DC/DC Voltage Conversion

The ISL73006SLH can operate across wide ranges of both input and output voltages; however, the step-down conversion has to adhere to the minimum off and minimum on timing requirements. You can simply determine the down conversion suitability by comparing the t_{ON} and t_{OFF} specifications to the duty cycle high time and low time, respectively, for the intended duty cycle. The timing constraints mostly impact extremely high or low-duty cycle conversions where the minimum off and on times are infringed up. Changing PVIN is the simple method to alleviate minimum on-time and off-time concerns.

5.6 Overcurrent Protection

Overcurrent protection (OCP) is provided for the sourcing and sinking output current conditions. An accurate current-sensing pilot device parallel to the upper MOSFET is used for peak current control signal and overcurrent protection. Current is sensed and monitored on the output current ripple at the most positive peak and negative valley amplitudes for the sourcing and sinking conditions. An excessive ripple current lowers the DC output current capability because of the peak detection used for OCP. OCP is triggered if the OCP threshold is exceeded in four of the eight preceding switching periods. On the 4th current peak above the OCP threshold, the device enters the fault state, stops switching, and the output is pulled low by the output loading. The device attempts to turn on again in a hiccup mode, and when the overcurrent condition goes away, the output soft starts again into a regulated output voltage. The typical sourcing OCP threshold is invoked at less than 2x the rated output current of 1A, providing headroom for the peak ripple current.

During the soft-start period, there is an additional level of overcurrent protection of a single instance at ~2A to protect against shorted or otherwise damaged loads. When invoked, this fault goes into hiccup restart cycling until a successful restart occurs.

5.7 Negative Overcurrent Protection (NOCP)

If an external source drives current into the VOUT pin, the controller attempts to regulate the output voltage by reversing its inductor current to absorb the externally sourced current. If the external source is low-impedance, it might reverse the current to an unacceptable level, and the controller initiates its negative overcurrent limit protection. The negative overcurrent protection is realized by monitoring the current through the lower FET. When the valley point of the inductor current reaches the negative current limit of typically -1.8A, the NOCP fault is declared, and the LX out goes into a high-Z state. The IC enters into a hiccup mode to restart. There is no valley current counter on the NOCP function.

5.8 Power Good

Power-Good (PG) is the output of a window comparator that continuously monitors the buck regulator output voltage. The PG output is actively held low when EN is low and during the buck regulator soft-start period. After soft-start completes, the PG pin becomes high impedance as long as the output voltage is in nominal regulation of the output voltage. When VFB is typically beyond ±6% of the nominal regulation voltage for ~5µs, the device open drain output pulls the PG output low. Add an external resistor from PG to a maximum of the PVIN voltage for PG signaling purposes.

5.9 UVLO, Enable, Soft-start, Disable and Soft-Stop

When PVIN is below the Undervoltage Lockout (UVLO) threshold, the regulator is inert until PVIN rises above the UVLO voltage of ~2.86V. The ISL73006SLH Enable pin provides three states of operation. Below the standby threshold (typically 0.68V), the ISL73006SLH is disabled and draws a typical 105µA from PVIN. The VCC LDO can start up with the EN pin between a typical 1.0V and 1.2V, and the part enters a standby state. Normal switching operation and soft-start begin when the EN pin is over 1.2V.

During startup, the ISL73006SLH critiques for Overvoltage (OV) and Over-Temperature (OT) faults and remains idle if either fault is active. The soft-start time relates to the operating switching frequency during startup. There is a delay from enable active to LX activity during which the ISL73006SLH internal circuitries are biased. The ISL73006SLH can seamlessly start into a pre-biased output, provided the output voltage is below the set regulation voltage. If the pre-biased output exceeds the regulation set point, the ISL73006SLH does not initiate LX switching but turns on the low-side MOSFET to pull the output down. Suppose the sinking output current reaches the negative output current limit (NOCL). In that case, it enters hiccup operation until the output is below the regulation set point and then proceeds through soft-start to LX switching. If the sinking output current does not reach the NOCL, the ISL73006SLH initiates soft-start when VOUT is pulled below the regulation set point. The device is disabled and enters the low current shutdown state when EN is < 0.3V. When a transition to a shutdown state occurs, the LX output is forced to a hi-Z state.

5.10 Thermal Protection

The device has integrated thermal protection. When the internal temperature reaches ~ +158°C, the regulator stops switching. After the internal temperature falls below ~ +130°C, the device resumes operation through soft-start. For continuous operation, do not exceed the +150°C junction temperature rating.

5.11 PWM Control and Compensation

The ISL73006SLH employs constant frequency peak current-mode pulse-width modulation (PWM) control for faster transient response and pulse-by-pulse current limiting. The current loop consists of the current-sensing circuit, slope compensation ramp, and PWM comparator.

Any regulator design starting point is knowing the operating conditions and design goals. These would include the input and output voltages, the switching frequency, the maximum transient current step, and the maximum transient output voltage tolerance. The following compensation equations guide completing an external slope and loop control compensation design.

5.12 Slope Compensation

The ISL73006SLH offers user-adjustable slope compensation using a resistor (R_{SLOPE}) from the SLOPE pin to ground to optimize the device performance and stability across the entire PWM duty-cycle range. Slope compensation is a technique in which the current feedback signal is modified by adding slope, that is, a linearly increasing voltage over time. You can set the external slope compensation ramp with a resistor from the slope pin to ground.

For applications with a maximum duty cycle of less than 50%, slope compensation can improve noise immunity, particularly at lighter loads. For applications with a greater than 50% duty cycle, you need slope compensation to prevent instability, seen as a sub-harmonic oscillation of the switching LX node. The minimum slope compensation required is $-V_{OUT}/2 \times$ output inductor (L_{OUT}).

5.13 External Configuration Application Implementation Equations

This section guides the design for the slope and loop compensations along with the loop bandwidth and limiting the output current transient voltage response. Use Equation 2 to set the inductor downslope.

(EQ. 2) $$S_L = \frac{V_{OUT}}{L}$$

The compensation slope is:

(EQ. 3) $$S_{COMP}\left[\frac{A}{\mu s}\right] = 162\left(\frac{R_{SLOPE}[k\Omega]}{500}\right)$$

Due to inductor tolerances and increased noise immunity, Renesas recommends using $S_L = S_{COMP}$ (deadbeat control) so:

(EQ. 4) $$R_{SLOPE}[k\Omega] = 62\frac{V_{OUT}[V]}{L[\mu H]}$$

Due to headroom issues, R_{SLOPE} value must be within $25k\Omega \le R_{SLOPE} \le 100k\Omega$.

Internal slope compensation is set to maximum slope compensation of 0.324.

R_{COMP} value is set by transient response requirement. We need to know Equation 6 and the transient step value ΔI_{OUT}.

(EQ. 5) $$k = \frac{\Delta V_{OUT}}{V_{OUT}}$$

We also need error amp transconductance (gm = 0.923mA/V) and modulator transconductance (GM = 4A/V, which means 250mV voltage step at COMP node causes 1A output current step). Calculate R_{COMP} using Equation 6.

(EQ. 6) $$R_{COMP} = \frac{\Delta I_{OUT}}{kV_{REF}g_{mEA}G_M}$$

Internal compensation is set in such a way as to ensure ±2% V_{OUT} transient response for ±0.5A load current step.

C_{COMP} defines compensator zero frequency:

(EQ. 7) $$fz = \frac{1}{2\pi R_{COMP}C_{COMP}}$$

Set fz to ft/10 to maximize phase margin. However, this slows down transient response recovery time. You can reduce this time by increasing fz (at the expense of the phase margin). In general, zero frequency should not exceed ft/3 (12.7deg loss of phase margin).

When R_{COMP} is determined, use Equation 8 to calculate the output capacitance, where gm = 0.923mS, GM = 4A/V, VREF = 0.6V, and unity gain frequency ft is typically $f_{SW}/10$.

(EQ. 8) $$C_{OUT\_MIN} = \frac{V_{REF}g_mG_MR_{COMP}}{2\pi f_tV_{OUT}}$$

Equation 8 does not guarantee that transient response is met in all cases. The main reason is the nonlinear nature of the switching regulator. To derive equations, approximate the modulator with a simple (and linear) GM stage, which means any fast dV/dt at the input of GM produces equally fast dI/dt at the output. Because the output inductor (L) limits dI/dt (dI/dt = V/L), in some cases (typically extremely low D or extremely large D), the current slew rate dI/dt = V/L might get limited by V/L in which case transient response is going to be larger than expected. In those cases, you must reduce L to increase dI/dt or increase C_{OUT} to slow down dV/dt at the GM input.

In the case of internal compensation (set for ±2% VOUT transient response with ±0.5A load current step), calculate COUT_MIN using Equation 9:

(EQ. 9) $$C_{OUT\_MIN}[\mu F] = \frac{40000}{2\pi f_t[kHz]V_{OUT}[V]}$$

Equations are derived for ideal C_{OUT}. Treat MLCCs as ideal capacitors because of small parasitic components (ESR and ESL). In cases where you cannot use them, carefully consider the ESR value. In the case of extremely fast transients (1A/ns for microprocessors), voltage drop (ESR x dI) appears extremely quickly, and the regulation loop cannot react that fast. In those cases, you need to increase C_{OUT}. Transient response effectively has two components (ESR and C_{OUT}). The solution is to reduce C_{OUT} transient by the ESR x dI product value. For example, if 2% transient is required and ESR x dI causes 0.5% transient response, 1.5% transient should be used to determine R_{COMP}.

Regarding loop stability, ESR zero must be canceled by a pole created with CPOLE such that:

(EQ. 10) $$ESR \times C_{OUT} = R_{COMP}C_{POLE}$$

The temperature coefficient of the ESR can be significant and cause difficulty with this. You need careful evaluation for wide temperature range operations. Consider a combination of Tantalum and MLCC capacitors to achieve high total capacitance with lower ESR.

5.14 Input Capacitor Selection

Use a mix of input bypass capacitors to control the voltage overshoot and undershoot across the internal MOSFETs of the synchronous buck regulator. Use small low ESR ceramic capacitors for high-frequency decoupling and bulk capacitors to supply the current needed each time the upper MOSFET turns on. Place the small ceramic capacitors physically close to the IC between the PVIN and PGND pins.

The critical parameters for the bulk input capacitance are the voltage and RMS current ratings. For reliable operation, select bulk capacitors with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. Their voltage rating should be at least 1.5 times greater than the maximum input voltage, while a voltage rating of 2.5 times is a conservative guideline when considering voltage derating performance to 125°C. Consult the capacitor datasheets for temperature derating tables. For most cases, the RMS current rating requirement for the input capacitor of a buck regulator is approximately 1/2 the DC load current.

Use Equation 11 to closely approximate the maximum RMS current through the input capacitors.

(EQ. 11)
$$I_{CINrms} = \sqrt{\frac{V_{OUT}}{V_{IN}} x \left({I_{OUT_{MAX}}}^2 x \left(1 - \frac{V_{OUT}}{V_{IN}}\right) + \frac{1}{12} x \left(\frac{V_{IN} - V_{OUT}}{Lxf_{OSC}} x \frac{V_{OUT}}{V_{IN}} \right)^2 \right)}$$

The minimum recommended input capacitance for the ISL73006SLH is 22µF. Place these high-frequency, low-ESR capacitors close to the VIN and PGND pins. These capacitors provide the instantaneous current into the buck regulator during the high-frequency switching transitions.

5.15 Output Capacitor Selection

An output capacitor is required to filter the inductor ripple current and supply the load transient current. The filtering requirements are a function of the switching frequency and the ripple current. The load transient requirements are a function of the slew rate (di/dt) and the magnitude of the transient load current. These requirements are generally achieved with a combination of bulk and decoupling capacitors with a careful layout.

High-frequency, low ESR ceramic capacitors initially supply the transient load current and reduce the current load slew rate seen by the bulk capacitors. The Effective Series Resistance (ESR) and voltage rating requirements generally determine the bulk filter capacitor values rather than actual capacitance requirements. Place high-frequency decoupling capacitors as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components.

The shape of the output voltage waveform during a load transient that represents the worst-case loading conditions ultimately determines the number of output capacitors and their type. When this load transient is applied to the regulator, most of the current required by the load is initially contributed by the output capacitors. This is due to the finite amount of time required for the inductor current to slew up or down to the level of the output current required by the load. This results in a momentary undershoot or overshoot in the output voltage. At the initial edge of the transient undershoot or overshoot, the Equivalent Series Inductance (ESL) of each capacitor induces a spike that adds on top of the voltage drop due to the ESR. After the initial spike, the output voltage dips down (load step on) or peaks up (load step off) as the output capacitor sources or sinks the transient load current until the output inductor current reaches the load current. Figure 41 shows a typical response of the output voltage to a transient load current.

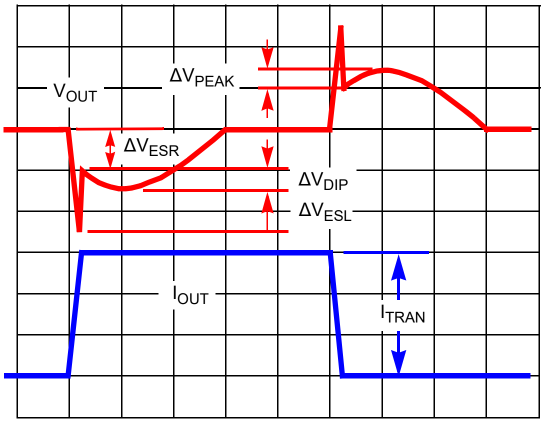


Figure 41. Typical Transient Response

Use Equation 12 to approximate the amplitudes of the voltage spikes caused by capacitor ESR and ESL, where I_{TRAN} = Output load current transient.:

(EQ. 12)

$$\Delta V_{ESR} = ESR \times I_{TRAN}$$

$$\Delta V_{ESL} = ESL \times \frac{dI_{TRAN}}{dt}$$

In a typical converter design, the ESR of the output capacitor bank impacts the transient response. The ESR and the ESL determine the number and types of output capacitors required to minimize the initial voltage spike at the output transient response. It may be necessary to place multiple output capacitors of both ceramic (to provide low ESR, ESL) and Tantalum (to provide the bulk capacitance in a small footprint) types in parallel to reduce the parasitic ESR and ESL to achieve minimize the magnitude of the output voltage spike during a load transient response.

The ESL of the capacitor is an important parameter and not usually listed in datasheets. You can use Equation 13 to approximate ESL if an Impedance vs Frequency curve is available, where f_{res} is the frequency where the lowest impedance is achieved (resonant frequency). The ESL of the capacitor becomes a concern when designing circuits that supply power to loads with high rates of change in the current.

(EQ. 13)

$$ESL = \frac{1}{C(2 \times \pi \times f_{res})^2}$$

If ΔV_{DIP} and/or ΔV_{PEAK} is too large for the output voltage limits, you may need to increase the capacitance. A trade-off between output inductance and output capacitance may be necessary in this situation.

5.16 Output Inductor Selection

The inductor value determines the ripple current of the converter. Choosing an inductor current requires a somewhat arbitrary choice of ripple current, ΔI. A reasonable starting point is ~33% of the total load current. The output inductor influences the response time of the regulator to a load transient. A smaller inductance value improves transient response but increases output voltage ripple. The inductor value determines the inductor ripple current, with the output voltage ripple being a function of the ripple current. Use Equation 14 to approximate the inductor ripple current and Equation 15 to approximate the output voltage ripple, where ESR is the output capacitor equivalent series resistance.

(EQ. 14) $$I_{RIPPLE} = \frac{(V_{IN} - V_{OUT})}{f_{SW} \times L} \times \frac{V_{OUT}}{V_{IN}}$$

(EQ. 15) $$V_{OUT\_RIPPLE} = I_{RIPPLE} \times ESR$$

Increasing inductance reduces the ripple current and output voltage ripple; however, the regulator response time to transient load increases.

One of the parameters limiting the regulator response to a load transient is the time required to change the inductor current. The response time is the time required to slew the inductor current from its initial level to the transient level. During this interval, the difference between the inductor and transient load current is sourced from or sunk into the output capacitor. Minimizing the response time reduces the amount of transient voltage overshoot and undershoot on the output capacitor.

The response time to a transient is different for the transient load on and off. Equation 16 gives the approximate response time to a load step, where I_{TRAN} is the transient load current step, t_{RISE} is the inductor response time to a turn-on load step, and t_{FALL} is the response time to a turn-off load step.

(EQ. 16) $$\text{Load On: } t_{RISE} = \frac{L \times I_{TRAN}}{V_{IN} - V_{OUT}} \qquad \text{Load Off: } t_{FALL} = \frac{L \times I_{TRAN}}{V_{OUT}}$$

The worst-case response time can be during either the load step on or off. Check for transient load response for both turn-on and turn-off at the minimum and maximum load current.

6. Layout Considerations

Proper layout of the PCB for the switching converter is important to ensure the switching converter works well to minimize EMI and noise and ensure first pass success of the design. Figure 42 shows the connections of the most critical top-layer components.

Note: Capacitors C_{IN} and C_{OUT} can each represent multiple physical capacitors.

Renesas recommends using a multilayer printed circuit board with buried GND planes. A critical connection is a thermal connection from the package thermal pad to the PCB PGND plane on the top layer. Additionally, connect the IC PGND pins to this GND plane. This connection of the GND pins to the system GND plane ensures a low-impedance path for all return currents and an excellent thermal path to dissipate heat. With this connection made, place the high-frequency ceramic input capacitor(s) across the PVIN and PGND pins. The bulk capacitance can be further away.

The power loop comprises the output inductor (L_{OUT}), the output capacitor (C_{OUT}), the LX pins, and the PGND pin. Make the power loop as short as possible and the connecting traces direct, short, and wide. An island for the LX node to contain the output inductor is noisy, so keep the voltage feedback trace away from this noisy area. Connect C_{OUT} tightly to L_{OUT} and directly as possible to the PGND pins.

If implemented, the external compensation loop should also be as short as possible, with the connecting traces to R_{COMP} and the C_{COMP} directly between the COMP and SGND pins. The SGND should be connected at 1 point to the PGND plane out of the current flow of the ground plane. A convenient place is under the package to the thermal pad. If implementing internal compensation, tie the COMP pin to VCC as directly as possible, likewise for internal SLOPE selection. The two latter connections are not as critical and can be placed last.

The heat of the IC is mainly dissipated through the thermal pad. Maximizing the copper area connected to the thermal pad is preferable. In addition, a solid buried ground plane is helpful for better EMI performance with a cutout of the top-level LX shape to reduce coupling. Renesas recommends referencing TB499 for guidance about via ground connections within the pad for the best thermal relief.

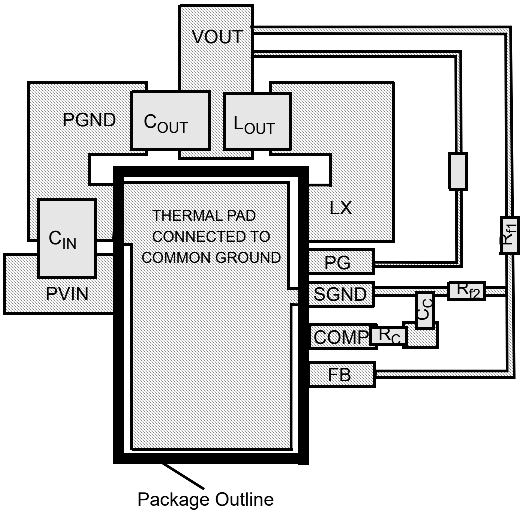


Figure 42. Layout Component Placement Suggestion

7. Die Characteristics

Table 1. Die and Assembly Related Information

Die Information	
Dimensions	2413µm x 3302µm (95 mils x 130 mils) Thickness: 305µm ±25µm (12 mils ±1 mil)
Interface Materials	
Glassivation	Type: 12kÅ Silicon Nitride on 3kÅ Oxide
Top Metallization	Type: Al , 0.5%Cu, 0.87% Si
Backside Finish	Silicon
Process	0.25µm BiCMOS
Assembly Information	
Substrate Potential	Floating
Additional Information	
Worst Case Current Density	$1.6 \times 10^5 A/cm^2$
Transistor Count	19366
Weight of Packaged Device	0.42 grams
Lid Characteristics	Finish: Gold Potential: Tied to package pin 8
Bottom Metal Characteristics	Finish: Gold Potential: Tied to package pin 8

7.1 Metallization Mask Layout

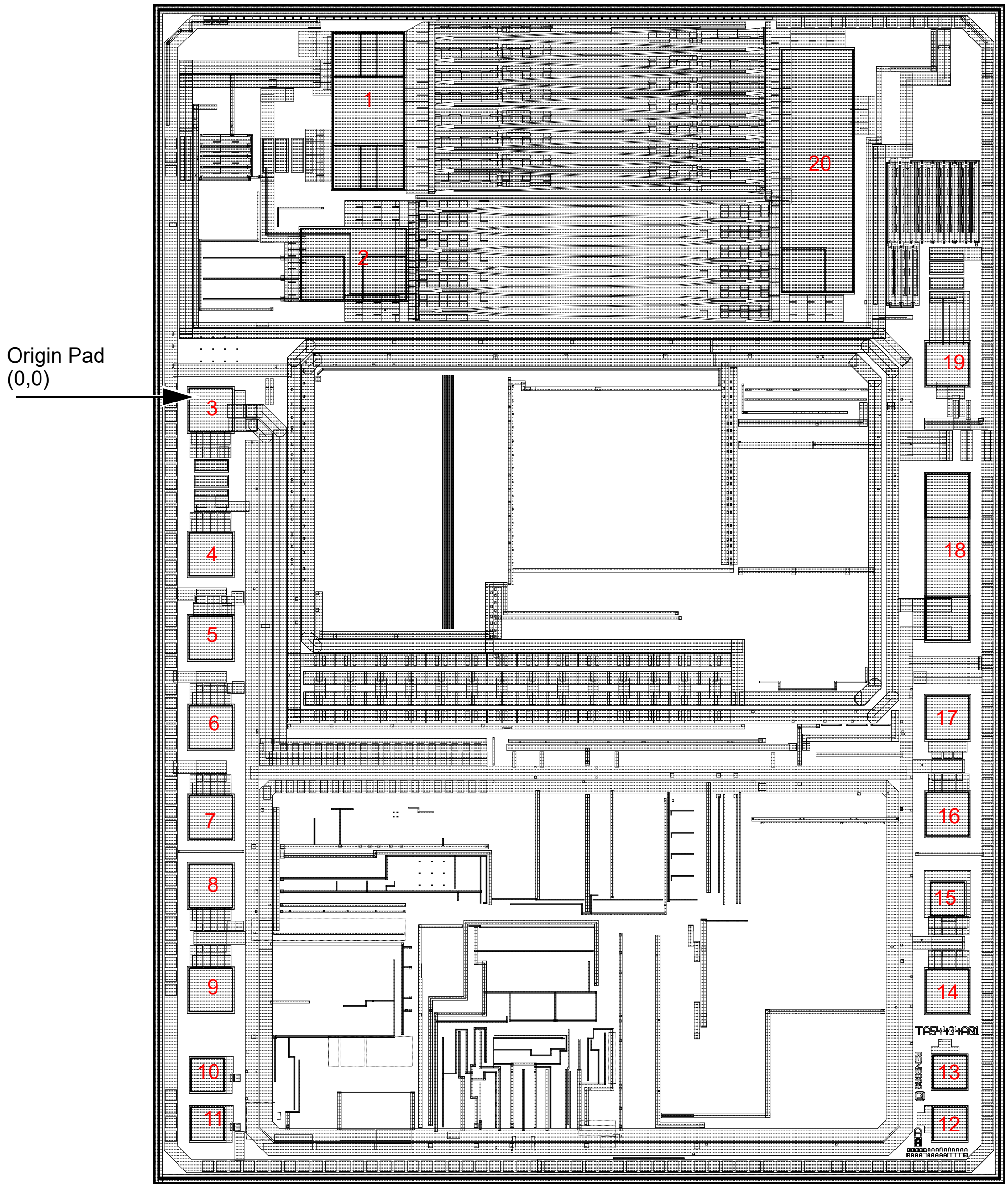


Table 2. Die Layout X-Y Coordinates[1]

Pad Number	Pad Name	X Opening Dimension (µm)	Y Opening Dimension (µm)	X Center of Pad Coordinate	Y Center of Pad Coordinate
1	PGND	193	422	403.64	2727.92
2	PVIN	285	193	392.45	886.42
3 (Origin)	AVIN	117	117	0	0
4	EN	117	117	0	-391.25
5	PVCC	117	117	0	-617.7
6	DVCC	117	117	0	-859.4

Table 2. Die Layout X-Y Coordinates[1] (Cont.)

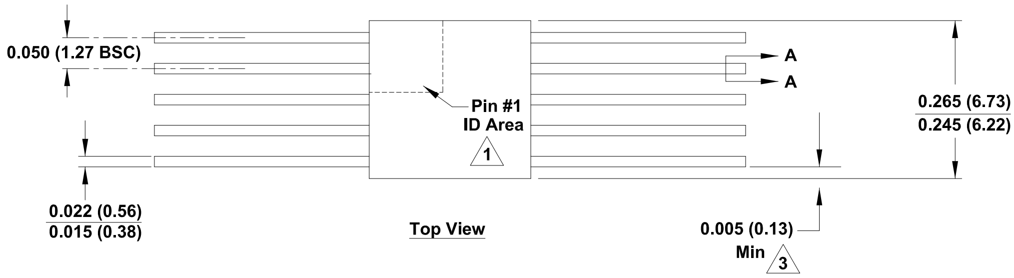
Pad Number	Pad Name	X Opening Dimension (µm)	Y Opening Dimension (µm)	X Center of Pad Coordinate	Y Center of Pad Coordinate
7	**DNB**	-	-	-	-
8	AVCC	117	117	0	-1288.85
9	SLOPE	117	117	0	-1570.2
10	**DNB**	-	-	-	-
11	**DNB**	-	-	-	-
12	**DNB**	-	-	-	-
13	**DNB**	-	-	-	-
14	**DNB**	-	-	-	-
15	**DNB**	-	-	-	-
16	FB	117	117	1993.3	-1094.95
17	COMP	117	117	1993.3	-833.6
18	SGND	117	470	1993.3	-399.1
19	PG	117	117	1993.3	124.85
20	LX	193	658	1640.85	647

1. Origin of coordinates is the center of pad 3, other pad coordinates are pad centers. **DNB - Do Not Bond to this pad.**

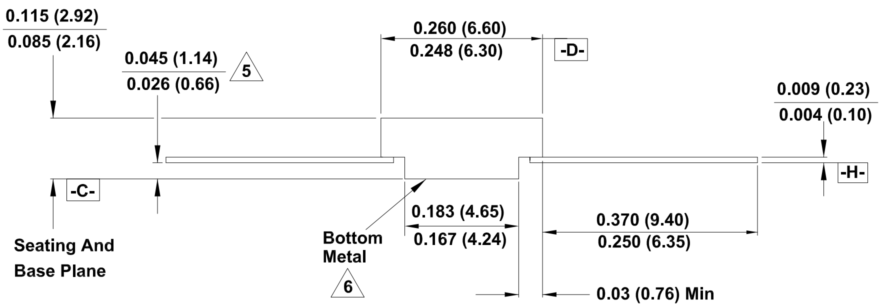
8. Package Outline Drawing

For the most recent package outline drawing, see K10.B.

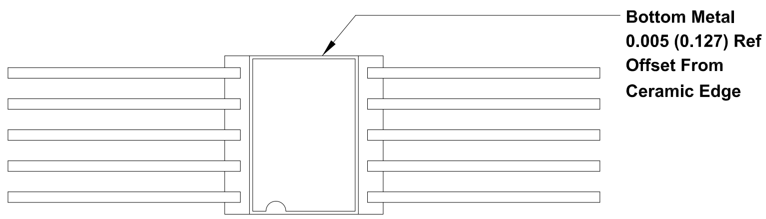
K10.B
10 Lead Ceramic Metal Seal Flatpack Package
Rev 1, 3/21



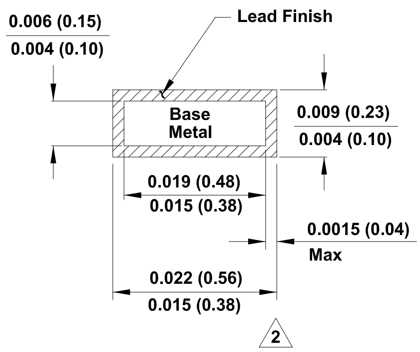
Top View



Side View



Bottom View



Section A-A

Notes:

1. Index area: A notch or a pin one identification mark is located adjacent to pin one and is located within the shaded area shown. The maufacturer's identification is not to be used as a pin one indentification mark.
2. The maximum limits of lead dimensions (section A-A) are measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Measure dimension at all four corners.
4. For bottom-brazed lead packages, no organic or polymeric materials are molded to the bottom of the package to cover the leads.
5. Dimension is measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension minimum is reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
6. The bottom of the package is a solderable metal surface.
7. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
8. Dimensions: INCH (mm), Controlling dimension: INCH.

9. Ordering Information

Part Name[1]	Radiation Hardness (Total Ionizing Dose)	Package Description RoHS Compliant)	Pkg. Dwg. #	Carrier Type	Temp. Range
ISL73006SLHMF	LDR to 75krad(Si)	10 Ld CDFP	K10.B	Tray	-55 to +125°C
ISL73006SLHMX[2]		Die	N/A	N/A	
ISL73006SLHF/PROTO[3]	N/A (For Evaluation Purposes)	10 Ld CDFP	K10.B	Tray	
ISL73006SLHX/SAMPLE[2][3]		Die Sample	N/A	N/A	
ISL73006SLHEV1Z[4]	12VIN to 3.3VOUT Evaluation Board Includes feature configuration jumpers for loop and slope compensation, test points and transient load generator				
ISL73006SLHDEMO1Z[4]	5VIN to 1.2VOUT Mini Demonstration Board Minimum BOM implementation with internally set loop and slope compensation				
ISL73006SLHDEMO2Z[4]	12VIN to 3.3VOUT Mini Demonstration Board Configured with externally set loop and slope compensation, set up for wide VIN of 8V to 16V to 3.3VOUT				
ISL73006SLHDEMO3Z[4]	5VIN to -5VOUT Mini Demonstration Board Configured with internally set loop and slope compensation, set up for VIN of 3V to 8V to -5VOUT				

1. These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. Die product tested at T_A = + 25°C. The wafer probe test includes functional and parametric testing sufficient to make the die capable of meeting the electrical performance outlined in the Electrical Specifications.
3. The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across temperature specified in this datasheet. The /SAMPLE parts are capable of meeting the electrical limits and conditions specified in this datasheet. The /SAMPLE parts do not receive 100% screening across temperature to the electrical limits. These part types do not come with a Certificate of Conformance.
4. The boards use the /PROTO parts. The /PROTO parts are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity.

10. Revision History

Revision	Date	Description
1.01	Mar 13, 2024	Corrected typo on page 1. Updated EC table Heading and notes. Updated the typical values for the following specifications: ▪ Standby Enable Voltage ▪ Shutdown Enable Voltage ▪ Enable Hysteresis Voltage
1.00	Dec 13, 2023	Initial release.

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