HS-OP470ARH, HS-OP470AEH

Radiation Hardened, Very Low Noise Quad Operational Amplifiers

The HS-OP470ARH and HS-OP470AEH are radiation hardened, monolithic quad operational amplifiers that provide highly reliable performance in harsh radiation environments. Excellent noise characteristics coupled with a unique array of dynamic specifications make these amplifiers well-suited for a variety of satellite system applications. Dielectrically isolated, bipolar processing makes these devices immune to single event latch-up.

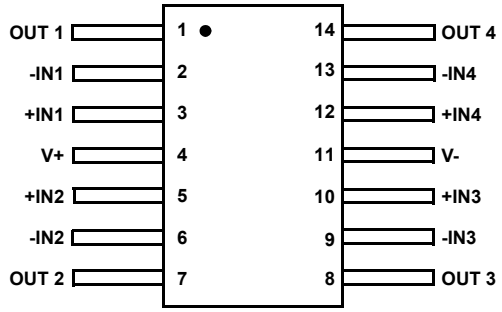
The HS-OP470ARH and HS-OP470AEH show almost no change in offset voltage after exposure to 100krad(Si) gamma radiation, with only a minor increase in current. Complementing these specifications is a post radiation open-loop gain in excess of 40kV/V.

These quad operational amplifiers are available in an industry standard pinout, allowing for immediate interchangeability with most other quad operational amplifiers.

The HS-OP470AEH replaces the obsoleted HS-OP470ARH.

Pin Configuration

(14 LD FLATPACK)
TOP VIEW



Features

- Electrically screened to SMD # 5962-98533
- QML qualified per MIL-PRF-38535 requirements
- Radiation acceptance testing - HS-OP470AEH
  - High dose rate (50-300rad(Si)/s). . . . . 100krad(Si)
  - Low dose rate (0.01rad(Si)/s) . . . . . .50krad(Si)
- Radiation acceptance testing - HS-OP470ARH
  - High dose rate (50-300rad(Si)/s). . . . . 100krad(Si)
- Low noise
  - At 1kHz . . . . . 4.3nV/$\sqrt{Hz}$ (typical)
  - At 1kHz . . . . . 0.6pA/$\sqrt{Hz}$ (typical)
- Low offset voltage . . . . . 2.1mV (maximum)
- High slew rate . . . . . .1.7V/µs (minimum)
- Gain bandwidth product . . . . . .8.0MHz (typical)

Applications

- High Q, active filters
- Voltage regulators
- Integrators
- Signal generators
- Voltage references
- Space environments

Ordering Information

ORDERING SMD NUMBER (Note 1)	PART NUMBER (Note 2)	RADIATION HARDNESS (Total Ionizing Dose)	PACKAGE DESCRIPTION (RoHS Compliant)	PKG. DWG. #	CARRIER TYPE	TEMP. RANGE
5962R9853302VXC	HS9-OP470AEH-Q	HDR to 100krad(Si), LDR to 50krad(Si)	14 Ld Flatpack	K14.A	Tray	-55 to +125°C
5962R9853302V9A	HS0-OP470AEH-Q (Note 3)		Die	-	-	
N/A	HS0-OP470AEH/SAMPLE (Notes 3, 4)	N/A	Die	-	-	
	HS9-OP470AEH/PROTO (Note 4)		14 Ld Flatpack	K14.A	Tray	
5962R9853301QXC	HS9-OP470ARH-8 **No longer available or supported**	HDR to 100krad(Si)	14 Ld Flatpack	K14.A	Tray	
5962R9853301VXC	HS9-OP470ARH-Q **No longer available or supported**					
5962R9853301V9A	HS0-OP470ARH-Q (Note 3) **No longer available or supported**		Die	-	-	
N/A	HS0-OP470ARH/SAMPLE (Notes 3, 4) **No longer available or supported**	N/A	Die	-	-	
	HS9-OP470ARH/PROTO (Note 4) **No longer available or supported**		14 Ld Flatpack	K14.A	Tray	
	HS-OP470AEHEV1Z (Note 5)	Evaluation Board				

1. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed must be used when ordering.
2. These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
3. Die product tested at T_A = + 25°C. The wafer probe test includes functional and parametric testing sufficient to make the die capable of meeting the electrical performance outlined in the SMD.
4. The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across temperature specified in the DLA SMD and are in the same form and fit as the qualified device. The /SAMPLE parts are capable of meeting the electrical limits and conditions specified in the DLA SMD. The /SAMPLE parts do not receive 100% screening across temperature to the DLA SMD electrical limits. These part types do not come with a Certificate of Conformance because they are not DLA qualified devices.
5. Evaluation board uses the /PROTO parts. The /PROTO parts are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity.

Die Characteristics

DIE DIMENSIONS:

95 mils x 99 mils x 19 mils ±1 mil
(2420µm x 2530µm x 483µm ±25.4µm)

INTERFACE MATERIALS:

Glassivation:

Type: Silox (SIO2) 1:6:1
Thickness: 8kÅ ±0.8kÅ (1kÅ undopped, 6kÅ dopped, cap 1kÅ undopped)

Top Metallization:

Type: Al/Cu 16kÅ ±2kÅ

Substrate:

Dielectrically Isolated (DI)

Backside Finish:

Silicon

ASSEMBLY RELATED INFORMATION:

Substrate potential:

Unbiased

Special assembly instructions

None

ADDITIONAL INFORMATION:

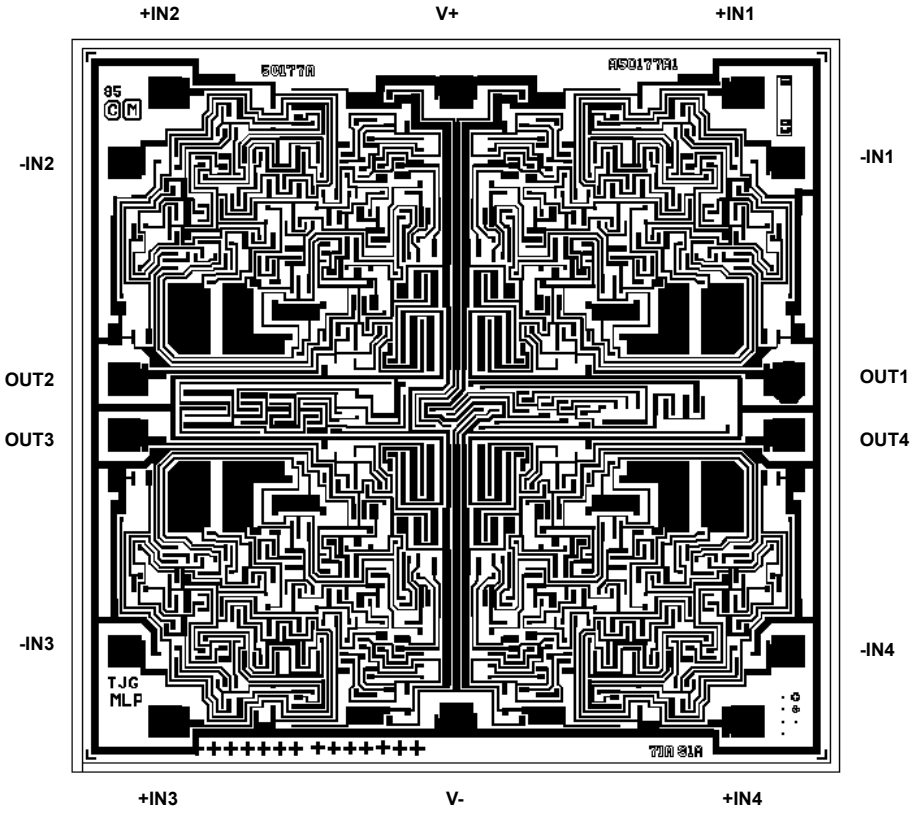
Worst Case Current Density:

$< 2.0 \times 10^5$ A/cm^2

Transistor Count:

175

Metallization Mask Layout



Package Outline Drawing

The package outline drawings is located at the end of this document and is accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

Revision History

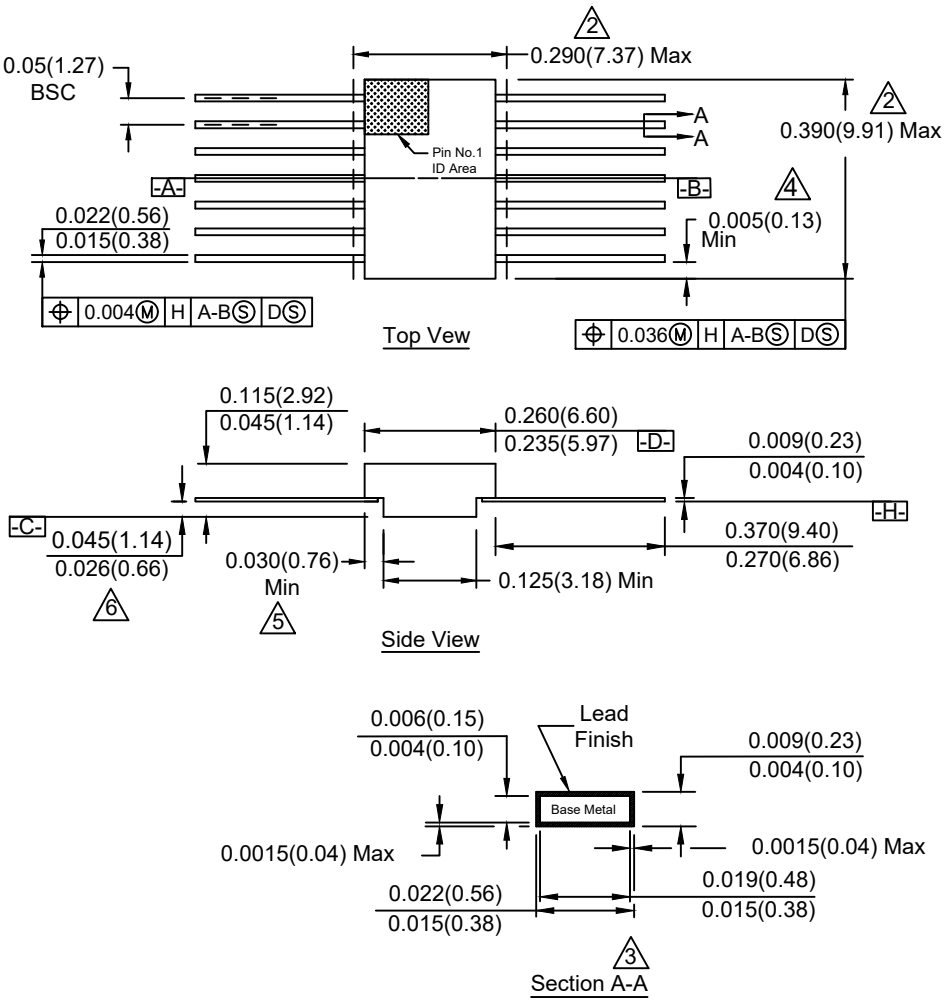
The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

DATE	REVISION	CHANGE
May 9, 2025	4.01	Updated POD K14.A to the latest revision; changes are as follows: -Applied latest template -Corrected typo in the mm value for dimension E1 from 7.11 to 7.37mm
May 18, 2021	4.0	Updated Radiation Acceptance testing features bullets. Updated the Ordering Information table. Updated Die Characteristics for Glassivation, Top Metalization, Substrate, and Assembly Related Information to match information in the SMD 5962-98533.
Sep 21, 2018	3.0	Added Related Literature section. Updated the Ordering Information table by adding HS0-OP470AEH/SAMPLE and HS0-OP470AEH/PROTO parts, removing part marking column, and adding Notes 3 and 4. Added Revision History section. Updated Disclaimer.

Package Outline Drawing

14 Lead Ceramic Metal Seal Flatpack Package

POD Number: K14.A, Revision no: 02, Date Created: Mar 4, 2025



Notes:

1 Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacture's identification shall not be used as a pin one identification mark.

2 This dimension allows for off-center lid, meniscus, and glass overrun.

3 The maximum limits of lead dimensions (section A-A) shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate finish is applied.

4 Measure dimension at all four corners.

5 For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.

6 This dimension shall be measured at the point of exit (beyond the meniscus) of the lead from the body. This dimension's minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.

7. Dimensioning and tolerancing per ANSI Y14.5M - 1982.

8. Dimensions: INCH(mm). Controlling dimension: INCH.

9. Compliant to MIL-STD-1835 CDFP3-F14 (F-2A, CONFIGURATION B).

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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