HS-201HSRH, HS-201HSEH

Radiation Hardened High Speed, Quad SPST, BiCMOS Analog Switch

Description

The HS-201HSRH and HS-201HSEH are monolithic BiCMOS analog switches featuring power-off high input impedance, very fast switching speeds and low ON-resistance. Fabrication on our DI RSG process ensures SEL immunity and only very slight low dose rate sensitivity (ELDRS). These Class V/Q devices are tested and guaranteed for 300krad(Si) total dose performance.

Power-off high input impedance enables the use of this device in redundant circuits without causing data bus signal degradation. ESD protection, overvoltage protection, fast switching times, low ON-resistance, and guaranteed radiation hardness make the HS-201HSRH ideal for any space application that requires improved switching performance.

Applications

- High speed multiplexing
- Sample and hold circuits
- Digital filters
- Operational amplifier gain switching networks
  - Integrator reset circuits

Features

- Electrically screened to DLA SMD# 5962-99618
  - QML qualified per MIL-PRF-38535
- TID Rad Hard Assurance (RHA) testing (HS-201HSRH)
  - HDR (50-300rad(Si)/s): 300krad(Si)
- TID Rad Hard Assurance (RHA) testing (HS-201HSEH)
  - HDR (50-300rad(Si)/s): 300krad(Si)
  - LDR (0.01rad(Si)/s): 50krad(Si)
- SEL immune: DI RSG process
- Power off high impedance: ±17V
- Fast switching times
  - t_{ON}: 110ns (max)
  - t_{OFF}: 80ns (max)
- Low ON-resistance: 50Ω (max)
- Pin compatible with industry-standard 201 types
- Operating supply range: ±10V to ±15V
- Wide analog voltage range (±15V supplies): ±15V
- TTL compatible

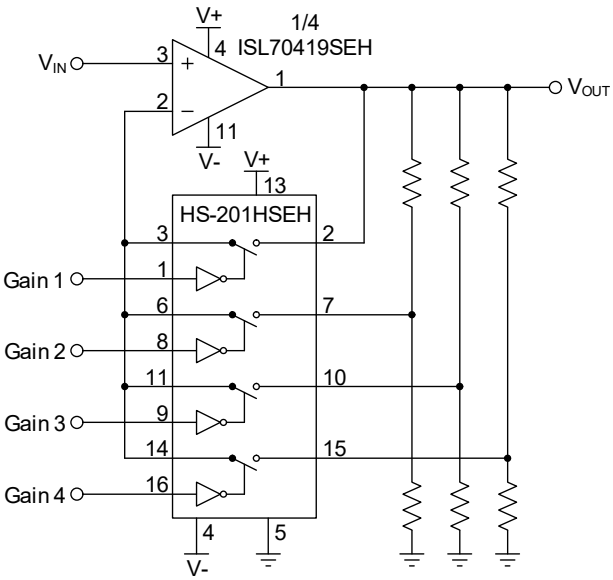


Figure 1. Typical Application

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1. Overview

1.1 Block Diagram

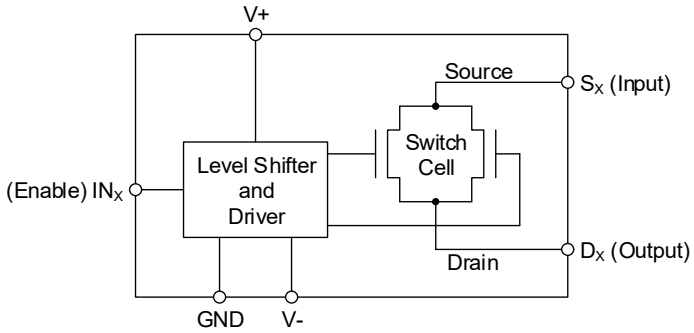


Figure 2. Block Diagram

2. Pin Information

2.1 Pin assignments

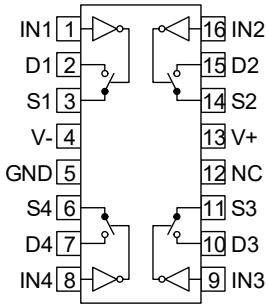


Figure 3. Pin Assignments - Top View

2.2 Pin Descriptions

Pin Number	Pin Name	Function
1, 8, 9, 16	INx	Low-active Switch Enable Input
2, 7, 10, 15	Dx	Drain: Analog Signal Output
3, 6, 11, 14	Sx	Source: Analog Signal Input
4	V-	Negative Chip Supply
5	GND	Reference for all Input and Output Voltages
13	V+	Positive Chip Supply

3. Specifications

Absolute Maximum Ratings

***Caution**:* Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
Positive Supply Voltage (V+ to Ground)	-	+18	V
Negative Supply Voltage (V- to Ground)	-	-18	V
Digital Input Voltage (V_{IN})	-17	+17	V
Analog Input Voltage; One Switch (V_S)	-17	+17	V
Maximum Power Dissipation (P_D)	-	750	mW
Lead Temperature (soldering 10 seconds)	-	265	°C
Junction Temperature (T_J)	-	175	°C
Storage temperature Range	-65	150	°C
Peak Current, S or D (pulsed at 1ms, 10% duty cycle max)	-	50	mA
Continuous Current Any Terminal	-	25	mA

3.1 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Supply Voltage Range (V+,V-)	±10	±15	V
Ambient Operating Temperature Range (T_A)	-55	125	°C

3.2 Thermal Information

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	16 Ld Flatpack	θ_{JA}	Junction to ambient	95	°C/W
		θ_{JC}	Junction to case	12	°C/W
	16 Ld SBDIP	θ_{JA}	Junction to ambient	80	°C/W
		θ_{JC}	Junction to case	12	°C/W

3.3 Electrical Specifications

V+ = +15V, V- = -15V, -55°C ≤ T_A ≤ +125°C unless otherwise specified.

Parameter	Symbol	Test Condition	Temp. (°C)	Min	Max	Unit
Analog Input Voltage Range[1]	V_S	-	T_A = +25°C	±10	±15	V
ON-Resistance	$R_{DS(ON)}$	V_S = ±10V I_D = 1mA V_{IN} = 0.8V	T_A = +25°C	-	50	Ω
			T_A = -55°C to +125°C	-	75	Ω
Source OFF Leakage Current[2]	$I_{S(OFF)}$	V_S = ±14V V_D = ±14V V_{IN} = 2.4V	T_A = +25°C	-	±10	nA
			T_A = -55°C to +125°C	-	±100	nA
Drain OFF Leakage Current	$I_{D(OFF)}$	V_S = ±14V V_D = ±14V V_{IN} = 2.4V	T_A = +25°C	-	±10	nA
			T_A = -55°C to +125°C	-	±100	nA
Channel ON Leakage Current	$I_{D(ON)}$	V_D = V_S = ±14V V_{IN} = 0.8V	T_A = +25°C	-	±10	nA
			T_A = -55°C to +125°C	-	±100	nA

V+ = +15V, V- = -15V, -55°C ≤ T_A ≤ +125°C unless otherwise specified. (Cont.)

Parameter	Symbol	Test Condition	Temp. (°C)	Min	Max	Unit
Input Leakage Current (Low)	I_{IL}	V_{IN} under Test = 0.8V All other V_{IN} = 4.0V	T_A = -55°C to +125°C	-	±500	µA
Input Leakage Current (High)	I_{IH}	V_{IN} under Test = 4.0V All other V_{IN} = 0.8V	T_A = -55°C to +125°C	-	±40	µA
Positive Supply Current	I+	V_{IN} = 2.4V or V_{IN} = 0.8V for all Switches	T_A = -55°C to +125°C	-	12	mA
Negative Supply Current	I-		T_A = -55°C to +125°C	-	12	mA
Logic Input Low Voltage	V_{IL}	V_S = -10V Input, I_D = 1mA Load	T_A = -55°C to +125°C	-	0.8	V
Logic Input High Voltage	V_{IH}		T_A = -55°C to +125°C	2.4	-	V
Switch On-Time	t_{ON}	R_L = 1kΩ, C_L = 35pF, V_S = ±10V, V_{IN} = 3V → 0V (Figure 3)	T_A = +25°C	-	110	ns
			T_A = -55°C to +125°C	-	130	ns
Switch Off-Time	t_{OFF}	R_L = 1kΩ, C_L = 35pF, V_S = ±10V, V_{IN} = 0V → 3V (Figure 3)	T_A = +25°C	-	80	ns
			T_A = -55°C to +125°C	-	110	ns
Power Off (V+ = V-) Leakage Current into the Source terminal of an Off Switch with Overvoltage applied.	$I_{S(OFF)}$ Overvoltage	V_S = -10V Input, I_D = 1mA Load	T_A = +25°C	-1	1	µA
			T_A = -55°C to +125°C	-5	5	µA

1. This parameter is not tested but guaranteed by the limits specified in this table.
2. There is no drain-to-source isolation.

3.5 Electrical Specifications – Post Radiation

V+ = +15V, V- = -15V, T_A = +25°C

Parameter	Symbol	Test Condition	Min	Max	Unit
ON-Resistance	$r_{DS(ON)}$	V_S = ±10V, I_D = 1mA, V_{IN} = 0.8V	-	50	Ω
Source OFF Leakage Current	$I_{S(OFF)}$	V_S = ±14V, V_D = ±14V, V_{IN} = 2.4V	-	±10	nA
Drain OFF Leakage Current	$I_{D(OFF)}$	V_S = ±14V, V_D = ±14V, V_{IN} = 2.4V	-	±10	nA
Channel ON Leakage Current	$I_{D(ON)}$	V_D = V_S = ±14V, V_{IN} = 0.8V	-	±10	nA
Input Leakage Current (Low)	I_{IL}	V_{IN} under Test = 0.8V, All other V_{IN} = 4.0V	-	±500	µA
Input Leakage Current (High)	I_{IH}	V_{IN} under Test = 4.0V, All other V_{IN} = 0.8V	-	±40	µA
Positive Supply Current	I+	V_{IN} = 2.4V or V_{IN} = 0.8V for all Switches	-	12	mA
Negative Supply Current	I-	V_{IN} = 2.4V or V_{IN} = 0.8V for all Switches	-	12	mA
Logic Input Low Voltage	V_{IL}	V_S = -10V Input, I_D = 1mA Load	-	0.8	V
Logic Input High Voltage	V_{IH}	V_S = -10V Input, I_D = 1mA Load	2.4	-	V
Switch On-Time	t_{ON}	R_L = 1kΩ, C_L = 35pF, V_S = ±10V (Figure 3), V_{IN} = 3V → 0V	-	130	ns
Switch Off-Time	t_{OFF}	R_L = 1kΩ, C_L = 35pF, V_S = ±10V (Figure 3), V_{IN} = 0V → 3V	-	80	ns
Power Off (V+ = V-) Leakage Current into the Source terminal of an Off Switch with Overvoltage applied.	$I_{S(OFF)}$ Overvoltage	V_S = ±17V, V_D = 0V, Unused Inputs tied to Ground	-5	5	µA

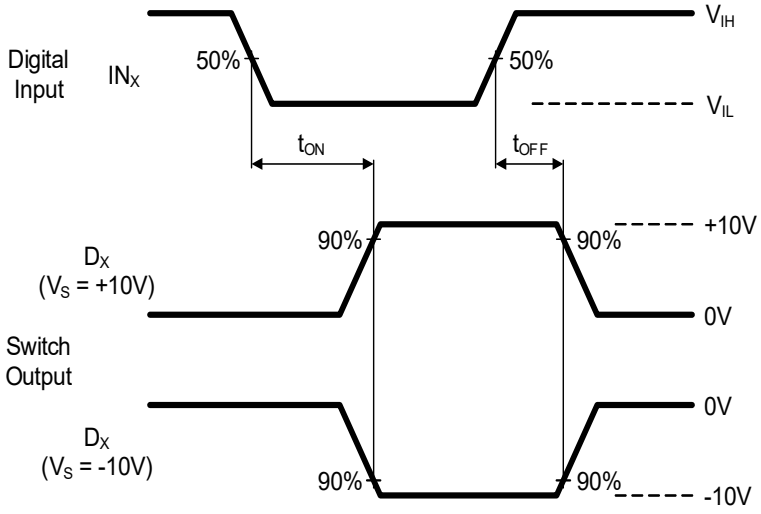


Figure 4. t_{ON}, t_{OFF} Definition

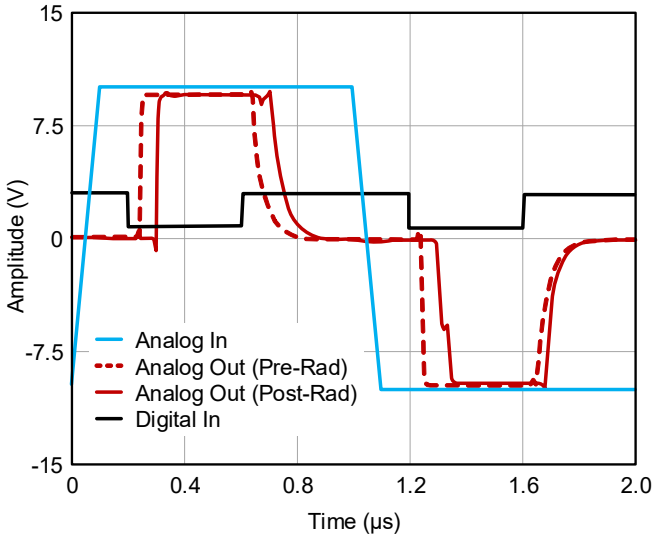


Figure 5. Post-Rad Prop-Delay Shift

4. Typical Performance Graphs

V+ = +15V, V- = -15V, T_A = +25°C, unless otherwise noted.

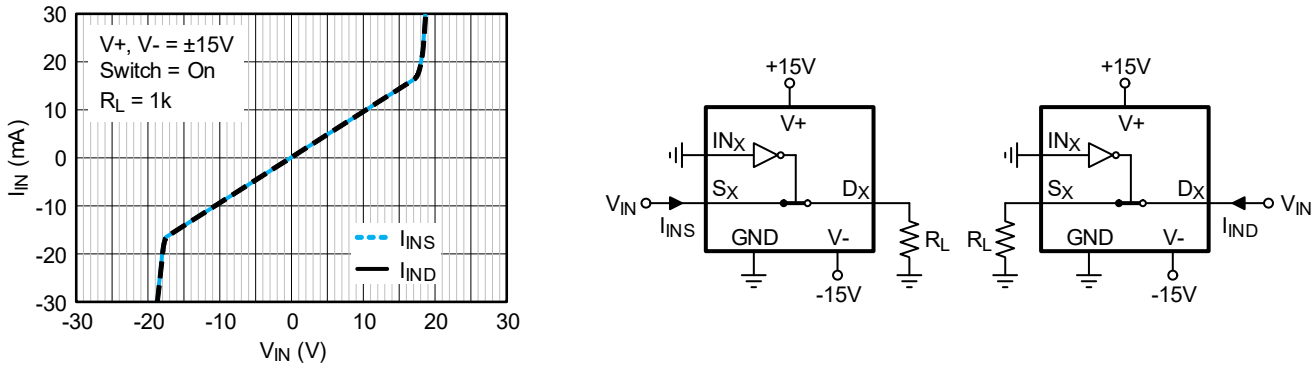


Figure 6. Input Current for Powered Switch in ON Position

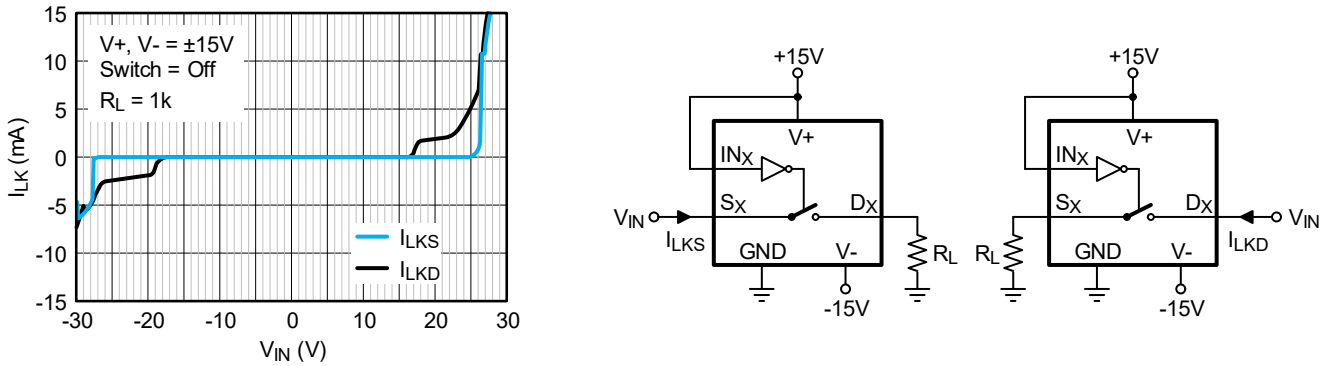


Figure 7. Input Leakage Current for Powered Switch in OFF Position

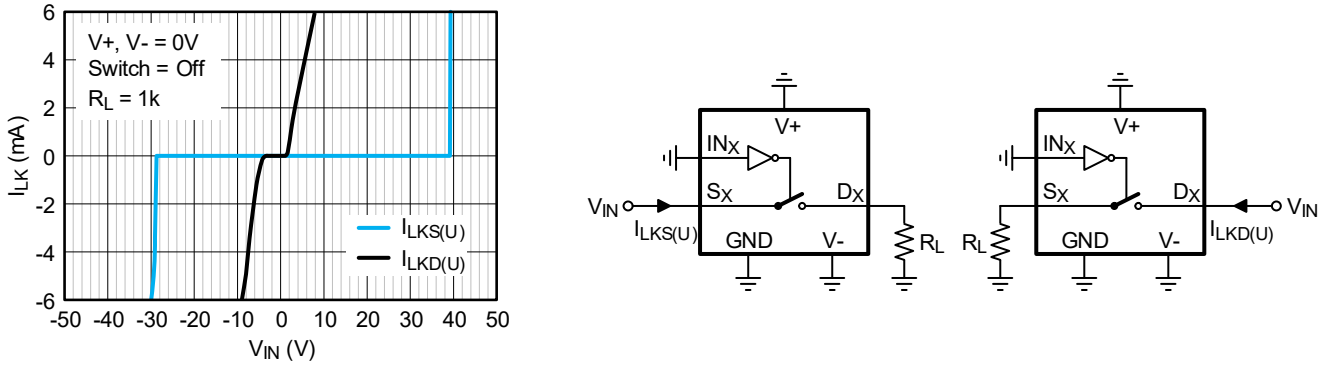


Figure 8. Input Leakage Current for Unpowered Switch (OFF by Design)

V+ = +15V, V- = -15V, T_A = +25°C, unless otherwise noted. (Cont.)

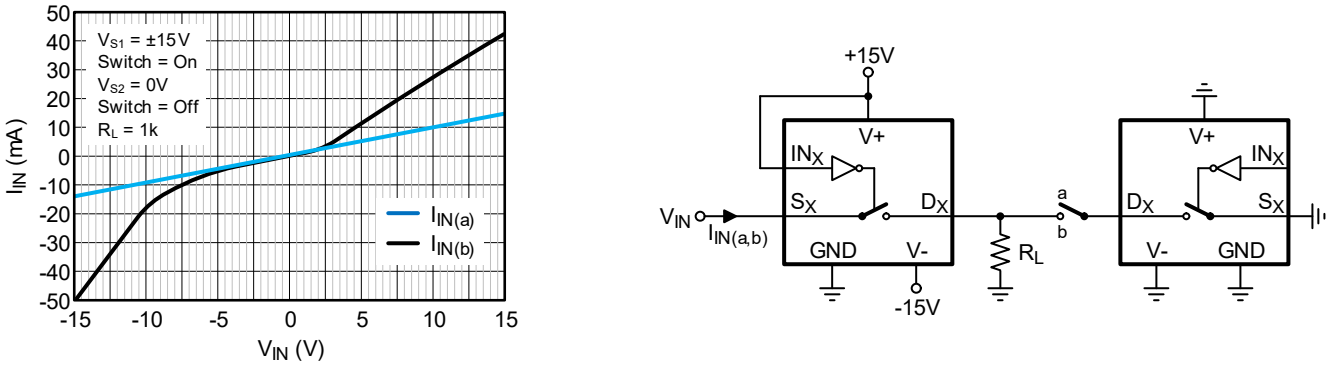


Figure 9. Input Current without Cold Sparing Device (a) and with Cold Sparing Device (b)

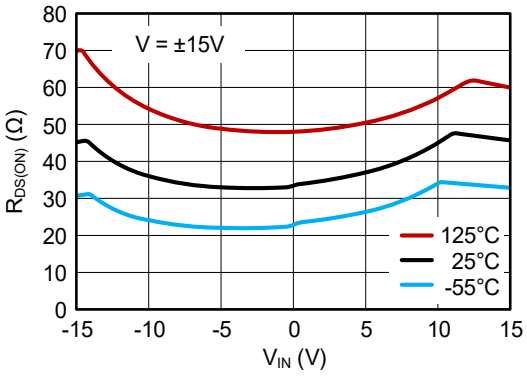


Figure 10. $r_{DS(ON)}$ vs Temperature

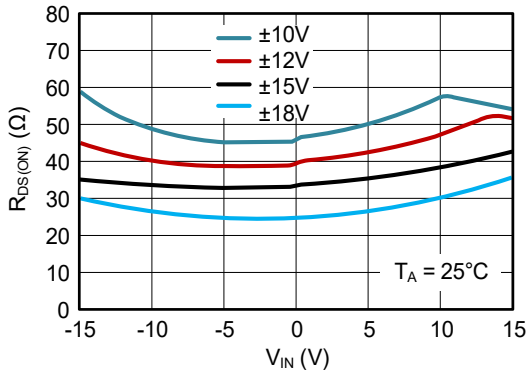


Figure 11. $R_{DS(ON)}$ vs Supply Voltage

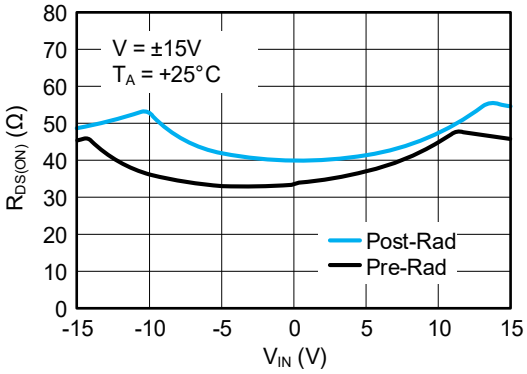


Figure 12. Pre-Rad and Post-Rad $R_{DS(ON)}$

5. Die and Assembly Information

Table 1. Die and Assembly Characteristics

Die Information	
Dimensions	4950µm x 2970µm (195 mils x 117 mils) Thickness: 483µm ±25.4µm (19 mils ±1 mil)
Interface Materials	
Glassivation	Type: Phosphorus Silicon Glass (PSG) Thickness: 8.0kÅ ±1.0kÅ
Metallization	Type: AlSiCu Thickness: 16.0kÅ ±2kÅ
Backside Finish	Silicon
Substrate	Rad Hard Silicon Gate, Dielectric Isolation
Assembly Information	
Substrate Potential	Unbiased (DI)
Additional Information	
Worst Case Current Density	$<2.0\times10^{5}A/cm^{2}$
Transistor Count	328

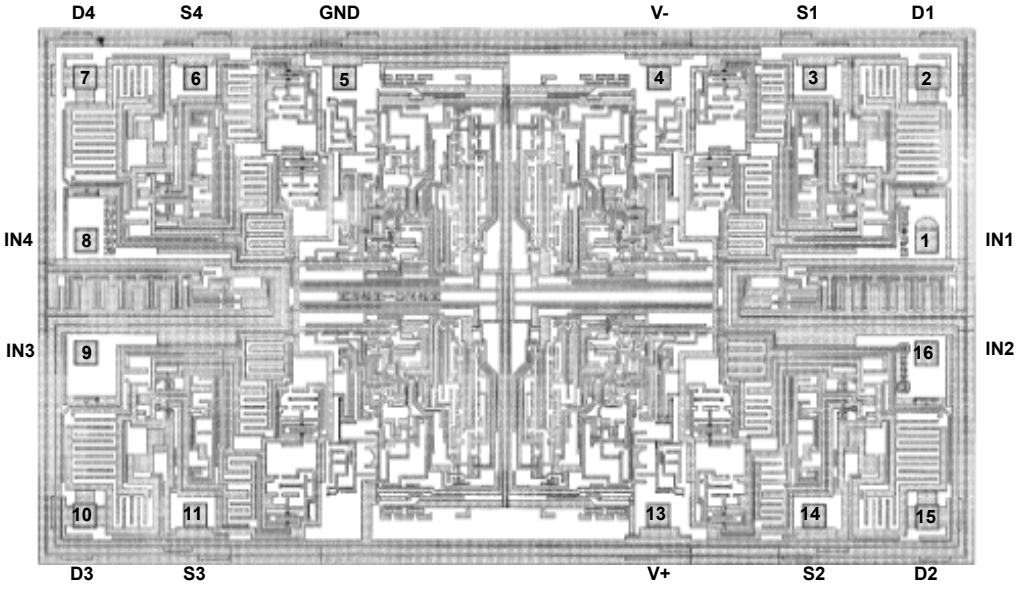


Figure 13. HS-201HSRH and HS-201HSEH Mask Layout

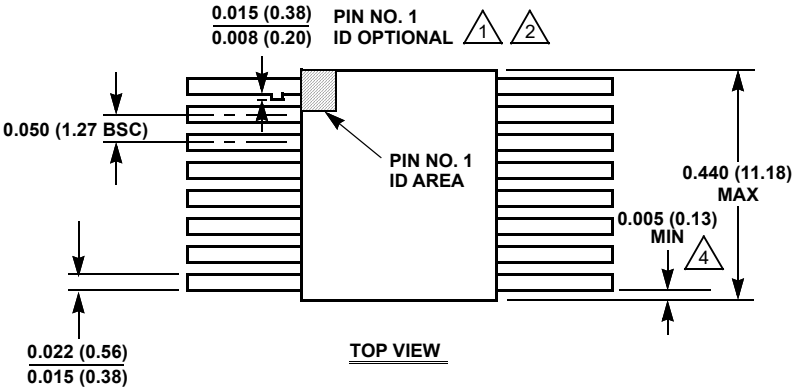
Table 2. Layout X-Y Coordinates[1]

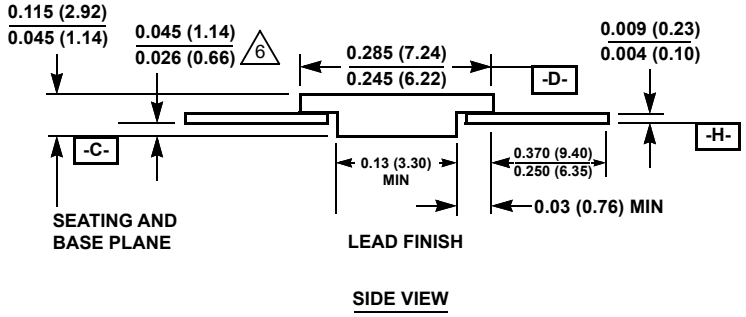
Pad Number[2]	Pad Name	X (µm)	Y (µm)
01	IN1	365.5	1080.5
02	D1	364.5	277
03	S1	935	280
04	V-	1733	280
05	GND	3345	280
06	S4	4097	280
07	D4	4667.5	277
08	IN4	4666.5	1080.5
09	IN3	4666.5	1632.5
10	D3	4667.5	2436
11	S3	4097	2433
12	No Pad	-	-
13	V+	1733	2433
14	S2	935	2433
15	D2	364.5	2436
16	IN2	365.5	1632.5

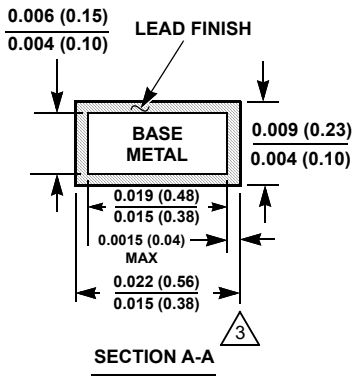
1. Origin of coordinates is the upper right hand corner of the die.
2. Pad numbers are increased counter clockwise around the die.

6. Package Outline Drawings

K16.A
16 Lead Ceramic Metal Seal Flatpack Package
Rev 2, 1/10



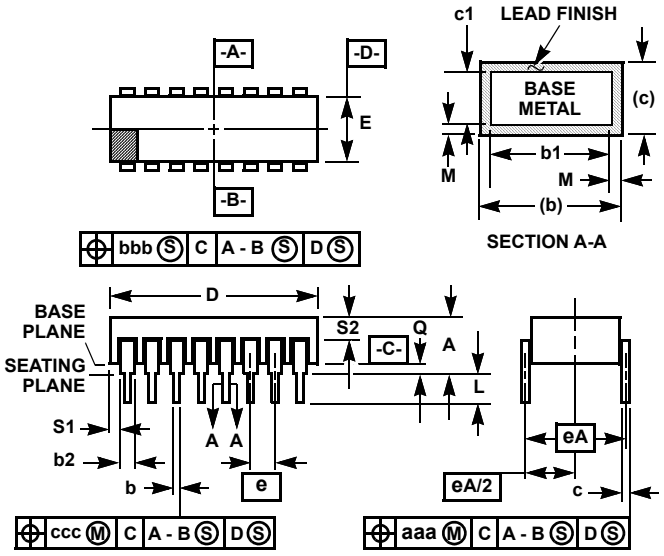




NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of the tab dimension do not apply.
3. The maximum limits of lead dimensions (section A-A) shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
4. Measure dimension at all four corners.
5. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
6. Dimension shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
7. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
8. Controlling dimension: INCH.

Ceramic Dual-In-Line Metal Seal Packages (SBDIP)



D16.3 **MIL-STD-1835 CDIP2-T16 (D-2, CONFIGURATION C)**
16 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	-
E	0.220	0.310	5.59	7.87	-
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90º	105º	90º	105º	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	16		16		8

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NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

7. Ordering Information

Ordering SMD Number[1]	Internal Part Number[2]	Radiation Hardness (Total Ionizing Dose)	Package Description (RoHS Compliant)	Pkg. Dwg. #	Temp. Range
5962F9961801VEC	HS1-201HSRH-Q	HDR to 300krad(Si)	16 Ld SBDIP	D16.3	-55 to +125°C
5962F9961802VEC	HS1-201HSEH-Q	HDR to 300krad(Si) LDR to 50krad(Si)			
5962F9961801QEC	HS1-201HSRH-8	HDR to 300krad(Si)			
5962F9961801VXC	HS9-201HSRH-Q	HDR to 300krad(Si)	16 Ld Flatpack	K16.A	-55 to +125°C
5962F9961802VXC	HS9-201HSEH-Q	HDR to 300krad(Si) LDR to 50krad(Si)			
5962F9961801QXC	HS9-201HSRH-8	HDR to 300krad(Si)			
5962F9961801V9A	HS0-201HSRH-Q[3]	HDR to 300krad(Si)	Die	-	-55 to +125°C
5962F9961802V9A	HS0-201HSEH-Q[3]	HDR to 300krad(Si) LDR to 50krad(Si)			
N/A	HS1-201HSRH/PROTO[4]	N/A	16 Ld SBDIP	D16.3	-55 to +125°C
	HS9-201HSRH/PROTO[4]		16 Ld Flatpack	K16.A	
	HS0-201HSRH/SAMPLE[3][4]		Die	-	

1. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The listed SMD numbers must be used when ordering.
2. These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
3. Die product tested at TA = + 25°C. The wafer probe test includes functional and parametric testing sufficient to make the die capable of meeting the electrical performance outlined in the SMD.
4. /PROTO and /SAMPLE note - The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across temperature specified in the DLA SMD and are in the same form and fit as the qualified device. The /SAMPLE parts can meet the electrical limits and conditions specified in the DLA SMD. The /SAMPLE parts do not receive 100% screening across temperature to the DLA SMD electrical limits. These part types do not come with a Certificate of Conformance because they are not DLA qualified devices.

8. Revision History

Revision	Date	Description
4.03	Nov 11, 2026	Updated Typical Performance Graphs.
4.02	Mar 18, 2026	▪ Applied latest template. ▪ Updated Features section. ▪ Added Figures 1 and 2. ▪ Updated Figure 3. ▪ Added Pin Descriptions section. ▪ Added Specifications sections. ▪ Added Typical Performance Graphs section.
4.01	May 8, 2024	▪ Fixed hyperlinks throughout. ▪ Updated Features bullets. ▪ Removed Related Literature ▪ Updated Ordering Information table. ▪ Removed About Intersil section.
4.00	Feb 21, 2017	▪ Changed die dimension from 2790µm x 4950µm (110 mils x 195 mils) to 4950µm x 2970µm (195mils x 117 mils). ▪ Added Table 1 “LAYOUT X-Y COORDINATES”. ▪ Changed pin names to match the pin names in the SMD data sheet. ▪ Added Revision History and About Intersil sections.

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