F6923

Dual-Channel Low Noise Amplifier 14GHz – 17GHz

Description

The F6923 is an ultra-low power consumption, dual-channel, low noise amplifier (LNA) RFIC designed for application in Ku-Band planar phased array antennas. The exceptional combination of low power consumption, low noise, high gain, and compact size, maximizes the antenna array G/T while minimizing overall system power dissipation. An external bias current provides gain control, standby mode, and temperature compensation.

The F6923 includes two independent gain/phase matched LNA channels in a compact 23-pin, 0.5mm pitch BGA package. All inputs and outputs are single-ended and 50Ω matched for ease of integration onto phased array antenna panels.

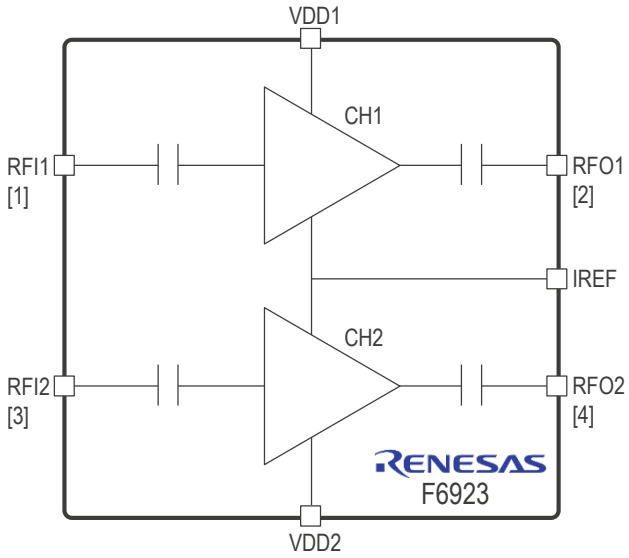

Figure 1. Block Diagram

Features

- Frequency: 14GHz – 17GHz
- Gain: 19.5dB
- Noise figure: 1.5dB
- Output P1dB: -1.5dBm
- Power consumption: 16mW/ch
- Channel isolation: 35dB
- Supply voltage: 0.9V – 1.0V
- Common bias control input
- Compact size for planar integration on λ/2 grid
- 2.7 × 2.7 × 0.9 mm, 23-pin BGA
- -40°C to +85°C ambient operating temperature range

Note: Performance is typical at 15.5GHz and nominal supply voltage. For more information, see the Specifications and Typical Performance Characteristics sections.

Applications

- Electronically Steered Phased Array Antennas (ESAs)
- Ku-Band Radar, SATCOM, and Common Data Link (CDL)
- Communication Systems

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1. Pin Information

1.1 Pin Assignments

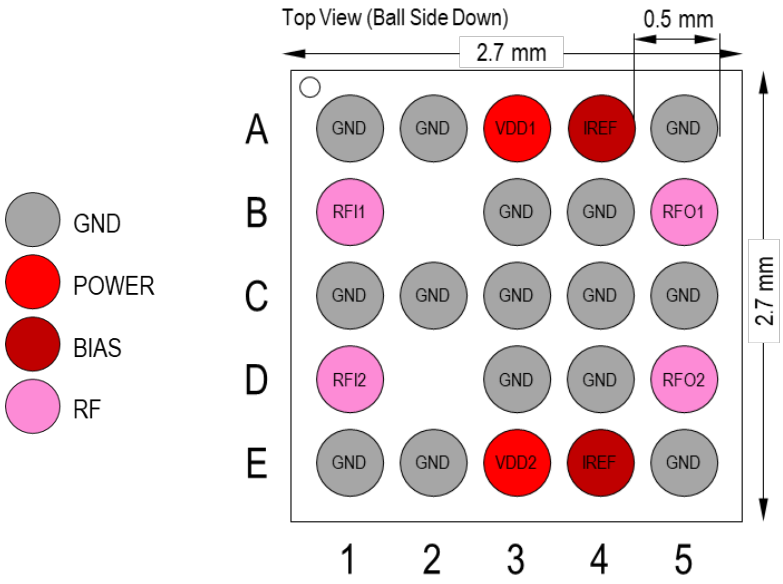


Figure 2. Pin Assignments – Top View

1.2 Pin Descriptions

Pin Number	Name	Type	I/O	Description
A1, A2, A5, B3, B4, C1, C2, C3, C4, C5, D3, D4, E1, E2, E5	GND	Ground	-	DC and RF ground.
A3	VDD1	Power	Input	Positive supply voltage input for channel 1. Channel 2 must also be enabled by powering VDD2 for channel 1 to be operable.
E3	VDD2	Power	Input	Positive supply voltage input for channel 2. For single channel operation of channel 2, channel 1 must be disabled by either floating or grounding VDD1.
A4, E4	IREF	Power	Input	Reference bias current input, tied to a common node shared by channels 1 and 2. Connect directly to a current source, voltage source through a resistor, or to the IBx pin of the F61xx.
B1	RFI1	Analog	Input	Channel 1 RF input port.
D1	RFI2	Analog	Input	Channel 2 RF input port.
B5	RFO1	Analog	Output	Channel 1 RF output port.
D5	RFO2	Analog	Output	Channel 2 RF output port.

2. Specifications

Caution: Exposure of the device to parameter values outside of the range listed below may reduce the operating lifetime and adversely and permanently alter the device characteristics. Furthermore, functional operation at or near absolute maximum ratings is not implied.

2.1 Absolute Maximum Ratings

Parameter	Symbol	Conditions	Minimum	Maximum	Unit
Supply Voltage	V_{DD}	-	-0.3	1.2	V
Reference Current	I_{REF}	-	0	200	µA
Input RF Pin DC Voltage	V_{DC_RFI}	-	-0.3	1.0	V
Output RF Pin DC Voltage	V_{DC_RFO}	-	-0.3	1.2	V
RF Input Power	P_{IN}	V_{DD} = 1.0V, VSWR < 2:1	-	0	dBm
Junction Temperature	T_J	-	-	125	°C
ESD – Human Body Model	V_{HBM}	JS-001-2012	-	750	V
ESD – Charged Device Model	V_{CDM}	JESD22-C101	-	250	V

2.2 Thermal Information

Parameter	Symbol	Value	Unit
Theta JB. Junction to board	θ_{JB}	14	°C/W
Theta JC. Junction to case. (case top)	θ_{JC}	108	°C/W
Theta JA. Junction to ambient	θ_{JA}	47	°C/W
Storage Temperature	T_{STOR}	-40 to +150	°C
Lead Temperature (soldering, 30s)	T_{LEAD}	260	°C

2.3 Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Unit
RF Frequency Range	f_{RF}	14	-	17	GHz
Power Supply Voltage	V_{DD}	0.9	0.95	1.0	V
Reference Bias Current at -40°C	I_{REF}	71	83	95	µA
Reference Bias Current at +25°C		94	110	127	µA
Reference Bias Current at +85°C		115	135	155	µA
Ambient Temperature	T_A	-40	-	85	°C
RF Pin Load Impedance	Z_{RF}	-	50	-	Ω

2.4 Electrical Specifications

Specifications apply when operated at T_{AMB} = +25°C.

2.4.1. DC Electrical Specifications

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Supply Current, Per Channel	I_{DD}	V_{DD} = 0.95V, I_{REF} = 110µA	-	17	-	mA
Supply Current, Idle-state [1]	I_{DD_IDLE}	I_{IREF} = 0µA	-	1	-	µA

1. IREF pin can be grounded or floating to achieve idle-state.

2.4.2. RF Electrical Specifications

Unless stated otherwise, all specifications are for V_{DD} = 0.95V, I_{REF} = 110µA, T_{AMB} = 25°C, Z_S = Z_L = 50Ω, f_{RF} = 15.5GHz.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Gain	G	-	-	19.5	-	dB
Gain Flatness vs. Frequency	G_{VAR_FREQ}	f_{RF} = 14GHz–17GHz	-	2	-	dB
		Within any 250MHz	-	0.2	-	dB
Noise Figure	NF	-	-	1.5	-	dB
Output 1dB Compression Point	OP1dB	-	-	-1.5	-	dBm
Output 3rd Order Intercept Point	OIP3	Pin = -35 dBm/tone, Δf = 1MHz	-	10	-	dBm
Input Return Loss	IRL	-	-	21	-	dB
Output Return Loss	ORL	-	-	15	-	dB
Reverse Isolation	ISO	-	-	35	-	dB
Channel-to-Channel Isolation	ISO_{CH-CH}	S21-S41. f_{RF} = 14GHz–17GHz	35	-	-	dB

3. Typical Application Circuits

Figure 3 shows two typical application circuits for biasing the F6923.

The top circuit uses a voltage source Vref to supply the bias reference current IREF through an external resistor Rref. Vref should be set to achieve the recommended IREF bias currents per the indicated formula. For the typical relationship between Viref and IREF, see Figure 13.

The bottom circuit uses the programmable IDAC of the Renesas F61xx beamforming device to provide the reference current directly to the F6923.

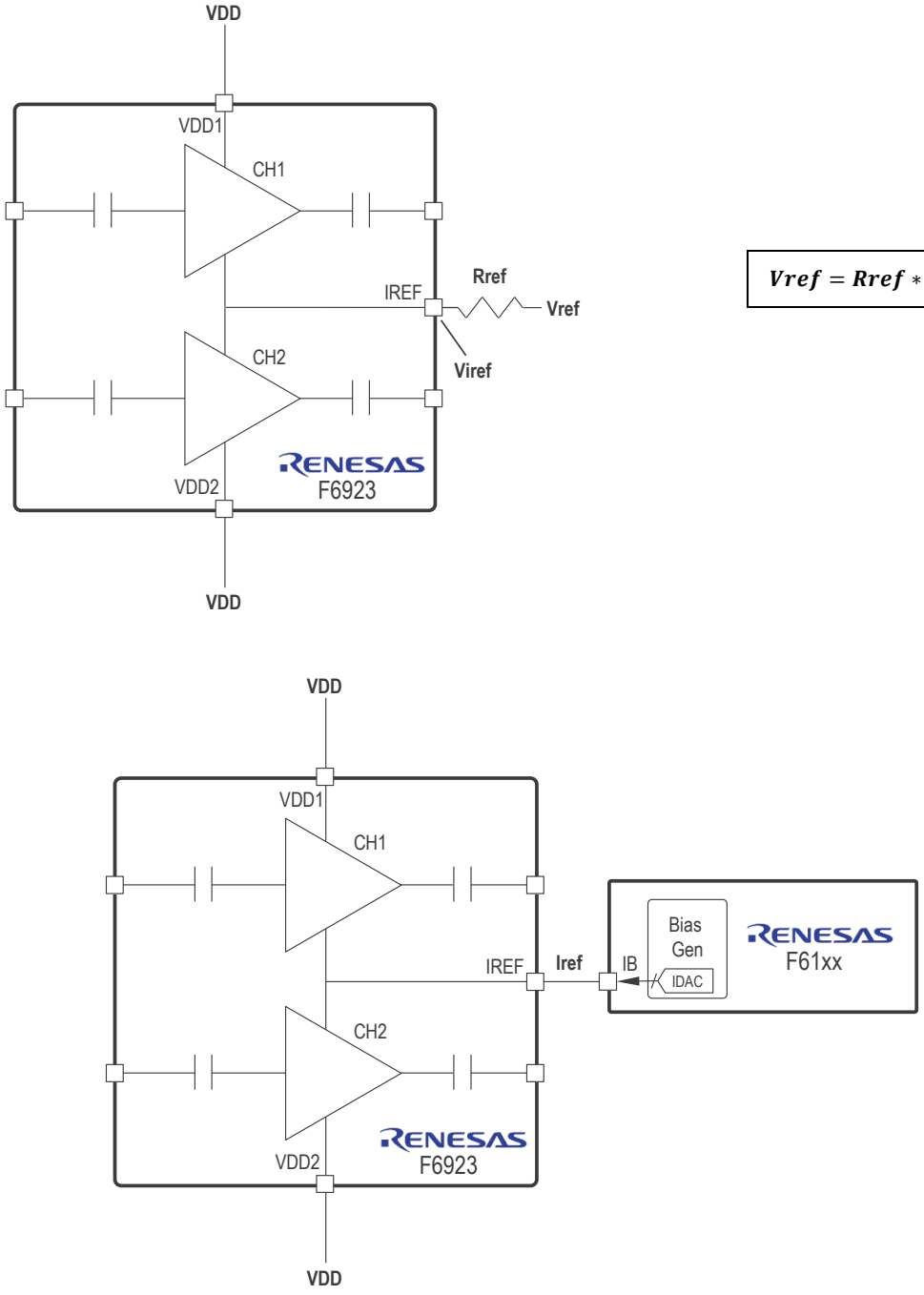


Figure 3. Typical Application Circuits

4. Typical Performance Characteristics

Unless stated otherwise, $Z_S = Z_L = 50\Omega$ on all RF ports, V_{DD} = 0.95V, and T_{AMB} = 25°C.

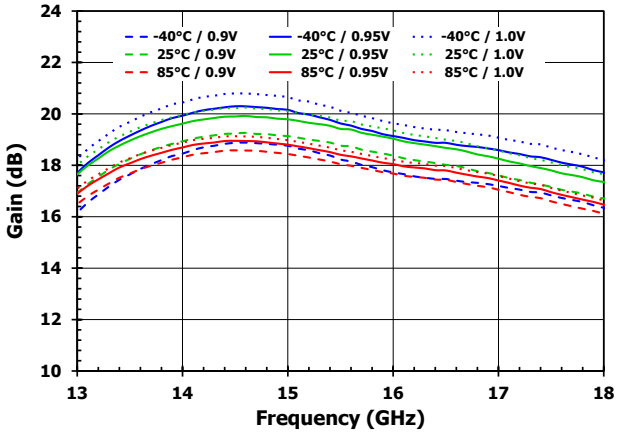


Figure 4. Gain

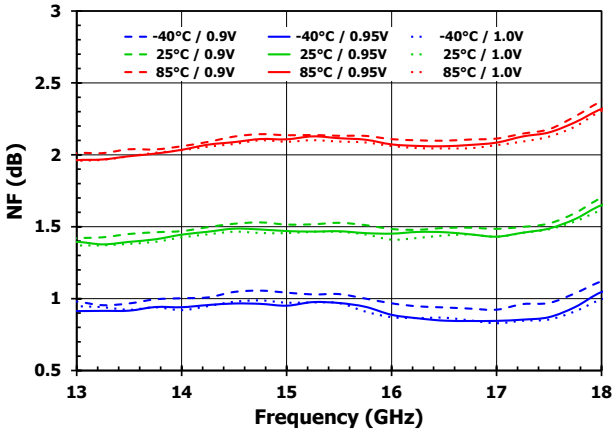


Figure 5. Noise Figure

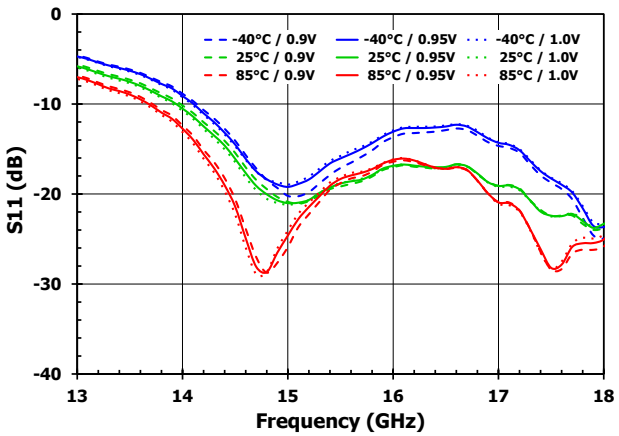


Figure 6. Input Match

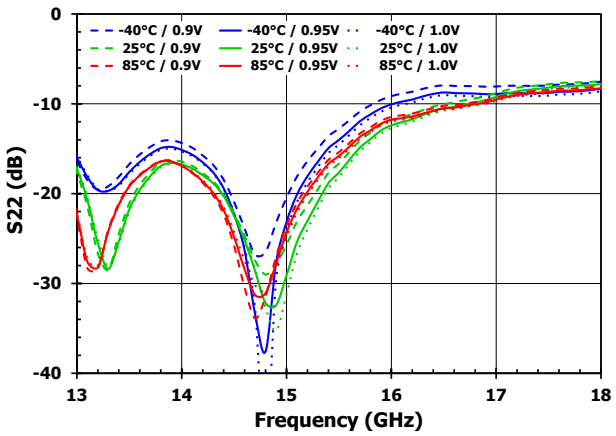


Figure 7. Output Match

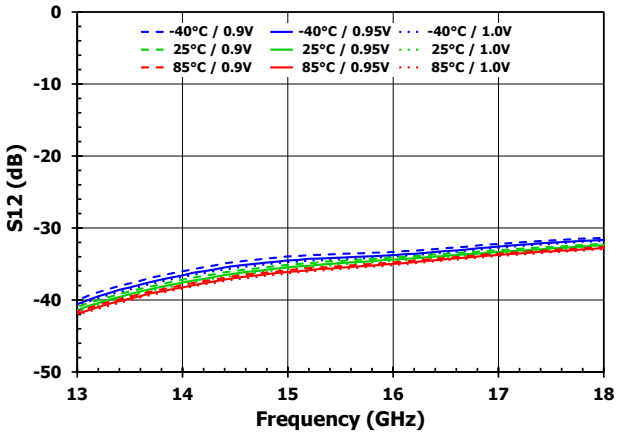


Figure 8. Input-to-Output Isolation

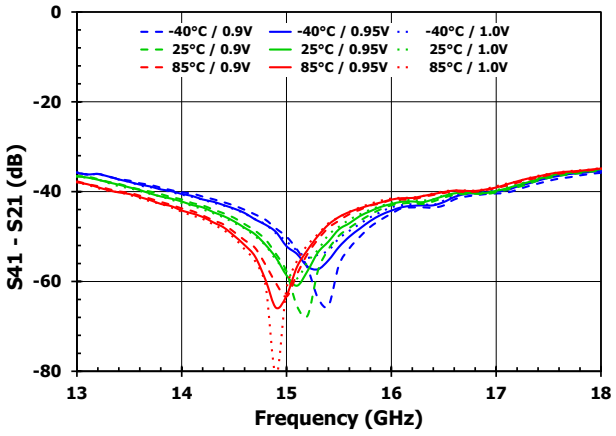


Figure 9. Channel-to-Channel Isolation

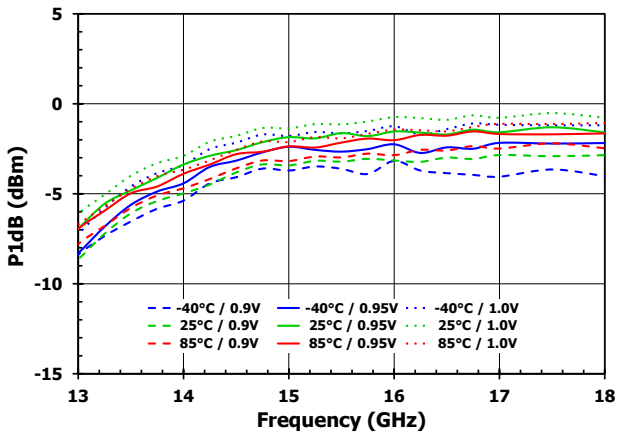


Figure 10. Output 1dB Compression

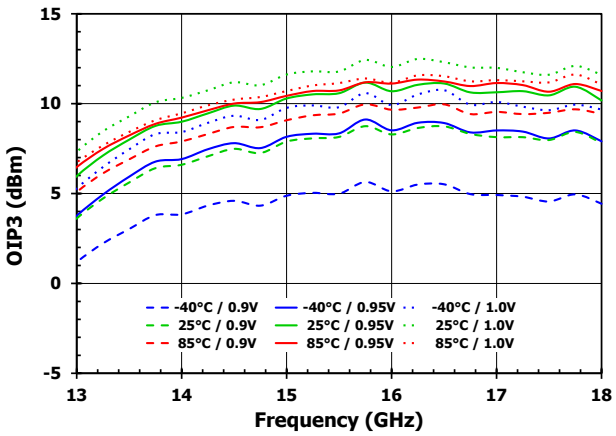


Figure 11. Output Third Order Intercept

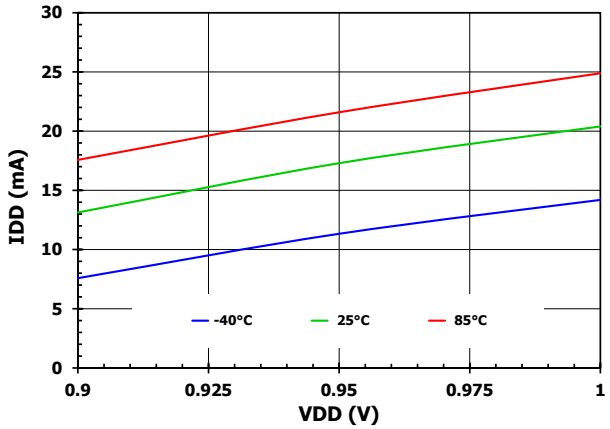


Figure 12. Supply Current, Per Channel

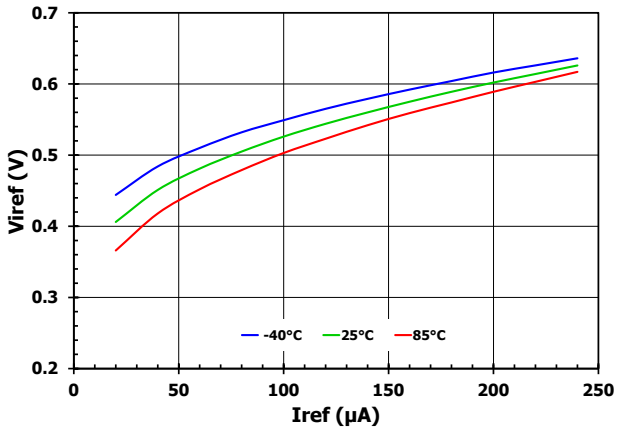


Figure 13. IREF Pin Voltage vs Current

5. Evaluation Board

For more information about the evaluation board, see the *F69xx Evaluation Board Manual* on the F6923 product page.

5.1 Evaluation Board Photos

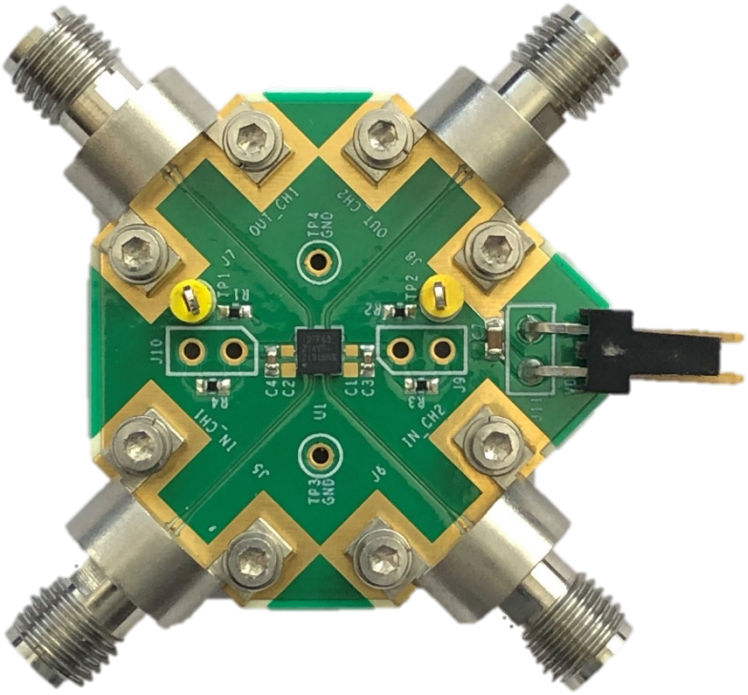


Figure 14. Evaluation Board – Top View

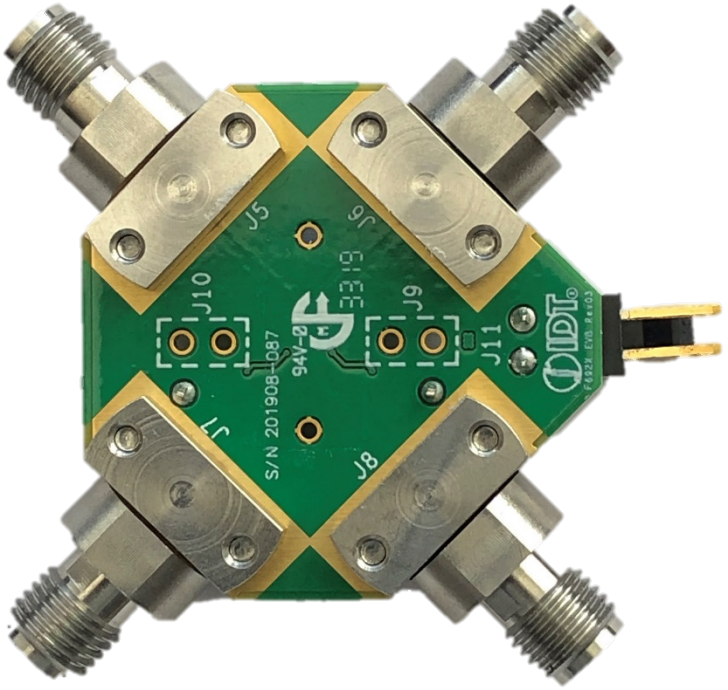


Figure 15. Evaluation Board – Bottom View

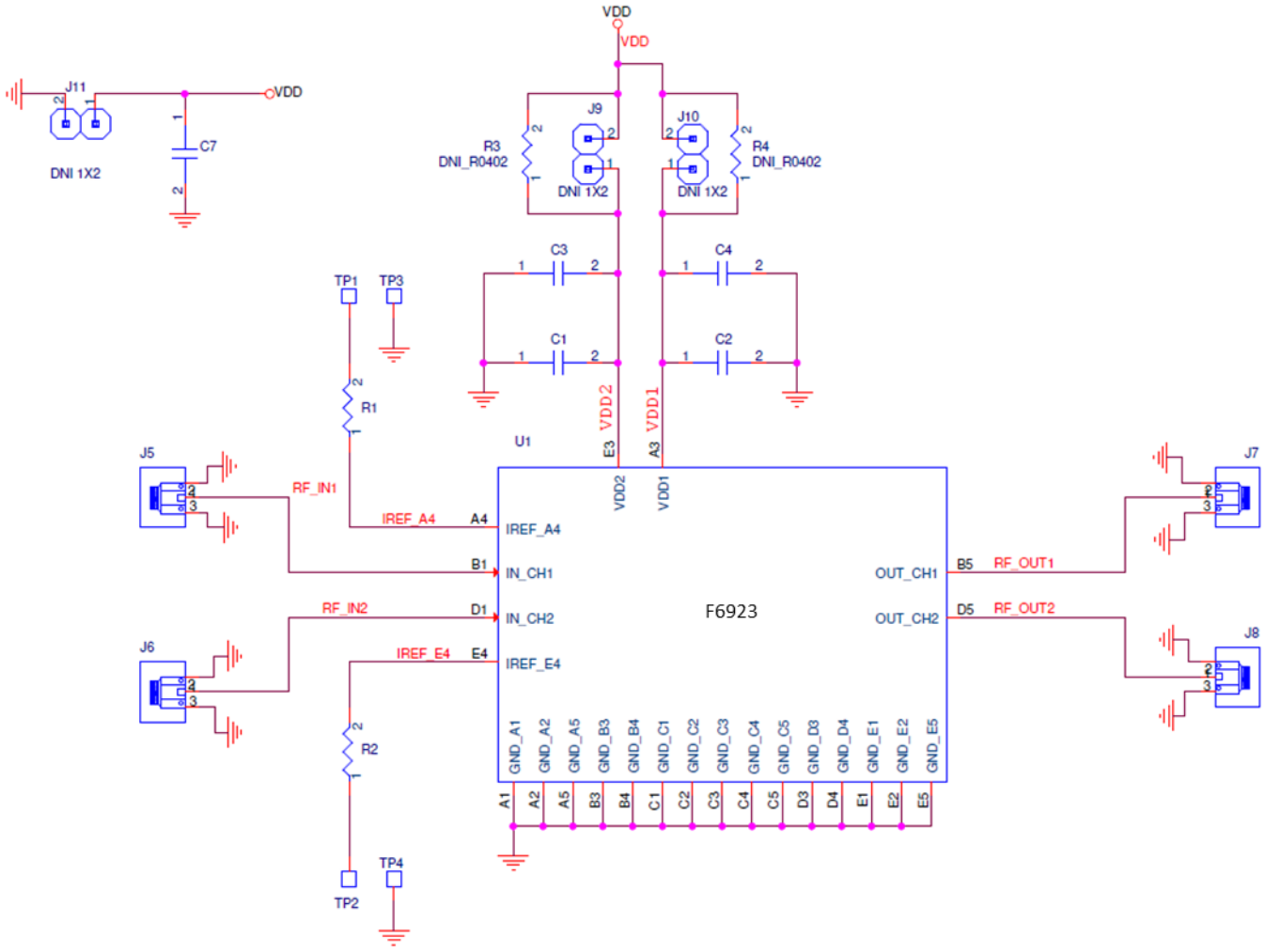


Figure 16. Evaluation Board – Schematic

Table 1. Bill of Material (BOM)

Part Ref.	QTY	Description	Manufacturer Part #	Manufacturer
C1, C2	2	33pF ±5%, 50V, C0G Ceramic Capacitor (0402)	GRM1555C1H330J	MURATA
C3, C4	2	1µF ±10%, 16V, X6S Ceramic Capacitor (0402)	GRM155C81C105K	MURATA
C7	1	10µF ±20%, 16V, X6S Ceramic Capacitor (0603)	GRM188C81C106M	MURATA
R1	1	3.4kΩ ±1%, 1/16W, Resistor (0402)	-	-
R2	1	DNI	-	-
R3, R4 [1]	2	0Ω Resistors (0402)	ERJ-2GE0R00X	PANASONIC
J5-J8	4	Edge Launch 2.92mm 40GHz	ELF-40-002	SIGNAL MICROWAVE
TP1, TP2	2	Test Point Yellow	5004	Keystone Electronics
J11	1	CONN HEADER R/A 2POS 2.54MM	1718571002	MOLEX

1. For single channel operation of Ch2, remove R4 to disconnect VDD1 from the VDD supply pin.

5.2 Evaluation Board Operation

This section provides basic information on operating the F6923 evaluation board. For more information about the evaluation board, see the *F69xx Evaluation Board Manual* on the F6923 product page.

5.2.1. Single Power Supply Operation

Connect the positive and negative outputs of a power supply (V_{DD}) to J11. In addition, connect the positive output of the V_{DD} supply to TP1. While there are two I_{REF} pins on the F6923 device (which are individually accessible via TP1 and TP2 on the evaluation board), these pins (A4 and E4) are internally connected to the same node on the IC, simultaneously controlling the bias of channels 1 and 2. Set the power supply to 0.95V and enable the power supply output. Monitor the V_{DD} supply output current to confirm the nominal bias point is set correctly (approximately 34mA).

5.2.2. Independent VDD and IREF Bias Control

5.2.2.1. Two Voltage Sources

Connect the positive and negative outputs of a power supply (V_{DD}) to J11. In addition, connect the positive output of a second supply (V_{REF}) to TP1 and the negative output to the negative output of the V_{DD} supply. Set both power supplies to 0.95V and enable the power supply outputs. Monitor the I_{DD} of the V_{DD} supply to confirm the nominal bias point is set correctly (approximately 34mA).

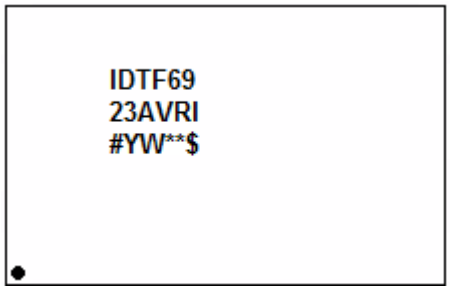
5.2.2.2. Voltage Source and Current Source

Connect the positive and negative outputs of a power supply (V_{DD}) to J11. In addition, connect an independent current supply (I_{REF}) to TP1 and the ground of the current supply to the negative terminal of the V_{DD} supply. Set V_{DD} to 0.95V, I_{REF} to 110µA and enable the power supply outputs. Monitor the I_{DD} of the V_{DD} supply to confirm the nominal bias point is set correctly (approximately 34mA).

6. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see Ordering Information for POD links). The package information is the most current data available and is subject to change without revision of this document.

7. Marking Diagram



- Lines 1 and 2: Renesas part number
- Line 3:
  - “#” is the device step
  - “YW” is the last digit of the year and workweek code
  - “**” is the lot sequential code
  - “$” is the mark location code

8. Ordering Information

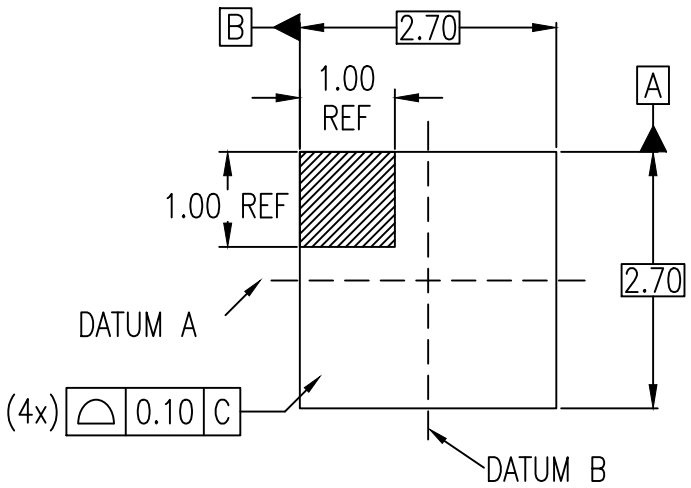
Part Number	Package	MSL Rating	Carrier Type	Temperature Range
F6923AVRI	2.7 × 2.7 × 0.9 mm 23-BGA	3	Tray	-40°C to +85°C
F6923AVRI8	2.7 × 2.7 × 0.9 mm 23-BGA	3	Reel	-40°C to +85°C
F6923EVB	F6923 Evaluation Board			

9. Revision History

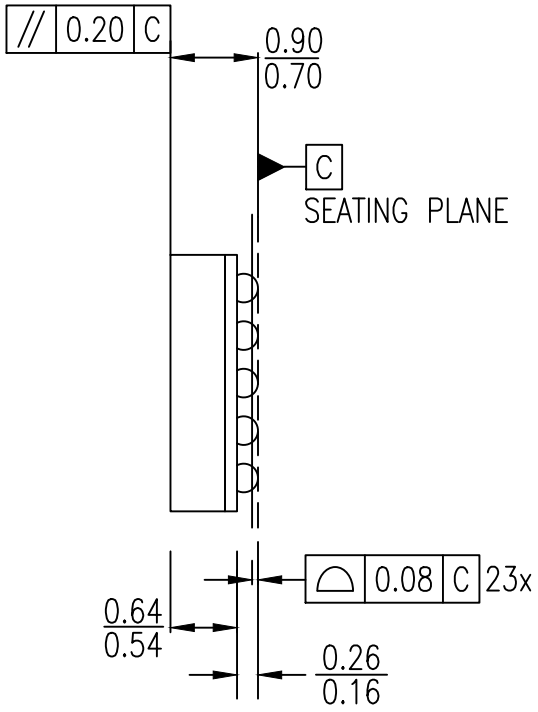
Revision	Date	Description
1.02	Nov 14, 2024	Updated Applications section on page 1.
1.01	Sep 17, 2024	▪ Updated VDD1 and VDD2 pin descriptions in section 1.2. ▪ Added EVB BOM note about single channel operation in Table 1.
1.00	Jul 6, 2021	Initial release.

23-FCCSP, Package Outline Drawing

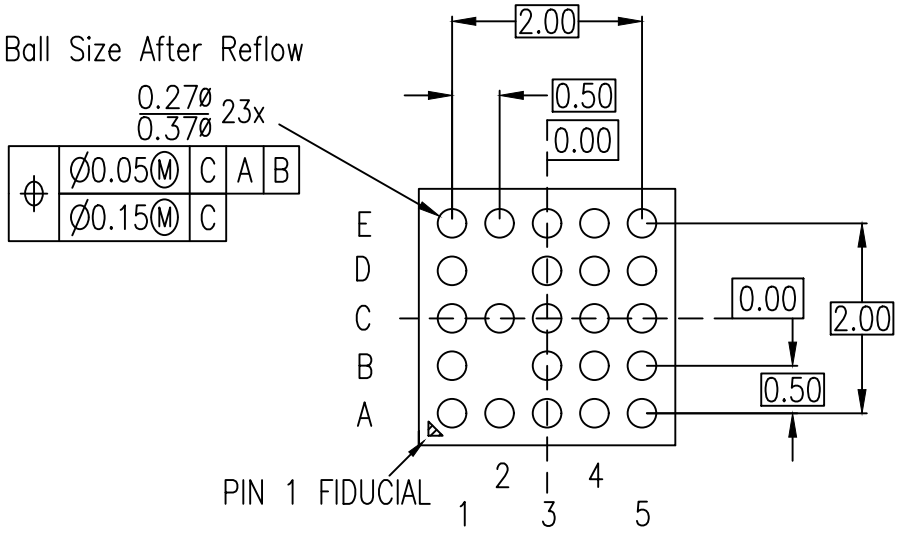
2.7 x 2.7 x 0.9 mm Body, 0.50 mm Pitch,
AVR23D1, PSC-4781-01, Rev 00, Page 1



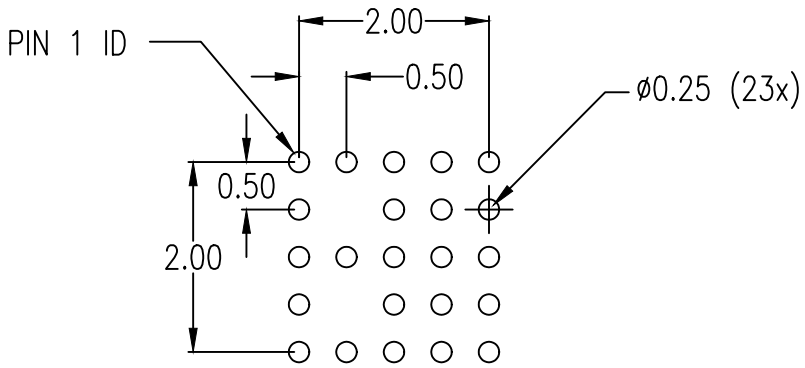
TOP VIEW



SIDE VIEW



BOTTOM VIEW
(BALL SIDE VIEW)



RECOMMENDED LAND PATTERN DIMENSION
(TOP VIEW)

NOTES:
1. ALL DIMENSION ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

Package Revision History		
Date Created	Rev No.	Description
Dec. 6, 2018	Rev 00	Initial Release

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