DA14850

AI Enable Low-Power Audio Processor

The DA14850 is Renesas Electronics next generation low power audio processor. The device combines Renesas Smart Codecs and PMIC devices to form a flexible, powerful chipset optimized for low power consumption and high-performance audio products. The DA14850 integrates an ARM® Cortex® M33F application processor, a Tensilica® Fusion F1 DSP, and a rich set of peripherals and communication interfaces including USB 2.0 HS/FS.

The DA14850 features multi-core AI (artificial intelligent) capability. The device integrated a dedicated low-power NNP (neural network processor) technology to support VAD (voice activity detection), HWD (hot-word-detection), acoustic event detection (ex. glass breaking, police car siren, and so on.), and audio scene detection (ex. restaurant, music, and so on.) to offer Machine-Learning contexture awareness features. The Renesas Electronics Reality AI tool seamlessly works with the integrated Cadence Fusion F1 DSP processor in DA14850. Renesas Electronics Reality AI tool comes with Renesas Electronics global support including AI model generation at highly compact code, design review, monitor tool, and many optional add-ons.

Renesas Electronics DA14850 processor enables USB audio applications as well as battery powered portable applications for sound detection and hearing enhancement.

Renesas Electronics ADP (Audio Development Platform) is a unified software development kit for the DA14850 and DA14870 product families. It comprises an extensive library of example projects, DSP libraries, peripheral drivers, a USB stack, along with the applicable classic Bluetooth audio, and Bluetooth® LE-Audio (Bluetooth Low Energy) protocol stack, as well as the API. The companion software includes Renesas Electronics AvStudio for audio tuning and configuration tool.

Key Benefits:

- Power consumption critical audio applications
- Optimized to work with one of the most power efficient Renesas Electronics PMICs
- A dedicated low power NNP core (neural network processor) for customizable audio detection such as hot-word-detection, acoustic event detection, and scene detection
- Multi-core AI (artificial intelligent) capability for best use case partitioning
- Comes with Renesas Electronics Reality AI tool for cloud base ML (machine learning) model generation*
- One audio platform approach of ADP (audio development platform) for Renesas USB and Bluetooth SoCs

Key Features

- Flexible processing power:
  - 40 MHz up to 160 MHz 32-bit ARM® Cortex® M33F
  - 40 MHz up to 320 MHz Tensilica Fusion F1 DSP
  - Always-on low power NNP for Voice Activation Detection (VAD) and Hot-Word Detector (HWD) engine
- Memories:
  - 256 kB System RAM
  - 1280 kB DSP RAM
  - External RAM expansion capability
  - 8 kB M33F Cache SRAM
  - 8 kB PSRAM Data cache
  - 4 kB One-Time-Programmable (OTP) memory
- Memory interfaces:
  - 80 MHz Quad/Octa SPI FLASH controller with On-the-fly M33 XIP decryption
  - 80 MHz Quad SPI PSRAM/FLASH Controller
- Clocking:
  - RCX32 kHz for start-up and standby (wake-up timer) with Real Time Clock (option for 32 kHz crystal)
  - 40 MHz crystal with 80 MHz Low-Power mode
  - 320 MHz SYS-PLL
  - 98.304/90.3168 MHz Fractional PLL for the audio clock domain
- Security:
  - Cryptographic engine with AES- 128/192/256, SHA-224/256
  - RAM based Entropy for software based True Random Number Generator
  - (TRNG) and FIPS 140-3 compliant DRBG
- Timers:
  - 5x General purpose timers, 24-bit/32-bit up/down timers with PWM

- 3x Watchdog timers
- Clock calibration circuit
- 3x Phase counters

- RTC:
  - 10 ms resolution
- Debug:
  - ARM CoreSight SoC-400 with single SWD interface for debugging Fusion F1 and M33
  - M33F External Trace Module (ETM)
  - M33F on-chip Micro Trace Buffer (MTB)
- Power management:
  - 0.95 V Analog
  - 1.8 V Analog
  - 0.8 V Digital
  - 3.3 V USB
  - 1.2 V and 1.8 V VDDIO selectable supply voltage
  - Power-On Reset and brownout detection with programmable thresholds
- Digital interfaces:
  - General Purpose I/Os with programmable pin assignment up to 25x for WLCSP, 50x for VFBGA
  - 3x UARTs up to 3 Mbps
  - 2x SPI+™ Master/Slave
  - 2x I2C Master/Slave 100 kHz, 400 kHz or 3.4 MHz
  - MIPI I3C controller up-to 12.5 MHz
  - 4x PDM DMIC interface 768 kHz – 4 MHz with hardware down sampler
  - Stereo PDM outs
  - 3x LED timers with load balancing PWM
  - 2x Digital Audio interface (DA) with I2S, PCM, TDM format master/slave interface up to 8x32 bits channels, 8-192 kHz, 11.025-88.4 kHz
  - 6x Sample Rate Converters
  - 8 + 16x DMA channels
- USB:
  - USB 2.0 HS/FS Device only
  - 1x IN/OUT Control Endpoint 0
  - 11x IN/OUT Control, ISOC, Bulk, INT endpoints with Dynamical FIFOs
  - 24 DMA channels
  - LPM L1 (ADC3), LPM L2
- Analog interfaces:
  - 12-bit SAR ADC, 1.5 M samples/s, for 6x external inputs 1.8 V and on-chip supplies and temp sensor measurements
  - On-chip Temperature sensor
- Packages:
  - WLCSP64, 2.90x3.42 mm2. Mixed pitch. 0.35 mm, 0.22 mm ball, staggered as fcBGA
  - VFBGA104, 4.20x4.65 mm2, staggered pitch 0.6 mm horizontal, 0.25 mm vertical, 0.22 mm ball

Applications

- USB headset, headphone, headphone processing amplifier
- USB and or wireless microphone
- USB speaker phones
- Portable audio processor/Co-processor
- Portable camera
- Hearing aids and Assistive sound systems
- Low power portable voice command applications
- Sound detection applications

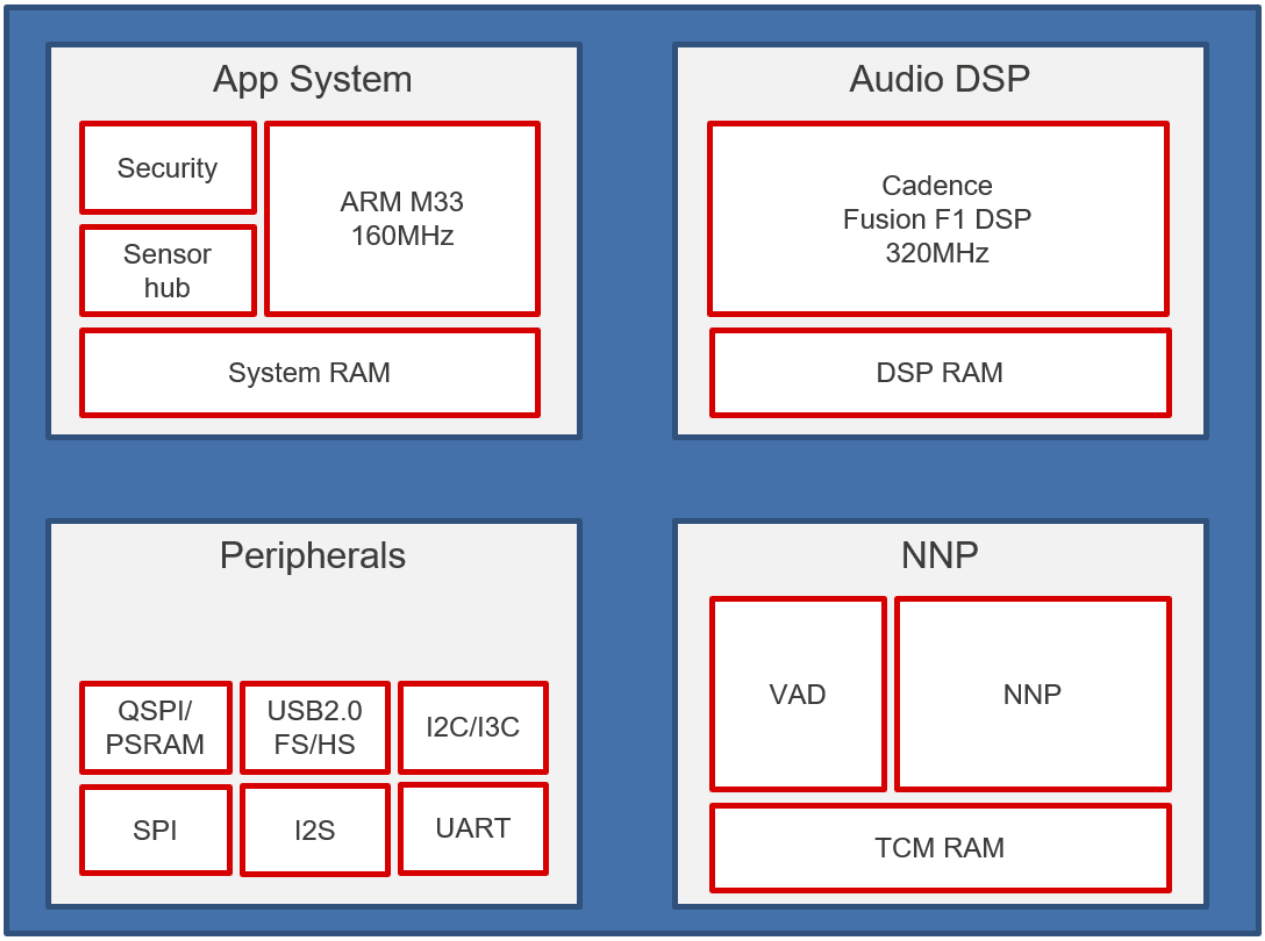

Figure 1. DA14850 block diagram

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1. Moisture Sensitivity Level

The Moisture Sensitivity Level (MSL) is an indicator for the maximum allowable time period (floor lifetime) in which a moisture sensitive plastic device, when removed from the dry bag, can be exposed to an environment with a maximum temperature of 30 °C and a maximum relative humidity of 60% RH before the solder reflow process.

WLCSP64 is qualified for MSL 1.

VFBGA104 package is qualified for MSL 3.

Table 1. MSL definitions

MSL level	Floor lifetime
MSL 4	72 hours
MSL 3	168 hours
MSL 2A	4 weeks
MSL 2	1 year
MSL 1	Unlimited at 30 °C/85%RH

2. Soldering Information

Refer to the IPC/JEDEC standard J-STD-020 for relevant soldering information. This document can be downloaded from http://www.jedec.org.

3. Package Outline Drawings

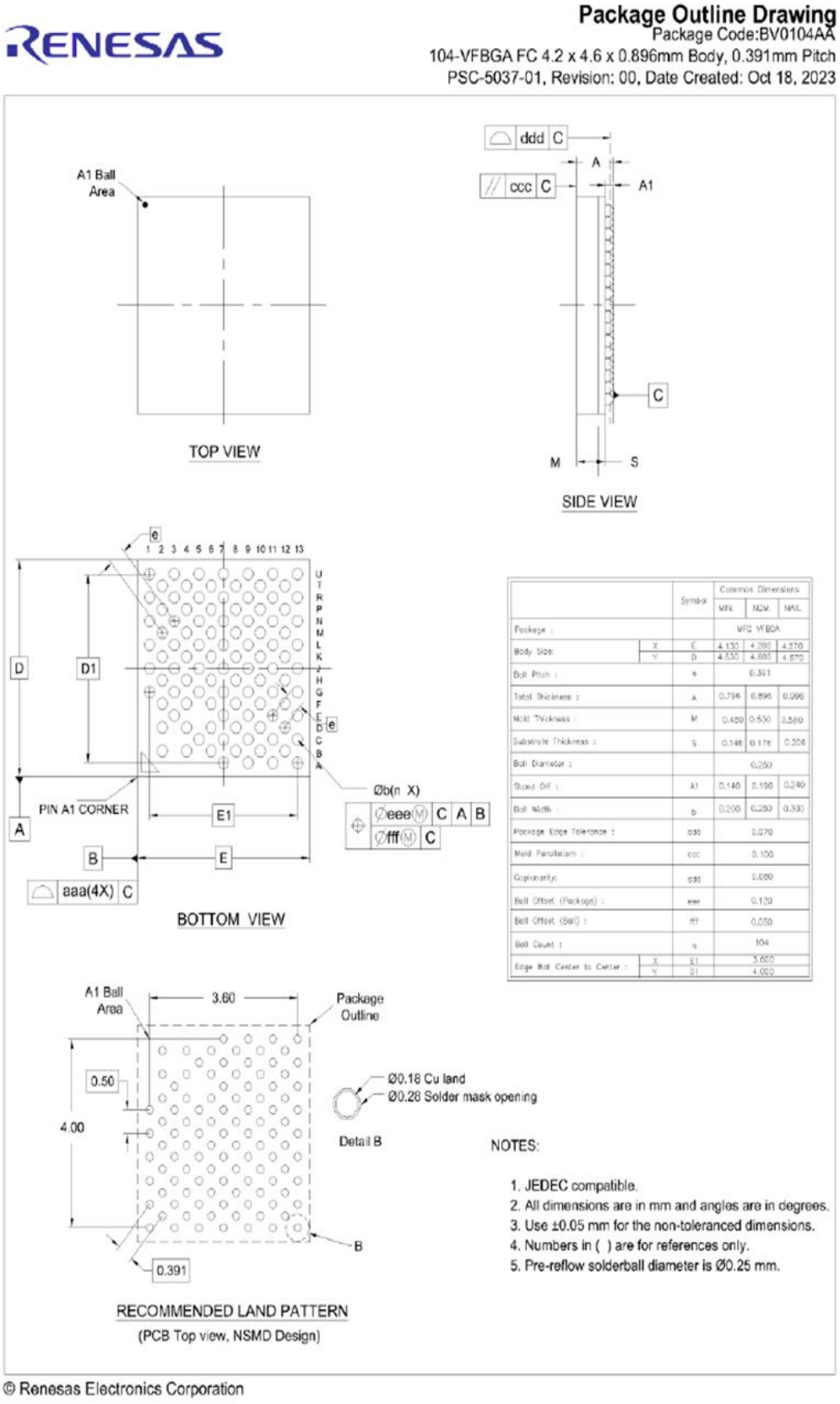

Figure 2. VFBGA104L package outline drawing

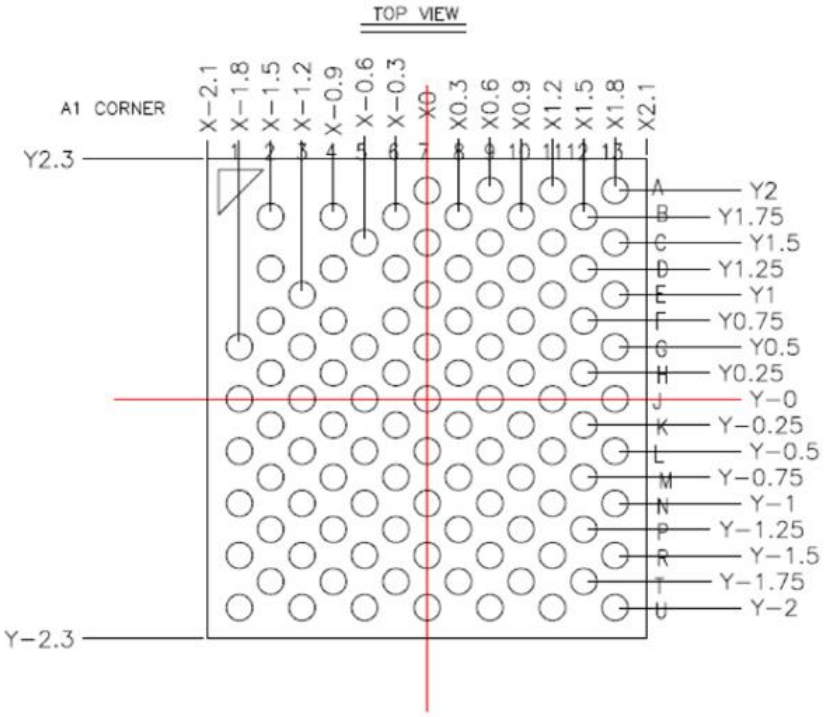

Figure 3. VFBGA104L ball coordinates (top view)

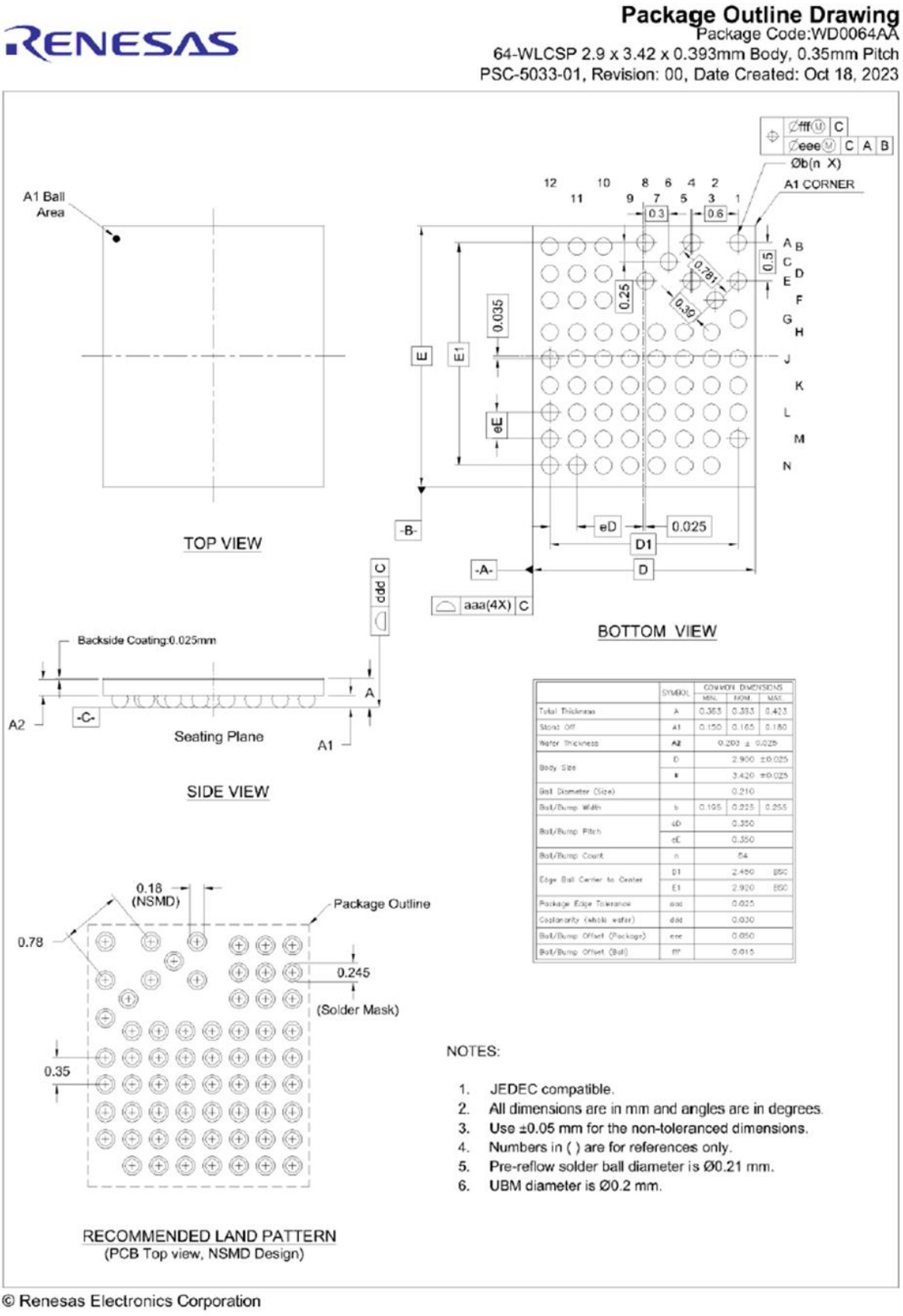

Figure 4. WLCSP64L outline drawing

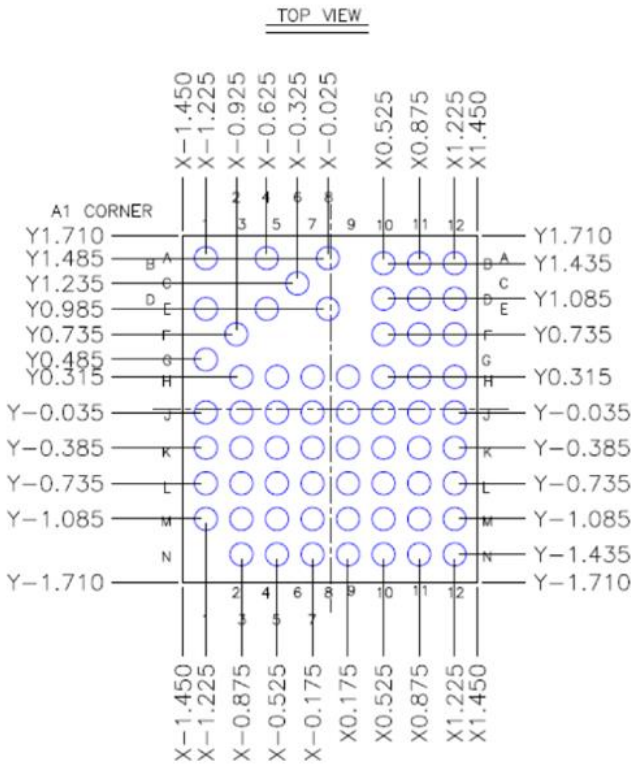

Figure 5. WLCSP64L ball coordinates (top view)

4. Ordering Information

Table 2. Ordering information

Device	Package	NNP	CPU memory	DSP memory	PSRAM interface	Size (mm)	Shipment form	Pack quantity Production Note 1
DA14850-10D00GH2	WLCSP64	No	256 kB	1280 kB	No	2.90 x 3.42	Reel	6000
DA14850-10N00GH2	WLCSP64	Yes	256 kB	1280 kB	No	2.90 x 3.42	Reel	6000
DA14850-11D00H22	VFBGA104	No	256 kB	1280 kB	Yes	4.20 x 4.60	Reel	5000
DA14850-11N00H22	VFBGA104	Yes	256 kB	1280 kB	Yes	4.20 x 4.60	Reel	5000

Note 1 Contact marketing for sample delivery.

5. Revision History

Revision	Date	Description
1.00	Jan 15, 2024	Initial version.

ROHS Compliance

Renesas Electronics' suppliers certify that its products are in compliance with the requirements of Directive 2011/65/EU of the European Parliament on the restriction of the use of certain hazardous substances in electrical and electronic equipment. RoHS certificates from our suppliers are available on request.