## Description

The 9ZXL1251 meets the demanding requirements of the Intel DB1200ZL specification, including the critical low-drift requirements of Intel CPUs. It is pin compatible to the 9ZXL1231 and integrates 24 termination resistors, saving 41mm$^2$ board area.

## Applications

Buffer for Romley, Grantley and Purley Servers, solid state storage and PCIe

## Output Features

- 12 LP-HCSL Output Pairs w/integrated terminations (Zo = 85Ω)

## Key Specifications

- Cycle-to-cycle jitter < 50ps
- Output-to-output skew < 50ps
- Input-to-output delay variation < 50ps
- PCIe Gen3 phase jitter < 1.0ps RMS
- Phase jitter: QPI/UPI > = 9.6GB/s < 0.2ps rms
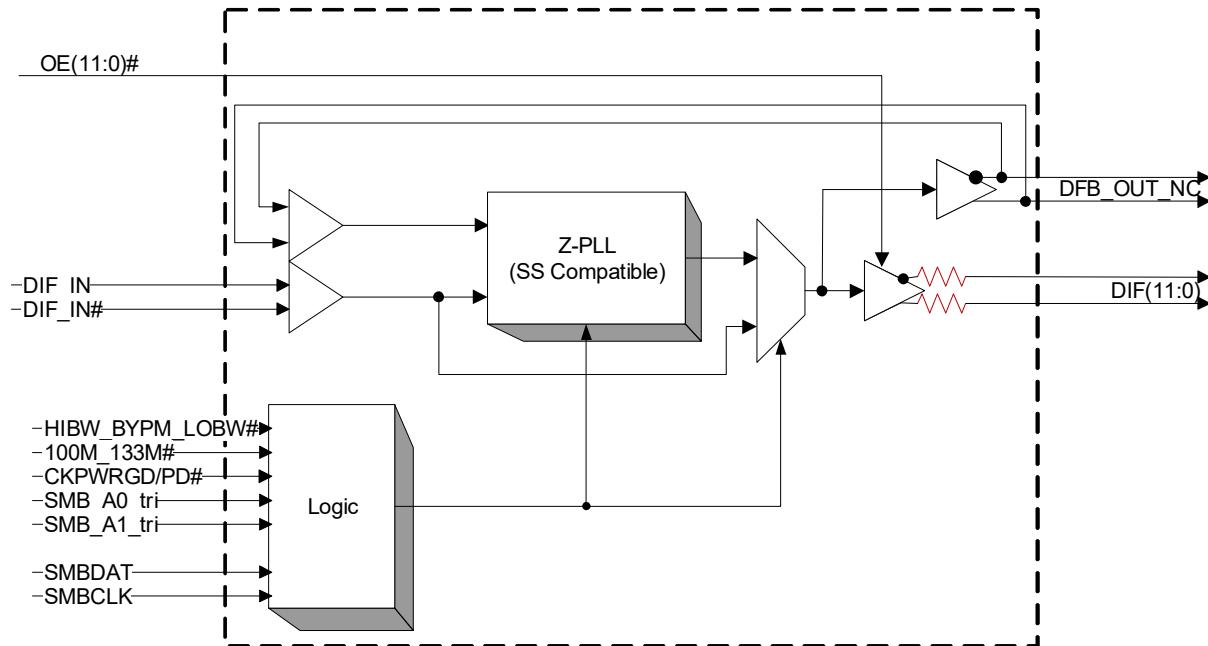
## Features

- 25MHz PFT clock delay management
- 85Ω Low-power push-pull HCSL outputs; eliminate 24 resistors, save 41mm$^2$ of area
- Pin compatible to 9ZX21201 and 9ZXL1231; easy path to power and area savings
- Space-saving 64-pin VFQFPN package
- Fixed feedback path for 0ps input-to-output delay
- 9 selectable SMBus addresses; multiple devices can share the same SMBus segment
- 12 OE# pins; hardware control of each output
- PLL or bypass mode; supports common and separate clock architectures
- Selectable PLL bandwidth; minimizes jitter peaking in downstream PLLs
- Spread spectrum compatible; tracks spreading input clock for low EMI
- -40°C to +85°C device available; supports demanding environmental applications

## Block Diagram



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January 28, 2021

# Pin Configuration
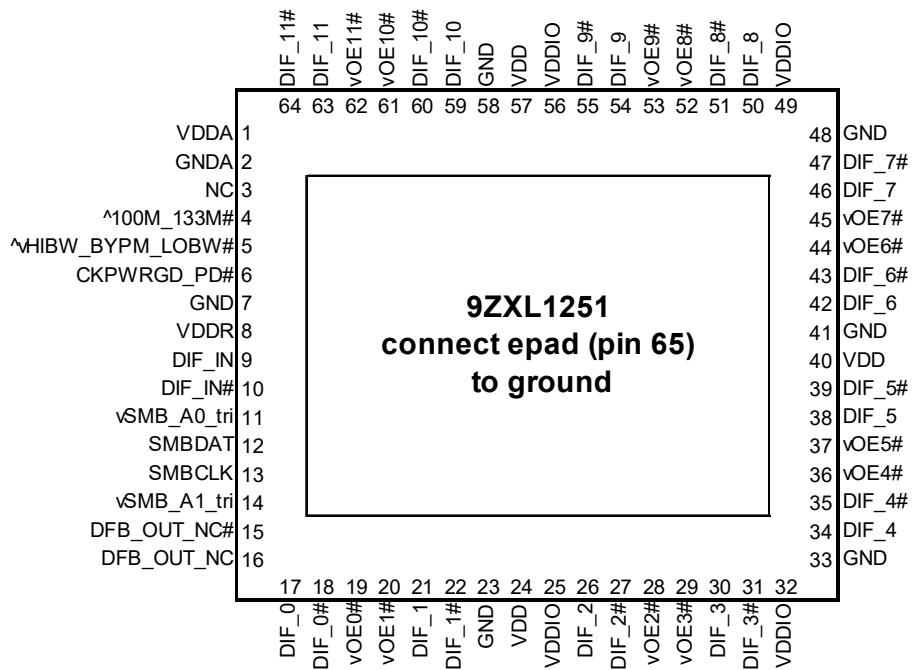


**9 x 9mm VFQFPN package**

Note: Pins with ^ prefix have internal 120K pullup
Pins with v prefix have internal 120K pulldowm
Pins with ^v prefix have internal 120K pullup/pulldown (biased to VDD/2)

## Power Management Table

| CKPWRGD_PD# | DIF_IN/ DIF_IN# | SMBus EN bit | DIF(11:0)/ DIF(11:0)# | PLL STATE IF NOT IN BYPASS MODE |
|---|---|---|---|---|
| 0 | X | X | Low/Low | OFF |
| 1 | Running | 0 | Low/Low | ON |
| | | 1 | Running | ON |

## Functionality at Power-up (PLL mode)

| 100M_133M# | DIF_IN MHz | DIF(11:0) |
|---|---|---|
| 1 | 100.00 | DIF_IN |
| 0 | 133.33 | DIF_IN |

## Power Connections

| Pin Number | | | Description |
|---|---|---|---|
| **VDD** | **VDDIO** | **GND** | |
| 1 | | 2 | Analog PLL |
| 8 | | 7 | Analog Input |
| 24,40,57 | 25,32,49,56 | 23,33,41,48, 58,65 | DIF clocks |

## PLL Operating Mode Readback Table

| HiBW_BypM_LoBW# | Byte0, bit 7 | Byte 0, bit 6 |
|---|---|---|
| Low (Low BW) | 0 | 0 |
| Mid (Bypass) | 0 | 1 |
| High (High BW) | 1 | 1 |

## PLL Operating Mode

| HiBW_BypM_LoBW# | MODE |
|---|---|
| Low | PLL Lo BW |
| Mid | Bypass |
| High | PLL Hi BW |

**NOTE: PLL is OFF in Bypass Mode**

## 9ZXL1251 SMBus Addressing

| Pin | | SMBus Address |
|---|---|---|
| SMB_A1_tri | SMB_A0_tri | |
| 0 | 0 | D8 |
| 0 | M | DA |
| 0 | 1 | DE |
| M | 0 | C2 |
| M | M | C4 |
| M | 1 | C6 |
| 1 | 0 | CA |
| 1 | M | CC |
| 1 | 1 | CE |

## Pin Descriptions

| PIN # | PIN NAME | TYPE | DESCRIPTION |
|---|---|---|---|
| 1 | VDDA | PWR | Power for the PLL core. |
| 2 | GNDA | GND | Ground pin for the PLL core. |
| 3 | NC | N/A | No Connection. |
| 4 | ^100M_133M# | IN | 3.3V Input to select operating frequency. This pin has an internal pull-up resistor. See Functionality Table for Definition |
| 5 | ^vHIBW_BYPM_LOBW# | LATCHED IN | Trilevel input to select High  BW, Bypass or Low  BW mode. This pin is biased to VDD/2 (Bypass mode) with internal pull up/pull down resistors. See PLL Operating Mode Table for |
| 6 | CKPWRGD_PD# | IN | 3.3V Input notifies device to sample latched inputs and start up on first high assertion, or exit Power Down Mode on subsequent assertions.  Low enters Power Down Mode. |
| 7 | GND | GND | Ground pin. |
| 8 | VDDR | PWR | 3.3V power for differential input clock (receiver).  This VDD should be treated as an analog power rail and filtered appropriately. |
| 9 | DIF_IN | IN | HCSL True input |
| 10 | DIF_IN# | IN | HCSL Complementary Input |
| 11 | vSMB_A0_tri | IN | SMBus address bit.  This is a tri-level input that works in conjunction with the SMB_A1 to decode 1 of 9 SMBus Addresses. It has an internal 120Kohm pull down resistor. |
| 12 | SMBDAT | I/O | Data pin of SMBUS circuitry, 5V tolerant |
| 13 | SMBCLK | IN | Clock pin of SMBUS circuitry, 5V tolerant |
| 14 | vSMB_A1_tri | IN | SMBus address bit.  This is a tri-level input that works in conjunction with the SMB_A0 to decode 1 of 9 SMBus Addresses.  It has an internal 120Kohm pull down resistor. |
| 15 | DFB_OUT_NC# | OUT | Complementary half of differential feedback output, provides feedback signal to the PLL for synchronization with input clock to eliminate phase error. This pin should NOT be connected on the circuit board, the feedback is internal to the package. |
| 16 | DFB_OUT_NC | OUT | True half of differential feedback output, provides feedback signal to the PLL for synchronization with the input clock to eliminate phase error. This pin should NOT be connected on the circuit board, the feedback is internal to the package. |
| 17 | DIF_0 | OUT | HCSL true clock output |
| 18 | DIF_0# | OUT | HCSL Complementary clock output |
| 19 | vOE0# | IN | Active low input for enabling DIF pair 0. This pin has an internal pull-down. 1 =disable outputs,  0 = enable outputs |
| 20 | vOE1# | IN | Active low input for enabling DIF pair 1.  This pin has an internal pull-down. 1 =disable outputs,  0 = enable outputs |
| 21 | DIF_1 | OUT | HCSL true clock output |
| 22 | DIF_1# | OUT | HCSL Complementary clock output |
| 23 | GND | GND | Ground pin. |
| 24 | VDD | PWR | Power supply, nominal 3.3V |
| 25 | VDDIO | PWR | Power supply for differential outputs |
| 26 | DIF_2 | OUT | HCSL true clock output |
| 27 | DIF_2# | OUT | HCSL Complementary clock output |
| 28 | vOE2# | IN | Active low input for enabling DIF pair 2.  This pin has an internal pull-down. 1 =disable outputs,  0 = enable outputs |
| 29 | vOE3# | IN | Active low input for enabling DIF pair 3.  This pin has an internal pull-down. 1 =disable outputs,  0 = enable outputs |
| 30 | DIF_3 | OUT | HCSL true clock output |
| 31 | DIF_3# | OUT | HCSL Complementary clock output |
| 32 | VDDIO | PWR | Power supply for differential outputs |
| 33 | GND | GND | Ground pin. |
| 34 | DIF_4 | OUT | HCSL true clock output |
| 35 | DIF_4# | OUT | HCSL Complementary clock output |
| 36 | vOE4# | IN | Active low input for enabling DIF pair 4.  This pin has an internal pull-down. 1 =disable outputs,  0 = enable outputs |
| 37 | vOE5# | IN | Active low input for enabling DIF pair 5.  This pin has an internal pull-down. 1 =disable outputs,  0 = enable outputs |

## Pin Descriptions (cont.)

| PIN # | PIN NAME | TYPE | DESCRIPTION |
|---|---|---|---|
| 38 | DIF_5 | OUT | HCSL true clock output |
| 39 | DIF_5# | OUT | HCSL Complementary clock output |
| 40 | VDD | PWR | Power supply, nominal 3.3V |
| 41 | GND | GND | Ground pin. |
| 42 | DIF_6 | OUT | HCSL true clock output |
| 43 | DIF_6# | OUT | HCSL Complementary clock output |
| 44 | vOE6# | IN | Active low input for enabling DIF pair 6.  This pin has an internal pull-down.<br>1 =disable outputs,  0 = enable outputs |
| 45 | vOE7# | IN | Active low input for enabling DIF pair 7.  This pin has an internal pull-down.<br>1 =disable outputs,  0 = enable outputs |
| 46 | DIF_7 | OUT | HCSL true clock output |
| 47 | DIF_7# | OUT | HCSL Complementary clock output |
| 48 | GND | GND | Ground pin. |
| 49 | VDDIO | PWR | Power supply for differential outputs |
| 50 | DIF_8 | OUT | HCSL true clock output |
| 51 | DIF_8# | OUT | HCSL Complementary clock output |
| 52 | vOE8# | IN | Active low input for enabling DIF pair 8.  This pin has an internal pull-down.<br>1 =disable outputs,  0 = enable outputs |
| 53 | vOE9# | IN | Active low input for enabling DIF pair 9.  This pin has an internal pull-down.<br>1 =disable outputs,  0 = enable outputs |
| 54 | DIF_9 | OUT | HCSL true clock output |
| 55 | DIF_9# | OUT | HCSL Complementary clock output |
| 56 | VDDIO | PWR | Power supply for differential outputs |
| 57 | VDD | PWR | Power supply, nominal 3.3V |
| 58 | GND | GND | Ground pin. |
| 59 | DIF_10 | OUT | HCSL true clock output |
| 60 | DIF_10# | OUT | HCSL Complementary clock output |
| 61 | vOE10# | IN | Active low input for enabling DIF pair 10.  This pin has an internal pull-down.<br>1 =disable outputs,  0 = enable outputs |
| 62 | vOE11# | IN | Active low input for enabling DIF pair 11. This pin has an internal pull-down.<br>1 =disable outputs,  0 = enable outputs |
| 63 | DIF_11 | OUT | HCSL true clock output |
| 64 | DIF_11# | OUT | HCSL Complementary clock output |
| 65 | epad | GND | epad, connect to ground |

# Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 9ZXL1251. These ratings, which are standard values for Renesas commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Supply Voltage | VDDx | | | | 4.6 | V | 1,2 |
| Input Low Voltage | $V_{IL}$ | | GND-0.5 | | | V | 1 |
| Input High Voltage | $V_{IH}$ | Except for SMBus interface | | | $V_{DD}$+0.5 | V | 1,3 |
| Input High Voltage | $V_{IHSMB}$ | SMBus clock and data pins | | | 5.5 | V | 1 |
| Storage Temperature | Ts | | -65 | | 150 | °C | 1 |
| Junction Temperature | Tj | | | | 125 | °C | 1 |
| Input ESD protection | ESD prot | Human Body Model | 2000 | | | V | 1 |

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Operation under these conditions is neither implied nor guaranteed.

[3] Not to exceed 4.6V.

# Electrical Characteristics–DIF_IN Clock Input Parameters

$T_{AMB}$ = $T_{COM}$ or $T_{IND}$, unless noted., Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Input Crossover Voltage - DIF_IN | $V_{CROSS}$ | Crossover Voltage | 150 | | 900 | mV | 1 |
| Input Swing - DIF_IN | $V_{SWING}$ | Differential value | 300 | | | mV | 1 |
| Input Slew Rate - DIF_IN | dv/dt | Measured differentially | 0.4 | | 8 | V/ns | 1,2 |
| Input Leakage Current | $I_{IN}$ | $V_{IN}$ = $V_{DD}$ , $V_{IN}$ = GND | -5 | | 5 | uA | |
| Input Duty Cycle | $d_{tin}$ | Measurement from differential waveform | 45 | | 55 | % | 1 |
| Input Jitter - Cycle to Cycle | $J_{DIFIn}$ | Differential Measurement | 0 | | 125 | ps | 1 |

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Slew rate measured through +/-75mV window centered around differential zero.

# Electrical Characteristics–SMBus

$T_{AMB}$ = $T_{COM}$ or $T_{IND}$, unless noted., Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| SMBus Input Low Voltage | $V_{ILSMB}$ | | | | 0.8 | V | |
| SMBus Input High Voltage | $V_{IHSMB}$ | | 2.1 | | $V_{DDSMB}$ | V | |
| SMBus Output Low Voltage | $V_{OLSMB}$ | At $I_{PULLUP}$ | | | 0.4 | V | |
| SMBus Sink Current | $I_{PULLUP}$ | At $V_{OL}$ | 4 | | | mA | |
| Nominal Bus Voltage | $V_{DDSMB}$ | | 2.7 | | 3.6 | V | 1 |
| SCLK/SDATA Rise Time | $t_{RSMB}$ | (Max VIL - 0.15) to (Min VIH + 0.15) | | | 1000 | ns | 1 |
| SCLK/SDATA Fall Time | $t_{FSMB}$ | (Min VIH + 0.15) to (Max VIL - 0.15) | | | 300 | ns | 1 |
| SMBus Operating Frequency | $f_{MAXSMB}$ | Maximum SMBus operating frequency | | | 400 | kHz | 5 |

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Control input must be monotonic from 20% to 80% of input swing.

[3] Time from deassertion until outputs are > 200mV.

[4] DIF_IN input.

[5] The differential input clock must be running for the SMBus to be active.

# Electrical Characteristics–Input/Supply/Common Parameters

$T_{AMB} = T_{COM}$ or $T_{IND}$, unless noted., Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Supply Voltage | VDDx | Supply voltage, except VDDIO | 3.135 | 3.3 | 3.465 | V | |
| Output Supply Voltage | VDDIO | Supply voltage for DIF outputs, if present | 0.95 | 1.05 | 3.465 | V | |
| Ambient Operating Temperature | $T_{AMB}$ | Commercial range ($T_{COM}$) | 0 | | 70 | °C | |
| | | Industrial range ($T_{IND}$) | -40 | | 85 | °C | |
| Input High Voltage | $V_{IH}$ | Single-ended inputs, except SMBus, tri-level inputs | 2 | | $V_{DD}$ + 0.3 | V | |
| Input Low Voltage | $V_{IL}$ | Single-ended inputs, except SMBus, tri-level inputs | GND - 0.3 | | 0.8 | V | |
| Input High Voltage | $V_{IHTRI}$ | Tri-Level Inputs | 2.2 | | $V_{DD}$ + 0.3 | V | |
| Input Mid Voltage | $V_{IMTRI}$ | Tri-Level Inputs | 1.2 | VDD/2 | 1.8 | V | |
| Input Low Voltage | $V_{ILTRI}$ | Tri-Level Inputs | GND - 0.3 | | 0.8 | V | |
| Input Current | $I_{IN}$ | Single-ended inputs, $V_{IN}$ = GND, $V_{IN}$ = VDD | -5 | | 5 | uA | |
| | $I_{INP}$ | Single-ended inputs $V_{IN}$ = 0 V; Inputs with internal pull-up resistors $V_{IN}$ = VDD; Inputs with internal pull-down resistors | -200 | | 200 | uA | |
| Input Frequency | $F_{ibyp}$ | $V_{DD}$ = 3.3 V, Bypass mode | 25 | | 150 | MHz | |
| | $F_{ipll}$ | $V_{DD}$ = 3.3 V, 100MHz PLL mode | 25 | 100.00 | 110 | MHz | |
| | $F_{ipll}$ | $V_{DD}$ = 3.3 V, 133.33MHz PLL mode | 120 | 133.33 | 147 | MHz | |
| Pin Inductance | $L_{pin}$ | | | | 7 | nH | 1 |
| Capacitance | $C_{IN}$ | Logic Inputs, except DIF_IN | 1.5 | | 5 | pF | 1 |
| | $C_{INDIF\_IN}$ | DIF_IN differential clock inputs | 1.5 | | 2.7 | pF | 1,4 |
| | $C_{OUT}$ | Output pin capacitance | | | 6 | pF | 1 |
| Clk Stabilization | $T_{STAB}$ | From $V_{DD}$ Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock | | 0.18 | 1.8 | ms | 1,2 |
| Input SS Modulation Frequency PCIe | $f_{MODINPCIe}$ | Allowable Frequency for PCIe Applications (Triangular Modulation) | 30 | | 33 | kHz | |
| OE# Latency | $t_{LATOE\#}$ | DIF start after OE# assertion DIF stop after OE# deassertion | 4 | | 10 | clocks | 1,2,3 |
| Tdrive_PD# | $t_{DRVPD}$ | DIF output enable after PD# de-assertion | | | 300 | us | 1,3 |
| Tfall | $t_F$ | Fall time of control inputs | | | 5 | ns | 2 |
| Trise | $t_R$ | Rise time of control inputs | | | 5 | ns | 2 |

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Control input must be monotonic from 20% to 80% of input swing.

[3] Time from deassertion until outputs are > 200mV.

[4] DIF_IN input.

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## Electrical Characteristics–DIF Low Power HCSL Outputs

$T_{AMB}$ = $T_{COM}$ or $T_{IND}$, unless noted., Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Slew rate | dV/dt | $T_{AMB}$ = $T_{COM}$, Scope averaging on | 1.6 | 3.3 | 4 | V/ns | 1,2,3 |
| | | $T_{AMB}$ = $T_{IND}$ Scope averaging on | 1.6 | 2.8 | 4.1 | V/ns | 1,2,3 |
| Slew rate matching | ΔdV/dt | Slew rate matching, Scope averaging on | | 7 | 20 | % | 1,2,4 |
| Voltage High | VHigh | Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on) | 660 | 754 | 850 | mV | |
| Voltage Low | VLow | | -150 | 62 | 150 | | |
| Max Voltage | Vmax | Measurement on single ended signal using absolute value. (Scope averaging off) | | 868 | 1150 | mV | |
| Min Voltage | Vmin | | -300 | -64 | | | |
| Crossing Voltage (abs) | Vcross_abs | Scope averaging off | 250 | 453 | 550 | mV | 1,5 |
| Crossing Voltage (var) | Δ-Vcross | Scope averaging off | | 17 | 140 | mV | 1,6 |

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Measured from differential waveform.

[3] Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

[4] Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

[5] Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

[6] The total variation of all Vcross measurements in any particular system. Note that this is a subset of Vcross_min/max (Vcross absolute) allowed. The intent is to limit Vcross induced modulation by setting Δ-Vcross to be smaller than Vcross absolute.

[7] At default SMBus settings.

## Electrical Characteristics–Current Consumption

$T_{AMB}$ = $T_{COM}$ or $T_{IND}$, unless noted., Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Operating Supply Current | $I_{DDA}$ | VDDA, PLL Mode@100MHz | | 13.4 | 20 | mA | 1 |
| | | VDDA, PLL Bypass Mode@100MHz | | 4.8 | 8 | mA | 1 |
| | $I_{DD}$ | All other VDD pins | | 16 | 25 | mA | |
| | $I_{DDIO}$ | VDDIO for DIF outputs, if applicable | | 81 | 95 | mA | |
| Power Down Current | $I_{DDA}$ | VDDA, PLL Mode@100MHz | | 3 | 5 | mA | 1 |
| | | VDDA, PLL Bypass Mode@100MHz | | 3 | 5 | mA | 1 |
| | $I_{DD}$ | All other VDD pins | | 0.14 | 1 | mA | |
| | $I_{DDIO}$ | VDDIO for DIF outputs, if applicable | | 0.01 | 0.3 | mA | |

[1.] Includes VDDR if applicable

# Electrical Characteristics–Skew and Differential Jitter Parameters

$T_{AMB}$ = $T_{COM}$ or $T_{IND}$, unless noted., Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| CLK_IN, DIF[x:0] | $t_{SPO\_PLL}$ | Input-to-Output Skew in PLL mode @100MHz, nominal temperature and voltage | -100 | 3 | 100 | ps | 1,2,4,5,8 |
| CLK_IN, DIF[x:0] | $t_{PD\_BYP}$ | Input-to-Output Skew in Bypass mode @100MHz, nominal temperature and voltage | 2.5 | 3.6 | 4.5 | ns | 1,2,3,5,8 |
| CLK_IN, DIF[x:0] | $t_{DSPO\_PLL}$ | Input-to-Output Skew Variation in PLL mode @100MHz, across voltage and temperature | -50 | 0 | 50 | ps | 1,2,3,5,8 |
| CLK_IN, DIF[x:0] | $t_{DSPO\_BYP}$ | Input-to-Output Skew Variation in Bypass mode @100MHz, across voltage and temperature, $T_{AMB}$ = $T_{COM}$ | -250 | | 250 | ps | 1,2,3,5,8 |
| | | Input-to-Output Skew Variation in Bypass mode @100MHz, across voltage and temperature, $T_{AMB}$ = $T_{IND}$ | -350 | | 350 | ps | 1,2,3,5,8 |
| DIF[x:0] | $t_{SKEW\_ALL}$ | Output-to-Output Skew across all outputs @100MHz, $T_{AMB}$ = $T_{COM}$ | | 36 | 50 | ps | 1,2,3,8 |
| | | Output-to-Output Skew across all outputs @100MHz, $T_{AMB}$ = $T_{IND}$ | | 38 | 65 | ps | 1,2,3,8 |
| PLL Jitter Peaking | $j_{peak-hibw}$ | LOBW#_BYPASS_HIBW = 1 | 0 | 1.2 | 2.5 | dB | 7,8 |
| PLL Jitter Peaking | $j_{peak-lobw}$ | LOBW#_BYPASS_HIBW = 0 | 0 | 0.8 | 2 | dB | 7,8 |
| PLL Bandwidth | $pll_{HIBW}$ | LOBW#_BYPASS_HIBW = 1 | 2 | 3 | 4 | MHz | 8,9 |
| PLL Bandwidth | $pll_{LOBW}$ | LOBW#_BYPASS_HIBW = 0 | 0.7 | 1.1 | 1.4 | MHz | 8,9 |
| Duty Cycle | $t_{DC}$ | Measured differentially, PLL Mode | 45 | 50 | 55 | % | 1 |
| Duty Cycle Distortion | $t_{DCD}$ | Measured differentially, Bypass Mode @100MHz | -1.5 | -0.6 | 0 | % | 1,10 |
| Jitter, Cycle to cycle | $t_{jcyc-cyc}$ | PLL mode | | 25 | 50 | ps | 1,11 |
| | | *Additive* Jitter in Bypass Mode | | 1 | 5 | ps | 1,11 |

**Notes for preceding table:**

[1] Measured into fixed 2pF load cap. Input to output skew is measured at the first output edge following the corresponding input.

[2] Measured from differential cross-point to differential cross-point. This parameter can be tuned with external feedback path, if present.

[3] All Bypass Mode Input-to-Output specs refer to the timing between an input edge and the specific output edge created by it.

[4] This parameter is deterministic for a given device.

[5] Measured with scope averaging on to find mean value.

[6] t is the period of the input clock.

[7] Measured as maximum pass band gain. At frequencies within the loop BW, highest point of magnification is called PLL jitter peaking.

[8.] Guaranteed by design and characterization, not 100% tested in production.

[9] Measured at 3 db down or half power point.

[10] Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in bypass mode.

# Electrical Characteristics–Phase Jitter Parameters

$T_{AMB}$ = $T_{COM}$ or $T_{IND}$, unless noted., Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | IND.LIMIT | UNITS | Notes |
|---|---|---|---|---|---|---|---|---|
| Phase Jitter, PLL Mode | $t_{jphPCIeG1}$ | PCIe Gen 1 | | 36 | 49 | 86 | ps (p-p) | 1,2,3 |
| | $t_{jphPCIeG2}$ | PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz | | 1.2 | 1.6 | 3 | ps (rms) | 1,2 |
| | | PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz) | | 2.2 | 2.8 | 3.1 | ps (rms) | 1,2 |
| | $t_{jphPCIeG3}$ | PCIe Gen 3 (PLL BW of 2-4MHz, CDR = 10MHz) | | 0.56 | 0.63 | 1 | ps (rms) | 1,2,4 |
| | $t_{jphQPI\_SMI}$ | QPI & SMI (100MHz or 133MHz, 4.8Gb/s, 6.4Gb/s 12UI) | | 0.22 | 0.48 | 0.5 | ps (rms) | 1,4 |
| | | QPI & SMI (100MHz, 8.0Gb/s, 12UI) | | 0.15 | 0.28 | 0.3 | ps (rms) | 1,4 |
| | | QPI & SMI (100MHz, 9.6Gb/s, 12UI) | | 0.11 | 0.17 | 0.2 | ps (rms) | 1,4 |
| *Additive* Phase Jitter, Bypass mode | $t_{jphPCIeG1}$ | PCIe Gen 1 | | 0.0 | 0.8 | n/a | ps (p-p) | 1,2,3 |
| | $t_{jphPCIeG2}$ | PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz | | 0.1 | 0.2 | n/a | ps (rms) | 1,2,5 |
| | | PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz) | | 0.4 | 0.5 | n/a | ps (rms) | 1,2,5 |
| | $t_{jphPCIeG3}$ | PCIe Gen 3 (PLL BW of 2-4 or 2-5 MHz, CDR = 10MHz) | | 0.0 | 0.0 | n/a | ps (rms) | 1,2,4,5 |
| | $t_{jphQPI\_SMI}$ | QPI & SMI (100MHz or 133MHz, 4.8Gb/s, 6.4Gb/s 12UI) | | 0.11 | 0.2 | n/a | ps (rms) | 1,4,5 |
| | | QPI & SMI (100MHz, 8.0Gb/s, 12UI) | | 0.00 | 0.01 | n/a | ps (rms) | 1,4,5 |
| | | QPI & SMI (100MHz, 9.6Gb/s, 12UI) | | 0.00 | 0.01 | n/a | ps (rms) | 1,4,5 |

[1] Applies to all outputs.

[2] See http://www.pcisig.com for complete specs.

[3] Sample size of at least 100K cycles. This figure extrapolates to 108ps pk-pk at 1M cycles for a BER of $1^{-12}$.

[4] Calculated from Intel-supplied Clock Jitter Tool v1.6.3.

[5] For RMS figures, additive jitter is calculated by solving the following equation: Additive jitter = SQRT[(total jitter)^2 - (input jitter)^2]

January 28, 2021

## Clock Periods–Differential Outputs with Spread Spectrum Disabled

| SSC OFF | Center Freq. MHz | Measurement Window | | | | | | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| | | 1 Clock | 1us | 0.1s | 0.1s | 0.1s | 1us | 1 Clock | | |
| | | -c2c jitter AbsPer Min | -SSC Short-Term Average Min | - ppm Long-Term Average Min | 0 ppm Period Nominal | + ppm Long-Term Average Max | +SSC Short-Term Average Max | +c2c jitter AbsPer Max | | |
| DIF | 100.00 | 9.94900 | | 9.99900 | 10.00000 | 10.00100 | | 10.05100 | ns | 1,2,3 |
| | 133.33 | 7.44925 | | 7.49925 | 7.50000 | 7.50075 | | 7.55075 | ns | 1,2,4 |

## Clock Periods–Differential Outputs with Spread Spectrum Enabled

| SSC ON | Center Freq. MHz | Measurement Window | | | | | | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| | | 1 Clock | 1us | 0.1s | 0.1s | 0.1s | 1us | 1 Clock | | |
| | | -c2c jitter AbsPer Min | -SSC Short-Term Average Min | - ppm Long-Term Average Min | 0 ppm Period Nominal | + ppm Long-Term Average Max | +SSC Short-Term Average Max | +c2c jitter AbsPer Max | | |
| DIF | 99.75 | 9.94906 | 9.99906 | 10.02406 | 10.02506 | 10.02607 | 10.05107 | 10.10107 | ns | 1,2,3 |
| | 133.00 | 7.44930 | 7.49930 | 7.51805 | 7.51880 | 7.51955 | 7.53830 | 7.58830 | ns | 1,2,4 |

**Notes:**

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy specifications are guaranteed with the assumption that the input clock complies with CK420BQ/CK410B+ accuracy requirements (+/-100ppm). The 9ZXL1251 itself does not contribute to ppm error.

[3] Driven by SRC output of main clock, 100 MHz PLL Mode or Bypass mode

[4] Driven by CPU output of main clock, 133 MHz PLL Mode or Bypass mode

**Differential Output Terminations**

| DIF Zo (Ω) | Rs (Ω) |
|---|---|
| 100 | NA |
| 85 | 0 |
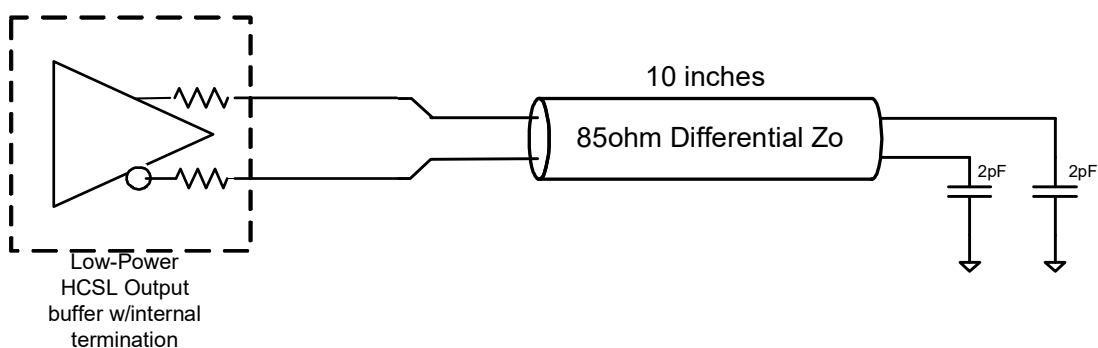
# General SMBus Serial Interface Information for 9ZXL1251

## How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- Renesas clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- Renesas clock will **acknowledge**
- Controller (host) sends the byte count = X
- Renesas clock will **acknowledge**
- Controller (host) starts sending Byte **N through Byte N+X-1**
- Renesas clock will **acknowledg**e each byte **one at a time**
- Controller (host) sends a Stop bit

## How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- Renesas clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- Renesas clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- Renesas clock will **acknowledge**
- Renesas clock will send the data byte count = X
- Renesas clock sends Byte **N+X-1**
- Renesas clock sends **Byte 0 through Byte X (if $X_{(H)}$ was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Write Operation | | | |
|---|---|---|---|
| Controller (Host) | | Renesas (Slave/Receiver) | |
| T | starT bit | | |
| Slave Address | | | |
| WR | WRite | | |
| | | ACK | |
| Beginning Byte = N | | | |
| | | ACK | |
| Data Byte Count = X | | | |
| | | ACK | |
| Beginning Byte N | | | |
| | | ACK | |
| O | | | |
| O | | | O |
| O | | | O |
| | | | O |
| Byte N + X - 1 | | | |
| | | ACK | |
| P | stoP bit | | |

(X Byte spans the Beginning Byte N through Byte N + X - 1 rows)

| Index Block Read Operation | | | |
|---|---|---|---|
| Controller (Host) | | Renesas | |
| T | starT bit | | |
| Slave Address | | | |
| WR | WRite | | |
| | | ACK | |
| Beginning Byte = N | | | |
| | | ACK | |
| RT | Repeat starT | | |
| Slave Address | | | |
| RD | ReaD | | |
| | | ACK | |
| | | Data Byte Count=X | |
| ACK | | Beginning Byte N | |
| ACK | | | O |
| O | | | O |
| O | | | O |
| O | | | |
| | | Byte N + X - 1 | |
| N | Not acknowledge | | |
| P | stoP bit | | |

(X Byte spans the Beginning Byte N through Byte N + X - 1 rows)

**SMBusTable: PLL Mode, and Frequency Select Register**

| Byte 0 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|------------------|------|---|---|---------|
| Bit 7 | 5 | PLL Mode 1 | PLL Operating Mode Rd back 1 | **R** | See PLL Operating Mode | | Latch |
| Bit 6 | 5 | PLL Mode 0 | PLL Operating Mode Rd back 0 | **R** | Readback Table | | Latch |
| Bit 5 | | | Reserved | | | | 0 |
| Bit 4 | | | Reserved | | | | 0 |
| Bit 3 | | PLL_SW_EN | Enable S/W control of PLL BW | RW | HW Latch | SMBus Control | 0 |
| Bit 2 | | PLL Mode 1 | PLL Operating Mode 1 | RW | See PLL Operating Mode | | 1 |
| Bit 1 | | PLL Mode 0 | PLL Operating Mode 1 | RW | Readback Table | | 1 |
| Bit 0 | 4 | 100M_133M# | Frequency Select Readback | **R** | 133MHz | 100MHz | Latch |

**Note:** Setting bit 3 to '1' allows the user to override the Latch value from pin 5 via use of bits 2 and 1. Use the values from the PLL Operating Mode Readback Table. Note that Bits 7 and 6 will keep the value originally latched on pin 5. A warm reset of

**SMBusTable: Output Control Register**

| Byte 1 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|------------------|------|---|---|---------|
| Bit 7 | 47/46 | DIF_7_En | Output Control - '0' overrides OE# pin | RW | | | 1 |
| Bit 6 | 43/42 | DIF_6_En | Output Control - '0' overrides OE# pin | RW | | | 1 |
| Bit 5 | 39/38 | DIF_5_En | Output Control - '0' overrides OE# pin | RW | | | 1 |
| Bit 4 | 35/34 | DIF_4_En | Output Control - '0' overrides OE# pin | RW | Low/Low | Enable | 1 |
| Bit 3 | 30/31 | DIF_3_En | Output Control - '0' overrides OE# pin | RW | | | 1 |
| Bit 2 | 26/27 | DIF_2_En | Output Control - '0' overrides OE# pin | RW | | | 1 |
| Bit 1 | 21/22 | DIF_1_En | Output Control - '0' overrides OE# pin | RW | | | 1 |
| Bit 0 | 17/18 | DIF_0_En | Output Control - '0' overrides OE# pin | RW | | | 1 |

**SMBusTable: Output Control Register**

| Byte 2 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|------------------|------|---|---|---------|
| Bit 7 | | | Reserved | | | | 0 |
| Bit 6 | | | Reserved | | | | 0 |
| Bit 5 | | | Reserved | | | | 0 |
| Bit 4 | | | Reserved | | | | 0 |
| Bit 3 | 64/63 | DIF_11_En | Output Control - '0' overrides OE# pin | RW | | | 1 |
| Bit 2 | 59/60 | DIF_10_En | Output Control - '0' overrides OE# pin | RW | Low/Low | Enable | 1 |
| Bit 1 | 54/55 | DIF_9_En | Output Control - '0' overrides OE# pin | RW | | | 1 |
| Bit 0 | 50/51 | DIF_8_En | Output Control - '0' overrides OE# pin | RW | | | 1 |

**SMBusTable: Reserved Register**

| Byte 3 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|------------------|------|---|---|---------|
| Bit 7 | | | Reserved | | | | 0 |
| Bit 6 | | | Reserved | | | | 0 |
| Bit 5 | | | Reserved | | | | 0 |
| Bit 4 | | | Reserved | | | | 0 |
| Bit 3 | | | Reserved | | | | 0 |
| Bit 2 | | | Reserved | | | | 0 |
| Bit 1 | | | Reserved | | | | 0 |
| Bit 0 | | | Reserved | | | | 0 |

**SMBusTable: Reserved Register**

| Byte 4 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|------------------|------|---|---|---------|
| Bit 7 | | | Reserved | | | | 0 |
| Bit 6 | | | Reserved | | | | 0 |
| Bit 5 | | | Reserved | | | | 0 |
| Bit 4 | | | Reserved | | | | 0 |
| Bit 3 | | | Reserved | | | | 0 |
| Bit 2 | | | Reserved | | | | 0 |
| Bit 1 | | | Reserved | | | | 0 |
| Bit 0 | | | Reserved | | | | 0 |

**SMBusTable: Vendor & Revision ID Register**

| Byte 5 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|---|
| Bit 7 | - | RID3 | REVISION ID | R | A rev = 0000 | | X |
| Bit 6 | - | RID2 | | R | | | X |
| Bit 5 | - | RID1 | | R | | | X |
| Bit 4 | - | RID0 | | R | | | X |
| Bit 3 | - | VID3 | VENDOR ID | R | - | - | 0 |
| Bit 2 | - | VID2 | | R | - | - | 0 |
| Bit 1 | - | VID1 | | R | - | - | 0 |
| Bit 0 | - | VID0 | | R | - | - | 1 |

**SMBusTable: DEVICE ID**

| Byte 6 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|---|
| Bit 7 | - | | Device ID 7 (MSB) | R | 1251 is 251 Decimal or FB Hex | | 1 |
| Bit 6 | - | | Device ID 6 | R | | | 1 |
| Bit 5 | - | | Device ID 5 | R | | | 1 |
| Bit 4 | - | | Device ID 4 | R | | | 1 |
| Bit 3 | - | | Device ID 3 | R | | | 1 |
| Bit 2 | - | | Device ID 2 | R | | | 0 |
| Bit 1 | - | | Device ID 1 | R | | | 1 |
| Bit 0 | - | | Device ID 0 | R | | | 1 |

**SMBusTable: Byte Count Register**

| Byte 7 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|---|
| Bit 7 | | | Reserved | | | | 0 |
| Bit 6 | | | Reserved | | | | 0 |
| Bit 5 | | | Reserved | | | | 0 |
| Bit 4 | - | BC4 | Writing to this register configures how many bytes will be read back. | RW | Default value is 8 hex, so 9 bytes (0 to 8) will be read back by default. | | 0 |
| Bit 3 | - | BC3 | | RW | | | 1 |
| Bit 2 | - | BC2 | | RW | | | 0 |
| Bit 1 | - | BC1 | | RW | | | 0 |
| Bit 0 | - | BC0 | | RW | | | 0 |

**SMBusTable: Reserved Register**

| Byte 8 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|---|
| Bit 7 | | | Reserved | | | | 0 |
| Bit 6 | | | Reserved | | | | 0 |
| Bit 5 | | | Reserved | | | | 0 |
| Bit 4 | | | Reserved | | | | 0 |
| Bit 3 | | | Reserved | | | | 0 |
| Bit 2 | | | Reserved | | | | 0 |
| Bit 1 | | | Reserved | | | | 0 |
| Bit 0 | | | Reserved | | | | 0 |

January 28, 2021

## Marking Diagrams

```
ICS
9ZXL1251AKL
LOT
COO YYWW
```

```
ICS
9ZXL1251AIL
LOT
COO YYWW
```

- Line 2: truncated part number
  - "I" denotes industrial temperature grade.
  - "L" denotes RoHS compliant package.
- Line 3: "LOT" denotes the lot number.
- Line 4:
  - "COO" denotes country of origin.
  - "YYWW" is the last two digits of the year and week that the part was assembled.
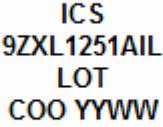
## Package Outline Drawings

The package outline drawings are appended at the end of this document. The package information is the most current data available.

## Ordering Information

| Part / Order Number | Shipping Package | Package | Temperature |
|---|---|---|---|
| 9ZXL1251AKLF | Trays | 64-pin VFQFPN | 0 to +70°C |
| 9ZXL1251AKLFT | Tape and Reel | 64-pin VFQFPN | 0 to +70°C |
| 9ZXL1251AKILF | Trays | 64-pin VFQFPN | -40 to +85°C |
| 9ZXL1251AKILFT | Tape and Reel | 64-pin VFQFPN | -40 to +85°C |

**"LF" suffix to the part number denotes Pb-Free configuration, RoHS compliant.**

**"A" is the device revision designator (will not correlate with the datasheet revision).**

## Revision History

| Revision Date | Description |
|---|---|
| July 23, 2015 | Update to final and Release |
| November 20, 2015 | 1. Updated QPI references to QPI/UPI<br>2. Updated DIF_IN table to match PCI SIG specification, no silicon change |
| January 28, 2021 | 1. Updated input frequency minimum values from 33MHz to 25MHz.<br>2. Added "25MHz PFT clock delay management" bullet to Features section on cover page.<br>3. Reformatted headers and footers to Renesas.<br>4. Updated Marking Diagram and Package Outline Drawings sections. |

# RENESAS

## 64-VFQFPN, Package Outline Drawing
9.0 x 9.0 x 0.85 mm Body, 0.5mm Pitch, Epad 6.15 x 6.15 mm
NLG64D2 Punch, PSC-4147-07, Rev 01, Page 1

PUNCH VERSION DRAWING



TOP VIEW

DETAIL A

SIDE VIEW

DETAIL B

BOTTOM VIEW
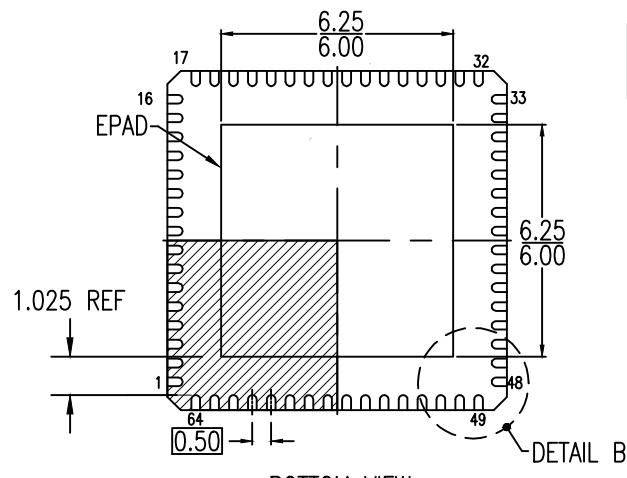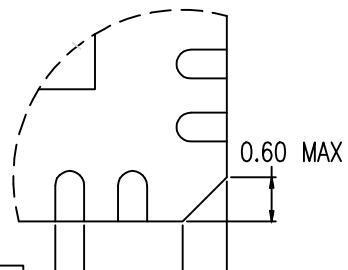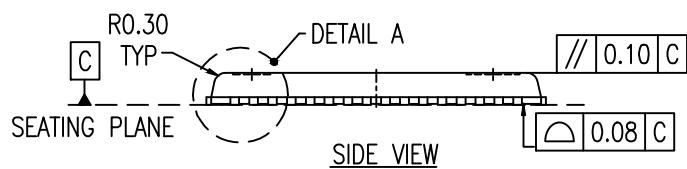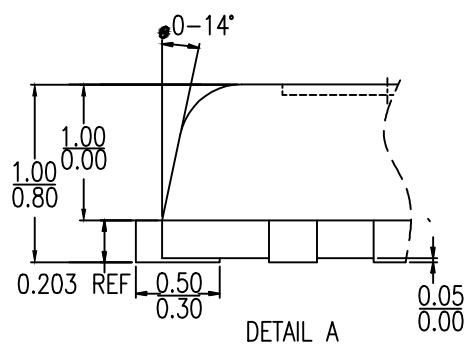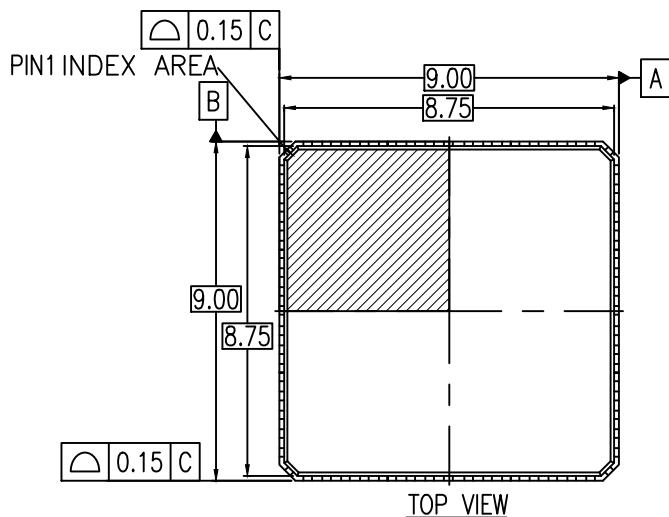
NOTES:
1. REFER TO JEDEC STD: MO0−220.
2. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15MM AND 0.30MM FROM THE TERMINAL TIP. THE TERMINAL HAS OPTIONAL RADIUS ON THE OTHER END OF THE TEMRINAL, THE DOMENSION B SHOULD NOT BE MEASURED IN THAT RADIUS AREA.

# RENESAS

## 64-VFQFPN, Package Outline Drawing
### 9.0 x 9.0 x 0.85 mm Body, 0.5mm Pitch, Epad 6.15 x 6.15 mm
### NLG64D2 Punch, PSC-4147-07, Rev 01, Page 2

INDEX AREA

9.30
8.20
0.25
0.50
0.55
0.25
9.30 8.20
6.15
0.50
0.55
6.15
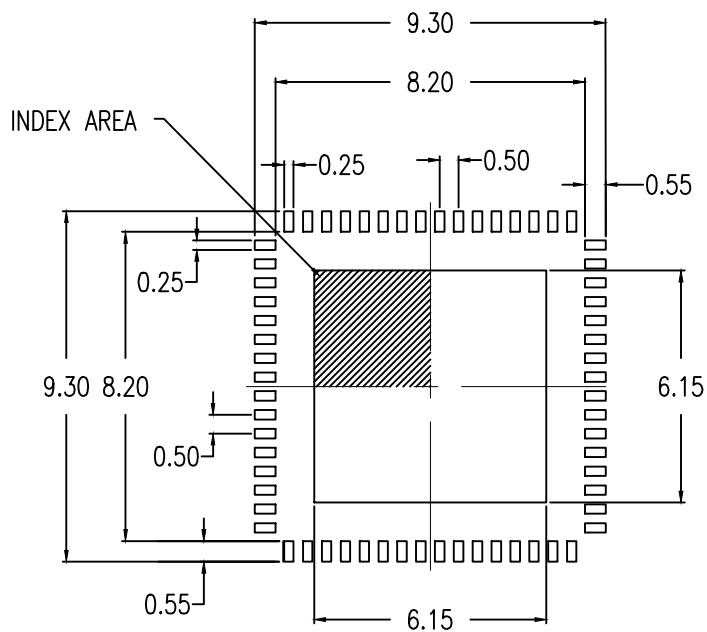
RECOMMENDED LAND PATTERN

NOTES:
1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW AS VIEWED ON PCB.
3. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
4. LAND PATTERN RECOMMENDATION PER IPC-7351 LP CALCULATOR.

| Package Revision History | | |
|---|---|---|
| Date Created | Rev No. | Description |
| Feb 20, 2018 | Rev 01 | Change QFN to VFQFPN, Added D2 |
| Nov 3, 2015 | Rev 00 | Initial Release |

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