RENESAS

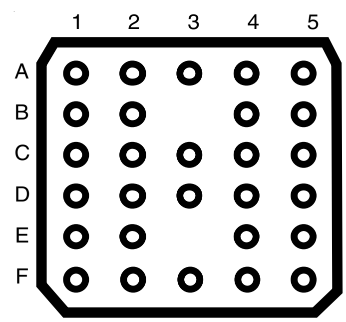
1.8V Low-Power Wide-Range Frequency Clock Driver

Recommended Application:
- DDR2 Memory Modules / Zero Delay Buffer Fan Out
- Provides complete DDR DIMM logic solution

Product Description/Features:
- Low skew, low jitter PLL clock driver
- 1 to 5 differential clock distribution (SSTL_18)
- Feedback pins for input to output synchronization
- Spread Spectrum tolerant inputs
- Auto PD when input signal is at a certain logic state

Switching Characteristics:
- Period jitter: 40ps
- Half-period jitter: 60ps
- CYCLE - CYCLE jitter 40ps
- OUTPUT - OUTPUT skew: 40ps

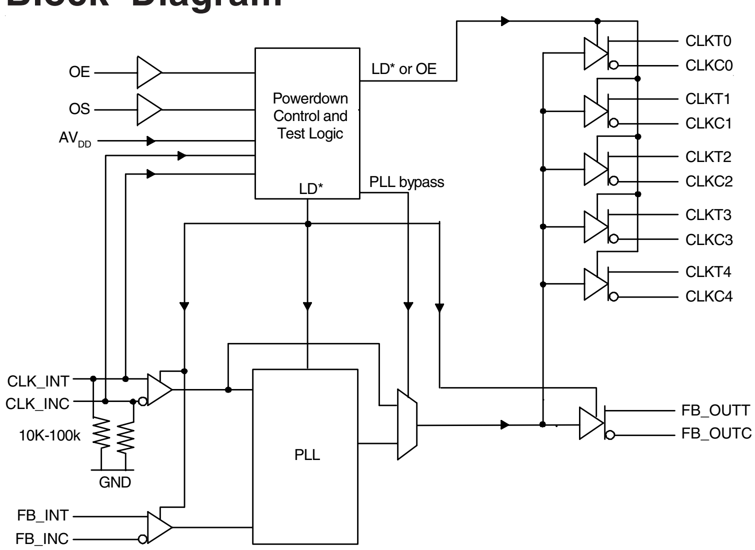
Pin Configuration



28-Ball BGA

Top View

Block Diagram



* The Logic Detect (LD) powers down the device when a logic low is applied to both CLK_INT and CLK_INC.

Ball Assignments

	1	2	3	4	5
A	CLKT0	CLKC0	CLKC1	CLKT1	FB_INT
B	CK_INT	V_{DD}	NB	V_{DD}	FB_INC
C	CK_INC	OE	V_{DD}	OS	FB_OUTC
D	AGND	GND	V_{DD}	GND	FB_OUTT
E	AVDD	GND	NB	GND	CLKT2
F	CLKC4	CLKT4	CLKC3	CLKT3	CLKC2

Pin Descriptions

Terminal Name	Description	Electrical Characteristics
AGND	Analog Ground	Ground
AV_{DD}	Analog power	1.8 V nominal
CLK_INT	Clock input with a (10K-100K Ohm) pulldown resistor	Differential input
CLK_INC	Complentary clock input with a (10K-100K Ohm) pulldown resistor	Differential input
FB_INT	Feedback clock input	Differential input
FB_INC	Complementary feedback clock input	Differential input
FB_OUTT	Feedback clock output	Differential output
FB_OUTC	Complementary feedback clock output	Differential output
OE	Output Enable (Asynchronous)	LVCMOS input
OS	Output Select (tied to GND or V_{DDQ})	LVCMOS input
GND	Ground	Ground
V_{DDQ}	Logic and output power	1.8V nominal
CLKT[0:4]	Clock outputs	Differential outputs
CLKC[0:4]	Complementary clock outputs	Differential outputs
NB	No ball	

The PLL clock buffer, **ICS97ULP845A**, is designed for a V_{DDQ} of 1.8 V, a AV_{DD} of 1.8 V and differential data input and output levels. Package options include a plastic 28-ball VFBGA.

ICS97ULP845A is a zero delay buffer that distributes a differential clock input pair (CLK_INT, CLK_INC) to five differential pair of clock outputs (CLKT[0:4], CLKC[0:4]) and one differential pair feedback clock outputs (FB_OUTT, FBOUTC). The clock outputs are controlled by the input clocks (CLK_INT, CLK_INC), the feedback clocks (FB_INT, FB_INC), the LVCMOS program pins (OE, OS) and the Analog Power input (AVDD). When OE is low, the outputs (except FB_OUTT/FB_OUTC) are disabled while the internal PLL continues to maintain its locked-in frequency. OS (Output Select) is a program pin that must be tied to GND or V_{DDQ}. When OS is high, OE will function as described above. When OS is low, OE has no effect on CLKT3/CLKC3 (they are free running in addition to FB_OUTT/FB_OUTC). When AV_{DD} is grounded, the PLL is turned off and bypassed for test purposes.

When both clock signals (CLK_INT, CLK_INC) are logic low, the device will enter a low power mode. An input logic detection circuit on the differential inputs, independent from the input buffers, will detect the logic low level and perform a low power state where all outputs, the feedback and the PLL are OFF. When the inputs transition from both being logic low to being differential signals, the PLL will be turned back on, the inputs and outputs will be enabled and the PLL will obtain phase lock between the feedback clock pair (FB_INT, FB_INC) and the input clock pair (CLK_INT, CLK_INC) within the specified stabilization time t_{STAB}.

The PLL in **ICS97ULP845A** clock driver uses the input clocks (CLK_INT, CLK_INC) and the feedback clocks (FB_INT, FB_INC) to provide high-performance, low-skew, low-jitter output differential clocks (CLKT[0:4], CLKC[0:4]). **ICS97ULP845A** is also able to track Spread Spectrum Clocking (SSC) for reduced EMI.

ICS97ULP845A is available in Commercial Temperature Range (0°C to 70°C) and Industrial Temperature Range (-40°C to +85°C). See Ordering Information for details

Function Table

Inputs					Outputs				PLL
AVDD	OE	OS	CLK_INT	CLK_INT	CLKT	CLKC	FB_OUTT	FB_OUTC	
GND	H	X	L	H	L	H	L	H	Bypassed/Off
GND	H	X	H	L	H	L	H	L	Bypassed/Off
GND	L	H	L	H	*L(Z)	*L(Z)	L	H	Bypassed/Off
GND	L	L	H	L	*L(Z), CLKT3 active	*L(Z), CLKC3 active	H	L	Bypassed/Off
1.8V(nom)	L	H	L	H	*L(Z)	*L(Z)	L	H	On
1.8V(nom)	L	L	H	L	*L(Z), CLKT3 active	*L(Z), CLKC3 active	H	L	On
1.8V(nom)	H	X	L	H	L	H	L	H	On
1.8V(nom)	H	X	H	L	H	L	H	L	On
1.8V(nom)	X	X	L	L	*L(Z)	*L(Z)	*L(Z)	*L(Z)	Off
1.8V(nom)	X	X	H	H	Reserved				

*L(Z) means the outputs are disabled to a low stated meeting the I_{ODL} limit.

Absolute Maximum Ratings

Supply Voltage (VDDQ & AVDD) . . . . -0.5V to 2.5V
Logic Inputs . . . . GND - 0.5V to V_{DDQ} + 0.5V
Ambient Operating Temperature . . . . -40°C to +85°C
Storage Temperature . . . . -65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

Commercial: TA = 0°C - 70°C; Industrial: TA = -40°C - +85°C;
Supply Voltage AVDDQ, VDDQ = 1.8 V +/- 0.1V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Current (CLK_INT, CLK_INC)	I_{IH}	V_I = V_{DDQ} or GND			±250	µA
Input Low Current (OE, OS, FB_INT, FB_INC)	I_{IL}	V_I = V_{DDQ} or GND			±10	µA
Output Disabled Low Current	I_{ODL}	OE = L, V_{ODL} = 100mV	100			µA
Operating Supply Current	$I_{DD1.8}$	C_L = 0pf @ 270MHz			TDB	mA
	I_{DDLD}	C_L = 0pf			500	µA
Input Clamp Voltage	V_{IK}	V_{DDQ} = 1.7V Iin = -18mA			-1.2	V
High-level output voltage	V_{OH}	I_{OH} = -100 A	V_{DDQ} - 0.2			V
		I_{OH} = -9 mA	1.1	1.45		V
Low-level output voltage	V_{OL}	I_{OL}=100 A		0.25	0.10	V
		I_{OL}=9 mA			0.6	V
Input Capacitance[1]	C_{IN}	V_I = GND or V_{DDQ}	2		3	pF
Output Capacitance[1]	C_{OUT}	V_{OUT} = GND or V_{DDQ}	2		3	pF

[1]Guaranteed by design, not 100% tested in production.

Recommended Operating Condition (see note1)

Commercial: TA = 0°C - 70°C; Industrial: TA = -40°C - +85°C;
Supply Voltage AVDDQ, VDDQ = 1.8 V +/- 0.1V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DDQ}, A_{VDD}		1.7	1.8	1.9	V
Low level input voltage	V_{IL}	CLK_INT, CLK_INC, FB_INC, FB_INT			0.35 x V_{DDQ}	V
		OE, OS			0.35 x V_{DDQ}	V
High level input voltage	V_{IH}	CLK_INT, CLK_INC, FB_INC, FB_INT	0.65 x V_{DDQ}			V
		OE, OS	0.65 x V_{DDQ}			V
DC input signal voltage (note 2)	V_{IN}		-0.3		V_{DDQ} + 0.3	V
Differential input signal voltage (note 3)	V_{ID}	DC - CLK_INT, CLK_INC, FB_INC, FB_INT	0.3		V_{DDQ} + 0.4	V
		AC - CLK_INT, CLK_INC, FB_INC, FB_INT	0.6		V_{DDQ} + 0.4	V
Output differential cross-voltage (note 4)	V_{OX}		V_{DDQ}/2 - 0.10		V_{DDQ}/2 + 0.10	V
Input differential cross-voltage (note 4)	V_{IX}		V_{DDQ}/2 - 0.15	V_{DD}/2	V_{DDQ}2 + 0.15	V
High level output current	I_{OH}				-9	mA
Low level output current	I_{OL}				9	mA
Operating free-air temperature	T_A		-40		85	°C

Notes:
1. Unused inputs must be held high or low to prevent them from floating.
2. DC input signal voltage specifies the allowable DC execution of differential input.
3. Differential inputs signal voltages specifies the differential voltage [VTR-VCP] required for switching, where VTR is the true input level and VCP is the complementary input level.
4. Differential cross-point voltage is expected to track variations of V_{DDQ} and is the voltage at which the differential signal must be crossing.

Timing Requirements

Commercial: TA = 0°C - 70°C; Industrial: TA = -40°C - +85°C;
Supply Voltage AVDDQ, VDDQ = 1.8 V +/- 0.1V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Max clock frequency	$freq_{op}$	1.8V±0.1V @ 25°C	95		370	MHz
Application Frequency Range	$freq_{App}$	1.8V±0.1V @ 25°C	160		350	MHz
Input clock duty cycle	d_{tin}		30		70	%
CLK stabilization	T_{STAB}			2.4	2.95	µs

Switching Characteristics[1]

Commercial: TA = 0°C - 70°C; Industrial: TA = -40°C - +85°C;
Supply Voltage AVDDQ, VDDQ = 1.8 V +/- 0.1V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Output enable time	t_{en}	OE to any output		4.73	8	ns
Output disable time	t_{dis}	OE to any output		5.82	8	ns
Period jitter	$t_{jit\ (per)}$		-30		30	ps
Half-period jitter	$t_{jit(hper)}$		-60		60	ps
Input slew rate	SLr1(i)	Input Clock	1	2.5	4	v/ns
		Output Enable (OE), (OS)	0.5			v/ns
Output clock slew rate	SLr1(o)		1.5	2.5	3	v/ns
Cycle-to-cycle period jitter	$t_{jit(cc+)}$		0		40	ps
	$t_{jit(cc-)}$		0		-40	ps
Dynamic Phase Offset	$t_{(\ )dyn}$		-20		20	ps
Static Phase Offset	t_{SPO}[2]		-50	0	50	ps
Output to Output Skew	t_{skew}				50	ps
SSC modulation frequency			30.00		33	kHz
SSC clock input frequency deviation			0.00		-0.50	%
PLL Loop bandwidth (-3 dB from unity gain)			2.0			MHz

Notes:
1. Switching characteristics guaranteed for application frequency range.
2. Static phase offset shifted by design.

Parameter Measurement Information

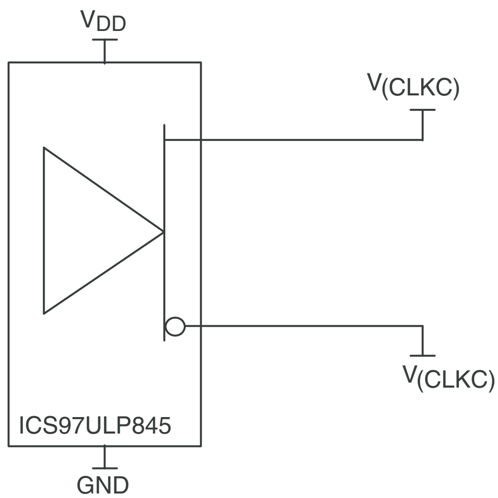


Figure 1. IBIS Model Output Load

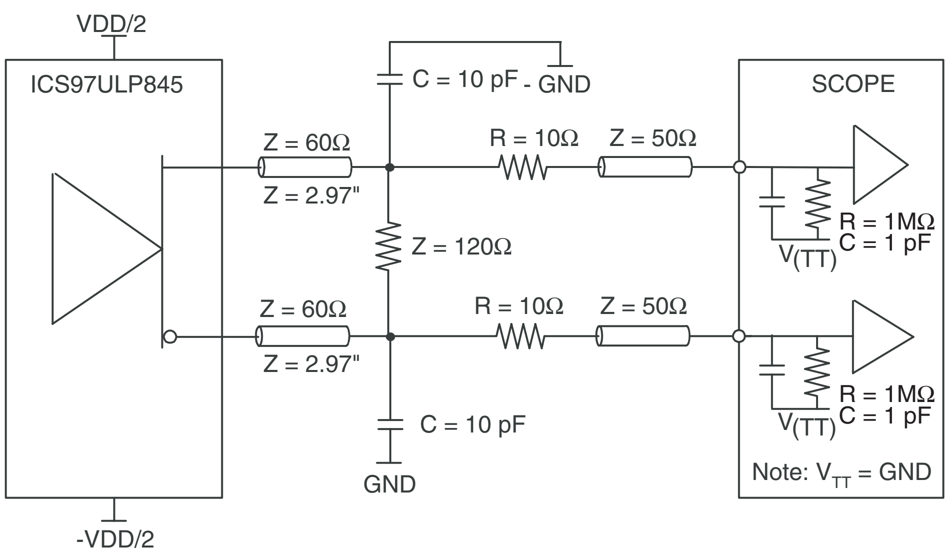
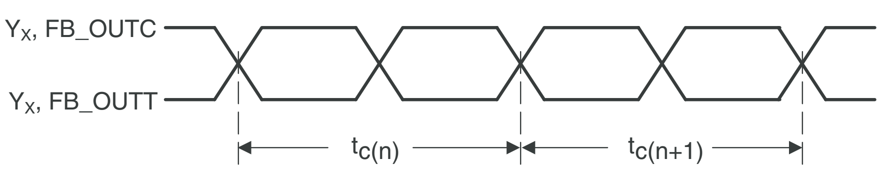


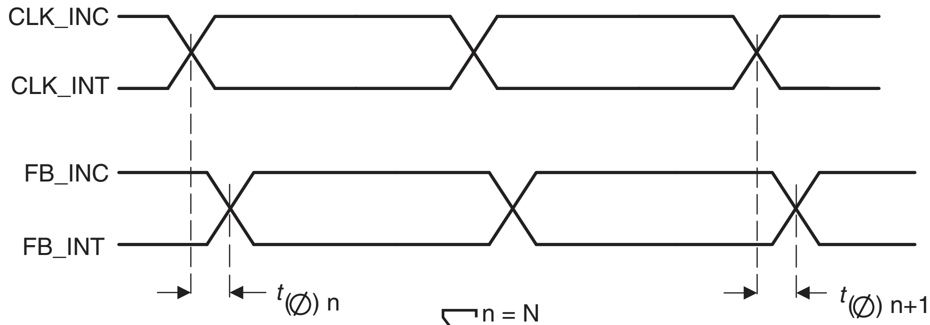
Figure 2. Output Load Test Circuit



$$t_{jit(cc)} = t_{c(n)} \pm t_{c(n+1)}$$

Figure 3. Cycle-to-Cycle Jitter

Parameter Measurement Information



$$t_{(\varnothing)} = \frac{\sum_{1}^{n=N} t_{(\varnothing)\,n}}{N}$$

(N is a large number of samples)

Figure 4. Static Phase Offset

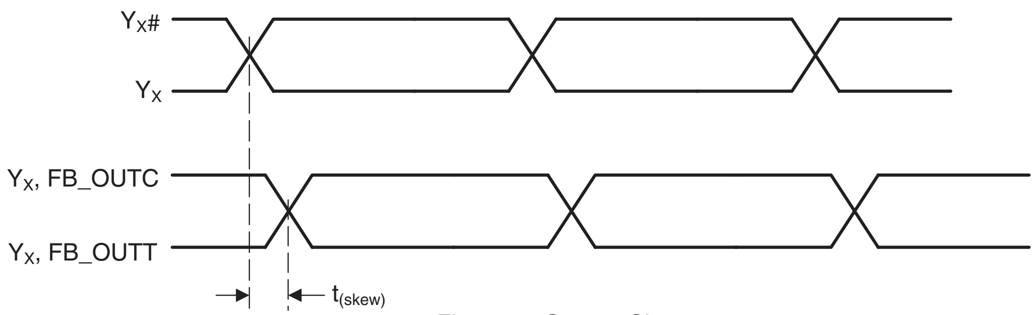
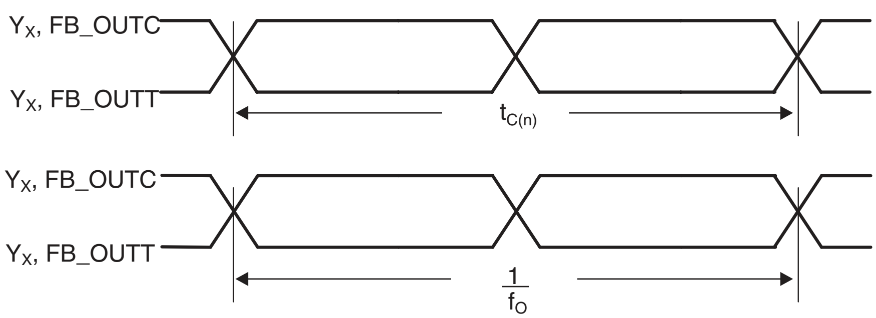


Figure 5. Output Skew



$$t_{(jit\_per)} = t_{c(n)} - \frac{1}{f_O}$$

Figure 6. Period Jitter

Parameter Measurement Information

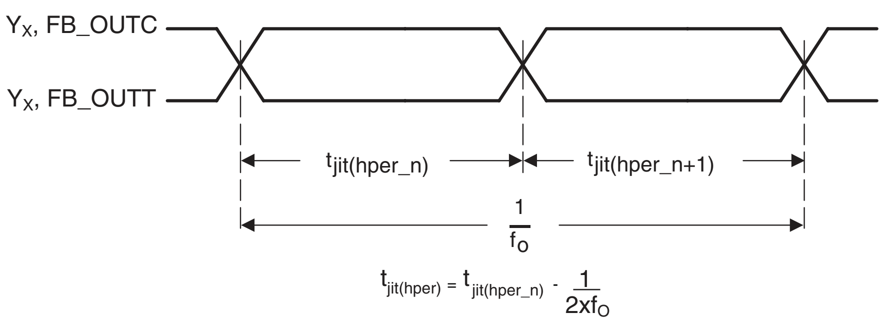


Figure 7. Half-Period Jitter

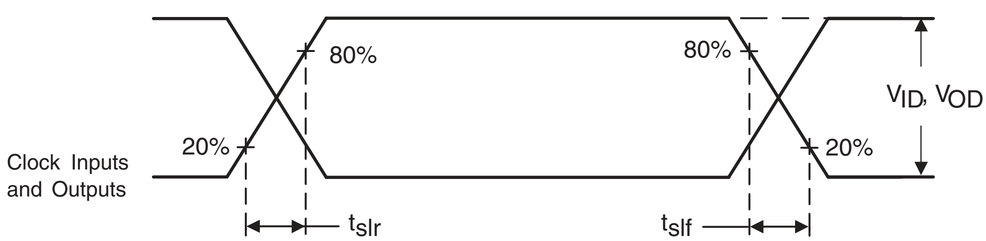


Figure 8. Input and Output Slew Rates

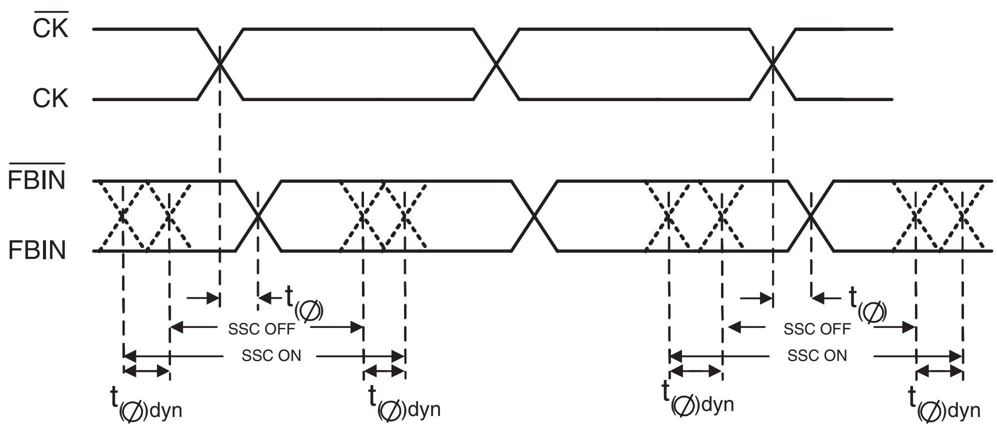


Figure 9. Dynamic Phase Offset

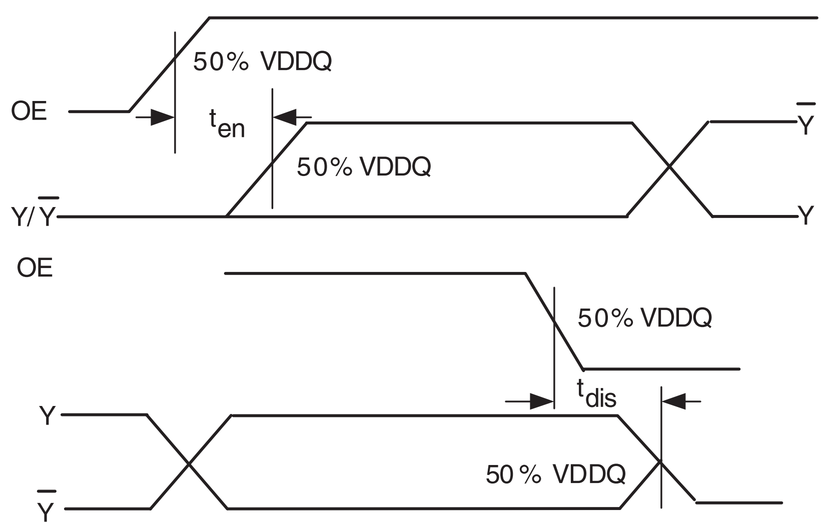


Figure 10. Time delay between OE and Clock Output (Y, $\overline{Y}$)

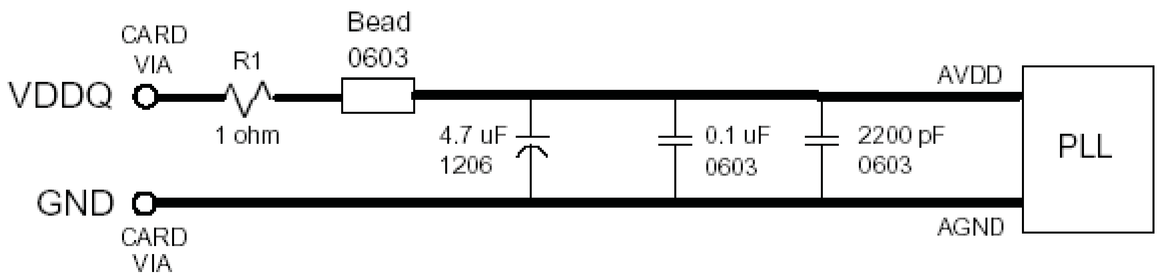
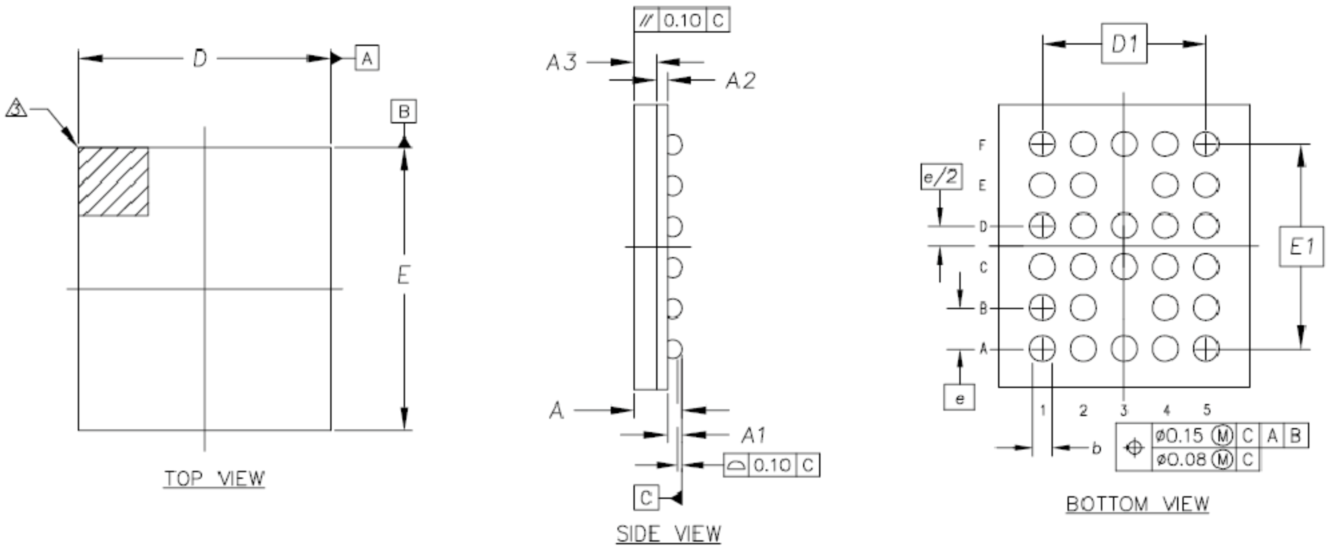


Figure 11. AV_{DD} Filtering

- Place the 2200pF capacitor close to the PLL.
- Use a wide trace for the PLL analog power & ground. Connect PLL & caps to AGND trace & connect trace to one GND via (farthest from PLL).
- Recommended bead: Fair-Rite P/N 2506036017Y0 or equivalent (0.8 Ohm DC max, 600 Ohms @ 100 MHz).



SYMBOL	Millimeter			Inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.90	1.00	0.031	0.035	0.039
A1	0.165	0.20	0.235	0.006	0.008	0.009
A2	0.16	0.20	0.24	0.006	0.008	0.009
A3	0.475	0.50	0.525	0.019	0.020	0.021
b	0.35	0.40	0.45	0.014	0.016	0.018
D	3.90	4.00	4.10	0.154	0.157	0.161
D1	2.60 BSC			0.102 BSC		
E	4.40	4.50	4.60	0.173	0.177	0.181
E1	3.25 BSC			0.128 BSC		
e	0.65 BSC			0.026 BSC		

Ordering Information

ICS97ULP845AH(LF)-T

Example:

ICS XXXX y **K** z **LF- T**

Designation for tape and reel packaging

Lead Free, RoHS Compliant (Optional)

Temperature Grade
Blank = 0°C to +70°C (Commercial)
I = -40°C to +85°C (Industrial)

Package Type
H = BGA

Revision Designator (will not correlate with datasheet revision)

Device Type

Prefix
ICS = Standard Device

1109D—06/19/07

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