General Description

The 8S89202 is a high speed 1-to-8 Differential-to-LVPECL Clock Divider and is part of the high performance clock solutions from IDT. The 8S89202 is optimized for high speed and very low output skew, making it suitable for use in demanding applications such as SONET, 1 Gigabit and 10 Gigabit Ethernet, and Fibre Channel. The internally terminated differential inputs and V_{REF_AC} pins allow other differential signal families such as LVPECL, LVDS and CML to be easily interfaced to the input with minimal use of external components.

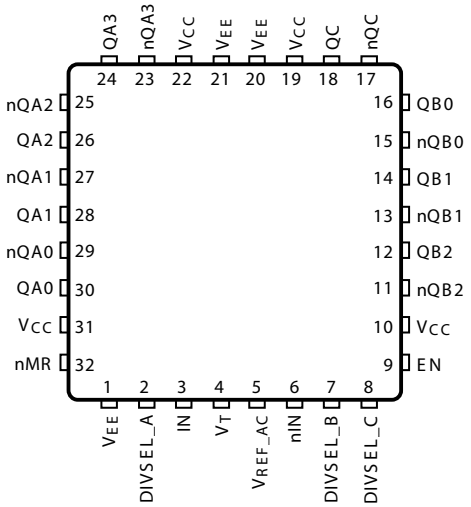
The device also has a selectable ÷1, ÷2, ÷4 output divider, which can allow the part to support multiple output frequencies from the same reference clock.

The 8S89202 is packaged in a small 5mm x 5mm 32-pin VFQFN package which makes it ideal for use in space-constrained applications.

Features

- Three output banks, consisting of eight LVPECL output pairs total
- INx, nINx inputs can accept the following differential input levels: LVPECL, LVDS, CML
- Selectable output divider values of ÷1, ÷2 and ÷4
- Maximum output frequency: 1.5GHz
- Maximum input frequency: 3GHz
- Bank skew: 6ps (typical)
- Part-to-part skew: 250ps (maximum)
- Additive phase jitter, RMS: 0.166ps (typical)
- Propagation delay: 854ps (typical)
- Output rise time: 156ps (typical)
- Full 2.5V±5% and 3.3V±10% operating supply voltage
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Pin Assignment



8S89202

32-Lead VFQFN
5mm x 5mm x 0.925mm package body
K Package
Top View

Block Diagram

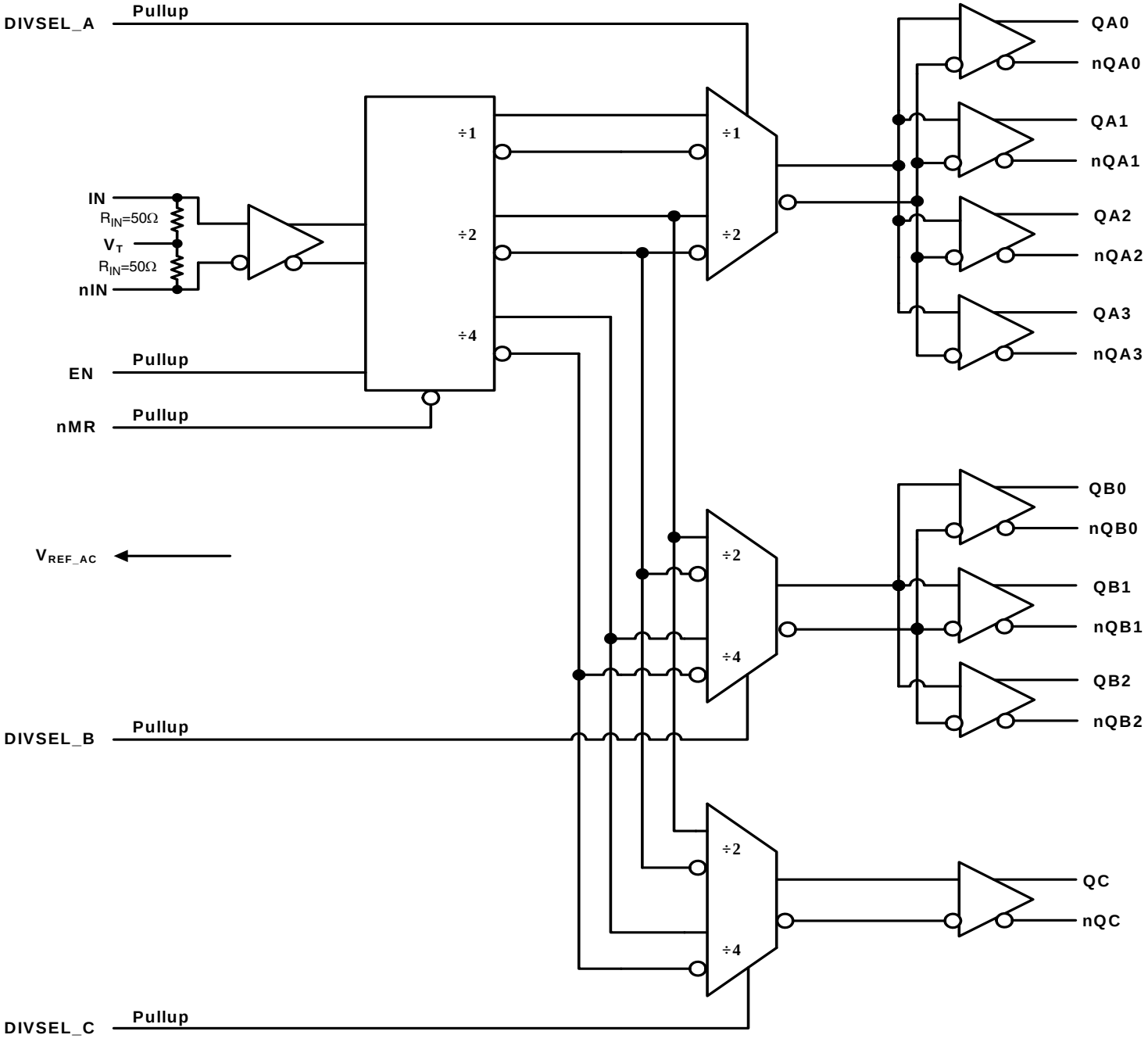


Table 1. Pin Descriptions

Number	Name	Type		Description
1, 20, 21	V_{EE}	Power		Negative supply pins.
2	DIVSEL_A	Input	Pullup	Output divider select pin. Controls output divider settings for Bank A. See Table 3 for additional information. LVCMOS/LVTTL interface levels.
3	IN	Input		Non-inverting differential LVPECL clock input. R_{IN} = 50Ω termination to $V_{T.}$
4	V_T	Input		Termination center-tap input.
5	V_{REF_AC}	Output		Reference voltage for AC-coupled applications.
6	nIN	Input		Inverting differential LVPECL clock input. R_{IN} = 50Ω termination to $V_{T.}$
7	DIVSEL_B	Input	Pullup	Output divider select pin. Controls output divider settings for Bank B. See Table 3 for additional information. LVCMOS/LVTTL interface levels.
8	DIVSEL_C	Input	Pullup	Output divider select pin. Controls output divider settings for Bank C. See Table 3 for additional information. LVCMOS/LVTTL interface levels.
9	EN	Input	Pullup	Output enable pin. See Table 3 for additional information. LVCMOS/LVTTL interface levels.
10, 19, 22, 31	V_{CC}	Power		Positive supply pins.
11, 12	nQB2, QB2	Output		Differential output pair. LVPECL interface levels.
13, 14	nQB1, QB1	Output		Differential output pair. LVPECL interface levels.
15, 16	nQB0, QB0	Output		Differential output pair. LVPECL interface levels.
17, 18	nQC, QC	Output		Differential output pair. LVPECL interface levels.
23, 24	nQA3, QA3	Output		Differential output pair. LVPECL interface levels.
25, 26	nQA2, QA2	Output		Differential output pair. LVPECL interface levels.
27, 28	nQA1, QA1	Output		Differential output pair. LVPECL interface levels.
29, 30	nQA0, QA0	Output		Differential output pair. LVPECL interface levels.
32	nMR	Input	Pullup	Master Reset. See additional 3 for additional information. LVCMOS/LVTTL interface levels.

NOTE: *Pullup* refers to internal input resistor. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			2		pF
R_{PULLUP}	Input Pullup Resistor			25		kΩ

Function Tables

Table 3. SEL Function Table

nMR	EN	DIVSEL_A	DIVSEL_B	DIVSEL_C	Output Bank A	Output Bank B	Output Bank C
0	n/a	n/a	n/a	n/a	0	0	0
1	0	n/a	n/a	n/a	0	0	0
1	1	0	0	0	÷1	÷2	÷2
1	1	1	1	1	÷2	÷4	÷4

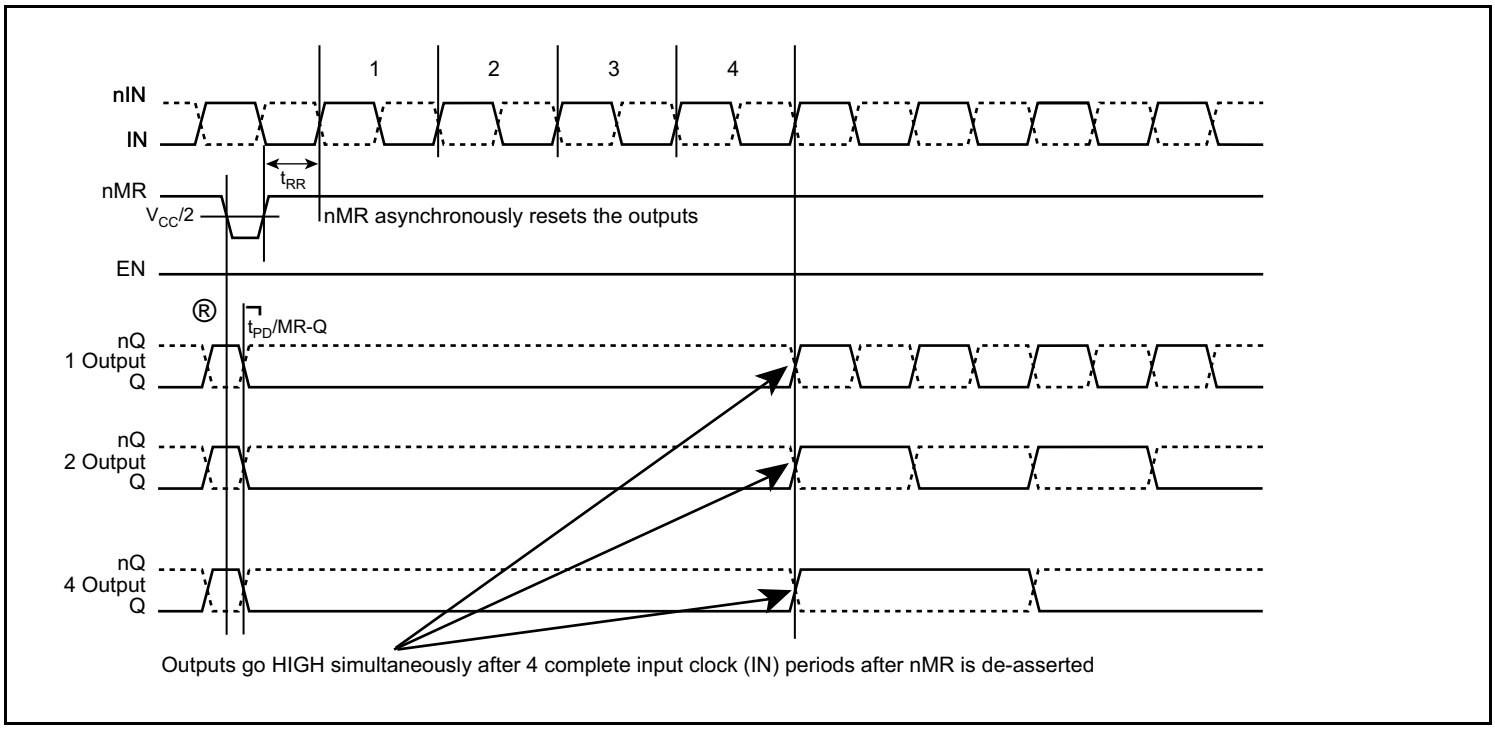
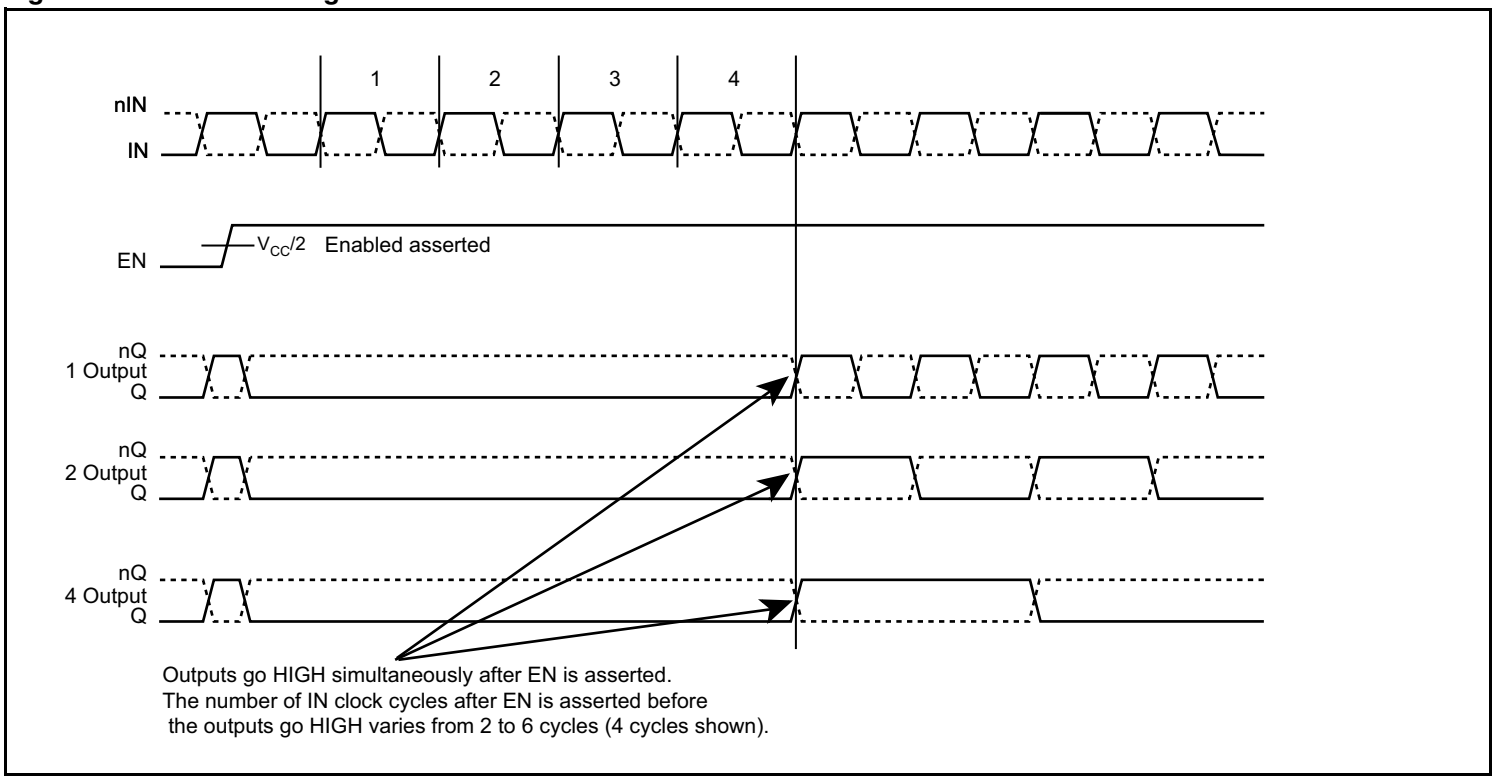


Figure 1A. Reset with Output Enabled

Figure 1B. Enabled Timing



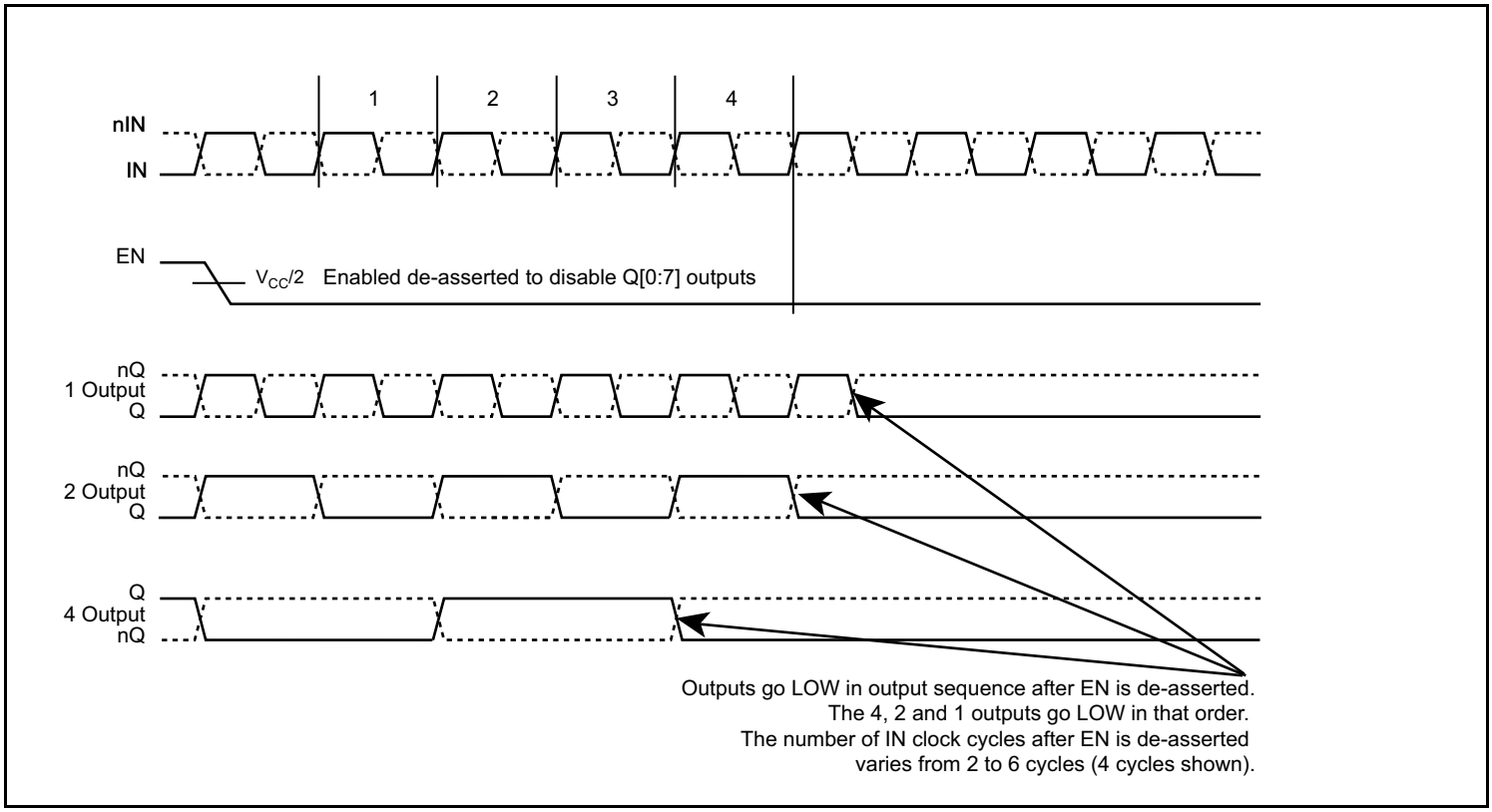


Figure 1C. Disabled Timing

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O Continuous Current Surge Current	 50mA 100mA
Input Current, IN, nIN	±50mA
V_T Current, I_{VT}	±100mA
Input Sink/Source, I_{REF_AC}	±2mA
Package Thermal Impedance, θ_{JA}	42.7°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{CC} = 2.5V ±5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		2.375	2.5	2.625	V
I_{EE}	Power Supply Current			117	131	mA

Table 4B. Power Supply DC Characteristics, V_{CC} = 3.3V ±10%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		2.97	3.3	3.63	V
I_{EE}	Power Supply Current			125	139	mA

Table 4C. LVCMOS/LVTTL DC Characteristics, V_{CC} = 3.3V ±10% or 2.5V ±5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	V_{CC} = 3.3V	2.2		V_{CC} + 0.3	V
		V_{CC} = 2.5V	1.7		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	V_{CC} = 3.3V	-0.3		0.8	V
		V_{CC} = 2.5V	-0.3		0.7	V
I_{IH}	Input High Current	V_{CC} = V_{IN} = 3.63V or 2.625V	-125		20	µA
I_{IL}	Input Low Current	V_{CC} = 3.63V or 2.625V, V_{IN} = 0V			-300	uA

Table 4D. Differential DC Characteristics, V_{CC} = 3.3V ± 10% or 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
R_{IN}	Input Resistance	IN, nIN	IN to VT, nIN to VT		50		Ω
V_{IH}	Input High Voltage	IN, nIN		0.15		V_{CC} +0.3	V
V_{IL}	Input Low Voltage	IN, nIN		0		V_{CC} -0.15	V
V_{IN}	Input Voltage Swing			0.15		V_{CC}	V
V_{DIFF_IN}	Differential Input Voltage Swing			0.3			V
V_{REF_AC}	Bias Voltage			V_{CC} -1.7	V_{CC} -1.3	V_{CC} -0.9	V

Table 4E. LVPECL DC Characteristics, V_{CC} = 3.3V ± 10%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} -1.65	V_{CC} -1.0	V_{CC} -0.5	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} -2.25	V_{CC} -1.8	V_{CC} -1.6	V
V_{OUT}	Output Voltage Swing		0.7	0.8	1.1	V
V_{DIFF_OUT}	Differential Output Voltage Swing		1.4	1.6	2.2	V

NOTE 1: Outputs terminated with 50Ω to V_{CC} – 2V.

Table 4F. LVPECL DC Characteristics, V_{CC} = 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} -1.35	V_{CC} -1.0	V_{CC} -0.70	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} -2.00	V_{CC} -1.75	V_{CC} -1.50	V
V_{OUT}	Output Voltage Swing		0.6	0.8	1.0	V
V_{DIFF_OUT}	Differential Output Voltage Swing		1.2	1.6	2.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CC} – 2V.

AC Electrical Characteristics

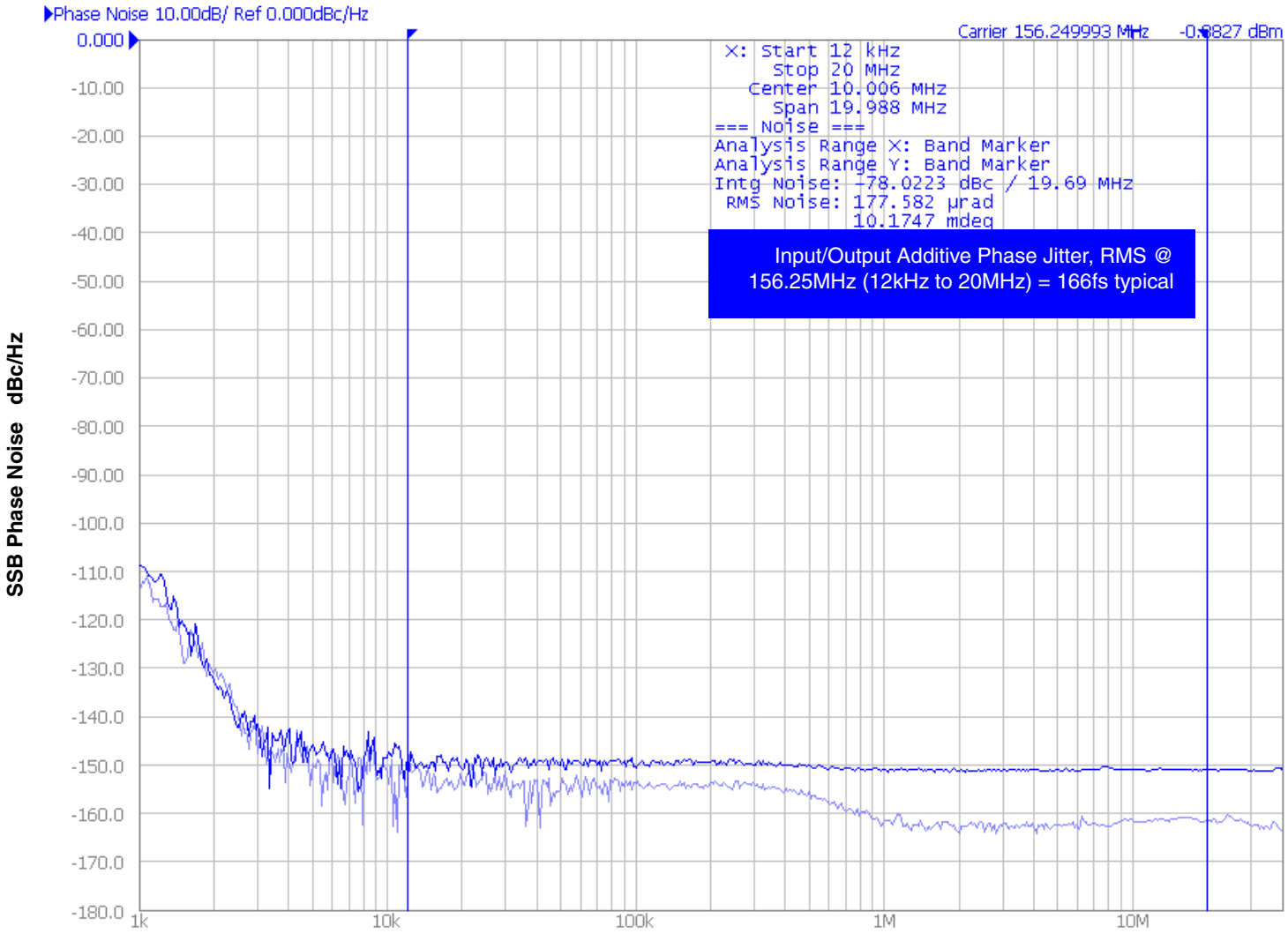
Table 5. AC Characteristics, V_{CC} = 3.3V ± 10% or 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency				1.5	GHz
f_{IN}	Input Frequency				3	GHz
t_{PD}	Propagation Delay; NOTE 1	IN to Qx	660	845	1020	ps
		nMR to Qx	600	772	905	ps
tsk(b)	Bank to Bank Skew; NOTE 2, 3	Same divide setting		6	26	ps
tsk(w)	Bank to Bank Skew; NOTE 2, 3	Different divide setting		27	103	ps
tsk(o)	Within-Bank Skew; NOTE 2, 4	Within same fanout bank		3	13	ps
tsk(pp)	Part-to-Part Skew; NOTE 2, 5				250	ps
t_{jit}	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section	156.25MHz, Integration Range: 12kHz to 20MHz		0.166	0.193	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	73	156	218	ps

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 4: Defined as skew within a bank of outputs at the same voltage and with equal load conditions.
NOTE 5: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

Additive Phase Jitter

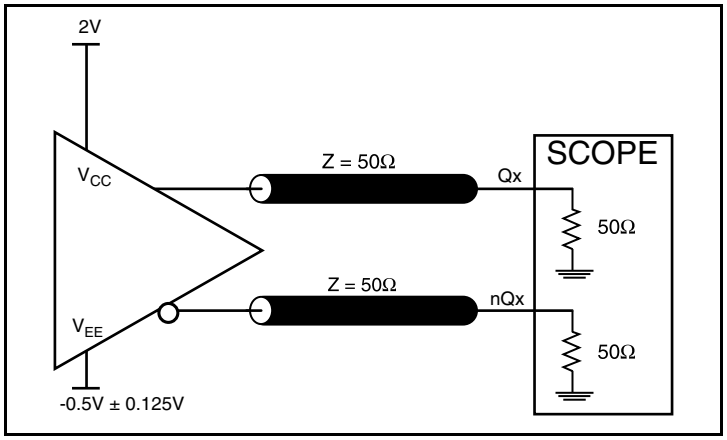
The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



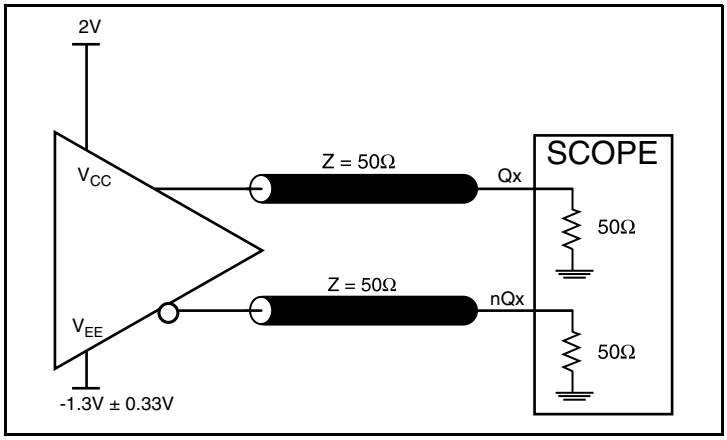
As with most timing specifications, phase noise measurements have issues relating to the limitations of the measurement equipment. The noise floor of the equipment can be higher or lower than the noise floor of the device. Additive phase noise is dependent on both the noise floor of the input source and measurement equipment.

The additive phase jitter for this device was measured using a Rohde & Schwarz SMA100 input source and an Agilent E5052 Phase noise analyzer.

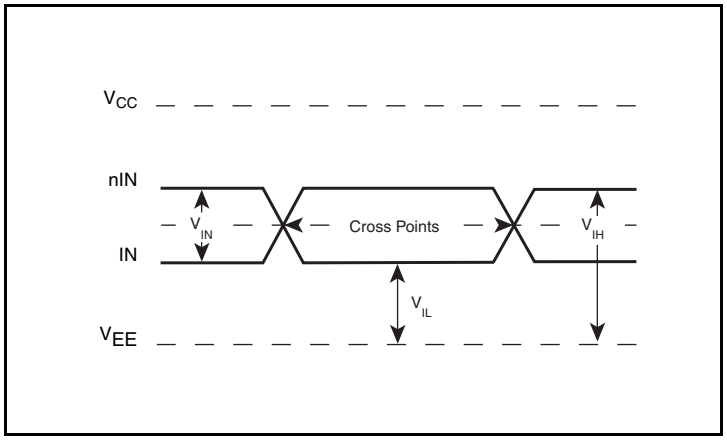
Parameter Measurement Information



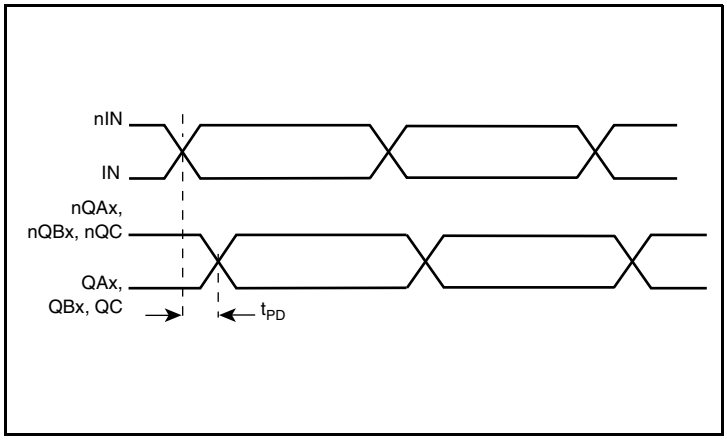
2.5V Output Load AC Test Circuit



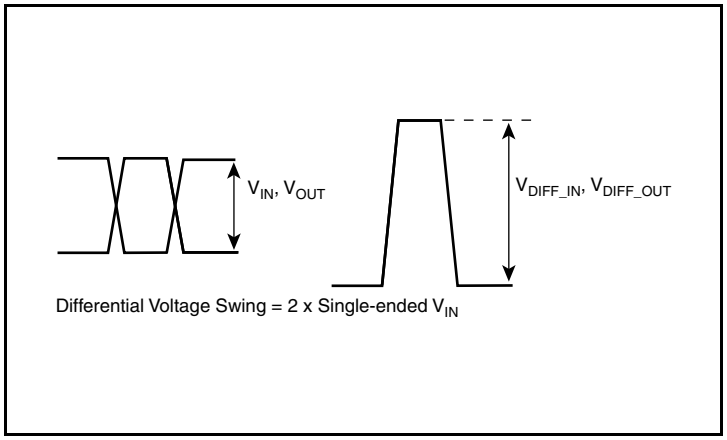
3.3V Output Load AC Test Circuit



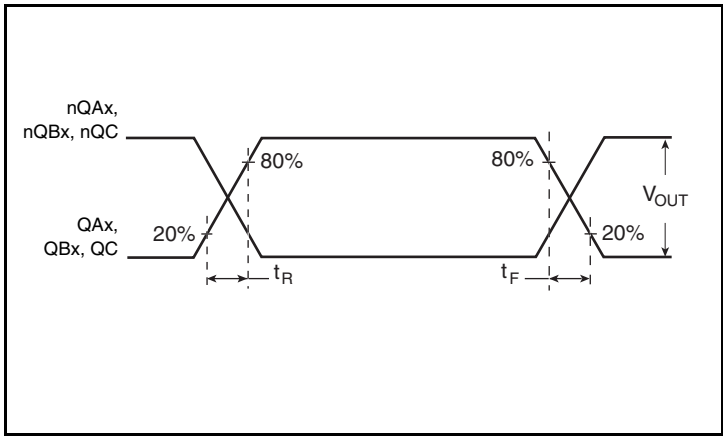
Input Levels



Propagation Delay

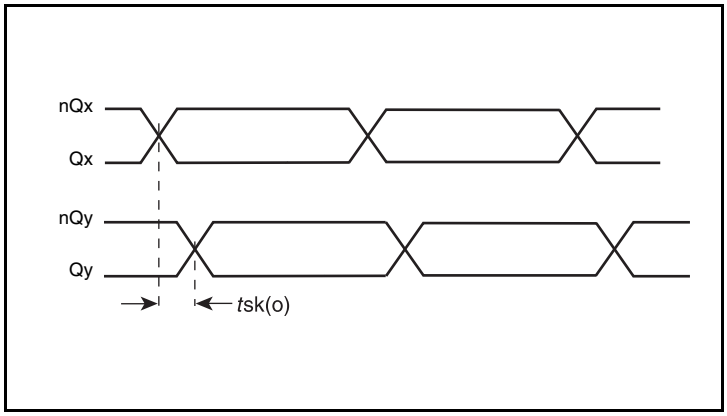


Single-Ended & Differential Input Swing

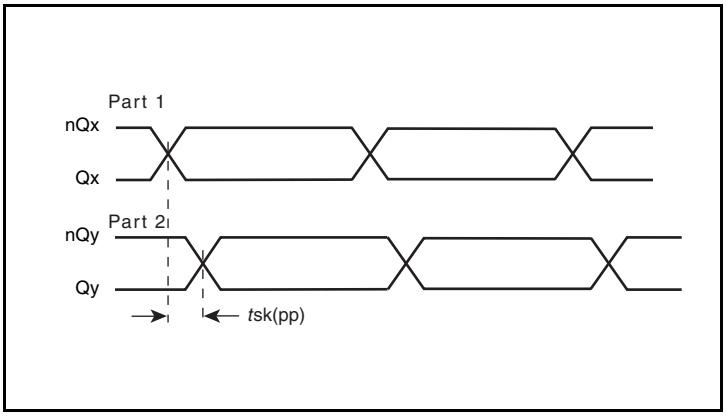


Output Rise/Fall Time

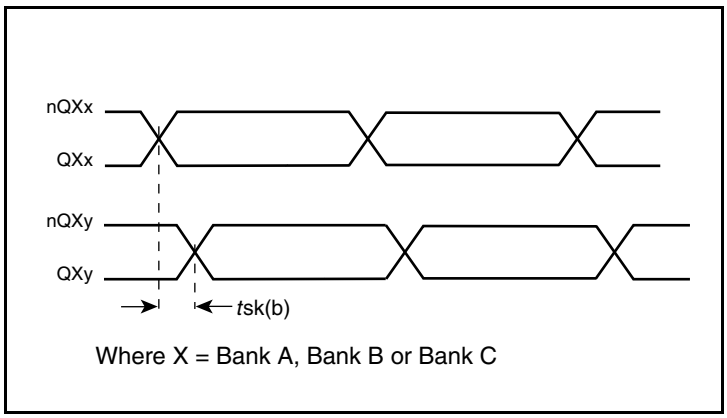
Parameter Measurement Information, continued



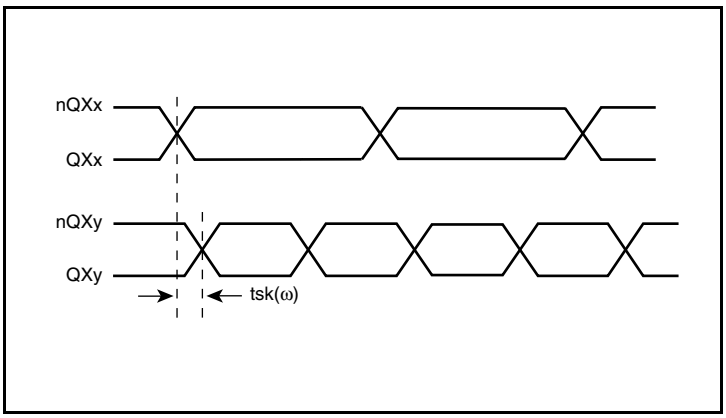
Within Bank Skew



Part-to-Part Skew



Bank to Bank Skew (same divide setting)



Bank to Bank (different divide settings)

Applications Information

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Select Pins

All control pins have internal pullups; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

2.5V LVPECL Input with Built-In 50Ω Termination Interface

The IN /nIN with built-in 50Ω terminations accept LVDS, LVPECL, CML and other differential signals. Both V_{OH} and V_{OL} must meet the V_{IN} and V_{IH} input requirements. *Figures 2A to 2D* show interface examples for the IN/nIN with built-in 50Ω termination input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

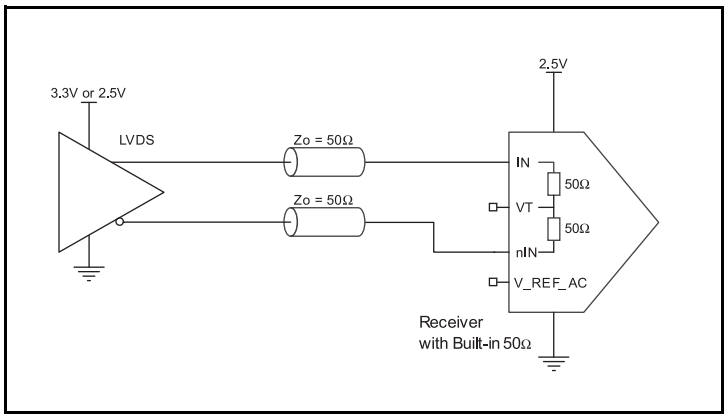


Figure 2A. IN/nIN Input with Built-In 50Ω Driven by an LVDS Driver

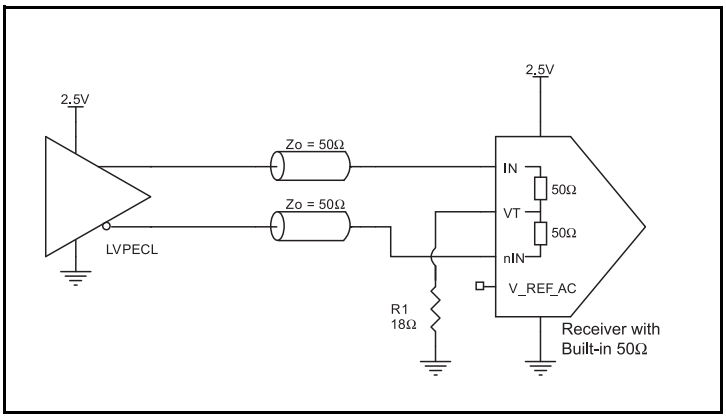


Figure 2B. IN/nIN Input with Built-In 50Ω Driven by an LVPECL Driver

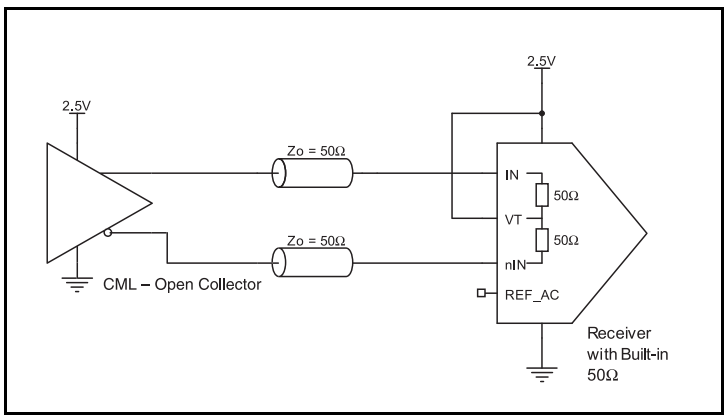


Figure 2C. IN/nIN Input with Built-In 50Ω Driven by a CML Driver

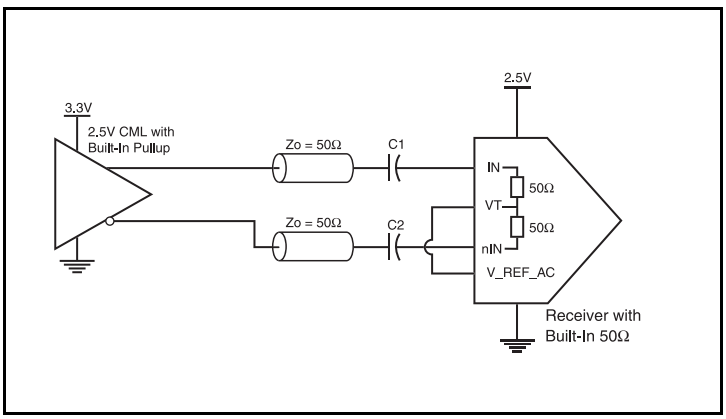


Figure 2D. IN/nIN Input with Built-In 50Ω Driven by a CML Driver with Built-In 50Ω Pullup

3.3V LVPECL Input with Built-In 50Ω Termination Interface

The IN /nIN with built-in 50Ω terminations accept LVDS, LVPECL, CML and other differential signals. Both V_{OH} and V_{OL} must meet the V_{IN} and V_{IH} input requirements. *Figures 3A to 3D* show interface examples for the IN /nIN input with built-in 50Ω terminations driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

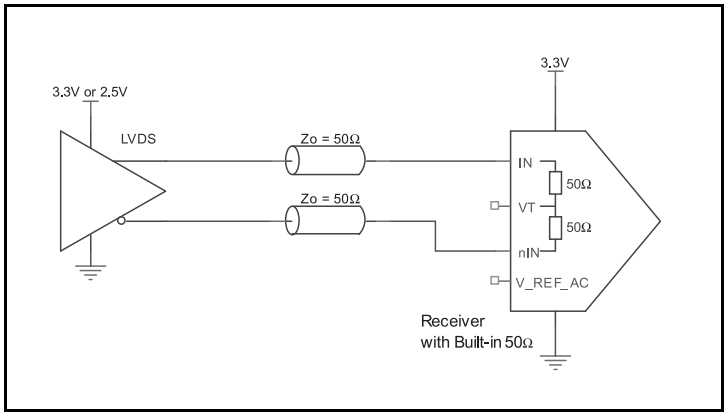


Figure 3A. IN/nIN Input with Built-In 50Ω Driven by an LVDS Driver

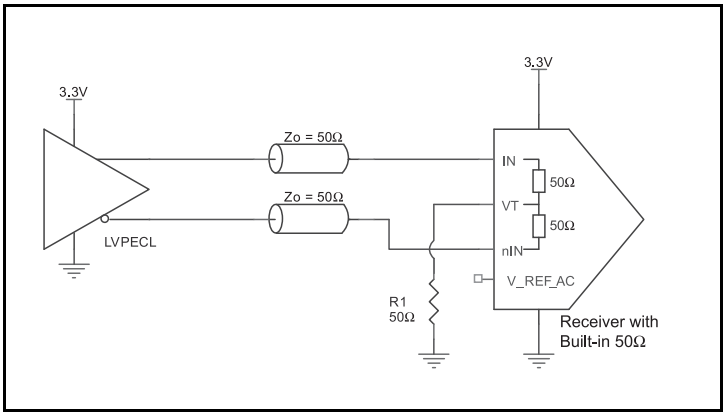


Figure 3B. IN/nIN Input with Built-In 50Ω Driven by an LVPECL Driver

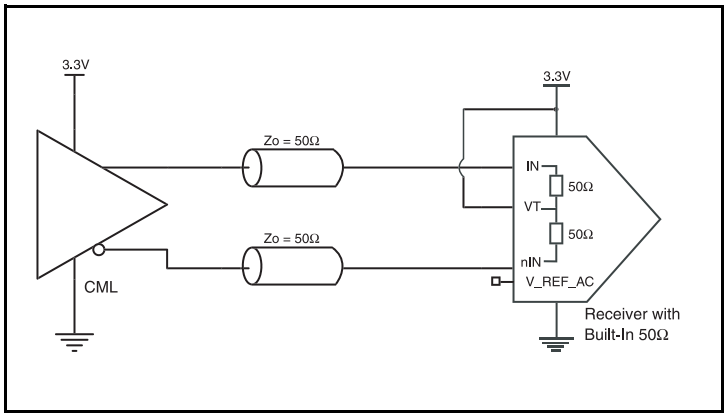


Figure 3C. IN/nIN Input with Built-In 50Ω Driven by a CML Driver with Open Collector

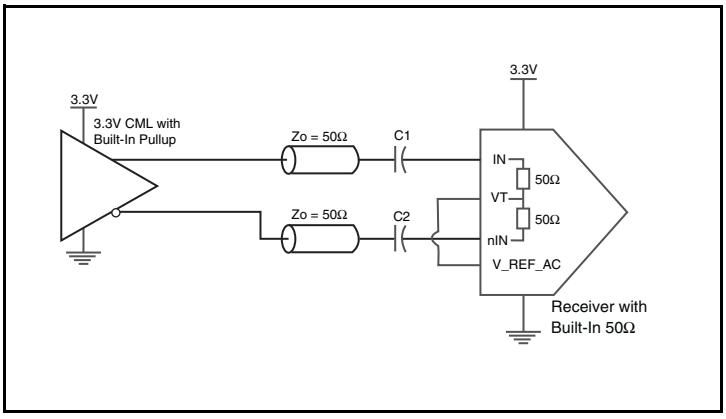


Figure 3D. IN/nIN Input with Built-In 50Ω Driven by a CML Driver with Built-In 50Ω Pullup

Termination for 2.5V LVPECL Outputs

Figure 4A and *Figure 4B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} – 2V. For V_{CC} = 2.5V, the V_{CC} – 2V is very close to ground level. The R3 in Figure 4B can be eliminated and the termination is shown in *Figure 4C.*

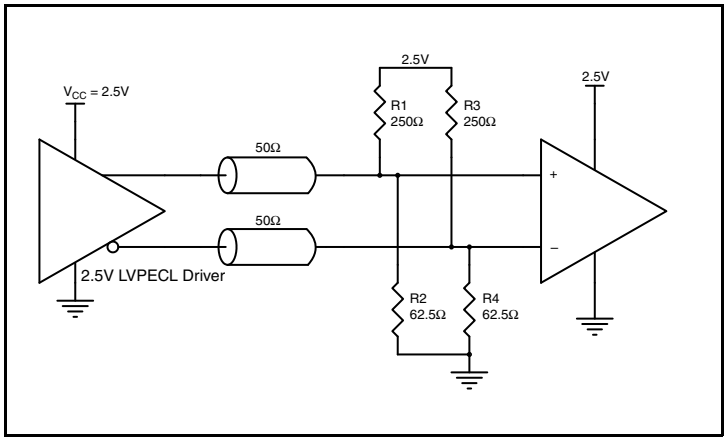


Figure 4A. 2.5V LVPECL Driver Termination Example

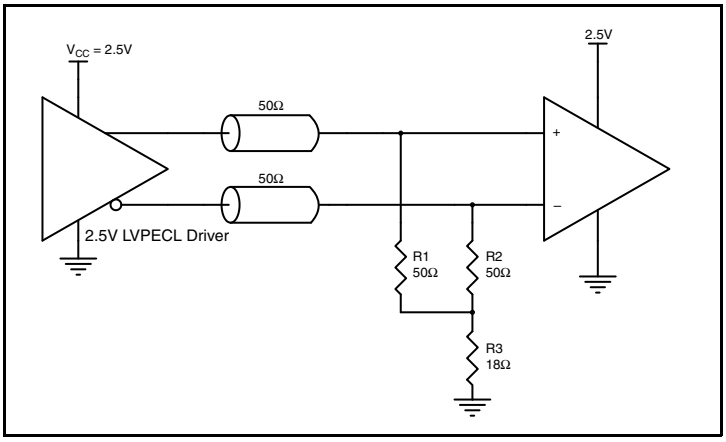


Figure 4B. 2.5V LVPECL Driver Termination Example

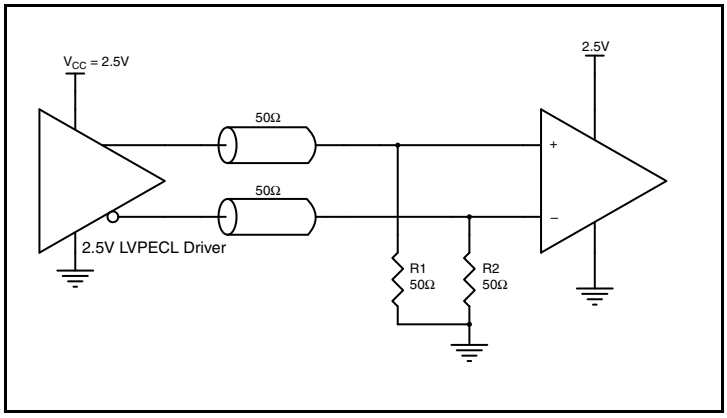


Figure 4C. 2.5V LVPECL Driver Termination Example

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential output is a low impedance follower output that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 5A and 5B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

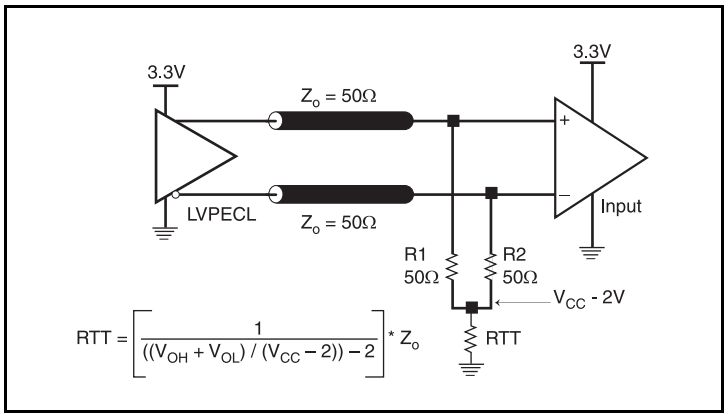


Figure 5A. 3.3V LVPECL Output Termination

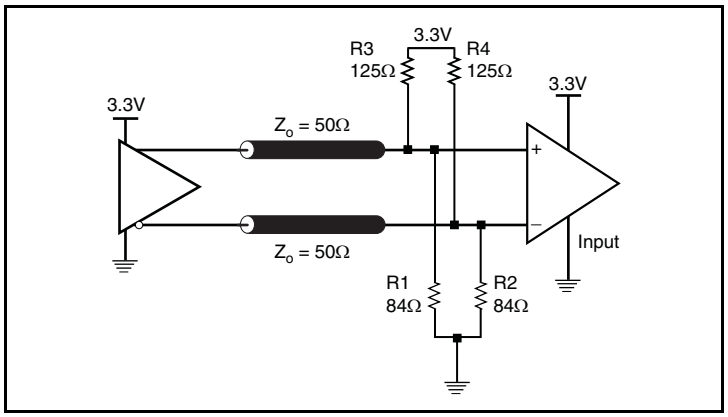


Figure 5B. 3.3V LVPECL Output Termination

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 6.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

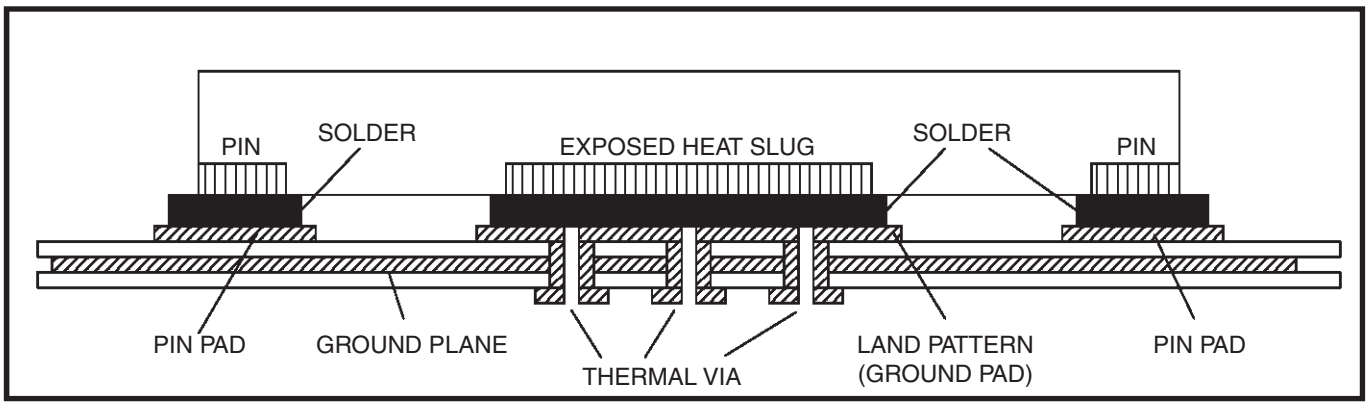


Figure 6. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Power Considerations

This section provides information on power dissipation and junction temperature for the 8S89202.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 8S89202 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.63V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

The maximum current at 85°C is as follows:
I_{EE_MAX} = 128mA

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.63V * 139mA = **504.57mW**
- Power $(outputs)_{MAX}$ = **27.8mW/Loaded Output pair**
  If all outputs are loaded, the total power is 8 * 27.8mW = **222.4mW**
- Power Dissipation for internal termination R_T
  Power $(R_T)_{MAX} = (V_{IN\_MAX})^2 / R_{T\_MIN}$ = $(1.1V)^2$ / 80Ω = **15.12mW**

Total Power$_{\_MAX}$ = (3.63V, with all outputs switching) = 504.57mW + 222.4mW + 15.12mW = **742.09mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 42.7°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.742W * 42.7°C/W = 116.7°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on input swing, the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 32 Lead VFQFN, Forced Convection

θ_{JA} **vs. Air Flow**			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	42.7°C/W	37.3°C/W	33.5°C/W

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pairs.

LVPECL output driver circuit and termination are shown in *Figure 7.*

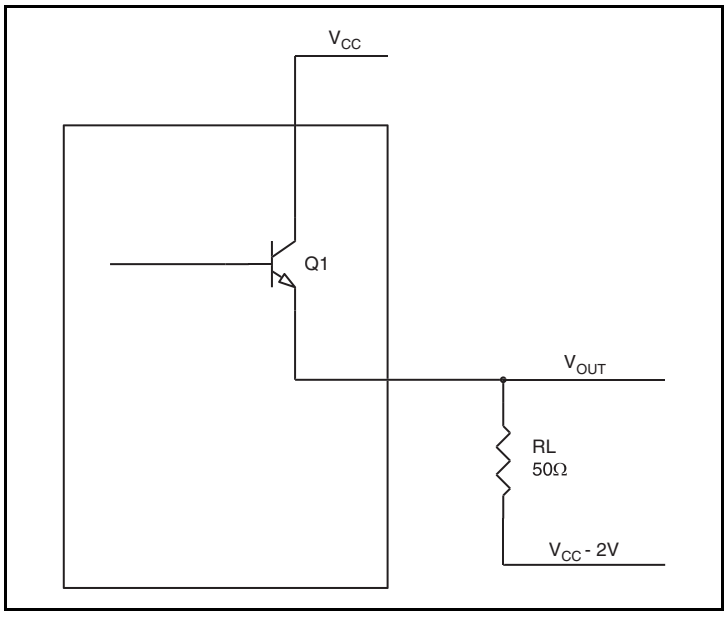


Figure 7. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} - 0.5V}$
  $(V_{CC\_MAX} - V_{OH\_MAX}) = \mathbf{0.5V}$
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} - 1.6V}$
  $(V_{CC\_MAX} - V_{OL\_MAX}) = \mathbf{1.6V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) =$
$[(2V – 0.5V)/50\Omega] * 0.5V =$ **15mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OL\_MAX}))/R_L] * (V_{CO\_MAX} – V_{OL\_MAX}) =$
$[(2V – 1.6V)/50\Omega] * 1.6V =$ **12.8mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **27.8mW**

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 32 Lead VFQFN

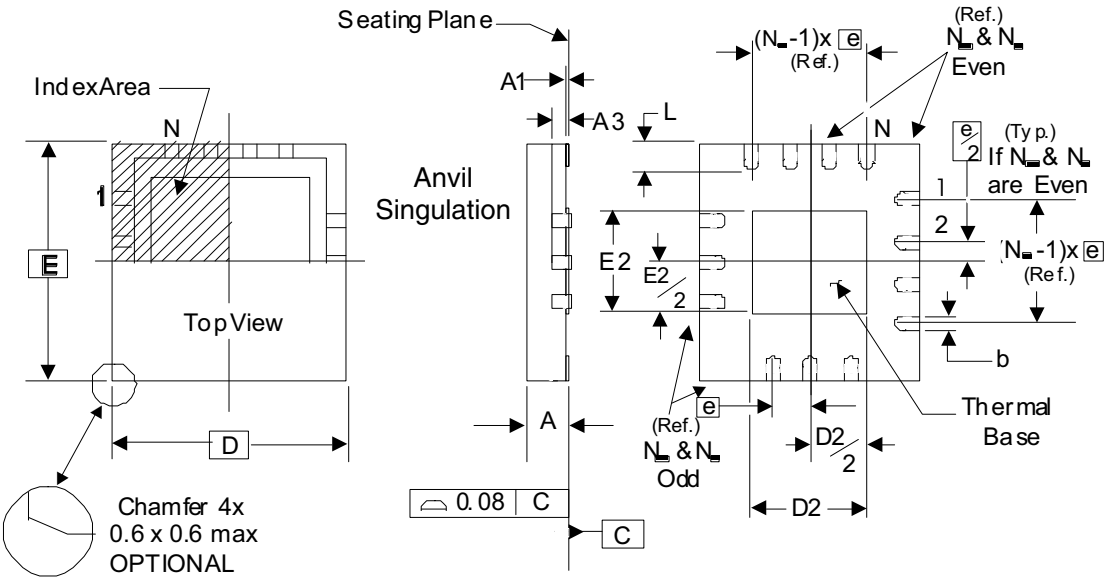
θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	42.7°C/W	37.3°C/W	33.5°C/W

Transistor Count

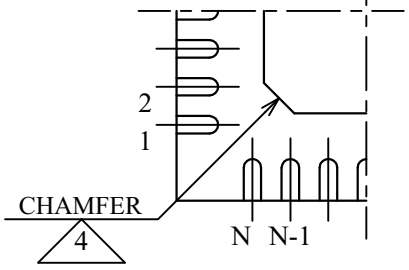
The transistor count for 8S89202: 689

32 Lead VFQFN Package Outline and Package Dimensions

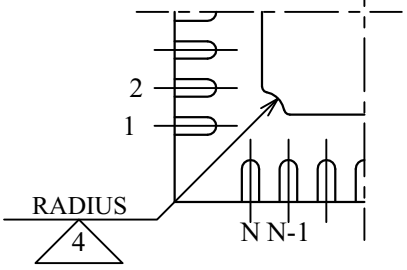
Package Outline - K Suffix for 32 Lead VFQFN



Bottom View w/Type A ID



Bottom View w/Type C ID



There are 2 methods of indicating pin 1 corner at the back of the VFQFN package:

1. Type A: Chamfer on the paddle (near pin 1)
2. Type C: Mouse bite on the paddle (near pin 1)

Table 9. Package Dimensions

JEDEC Variation: VHHD-2/-4 All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		32	
A	0.80		1.00
A1	0		0.05
A3		0.25 Ref.	
b	0.18	0.25	0.30
N_D & N_E			8
D & E		5.00 Basic	
D2 & E2	3.0		3.3
e		0.50 Basic	
L	0.30	0.40	0.50

NOTE: The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pinout are shown on the front page. The package dimensions are in Table 9.

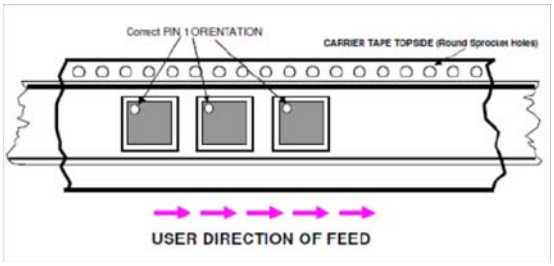
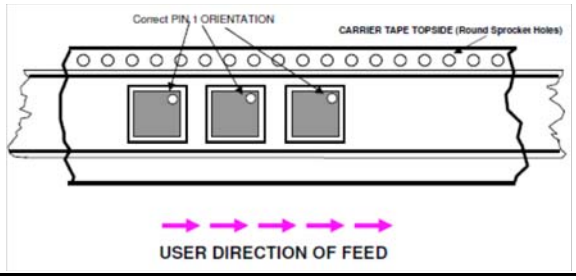
Reference Document: JEDEC Publication 95, MO-220

Ordering Information

Table 8. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8S89202BKILF	ICS89202BIL	“Lead-Free” 32 Lead VFQFN	Tray	-40°C to 85°C
8S89202BKILFT	ICS89202BIL	“Lead-Free” 32 Lead VFQFN	Tape & Reel, pin 1 orientation: EIA-481-C	-40°C to 85°C
8S89202BKILF/W	ICS89202BIL	“Lead-Free” 32 Lead VFQFN	Tape & Reel, pin 1 orientation EIA-481-D	-40°C to 85°C

Table 9. Pin 1 Orientation in Tape and Reel Packaging

Part Number Suffix	Pin 1 Orientation	Illustration
T	Quadrant 1 (EIA-481-C)	
/W	Quadrant 2 (EIA-481-D)	

Revision History Sheet

Rev	Table	Page	Description of Change	Date
B	T9 8	21 21	Added Pin 1 Orientation in Tape and Reel Table. Ordering Information - Added W part number.	7/1/15

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