

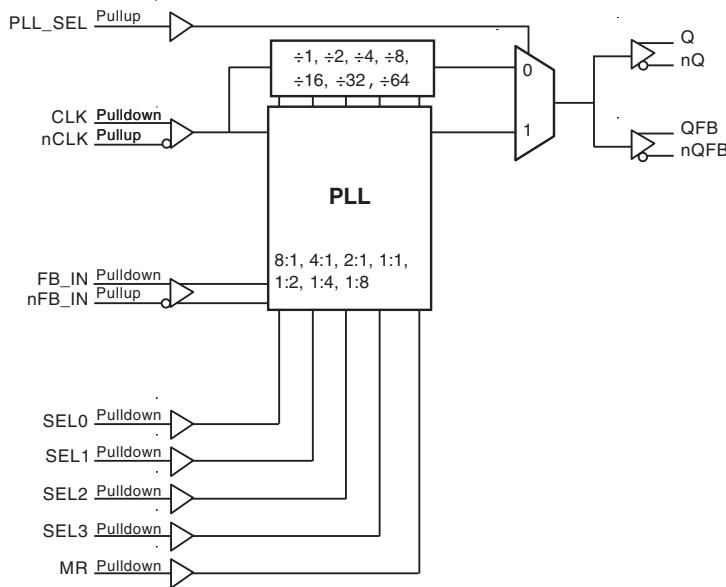
## General Description

The 8725B-21 is a highly versatile 1:1 Differential-to-HSTL Clock Generator. The CLK, nCLK pair can accept most standard differential input levels. The 8725B-21 has a fully integrated PLL and can be configured as zero delay buffer, multiplier or divider, and has an output frequency range of 31.25MHz to 630MHz. The reference divider, feedback divider and output divider are each programmable, thereby allowing for the following output-to-input frequency ratios: 8:1, 4:1, 2:1, 1:1, 1:2, 1:4, 1:8. The external feedback allows the device to achieve “zero delay” between the input clock and the output clocks. The PLL\_SEL pin can be used to bypass the PLL for system test and debug purposes. In bypass mode, the reference clock is routed around the PLL and into the internal output dividers.

## Features

- One differential HSTL output pair
- One differential feedback output pair
- Differential CLK, nCLK input pair
- CLK, nCLK pair can accept the following differential input levels: LVPECL, LVDS, HSTL, HCSL, SSTL
- Output frequency range: 31.25MHz to 630MHz
- Input frequency range: 31.25MHz to 630MHz
- VCO range: 250MHz to 630MHz
- External feedback for “zero delay” clock regeneration with configurable frequencies
- Programmable dividers allow for the following output-to-input frequency ratios: 8:1, 4:1, 2:1, 1:1, 1:2, 1:4, 1:8
- Cycle-to-cycle jitter: 50ps (maximum)
- Output skew: 50ps (maximum)
- Static phase offset: 200ps (maximum)
- 3.3V core, 1.8V output operating supply
- 0°C to 70°C ambient operating temperature

## Block Diagram



## Pin Assignment

CLK	1	20	nc
nCLK	2	19	SEL1
MR	3	18	SEL0
VDD	4	17	VDD
nFB_IN	5	16	PLL_SEL
FB_IN	6	15	VDDA
SEL2	7	14	SEL3
GND	8	13	VDDO
nQFB	9	12	Q
QFB	10	11	nQ

**8725B-21**  
20-Lead SOIC  
7.5mm x 12.8mm package body

## Pin Descriptions and Characteristics

**Table 1. Pin Descriptions<sup>1</sup>**

Number	Name	Type	Description
1	CLK	Input	Pulldown
2	nCLK	Input	Pullup
3	MR	Input	Pulldown
			Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Q and QFB to go low and the inverted outputs nQ and nQFB to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS / LVTTL interface levels.
4	V <sub>DD</sub>	Power	
5	nFB_IN	Input	Pullup
			Inverting differential feedback input to phase detector for regenerating clocks with "Zero Delay." Connect to pin 9.
6	FB_IN	Input	Pulldown
			Non-inverted differential feedback input to phase detector for regenerating clocks with "Zero Delay." Connect to pin 10.
7	SEL2	Input	Pulldown
			Determines output divider values in Table 3. LVCMOS / LVTTL interface levels.
8	GND	Power	
9	nQFB	Output	
			Inverting differential feedback output. HSTL interface levels.
10	QFB	Output	
			Non-inverting differential feedback output. HSTL interface levels.
11	nQ	Output	
			Inverting differential output. HSTL interface levels.
12	Q	Output	
			Non-inverting differential output. HSTL interface levels.
13	V <sub>DDO</sub>	Power	
			Output supply pin.
14	SEL3	Input	Pulldown
			Determines output divider values in Table 3. LVCMOS / LVTTL interface levels.
15	V <sub>DDA</sub>	Power	
			Analog supply pin.
16	PLL_SEL	Input	Pullup
			PLL select. Selects between the PLL and reference clock as the input to the dividers. When LOW, selects reference clock. When HIGH, selects PLL. LVCMOS/LVTTL interface levels.
17	V <sub>DD</sub>	Power	
			Core supply pins.
18	SEL0	Input	Pulldown
			Determines output divider values in Table 3. LVCMOS / LVTTL interface levels.
19	SEL1	Input	Pulldown
			Determines output divider values in Table 3. LVCMOS / LVTTL interface levels.
20	nc	Unused	
			No connect.

NOTE 1. *Pullup* and *Pulldown* refer to internal input resistors. See [Table 2, Pin Characteristics](#), for typical values.

**Table 2. Pin Characteristics**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
R <sub>PULLUP</sub>	Input Pullup Resistor			51		kΩ
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			51		kΩ

## Function Tables

Table 3A. Control Input Function Table

Inputs					Outputs PLL_SEL = 1 PLL Enable Mode
SEL3	SEL2	SEL1	SEL0	Reference Frequency Range (MHz)	Q, nQ
0	0	0	0	250 - 630	$\div 1$
0	0	0	1	125 - 315	$\div 1$
0	0	1	0	62.5 - 157.5	$\div 1$
0	0	1	1	31.25 - 78.75	$\div 1$
0	1	0	0	250 - 630	$\div 2$
0	1	0	1	125 - 315	$\div 2$
0	1	1	0	62.5 - 157.5	$\div 2$
0	1	1	1	250 - 630	$\div 4$
1	0	0	0	125 - 315	$\div 4$
1	0	0	1	250 - 630	$\div 8$
1	0	1	0	125 - 315	$\times 2$
1	0	1	1	62.5 - 157.5	$\times 2$
1	1	0	0	31.25 - 78.75	$\times 2$
1	1	0	1	62.5 - 157.5	$\times 4$
1	1	1	0	31.25 - 78.75	$\times 4$
1	1	1	1	31.25 - 78.75	$\times 8$

Table 3B. PLL Bypass Function Table

Inputs				Outputs PLL_SEL = 0 PLL Bypass Mode
SEL3	SEL2	SEL1	SEL0	Q, nQ, QFB, nQFB
0	0	0	0	$\div 4$
0	0	0	1	$\div 4$
0	0	1	0	$\div 4$
0	0	1	1	$\div 8$
0	1	0	0	$\div 8$
0	1	0	1	$\div 8$
0	1	1	0	$\div 16$
0	1	1	1	$\div 16$
1	0	0	0	$\div 32$
1	0	0	1	$\div 64$
1	0	1	0	$\div 2$
1	0	1	1	$\div 2$
1	1	0	0	$\div 4$
1	1	0	1	$\div 1$
1	1	1	0	$\div 2$
1	1	1	1	$\div 1$

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, $V_{DD}$	4.6V
Inputs, $V_I$	-0.5V to $V_{DD} + 0.5V$
Outputs, $V_O$	-0.5V to $V_{DDO} + 0.5V$
Package Thermal Impedance, $\theta_{JA}$	46.2°C/W (0 Ifpm)
Storage Temperature, $T_{STG}$	-65°C to 150°C
Junction Temperature	125°C

## DC Electrical Characteristics

**Table 4A. Power Supply DC Characteristics,  $V_{DD} = V_{DDA} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = 0^\circ C$  to  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Core Supply Voltage		3.135	3.3	3.465	V
$V_{DDA}$	Analog Supply Voltage		3.135	3.3	3.465	V
$V_{DDO}$	Output Supply Voltage		1.6	1.8	2.0	V
$I_{DD}$	Power Supply Current				137	mA
$I_{DDA}$	Analog Supply Current				17	mA
$I_{DDO}$	Output Supply Current	No Load		0		mA

**Table 4B. LVC MOS/LV TTL DC Characteristics,  $V_{DD} = V_{DDA} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = 0^\circ C$  to  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage		2		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage		-0.3		0.8	V
$I_{IH}$	Input High Current Current	SEL[0:3], MR	$V_{DD} = V_{IN} = 3.465V$		150	$\mu A$
		PLL_SEL	$V_{DD} = V_{IN} = 3.465V$		5	$\mu A$
$I_{IL}$	Input Low Current	SEL[0:3], MR	$V_{DD} = 3.465V$ , $V_{IN} = 0V$	-5		$\mu A$
		PLL_SEL	$V_{DD} = 3.465V$ , $V_{IN} = 0V$	-150		$\mu A$

**Table 4C. Differential DC Characteristics,  $V_{DD} = V_{DDA} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = 0^\circ C$  to  $70^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$I_{IH}$	Input High Current	$V_{DD} = V_{IN} = 3.465V$			150	$\mu A$
		$V_{DD} = V_{IN} = 3.465V$			5	$\mu A$
$I_{IL}$	Input Low Current	$V_{DD} = 3.465V$ , $V_{IN} = 0V$	-5			$\mu A$
		$V_{DD} = 3.465V$ , $V_{IN} = 0V$	-150			$\mu A$
$V_{PP}$	Peak-to-Peak Voltage <sup>1</sup>		0.15		1.3	V
$V_{CMR}$	Common Mode Input Voltage <sup>1, 2</sup>		GND + 0.5		$V_{DD} - 0.85$	V

NOTE 1.  $V_{IL}$  should not be less than -0.3V.NOTE 2. Common mode input voltage is defined as  $V_{IH}$ .**Table 4D. HSTL DC Characteristics,  $V_{DD} = V_{DDA} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = 0^\circ C$  to  $70^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OH}$	Output High Voltage <sup>1</sup>		1.0		1.4	V
$V_{OL}$	Output Low Voltage <sup>1</sup>		0		0.4	V
$V_{ox}$	Output Crossover Voltage <sup>2</sup>		40		60	%
$V_{SWING}$	Peak-to-Peak Output Voltage Swing		0.6		1.1	V

NOTE 1. Outputs termination with  $50\Omega$  to ground.

NOTE 2. Defined with respect to output voltage swing at a given condition.

**Table 5. Input Frequency Characteristics,  $V_{DD} = V_{DDA} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = 0^\circ C$  to  $70^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units	
$F_{IN}$	Input Frequency	CLK, nCLK	PLL_SEL = 1	31.25		630	MHz
			PLL_SEL = 0			630	MHz

## AC Electrical Characteristics

**Table 6. AC Characteristics,  $V_{DD} = V_{DDA} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ <sup>1, 2</sup>**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Output Frequency				630	MHz
$t_{PD}$	Propagation Delay <sup>3</sup>	PLL_SEL = 0V, $f \leq 630\text{MHz}$	3.2		4.5	ns
$t_{sk(\emptyset)}$	Static Phase Offset <sup>4, 5</sup>	PLL_SEL = 3.3V	-125	37.5	200	ps
$t_{sk(o)}$	Output Skew <sup>5, 6</sup>	PLL_SEL = 0V			50	ps
$t_{jit(cc)}$	Cycle-to-Cycle Jitter <sup>5, 7</sup>				50	ps
$t_{jit(\theta)}$	Phase Jitter <sup>5, 7, 8</sup>				$\pm 50$	ps
$t_L$	PLL Lock Time				1	ms
$t_R / t_F$	Output Rise/Fall Time	20% to 80% @ 50MHz	300		700	ps
$t_{PW}$	Output Pulse Width		$t_{PERIOD}/2 - 90$	$t_{PERIOD}/2$	$t_{PERIOD}/2 + 90$	ps

NOTE 1. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 2. All parameters measured at  $f_{MAX}$  unless noted otherwise.

NOTE 3. Measured from the differential input crossing point to the differential output crossing point.

NOTE 4. Defined as the time difference between the input reference clock and the average feedback input signal, when the PLL is locked and the input reference frequency is stable.

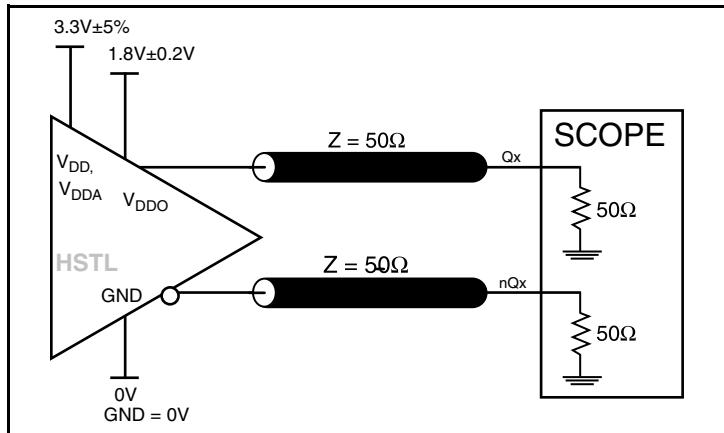
NOTE 5. This parameter is defined in accordance with JEDEC Standard 65.

NOTE 6. Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.

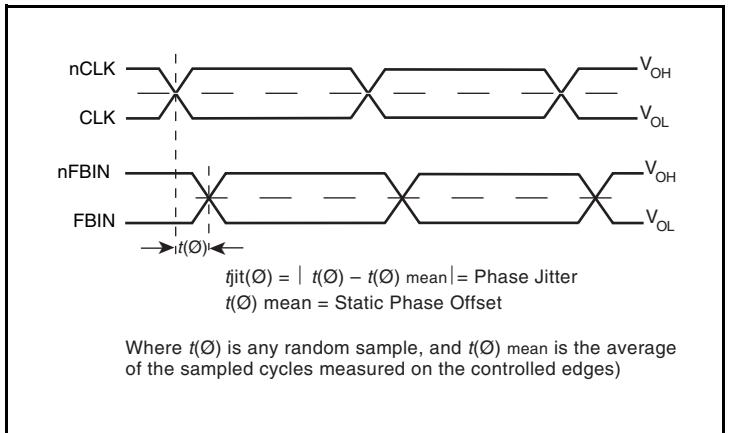
NOTE 7. Characterized at VCO frequency of 622MHz.

NOTE 8. Phase jitter is dependent on the input source used.

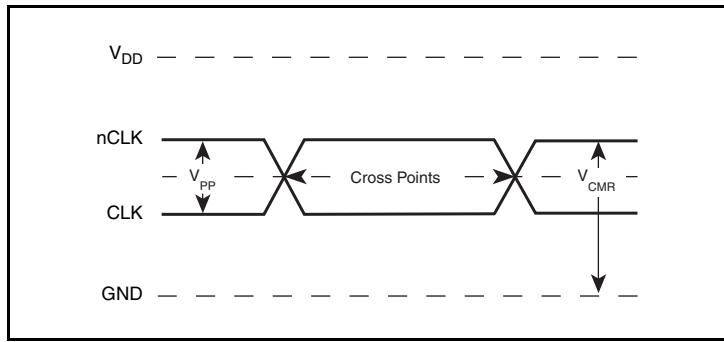
## Parameter Measurement Information



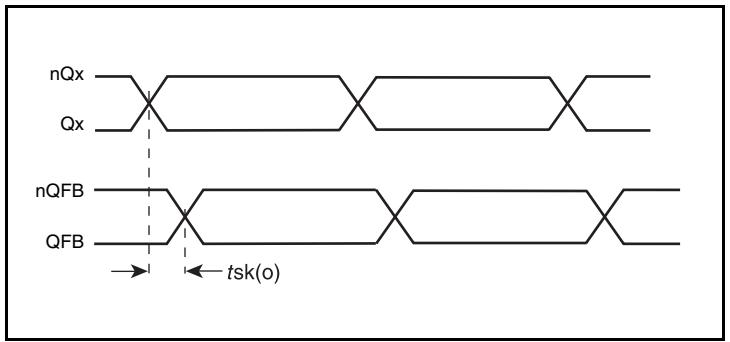
3.3V Core/1.8V Output Load AC Test Circuit



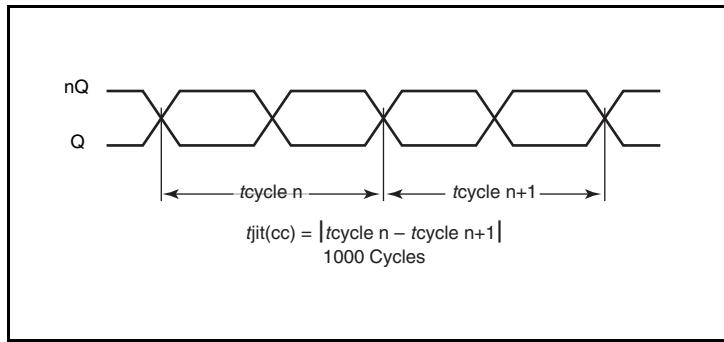
Phase Jitter and Static Phase Offset



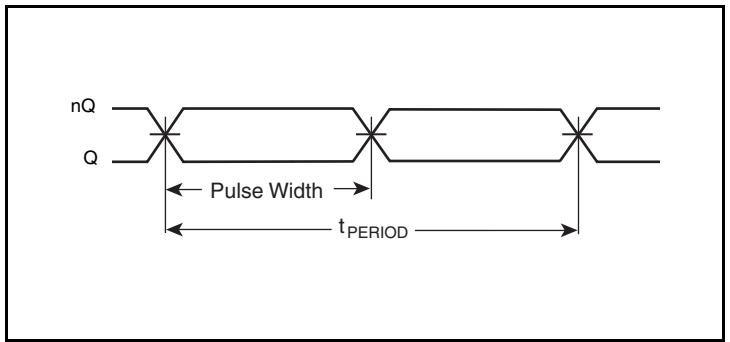
Differential Input Level



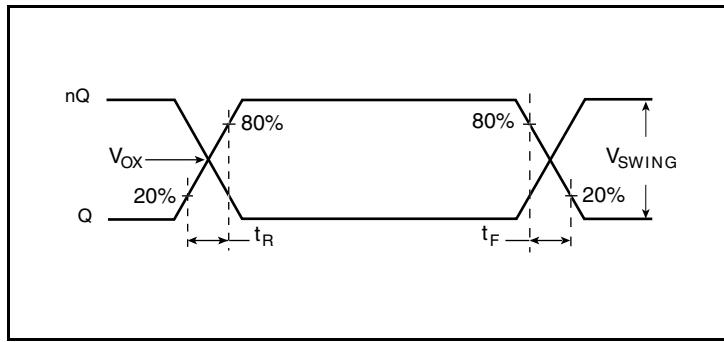
Output Skew



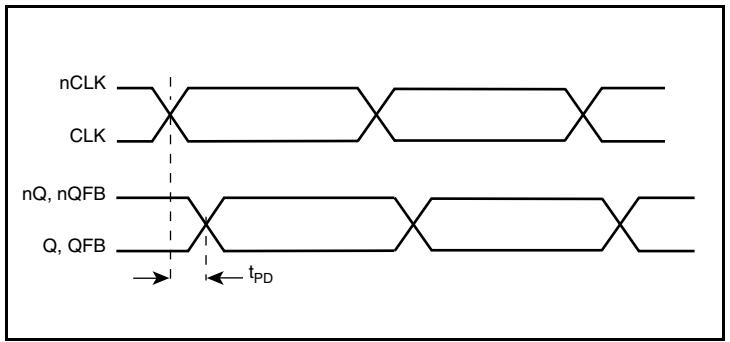
Cycle-to-Cycle Jitter



Output Pulse Width



Output Rise/Fall Time



Propagation Delay

## Applications Information

### Recommendations for Unused Input Pins

#### Inputs:

##### LVC MOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A  $1\text{k}\Omega$  resistor can be used.

## Wiring the Differential Input to Accept Single-Ended Levels

*Figure 1* shows how a differential input can be wired to accept single ended levels. The reference voltage  $V_1 = V_{DD}/2$  is generated by the bias resistors  $R1$  and  $R2$ . The bypass capacitor ( $C1$ ) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of  $R1$  and  $R2$  might need to be adjusted to position the  $V_1$  in the center of the input voltage swing. For example, if the input clock swing is  $2.5\text{V}$  and  $V_{DD} = 3.3\text{V}$ ,  $R1$  and  $R2$  value should be adjusted to set  $V_1$  at  $1.25\text{V}$ . The values below are for when both the single ended swing and  $V_{DD}$  are at the same voltage. This configuration requires that the sum of the output impedance of the driver ( $R_o$ ) and the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First,  $R3$  and  $R4$  in parallel should equal the transmission line impedance. For most  $50\Omega$  applications,  $R3$  and  $R4$  can be  $100\Omega$ .

The values of the resistors can be increased to reduce the loading for slower and weaker LVC MOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVC MOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however  $V_{IL}$  cannot be less than  $-0.3\text{V}$  and  $V_{IH}$  cannot be more than  $V_{DD} + 0.3\text{V}$ . Suggested edge rate faster than  $1\text{V/ns}$ . Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

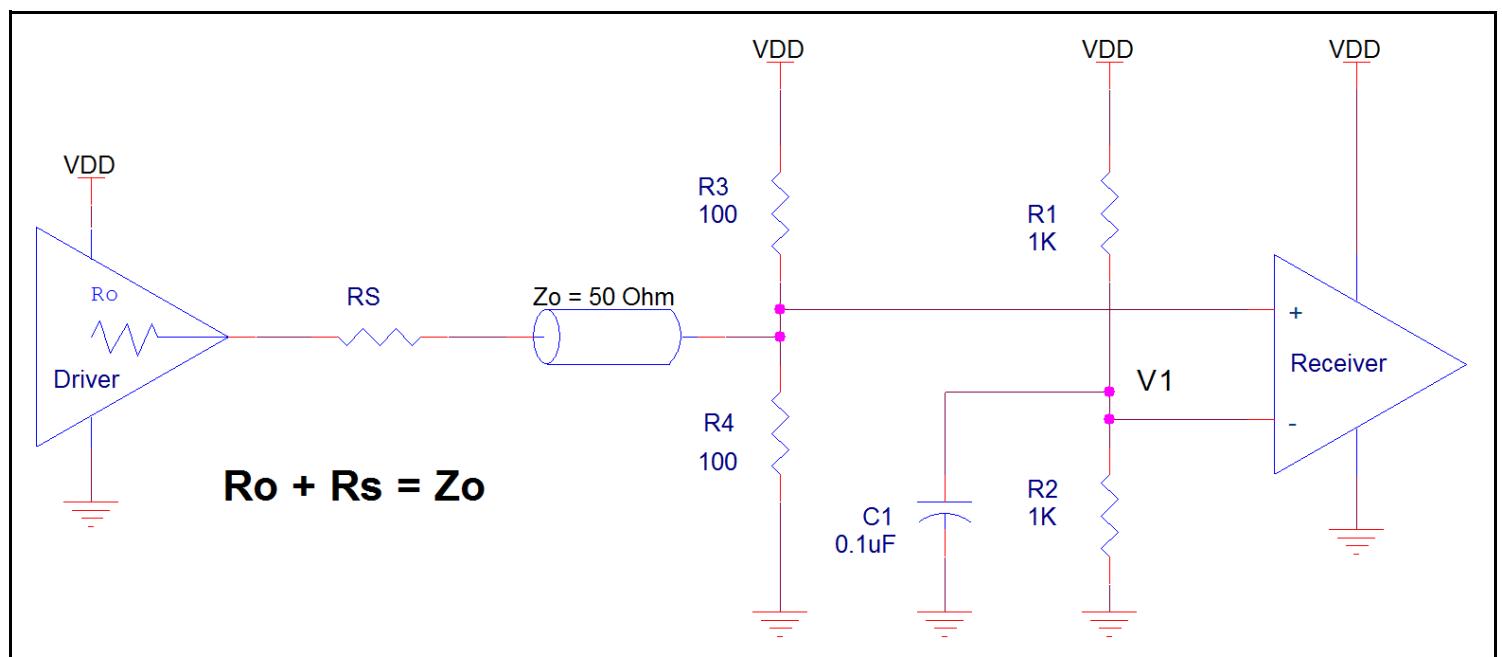
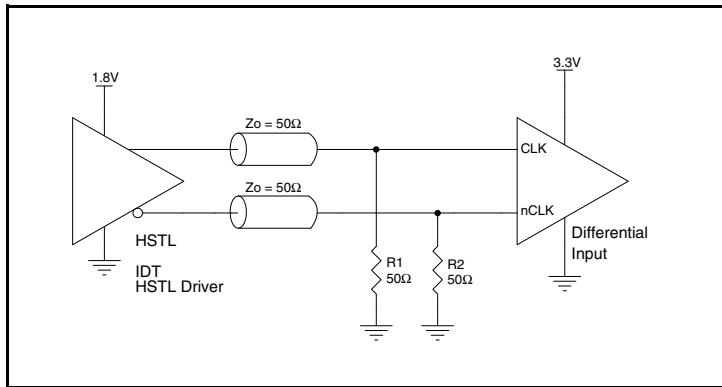


Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

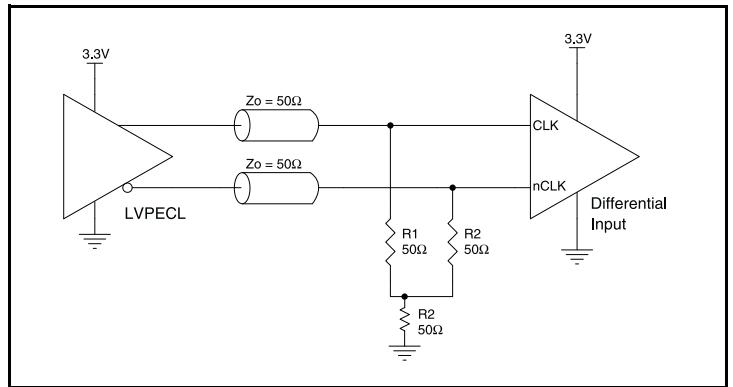
## Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, HSTL, SSTL, HCSL and other differential signals. Both  $V_{SWING}$  and  $V_{OH}$  must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. [Figure 2A](#) to [Figure 2F](#) show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only.

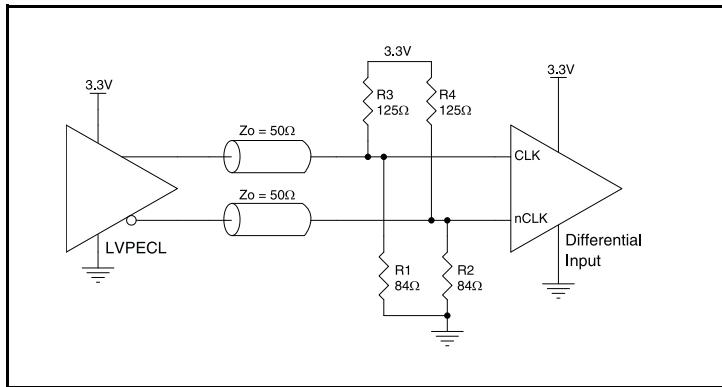
Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in [Figure 2A](#), the input termination applies for IDT open emitter HSTL drivers. If you are using an HSTL driver from another vendor, use their termination recommendation.



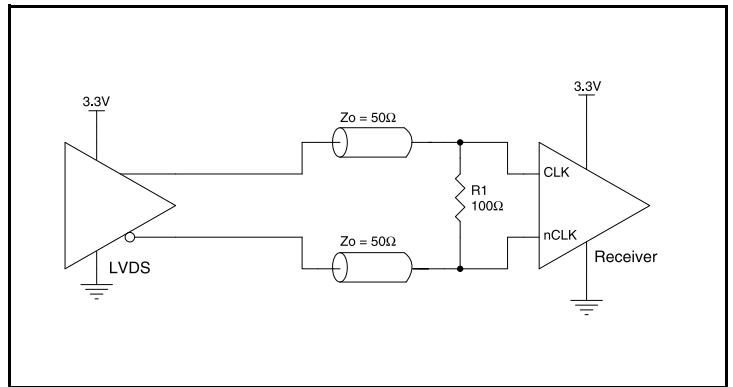
**Figure 2A. CLK/nCLK Input Driven by an IDT Open Emitter HSTL Driver**



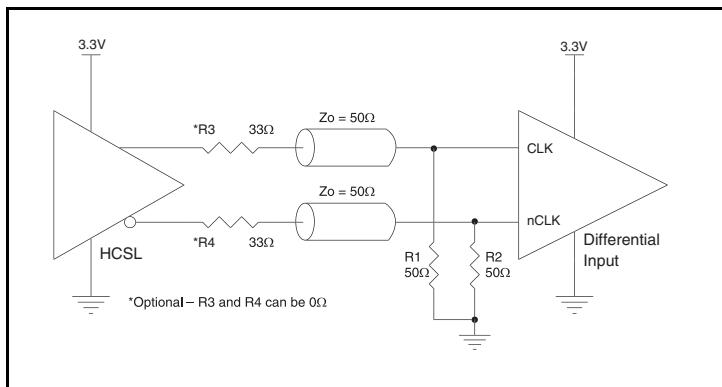
**Figure 2D. CLK/nCLK Input Driven by a 3.3V LVPECL Driver**



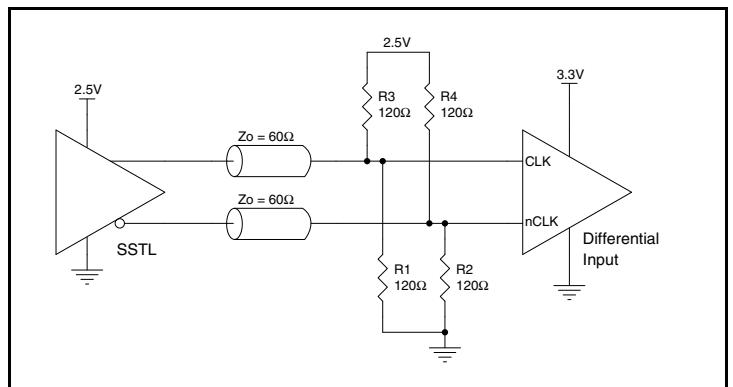
**Figure 2B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver**



**Figure 2E. CLK/nCLK Input Driven by a 3.3V LVDS Driver**



**Figure 2C. CLK/nCLK Input Driven by a 3.3V HCSL Driver**



**Figure 2F. CLK/nCLK Input Driven by a 2.5V SSTL Driver**

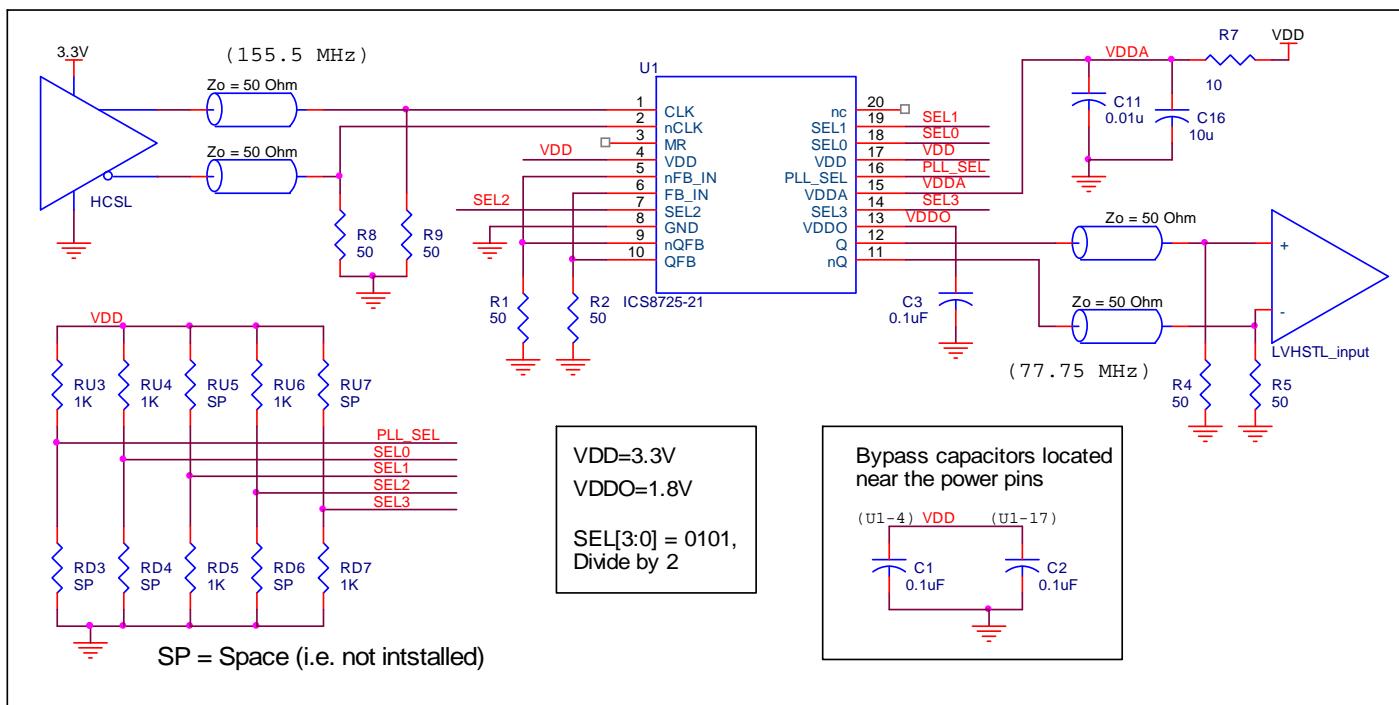
## Schematic Example

**Figure 3** shows a schematic example of the 8725B-21. In this example, the input is driven by an HCSL driver. The zero delay buffer is configured to operate at 155.52MHz input and 77.75MHz output. The logic control pins are configured as follows:

SEL[3:0] = 0101

PLL\_SEL = 1

For 8725B-21, the decoupling capacitors should be physically located near the power pin.



**Figure 3. 8725B-21 HSTL Buffer Schematic Example**

## Power Considerations

This section provides information on power dissipation and junction temperature for the 8725B-21. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the 8725B-21 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{DD} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{DD\_MAX} * (I_{DD\_MAX} + I_{DDA\_MAX}) = 3.465V * (137mA + 17mA) = 533.6\text{mW}$
- Power (outputs)<sub>MAX</sub> = **32.8mW/Loaded Output pair**

**Total Power<sub>MAX</sub>** (3.465V, with all outputs switching) = 533.6mW + 32.8mW = **566.4mW**

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for is 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * P_{d\_total} + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$P_{d\_total}$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 39.7°C/W per [Table 7](#) below.

Therefore,  $T_j$  for an ambient temperature of 70°C with all outputs switching is:

$70^\circ\text{C} + 0.566\text{W} * 39.7^\circ\text{C/W} = 111^\circ\text{C}$ . This is below the limit of 125°C.

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (single layer or multi-layer).

**Table 7. Thermal Resistance  $\theta_{JA}$  for 20-Lead SOIC, Forced Convection<sup>1</sup>**

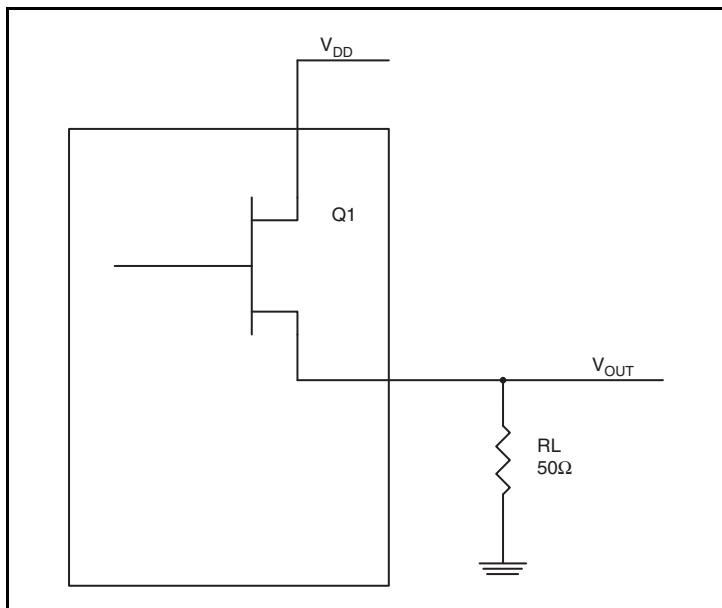
$\theta_{JA}$ vs. Air Flow			
Linear Feet per Minute	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	83.2°C/W	65.7°C/W	57.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	46.2°C/W	39.7°C/W	36.8°C/W

NOTE 1. Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

### 3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

HSTL output driver circuit and termination are shown in *Figure 4*.



**Figure 4. HSTL Driver Circuit and Termination**

To calculate worst case power dissipation into the load, use the following equations which assume a  $50\Omega$  load.

$P_{d\_H}$  is power dissipation when the output drives high.

$P_{d\_L}$  is the power dissipation when the output drives low.

$$P_{d\_H} = (V_{OH\_MAX}/R_L) * (V_{DD\_MAX} - V_{OH\_MAX})$$

$$P_{d\_L} = (V_{OL\_MAX}/R_L) * (V_{DD\_MAX} - V_{OL\_MAX})$$

$$P_{d\_H} = (1.0V/50\Omega) * (2V - 1.0V) = 20mW$$

$$P_{d\_L} = (0.4V/50\Omega) * (2V - 0.4V) = 12.8mW$$

$$\text{Total Power Dissipation per output pair} = P_{d\_H} + P_{d\_L} = 32.8mW$$

## Reliability Information

Table 8.  $\theta_{JA}$  vs. Air Flow Table for a 20-Lead TSSOP<sup>1</sup>

$\theta_{JA}$ vs. Air Flow			
Linear Feet per Minute	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	83.2°C/W	65.7°C/W	57.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	46.2°C/W	39.7°C/W	36.8°C/W

NOTE 1. Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

## Transistor Count

The transistor count for 8725B-21 is: 2969

## Package Outline and Package Dimensions

Package Outline - M Suffix for 20-Lead SOIC

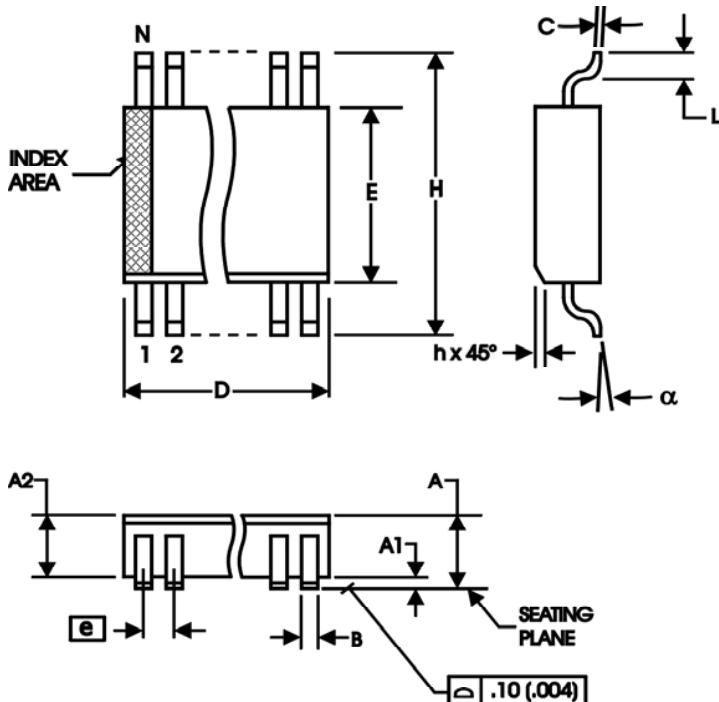


Table 9. Package Dimensions for 20-Lead SOIC

300 Millimeters All Dimensions in Millimeters		
Symbol	Minimum	Maximum
N	20	
A		2.65
A1	0.10	
A2	2.05	2.55
B	0.33	0.51
C	0.18	0.32
D	12.60	13.00
E	7.40	7.60
e	1.27 Basic	
H	10.00	10.65
h	0.25	0.75
L	0.40	1.27
a	0°	8°

Reference Document: JEDEC Publication 95, MS-013, MS-119

## Ordering Information

**Table 10. Ordering Information**

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS8725BM-21LF	ICS8725BM-21LF	20-Lead SOIC, Lead-Free	Tube	0°C to 70°C
ICS8725BM-21LFT	ICS8725BM-21LF	20-Lead SOIC, Lead-Free	Tape & Reel	0°C to 70°C



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