

# 3.3V CMOS 16-BIT BUS TRANSCIVER/REGISTER WITH 3-STATE OUTPUTS, 5 VOLT TOLERANT I/O AND BUS-HOLD

**IDT74LVCH16646A**  
**NOT RECOMMENDED  
FOR NEW DESIGNS**

## FEATURES:

- Typical  $t_{sk(o)}$  (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- $V_{cc} = 3.3V \pm 0.3V$ , Normal Range
- $V_{cc} = 2.7V$  to 3.6V, Extended Range
- CMOS power levels (0.4 $\mu$ W typ. static)
- All inputs, outputs, and I/O are 5V tolerant
- Supports hot insertion
- Available in TSSOP package

## DRIVE FEATURES:

- High Output Drivers:  $\pm 24mA$
- Reduced system switching noise

## APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

## DESCRIPTION:

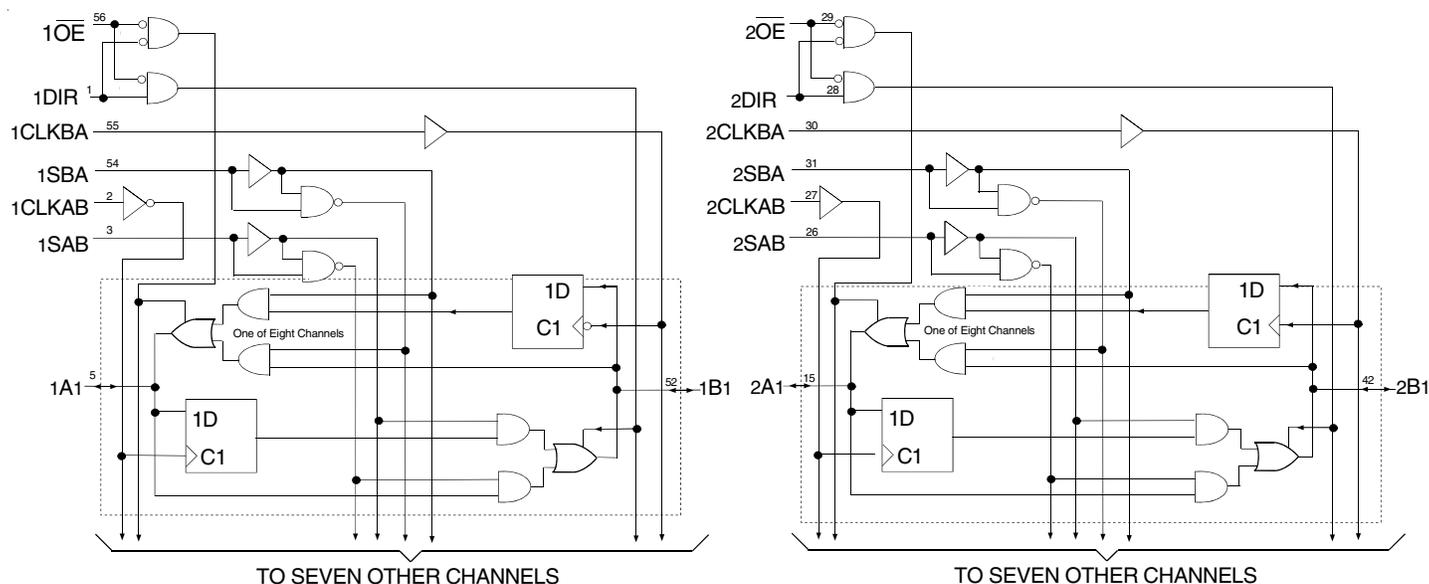
The LVCH16646A 16-bit bus transceiver and register is built using advanced dual metal CMOS technology. This high-speed, low power device is organized as two independent 8-bit D-type transceivers with 3-state D-type registers. The controls circuitry is organized for multiplexed transmission of data between A bus and B bus either directly or from the internal storage registers. Each 8-bit transceiver/register features direction control (DIR), over-riding Output Enable control ( $\overline{OE}$ ) and Select lines (SAB and SBA) to select either real-time data or stored data. Separate clock inputs are provided for A and B port registers. Data on the A or B data bus, or both, can be stored in the internal registers by the low-to-high transitions at the appropriate clock pins. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

All pins can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V supply system.

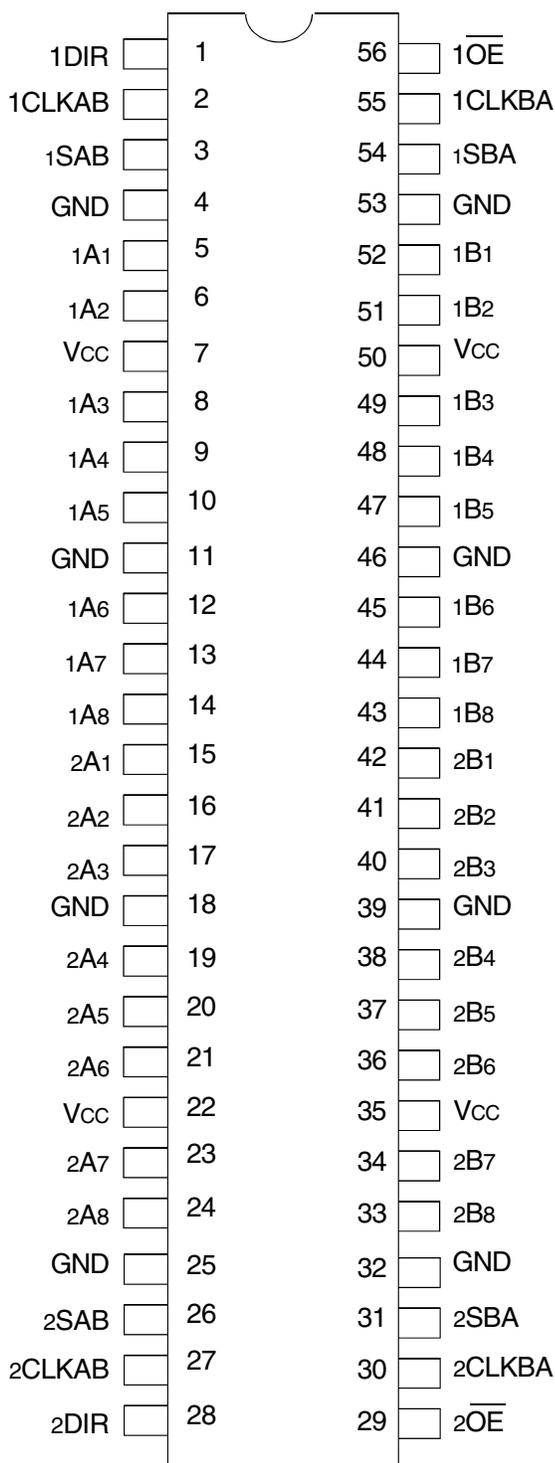
The LVCH16646A has been designed with a  $\pm 24mA$  output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

The LVCH16646A has "bus-hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

## FUNCTIONAL BLOCK DIAGRAM



## PIN CONFIGURATION



TSSOP  
TOP VIEW

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Description	Max	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +6.5	V
TSTG	Storage Temperature	-65 to +150	°C
IOUT	DC Output Current	-50 to +50	mA
I <sub>IK</sub> I <sub>OK</sub>	Continuous Clamp Current, V <sub>I</sub> < 0 or V <sub>O</sub> < 0	-50	mA
I <sub>CC</sub> I <sub>SS</sub>	Continuous Current through each V <sub>CC</sub> or GND	±100	mA

### NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## CAPACITANCE (T<sub>A</sub> = +25°C, F = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	4.5	6	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	6.5	8	pF
C <sub>I/O</sub>	I/O Port Capacitance	V <sub>IN</sub> = 0V	6.5	8	pF

### NOTE:

- As applicable to the device type.

## PIN DESCRIPTION

Pin Names	Description
xAx	Data Register A Inputs <sup>(1)</sup> Data Register B Outputs
xBx	Data Register B Inputs <sup>(1)</sup> Data Register A Outputs
xCLKAB, xCLKBA	Clock Pulse Inputs
xSAB, xSBA	Output Data Source Select Inputs
x $\overline{OE}$	Output Enable Inputs
xDIR	Direction Control Inputs

### NOTE:

- These pins have "Bus-Hold". All other pins are standard inputs, outputs, or I/Os.

## FUNCTION TABLE(1)

Inputs						Data I/O <sup>(2)</sup>		Operation or Function
x $\overline{OE}$	xDIR	xCLKAB	xCLKBA	xSAB	xSBA	xAx	xBx	
X	X	↑	X	X	X	Input	Unspecified	Store A, B unspecified <sup>(2)</sup>
X	X	X	↑	X	X	Unspecified	Input	Store B, A unspecified <sup>(2)</sup>
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	H or L	H or L	X	X	Input	Input	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real time A data to B bus
L	H	H or L	X	H	X	Input	Output	Stored A data to B bus

### NOTES:

- H = HIGH Voltage Level  
X = Don't Care  
L = LOW Voltage Level  
↑ = LOW-to-HIGH transition
- The data output functions may be enabled or disabled by various signals at the x $\overline{OE}$  or xDIR inputs. Data input functions are always enabled, i.e. data at the bus pins will be stored on every LOW-to-HIGH transition of the clock inputs.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

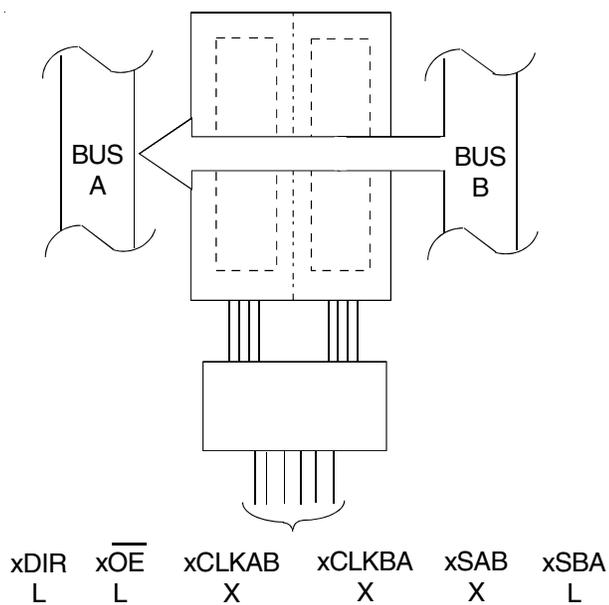
Following Conditions Apply Unless Otherwise Specified:

Operating Condition: TA = -40°C to +85°C

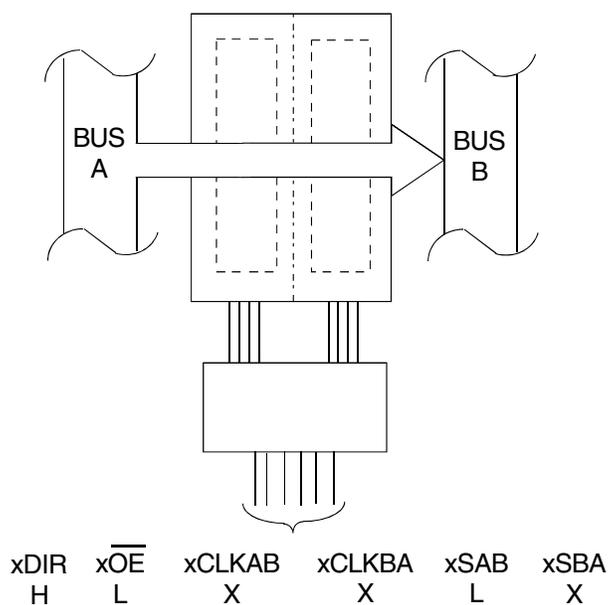
Symbol	Parameter	Test Conditions		Min.	Typ. <sup>(1)</sup>	Max.	Unit
VIH	Input HIGH Voltage Level	VCC = 2.3V to 2.7V		1.7	—	—	V
		VCC = 2.7V to 3.6V		2	—	—	
VIL	Input LOW Voltage Level	VCC = 2.3V to 2.7V		—	—	0.7	V
		VCC = 2.7V to 3.6V		—	—	0.8	
IIH IIL	Input Leakage Current	VCC = 3.6V	VI = 0 to 5.5V	—	—	±5	μA
IOZH IOZL	High Impedance Output Current (3-State Output pins)	VCC = 3.6V	VO = 0 to 5.5V	—	—	±10	μA
IOFF	Input/Output Power Off Leakage	VCC = 0V, VIN or VO ≤ 5.5V		—	—	±50	μA
VIK	Clamp Diode Voltage	VCC = 2.3V, IIN = -18mA		—	-0.7	-1.2	V
VH	Input Hysteresis	VCC = 3.3V		—	100	—	mV
ICCL ICCH IC CZ	Quiescent Power Supply Current	VCC = 3.6V	VIN = GND or VCC	—	—	10	μA
			3.6 ≤ VIN ≤ 5.5V <sup>(2)</sup>	—	—	10	
ΔIcc	Quiescent Power Supply Current Variation	One input at VCC - 0.6V, other inputs at VCC or GND		—	—	500	μA

### NOTES:

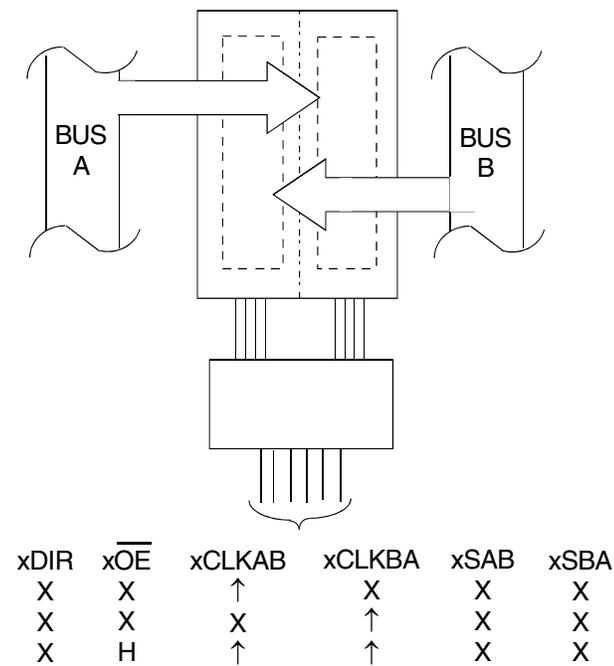
- Typical values are at VCC = 3.3V, +25°C ambient.
- This applies in the disabled state only.



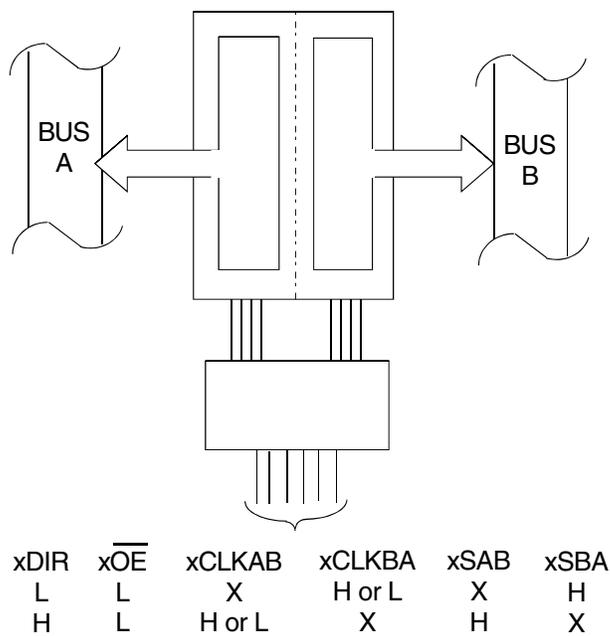
*Real-Time Transfer  
Bus B to A*



*Real-Time Transfer  
Bus A to B*



*Storage from  
A, B, or A and B*



*Transfer Stored  
Data to A and/or B*

## BUS-HOLD CHARACTERISTICS

Symbol	Parameter <sup>(1)</sup>	Test Conditions		Min.	Typ. <sup>(2)</sup>	Max.	Unit
IBHH IBHL	Bus-Hold Input Sustain Current	V <sub>CC</sub> = 3V	V <sub>I</sub> = 2V	-75	—	—	μA
			V <sub>I</sub> = 0.8V	75	—	—	
IBHH IBHL	Bus-Hold Input Sustain Current	V <sub>CC</sub> = 2.3V	V <sub>I</sub> = 1.7V	—	—	—	μA
			V <sub>I</sub> = 0.7V	—	—	—	
IBHHO IBHLO	Bus-Hold Input Overdrive Current	V <sub>CC</sub> = 3.6V	V <sub>I</sub> = 0 to 3.6V	—	—	±500	μA

**NOTES:**

1. Pins with Bus-Hold are identified in the pin description.
2. Typical values are at V<sub>CC</sub> = 3.3V, +25°C ambient.

## OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = 2.3V to 3.6V	I <sub>OH</sub> = -0.1mA	V <sub>CC</sub> -0.2	—	V
		V <sub>CC</sub> = 2.3V	I <sub>OH</sub> = -6mA	2	—	
		V <sub>CC</sub> = 2.3V	I <sub>OH</sub> = -12mA	1.7	—	
		V <sub>CC</sub> = 2.7V		2.2	—	
		V <sub>CC</sub> = 3V		2.4	—	
			V <sub>CC</sub> = 3V	I <sub>OH</sub> = -24mA	2	
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = 2.3V to 3.6V	I <sub>OL</sub> = 0.1mA	—	0.2	V
		V <sub>CC</sub> = 2.3V	I <sub>OL</sub> = 6mA	—	0.4	
			I <sub>OL</sub> = 12mA	—	0.7	
		V <sub>CC</sub> = 2.7V	I <sub>OL</sub> = 12mA	—	0.4	
		V <sub>CC</sub> = 3V	I <sub>OL</sub> = 24mA	—	0.55	

**NOTE:**

1. V<sub>IH</sub> and V<sub>IL</sub> must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V<sub>CC</sub> range. T<sub>A</sub> = -40°C to +85°C.

## OPERATING CHARACTERISTICS, V<sub>CC</sub> = 3.3V ± 0.3V, T<sub>A</sub> = 25°C

Symbol	Parameter	Test Conditions	Typical	Unit
CPD	Power Dissipation Capacitance per Transceiver Outputs enabled	C <sub>L</sub> = 0pF, f = 10Mhz	60	pF
CPD	Power Dissipation Capacitance per Transceiver Outputs disabled		12	

## SWITCHING CHARACTERISTICS(1)

Symbol	Parameter	V <sub>CC</sub> = 2.7V		V <sub>CC</sub> = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	
f <sub>MAX</sub>		150	—	150	—	MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay xAx to xBx or xBx to xAx	—	6.8	1.3	5.7	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay xCLKBA or xCLKAB to xAx or xBx	—	7.9	1.8	6.7	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay xSBA or xSAB to xAx or xBx	—	9.2	1.7	7.7	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time x $\overline{OE}$ to xAx or Bx	—	8.5	1.3	6.9	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time xDIR to xAx or Bx	—	8.5	1.4	7.2	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time x $\overline{OE}$ to xAx or Bx	—	7.7	2.1	6.9	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time xDIR to xAx or Bx	—	7.8	2	7	ns
t <sub>SU</sub>	Set-up Time xAx or xBx before CLKAB $\uparrow$ or CLKBA $\uparrow$	3.2	—	2.9	—	ns
t <sub>H</sub>	Hold Time xAx or xBx after CLKAB $\uparrow$ or CLKBA $\uparrow$	0	—	0.3	—	ns
t <sub>w</sub>	Pulse Duration, CLK HIGH or LOW	3.3	—	3.3	—	ns
t <sub>SK(o)</sub>	Output Skew <sup>(2)</sup>	—	—	—	500	ps

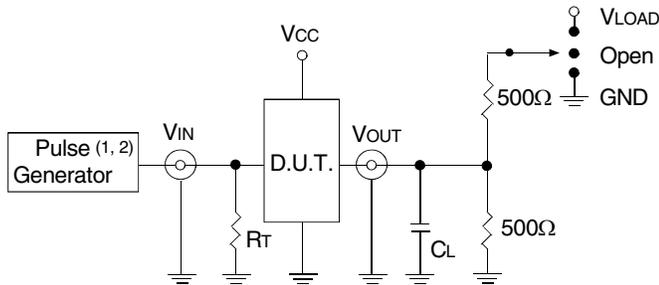
**NOTES:**

1. See TEST CIRCUITS AND WAVEFORMS. T<sub>A</sub> = - 40°C to + 85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

## TEST CIRCUITS AND WAVEFORMS

### TEST CONDITIONS

Symbol	V <sub>CC</sub> <sup>(1)</sup> =3.3V±0.3V	V <sub>CC</sub> <sup>(1)</sup> =2.7V	V <sub>CC</sub> <sup>(2)</sup> =2.5V±0.2V	Unit
V <sub>LOAD</sub>	6	6	2 x V <sub>CC</sub>	V
V <sub>IH</sub>	2.7	2.7	V <sub>CC</sub>	V
V <sub>T</sub>	1.5	1.5	V <sub>CC</sub> / 2	V
V <sub>LZ</sub>	300	300	150	mV
V <sub>HZ</sub>	300	300	150	mV
C <sub>L</sub>	50	50	30	pF



LVC Link

Test Circuit for All Outputs

#### DEFINITIONS:

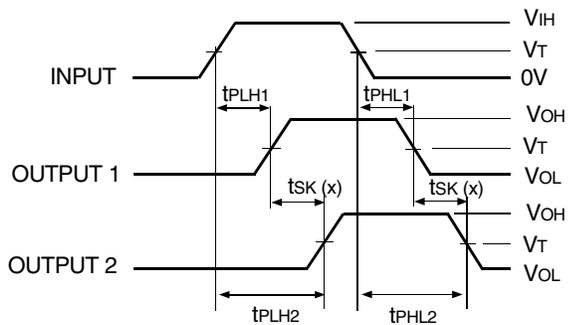
C<sub>L</sub> = Load capacitance: includes jig and probe capacitance.  
R<sub>T</sub> = Termination resistance: should be equal to Z<sub>OUT</sub> of the Pulse Generator.

#### NOTES:

1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t<sub>r</sub> ≤ 2.5ns; t<sub>r</sub> ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t<sub>r</sub> ≤ 2ns; t<sub>r</sub> ≤ 2ns.

### SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V <sub>LOAD</sub>
Disable High Enable High	GND
All Other Tests	Open



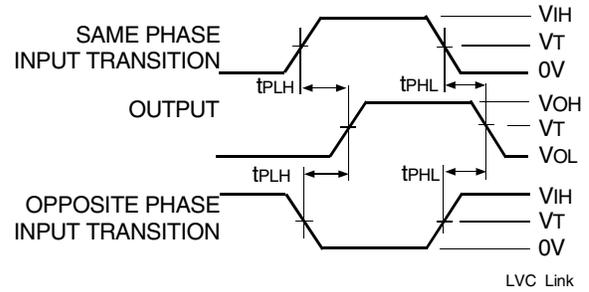
$$tsk(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

LVC Link

Output Skew - tsk(x)

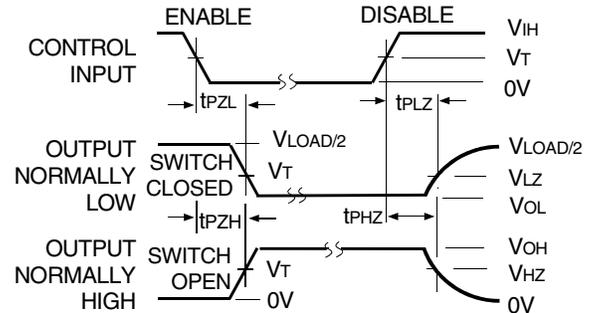
#### NOTES:

1. For tsk(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For tsk(b) OUTPUT1 and OUTPUT2 are in the same bank.



LVC Link

Propagation Delay

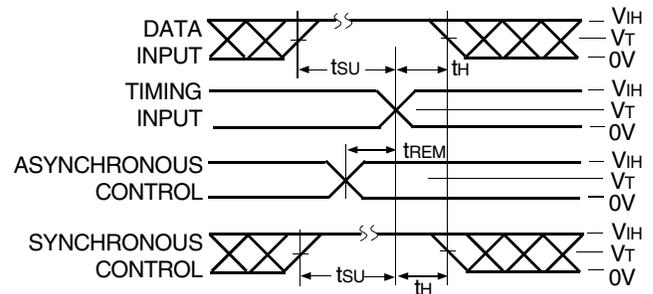


LVC Link

Enable and Disable Times

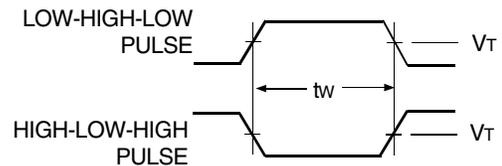
#### NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.



LVC Link

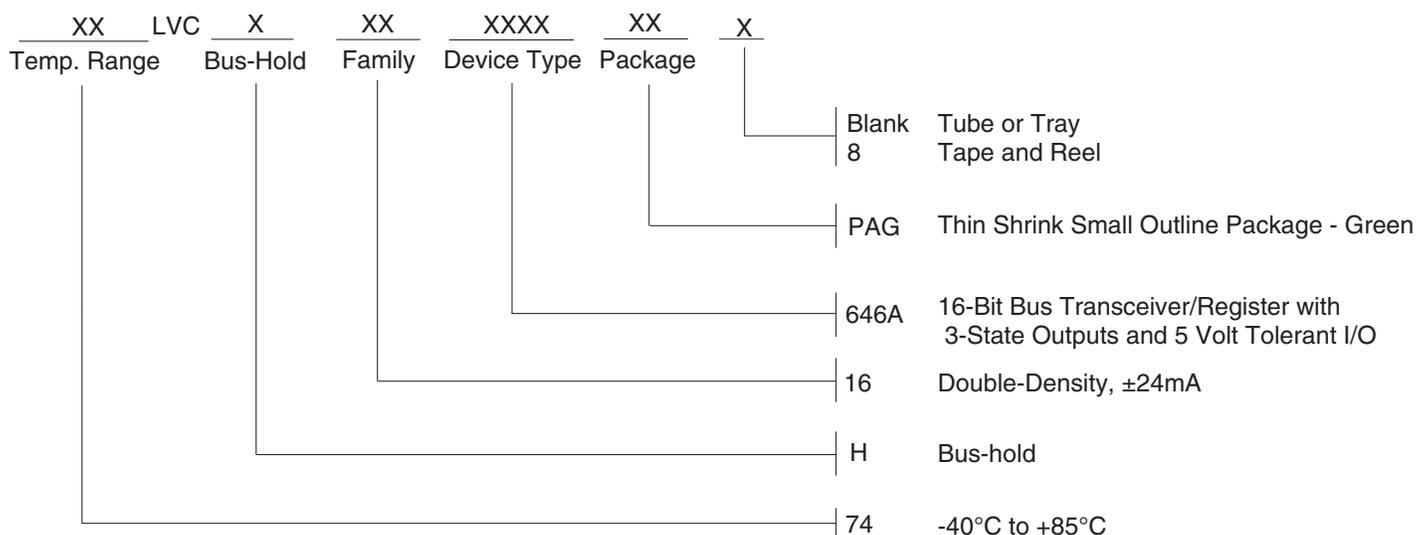
Set-up, Hold, and Release Times



LVC Link

Pulse Width

## ORDERING INFORMATION



## DATASHEET DOCUMENT HISTORY

01/28/2016 Pg. 1, 2, 8 Updated the ordering information by removing IDT notation, non RoHS parts and adding Tape and Reel information.

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