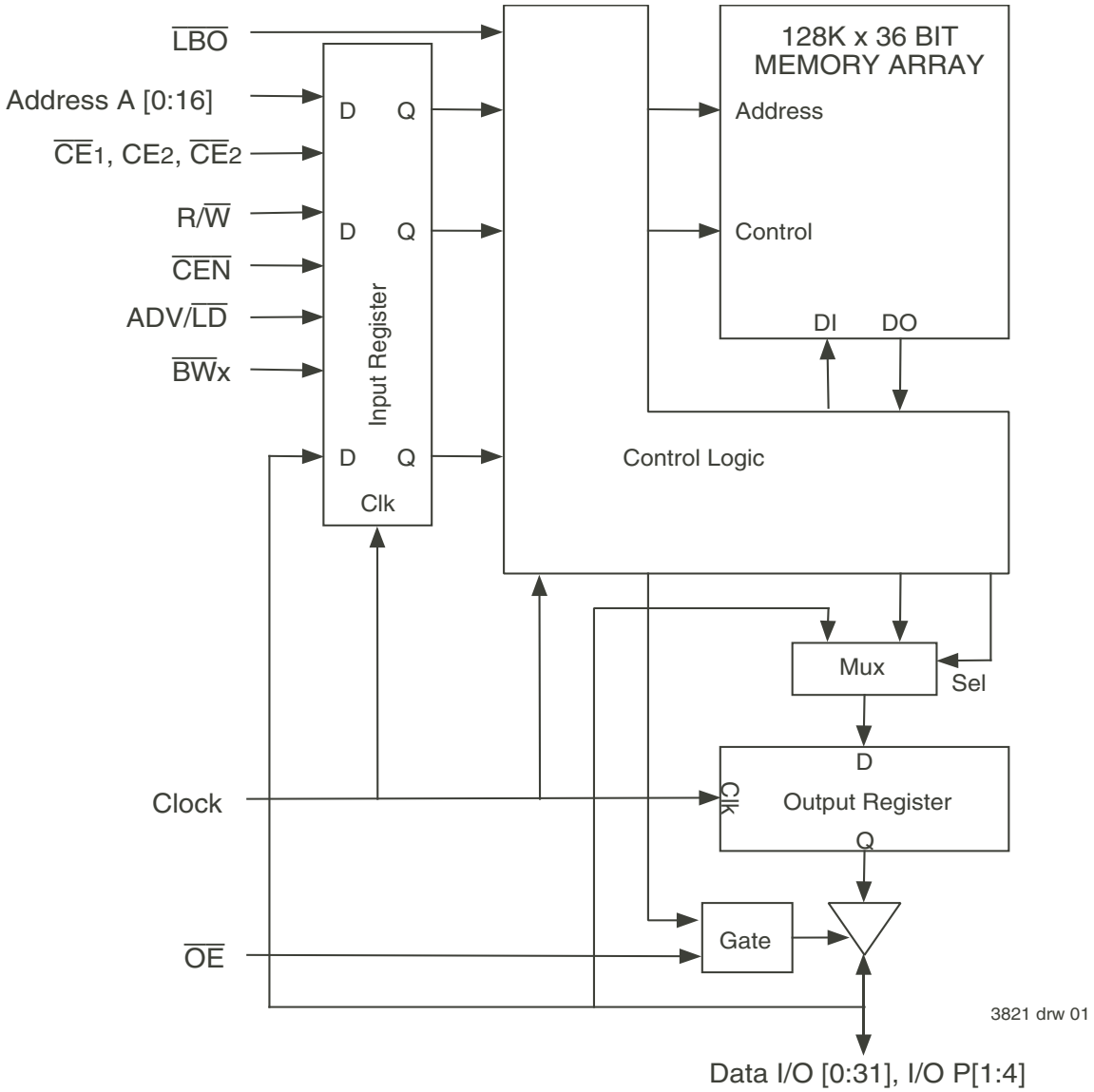
128K x 36, 3.3V Synchronous SRAM with ZBT™ Feature Burst Counter and Pipelined Outputs

IDT71V546S

Features

- 128K x 36 memory configuration, pipelined outputs
- Supports high performance system speed - 133 MHz (4.2 ns Clock-to-Data Access)
- ZBT™ Feature - No dead cycles between write and read cycles
- Internally synchronized registered outputs eliminate the need to control $\overline{OE}$
- Single R/$\overline{W}$ (READ/WRITE) control pin
- Positive clock-edge triggered address, data, and control signal registers for fully pipelined applications
- 4-word burst capability (interleaved or linear)
- Individual byte write ($\overline{BW}_1$ - $\overline{BW}_4$) control (May tie active)
- Three chip enables for simple depth expansion
- Single 3.3V power supply (±5%)
- Packaged in a JEDEC standard 100-pin TQFP package
- Green parts available, see Ordering Information

Functional Block Diagram



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Description

The IDT71V546 is a 3.3V high-speed 4,718,592-bit (4.5 Megabit) synchronous SRAM organized as 128K x 36 bits. It is designed to eliminate dead bus cycles when turning the bus around between reads and writes, or writes and reads. Thus it has been given the name ZBT™, or Zero Bus Turn-around.

Address and control signals are applied to the SRAM during one clock cycle, and two cycles later its associated data cycle occurs, be it read or write.

The IDT71V546 contains data I/O, address and control signal registers. Output enable is the only asynchronous signal and can be used to disable the outputs at any given time.

A Clock Enable ($\overline{CEN}$) pin allows operation of the IDT71V546 to be suspended as long as necessary. All synchronous inputs are ignored when $\overline{CEN}$ is high and the internal device registers will hold their previous values.

There are three chip enable pins ($\overline{CE}_1$, CE_2, $\overline{CE}_2$) that allow the user to deselect the device when desired. If any one of these three is not active when ADV/$\overline{LD}$ is low, no new memory operation can be initiated and any burst that was in progress is stopped. However, any pending data transfers (reads or writes) will be completed. The data bus will tri-state two cycles after the chip is deselected or a write initiated.

The IDT71V546 has an on-chip burst counter. In the burst mode, the IDT71V546 can provide four cycles of data for a single address presented to the SRAM. The order of the burst sequence is defined by the $\overline{LBO}$ input pin. The $\overline{LBO}$ pin selects between linear and interleaved burst sequence. The ADV/$\overline{LD}$ signal is used to load a new external address (ADV/$\overline{LD}$ = LOW) or increment the internal burst counter (ADV/$\overline{LD}$ = HIGH).

The IDT71V546 SRAM utilizes a high-performance, high-volume 3.3V CMOS process, and is packaged in a JEDEC standard 14mm x 20mm 100- pin thin plastic quad flatpack (TQFP) for high board density.

Pin Description Summary

A_0 - A_{16}	Address Inputs	Input	Synchronous
$\overline{CE}_1$, CE_2, $\overline{CE}_2$	Three Chip Enables	Input	Synchronous
$\overline{OE}$	Output Enable	Input	Asynchronous
R/$\overline{W}$	Read/Write Signal	Input	Synchronous
$\overline{CEN}$	Clock Enable	Input	Synchronous
$\overline{BW}_1$, $\overline{BW}_2$, $\overline{BW}_3$, $\overline{BW}_4$	Individual Byte Write Selects	Input	Synchronous
CLK	Clock	Input	N/A
ADV/$\overline{LD}$	Advance Burst Address / Load New Address	Input	Synchronous
$\overline{LBO}$	Linear / Interleaved Burst Order	Input	Static
I/O_0 - I/O_{31}, I/O_{P1} - I/O_{P4}	Data Input/Output	I/O	Synchronous
V_{DD}	3.3V Power	Supply	Static
V_{SS}	Ground	Supply	Static

3821 tbl 01

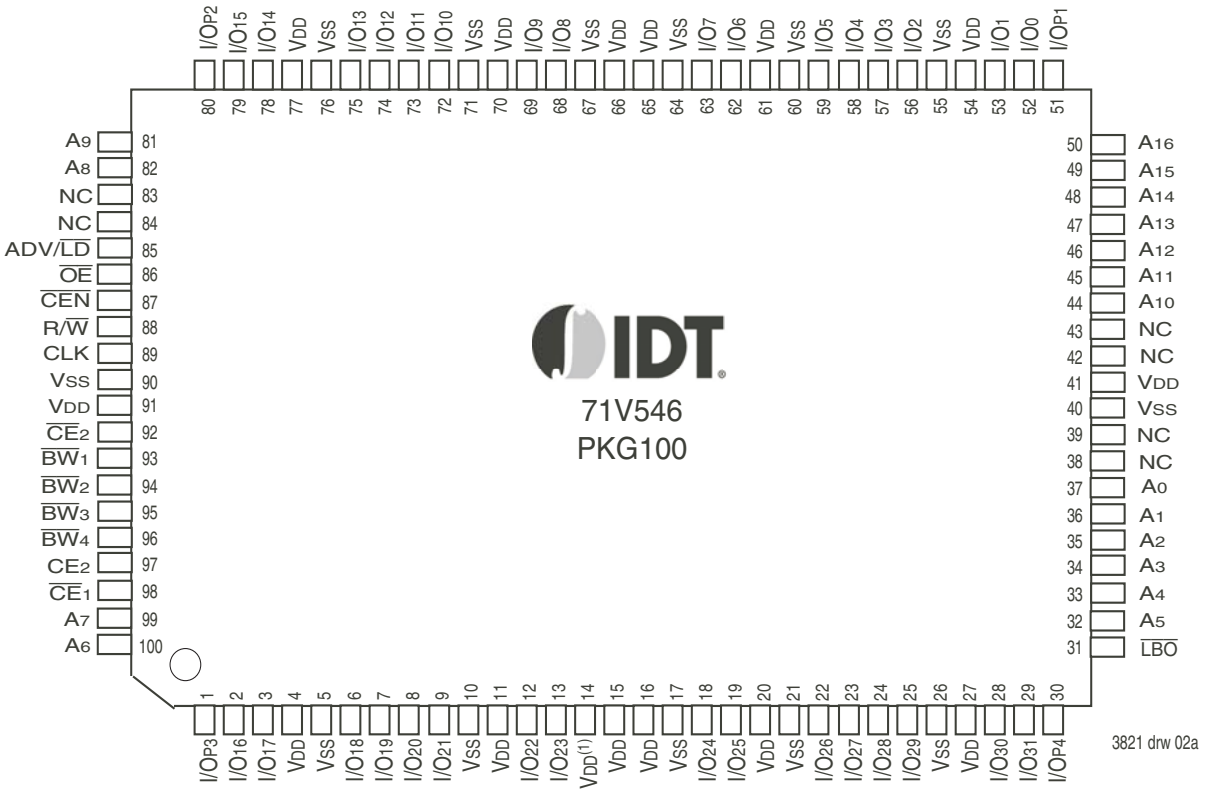
Pin Definitions(1)

Symbol	Pin Function	I/O	Active	Description
A_0 - A_{16}	Address Inputs	I	N/A	Synchronous Address inputs. The address register is triggered by a combination of the rising edge of CLK and ADV/$\overline{LD}$ Low, $\overline{CEN}$ Low and true chip enables.
ADV/$\overline{LD}$	Address/Load	I	N/A	ADV/$\overline{LD}$ is a synchronous input that is used to load the internal registers with new address and control when it is sampled low at the rising edge of clock with the chip selected. When ADV/$\overline{LD}$ is low with the chip deselected, any burst in progress is terminated. When ADV/$\overline{LD}$ is sampled high then the internal burst counter is advanced for any burst that was in progress. The external addresses are ignored when ADV/$\overline{LD}$ is sampled high.
R/$\overline{W}$	Read/Write	I	N/A	R/$\overline{W}$ signal is a synchronous input that identified whether the current load cycle initiated is a Read or Write access to the memory array. The data bus activity for the current cycle takes place two clock cycles later.
$\overline{CEN}$	Clock Enable	I	LOW	Synchronous Clock Enable Input. When $\overline{CEN}$ is sampled high, all other synchronous inputs, including clock are ignored and outputs remain unchanged. The effect of $\overline{CEN}$ sampled high on the device outputs is as if the low to high clock transition did not occur. For normal operation, $\overline{CEN}$ must be sampled low at rising edge of clock.
$\overline{BW}_1$ - $\overline{BW}_4$	Individual Byte Write Enables	I	LOW	Synchronous byte write enables. Enable 9-bit byte has its own active low byte write enable. On load write cycles (When R/$\overline{W}$ and ADV/$\overline{LD}$ are sampled low) the appropriate byte write signal ($\overline{BW}_1$ - $\overline{BW}_4$) must be valid. The byte write signal must also be valid on each cycle of a burst write. Byte Write signals are ignored when R/$\overline{W}$ is sampled high. The appropriate byte(s) of data are written into the device two cycles later. $\overline{BW}_1$ - $\overline{BW}_4$ can all be tied low if always doing write to the entire 36-bit word.
$\overline{CE}_1$, $\overline{CE}_2$	Chip Enables	I	LOW	Synchronous active low chip enable. $\overline{CE}_1$ and $\overline{CE}_2$ are used with CE_2 to enable the IDT71V546. ($\overline{CE}_1$ or $\overline{CE}_2$ sampled high or CE_2 sampled low) and ADV/$\overline{LD}$ low at the rising edge of clock, initiates a deselect cycle. the ZBT™ has a two cycle deselect, i.e., the data bus will tri-state two clock cycles after deselect is initiated.
CE2	Chip Enable	I	HIGH	Synchronout active high chip enable. CE_2 is used with $\overline{CE}_1$ and $\overline{CE}_2$ to enable the chip. CE_2 has inverted polarity but otherwise identical to $\overline{CE}_1$ and $\overline{CE}_2$.
CLK	Clock	I	N/A	This is the clock input to the IDT71V546. Except for $\overline{OE}$, all timing references for the device are made with respect to the rising edge of CLK.
I/O_0 - I/O_{31} I/O_{P1} - I/O_{P4}	Data Input/Output	I/O	N/A	Synchronous data input/output (I/O) pins. Both the data input path and data output path are registered and triggered by the rising edge of CLK.
$\overline{LBO}$	Linear Burst Order	I	LOW	Burst order selection input. When $\overline{LBO}$ is high the Interleaved burst sequence is selected. When $\overline{LBO}$ is low the Linear burst sequence is selected. $\overline{LBO}$ is a static DC input.
$\overline{OE}$	Output Enable	I	LOW	Asynchronous output enable. $\overline{OE}$ must be low to read data from the 71V546. When $\overline{OE}$ is high the I/O pins are in a high-impedance state. $\overline{OE}$ does not need to be actively controlled for read and write cycles. In normal operation, $\overline{OE}$ can be tied low.
V_{DD}	Power Supply	N/A	N/A	3.3V power supply input.
V_{SS}	Ground	N/A	N/A	Ground pin.

3821 tbl 02

NOTE:
1. All synchronous inputs must meet specified setup and hold times with respect to CLK.

Pin Configuration — 128K X 36



100 TQFP
Top View

NOTE:
1. Pin 14 does not have to be connected directly to V_{DD} as long as the input voltage is $\geq V_{IH}$.

Absolute Maximum Ratings(1)

Symbol	Rating	Commercial & Industrial Values	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	-0.5 to V_{DD}+0.5	V
T_A(4)	**Commercial** Operating Ambient Temperature	0 to +70	°C
	Industrial Operating Ambient Temperature	-40 to +85	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-55 to +125	°C
P_T	Power Dissipation	2.0	W
I_{OUT}	DC Output Current	50	mA

3821 tbl 05

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{DD} and Input terminals only.
3. I/O terminals.
4. During production testing, the case temperature equals the ambient temperature.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}(3)	Supply Voltage	3.135	3.3	3.465	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage - Inputs	2.0	—	4.6	V
V_{IH}	Input High Voltage - I/O	2.0	—	V_{DD}+0.3(2)	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

3821 tbl 04

NOTES:
1. V_{IL} (min.) = –1.0V for pulse width less than $t_{CYC/2}$, once per cycle.
2. V_{IH} (max.) = +6.0V for pulse width less than $t_{CYC/2}$, once per cycle.
3. V_{DD} needs to be ramped up smoothly to the operating level. If there are any glitches on V_{DD} that cause the voltage level to drop below 2.0 volts then the device needs to be reset by holding V_{DD} to 0.0 volts for a minimum of 100 ms.

Recommended Operating Temperature and Supply Voltage

Grade	Ambient Temperature(1)	V_{SS}	V_{DD}
Commercial	0°C to +70°C	0V	3.3V±5%
Industrial	-40°C to +85°C	0V	3.3V±5%

3821 tbl 03

NOTES:
1. During production testing, the case temperature equals the ambient temperature.

100 TQFP Capacitance

(T_A = +25°C, f = 1.0MHz, TQFP package)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	5	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	7	pF

3821 tbl 06

NOTE:
1. This parameter is guaranteed by device characterization, but not production tested.

Synchronous Truth Table(1)

$\overline{CEN}$	R/$\overline{W}$	Chip(5) Enable	ADV/$\overline{LD}$	$\overline{BW}$x	ADDRESS USED	PREVIOUIS CYCLE	CURRENT CYCLE	I/O (2 cycles later)
L	L	Select	L	Valid	External	X	LOAD WRITE	D(7)
L	H	Select	L	X	External	X	LOAD READ	Q(7)
L	X	X	H	Valid	Internal	LOAD WRITE/ BURST WRITE	BURST WRITE (Advance Burst Counter)(2)	D(7)
L	X	X	H	X	Internal	LOAD READ/ BURST READ	BURST READ (Advance Burst Counter)(2)	Q(7)
L	X	Deselect	L	X	X	X	DESELECT or STOP(3)	HiZ
L	X	X	H	X	X	DESELECT / NOOP	NOOP	HiZ
H	X	X	X	X	X	X	SUSPEND(4)	Previous Value

3821 tbl 07

NOTES:

1. L = V_{IL}, H = V_{IH}, X = Don't Care.
2. When ADV/$\overline{LD}$ signal is sampled high, the internal burst counter is incremented. The R/$\overline{W}$ signal is ignored when the counter is advanced. Therefore the nature of the burst cycle (Read or Write) is determined by the status of the R/$\overline{W}$ signal when the first address is loaded at the beginning of the burst cycle.
3. Deselect cycle is initiated when either ($\overline{CE}_1$, or $\overline{CE}_2$ is sampled high or CE_2 is sampled low) and ADV/$\overline{LD}$ is sampled low at rising edge of clock. The data bus will tri-state two cycles after deselect is initiated.
4. When $\overline{CEN}$ is sampled high at the rising edge of clock, that clock edge is blocked from propagating through the part. The state of all the internal registers and the I/Os remains unchanged.
5. To select the chip requires $\overline{CE}_1$ = L, $\overline{CE}_2$ = L, CE_2 = H on these chip enables. Chip is deselected if either one of the chip enables is false.
6. Device Outputs are ensured to be in High-Z after the first rising edge of clock upon power-up.
7. Q - Data read from the device, D - data written to the device.

Partial Truth Table for Writes(1)

Operation	R/$\overline{W}$	$\overline{BW}_1$	$\overline{BW}_2$	$\overline{BW}_3$	$\overline{BW}_4$
READ	H	X	X	X	X
WRITE ALL BYTES	L	L	L	L	L
WRITE BYTE 1 (I/O [0:7], I/O_{P1})(2)	L	L	H	H	H
WRITE BYTE 2 (I/O [8:15], I/O_{P2})(2)	L	H	L	H	H
WRITE BYTE 3 (I/O [16:23], I/O_{P3})(2)	L	H	H	L	H
WRITE BYTE 4 (I/O [24:31], I/O_{P4})(2)	L	H	H	H	L
NO WRITE	L	H	H	H	H

3821 tbl 08

NOTES:

1. L = V_{IL}, H = V_{IH}, X = Don't Care.
2. Multiple bytes may be selected during the same cycle.

Interleaved Burst Sequence Table ($\overline{LBO}$=VDD)

	Sequence 1		Sequence 2		Sequence 3		Sequence 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
Second Address	0	1	0	0	1	1	1	0
Third Address	1	0	1	1	0	0	0	1
Fourth Address(1)	1	1	1	0	0	1	0	0

3821 tbl 09

NOTE:
1. Upon completion of the Burst sequence the counter wraps around to its initial state and continues counting.

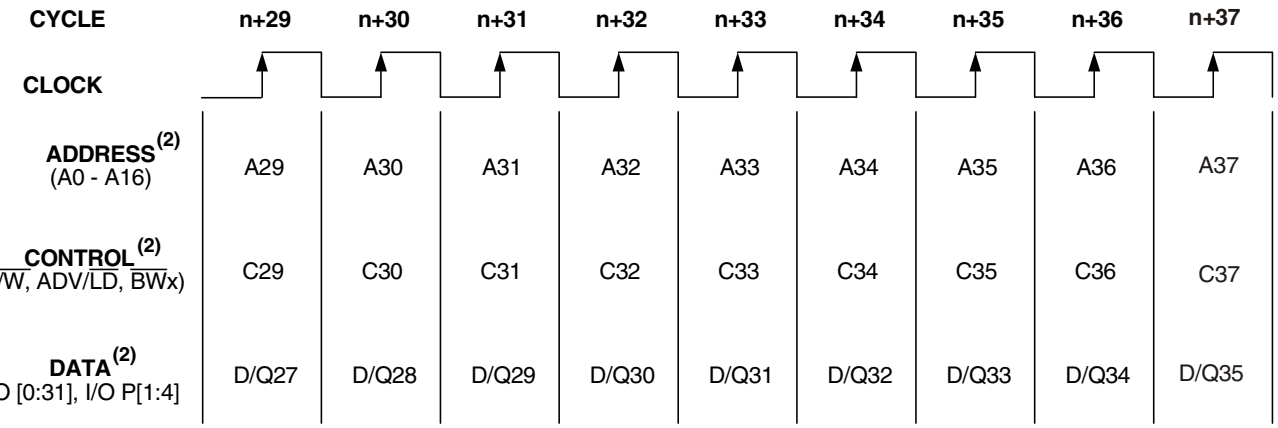
Linear Burst Sequence Table ($\overline{LBO}$=VSS)

	Sequence 1		Sequence 2		Sequence 3		Sequence 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
Second Address	0	1	1	0	1	1	0	0
Third Address	1	0	1	1	0	0	0	1
Fourth Address(1)	1	1	0	0	0	1	1	0

3821 tbl 10

NOTE:
1. Upon completion of the Burst sequence the counter wraps around to its initial state and continues counting.

Functional Timing Diagram(1)



3821 drw 03

NOTES:
1. This assumes $\overline{CEN}$, $\overline{CE}_1$, CE_2, $\overline{CE}_2$ are all true.
2. All Address, Control and Data_In are only required to meet set-up and hold time with respect to the rising edge of clock. Data_Out is valid after a clock-to-data delay from the rising edge of clock.

Device Operation - Showing Mixed Load, Burst, Deselect and NOOP Cycles(2)

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}$(1)	$\overline{CEN}$	$\overline{BW}$x	$\overline{OE}$	I/O	Comments
n	A0	H	L	L	L	X	X	X	Load read
n+1	X	X	H	X	L	X	X	X	Burst read
n+2	A1	H	L	L	L	X	L	Q0	Load read
n+3	X	X	L	H	L	X	L	Q_{0+1}	Deselect or STOP
n+4	X	X	H	X	L	X	L	Q1	NOOP
n+5	A2	H	L	L	L	X	X	Z	Load read
n+6	X	X	H	X	L	X	X	Z	Burst read
n+7	X	X	L	H	L	X	L	Q2	Deselect or STOP
n+8	A3	L	L	L	L	L	L	Q_{2+1}	Load write
n+9	X	X	H	X	L	L	X	Z	Burst write
n+10	A4	L	L	L	L	L	X	D3	Load write
n+11	X	X	L	H	L	X	X	D_{3+1}	Deselect or STOP
n+12	X	X	H	X	L	X	X	D4	NOOP
n+13	A5	L	L	L	L	L	X	Z	Load write
n+14	A6	H	L	L	L	X	X	Z	Load read
n+15	A7	L	L	L	L	L	X	D5	Load write
n+16	X	X	H	X	L	L	L	Q6	Burst write
n+17	A8	H	L	L	L	X	X	D7	Load read
n+18	X	X	H	X	L	X	X	D_{7+1}	Burst read
n+19	A9	L	L	L	L	L	L	Q8	Load write

3821 tbl 11

NOTES:
1. $\overline{CE}$ = L is defined as $\overline{CE}_1$ = L, $\overline{CE}_2$ = L and CE_2 = H. CE = H is defined as $\overline{CE}_1$ = H, $\overline{CE}_2$ = H or CE_2 = L.
2. H = High; L = Low; X = Don't Care; Z = High Impedance.

Read Operation(1)

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}$(2)	$\overline{CEN}$	$\overline{BW}$x	$\overline{OE}$	I/O	Comments
n	A0	H	L	L	L	X	X	X	Address and Control meet setup
n+1	X	X	X	X	L	X	X	X	Clock Setup Valid
n+2	X	X	X	X	X	X	L	Q0	Contents of Address A0 Read Out

3821 tbl 12

NOTES:
1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\overline{CE}$ = L is defined as $\overline{CE}_1$ = L, $\overline{CE}_2$ = L and CE_2 = H. $\overline{CE}$ = H is defined as $\overline{CE}_1$ = H, $\overline{CE}_2$ = H or CE_2 = L.

Burst Read Operation(1)

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}$(2)	$\overline{CEN}$	$\overline{BW}$x	$\overline{OE}$	I/O	Comments
n	A0	H	L	L	L	X	X	X	Address and Control meet setup
n+1	X	X	H	X	L	X	X	X	Clock Setup Valid, Advance Counter
n+2	X	X	H	X	L	X	L	Q0	Address A0 Read Out, Inc. Count
n+3	X	X	H	X	L	X	L	Q_{0+1}	Address A_{0+1} Read Out, Inc. Count
n+4	X	X	H	X	L	X	L	Q_{0+2}	Address A_{0+2} Read Out, Inc. Count
n+5	A1	H	L	L	L	X	L	Q_{0+3}	Address A_{0+3} Read Out, Load A1
n+6	X	X	H	X	L	X	L	Q0	Address A0 Read Out, Inc. Count
n+7	X	X	H	X	L	X	L	Q1	Address A1 Read Out, Inc. Count
n+8	A2	H	L	L	L	X	L	Q_{1+1}	Address A_{1+1} Read Out, Load A2

3821 tbl 13

NOTES:
1. H = High; L = Low; X = Don't Care; Z = High Impedance..
2. $\overline{CE}$ = L is defined as $\overline{CE}_1$ = L, $\overline{CE}_2$ = L and CE2 = H. CE = H is defined as $\overline{CE}_1$ = H, $\overline{CE}_2$ = H or CE2 = L.

Write Operation(1)

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}$(2)	$\overline{CEN}$	$\overline{BW}$x	$\overline{OE}$	I/O	Comments
n	A0	L	L	L	L	L	X	X	Address and Control meet setup
n+1	X	X	X	X	L	X	X	X	Clock Setup Valid
n+2	X	X	X	X	L	X	X	D0	Write to Address A0

3821 tbl 14

NOTES:
1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\overline{CE}$ = L is defined as $\overline{CE}_1$ = L, $\overline{CE}_2$ = L and CE2 = H. $\overline{CE}$ = H is defined as $\overline{CE}_1$ = H, $\overline{CE}_2$ = H or CE_2 = L.

Burst Write Operation(1)

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}$(2)	$\overline{CEN}$	$\overline{BW}$x	$\overline{OE}$	I/O	Comments
n	A0	L	L	L	L	L	X	X	Address and Control meet setup
n+1	X	X	H	X	L	L	X	X	Clock Setup Valid, Inc. Count
n+2	X	X	H	X	L	L	X	D0	Address A0 Write, Inc. Count
n+3	X	X	H	X	L	L	X	D_{0+1}	Address A_{0+1} Write, Inc. Count
n+4	X	X	H	X	L	L	X	D_{0+2}	Address A_{0+2} Write, Inc. Count
n+5	A1	L	L	L	L	L	X	D_{0+3}	Address A_{0+3} Write, Load A1
n+6	X	X	H	X	L	L	X	D0	Address A0 Write, Inc. Count
n+7	X	X	H	X	L	L	X	D1	Address A1 Write, Inc. Count
n+8	A2	L	L	L	L	L	X	D_{1+1}	Address A_{1+1} Write, Load A2

3821 tbl 15

NOTES:
1. H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance.
2. $\overline{CE}$ = L is defined as $\overline{CE}_1$ = L, $\overline{CE}_2$ = L and CE2 = H. $\overline{CE}$ = H is defined as $\overline{CE}_1$ = H, $\overline{CE}_2$ = H or CE_2 = L.

Read Operation With Clock Enable Used(1)

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}$(2)	$\overline{CEN}$	$\overline{BW}$x	$\overline{OE}$	I/O	Comments
n	A0	H	L	L	L	X	X	X	Address and Control meet setup
n+1	X	X	X	X	H	X	X	X	Clock n+1 Ignored
n+2	A1	H	L	L	L	X	X	X	Clock Valid
n+3	X	X	X	X	H	X	L	Q0	Clock Ignored. Data Q0 is on the bus
n+4	X	X	X	X	H	X	L	Q0	Clock Ignored. Data Q0 is on the bus
n+5	A2	H	L	L	L	X	L	Q0	Address A0 Read out (but trans.)
n+6	A3	H	L	L	L	X	L	Q1	Address A1 Read out (bus trans.)
n+7	A4	H	L	L	L	X	L	Q2	Address A2 Read out (bus trans.)

3821 tbl 16

NOTES:
1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\overline{CE}$ = L is defined as $\overline{CE}_1$ = L, $\overline{CE}_2$ = L and CE2 = H. $\overline{CE}$ = H is defined as $\overline{CE}_1$ = H, $\overline{CE}_2$ = H or CE2 = L.

Write Operation with Clock Enable Used(1)

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}$(2)	$\overline{CEN}$	$\overline{BW}$x	$\overline{OE}$	I/O	Comments
n	A0	L	L	L	L	L	X	X	Address and Control meet setup
n+1	X	X	X	X	H	X	X	X	Clock n+1 Ignored
n+2	A1	L	L	L	L	L	X	X	Clock Valid
n+3	X	X	X	X	H	X	X	X	Clock Ignored
n+4	X	X	X	X	H	X	X	X	Clock Ignored
n+5	A2	L	L	L	L	L	X	D0	Write data D0
n+6	A3	L	L	L	L	L	X	D1	Write data D1
n+7	A4	L	L	L	L	L	X	D2	Write data D2

3821 tbl 17

NOTES:
1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\overline{CE}$ = L is defined as $\overline{CE}_1$ = L, $\overline{CE}_2$ = L and CE2 = H. $\overline{CE}$ = H is defined as $\overline{CE}_1$ = H, $\overline{CE}_2$ = H or CE2 = L.

Read Operation With Chip Enable Used(1)

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}$(1)	$\overline{CEN}$	$\overline{BW}$x	$\overline{OE}$	I/O	Comments
n	X	X	L	H	L	X	X	?	Deselected
n+1	X	X	L	H	L	X	X	?	Deselected
n+2	A0	H	L	L	L	X	X	Z	Address and Control meet setup
n+3	X	X	L	H	L	X	X	Z	Deselected or STOP
n+4	A1	H	L	L	L	X	L	Q0	Address A0 read out. Load A1
n+5	X	X	L	H	L	X	X	Z	Deselected or STOP
n+6	X	X	L	H	L	X	L	Q1	Address A1 Read out. Deselected
n+7	A2	H	L	L	L	X	X	Z	Address and Control meet setup
n+8	X	X	L	H	L	X	X	Z	Deselected or STOP
n+9	X	X	L	H	L	X	L	Q2	Address A2 read out. Deselected

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NOTES:
1. H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance.
2. $\overline{CE}$ = L is defined as $\overline{CE}_1$ = L, $\overline{CE}_2$ = L and CE_2 = H. $\overline{CE}$ = H is defined as $\overline{CE}_1$ = H, $\overline{CE}_2$ = H or CE_2 = L.
3. Device Outputs are ensured to be in High-Z after the first rising edge of clock upon power-up.

Write Operation With Chip Enable Used(1)

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}$(1)	$\overline{CEN}$	$\overline{BW}$x	$\overline{OE}$	I/O	Comments
n	X	X	L	H	L	X	X	?	Deselected
n+1	X	X	L	H	L	X	X	?	Deselected
n+2	A0	L	L	L	L	L	X	Z	Address and Control meet setup
n+3	X	X	L	H	L	X	X	Z	Deselected or STOP
n+4	A1	L	L	L	L	L	X	D0	Address D0 Write In. Load A1
n+5	X	X	L	H	L	X	X	Z	Deselected or STOP
n+6	X	X	L	H	L	X	X	D1	Address D1 Write In. Deselected
n+7	A2	L	L	L	L	L	X	Z	Address and Control meet setup
n+8	X	X	L	H	L	X	X	Z	Deselected or STOP
n+9	X	X	L	H	L	X	X	D2	Address D2 Write In. Deselected

3821 tbl 19

NOTES:
1. H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance.
2. $\overline{CE}$ = L is defined as $\overline{CE}_1$ = L, $\overline{CE}_2$ = L and CE_2 = H. $\overline{CE}$ = H is defined as $\overline{CE}_1$ = H, $\overline{CE}_2$ = H or CE_2 = L.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{DD} = 3.3V +/-5%)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{DD} = Max., V_{IN} = 0V to V_{DD}	—	5	µA
$\|I_{LI}\|$	$\overline{LBO}$ Input Leakage Current[1]	V_{DD} = Max., V_{IN} = 0V to V_{DD}	—	30	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE} \geq V_{IH}$ or $\overline{OE} \geq V_{IH}$, V_{OUT} = 0V toV_{DD}, V_{DD} = Max.	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 5mA, V_{DD} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -5mA, V_{DD} = Min.	2.4	—	V

3821 tbl 20

NOTE:
1. The $\overline{LBO}$ pin will be internally pulled to V_{DD} if it is not actively driven in the application.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range[1] (V_{DD} = 3.3V +/-5%, V_{HD} = V_{DD}–0.2V, V_{LD} = 0.2V)

Symbol	Parameter	Test Conditions	S133		S100		Unit
			Com'l	Ind	Com'l	Ind	
I_{DD}	Operating Power Supply Current	Device Selected, Outputs Open, ADV/LD = X, V_{DD} = Max., $V_{IN} \geq V_{IH}$ or $\leq V_{IL}$, f = f_{MAX}[2]	300	310	250	260	mA
I_{SB1}	CMOS Standby Power Supply Current	Device Deselected, Outputs Open, V_{DD} = Max., $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$, f = 0[2]	40	45	40	45	mA
I_{SB2}	Clock Running Power Supply Current	Device Deselected, Outputs Open, V_{DD} = Max., $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$, f = f_{MAX}[2]	110	120	100	110	mA
I_{SB3}	Idle Power Supply Current	Device Selected, Outputs Open, CEN $\geq V_{IH}$ V_{DD} = Max., $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$, f = f_{MAX}[2]	40	45	40	45	mA

3821 tbl 21

NOTES:
1. All values are maximum guaranteed values.
2. At f = f_{MAX}, inputs are cycling at the maximum frequency of read cycles of 1/t_{CYC}; f=0 means no input lines are changing.

AC Test Loads

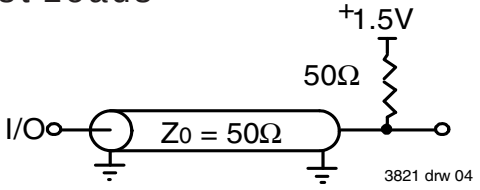

Figure 1. AC Test Load

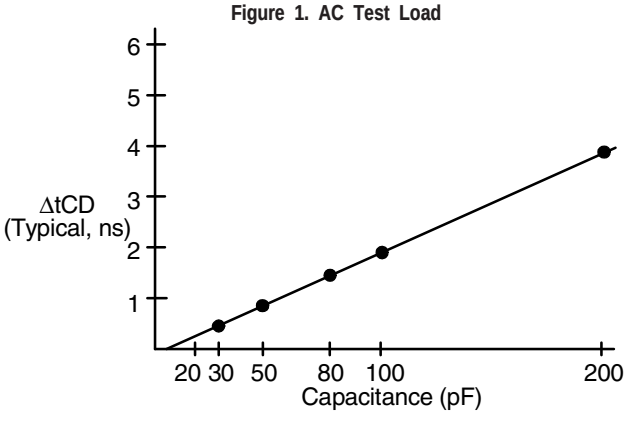

Figure 2. Lumped Capacitive Load, Typical Derating

AC Test Conditions

Input Pulse Levels	0 to 3V
Input Rise/Fall Times	2ns
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
AC Test Load	See Figures 1

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AC Electrical Characteristics

(VDD = 3.3V +/-5%, Commercial and Industrial Temperature Ranges)

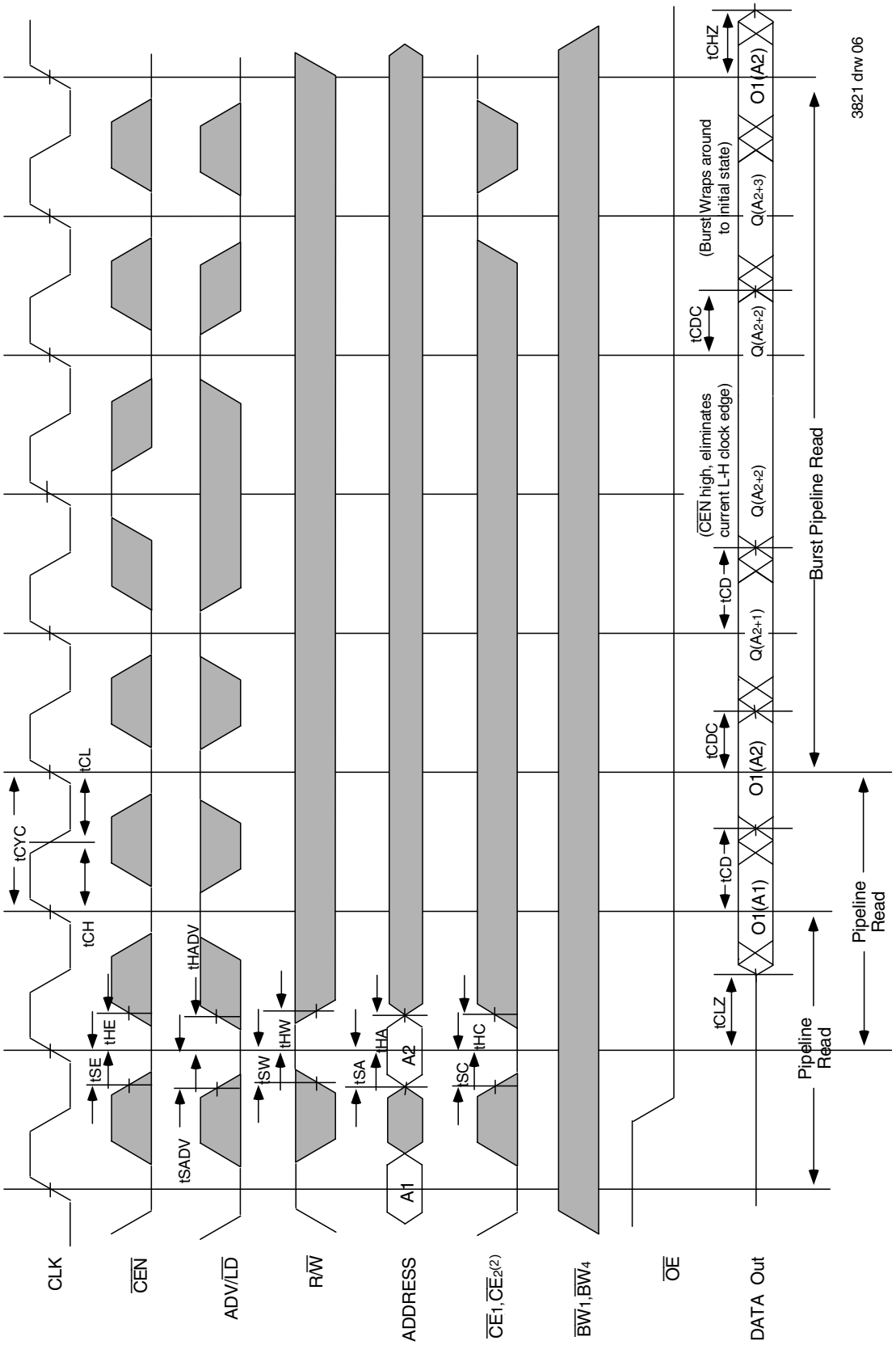
Symbol	Parameter	71V546S133		71V546S100		Unit
		Min.	Max.	Min.	Max.	
Clock Parameters						
t_{CYC}	Clock Cycle Time	7.5	—	10	—	ns
t_F(1)	Clock Frequency	—	133	—	100	MHz
t_{CH}(2)	Clock High Pulse Width	2.5	—	3.5	—	ns
t_{CL}(2)	Clock Low Pulse Width	2.5	—	3.6	—	ns
Output Parameters						
t_{CD}	Clock High to Valid Data	—	4.2	—	5	ns
t_{CDC}	Clock High to Data Change	1.5	—	1.5	—	ns
t_{CLZ}(3,4,5)	Clock High to Output Active	1.5	—	1.5	—	ns
t_{CHZ}(3,4,5)	Clock High to Data High-Z	1.5	3.5	1.5	3.5	ns
t_{OE}	Output Enable Access Time	—	4.2	—	5	ns
t_{OLZ}(3,4)	Output Enable Low to Data Active	0	—	0	—	ns
t_{OHZ}(3,4)	Output Enable High to Data High-Z	—	3.5	—	3.5	ns
Setup Times						
t_{SE}	Clock Enable Setup Time	2.0	—	2.2	—	ns
t_{SA}	Address Setup Time	2.0	—	2.2	—	ns
t_{SD}	Data in Setup Time	1.7	—	2.0	—	ns
t_{SW}	Read/Write (R/W) Setup Time	2.0	—	2.2	—	ns
t_{SADV}	Advance/Load (ADV/LD) Setup Time	2.0	—	2.2	—	ns
t_{SC}	Chip Enable/Select Setup Time	2.0	—	2.2	—	ns
t_{SB}	Byte Write Enable (BWx) Setup Time	2.0	—	2.2	—	ns
Hold Times						
t_{HE}	Clock Enable Hold Time	0.5	—	0.5	—	ns
t_{HA}	Address Hold Time	0.5	—	0.5	—	ns
t_{HD}	Data in Hold Time	0.5	—	0.5	—	ns
t_{HW}	Read/Write (R/W) Hold Time	0.5	—	0.5	—	ns
t_{HADV}	Advance/Load (ADV/LD) Hold Time	0.5	—	0.5	—	ns
t_{HC}	Chip Enable/Select Hold Time	0.5	—	0.5	—	ns
t_{HB}	Byte Write Enable (BWx) Hold Time	0.5	—	0.5	—	ns

3821 tbl 23

NOTES:

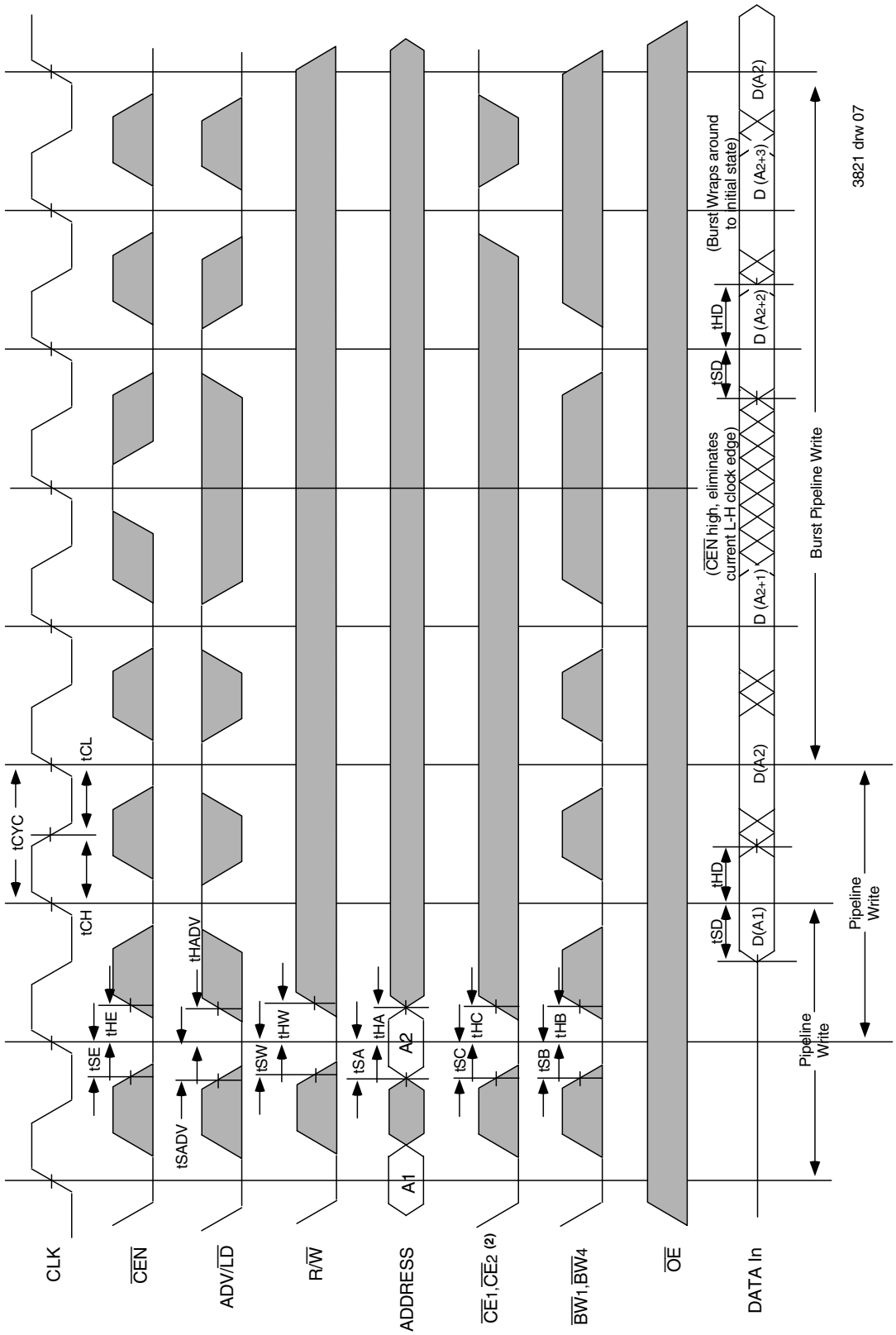
1. $t_F = 1/t_{CYC}$.
2. Measured as HIGH above 2.0V and LOW below 0.8V.
3. Transition is measured ±200mV from steady-state.
4. These parameters are guaranteed with the AC load (Figure 1) by device characterization. They are not production tested.
5. To avoid bus contention, the output buffers are designed such that t_{CHZ} (device turn-off) is about 2 ns faster than t_{CLZ} (device turn-on) at a given temperature and voltage. The specs as shown do not imply bus contention because t_{CLZ} is a Min. parameter that is worse case at totally different test conditions (0 deg. C, 3.465V) than t_{CHZ}, which is a Max. parameter (worse case at 70 deg. C, 3.135V).

Timing Waveform of Read Cycle(1,2,3,4)



NOTES:
1. Q (A1) represents the first output from the external address A1. Q (A2) represents the first output from the external address A2; Q ($A2+1$) represents the next output data in the burst sequence of the base address A2, etc. where address bits A0 and A1 are advancing for the four word burst in the sequence defined by the state of the $\overline{LBO}$ input.
2. CE_2 timing transitions are identical but inverted to the $\overline{CE}_1$ and $\overline{CE}_2$ signals. For example, when $\overline{CE}_1$ and $\overline{CE}_2$ are LOW on this waveform, CE_2 is HIGH.
3. Burst ends when new address and control are loaded into the SRAM by sampling ADV/$\overline{LD}$ LOW.
4. R/$\overline{W}$ is don't care when the SRAM is bursting (ADV/$\overline{LD}$ sampled HIGH). The nature of the burst access (Read or Write) is fixed by the state of the R/$\overline{W}$ signal when new address and control are loaded into the SRAM.

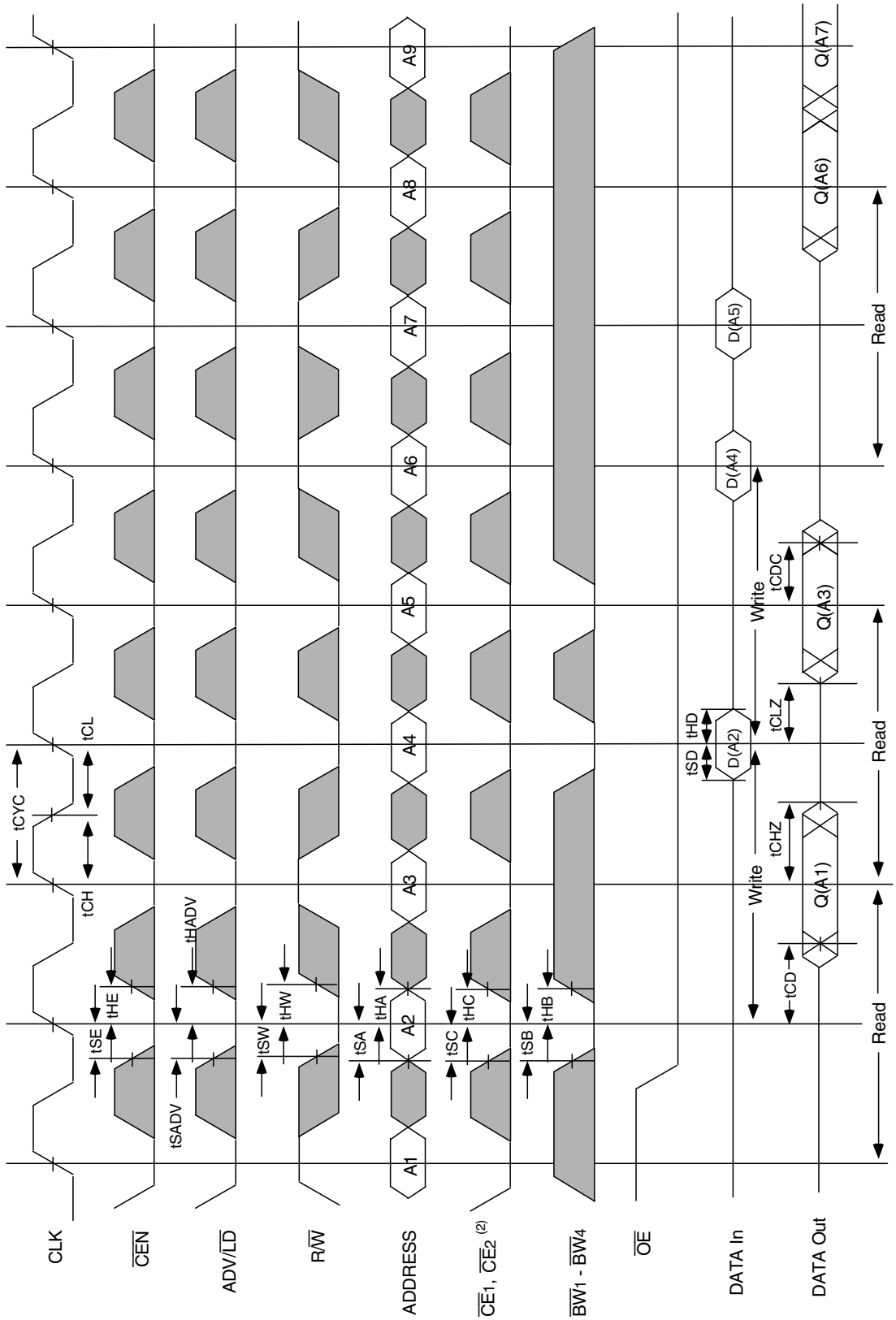
Timing Waveform of Write Cycles(1,2,3,4,5)



NOTES:

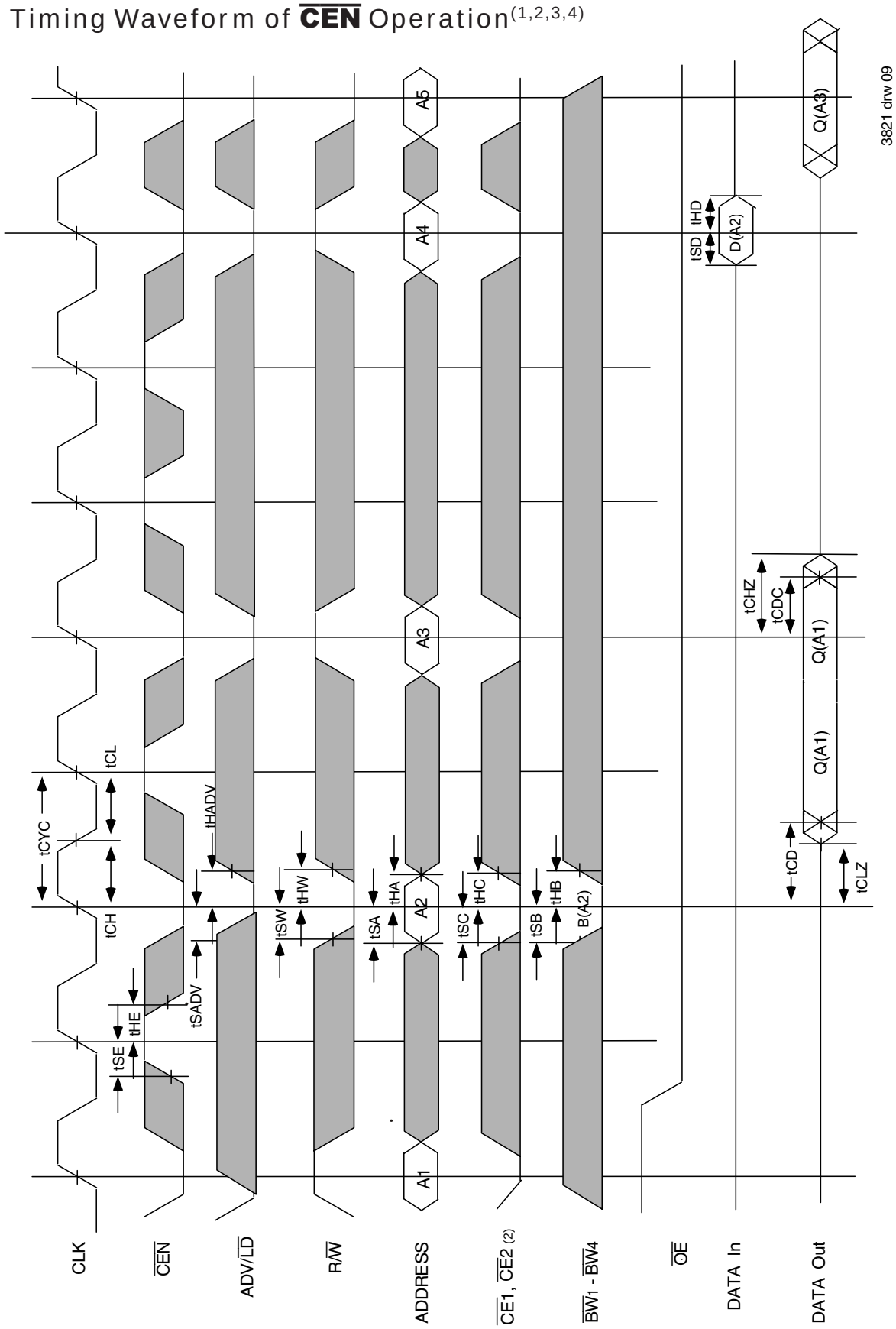
1. D (A1) represents the first input to the external address A1. D (A2) represents the first input to the external address A2; D (A2+1) represents the next input data in the burst sequence of the base address A2, etc. where address bits A0 and A1 are advancing for the four word burst in the sequence defined by the state of the $\overline{LBO}$ input.
2. CE_2 timing transitions are identical but inverted to the $\overline{CE}_1$ and $\overline{CE}_2$ signals. For example, when $\overline{CE}_1$ and $\overline{CE}_2$ are LOW on this waveform, CE_2 is HIGH.
3. Burst ends when new address and control are loaded into the SRAM by sampling ADV/$\overline{LD}$ LOW.
4. R/$\overline{W}$ is don't care when the SRAM is bursting (ADV/$\overline{LD}$ sampled HIGH). The nature of the burst access (Read or Write) is fixed by the state of the R/$\overline{W}$ signal when new address and control are loaded into the SRAM.
5. Individual Byte Write signals ($\overline{BWx}$) must be valid on all write and burst-write cycles. A write cycle is initiated when R/$\overline{W}$ signal is sampled LOW. The byte write information comes in two cycles before the actual data is presented to the SRAM.

Timing Waveform of Combined Read and Write Cycles(1,2,3)



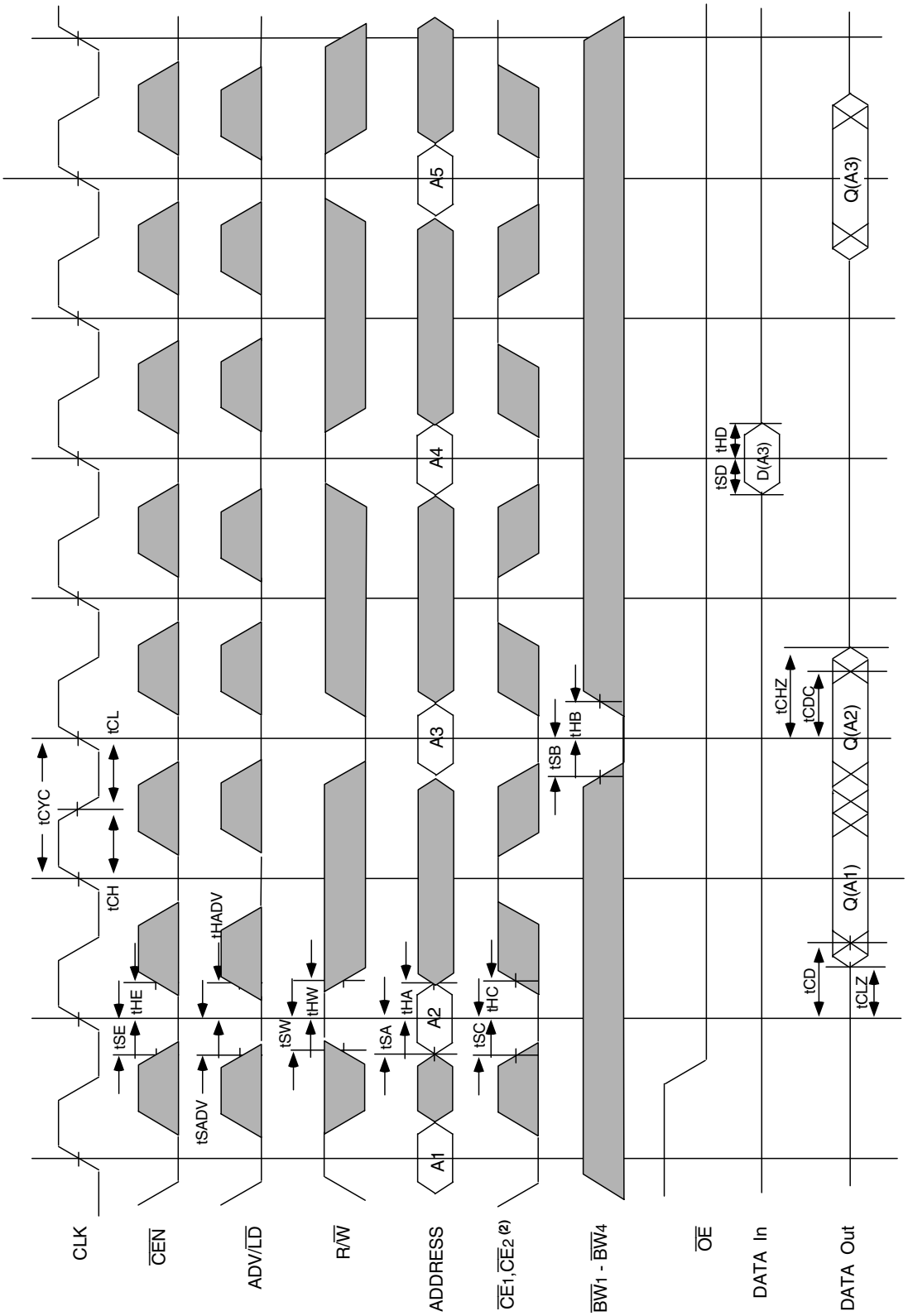
NOTES:
1. Q (A1) represents the first output from the external address A1. D (A2) represents the input data to the SRAM corresponding to address A2.
2. $\overline{CE}_2$ timing transitions are identical but inverted to the $\overline{CE}_1$ and $\overline{CE}_2$ signals. For example, when $\overline{CE}_1$ and $\overline{CE}_2$ are LOW on this waveform, CE_2 is HIGH.
3. Individual Byte Write signals ($\overline{BW}x$) must be valid on all write and burst-write cycles. A write cycle is initiated when $R/\overline{W}$ signal is sampled LOW. The byte write information comes in two cycles before the actual data is presented to the SRAM.

Timing Waveform of $\overline{CEN}$ Operation(1,2,3,4)



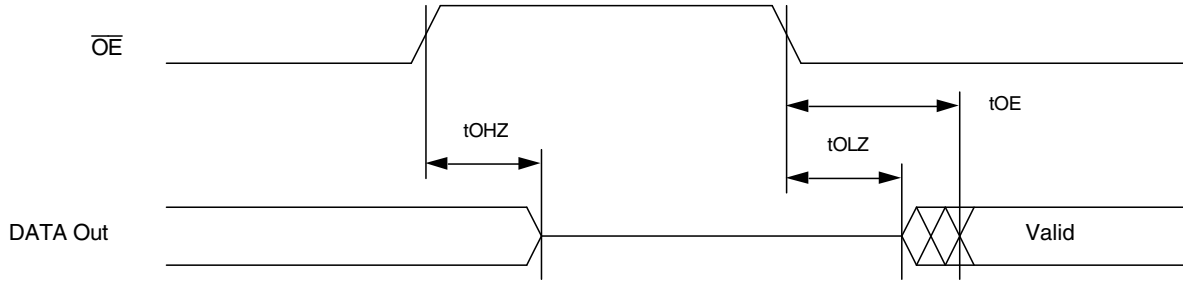
NOTES:
1. Q (A1) represents the first output from the external address A1. D (A2) represents the input data to the SRAM corresponding to address A2.
2. $\overline{CE}_2$ timing transitions are identical but inverted to the $\overline{CE}_1$ and $\overline{CE}_2$ signals. For example, when $\overline{CE}_1$ and $\overline{CE}_2$ are LOW on this waveform, CE_2 is HIGH..
3. $\overline{CEN}$ when sampled high on the rising edge of clock will block that L-H transition of the clock from propagating into the SRAM. The part will behave as if the L-H clock transition did not occur. All internal registers in the SRAM will retain their previous state.
4. Individual Byte Write signals ($\overline{BW}x$) must be valid on all write and burst-write cycles. A write cycle is initiated when R/$\overline{W}$ signal is sampled LOW. The byte write information comes in two cycles before the actual data is presented to the SRAM.

Timing Waveform of $\overline{CS}$ Operation(1,2,3,4)



NOTES:
1. Q (A1) represents the first output from the external address A1. D (A3) represents the input data to the SRAM corresponding to address A3 etc.
2. CE_2 timing transitions are identical but inverted to the $\overline{CE}_1$ and $\overline{CE}_2$ signals. For example, when $\overline{CE}_1$ and $\overline{CE}_2$ are LOW on this waveform, CE_2 is HIGH.
3. When either one of the Chip enables ($\overline{CE}_1$, CE_2, $\overline{CE}_2$) is sampled inactive at the rising clock edge, a deselect cycle is initiated. The data-bus tri-states two cycles after the initiation of the deselect cycle. This allows for any pending data transfers (reads or writes) to be completed.
4. Individual Byte Write signals ($\overline{BW}x$) must be valid on all write and burst-write cycles. A write cycle is initiated when $R/\overline{W}$ signal is sampled LOW. The byte write information comes in two cycles before the actual data is presented to the SRAM.

Timing Waveform of $\overline{OE}$ Operation(1)



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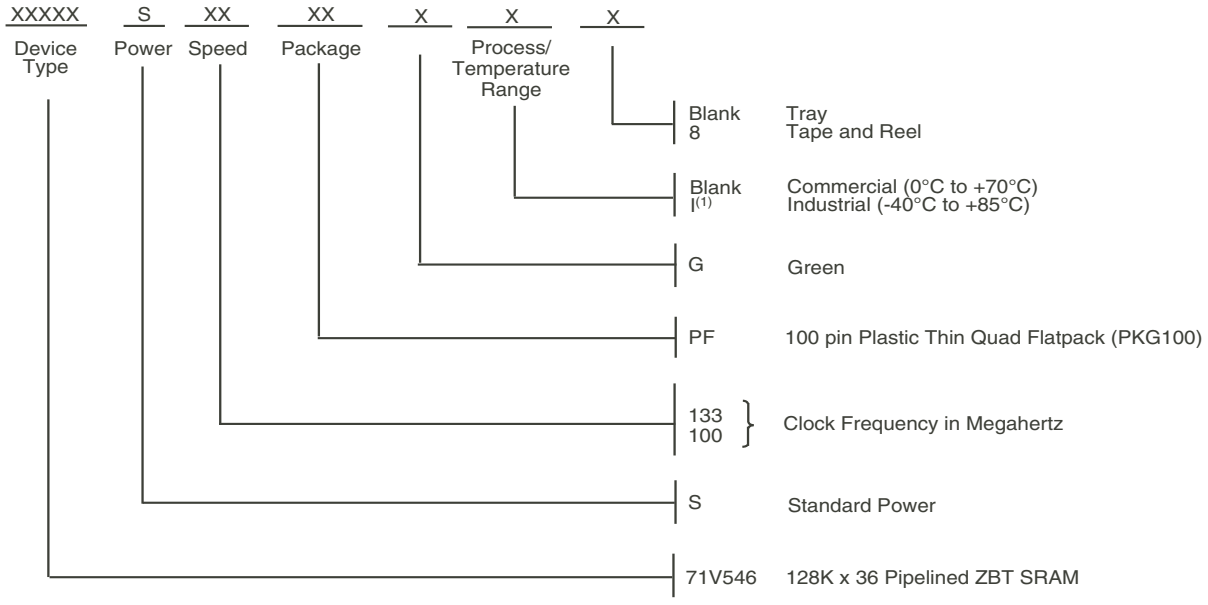
NOTE:
1. A read operation is assumed to be in progress.

Ordering Information



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NOTES:
1. Contact your local sales office for Industrial temp range for other speeds, packages and powers.

Orderable Part Information

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
100	71V546S100PFG	PKG100	TQFP	C
	71V546S100PFG8	PKG100	TQFP	C
	71V546S100PFGI	PKG100	TQFP	I
	71V546S100PFGI8	PKG100	TQFP	I
133	71V546S133PFG	PKG100	TQFP	C
	71V546S133PFG8	PKG100	TQFP	C
	71V546S133PFGI	PKG100	TQFP	I
	71V546S133PFGI8	PKG100	TQFP	I

3821t25.tbl

Datasheet Document History

6/15/99		Updated to new format
9/13/99	Pg. 12	Corrected I_{SB3} conditions
	Pg. 20	Added Datasheet Document History
12/31/99	Pg. 3, 12, 13, 19	Added Industrial Temperature range offerings
11/22/05	Pg. 3,4	Moved Operating temperature & DC operating tables from page 3 to new page 5. Moved Absolute rating & Capacitance tables from page 4 to new page 5. Add clarification note to Recommended Operating Temperature and Absolute Max Ratings tables.
	Pg. 20	Updated order information with "Restricted hazardous substance device"
02/23/07	Pg. 20	Added X generation die step to data sheet ordering information
10/18/08	Pg. 20	Removed "IDT" for orderable part number
08/18/17	Pg. 1	Removed all information for 71V546XS In Features: Added text: "Green parts available, see Ordering Information" Moved the FBD from page 3 to page 1 in accordance with our standard datasheet format
	Pg. 2	Removed the IDT in reference to fabrication
	Pg. 4	Updated the TQFP pin configuration by rotating package pin labels and pin numbers 90 degrees counter clockwise added IDT logo & in accordance with the packaging code, changed the PK100 designation to PKG100 , changed the text to be in alignment with new diagram marking specs Removed footnote 2 and the 2 annotation for NC pins 83 & 84 in the TQFP pin configuration
	Pg. 13	Removed 117 MHz speed grade offering from the DC Electrical table
	Pg. 14	Removed 117 MHz speed grade offering from the AC Electrical table
	Pg. 20	Removed Tube indicator, updated "Restricted hazardous substance" device to "Green" Updated package code in Ordering Information from PK100 to PKG100 and removed the 117 MHz speed grade offering Added Orderable Part Information Removed the 100 Thin Quad Flatpack Packaging Table

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