QUADRACLOCK QUADRATURE DELAY BUFFER ICS672-01/02

Description

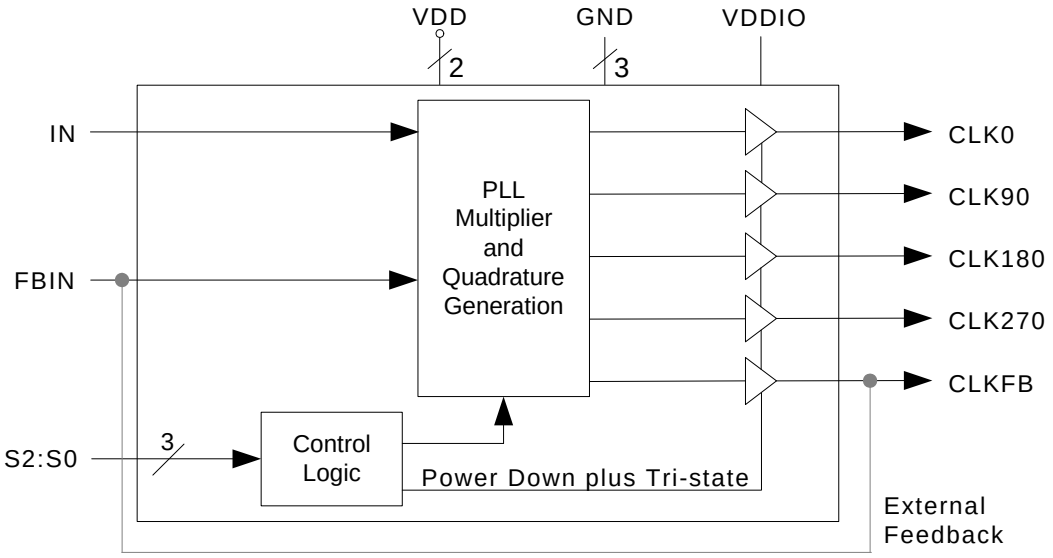
The ICS672-01/02 are zero delay buffers that generate four output clocks whose phases are spaced at 90° intervals. Based on IDT's proprietary low jitter Phase-Locked Loop (PLL) techniques, each device provides five low-skew outputs, with clock rates up to 84 MHz for the ICS672-01 and up to 135 MHz for the ICS672-02. By providing outputs delayed one quarter clock cycle, the device is useful for systems requiring early or late clocks. The ICS672-01/02 include multiplier selections of x0.5, x1, x2, x3, x4, x5, or x6. They also offer a mode to power-down all internal circuitry and tri-state the outputs. In normal operation, output clock FBCLK is tied to the FBIN pin.

IDT manufactures the largest variety of clock generators and buffers, and is the largest clock supplier in the world.

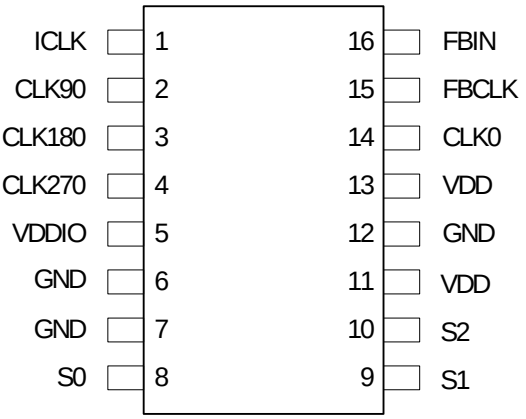
Features

- Packaged in 16-pin SOIC
- Pb (lead) free package, RoHS compliant
- Input clock range from 5 MHz to 150 MHz (depends on multiplier)
- Clock outputs from up to 84 MHz (ICS672-01) and up to 135 MHz (ICS672-02)
- Zero input-output delay
- Integrated x0.5, x1, x2, x3, x4, x5, or x6 selections
- Four accurate (<250 ps) outputs with 0°, 90°, 180°, and 270° phase shift from ICLK, and one FBCLK (0°)
- Separate supply for output clocks from 2.5 V to 5 V
- Full CMOS outputs (TTL compatible)
- Tri-state mode for board-level testing
- Includes Power-down for power savings
- Advanced, low power, sub-micron CMOS process
- 3.3 V to 5 V operating voltage
- Industrial temperature version available

Block Diagram



Pin Assignment



Output Clock Mode Select Table

S2	S1	S0	Output Clocks
0	0	0	Power-down + tri-state
0	0	1	x1
0	1	0	x2
0	1	1	x3
1	0	0	x4
1	0	1	x5
1	1	0	x6
1	1	1	x0.5

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	ICLK	Input	Clock input.
2	CLK90	Output	Clock output (90° delayed from CLK0).
3	CLK180	Output	Clock output (180° delayed from CLK0).
4	CLK270	Output	Clock output (270° delayed from CLK0).
5	VDDIO	Power	Supply voltage for input and output clocks. Must not exceed VDD.
6, 7, 12	GND	Power	Connect to ground.
8	S0	Input	Select input 0. See table above.
9	S1	Input	Select input 1. See table above.
10	S2	Input	Select input 2. See table above.
11, 13	VDD	Power	Connect to 3.3 V or 5.0 V.
14	CLK0	Output	Clock output phase aligned to ICLK.
15	FBCLK	Output	Feedback clock output (0° phase shift from CLK0).
16	FBIN	Input	Feedback clock input. in normal operation, connect to FBCLK.

External Components

The ICS672-01/02 requires a minimum number of external components for proper operation. Decoupling capacitors of 0.01µF should be connected between VDD and GND on pins 11 and 12, and VDD and GND on pins 13 and 12, and VDDIO and GND on pins 5 and 6, as close to the device as possible. A series termination resistor of 33Ω may be used close to each clock output pin to reduce reflections.

Operation and Applications

The ICS672-01/02 each provide a total of five output clocks with multiple phase shifts relative to the input clock (ICLK). Phase shifts of 0° (CLK0), 90° (CLK90), 180° (CLK180), and 270° (CLK270) are provided, plus one feedback clock (FBCLK). All output clocks will be a multiple of the input clock, as determined by the table on page 2. Refer to the illustrations in Figure 1 and Figure 2.

FBCLK is connected to the feedback input (FBIN) to provide a zero delay through the ICS672-01/02. FBCLK has a 0° phase shift from ICLK.

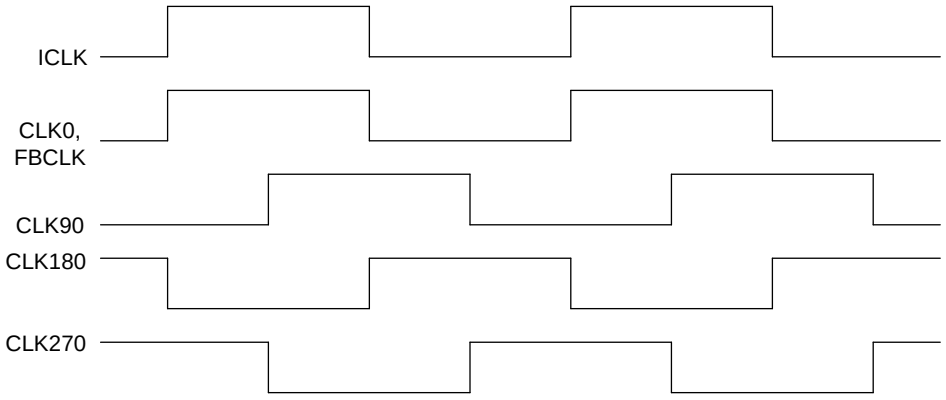


Figure 1. Phase alignment of input and output clocks (x1 multiplier)

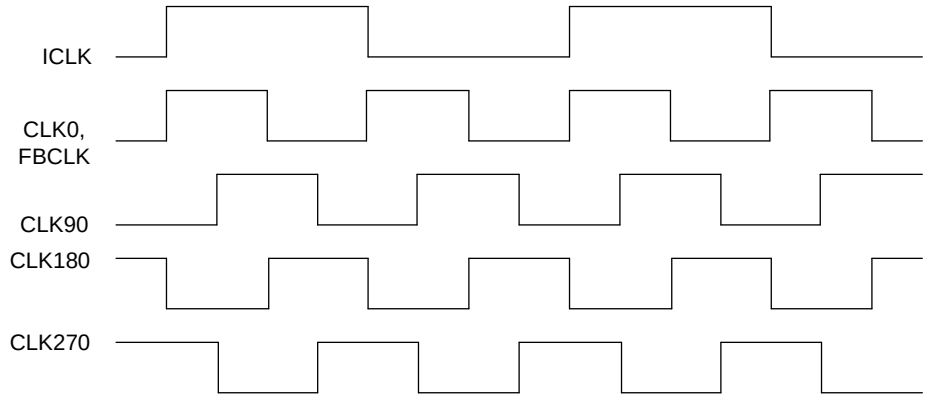


Figure 2. Phase alignment of input and output clocks (x2 multiplier)

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS672-01/02. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	-0.5 V to 7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Electrostatic Discharge (MIL-STD-883)	2000 V
Ambient Operating Temperature (commercial)	0 to +70° C
Ambient Operating Temperature (industrial, -02 only)	-40 to +85° C
Storage Temperature	-65 to +150° C
Junction Temperature	150° C
Soldering Temperature	260° C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0		+70	° C
Power Supply Voltage (measured in respect to GND)	+3.13		+5.5	V

DC Electrical Characteristics

VDD = VDDIO = 3.3 V, Ambient temperature 0 to +70° C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.13		5.50	V
Operating Voltage	VDDIO		2.375		VDD	V
Input High Voltage	V_{IH}	ICLK only	VDDIO/2+0.5			V
Input Low Voltage	V_{IL}	ICLK only			VDDIO/2-0.5	V
Input High Voltage	V_{IH}		2			V
Input Low Voltage	V_{IL}				0.8	V
Output High Voltage	V_{OH}	I_{OH} = -12 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 12 mA			0.4	V
Output High Voltage, CMOS level	V_{OH}	I_{OH} = -8 mA	VDDIO-0.4			V
Operating Supply Current	IDD	No Load, S1=1, S0=0, S2=0, Note 1		11		mA

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Supply Current	IDD	No Load, S1=1, S0=0, S2=0, Notes 2, 6		22		mA
		No Load, S1=1, S0=0, S2=0, Notes 2, 7		66		mA
Short Circuit Current	I_{OS}	Each output		±50		mA
Input Capacitance	C_{IN}	OE, select pins		7		pF

AC Electrical Characteristics

VDD = VDDIO = 3.3 V, Ambient Temperature 0 to +70° C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Clock Frequency	f_{IN}	Note 3	5		150	MHz
Output Clock Frequency		ICS672-01	15		84	MHz
Output Clock Frequency		ICS672-02	15		135	MHz
Output Rise Time	t_{OR}	0.8 to 2.0 V, no load, C_L = 15 pF			1.0	ns
Output Fall Time	t_{OF}	2.0 to 0.8 V, no load, C_L = 15 pF			1.0	ns
Output Clock Duty Cycle, VDDIO = 3.3 V	t_{DC}	At VDDIO/2	45	50	55	%
Phased Outputs Accuracy		Rising edges at VDDIO/2, Note 4	-250		250	ps
Input to Output Skew		ICLK to CLK0, Note 5	-300		300	ps
Maximum Absolute Jitter				75		ps
Cycle to Cycle Jitter		15 pF loads		150		ps

Note 1: With ICLK = 20 MHz, FBCLK to FBIN, all outputs at 40 MHz.

Note 2: With ICLK = 66.5 MHz, FBCLK to FBIN, all outputs at 133 MHz.

Note 3: Value depends on multiplier. Must also meet output clock frequency.

Note 4: With CLK0CLK270 equally loaded, and output frequency > 60 MHz.

Note 5: Rising edge of ICLK compared with rising edge of CLk0, with FBCLK connected to FBIN, 15 pF load on CLK0, and CLK0 > 60 MHz.

Note 6: Commercial grade.

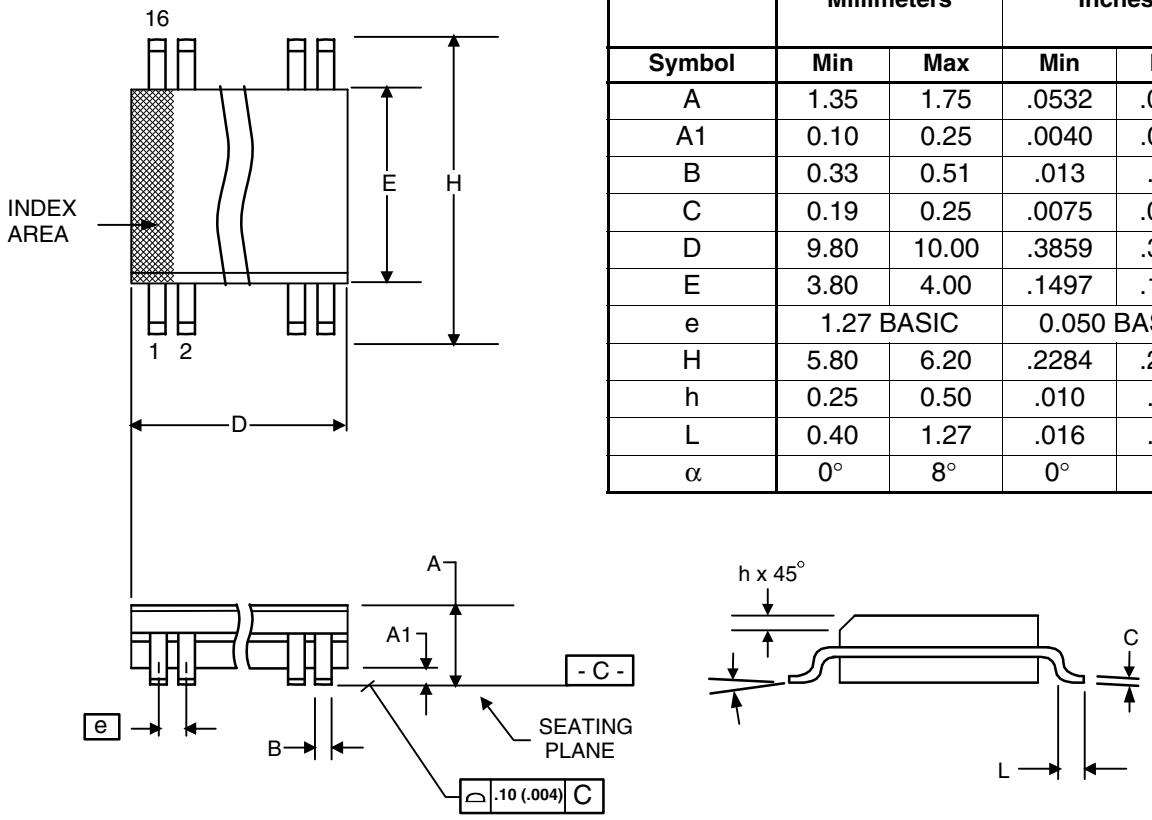
Note 7: Industrial grade.

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		120		° C/W
	θ_{JA}	1 m/s air flow		115		° C/W
	θ_{JA}	3 m/s air flow		105		° C/W
Thermal Resistance Junction to Case	θ_{JC}			58		° C/W

Package Outline and Package Dimensions (16-pin SOIC, 150 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	**Min**	**Max**	**Min**	**Max**
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.013	.020
C	0.19	0.25	.0075	.0098
D	9.80	10.00	.3859	.3937
E	3.80	4.00	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
672M-01LF	ICS672M-01LF	Tubes	16-pin SOIC	0 to +70° C
672M-01LFT	ICS672M-01LF	Tape and Reel	16-pin SOIC	0 to +70° C
672M-02LF	ICS672M-02LF	Tubes	16-pin SOIC	0 to +70° C
672M-02LFT	ICS672M-02LF	Tape and Reel	16-pin SOIC	0 to +70° C
672M-02ILF	672M-02ILF	Tubes	16-pin SOIC	-40 to +85° C
672M-02ILFT	672M-02ILF	Tape and Reel	16-pin SOIC	-40 to +85° C

"LF" denotes Pb (lead) free package.

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