

RJE0620JPD

–60V, –10A, P Channel Thermal FET
Power Switching

R07DS1235EJ0200
Rev.2.00
Mar 02, 2020

Description

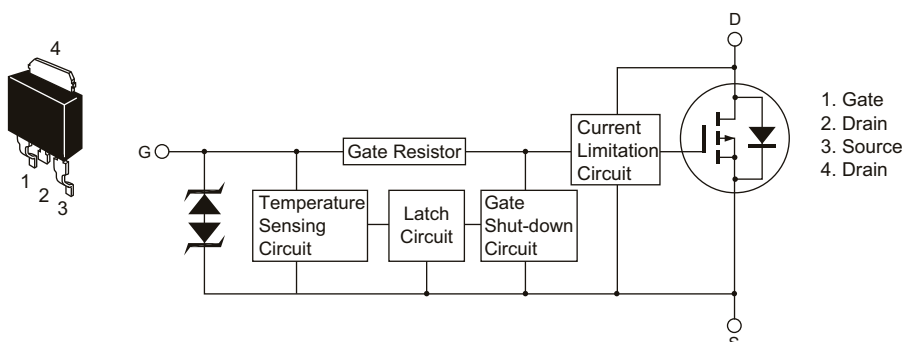
This FET has the over temperature shut-down capability sensing to the junction temperature. This FET has the built-in over temperature shut-down circuit in the gate area. And this circuit operation to shut-down the gate voltage in case of high junction temperature like applying over power consumption, over current etc..

Features

- Built-in the over temperature shut-down circuit.
- High endurance capability against to the short circuit.
- Latch type shut down operation (need 0 voltage recovery).
- Built-in the current limitation circuit.
- High density mounting
- Power supply voltage applies 12 V and 24 V.
- AEC-Q101 compliant

Outline

RENESAS Package code: PRSS0004ZD-C
(Package name: DPAK (S))



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–60	V
Gate to source voltage	V_{GSS}	–16	V
	V_{GSS}	2.5	V
Drain current	I_D ^{Note 3}	–10	A
Body-drain diode reverse drain current	I_{DR}	–10	A
Avalanche current	I_{AP} ^{Note 2}	–7	A
Avalanche energy	E_{AR} ^{Note 2}	210	mJ
Channel dissipation	P_{ch} ^{Note 1}	40	W
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	–55 to +150	°C

Notes: 1. $T_{ch} = 25^\circ\text{C}$

2. $T_{ch} = 25^\circ\text{C}$, $R_g \geq 50 \Omega$

3. It provides by the current limitation lower bound value.

Typical Operation Characteristics

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input voltage	V _{IH}	-3.5	—	—	V	
	V _{IL}	—	—	-1.2	V	
Input current (Gate non shut down)	I _{IH1}	—	—	-100	μA	V _i = -8 V, V _{DS} = 0
	I _{IH2}	—	—	-50	μA	V _i = -3.5 V, V _{DS} = 0
	I _{IL}	—	—	-1	μA	V _i = -1.2 V, V _{DS} = 0
Input current (Gate shut down)	I _{IH(sD)1}	—	-0.8	—	mA	V _i = -8 V, V _{DS} = 0
	I _{IH(sD)2}	—	-0.35	—	mA	V _i = -3.5 V, V _{DS} = 0
Shut down temperature	T _{SD}	—	175	—	°C	Channel temperature
Gate operation voltage	V _{OP}	-3.5	—	-12	V	
Drain current (Current limitation value)	I _D limit	-10	—	—	A	V _{GS} = -12 V, V _{DS} = -10 V ^{Note 4}

Notes; 4. Pulse test

Electrical Characteristics

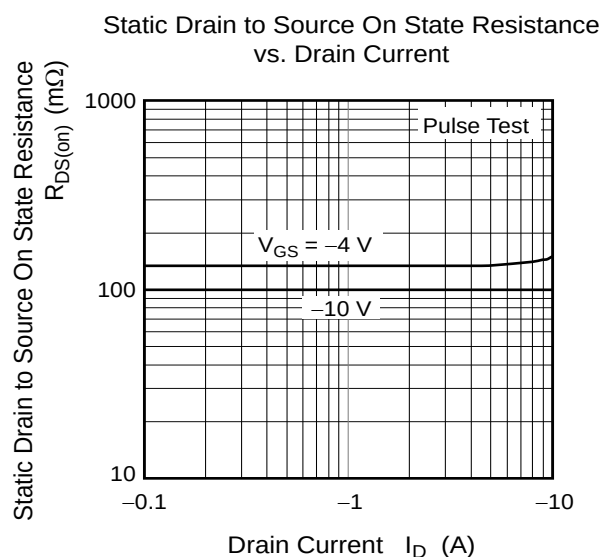
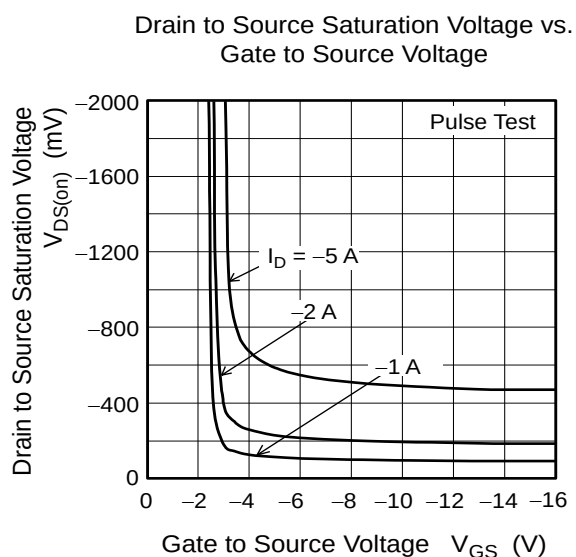
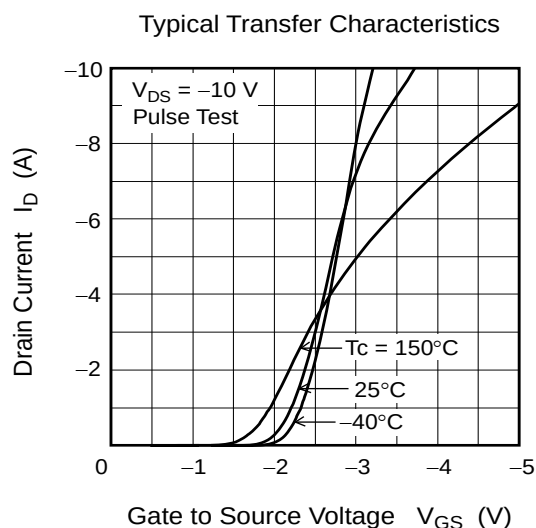
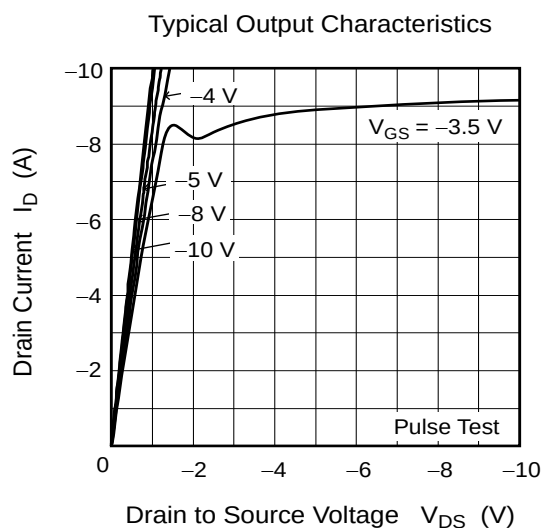
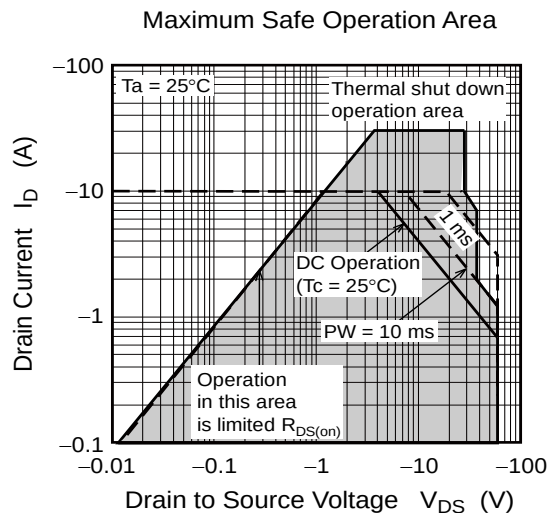
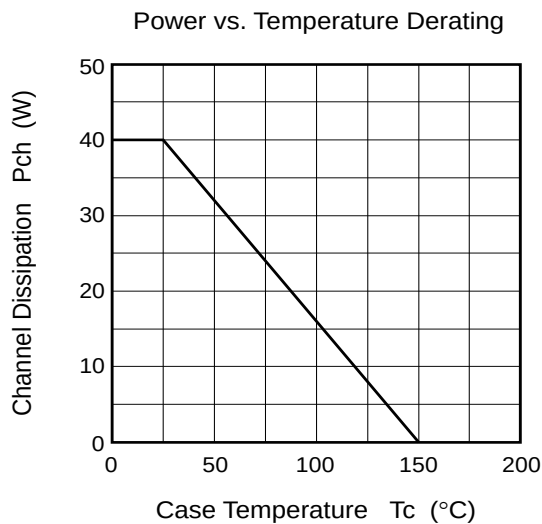
(Ta = 25°C)

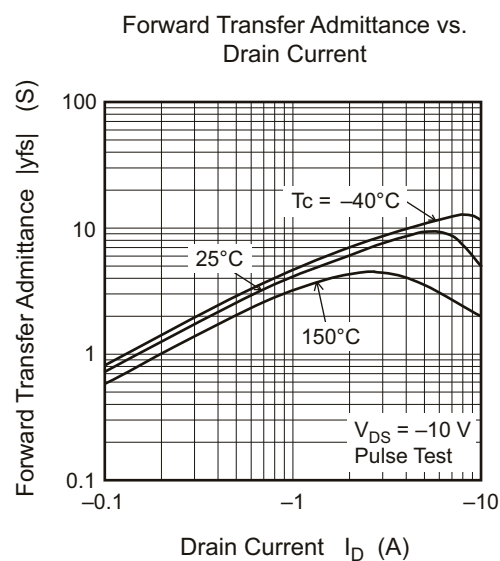
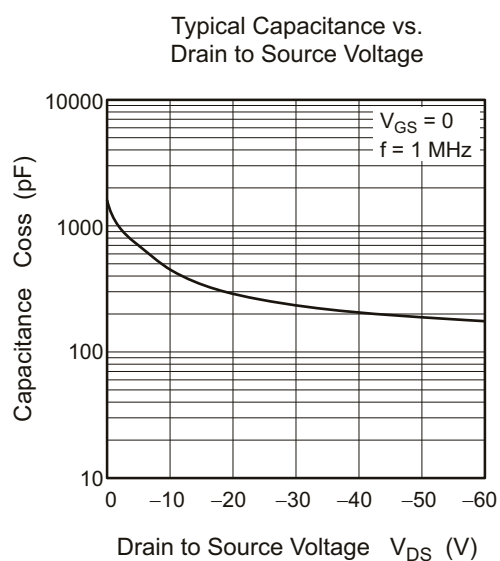
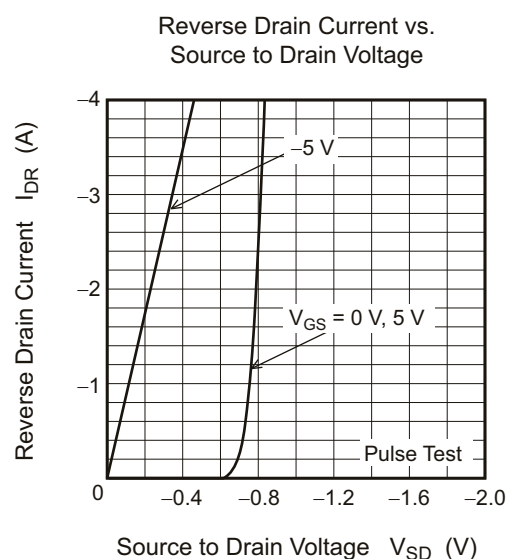
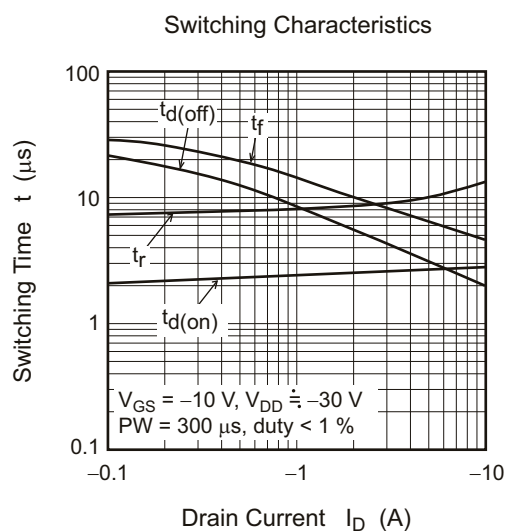
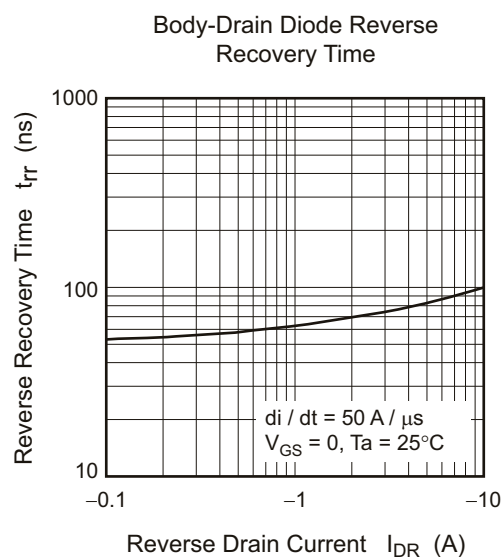
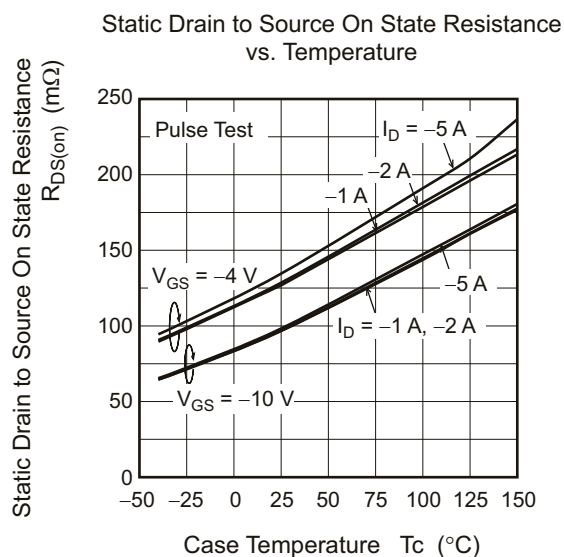
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain current	I _{D1}	—	—	-16	A	V _{GS} = -3.5 V, V _{DS} = -10 V ^{Note 5}
	I _{D2}	—	—	-10	mA	V _{GS} = -1.2 V, V _{DS} = -10 V
	I _{D3}	-10	—	—	A	V _{GS} = -12 V, V _{DS} = -10 V ^{Note 5}
Drain to source breakdown voltage	V _{(BR)DSS}	-60	—	—	V	I _D = -10 mA, V _{GS} = 0
Gate to source breakdown voltage	V _{(BR)GSS}	-16	—	—	V	I _G = -800 μA, V _{DS} = 0
	V _{(BR)GSS}	2.5	—	—	V	I _G = 100 μA, V _{DS} = 0
Gate to source leak current	I _{GSS1}	—	—	-100	μA	V _{GS} = -8 V, V _{DS} = 0
	I _{GSS2}	—	—	-50	μA	V _{GS} = -3.5 V, V _{DS} = 0
	I _{GSS3}	—	—	-1	μA	V _{GS} = -1.2 V, V _{DS} = 0
	I _{GSS4}	—	—	100	μA	V _{GS} = 2.4 V, V _{DS} = 0
Input current (shut down)	I _{GS(OP)1}	—	-0.8	—	mA	V _{GS} = -8 V, V _{DS} = 0
	I _{GS(OP)2}	—	-0.35	—	mA	V _{GS} = -3.5 V, V _{DS} = 0
Zero gate voltage drain current	I _{DSS1}	—	—	-10	μA	V _{DS} = -60 V, V _{GS} = 0
Gate to source cutoff voltage	V _{GS(off)}	-1.0	—	-2.1	V	V _{DS} = -10 V, I _D = -1 mA
Forward transfer admittance	y _{fs}	5	9	—	S	I _D = -5 A, V _{DS} = -10 V ^{Note 5}
Static drain to source on state resistance	R _{DS(on)}	—	131	180	mΩ	I _D = -5 A, V _{GS} = -4 V ^{Note 5}
	R _{DS(on)}	—	100	120	mΩ	I _D = -5 A, V _{GS} = -10 V ^{Note 5}
Output capacitance	C _{oss}	—	444	—	pF	V _{DS} = -10 V, V _{GS} = 0, f = 1MHz
Turn-on delay time	t _{d(on)}	—	2.6	—	μs	V _{GS} = -10 V, I _D = -5 A, R _L = 6 Ω
Rise time	t _r	—	10.6	—	μs	
Turn-off delay time	t _{d(off)}	—	3.1	—	μs	
Fall time	t _f	—	6.0	—	μs	
Body-drain diode forward voltage	V _{DF}	—	-0.93	—	V	I _F = -10 A, V _{GS} = 0 ^{Note 5}
Body-drain diode reverse recovery time	t _{rr}	—	100	—	ns	I _F = -10 A, V _{GS} = 0 di/dt = 50 A/μs
Over load shut down operation time ^{Note 6}	t _{os1}	—	2.2	—	ms	V _{GS} = -5 V, V _{DD} = -16 V
	t _{os2}	—	1.1	—	ms	V _{GS} = -5 V, V _{DD} = -24 V

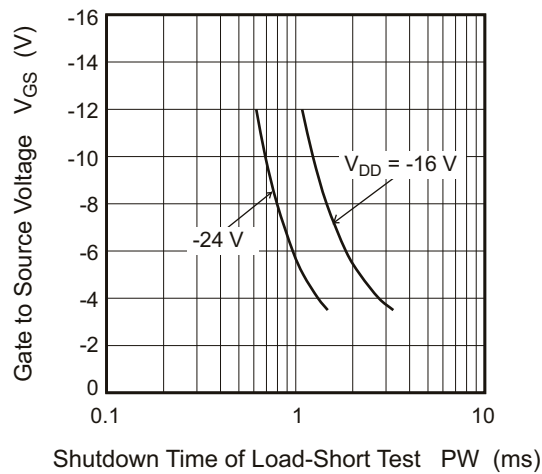
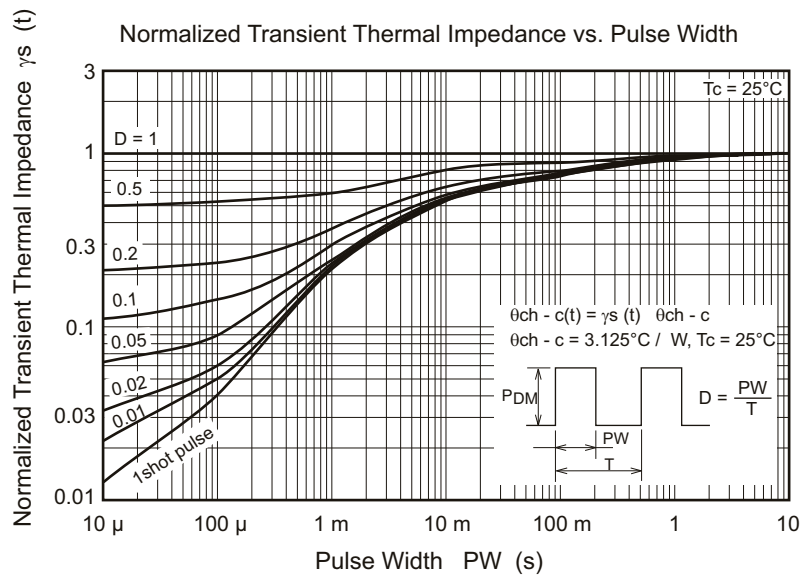
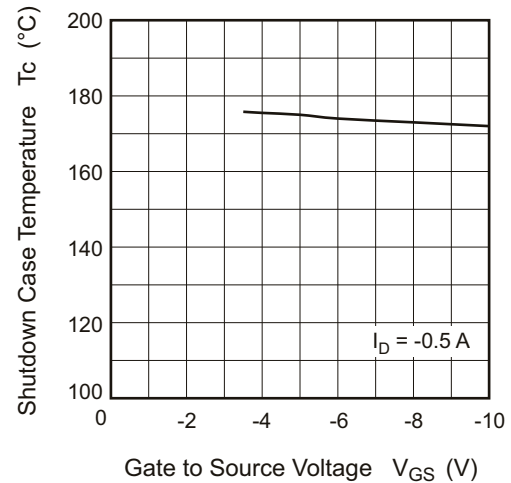
Notes: 5. Pulse test

6. Including the junction temperature rise of the over loaded condition.

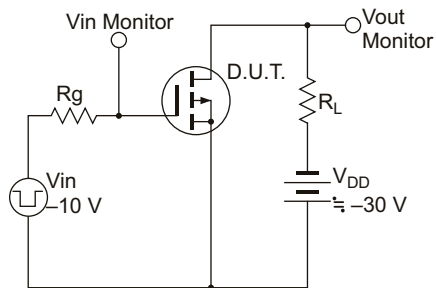
Main Characteristics



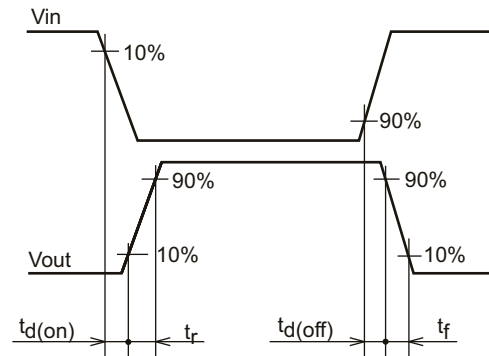


Gate to Source Voltage vs.
Shutdown Time of Load-Short TestShutdown Case Temperature vs.
Gate to Source Voltage

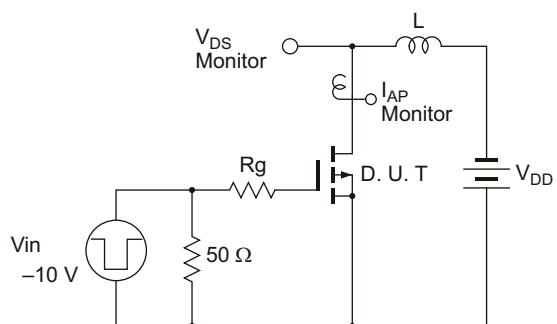
Switching Time Test Circuit



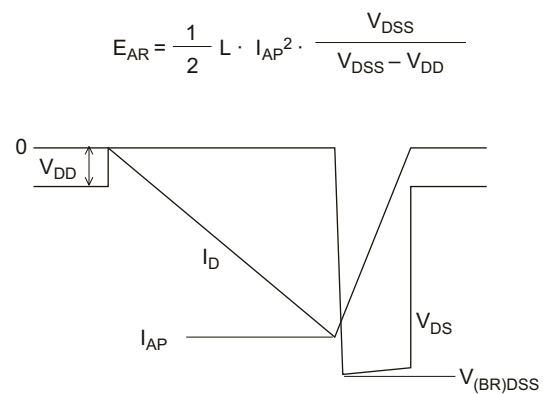
Waveform



Avalanche Test Circuit



Avalanche Waveform



Package Dimensions

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]	Unit: mm
DPAK(S)	SC-63	PRSS0004ZD-C	DPAK(S) / DPAK(S)V	0.28g	

The drawing shows the mechanical dimensions of the RJE0620JPD package in millimeters. The top view shows a rectangular package with a width of 6.5 ± 0.3 mm and a body width of 5.6 ± 0.5 mm. The height is 1.5 ± 0.5 mm. The side view shows a maximum height of 1.2 mm for the top flange, a main body height of 5.5 ± 0.5 mm, and a base height of 2.5 ± 0.5 mm. The base has a width of 2.29 ± 0.5 mm and a pin pitch of 1.0 mm maximum. The bottom view shows a pin width of 0.8 ± 0.1 mm and a pin pitch of 2.29 ± 0.5 mm. The side view also shows a pin width of 0.55 ± 0.1 mm and a pin height of $0 - 0.25$ mm. The bottom view shows a pin width of 0.55 ± 0.1 mm and a pin height of 0.55 ± 0.1 mm. The bottom view also shows a pin width of 0.55 ± 0.1 mm and a pin height of 0.55 ± 0.1 mm.

Ordering Information

Orderable Part Number	Quantity	Shipping Container
RJE0620JPD-00-J3	3000 pcs	Taping

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