# OSCAR™ USER CONFIGURABLE PECL CLOCK

ICS525-04

## Description

The ICS525-04 OSCaR™ is the most flexible way to generate a high quality, high frequency differential PECL clock output from a crystal or CMOS clock input. The name OSCaR™ stands for Oscillator Replacement, as it is designed to replace crystal oscillators in almost any electronic system. Users can easily configure the device to produce nearly any output frequency from any input frequency by grounding or floating the select pins. Neither microcontroller, software, nor device programmer are needed to set the frequency. Using Phase Locked Loop techniques, the device accepts a crystal or clock to produce output clocks up to 156 MHz at 3.3V, keeping them frequency locked together.

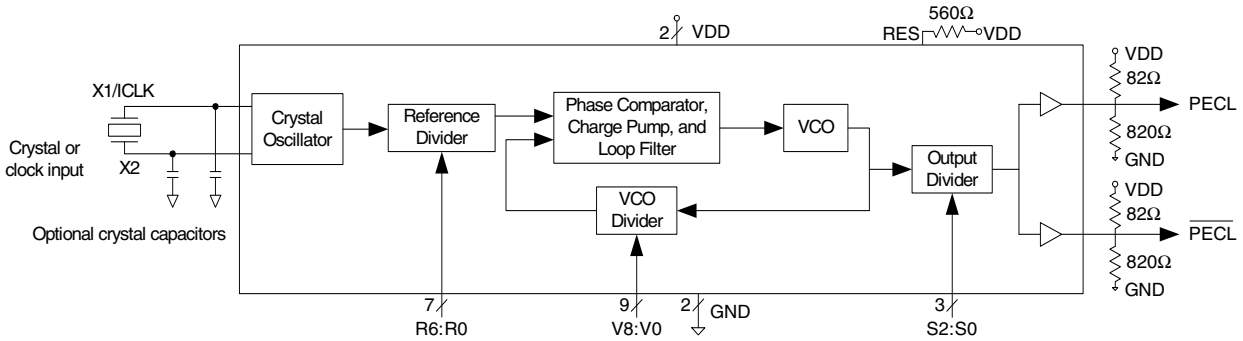
For simple multipliers to produce common frequencies, refer to the LOCO™ family of parts, which are smaller and more cost effective.

This product is intended for clock generation. It has low output jitter (variation in the output period), but input to output skew and jitter are not defined nor guaranteed. For applications which require defined input to output timing, use the ICS527-02.

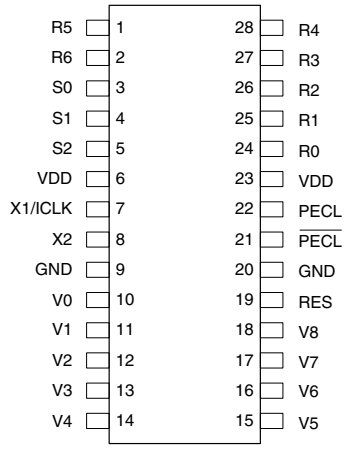
## Features

- Packaged as 28 pin SSOP (150 mil body)
- Highly accurate frequency generation
- User determines the output frequency by setting all internal dividers
- Eliminates need for custom oscillators
- No software needed
- Pull-ups on select inputs
- Input crystal frequency of 5 - 27 MHz
- Input clock frequency of 2 - 50 MHz
- Output clock frequencies up to 156 MHz at 3.3V
- Output clock frequencies up to 200 MHz at 5V
- Very low jitter
- PECL levels set by external resistors
- Operating voltage of 3.3V or 5V
- Ideal for oscillator replacement
- Industrial temperature version available
- Advanced, low power CMOS process

## Block Diagram



## Pin Assignment




28 pin 150 mil body SSOP

## Maximum Output Frequency and Output Divider Table

| S2 Pin 5 | S1 Pin 4 | S0 Pin 3 | CLK Output Divider | Max Output Frequency (MHz) | | | |
|---|---|---|---|---|---|---|---|
| | | | | VDD = 5V | | VDD = 3.3V | |
| | | | | 0 - 70 ° C | -40 - 85 ° C | 0 - 70 ° C | -40 - 85 ° C |
| 0 | 0 | 0 | 6 | 45 | 44 | 27 | 26 |
| 0 | 0 | 1 | 2 | 120 | 117 | 81 | 77 |
| 0 | 1 | 0 | 8 | 34 | 33 | 20 | 19 |
| 0 | 1 | 1 | 4 | 68 | 66 | 40 | 38 |
| 1 | 0 | 0 | 5 | 54 | 53 | 32 | 31 |
| 1 | 0 | 1 | 7 | 39 | 38 | 23 | 22 |
| 1 | 1 | 0 | 1 | 200 | 195 | 162 | 154 |
| 1 | 1 | 1 | 3 | 90 | 89 | 54 | 51 |

## Pin Descriptions

| Pin Number | Pin Name | Pin Type | Pin Description |
|---|---|---|---|
| 1 | R5 | Input | Reference divider word input pins determined by user. Forms a binary number from 0 to 127. Internal pull-up. |
| 2 | R6 | Input | Reference divider word input pins determined by user. Forms a binary number from 0 to 127. Internal pull-up. |
| 3 | S0 | Input | Select pins for output divider determined by user. See table above. Internal pull-up. |
| 4 | S1 | Input | Select pins for output divider determined by user. See table above. Internal pull-up. |
| 5 | S2 | Input | Select pins for output divider determined by user. See table above. Internal pull-up. |
| 6 | VDD | Power | Connect to VDD. |
| 7 | X1/ICLK | Input | Crystal connection. Connect to a parallel resonant crystal or input clock. |
| 8 | X2 | Input | Crystal connection. Connect to a crystal or leave unconnected for clock. |
| 9 | GND | Power | Connect to ground. |
| 10 - 18 | V0 - V8 | Input | VCO divider word input pins determined by user. Forms a binary number from 0 to 511. Internal pull-up. |
| 19 | RES | Input | Bias resistor input. Connect a resistor between this pin and VDD. |
| 20 | GND | Power | Connect to ground. |
| 21 | $\overline{\text{PECL}}$ | Output | Complementary PECL output. Connect resistor load to this pin. |
| 22 | PECL | Output | PECL output. Connect resistor load to this pin. |
| 23 | VDD | Power | Connect to VDD. |
| 24 | R0 | Input | Reference divider word input pins determined by user. Forms a binary number from 0 to 127. Internal pull-up. |
| 25 | R1 | Input | Reference divider word input pins determined by user. Forms a binary number from 0 to 127. Internal pull-up. |
| 26 | R2 | Input | Reference divider word input pins determined by user. Forms a binary number from 0 to 127. Internal pull-up. |
| 27 | R3 | Input | Reference divider word input pins determined by user. Forms a binary number from 0 to 127. Internal pull-up. |
| 28 | R4 | Input | Reference divider word input pins determined by user. Forms a binary number from 0 to 127. Internal pull-up. |

# External Components

## Decoupling Capacitors

As with any high performance mixed-signal IC, the ICS525-04 must be isolated from system power supply noise to perform optimally.

Decoupling capacitors of 0.01µF must be connected between each VDD and the GND, one on each side of the chip.The capacitor must be connected close to the device to minimize lead inductance. No external power supply filtering is required for this device.

## External Resistors

A 560Ω resistor must be connected between RES (pin 19) and VDD. A total of four resistors are needed for the PECL outputs as shown on the block diagram on page 1. The value of these resistors are shown, but can be varied to change the differential pair output swing and the common mode voltage. Consult application note MAN09 for more information.

## Crystal Load Capacitors

The total on-chip capacitance for a crystal is approximately 16 pF, so a parallel resonant, fundamental mode crystal with this value of load (correlation) capacitance should be used. For crystals with a specified load capacitance greater than 16 pF, crystal capacitors may be connected from each of the pins X1 and X2 to Ground as shown in the block diagram. The value (in pF) of these crystal caps should be (CL - 16)*2, where CL is the crystal load capacitance. These external capacitors are only required for applications where the exact frequency is critical. For a clock input, connect to X1 and leave X2 unconnected (no capacitors on either).

## Determining the Output Frequency

Users have full control in setting the desired output frequency over the range shown in the table on page 2. To replace a standard oscillator, users should connect the divider select input pins directly to ground (or VDD, although this is not required because of internal pull-ups) during Printed Circuit Board layout. The ICS525-04 will automatically produce the correct clock when all components are soldered. It is also possible to connect the inputs to parallel I/O ports to switch frequencies. By choosing divides carefully, the number of inputs which need to be changed can be minimized. Observe the restrictions on allowed values of VDW and RDW.

The output of the ICS525-04 can be determined by the following simple equation:

$$\text{PECL Frequency} = \text{Input Frequency} \times \frac{VDW + 8}{(RDW + 2) \bullet OD}$$

Where:

Reference Divider Word (RDW) = 0 to 127

VCO Divider Word (VDW) = 0 to 511

Output Divider (OD) = values on page 2

Also, the following operating ranges should be observed:

$$10M < \text{Input Frequency} \times \frac{VDW + 8}{(RDW + 2)} < 200M(5V) \text{or} 162M(3.3v))$$

$$200kHz < \frac{\text{InputFrequency}}{(RDW + 2)}$$

See table on page 2 for full details of maximum output.

The dividers are expressed as integers. For example, if a 66.66 MHz output on CLK1 is desired from a 14.31818 MHz input, the VCO divider word (VDW) should be 276, with an output divide (OD) of 2. In this example, R6:R0 is 0111011, V8:V0 is 100010100 and S2:S0 is 001. Since all of these inputs have pull-up resistors, it is only necessary to ground the zero pins, namely V7, V6, V5, V3, V1, V0, R6, R2, S2, and S1.

To determine the best combination of VCO, reference, and output divide, use the ICS525 Calculator on our web site: www.idt.com. The online form is easy to use and quickly shows you up to three options for these settings.

## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS525-04. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item | Rating |
|---|---|
| Supply Voltage, VDD | 7V |
| All Inputs and Outputs | -0.5V to VDD+0.5V |
| Ambient Operating Temperature | -40 to +85° C |
| Storage Temperature | -65 to +150° C |
| Junction Temperature | 175° C |
| Soldering Temperature | 260° C |

## Recommended Operation Conditions

| Parameter | Min. | Typ. | Max. | Units |
|---|---|---|---|---|
| Ambient Operating Temperature, ICS525R-04 | 0 | | +70 | ° C |
| Ambient Operating Temperature, ICS525R-04I | -40 | | +85 | ° C |
| Power Supply Voltage (measured in respect to GND) | +3.0 | | +5.5 | V |

## DC Electrical Characteristics

Unless stated otherwise, VDD = 3.3V ±10%, Ambient Temperature 0 to +70° C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Operating Voltage | VDD | | 3.0 | | 5.5 | V |
| Supply Current | IDD | 15 MHz in, 60MHz out, no load | | 34 | | mA |
| | | 15MHz in, 60MHz out, VDD = 5V | | 60 | | mA |
| Input High Voltage | $V_{IH}$ | | 2 | | | V |
| Input Low Voltage | $V_{IL}$ | | | | 0.8 | V |
| Input High Voltage | $V_{IH}$ | X1/ICLK only | VDD/2+1 | VDD/2 | | V |
| Input Low Voltage | $V_{IL}$ | X1/ICLK only | | VDD/2 | VDD/2-1 | V |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -12 mA | 2.4 | | | V |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 12 mA | | | 0.4 | V |
| Input Capacitance | $C_{IN}$ | V, R, S select pins | | 5 | | pF |
| On-chip pull-up resistor | $R_{PU}$ | V, R, S select pins | | 270 | | kΩ |

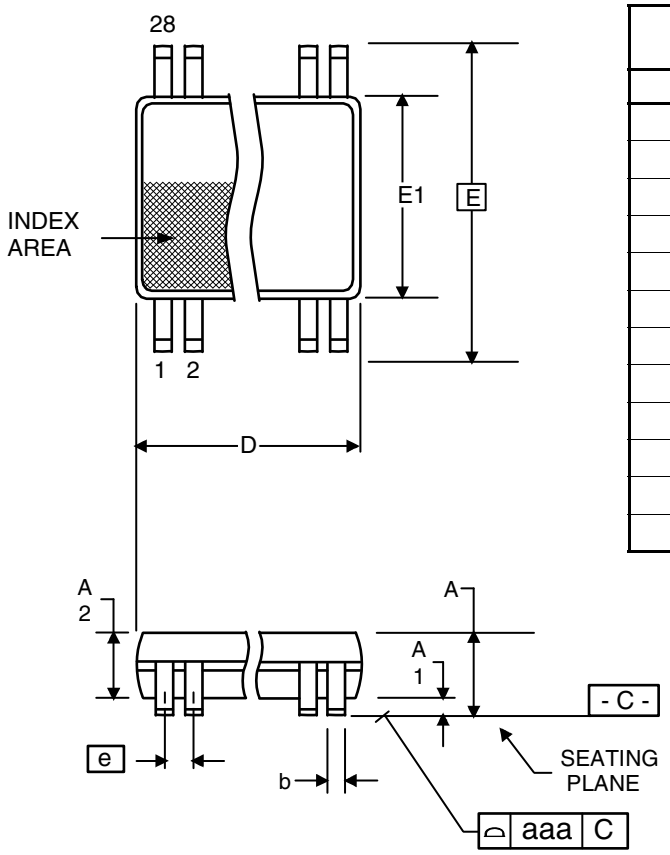
## AC Electrical Characteristics

Unless stated otherwise, VDD = 3.3V ±5%, Ambient Temperature -40 to +85° C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Input Frequency | $F_{IN}$ | Crystal input | 5 | | 27 | MHz |
| | | Clock input | 2 | | 50 | MHz |
| Output Frequency with OD=2, VDD=4.5 to 5 | $F_{OUT}$ | 0 to +70° C | 1 | | 120 | MHz |
| | | -40 to +85° C | 1 | | 117 | MHz |
| Output Frequency with OD=2, VDD=3.0 to 3.3 | $F_{OUT}$ | 0 to +70° C | 1 | | 81 | MHz |
| | | -40 to +85° C | 1 | | 77 | MHz |
| Absolute Clock Period Jitter | $t_{ja}$ | Deviation from mean | | ± 50 | | ps |
| One sigma Clock Period Jitter | $t_{js}$ | | | 20 | | ps |

## Package Outline and Package Dimensions (28 pin SSOP, 150 mil Body, 0.025 mm Pitch)

Package dimensions are kept current with JEDEC Publication No. 95, MO-153




| | Millimeters | | Inches | |
|---|---|---|---|---|
| Symbol | Min | Max | Min | Max |
| A | 1.35 | 1.75 | .053 | .069 |
| A1 | 0.10 | 0.25 | .0040 | .010 |
| A2 | -- | 1.50 | -- | .059 |
| b | 0.20 | 0.30 | .008 | .012 |
| C | 0.18 | 0.25 | .007 | .010 |
| D | 9.80 | 10.00 | .386 | .394 |
| E | 5.80 | 6.20 | .228 | .244 |
| E1 | 3.80 | 4.00 | .150 | .157 |
| e | 0.635 Basic | | 0.025 Basic | |
| L | 0.40 | 1.27 | .016 | .050 |
| α | 0° | 8° | 0° | 8° |
| aaa | -- | 0.10 | -- | 0.004 |

## Ordering Information

| Part / Order Number | Marking | Shipping Packaging | Package | Temperature |
|---|---|---|---|---|
| 525R-04LF | ICS525R-04LF | Tubes | 28-pin SSOP | 0 to +70° C |
| 525R-04LFT | ICS525R-04LF | Tape and Reel | 28-pin SSOP | 0 to +70° C |
| 525R-04ILF | ICS525R-04ILF | Tubes | 28-pin SSOP | -40 to +85° C |
| 525R-04ILFT | ICS525R-04ILF | Tape and Reel | 28-pin SSOP | -40 to +85° C |

**"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.**

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