

2SJ601-ZK

P-Channel Power [MOS FET](#)

-60V, -36A, 31mΩ

R07DS1591EJ0200

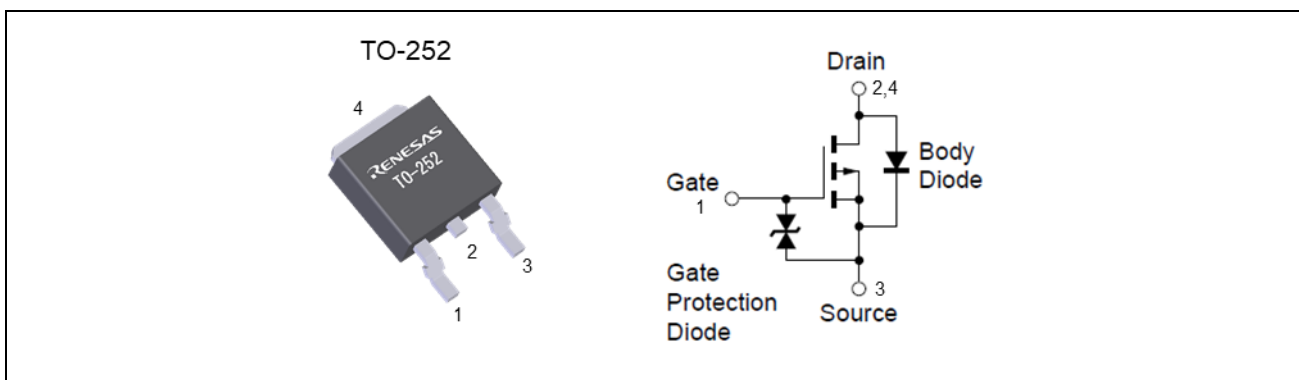
Rev.2.00

Feb.3.2025

Features

- Low on-state resistance
RDS(on)1 = 31 mΩ MAX. (VGS = -10 V, ID = -18 A)
RDS(on)2 = 46 mΩ MAX. (VGS = -4.0 V, ID = -18 A)
- Low Ciss: Ciss = 3300 pF TYP.
- Built-in gate protection diode
- Applications : For switching

Outline



Absolute Maximum Ratings

(Tj=25°C unless otherwise notice.)

Item	Symbol	Ratings	Unit
Drain to Source Voltage	V _{DSS}	-60	V
Gate to Source Voltage	V _{GSS}	±20	V
Drain Current (DC)	I _{D(DC)} Notes1,2,5	±36	A
Drain Current (pulse)	I _{D(pulse)} Notes1,3,5	±120	A
Power Dissipation T _c = 25°C	P _D Notes5	65	W
Power Dissipation T _a = 25°C	P _D Notes5	1.0	W
Junction Temperature	T _j	150	°C
Storage Temperature	T _{stg}	-55 to 150	°C
Single Avalanche Current	I _{AS} Notes4	-36	A
Single Avalanche Energy	E _{AS} Notes4	123	mJ

Thermal Resistance

Item	Symbol	Max	Unit
Junction to Case Thermal Resistance	R _{th(j-c)} Notes5	1.92	°C/W
Junction to Ambient Thermal Resistance	R _{th(j-a)} Notes5	125	°C/W

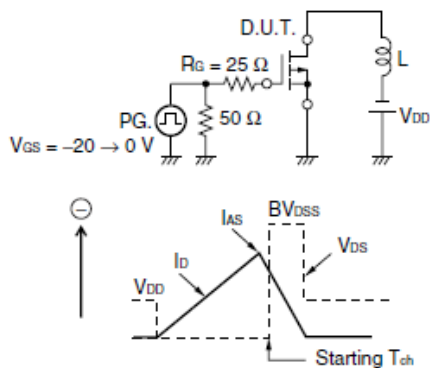
Electrical Characteristics

(T_j=25°C unless otherwise notice.)

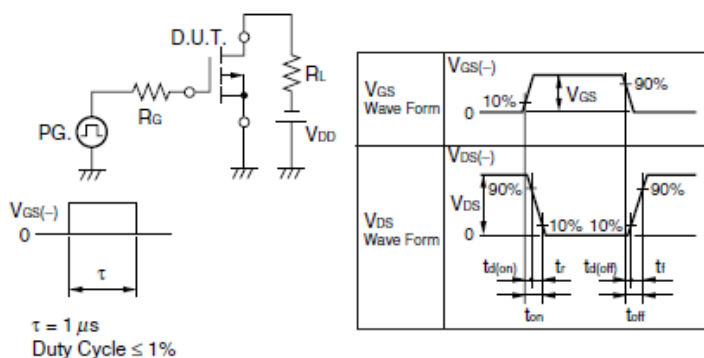
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I _{DSS}	—	—	-10	μA	V _{DS} = -60 V, V _{GS} = 0 V
Gate Leakage Current	I _{GSS}	—	—	±10	μA	V _{GS} = ±20 V, V _{DS} = 0 V
Gate to Source Threshold Voltage	V _{GS(th)}	-1.5	-2.0	-2.5	V	V _{DS} = -10 V, I _D = -1 mA
Forward Transfer Admittance	y _{fs}	15	30	—	S	V _{GS} = -10 V, I _D = -18 A
Drain to Source On-state Resistance	R _{DS(on)}	—	25	31	mΩ	V _{GS} = -10 V, I _D = -18 A
	R _{DS(on)}	—	32	46	mΩ	V _{GS} = -4.0 V, I _D = -18 A
Input Capacitance	C _{iss}	—	3300	—	pF	V _{DS} = -10 V V _{GS} = 0 V f = 1 MHz
Output Capacitance	C _{oss}	—	580	—	pF	
Reverse Transfer Capacitance	C _{rss}	—	230	—	pF	
Turn-on Delay Time	t _{d(on)}	—	11	—	ns	V _{DD} = -30 V I _D = -18 A V _{GS} = -10 V R _G = 0 Ω
Rise Time	t _r	—	12	—	ns	
Turn-off Delay Time	t _{d(off)}	—	80	—	ns	
Fall Time	t _f	—	53	—	ns	
Total Gate Charge	Q _g	—	63	—	nC	V _{DD} = -48 V V _{GS} = -10 V I _D = -36 A
Gate to Source Charge	Q _{gs}	—	10	—	nC	
Gate to Drain Charge	Q _{gd}	—	16	—	nC	
Body Diode Forward Voltage	V _{F(S-D)}	—	1.0	—	V	I _F = 36 A, V _{GS} = 0 V
Reverse Recovery Time	t _{rr}	—	52	—	ns	I _F = 36 A, V _{GS} = 0 V di/dt = 100 A/μs
Reverse Recovery Charge	Q _{rr}	—	108	—	nC	

- Notes
1. T_c = 25°C
 2. Value is limited by overall system design including PCB
 3. P_W ≤ 10 μs
 4. L = 100 μH, V_{DD} = -30 V, V_{GS} = -20 → 0 V, R_G = 25 Ω
 5. Defined by design. Not subject to production test.

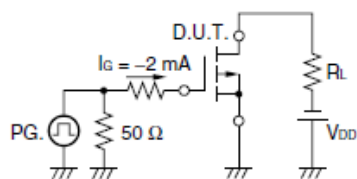
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

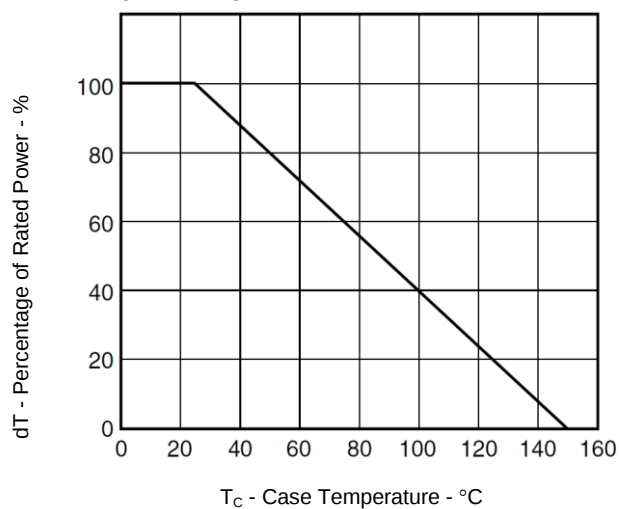


TEST CIRCUIT 3 GATE CHARGE

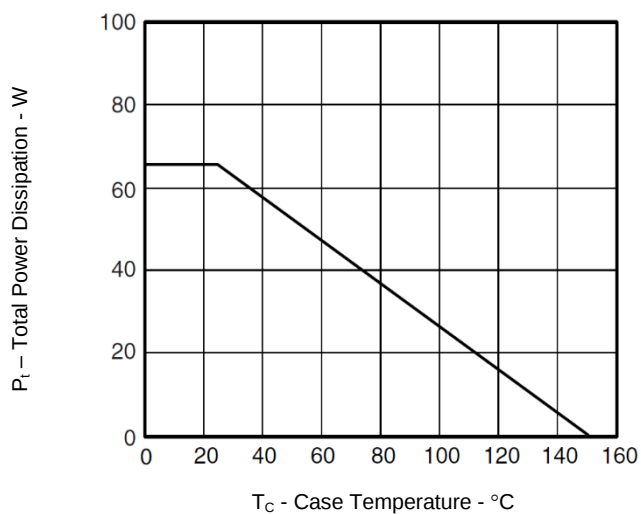


Typical Characteristics

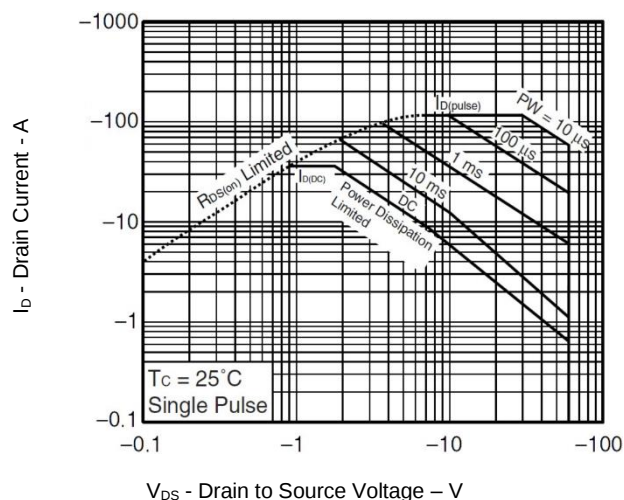
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



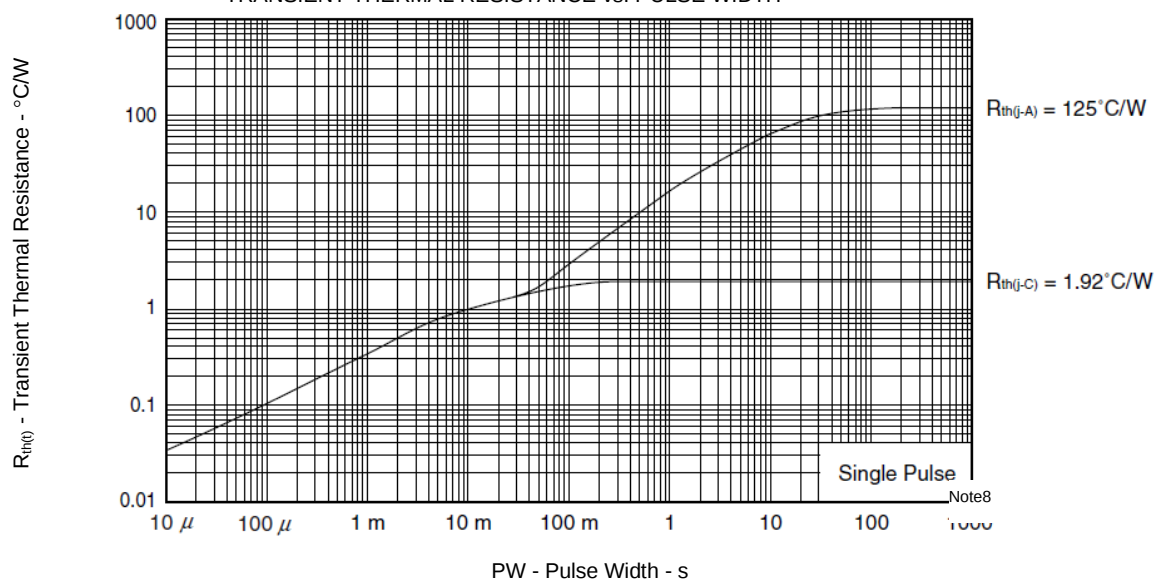
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



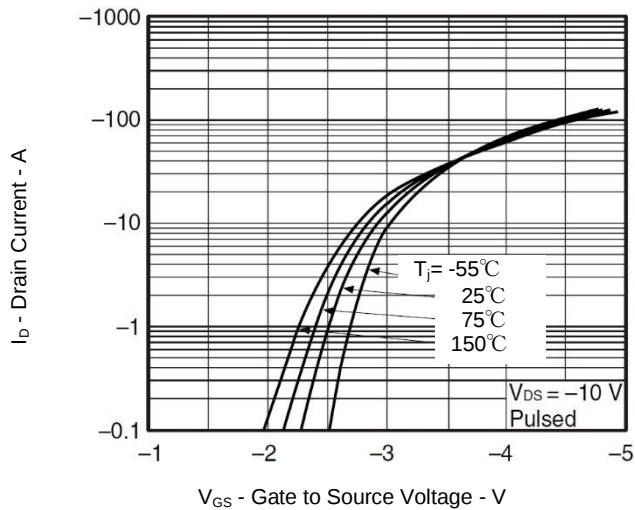
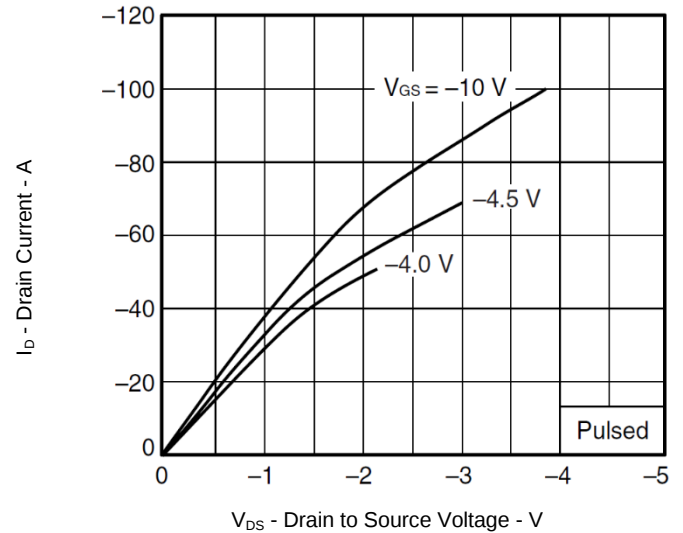
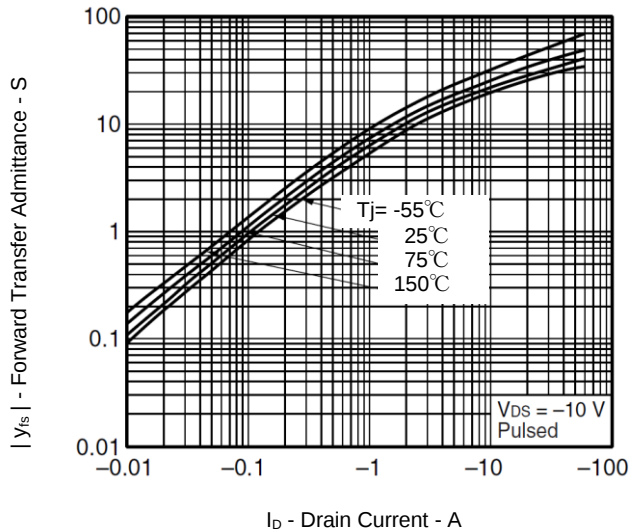
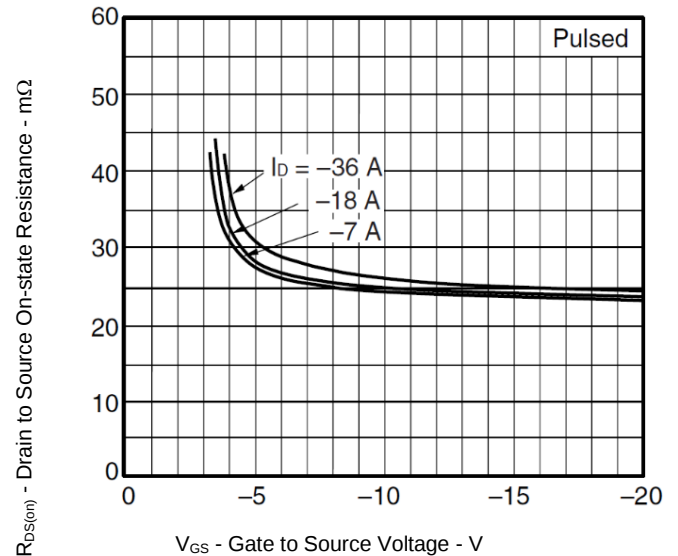
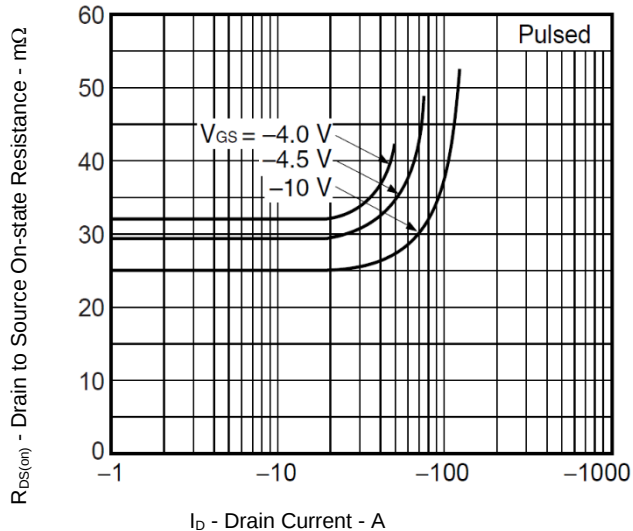
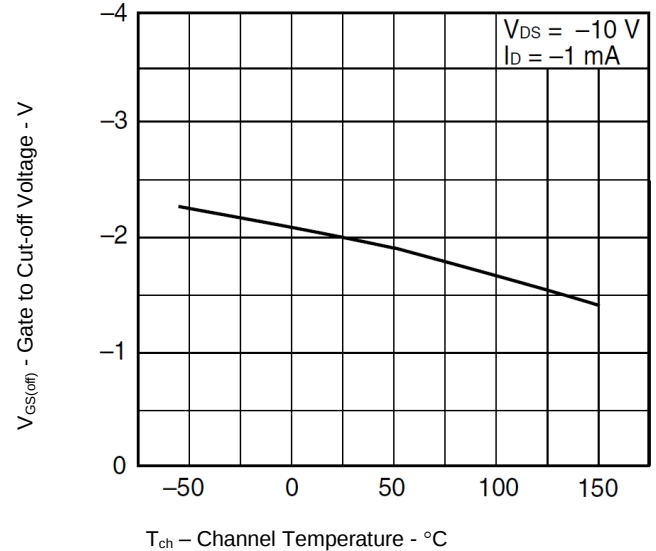
FORWARD BIAS SAFE OPERATING AREA

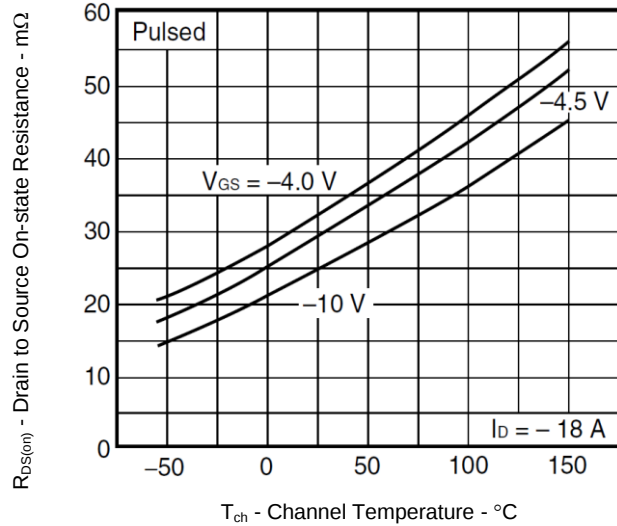
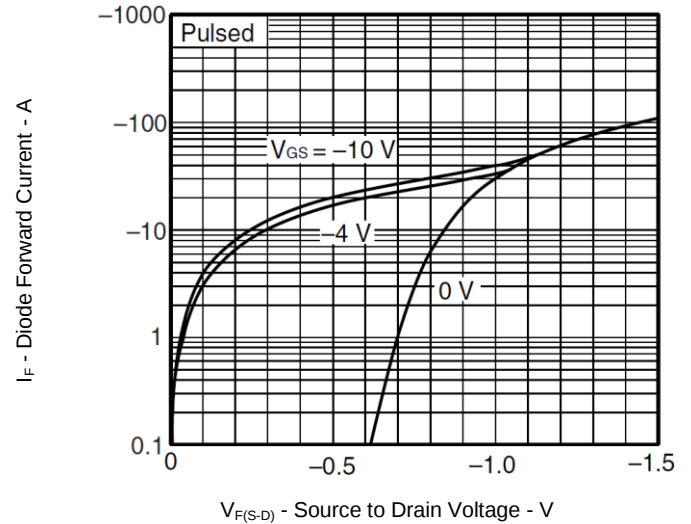


TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

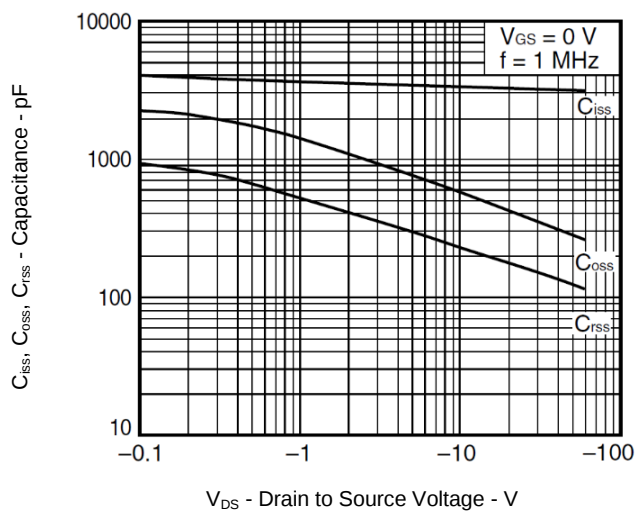


FORWARD TRANSFER CHARACTERISTICS

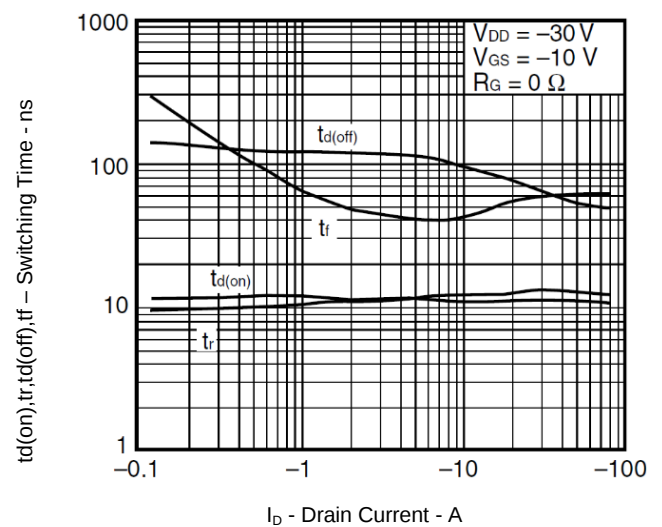
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGEFORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENTDRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGEDRAIN TO SOURCE ON-STATE
RESISTANCE vs. DRAIN CURRENTGATE TO SOURCE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE

DRAIN TO SOURCE ON-STATE RESISTANCE vs.
CHANNEL TEMPERATURESOURCE TO DRAIN DIODE
FORWARD VOLTAGE

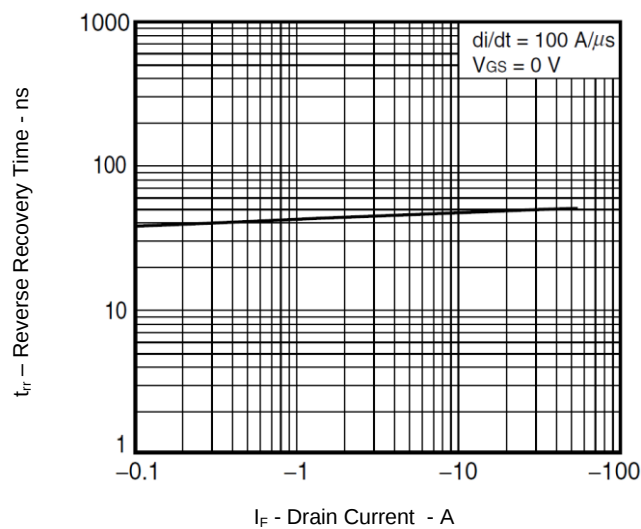
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



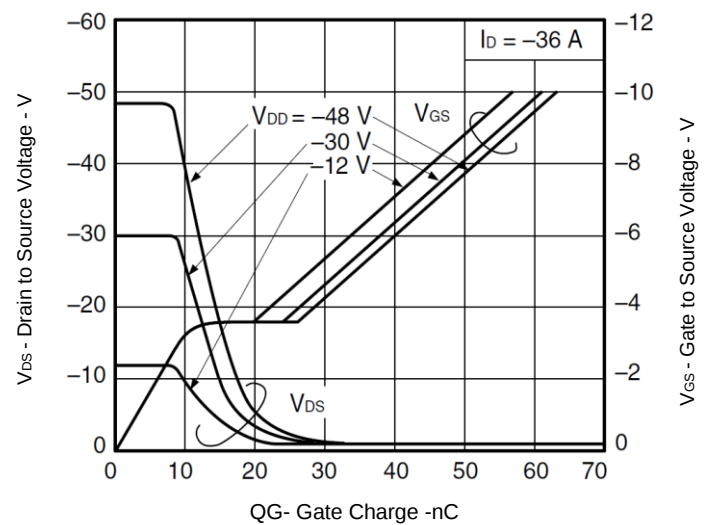
SWITCHING CHARACTERISTICS

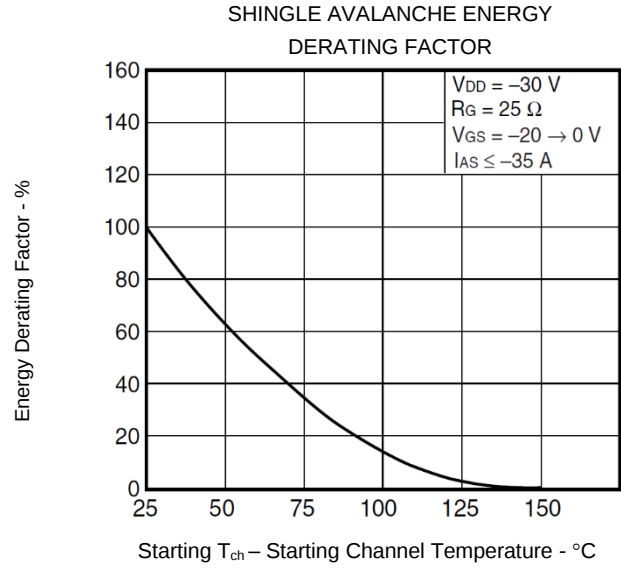
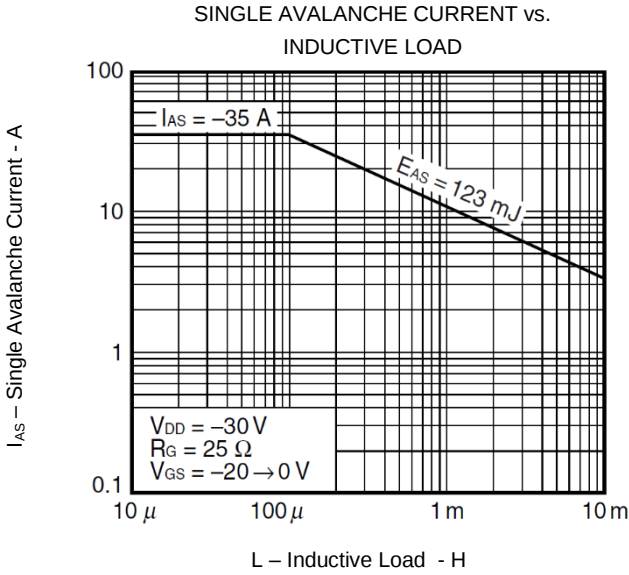


REVERSE RECOVERY TIME vs. DRAIN CURRENT



DYNAMIC INPUT/OUTPUT CHARACTERISTICS





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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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Revision History

Rev.	Date	Description	
		Page	Summary
-	Aug 2006	-	Previous No. D14646EJ5V0DS00
2.00	Feb 3 , 2025	7	Changed Package Dimensions