IS-1845ASRH, IS-1845ASEH

Single Event Radiation Hardened High Speed, Current Mode PWM

FN9001
Rev.7.01
Feb 16, 2022

The IS-1845ASRH, IS-1845ASEH are designed to be used in switching power supplies operating in current-mode. Every other rising edge of the on-chip oscillator turns on the output. Turn-off is controlled by the current sense comparator and occurs when the sensed current reaches a peak controlled by the error amplifier. Turn-off can also be triggered by the end of the oscillator period. These devices feature a single output operating from zero to less than 50% duty cycle.

Constructed with Renesas Rad Hard Silicon Gate (RSG) dielectrically isolated BiCMOS process, these devices are immune to single event latch-up and have been specifically designed to provide a high level of immunity to single event transients. All specified parameters are ensured and tested for 300krad(Si) total dose performance at a high dose rate and 50krad(Si) total dose at a low dose rate.

Detailed Electrical Specifications for these devices are contained in the SMD 5962-01509.

Features

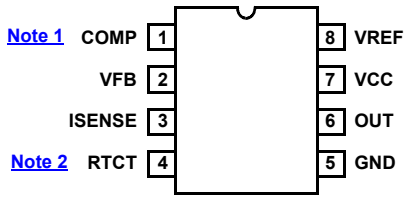
- Electrically Screened to DSCC SMD # 5962-01509
- QML Qualified per MIL-PRF-38535 Requirements
- Radiation acceptance testing - IS-1845ASRH
  - High Dose Rate . . . . . 300krad(Si) (Max)
- Radiation acceptance testing - IS-1845ASEH
  - High Dose Rate . . . . . 300krad(Si) (Max)
  - Low Dose Rate . . . . . 50krad(Si) (Max)
- SEE hardness (see SEE report for details)
  - SEL Immune . . . . . Dielectrically Isolated
  - SEU Immune. . . . . 35MeV/mg/cm^2
  - SEU Cross-Section at 89MeV/mg/cm^2. . . . . 5x10^{-6}cm^2
- Low Start-up Current . . . . . 100µA (Typ)
- Fast Propagation Delay. . . . . .80ns (Typ)
- Supply Voltage Range . . . . . 12V to 20V
- High Output Drive. . . . . 1A (Peak, Typ)
- Undervoltage Lockout . . . . . 8.8V Start (Typ), 8.2V Stop (Typ)

Applications

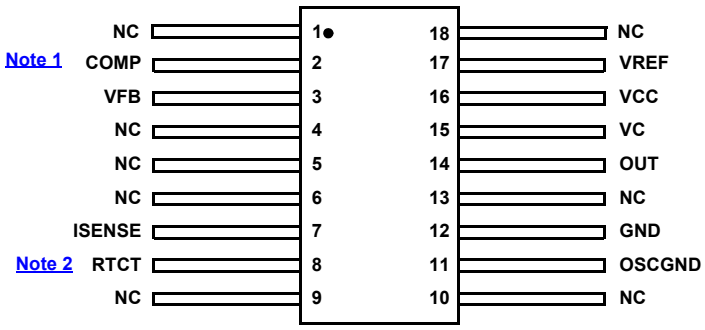
- Current-Mode Switching Power Supplies
- Control of High Current FET Drivers
- Motor Speed and Direction Control

Pin Configurations

IS7-1845ASRH, IS7-1845ASEH
(8 LD CDIP2-T8 SBDIP)
TOP VIEW



IS9-1845ASRH, IS9-1845ASEH
(18 LD FLATPACK)
TOP VIEW



NOTES:

1. Grounding the COMP pin does not inhibit the output. The output may be inhibited by applying >1.2V to the ISENSE pin.
2. This part is production tested with C_t = 3.3nF and R_t = 10k timing components only.

Ordering Information

SMD ORDERING NUMBER (Note 3)	PART NUMBER (Note 4)	RADIATION HARDNESS (Total Ionizing Dose)	PACKAGE DESCRIPTION (RoHS Compliant)	PKG. DWG. #	TEMP. RANGE
5962F0150901V9A	IS0-1845ASRH-Q (Note 5)	HDR to 300krad(Si)	Die	N/A	-50 to +125°C
5962F0150902V9A	IS0-1845ASEH-Q (Note 5)	HDR to 300krad(Si), LDR to 50krad(Si)			
N/A	IS0-1845ASRH/SAMPLE (Notes 5, 6)	N/A			
5962F0150901VPC	IS7-1845ASRH-Q	HDR to 300krad(Si)	8 Ld SBDIP	D8.3	
5962F0150901QPC	IS7-1845ASRH-8				
5962F0150902VPC	IS7-1845ASEH-Q	HDR to 300krad(Si), LDR to 50krad(Si)			
N/A	IS7-1845ASRH/PROTO (Note 6)	N/A			
5962F0150901VXC	IS9-1845ASRH-Q	HDR to 300krad(Si)	18 Ld Flatpack	K18.B	
5962F0150901QXC	IS9-1845ASRH-8				
5962F0150902VXC	IS9-1845ASEH-Q	HDR to 300krad(Si), LDR to 50krad(Si)			
N/A	IS9-1845ASRH/PROTO (Note 6)	N/A			

NOTES:

3. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed must be used when ordering.
4. These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
5. Die product tested at T_A = + 25°C. The wafer probe test includes functional and parametric testing sufficient to make the die capable of meeting the electrical performance outlined in SMD.
6. The /PROTO and /SAMPLE parts are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across temperature specified in the DLA SMD and are in the same form and fit as the qualified device. The /SAMPLE parts are capable of meeting the electrical limits and conditions specified in the DLA SMD. The /SAMPLE parts do not receive 100% screening across temperature to the DLA SMD electrical limits. These part types do not come with a Certificate of Conformance because they are not DLA qualified devices.

Typical Performance Curves

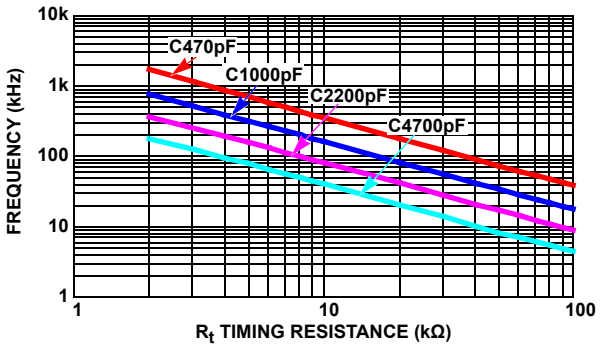


FIGURE 1. OSCILLATOR FREQUENCY vs R_t and C_t

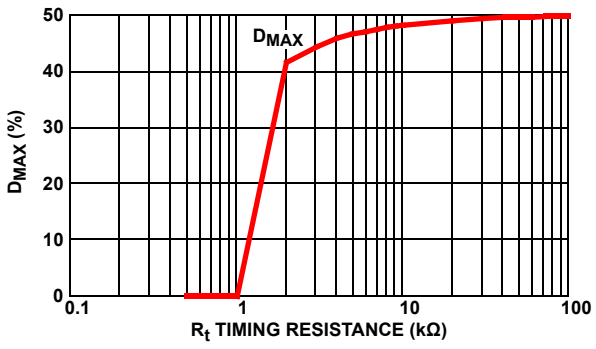


FIGURE 2. MAXIMUM DUTY CYCLE vs R_t

Die Characteristics

DIE DIMENSIONS

3090µm x 4080µm (121.6 mils x 159.0 mils)
Thickness: 483µm ± 25.4µm (19 mils ± 1 mil)

INTERFACE MATERIALS

Glassivation

Type: Phosphorus Silicon Glass (PSG)
Thickness: 8.0kA ± 1.0kA

Top Metallization

Type: AlSiCu
Thickness: 16.0kA ± 2kA

Substrate

Radiation Hardened Silicon Gate, Dielectric Isolation

Backside Finish

Silicon

ASSEMBLY RELATED INFORMATION

Substrate Potential

Unbiased (DI)

ADDITIONAL INFORMATION

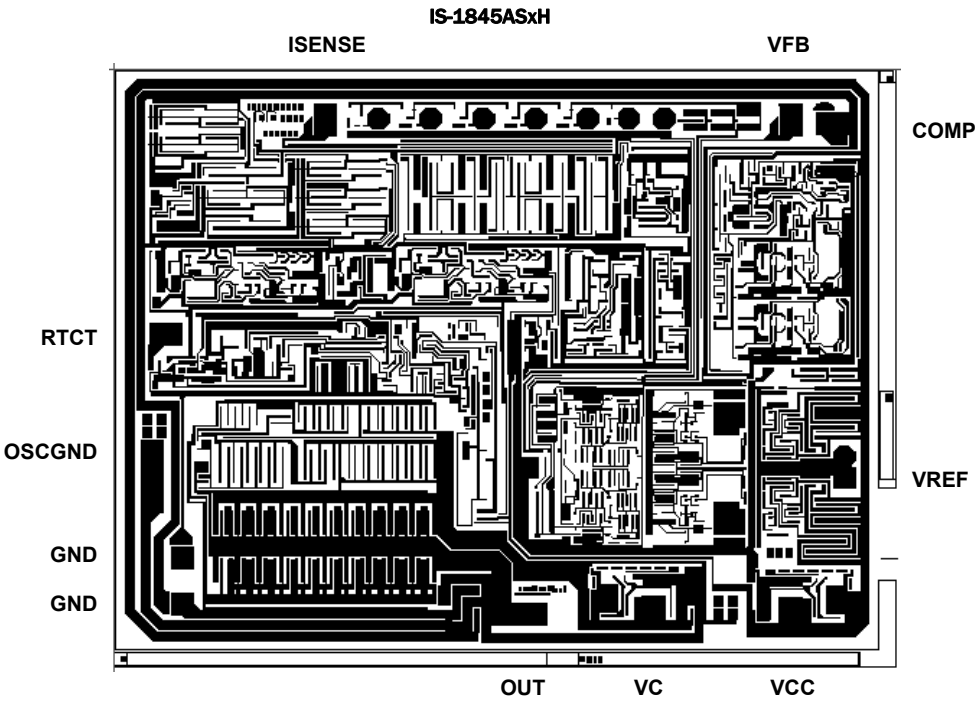
Worst Case Current Density

$<2.0 \times 10^5$ A/cm^2

Transistor Count

582

Metallization Mask Layout



NOTES:

7. Both the GND pads must be bonded to ground.
8. The OUT double-sized bond pad must be double bonded for current sharing purposes.
9. The OSCGND double-sized bond pad must be double bonded to ground for current sharing purposes.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

DATE	REVISION	CHANGE
Feb 16, 2022	7.01	Updated page 1 description. Updated Radiation Environment feature bullets. Updated Note 2. Updated ordering information table by adding Note 5, updating Note 6, adding Radiation Hardness information, and reformatting. Updated Figure 2.
Nov 1, 2019	7.00	Added Related Literature Updated Links throughout. Updated Ordering information by updating temperature for die parts and adding applicable notes. Added Revision History. Updated Disclaimer.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/