Supplemental Information

This Document Errata reflects changes required for the device datasheet of 82V3380.

Revision History

March 01, 2011: First version of documentation errata for the affected devices.

Errata Item

Pages 40 and 41 - Refer to Tables 25 and 26.
- Add a Note for both tables to reflect the errata.

CURRENT:

OUT7 does support 25MHz or 125MHz when Non-Ethernet clock signals are selected for OUT3.

CHANGE TO:

OUT7 **doesn't** support 25MHz or 125MHz when Non-Ethernet clock signals are selected for OUT3.

Page 40, Table 25 **-** Outputs on OUT1 ~ OUT7 if Derived from T0/T4 DPLL Outputs
- Add a Note at the bottom side of the table.

CURRENT:

No comment regarding errata.

CHANGE TO:

Add Note 4:
OUT7 doesn't support 25MHz or 125MHz when Non-Ethernet clock signals are selected for OUT3.

Page 41, Table 26 **-** Outputs on OUT1 ~ OUT7 if Derived from T0 APLL
- Add a Note at the bottom side of the table.

CURRENT:

No comment regarding errata.

CHANGE TO:

Add Note 3:
OUT7 doesn't support 25MHz or 125MHz when Non-Ethernet clock signals are selected for OUT3.

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