

**General Configuration**

Parameter	Value
Jitter	< 150 fs
Package	2.5 x 2 mm
Output Frequency	1000 MHz
Frequency Stability	± 25 ppm
VDD Voltage	3.3 V
Output Type	LVPECL
Output Enable/Disable Position (E/D) Position	Pin 5
Temperature Grade	-40°C to +85°C

**Pin Assignment**

Pin Number	Pin Name	Description
1	NC	No connect
2	NC	No connect
3	VC (NA)	Voltage Control (Not active for XO mode)
4	SDA (NA)	Serial data (Not active for XO mode)
5	OE	Output Enable (0 = output disabled; pulled high internally)
6	SCL (NA)	Serial Clock (Not active for XO mode)
7	VDD Output	Supply voltage output stage - must be connected to VDD Core
8	Output 0	Output
9	Output 0b	Complementary output
10	Ground Output	Ground Output/Ground Core/E-pad all connect to Common Ground
11	VDD Core	Supply voltage system core - must be connected to VDD Output
12	Ground Core	Ground Output/Ground Core/E-pad all connect to Common Ground

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