# U2BFCC/10/6 Switching voltage regulator(SVR) guideline

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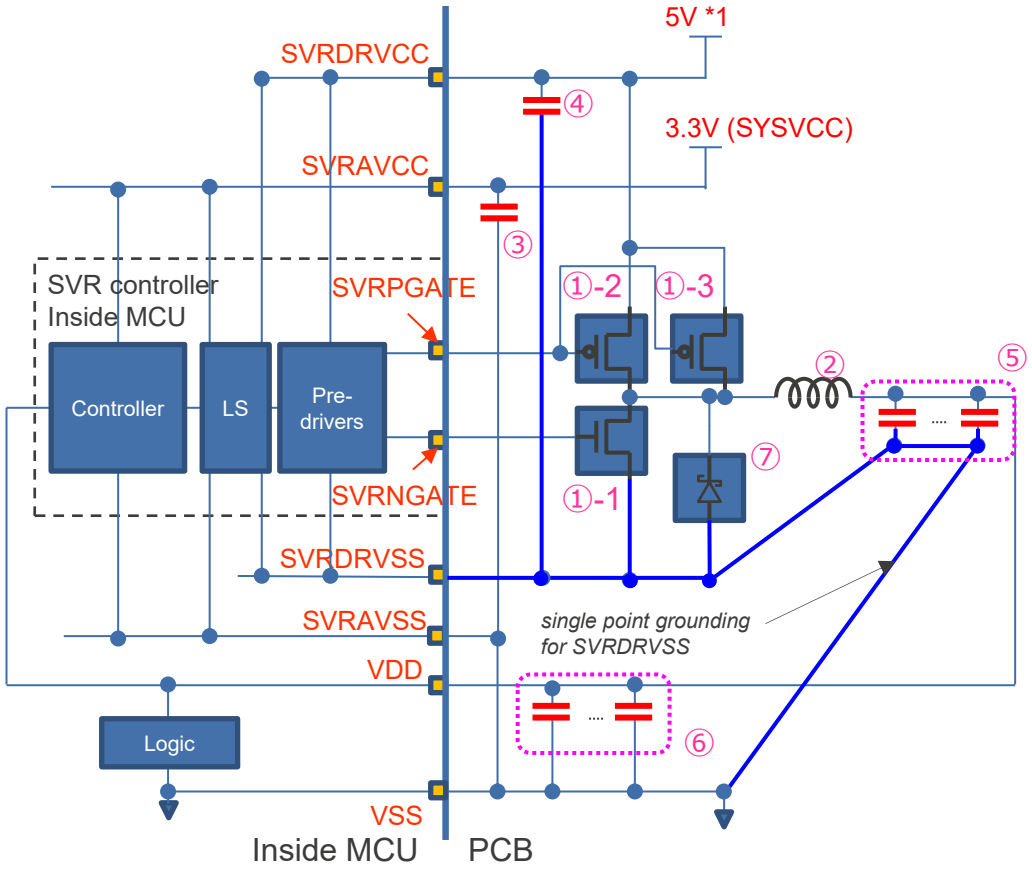
# U2BFCC/10/6 SVR circuit

## Case1: SVRDRVCC=5V and SYSVCC=VCC=SVRAVCC=3.3V

Comply with the guidelines below in mounting to obtain a VDD within the specified range if you are using a Target MOSFETs as an SVR drivers to handle the VDD power supply. However, the guidelines specifically apply when the SVR is that stated above. Using a different transistor will require separate detailed consideration.




| Item | # | Reference value (typ.) | Note | Placement |
|---|---|---|---|---|
| MOSFET | ① | See page 5 | Target MOSFETs is shown on page 5. | Close to SVRPGATE and SVRNGATE pin of MCU. Connect Pch MOSFET's source to SVRDRVCC. Connect Nch MOSFET's source to SVRDRVSS. |
| Inductor | ② | See page 6 | DC Resistance(DCR) ≦ 40mΩ | Close to MOSFET |
| Capacitor (between SVRAVCC and SVRAVSS) | ③ | 1uF | Capacitance tolerance: ±10%, Temperature characteristics: X7R, X8R, ESR: <50 mΩ | Close to SVRAVCC and SVRAVSS pin of MCU |
| Capacitor (between SVRDRVCC and SVRDRVSS) | ④ | ≥ 24.1uF | Capacitance tolerance: ±10%, Temperature characteristics: X7R, X8R, ESR <10 mΩ (@0.1MHz to 5MHz, total value of parts) | Close to SVRDRVCC and SVRDRVSS pin of MCU |
| Capacitor (between VDD and SVRDRVSS) | ⑤ | See page 6 | Capacitance tolerance: ±10%, Temperature characteristics: X7R, X8R, ESR <10 mΩ (@0.1MHz to 5MHz, total value of parts) | Close to Inductor |
| Capacitor (between VDD and VSS) | ⑥ | ≥ 0.1uF x 8 | Capacitance tolerance: ±10%, Temperature characteristics: X7R, X8R, ESR: <50 mΩ | Close to thermal ball of MCU (opposite side of MCU of PCB) |
| Schottky diode | ⑦ | See page 5 | Target Schottky diode is shown on page 7. | Close to N-ch MOSFET(①-1) |

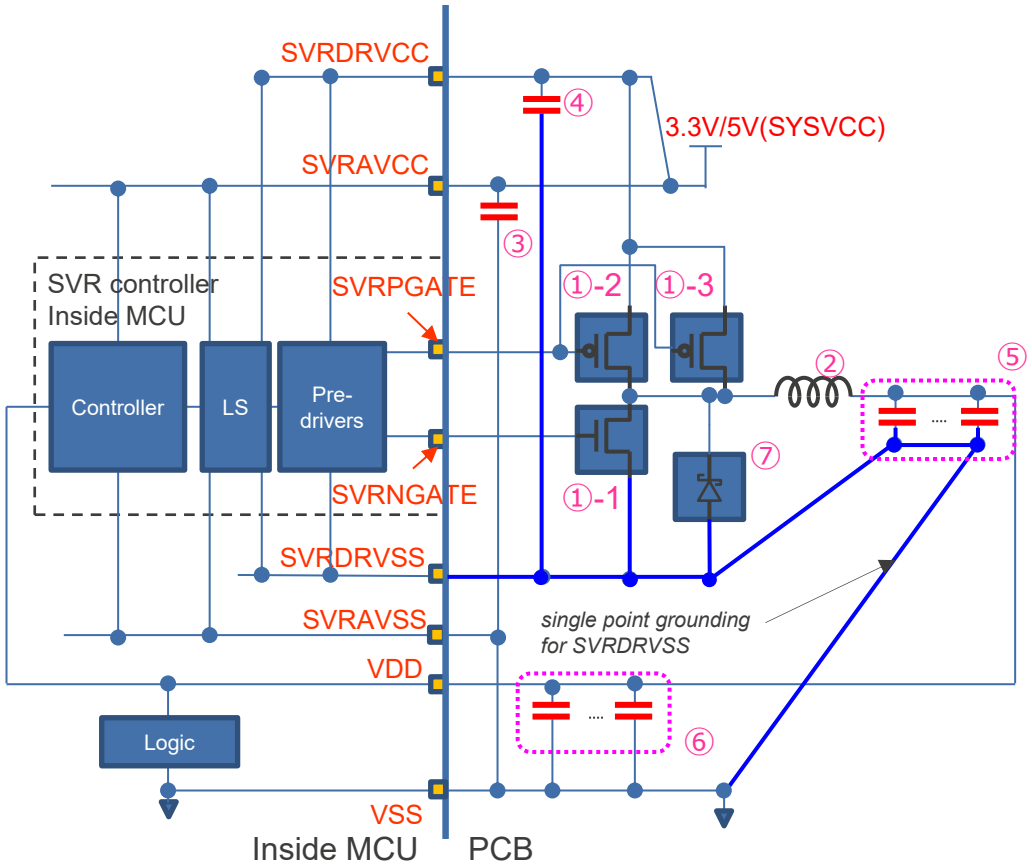
CAUTION

1. Load transient current of VDD (dI) should be kept the specification. Please refer the user's manual.
2. SVRDRVCC and SVRDRVSS should be separated from other power/ground for EMC improving. (e.g., single point grounding)
3. Output resistance and dead time of SVRPGATE and SVRNGATE can be configured by option byte settings. Please refer the user's manual.

# U2BFCC/10/6 SVR circuit

## Case2: SVRDRVCC=SYSVCC=VCC=SVRAVCC=3.3V/5V

Comply with the guidelines below in mounting to obtain a VDD within the specified range if you are using a Target MOSFETs as an SVR drivers to handle the VDD power supply. However, the guidelines specifically apply when the SVR is that stated above. Using a different transistor will require separate detailed consideration.




| Item | # | Reference value (typ.) | Note | Placement |
|---|---|---|---|---|
| MOSFET | ① | See page 5 | Target MOSFETs is shown on page 5. | Close to SVRPGATE and SVRNGATE pin of MCU. Connect Pch MOSFET's source to SVRDRVCC. Connect Nch MOSFET's source to SVRDRVSS. |
| Inductor | ② | See page 6 | DC Resistance(DCR) ≦ 40mΩ | Close to MOSFET |
| Capacitor (between SVRAVCC and SVRAVSS) | ③ | 1uF | Capacitance tolerance: ±10%, Temperature characteristics: X7R, X8R, ESR: <50 mΩ | Close to SVRAVCC and SVRAVSS pin of MCU |
| Capacitor (between SVRDRVCC and SVRDRVSS) | ④ | ≥ 24.1uF | Capacitance tolerance: ±10%, Temperature characteristics: X7R, X8R, ESR <10 mΩ (@0.1MHz to 5MHz, total value of parts) | Close to SVRDRVCC and SVRDRVSS pin of MCU |
| Capacitor (between VDD and SVRDRVSS) | ⑤ | See page 6 | Capacitance tolerance: ±10%, Temperature characteristics: X7R, X8R, ESR <10 mΩ (@0.1MHz to 5MHz, total value of parts) | Close to Inductor |
| Capacitor (between VDD and VSS) | ⑥ | ≥ 0.1uF x 8 | Capacitance tolerance: ±10%, Temperature characteristics: X7R, X8R, ESR: <50 mΩ | Close to thermal ball of MCU (opposite side of MCU of PCB) |
| Schottky diode | ⑦ | See page 5 | Target Schottky diode is shown on page 7. | Close to N-ch MOSFET(①-1) |

CAUTION

1. Load transient current of VDD (dI) should be kept the specification. Please refer the user's manual.
2. SVRDRVCC and SVRDRVSS should be separated from other power/ground for EMC improving. (e.g., single point grounding)
3. Output resistance and dead time of SVRPGATE and SVRNGATE can be configured by option byte settings. Please refer the user's manual.

# ①MOSFETs

The following table shows the combinations used for evaluation.

| # | Type | Supplier | MOSFET | Id (absolute maximum rating) [A] | Rdson (Vgs=4.5V) [mOhm] | | Vth [V] | Ciss [pF] | Crss [pF] | Conditions |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Max | Typ | Max | Max | Typ | Typ | |
| ①-1 | Nch | Vishay | SQS420EN | 8 | 24 | 28 | 1.5 | 392 | 40 | SVRDRVCC=3.3V |
| | | | SQS460EN | 8 | 30 | 36 | 2.5 | 603 | 50 | SVRDRVCC=5V |
| ①-2 | Pch | | SQ3425EV | -4.3 | 49 | 60 | -1.4 | 560 | 126 | SVRDRVCC=3.3V/5V |
| ①-1 | Nch | Nexperia | PMPB20XNEA | 4.8 | 16 | 20 | 1.25 | 930 | 144 | SVRDRVCC=3.3V |
| | | | BUK9D23-40E | 12 | 22 | 30 | 2.1 | 637 | 52 | SVRDRVCC=5V |
| ①-2, ①-3 | Pch | | PMV30XPEA | -2.8 *2 | 28 | 34 | -1.25 | 1465 | 133 | SVRDRVCC=3.3V/5V |

For details of MOSFET, please contact each supplier.

Note1: If prefer using the different transistor other than the above, please choose the transistor as equivalent as the above each specification, and fully evaluate and judge by customer liability.

Note2: Two Pch MOSFETs are required when the ISOVDD current consumption of MCU exceed the Id of absolute maximum rating of Pch MOSFET on use case. Therefore, U2B6 does not require the Pch MOSFET of ①-3.

# ②⑤Configuration of Lout and Cout for U2BFCC

The following table shows the four combinations（a, b, c and d）used for evaluation.

| | Value | Recommended parts, Supplier | a | b | c | d |
|---|---|---|---|---|---|---|
| Switching frequency (Option byte) | - | - | 465kHz | 930kHz | 1.42MHz | 2.1MHz |
| ②Inductor (Lout) | 4.7uH | SPM6545VT- 4R7M-D, TDK or ETQP4M4R7KVK, Panasonic | ✓ | N/A | N/A | N/A |
| | 2.2uH | SPM5030VT- 2R2M-D, TDK or ETQP3M2R2KVN, Panasonic | N/A | ✓ | N/A | N/A |
| | 1.5uH | SPM5030VT- 1R5M-D, TDK or ETQP3M1R5KVP, Panasonic | N/A | N/A | ✓ | N/A |
| | 1uH | SPM5030VT- 1R0M-D ,TDK or ETQP3M1R0KVP, Panasonic | N/A | N/A | N/A | ✓ |
| ⑤Capacitor (between VDD and VSS) (Cout) | 10uF | GCM32ER71E106KA57, Murata | N/A | N/A | N/A | N/A |
| | 22uF | GCM32ER71A226KE12, Murata | N/A | 1pcs | 4pcs | 3pcs |
| | 47uF | GCM32ER70J476ME19, Murata (*1) GCM32ER70J476KE19, Murata (*1) | 4pcs | 2pcs | N/A | N/A |
| | Total | | ≧ 188uF | ≧ 116uF | ≧ 88uF | ≧ 66uF |

Note 1: GCM32ER70J476KE19 (capacitance tolerance: ±10%) is highly recommended in severe conditions (e.g., high temperature and/or full operating load)
Note: For details of Inductor and Capacitor, please contact each supplier.

# ②⑤Configuration of Lout and Cout for U2B10

The following table shows the four combinations（a, b1, b2, c and d）used for evaluation.

| | Value | Recommended parts, Supplier | a | b1 | b2 | c | d |
|---|---|---|---|---|---|---|---|
| SVRDRVCC voltage | - | - | 3.3V/5V | 3.3V | 5V | 3.3V/5V | 3.3V/5V |
| Switching frequency (Option byte) | - | - | 465kHz | 930kHz | 930kHz | 1.42MHz | 2.1MHz |
| ②Inductor (Lout) | 4.7uH | SPM6545VT- 4R7M-D, TDK or ETQP4M4R7KVK, Panasonic | ✓ | N/A | N/A | N/A | N/A |
| | 2.2uH | SPM5030VT- 2R2M-D, TDK or ETQP3M2R2KVN, Panasonic | N/A | ✓ | ✓ | N/A | N/A |
| | 1.5uH | SPM5030VT- 1R5M-D, TDK or ETQP3M1R5KVP, Panasonic | N/A | N/A | N/A | ✓ | N/A |
| | 1uH | SPM5030VT- 1R0M-D ,TDK or ETQP3M1R0KVP, Panasonic | N/A | N/A | N/A | N/A | ✓ |
| ⑤Capacitor (between VDD and VSS) (Cout) | 10uF | GCM32ER71E106KA57, Murata | N/A | N/A | N/A | N/A | N/A |
| | 22uF | GCM32ER71A226KE12, Murata | N/A | N/A | 1pcs | 4pcs | 3pcs |
| | 47uF | GCM32ER70J476ME19, Murata (*1)<br>GCM32ER70J476KE19, Murata (*1) | 4pcs | 3pcs | 2pcs | N/A | N/A |
| | Total | | ≧ 188uF | ≧ 141uF | ≧ 116uF | ≧ 88uF | ≧ 66uF |

Note 1: GCM32ER70J476KE19 (capacitance tolerance: ±10%) is highly recommended in severe conditions (e.g., high temperature and/or full operating load)
Note: For details of Inductor and Capacitor, please contact each supplier.

# ②⑤Configuration of Lout and Cout for U2B6

The following table shows the four combinations（a, b, c and d）used for evaluation.

| | Value | Recommended parts, Supplier | a | b | c | d |
|---|---|---|---|---|---|---|
| Switching frequency (Option byte) | - | - | 465kHz | 930kHz | 1.42MHz | 2.1MHz |
| ②Inductor (Lout) | 6.8uH | SPM6545VT- 6R8M-D, TDK or ETQP3M6R8KVN, Panasonic | N/A | N/A | N/A | N/A |
| | 4.7uH | SPM5030VT- 4R7M-D, TDK or ETQP3M4R7KVP, Panasonic | ✓ | N/A | N/A | N/A |
| | 2.2uH | SPM5030VT- 2R2M-D, TDK or ETQP3M2R2KVP, Panasonic | N/A | ✓ | N/A | N/A |
| | 1.5uH | SPM5030VT- 1R5M-D, TDK or ETQP3M1R5KVP, Panasonic | N/A | N/A | ✓ | N/A |
| | 1uH | SPM5030VT- 1R0M-D ,TDK or ETQP3M1R0KVP, Panasonic | N/A | N/A | N/A | ✓ |
| ⑤Capacitor (between VDD and VSS) (Cout) | 10uF | GCM32ER71E106KA57, Murata | N/A | N/A | N/A | N/A |
| | 22uF | GCM32ER71A226KE12, Murata | 1pcs | 4pcs | 3pcs | 3pcs |
| | 47uF | GCM32ER70J476ME19, Murata (*1)<br>GCM32ER70J476KE19, Murata (*1) | 2pcs | N/A | N/A | N/A |
| | Total | | ≧ 110uF | ≧ 88uF | ≧ 66uF | ≧ 66uF |

Note 1: GCM32ER70J476KE19 (capacitance tolerance: ±10%) is highly recommended in severe conditions (e.g., high temperature and/or full operating load)

Note: For details of Inductor and Capacitor, please contact each supplier.

# ⑦Schottky diode

The following table shows the parts used for evaluation.

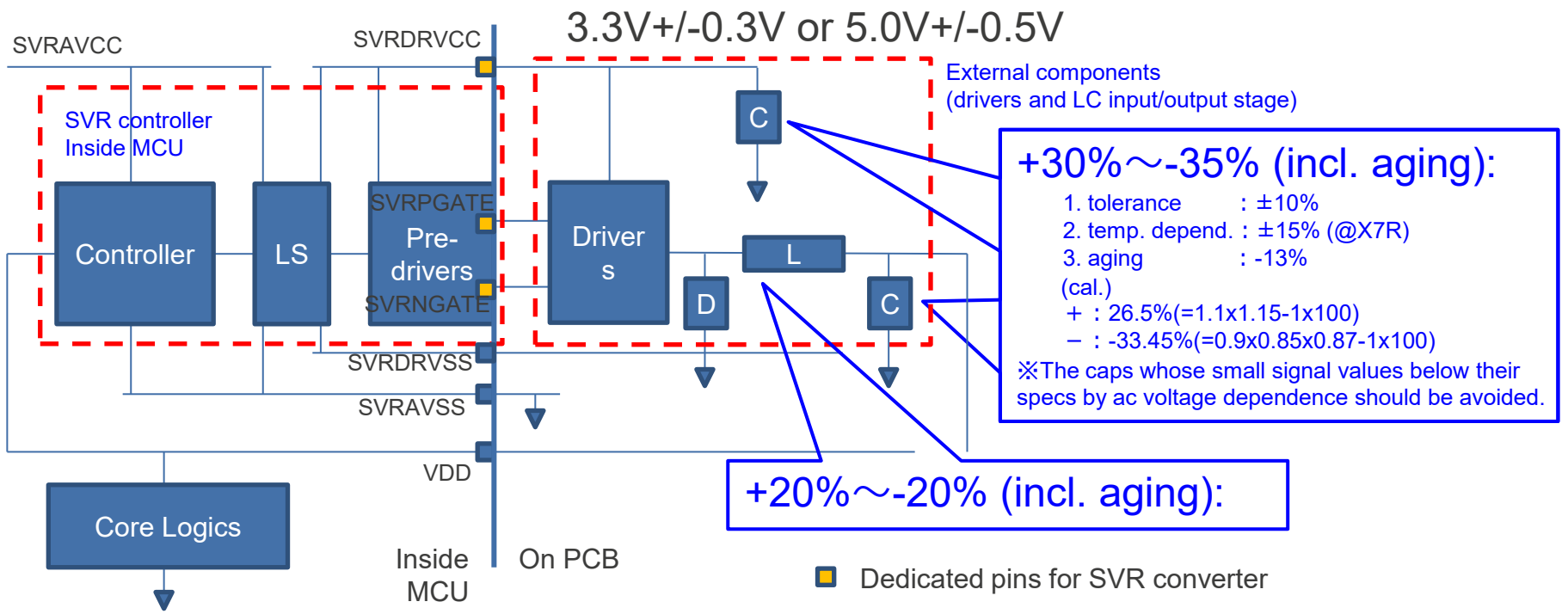
| # | Type | Supplier | DIODE | | | |
|---|---|---|---|---|---|---|
| | | | | $I_{F\ (AV)}$ [A] | $V_R$ [V] | $V_F$ (@IF=3A, 25℃) [mV] |
| | | | | Max | Max | Max |
| ⑦ | Schottky diode | Nexperia | PMEG6030ETP | 3 | 60 | 530 |

For details of diode, please contact each supplier.

Note1:
If prefer using the different diode other than the above, please choose the diode as equivalent as the above each specification, and fully evaluate and judge by customer liability.

Note2:
Used when necessary for improving power efficiency and measures against heat generation of Nch MOSFET.

# L,C variations acceptable for SVR



# Option byte settings for U2BFCC

Table 1: Option byte settings are fixed values for each configurations (SVRDRVCC, Fsw, Cout, Lout).
Table 2:

- Adjusting SVRAJPRDSR[3:0] considering the trade-off between efficiency and noise reduction.
  SVRAJPRDSR[3:0]=4‘b0111(SVRDRVCC=5V),4'b1111(SVRDRVCC=3.3V) are good starting points for the gate driver strength setting.
- Adjusting SVRAJDTP [2:0] and SVRAJDTN [2:0] to match the MOSFET can optimize efficiency.
  Please refer to the following page.

Table1 Option byte for PID, internal ADC and output pulse width setting

| Configurations | | | | Option byte setting | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SVRDRVCC [V] | Fsw [MHz] | Cout [uF] | Lout [uH] | SVRFSWMODE[1:0] | SVRKPVSCL[13:0] | SVRKIVSCL[13:0] | SVRKDVSCL[13:0] | SVRADNSMP[7:0] | SVRADTHRESH[7:0] | SVRADTHRESHE[7:0] | SVRMINSKIPDUTY[1:0] | SVRMAXDUTY[7:0] |
| 5 | 0.465 | 188 | 4.7 | 2'b00 | 14'b00010111101111 | 14'b00100111110010 | 14'b00010101001010 | 8'b00010000 | 8'b10101010 | 8'b11111001 | 2'b11 | 8'b11111100 |
| 5 | 0.930 | 116 | 2.2 | 2'b01 | 14'b00010100111101 | 14'b00100000011010 | 14'b00010100001110 | 8'b00010000 | 8'b00101010 | 8'b01111001 | 2'b11 | 8'b01111100 |
| 5 | 1.42 | 88 | 1.5 | 2'b10 | 14'b00010101000101 | 14'b00011100010001 | 14'b00010111011111 | 8'b00010000 | 8'b00101010 | 8'b00100101 | 2'b00 | 8'b01010000 |
| 5 | 2.1 | 66 | 1.0 | 2'b11 | 14'b00001110111100 | 14'b00001111000001 | 14'b00010110001100 | 8'b00001010 | 8'b00101000 | 8'b11111001 | 2'b00 | 8'b00111110 |
| 3.3 | 0.465 | 188 | 4.7 | 2'b00 | 14'b00100100010010 | 14'b00111100110010 | 14'b00100000010100 | 8'b00010000 | 8'b10101010 | 8'b11111001 | 2'b11 | 8'b11111100 |
| 3.3 | 0.930 | 116 | 2.2 | 2'b01 | 14'b00100000000001 | 14'b00110001100001 | 14'b00011110111001 | 8'b00010000 | 8'b00000011 | 8'b01010010 | 2'b11 | 8'b01111100 |
| 3.3 | 1.42 | 88 | 1.5 | 2'b10 | 14'b00011100010100 | 14'b00100011100101 | 14'b00100001101000 | 8'b00010000 | 8'b00101110 | 8'b00101001 | 2'b00 | 8'b01010000 |
| 3.3 | 2.1 | 66 | 1.0 | 2'b11 | 14'b00011111100111 | 14'b00100101011001 | 14'b00100111111001 | 8'b00001010 | 8'b00101000 | 8'b11111001 | 2'b00 | 8'b00111110 |

Table2 Option byte for gate driver

| Option byte setting | | | | |
|---|---|---|---|---|
| SVRAJPRDSR[5:0] | SVRAJDTP[2:0] | SVRAJDTN[2:0] | SVRENSSCG | SVRAJSSCGD[1:0] |
| Please refer “Option byte settings [3/3]” | | | | |

# Option byte settings for U2B10

Table 1: Option byte settings are fixed values for each configurations (SVRDRVCC, Fsw, Cout, Lout).
Table 2:

- Adjusting SVRAJPRDSR[3:0] considering the trade-off between efficiency and noise reduction.
  SVRAJPRDSR[3:0]=4‘b0111(SVRDRVCC=5V),4'b1111(SVRDRVCC=3.3V) are good starting points for the gate driver strength setting.
- Adjusting SVRAJDTP [2:0] and SVRAJDTN [2:0] to match the MOSFET can optimize efficiency.
  Please refer to the following page.

Table1 Option byte for PID, internal ADC and output pulse width setting

| Configurations | | | | Option byte setting | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SVRDRVCC [V] | Fsw [MHz] | Cout [uF] | Lout [uH] | SVRFSWMODE[1:0] | SVRKPVSCL[13:0] | SVRKIVSCL[13:0] | SVRKDVSCL[13:0] | SVRADNSMP[7:0] | SVRADTHRESH[7:0] | SVRADTHRESHE[7:0] | SVRMINSKIPDUTY[1:0] | SVRMAXDUTY[7:0] |
| 5 | 0.465 | 188 | 4.7 | 2'b00 | 14'b00010111101111 | 14'b00100111110010 | 14'b00010101001010 | 8'b00010000 | 8'b10101010 | 8'b11111001 | 2'b11 | 8'b11111100 |
| 5 | 0.930 | 116 | 2.2 | 2'b01 | 14'b00010100111101 | 14'b00100000011010 | 14'b00010100001110 | 8'b00010000 | 8'b00101010 | 8'b01111001 | 2'b11 | 8'b01111100 |
| 5 | 1.42 | 88 | 1.5 | 2'b10 | 14'b00010101000101 | 14'b00011100010001 | 14'b00010111011111 | 8'b00010000 | 8'b00101010 | 8'b00100101 | 2'b00 | 8'b01010011 |
| 5 | 2.1 | 66 | 1.0 | 2'b11 | 14'b00010100101100 | 14'b00011000011110 | 14'b00011010000111 | 8'b00001010 | 8'b00101000 | 8'b11111001 | 2'b00 | 8'b00111110 |
| 3.3 | 0.465 | 188 | 4.7 | 2'b00 | 14'b00100100010010 | 14'b00111100110010 | 14'b00100000010100 | 8'b00010000 | 8'b10101010 | 8'b11111001 | 2'b11 | 8'b11111100 |
| 3.3 | 0.930 | 141 | 2.2 | 2'b01 | 14'b00100000100110 | 14'b00101011101101 | 14'b00100100010100 | 8'b00010000 | 8'b01110111 | 8'b01000110 | 2'b11 | 8'b01111100 |
| 3.3 | 1.42 | 88 | 1.5 | 2'b10 | 14'b00011100010100 | 14'b00100011100101 | 14'b00100001101000 | 8'b00010000 | 8'b00101110 | 8'b00101001 | 2'b00 | 8'b01010011 |
| 3.3 | 2.1 | 66 | 1.0 | 2'b11 | 14'b00011111100111 | 14'b00100101011001 | 14'b00100111111001 | 8'b00001010 | 8'b00101000 | 8'b11111001 | 2'b00 | 8'b00111110 |

Table2 Option byte for gate driver

| Option byte setting | | | | |
|---|---|---|---|---|
| SVRAJPRDSR[5:0] | SVRAJDTP[2:0] | SVRAJDTN[2:0] | SVRENSSCG | SVRAJSSCGD[1:0] |
| Please refer “Option byte settings [3/3]” | | | | |

# Option byte settings for U2B6

Table 1: Option byte settings are fixed values for each configurations (SVRDRVCC, Fsw, Cout, Lout).
Table 2:

- Adjusting SVRAJPRDSR[3:0] considering the trade-off between efficiency and noise reduction.
  SVRAJPRDSR[3:0]=4'b0101(SVRDRVCC=5V),4'b1111(SVRDRVCC=3.3V) are good starting points for the gate driver strength setting.
- Adjusting SVRAJDTP [2:0] and SVRAJDTN [2:0] to match the MOSFET can optimize efficiency.
  Please refer to the following page.

Table1 Option byte for PID, internal ADC and output pulse width setting

| Configurations | | | | Option byte setting | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SVRDRVCC [V] | Fsw [MHz] | Cout [uF] | Lout [uH] | SVRFSWMODE[1:0] | SVRKPVSCL[13:0] | SVRKIVSCL[13:0] | SVRKDVSCL[13:0] | SVRADNSMP[7:0] | SVRADTHRESH[7:0] | SVRADTHRESHE[7:0] | SVRMINSKIPDUTY[1:0] | SVRMAXDUTY[7:0] |
| 5 | 0.465 | 110 | 4.7 | 2'b00 | 14'b00001101111001 | 14'b00010111010010 | 14'b00001100011000 | 8'b00010000 | 8'b10101010 | 8'b11111001 | 2'b11 | 8'b11111100 |
| 5 | 0.930 | 88 | 2.2 | 2'b01 | 14'b00010001101110 | 14'b00011011011011 | 14'b00010001000111 | 8'b00010000 | 8'b00101010 | 8'b01111001 | 2'b11 | 8'b01111100 |
| 5 | 1.42 | 66 | 1.5 | 2'b10 | 14'b00001111110100 | 14'b00010101001100 | 14'b00010001100111 | 8'b00010000 | 8'b00101010 | 8'b00100101 | 2'b00 | 8'b01010011 |
| 5 | 2.1 | 66 | 1.0 | 2'b11 | 14'b00001110111100 | 14'b00001111000001 | 14'b00010110001100 | 8'b00001010 | 8'b00101000 | 8'b11111001 | 2'b00 | 8'b00111110 |
| 3.3 | 0.465 | 110 | 4.7 | 2'b00 | 14'b00010101001110 | 14'b00100011100100 | 14'b00010010111010 | 8'b00010000 | 8'b10101010 | 8'b11111001 | 2'b11 | 8'b11111100 |
| 3.3 | 0.930 | 88 | 2.2 | 2'b01 | 14'b00010100010110 | 14'b00011011010001 | 14'b00010110101010 | 8'b00010000 | 8'b01110111 | 8'b01000110 | 2'b11 | 8'b01111100 |
| 3.3 | 1.42 | 66 | 1.5 | 2'b10 | 14'b00010101001111 | 14'b00011010101100 | 14'b00011001001110 | 8'b00010000 | 8'b00101110 | 8'b00101001 | 2'b00 | 8'b01010011 |
| 3.3 | 2.1 | 66 | 1.0 | 2'b11 | 14'b00011111100111 | 14'b00100101011001 | 14'b00100111111001 | 8'b00001010 | 8'b00101000 | 8'b11111001 | 2'b00 | 8'b00111110 |

Table2 Option byte for gate driver

| Option byte setting | | | | |
|---|---|---|---|---|
| SVRAJPRDSR[5:0] | SVRAJDTP[2:0] | SVRAJDTN[2:0] | SVRENSSCG | SVRAJSSCGD[1:0] |
| Please refer “Option byte settings [3/3]” | | | | |

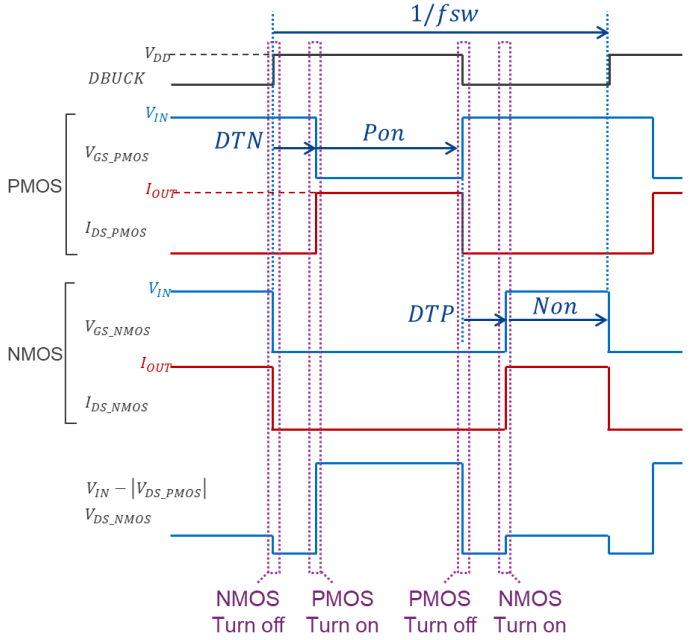
# Option byte settings

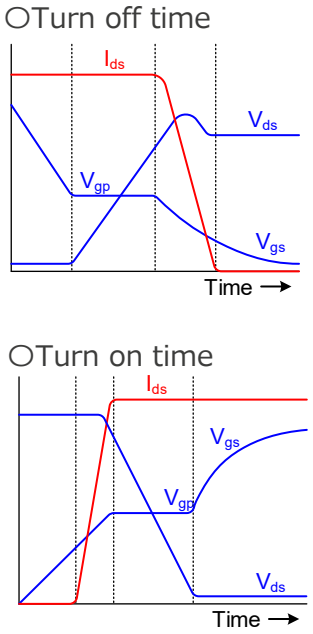
In order to avoid excessive current, the switching timing of MOSFETs should be controlled to have non-overlap time between the on-times of Hi-side(PMOS) and Lo-side(NMOS). So dead time should be set to satisfy the following relations.

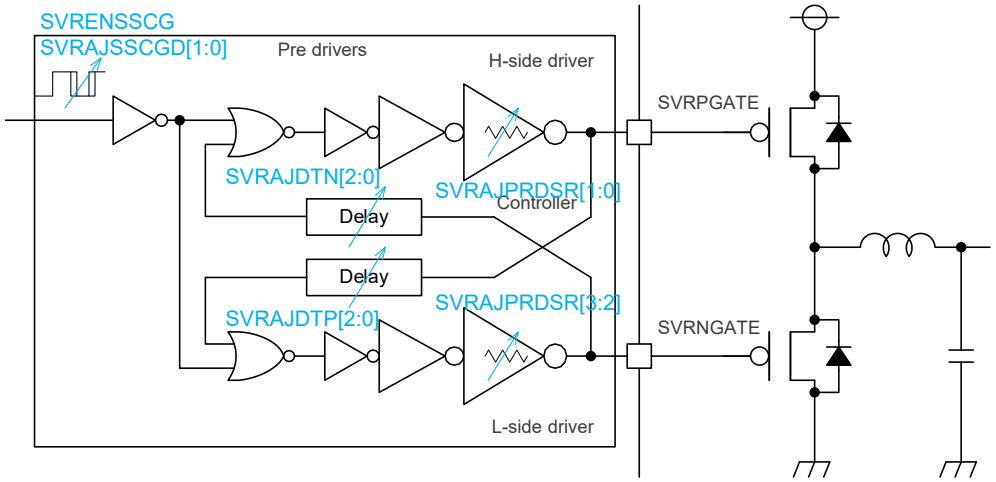
Dead time of Hi-side:OFF->Lo-side:ON min > PMOS Turn off time max

Dead time of Lo-side:OFF->Hi-side:ON min > NMOS Turn off time max

Regarding the turn off time of MOSFETs, could you please get their information from the MOSFETs supplier you choose.




Note: Relation of 1/fsw, DTN, DTP, Pon and Non are follows.

- 1/fsw, DTN and DTP: fixed value by each OPBT settings.
- Pon and Non: Variable with ISOVDD current.
- Non = 1/fsw – (Pon + DTN +DTP)

# Option byte settings

Table2 Option byte for output resistance of gate driver

| # | Pin conditions SVRAJPRDSR[5:0] [5:4] = 2'b10 (fix) [3:2] for SVRNGATE [1:0] for SVRPGATE | Output resistance [ohm] | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | VCC=3.0 to 3.6[V] (@Vds=1.0V) | | | | | | VCC=4.5 to 5.5[V] (@Vds=2.5V) | | | | | |
| | | PMOS (pull-up) | | | NMOS (pull-down) | | | PMOS (pull-up) | | | NMOS (pull-down) | | |
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |
| 1 | 4'b1111 | 1.4 | 1.7 | 2.5 | 1.4 | 1.7 | 2.5 | 1.3 | 1.6 | 2.3 | 1.3 | 1.6 | 2.3 |
| 2 | 4'b1010 | 2.0 | 2.7 | 4.3 | 2.0 | 2.7 | 4.3 | 1.9 | 2.5 | 3.9 | 1.9 | 2.5 | 3.9 |
| 3 | 4'b0101 | 3.3 | 4.6 | 7.8 | 3.3 | 4.6 | 7.8 | 3.3 | 4.5 | 7.2 | 3.3 | 4.5 | 7.2 |
| 4 | 4'b0000 | 11.2 | 16.4 | 28.9 | 11.2 | 16.4 | 28.9 | 12.0 | 16.9 | 27.7 | 12.3 | 16.9 | 27.7 |

Table3 Option byte for dead time of gate driver for Switching frequency = 0.465M, 0.930M and 1.42MHz

| # | Pin conditions SVRAJDTP[2:0] SVRAJDTN[2:0] | Dead time [ns] | | | | | |
|---|---|---|---|---|---|---|---|
| | | VCC=3.0 to 3.6[V] | | | VCC=4.5 to 5.5[V] | | |
| | | Min | Typ | Max | Min | Typ | Max |
| 1 | 3'b000 | 33 | 42 | 53 | 33 | 42 | 53 |
| 2 | 3'b001 | 41 | 51 | 64 | 41 | 51 | 62 |
| 3 | 3'b010 | 49 | 60 | 74 | 50 | 60 | 74 |
| 4 | 3'b011 | 57 | 69 | 85 | 58 | 69 | 83 |
| 5 | 3'b100 | 80 | 96 | 117 | 81 | 96 | 116 |
| 6 | 3'b101 | 104 | 123 | 149 | 104 | 123 | 147 |
| 7 | 3'b110 | 151 | 177 | 212 | 151 | 177 | 211 |
| 8 | 3'b111 | 198 | 231 | 276 | 198 | 231 | 274 |

Table4 Option byte for dead time of gate driver for Switching frequency = 2.1MHz

| # | Pin conditions SVRAJDTP[2:0] SVRAJDTN[2:0] | Dead time [ns] | | | | | |
|---|---|---|---|---|---|---|---|
| | | VCC=3.0 to 3.6[V] | | | VCC=4.5 to 5.5[V] | | |
| | | Min | Typ | Max | Min | Typ | Max |
| 1 | 3'b000 | 25 | 34 | 44 | 27 | 34 | 42 |
| 2 | 3'b001 | 31 | 41 | 53 | 33 | 41 | 50 |
| 3 | 3'b010 | 38 | 49 | 61 | 39 | 49 | 60 |
| 4 | 3'b011 | 44 | 56 | 70 | 46 | 57 | 69 |
| 5 | 3'b100 | 64 | 78 | 96 | 66 | 79 | 95 |
| 6 | 3'b101 | 83 | 101 | 123 | 85 | 101 | 121 |
| 7 | 3'b110 | 122 | 145 | 175 | 124 | 146 | 173 |
| 8 | 3'b111 | 161 | 190 | 228 | 163 | 190 | 226 |

Table5 Option byte for SSCG range of gate driver for Switching frequency = 0.465M, 0.930M and 1.42MHz

| # | Pin conditions SVRAJSSCGD[1:0] | Frequency dithering range [%] | | |
|---|---|---|---|---|
| | | Min | Typ | Max |
| 1 | 2'b00 | - | - | 5 |
| 2 | 2'b01 | - | - | 9 |
| 3 | 2'b10 | Setting prohibited | | |
| 4 | 2'b11 | | | |

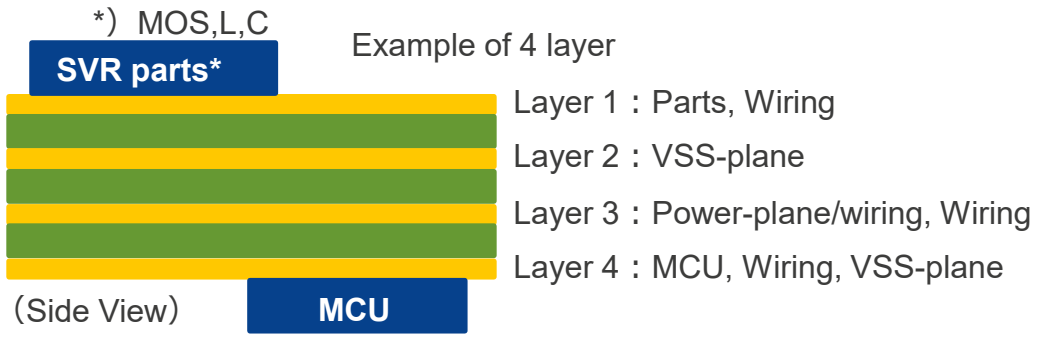
Table6 Option byte for SSCG range of gate driver for Switching frequency = 2.1MHz

| # | Pin conditions SVRAJSSCGD[1:0] | Frequency dithering range [%] | | |
|---|---|---|---|---|
| | | Min | Typ | Max |
| 1 | 2'b00 | - | - | 6 |
| 2 | 2'b01 | Setting prohibited | | |
| 3 | 2'b10 | | | |
| 4 | 2'b11 | | | |

Note: The values in the tables are simulation results and are not guaranteed.

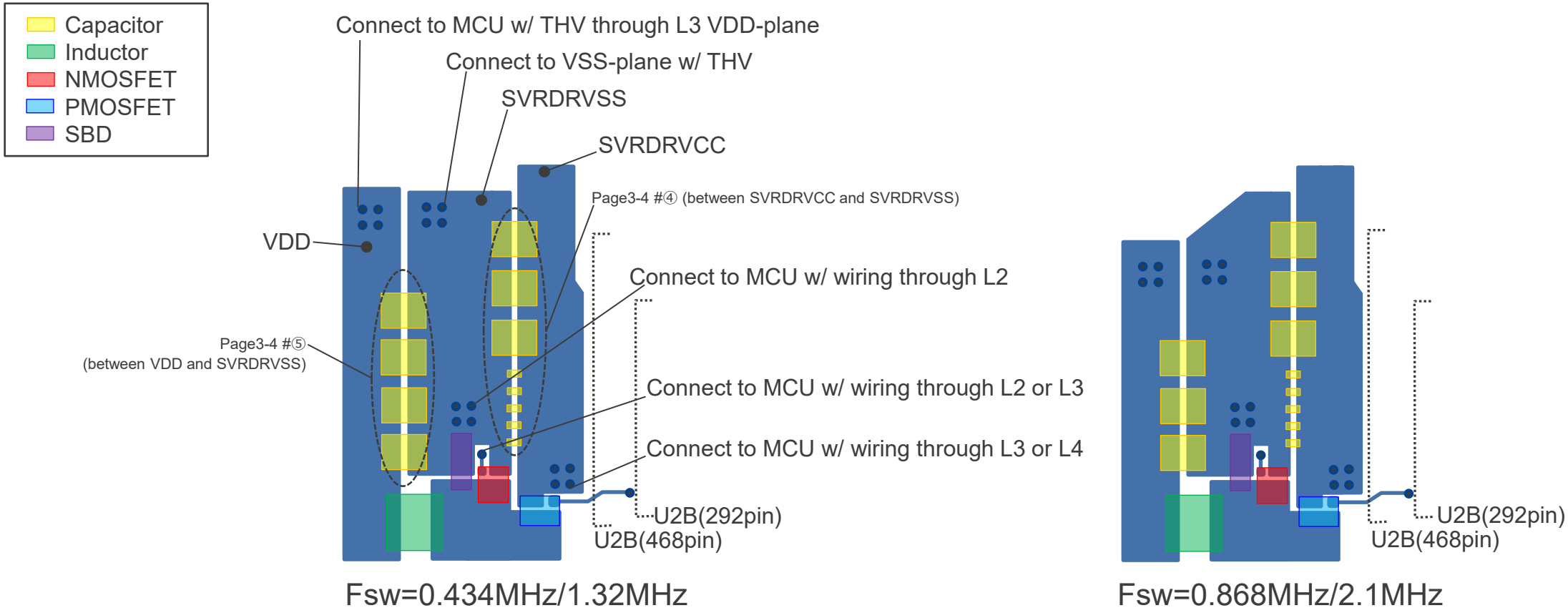
# PCB layout guideline [1/5]

## Example of PCB structure and conductive layer arrangement



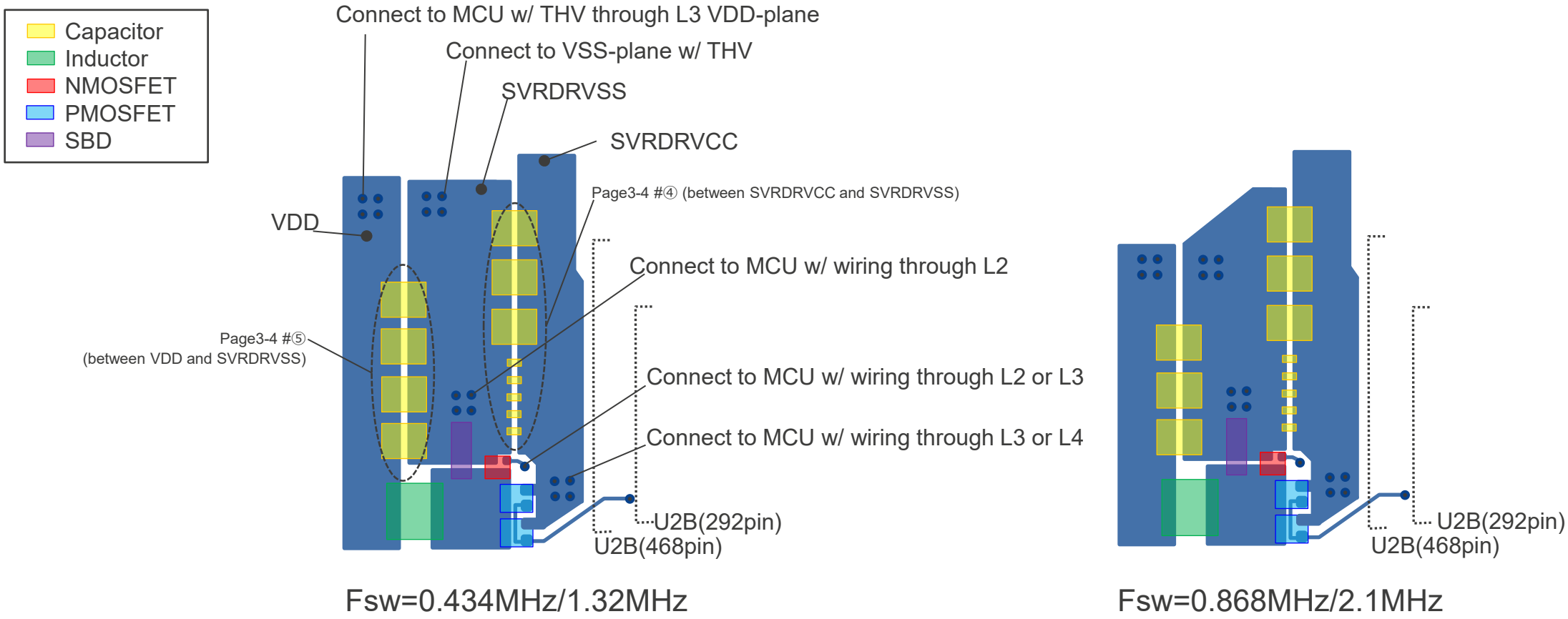
# PCB layout guideline [2/5]

## Example of PCB layout for MOSFETs(SQS420EN/SQ3425EV) of Vishay



# PCB layout guideline [3/5]

## Example of PCB layout for MOSFETs(PMPB20XNEA/PMV30XPEA) of Nexperia



# PCB layout guideline [4/5]

## Recommended PCB design rule:

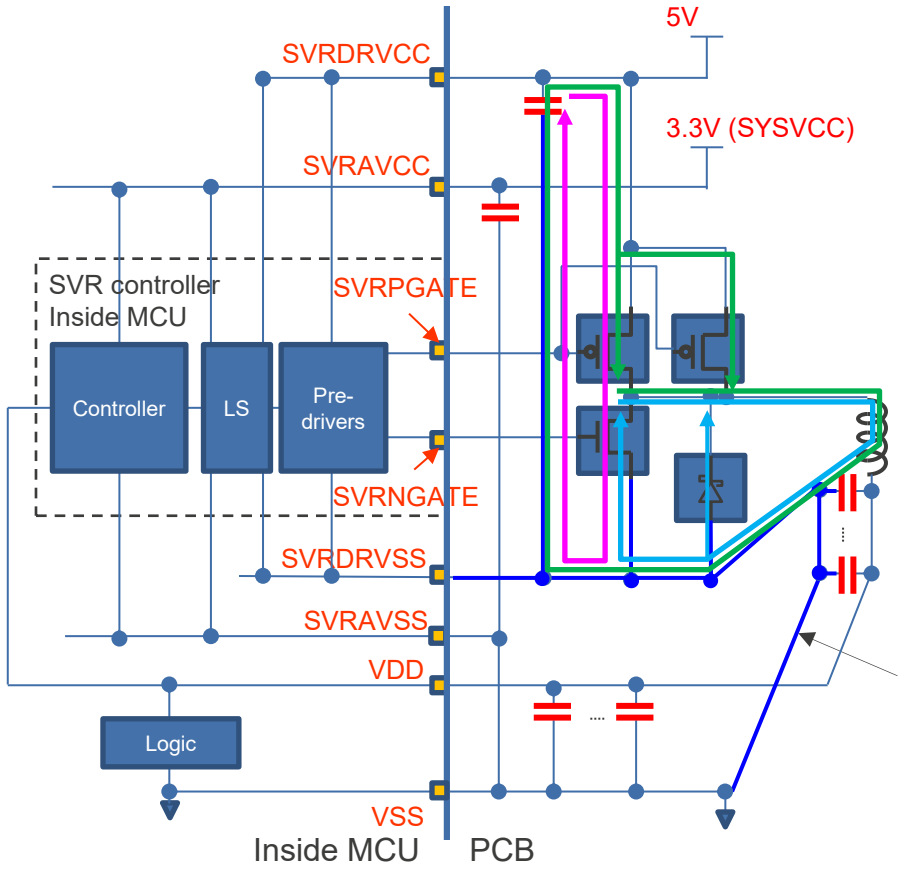
1) The part (C, MOS, L) of SVRDRVCC and the part (C) of VDD are arranged in the same layer (Layer 1). The distance between MOS and L, L and VDD-C should be within 3 mm each.
2) The VSS plane is arranged in the layer adjacent to the SVR part area (Layer 2) of Layer 1.
3) The MCU may be mounted on the same surface (Layer 1) as the component of the SVR.
4) Power supplies (including SVRAVCC) other than SVRDRVCC and VDD should be placed in the layer (Layer 3) between the VSS plane layer (Layer 2) and Layer 4.
5) In the case of a six-layer board, add two layers between Layer 3 (power supply wiring layer) and Layer 4. (eg Layer 3 = power supply, wiring, Layer 4 = VSS)
6) The pattern width of SVRDRVCC and VDD is 5 mm or more. The number of vias is 4 or more @ Φ0.6 mm (8 or more @ Φ0.3 mm).
7) Wiring the pattern width of SVRDRVSS at 1 mm or more. When the pattern width is less than 1 mm, it may be combined with the adjacent layer (eg Layer 1 = 0.5 mm, Layer 2 = 0.5 mm).
8) SVRDRVSS should be connected to VSS through via(4 or more @Φ0.6mm) of SVRDRVSS in the vicinity of C located far from L.
9) C between SVRDRVCC and SVRDRVSS is located close to the MCU from the small capacity C.
10) C of SVRAVCC and SVRAVSS are placed closest to MCU. SVRAVCC is connected to SYSVCC and VCC. SVRAVSS is connected to VSS.
11) SVRPGATE / N wiring, MOS, L, SVRDRVCC, SVRDRVSS should not run in the same layer / adjacent layer as analogue high-sensitivity wiring.

1)2)4)5)11) To prevent SVR noise from diffusing to other power supplies, analog wiring, etc.
3) When SVR components can be arranged from the MCU without using vias, MCU and SVR components may be the same layer. On the other hand, if it can not be arranged, the MCU and the SVR part are separate layers only.
6)7)8) The pattern width and the number of vias consider the current amount.
Estimated pattern width is 1 mm / 1A. As a measure of the number of vias, Φ 0.25 mm: 0.8 A / piece, Φ 0.5 mm: 1.6 A / piece, Φ 1 mm: 3.2 A / piece.
6)8) Noise of SVR is superimposed on SVRDRVSS. In order not to diffuse noise to VSS, noise is reduced with via (1.5 nH or less) and then connected to VSS.
9)10) A ceramic capacitor having a small capacitance value has a high self-resonant frequency. That is, high frequency noise suppression effect is high.
In order to maximize this effect, a ceramic capacitor is placed close to the MCU (reduces parasitic inductance of the wiring).

# PCB layout guideline [5/5]

## Miscellaneous:

1) Difference in HS/LS current loop area should be designed as small as possible*
*If you prefer something different from the transistors listed on page 5, please design the layout based on above for suppressing SVR noise.
2) Please note that SVRDRVSS is return path for SVRPGATE/SVRNAGATE signaling.




➡ **HS current loop** (current loop when PMOS is turn on)
➡ **LS current loop** (current loop when NMOS is turn on)
➡ High di/dt loop**

**Mainly it caused by recovery current of body-diode of MOS, but it can be suppressed by dead-time setting. Parasitic resonance can also be a cause of this, but it can be avoided by designing the overall layout of the DCDC section to be as compact as possible (relative with this design rule9 in page15).

*Grounding for SVRDRVSS by using a few number of through hole via(THV). For applications with low VDD core current (ex. <1A), single THV/point grounding for SVRDRVSS is acceptable*

# Revision History

| Revision | Page | Items | Date |
|---|---|---|---|
| 1.0 | - | New Release | March 31, 2023 |
| 1.1 | 6, 7, 8 | - Added the capacitor parts and note. | September 29, 2023 |
| | 7, 12 | - Added values in tables for U2B10. | |
| | 11, 12, 13 | - Updated explanation for table 2. | |
| | 6 | - Typo fixed<br>Old: ⑤Total ≥104uF for combination b<br>New: ⑤Total ≥116uF for combination b | |
| | 15 | - Typo fixed<br>Old: [2:0] for SVRPGATE<br>New: [1:0] for SVRPGATE | |
| 1.2 | - | Correction of the format | July 5, 2025 |

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