Termination Options for High-Speed LVCMOS Driver Clock Drivers

This application note provides examples of high-speed LVCMOS clock drivers and their termination options, as well as the general rules for high-speed digital board design.

Contents

1. Introduction

For high-speed LVCMOS drivers, general rules for high-speed digital board design must be followed. Proper termination is required to ensure signal quality and Electro-Magnetic Interference (EMI) reduction.

There are many different termination schemes for single-ended LVCMOS drivers. This application note discusses parallel termination, AC termination and series termination. The following termination approaches are only general recommendations under ideal conditions. Board designers should consult with their signal integrity engineers or verify through simulations in their system environment.

2. Parallel (DC) Termination

The standard termination of an LVCMOS driver in a Z_O = 50Ω transmission line environment is shown in Figure 1. The driver is terminated with 50Ω pull-down to VTT = V_{DDO}/2 at the receiver end. The LVCMOS clock buffer characterization set up is terminated in similar manner using split power supplies approach (see test condition in the datasheet of an LVCMOS driver). In actual applications, the equivalent parallel termination can be used as shown in Figure 2. The LVCMOS parallel termination has the same effect as the standard LVCMOS shown in Figure 1. The parallel termination shown in Figure 2 can eliminate the need of VTT = V_{DDO}/2 power supply (or reference voltage). The power dissipation calculation is described in detail in application note AN-809.

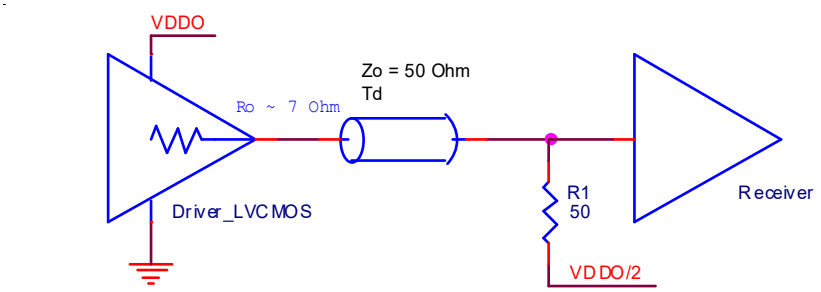

Figure 1. LVCMOS Driver Standard Termination

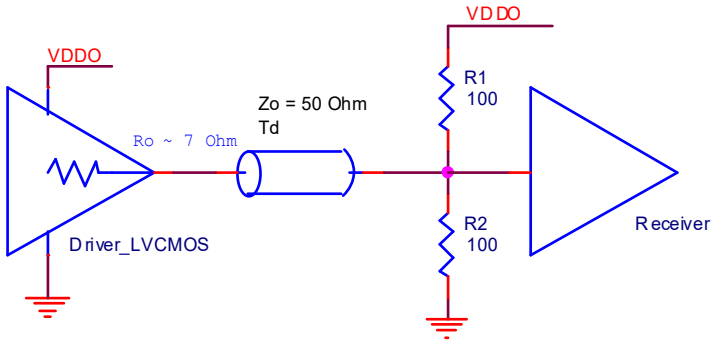

Figure 2. LVCMOS Parallel Termination

3. AC Termination

The LVCMOS driver AC termination in a 50Ω transmission line environment is shown in Figure 3. The majority of load current is drawn during transient region (in other words, rising edge and falling edge). This termination consumes less power than the parallel termination. The proper value of capacitor C1 depends on the trace delay and capacitance of the transmission line. Some PC board layout or simulation software tools provide a feature of calculating the transmission line capacitance by entering the trace information (see References, [1]).

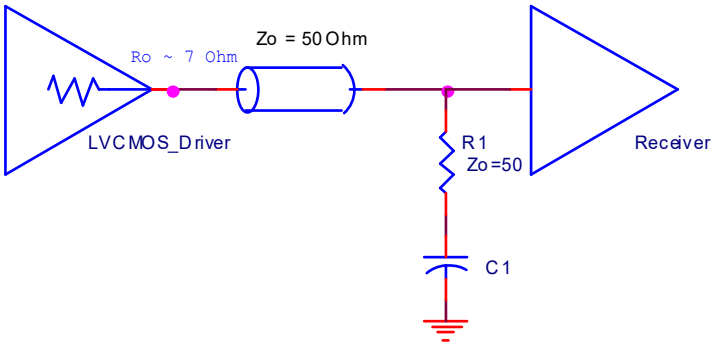

Figure 3. AC Termination

4. Series Termination

Series termination is a common termination scheme for LVCMOS drivers. Figure 4 shows a simple series termination for LVCMOS drivers with an output impedance of 7Ω. The Power Dissipation of this termination scheme is described in a separate document.

The typical output impedance R_O of a high-speed LVCMOS driver is approximately 7Ω to 16Ω (some parts might have different R_O value. Refer to the datasheet for the output impedance). For example, the closest R_S series resistor value for R_O = 7Ω can be calculated as follows:

$$R_S = Z_O - R_O = 43\Omega$$

In Figure 4, the footprint for an optional series resistor R3, or optional capacitor C1, at the receiver input is recommended for adjusting the edge rate or overshoot if necessary.

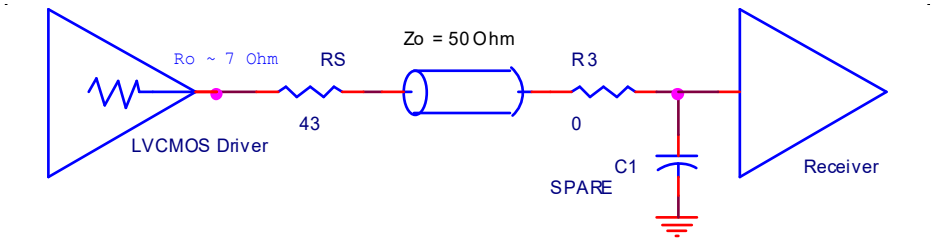

Figure 4. One-to-One LVCMOS Series Termination

When the number of drivers is not equal to number of receivers as shown in Figure 6, the series resistor value RS is calculated as follows:

$$R_S = Z_O - (R_O \times M)/(N)$$

where N = number of driver(s); M = number of receiver(s)

This configuration assumes that all the trace delays and load conditions are equally matched.

For example, one driver driving two receivers as shown in Figure 5, with N = 1 and M = 2, the series resistor is calculated to be R_S = 36Ω. The trace delays (Td) on TL1 are equal. The loading conditions on both receivers should also be equal.

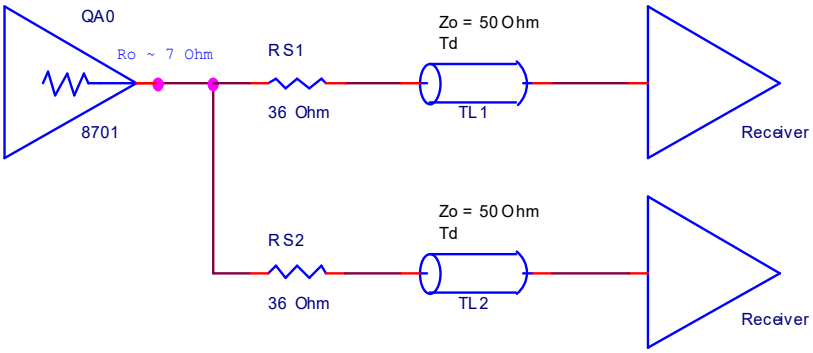

Figure 5. Series Termination for One LVCMOS Driver Driving Two Receivers

For five drivers driving six receivers, the closest series resistor can be calculated as follows:

$$N = 5,\ N = 6,\ Z_O = 50\Omega,\ R_O = 7\Omega$$

$$R_S = 50 - (7 \times 6)/5 = 41.6\Omega$$

The above result is straight from the calculations. The closest available resistor value should be chosen based on these calculations.

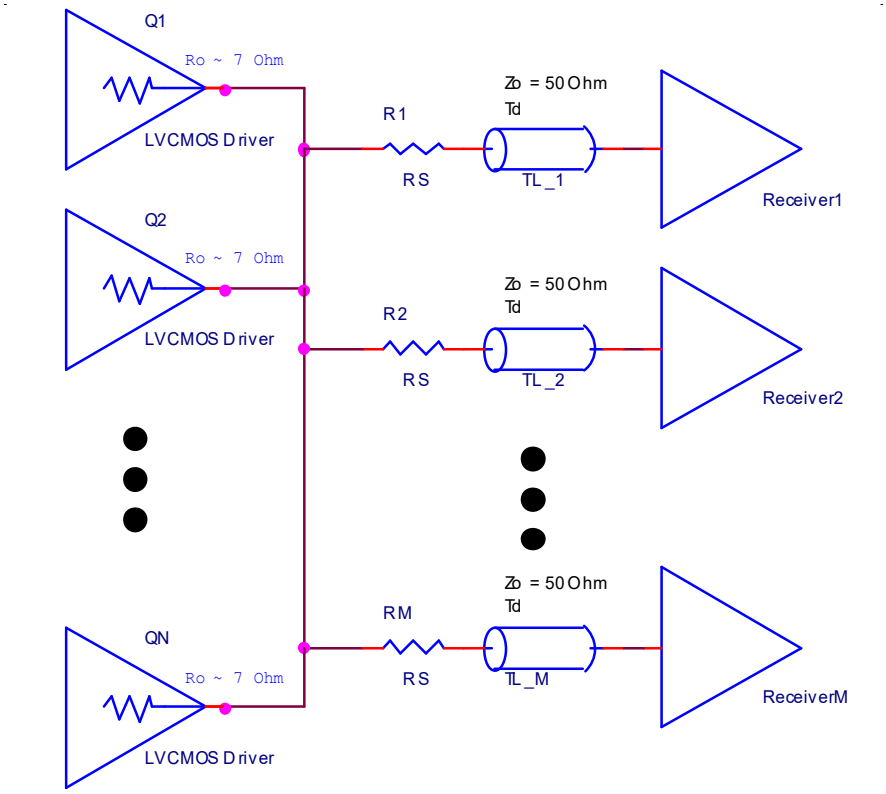

Figure 6. Tie 'N' Outputs Together to Drive 'M' Receivers

5. PC Board Layout with Option of Multiple Terminations Scheme

For signal integrity, ensure to take the necessary precautions and adhere to the following the high-speed digital design rules whenever possible. In most cases, the board design cannot fully comply with the high-speed design rules due to constraints on the board environment, for example, available space, cost, etc. There are always some unknown parameters or interferences in the system environment. The signal quality can only be optimized through the experiment of one termination scheme may work better than the other. While capturing a schematic for a PC Board layout, if there is available space, it is recommended to provide options to choose different termination schemes. Figure 7 shows an example schematic for a PC board footprint that provides an option of choosing various types of terminations.

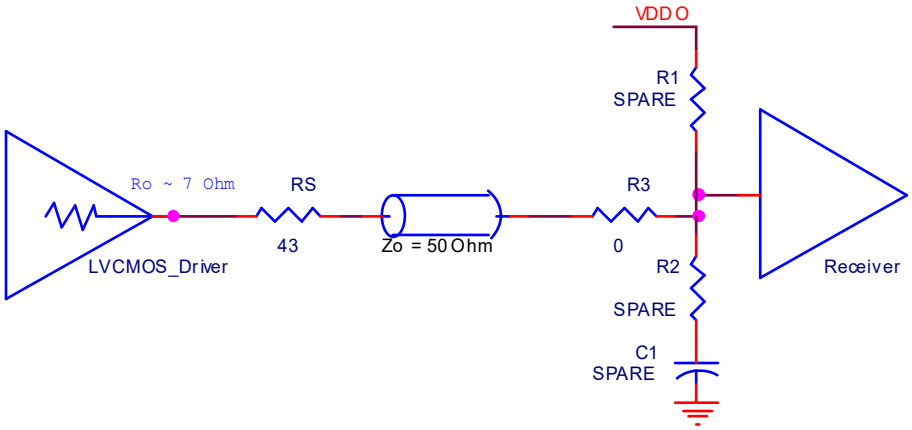

Figure 7. PC Board Layout Provides Footprint for Choosing Various Termination Options

6. References

[1] Kaufer, Steve, Crisafulli, Kellee, Terminating Trace on High-Speed PCBs, Printed Circuit Design, March 1998

[2] Dr. Johnson, Howard, Dr. Graham, Martin, High-Speed Digital Design, A Handbook of Black Magic, Prentice Hall, 1993

7. Revision History

Revision	Date	Description
1.01	Nov 14, 2023	▪ Changed document title to “Termination Options for High-Speed LVCMOS Driver Clock Drivers” from “AN-895 Termination–LVCMOS”. ▪ Reformatted document to the latest template.
-	May 13, 2014	Initial release.

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