RL78/G14, R8C/36M Group

Migration Guide from R8C to RL78: Interrupts

R01AN1432EJ0100
Rev. 1.00
June 1, 2013

Abstract

This document describes how to migrate interrupts for the R8C/36M to interrupts for the RL78/G14.

Products

RL78/G14, R8C/36M Group

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Differences between the R8C/36M Group and RL78/G14

1.1 Interrupts

Table 1.1 lists the general differences in interrupts.

Table 1.1 General Differences in Interrupts

Item	R8C/36M Group	RL78/G14
Maskable interrupts	Peripheral function interrupts (1)	Peripheral function interrupts
Non-maskable interrupts	• Software interrupts — Undefined instruction (UND instruction) — Overflow (INTO instruction) — BRK instruction — INT instruction	• Software interrupt — BRK instruction
	• Special interrupts — Watchdog timer — Oscillation stop detection — Voltage monitor 1/comparator A1 (2) — Voltage monitor 2/comparator A2 (2) — Single step (3) — Address break (3) — Address match	N/A
Interrupt priority levels	0 to 7 (4)	0 to 3 (5)
Type of vector table	• Fixed vector table • Relocatable vector table	Vector table
Vector table address	• Fixed address is in the fixed vector table • Relocatable address is in the relocatable vector table: (optional)	Fixed address

Notes: 1. Peripheral function interrupts are generated by the peripheral functions in the MCU.
2. A non-maskable or maskable interrupt can be selected by bits IRQ1SEL and IRQ2SEL in the CMPA register.
3. Do not use these interrupts. These are provided exclusively for use by development tools.
4. Level 0 is given low priority (interrupt disabled) and level 7 is given high priority.
5. Level 3 is given low priority and level 0 is given high priority.

1.2 Differences on $\overline{\text{INT}}$ Interrupt

Table 1.2 lists the differences in $\overline{\text{INT}}$ interrupts between the R8C/36M Group and RL78/G14.

Table 1.2 Differences in the $\overline{\text{INT}}$ Interrupt

Item	R8C/36M Group	RL78/G14
$\overline{\text{INT}}$ interrupt pin	$\overline{\text{INT0}}$ to $\overline{\text{INT4}}$ (refer to Table 1.3)	INTP0 to INTP11 (refer to Table 1.4)
Digital filter	Available	N/A

Table 1.3 $\overline{\text{INT}}$ Interrupt Pin Configuration in the R8C/36M Group

Pin Name	Assigned Pins
$\overline{\text{INT0}}$	P4_5
$\overline{\text{INT1}}$	P1_5, P1_7, P2_0, P3_2, or P3_6
$\overline{\text{INT2}}$	P3_2 or P6_6
$\overline{\text{INT3}}$	P3_3 or P6_7
$\overline{\text{INT4}}$	P6_5

Table 1.4 INTP Interrupt Pin Configuration in the RL78/G14

Pin Name	Assigned Pins
INTP0	P137
INTP1	P50, (P46) (1)
INTP2	P51, (P47) (1)
INTP3	P30
INTP4	P31
INTP5	P16
INTP6	P140
INTP7	P141
INTP8	P74
INTP9	P75
INTP10	P76
INTP11	P77

Note: 1. INTP1 and INTP2 in the 100-pin package are assigned to P46 and P47, respectively.

1.3 Differences in Key Input Interrupts

Differences between the R8C/36M Group key input interrupts and the RL78/G14 key input interrupts are listed in the table below.

Table 1.5 Differences in Key Input Interrupts

Item	R8C/36M Group	RL78/G14
Key input interrupt pin	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$ (refer to Table 1.6)	KR0 to KR7 (refer to Table 1.7)
Key input polarity	• Rising edge • Falling edge	Falling edge

Table 1.6 Key Input Interrupt Pin Configuration in the R8C/36M Group

Pin Name	Assigned Pins
$\overline{\text{KI0}}$	P1_0
$\overline{\text{KI1}}$	P1_1
$\overline{\text{KI2}}$	P1_2
$\overline{\text{KI3}}$	P1_3

Table 1.7 Key Input Interrupt Pin Configuration in the RL78/G14 (1)

Pin Name	Assigned Pins
KR0	P70
KR1	P71
KR2	P72
KR3	P73
KR4	P74
KR5	P75
KR6	P76
KR7	P77

Note: 1. KR0 to KR3 are available in the 40-pin and 44-pin packages, KR0 to KR5 are available in the 48-pin package, and KR0 to KR7 are available in the 52-pin, 64-pin, 80-pin, and 100-pin packages.

2. Register Compatibility

2.1 Interrupts

Table 2.1 lists the compatibility of registers associated with interrupts.

Table 2.1 Compatibility of Registers Associated with Interrupts

Item	R8C/36M Group	RL78/G14
Interrupt priority level select	• Interrupt control register Bits ILVL0 to ILVL2	• Priority specification flag register Bits XXPR1X and XXPR0X
Interrupt request flag	• Interrupt control register IR bit	• Interrupt request flag register XXIFX bit
Interrupt handling control	• Interrupt control register Bits ILVL0 to ILVL2 (level 0: interrupt disabled)	• Interrupt mask flag register XXMKX bit
Maskable interrupt enable control	• FLG register I flag	• PSW register IE flag
Processor interrupt priority specification	• FLG register IPL	• PSW register ISP1 and ISP0

Note: For details on bits XXPR1X, XXPR0X, XXIFX, and XXMKX, refer to the RL78/G14 User's Manual: Hardware.

2.2 Registers Associated with the $\overline{\text{INT}}$ Interrupt

Table 2.2 lists the compatibility of registers associated with the $\overline{\text{INT}}$ interrupt.

Table 2.2 Compatibility of Registers Associated with the $\overline{\text{INT}}$ Interrupt

Item	R8C/36M Group	RL78/G14
$\overline{\text{INT}}$ input polarity switch	• INTiIC register POL bit • INTEN register INTkPL bit • INTEN1 register INT4PL bit	• Registers EGP0 and EGP1 EGPn bit • Registers EGN0 and EGN1 EGNn bit
$\overline{\text{INT}}$ pin select	• INTSR register	N/A
$\overline{\text{INT}}$ input enable	• INTEN register INTkEN bit • INTEN1 register INT4EN bit	• Registers EGP0 and EGP1 EGPn bit • Registers EGN0 and EGN1 EGNn bit (Edge detection is disabled when bits EGPn and EGNn are 0)
$\overline{\text{INT}}$ input filter select	• INTF register Bits INTkF0 and INTkF1 • INTF1 register Bits INT4F0 and INT4F1	N/A

i = 0 to 4; k = 0 to 3; n = 0 to 11

2.3 Registers Associated with Key Input Interrupt

Table 2.3 lists the compatibility of registers associated with the key input interrupt.

Table 2.3 Compatibility of Registers Associated with the Key Input Interrupt

Item	R8C/36M Group	RL78/G14
Key input polarity select	• KIEN register KIjPL bit	N/A
Key input enable	• KIEN register KIjEN bit	• KRM register KRMn bit

j = 0 to 3; n = 0 to 7

3. Comparison of Interrupt Operation Settings

3.1 Maskable Interrupts

3.1.1 R8C/36M Group

In the R8C/36M Group, maskable interrupts are enabled or disabled by setting the I flag in the FLG register, IPL (Processor Interrupt Priority Level) and bits ILVL0 to ILVL2 in interrupt control registers. The IR bit in interrupt control registers indicates whether there is an interrupt request or not.

Table 3.1 lists the functions of the I flag. Table 3.2 lists the functions of the IPL. Table 3.3 lists the functions of the IR bit in the interrupt control register. Table 3.4 lists the functions of the interrupt priority level select bits.

Table 3.1 I Flag Functions

I Flag	Function
0	Disable maskable interrupts
1	Enable maskable interrupts

Table 3.2 IPL Functions

IPL	Function
000b	Interrupt level 1 and above are enabled
001b	Interrupt level 2 and above are enabled
010b	Interrupt level 3 and above are enabled
011b	Interrupt level 4 and above are enabled
100b	Interrupt level 5 and above are enabled
101b	Interrupt level 6 and above are enabled
110b	Interrupt level 7 and above are enabled
111b	All maskable interrupts are disabled

Table 3.3 Interrupt Request Bit Functions

IR Bit	Function
0	No interrupt requested
1	Interrupt requested

Table 3.4 Interrupt Priority Level Select Bits Functions

ILVL2 Bit	ILVL1 Bit	ILVL0 Bit	Interrupt Priority Level	Priority
0	0	0	Level 0 (interrupt disabled)	N/A
0	0	1	Level 1	Low
0	1	0	Level 2	↓
0	1	1	Level 3	
1	0	0	Level 4	
1	0	1	Level 5	
1	1	0	Level 6	
1	1	1	Level 7	High

Interrupts are acknowledged when:

- I flag = 1
- IR bit = 1
- Interrupt priority level > IPL

3.1.2 RL78/G14

In RL78/G14, maskable interrupts are enabled or disabled by setting the flags IE, ISP0, and ISP1 in the PSW register, bits XXPR1X and XXPR0X in the priority specification flag register and the XXMKX bit in the interrupt mask flag register. The XXIFX bit in the interrupt request flag registers indicates whether there is an interrupt request or not.

Table 3.5 lists the functions of IE flag. Table 3.6 lists the functions of flags ISP1 and ISP0. Table 3.7 lists the functions of the interrupt request flag. Table 3.8 lists the functions of the interrupt servicing control bit. Table 3.9 lists the functions of priority level select bits.

Table 3.5 IE Flag Functions

IE Flag	Function
0	Maskable interrupt requests are disabled
1	Maskable interrupt requests are enabled

Table 3.6 ISP1 and ISP0 Flag Functions

ISP1 Flag	ISP0 Flag	Function
0	0	Interrupt of level 0 is enabled (interrupt of level 1 or 0 is being serviced)
0	1	Interrupt of level 0 and 1 are enabled (interrupt of level 2 is being serviced)
1	0	Interrupt of level 0 to 2 are enabled (interrupt of level 3 is being serviced)
1	1	All interrupts are enabled (wait for an acknowledgment of interrupt)

Table 3.7 Interrupt Request Flag Functions

XXIFX Flag	Function
0	No interrupt request signal is generated
1	Interrupt request is generated, interrupt request status

Note: For details on the XXIFX bit, refer to the RL78/G14 User's Manual: Hardware.

Table 3.8 Interrupt Servicing Control Bit Functions

XXMKX Bit	Function
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Note: For details on the XXMKX bit, refer to the RL78/G14 User's Manual: Hardware.

Table 3.9 Priority Level Select Bit Functions

XXPR1X Bit	XXPR0X Bit	Function
0	0	Specify level 0 (high priority level)
0	1	Specify level 1
1	0	Specify level 2
1	1	Specify level 3 (low priority level)

Note: For details on bits XXPR1X and XXPR0X, refer to the RL78/G14 User's Manual: Hardware.

Interrupts are acknowledged when:

- Interrupt request flag = 1
- Interrupt mask flag = 0
- IE flag = 1
- Interrupt priority level ≤ ISP1, ISP0

3.2 $\overline{\text{INT}}$ Interrupt

3.2.1 R8C/36M Group

In the R8C/36M Group, set the INTjEN bit in the INTEN register and the INT4EN bit in the INTEN1 register to enable or disable the $\overline{\text{INT}}$ interrupt (j = 0 to 3). Table 3.10 lists the settings to enable and disable the $\overline{\text{INTi}}$ interrupt (i = 0 to 4).

Set the INTjPL bit in the INTEN register, the INT4PL bit in the INTEN1 register, and the POL bit in the INTiIC register to specify the input polarity. Table 3.11 lists the settings of the $\overline{\text{INTi}}$ input polarity select bit, and Table 3.12 lists the settings of the polarity switch bit.

Set registers INTF and INTF1 to specify the $\overline{\text{INTi}}$ input filter. Table 3.13 lists the functions of $\overline{\text{INTi}}$ input filter select bit.

Set the INTSR register to select which pins to assign for $\overline{\text{INT1}}$ to $\overline{\text{INT3}}$ interrupts. Table 3.14 to Table 3.16 list the functions of interrupt input pin select bits.

Table 3.10 Enabling and Disabling the $\overline{\text{INTi}}$ Interrupt

INTiEN Bit	Function
0	Disable a maskable interrupt
1	Enable a maskable interrupt

Table 3.11 $\overline{\text{INTi}}$ Input Polarity Select Bit Functions

INTiPL Bit (1, 2)	Function
0	One edge
1	Both edges

Notes: 1. To set the INTiPL bit to 1 (both edges), set the POL bit in the INTiIC register to 0 (falling edge selected).
2. The IR bit in the INTiIC register may be set to 1 (interrupt requested) when the POL bit is rewritten.

Table 3.12 Polarity Switch Bit Functions

POL Bit (1)	Function
0	Falling edge selected
1	Rising edge selected (2)

Notes: 1. The IR bit in the INTiIC register may be set to 1 (interrupt requested) when the POL bit is rewritten.
2. To set the INTiPL bit in the INTEN register to 1 (both edges), set the POL bit to 0 (falling edge selected).

Table 3.13 $\overline{\text{INTi}}$ Input Filter Select Bit Functions

INTiF0 Bit	INTiF1 Bit	Function
0	0	No filter
0	1	Filter with f1 sampling
1	0	Filter with f8 sampling
1	1	Filter with f32 sampling

i = 0 to 4

Table 3.14 $\overline{\text{INT1}}$ Pin Select Bit Functions

INT1SEL0 Bit	INT1SEL1 Bit	INT1SEL2 Bit	Function
0	0	0	P1_7 assigned
0	0	1	P1_5 assigned
0	1	0	P2_0 assigned
0	1	1	P3_6 assigned
1	0	0	P3_2 assigned

Table 3.15 $\overline{\text{INT2}}$ Pin Select Bit Functions

INT2SEL0 Bit	Function
0	P6_6 assigned
1	P3_2 assigned

Table 3.16 $\overline{\text{INT3}}$ Pin Select Bit Functions

INT3SEL0 Bit	INT3SEL1 Bit	Function
0	0	P3_3 assigned
0	1	Do not set.
1	0	P6_7 assigned
1	1	Do not set.

3.2.2 RL78/G14

In RL78/G14, valid edges of pins INTP0 to INTP11 are specified by setting registers EGPm and EGNm (m = 0 and 1).

Table 3.17 lists the functions of the INTPn pin valid edge select bit, and Table 3.18 lists the ports corresponding to bits EGPn and EGNn (n = 0 to 11).

Table 3.17 INTPn Pin Valid Edge Selection Bit Functions

EGPn Bit	EGNn Bit	Function
0	0	Edge detection disabled
0	1	Falling edge
1	0	Rising edge
1	1	Both rising and falling edges

Table 3.18 Ports Corresponding to Bits EGPn and EGNn (n = 0 to 11)

Detection Enable Bit		Corresponding Port
EGP0	EGN0	INTP0
EGP1	EGN1	INTP1
EGP2	EGN2	INTP2
EGP3	EGN3	INTP3
EGP4	EGN4	INTP4
EGP5	EGN5	INTP5
EGP6	EGN6	INTP6
EGP7	EGN7	INTP7
EGP8	EGN8	INTP8
EGP9	EGN9	INTP9
EGP10	EGN10	INTP10
EGP11	EGN11	INTP11

3.3 Key Input Interrupt

3.3.1 R8C/36M Group

In the R8C/36M Group, set the KIjEN bit in the KIEN register to enable or disable the key input interrupt, and set the KIjPL bit in the KIEN register to specify the input polarity (j = 0 to 3).

Table 3.19 lists the settings to enable and disable the key input interrupt, and Table 3.20 lists the functions of the key input polarity select bit.

Table 3.19 Enabling and Disabling the Key Input Interrupt

KIjEN Bit	Function
0	Disable the key input interrupt
1	Enable the key input interrupt

Table 3.20 Key Input Polarity Select Bit Functions

KIjPL Bit	Function
0	Falling edge
1	Rising edge

3.3.2 RL78/G14

In RL78/G14, set the KRMn bit in the KRM register to enable or disable the key interrupt.

Table 3.21 lists the functions of the key interrupt mode control bit.

Table 3.21 Key Interrupt Mode Control Bit Functions

KRMn Bit	Function
0	Does not detect key interrupt signal
1	Detects key interrupt signal

n = 0 to 7

3.4 Interrupt Priority Level

3.4.1 R8C/36M Group

In the R8C/36M Group, an interrupt with the higher priority is acknowledged when two or more interrupt requests are generated while a single instruction is being executed. Note that if two or more interrupts have the same priority level, their interrupt priority is resolved by hardware, with the higher priority interrupts acknowledged.

The priority of special interrupts is set by hardware.

3.4.2 RL78/G14

In RL78/G14, when two or more maskable interrupt requests are generated simultaneously, the request with a higher priority level specified in the priority specification flag is acknowledged first. If two or more interrupt requests have the same priority level, the request with the highest default priority is acknowledged first.

3.5 Register Saving

3.5.1 R8C/36M Group

In the R8C/36M Group, the FLG register and the PC (program counter) are saved in the stack. To be more specific, the 4 high-order bits in the PC, and the 4 high-order bits (IPL) and 8 low-order bits in the FLG register (16 bits in total) are saved in the stack first, and then the 16 low-order bits in the PC are saved.

3.5.2 RL78/G14

In RL78/G14, when a maskable interrupt request is acknowledged, the PC is saved in the stack after the program status word (PSW) is saved.

4. Interrupt Vectors

The configuration of interrupt vectors varies between the R8C/36M Group and RL78/G14. The R8C/36M Group has fixed vector tables and relocatable vector tables, and RL78/G14 has address-fixed vector tables.

4.1 R8C/36M Group

4.1.1 Fixed Vector Tables

Fixed vector tables are allocated from addresses 0FFDCh to 0FFFh. There are 4 bytes in a vector. Fixed vector tables are listed in the table below.

Table 4.1 Fixed Vector Tables

Interrupt Source	Vector Addresses	Remarks
Undefined instruction	0FFDCh to 0FFDFh	Interrupt with UND instruction
Overflow	0FFE0h to 0FFE3h	Interrupt with INTO instruction
BRK instruction	0FFE4h to 0FFE7h	If the value of address 0FFE6h is FFH, program execution starts from the address shown by the vector in the relocatable vector table.
Address match	0FFE8h to 0FFEBh	
Single step (1)	0FFECh to 0FFEFh	
Watchdog timer, Oscillation stop detection, Voltage monitor 1/comparator A1 (2), Voltage monitor 2/comparator A2 (3)	0FFF0h to 0FFF3h	
Address break (1)	0FFF4h to 0FFF7h	
Reserved	0FFF8h to 0FFFBh	
Reset	0FFFCh to 0FFFFh	

Notes: 1. Do not use these interrupts. They are provided exclusively for use by development tools.
2. Voltage monitor 1/comparator A1 interrupt is selected when the IRQ1SEL bit in the CMPA register is set to 0 (nonmaskable interrupt).
3. Voltage monitor 2/comparator A2 interrupt is selected when the IRQ2SEL bit in the CMPA register is set to 0 (nonmaskable interrupt).

4.1.2 Relocatable Vector Table

Relocatable vector tables occupy 256 bytes beginning from the start address set in the INTB register. Table 4.2 lists the relocatable vector tables.

Table 4.2 Relocatable Vector Tables

Interrupt Source	Vector Addresses Address (L) to Address (H)	Software Interrupt Number	Interrupt Control Register
BRK instruction (1)	+0 to +3 (0000h to 0003h)	0	
Flash memory ready	+4 to +7 (0004h to 0007h)	1	FMRDYIC
Reserved		2 to 5	N/A
$\overline{\text{INT4}}$	+24 to +27 (0018h to 001BFh)	6	INT4IC
Timer RC	+28 to +31 (001Ch to 001Fh)	7	TRCIC
Timer RD0	+32 to +35 (0020h to 0023h)	8	TRD0IC
Timer RD1	+36 to +39 (0024h to 0027h)	9	TRD1IC
Timer RE	+40 to +43 (0028h to 002Bh)	10	TREIC
UART2 transmit/NACK2	+44 to +47 (002Ch to 002Fh)	11	S2TIC
UART2 receive/ACK2	+48 to +51 (0030h to 0033h)	12	S2RIC
Key input	+52 to +55 (0034h to 0037h)	13	KUPIC
A/D conversion	+56 to +59 (0038h to 003Bh)	14	ADIC
Synchronous serial communication unit/ I^2C bus interface (2)	+60 to +63 (003Ch to 003Fh)	15	SSUIC/IICIC
Timer RF compare 1	+64 to +67 (0040h to 0043h)	16	CMP1IC
UART0 transmit	+68 to +71 (0044h to 0047h)	17	S0TIC
UART0 receive	+72 to +75 (0048h to 004Bh)	18	S0RIC
UART1 transmit	+76 to +79 (004Ch to 004Fh)	19	S1TIC
UART0 receive	+80 to +83 (0050h to 0053h)	20	S1RIC
$\overline{\text{INT2}}$	+84 to +87 (0054h to 0057h)	21	INT2IC
Timer RA	+88 to +91 (0058h to 005Bh)	22	TRAIC
Reserved		23	N/A
Timer RB	+96 to +99 (0060h to 0063h)	24	TRBIC
$\overline{\text{INT1}}$	+100 to +103 (0064h to 0067h)	25	INT1IC
$\overline{\text{INT3}}$	+104 to +107 (0068h to 006Bh)	26	INT3IC
Timer RF	+108 to +111 (006Ch to 006Fh)	27	TRFIC
Timer RF compare 0	+112 to +115 (0070h to 0073h)	28	CMP0IC
$\overline{\text{INT0}}$	+116 to +119 (0074h to 0077h)	29	INT0IC
UART2 bus collision detection	+120 to +123 (0078h to 007Bh)	30	U2BCNIC
Timer RF capture	+124 to +127 (007Ch to 007Fh)	31	CAPIC
Software (1)	+128 to +131 (0080h to 0083h) to +164 to +167 (00A4h to 00A7h)	32 to 41	N/A
Reserved		42	N/A
Timer RG	+172 to +175 (00ACh to 00AFh)	43	TRGIC
Reserved		44 to 49	N/A
Voltage monitor 1/ comparator A1 (3)	+200 to +203 (00C8h to 00CBh)	50	VCMP1IC
Voltage monitor 2/ comparator A2 (3)	+204 to +207 (00CCh to 00CFh)	51	VCMP2IC
Reserved		52 to 55	N/A
Software	+224 to +227 (00E0h to 00E3h) to +252 to +255 (00FCh to 00FFh)	56 to 63	N/A

Notes 1. These interrupts are not disabled by the I flag.
2. These are selectable by the IICSEL bit in the SSUIICSR register.
3. These interrupt sources can be selected when using maskable interrupts.

4.2 RL78/G14

RL78/G14 vector tables include the interrupt sources and reset sources. There are 2 bytes in each vector code. Set the program start address where the CPU branches when interrupts or reset sources are generated in the RL78/G14 vector tables. The destination start address is a 64 KB address from 00000H to 0FFFFH. The highest default priority is 0 and the lowest is 44. When an interrupt request is acknowledged, the CPU branches to the address set in the corresponding interrupt vector. Vector tables are listed in Table 4.3 to Table 4.5.

Table 4.3 Vector Table (1/3)

Default Priority	Interrupt Source		Internal/ External	Vector Table Address
	Name	Trigger		
0	INTWDTI	Watchdog timer interval (75% of overflow time + 1/2f_{IL})	Internal	0004H
1	INTLVI	Voltage detected		0006H
2	INTP0	Pin input edge detected	External	0008H
3	INTP1			000AH
4	INTP2			000CH
5	INTP3			000EH
6	INTP4			0010H
7	INTP5			0012H
8	INTST2/ INTCSI20/ INTIIC20	UART2 transmission transfer end or buffer empty interrupt/ CSI20 transfer end or buffer empty interrupt/ IIC20 transfer end	Internal	0014H
9	INTSR2/ INTCSI21/ INTIIC21	UART2 reception transfer end/ CSI21 transfer end or buffer empty interrupt/ IIC21 transfer end		0016H
10	INTSRE2	UART2 reception communication error occurred		0018H
	INTTM11H	End of timer channel 11 count or capture (when an 8-bit timer is operating)		
11	INTST0/ INTCSI00/ INTIIC00	UART0 transmission transfer end/ CSI00 transfer end or buffer empty interrupt/ IIC00 transfer end		001EH
12	INTSR0/ INTCSI01/ INTIIC01	UART0 reception transfer end/ CSI01 transfer end or buffer empty interrupt/ IIC01 transfer end		0020H
13	INTSRE0	UART0 reception communication error occurred		0022H
	INTTM01H	End of timer channel 1 count or capture (when an 8-bit timer is operating)		

Table 4.4 Vector Table (2/3)

Default Priority	Interrupt Source		Internal/ External	Vector Table Address
	Name	Trigger		
14	INTST1/ INTCSI10/ INTIIC10	UART1 transmission transfer end or buffer empty interrupt/CSI10 transfer end or buffer empty interrupt/IIC10 transfer end	Internal	0024H
15	INTSR1/ INTCSI11/ INTIIC11	UART1 reception transfer end/CSI11 transfer end or buffer empty interrupt/IIC11 transfer end		0026H
16	INTSRE1	UART1 reception communication error occurred		0028H
	INTTM03H	End of timer channel 3 count or capture (when an 8-bit timer is operating)		
17	INTIICA0	End of IICA0 communication		002AH
18	INTTM00	End of timer channel 0 count or capture		002CH
19	INTTM01	End of timer channel 1 count or capture		002EH
20	INTTM02	End of timer channel 2 count or capture		0030H
21	INTTM03	End of timer channel 3 count or capture		0032H
22	INTAD	End of A/D conversion		0034H
23	INTRTC	Fixed-cycle signal of real-time clock/alarm match detected		0036H
24	INTIT	Interval signal detected		0038H
25	INTKR	Key return signal detected	External	003AH
26	INTST3/ INTCSI30/ INTIIC30	UART3 transmission transfer end or buffer empty interrupt/CSI30 transfer end or buffer empty interrupt/IIC30 transfer end	Internal	003CH
27	INTSR3/ INTCSI31/ INTIIC31	UART3 reception transfer end/CSI31 transfer end or buffer empty interrupt/IIC31 transfer end		003EH
28	INTTRJ0	Timer RJ underflow		0040H
29	INTTM10	End of timer channel 10 count or capture		0042H
30	INTTM11	End of timer channel 11 count or capture		0044H
31	INTTM12	End of timer channel 12 count or capture		0046H
32	INTTM13	End of timer channel 13 count or capture		0048H
33	INTP6	Pin input edge detected	External	004AH
34	INTP7			004CH
35	INTP8			004EH
36	INTP9			0050H
37	INTP10	Pin input edge detected	External	0052H
	INTCMP0	Comparator detection 0	Internal	
38	INTP11	Pin input edge detection	External	0054H
	INTCMP1	Comparator detection 1	Internal	
39	INTTRD0	Timer RD0 input capture, compare match, overflow, underflow interrupt	Internal	0056H
40	INTTRD1	Timer RD1 input capture, compare match, overflow, underflow interrupt		0058H

Table 4.5 Interrupt Source List (3/3)

Default Priority	Interrupt Source		Internal/ External	Vector Table Address
	Name	Trigger		
41	INTTRG	Timer RG input capture, compare match, overflow, underflow interrupt	Internal	005AH
42	INTSRE3	UART3 reception communication error occurred		005CH
	INTTM13H	End of timer channel 13 count or capture (when an 8-bit timer is operating)		
43	INTIICA1	End of IICA1 communication		0060H
44	INTFL	End of sequencer interrupt		0062H
N/A	BRK	BRK instruction executed	N/A	007EH
	RESET	$\overline{\text{RESET}}$ pin input		0000H
	POR	Power-on-reset		
	LVD	Voltage detected		
	WDT	Overflow of watchdog timer		
	TRAP	Illegal instruction executed		
	IAW	Illegal-memory access		
	RAMTOP	RAM parity error		

5. Reference Documents

User's Manual: Hardware
RL78/G14 User's Manual: Hardware Rev.1.00
R8C/36M Group User's Manual: Hardware Rev.1.00
The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

Website and Support

Renesas Electronics website
http://www.renesas.com

Inquiries
http://www.renesas.com/contact/

REVISION HISTORY	RL78/G14, R8C/36M Group Migration Guide from R8C to RL78: Interrupts

Rev.	Date	Description	
		Page	Summary
1.00	June 1, 2013	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.
   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
3. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from such alteration, modification, copy or otherwise misappropriation of Renesas Electronics product.
5. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.
   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots etc.
   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; and safety equipment etc.
   Renesas Electronics products are neither intended nor authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems, surgical implantations etc.), or may cause serious property damages (nuclear reactor control systems, military equipment etc.). You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application for which it is not intended. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for which the product is not intended by Renesas Electronics.
6. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
7. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or systems manufactured by you.
8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
9. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You should not use Renesas Electronics products or technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. When exporting the Renesas Electronics products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations.
10. It is the responsibility of the buyer or distributor of Renesas Electronics products, who distributes, disposes of, or otherwise places the product with a third party, to notify such third party in advance of the contents and conditions set forth in this document, Renesas Electronics assumes no responsibility for any losses incurred by you or third parties as a result of unauthorized use of Renesas Electronics products.
11. This document may not be reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

RENESAS

SALES OFFICES Renesas Electronics Corporation http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 /-7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

Colophon 2.2