RL78/G14, H8/36109

Migration Guide from H8 to RL78: Power-Down Modes

Introduction

This application note describes how to migrate the Power-Down Modes of H8/36109 to the Standby Function of RL78/G14 (100-pin package).

Target Device

RL78/G14, H8/36109

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Functions of Power-Down Modes

Table 1.1 shows the functions of the Power-Down Modes of H8/36109, and Table 1.2 shows the functions of the Standby Function of RL78/G14.

Table 1.1 Function of the Power-Down Modes of H8/36109

Function	Explanation
Subactive mode	The CPU and all on-chip peripheral modules operate on the subclock. The subclock frequency can be selected from φw/2, φw/4, or φw/8.
Sleep mode	The CPU halts. On-chip peripheral modules operate on the system clock.
Subsleep mode	The CPU halts. On-chip peripheral modules operate on the subclock.
Standby mode	The CPU and all on-chip peripheral modules halt. When the clock time-base function is selected, the RTC operates.

Table 1.2 Function of the Standby Function of RL78/G14

Function	Explanation
Normal operation mode (subsystem clock)(Note1)	When the CSS bit of the CKC register is set to 1 while the subsystem clock is operating, the subsystem clock becomes the CPU clock and the normal operation mode continues.
HALT mode	HALT instruction execution sets the HALT mode. In the HALT mode, the CPU operation clock is stopped. If the highspeed system clock oscillator, high-speed on-chip oscillator, or subsystem clock oscillator is operating before the HALT mode is set, oscillation of each clock continues. In this mode, the operating current is not decreased as much as in the STOP mode, but the HALT mode is effective for restarting operation immediately upon interrupt request generation and carrying out intermittent operations frequently.
STOP mode	STOP instruction execution sets the STOP mode. In the STOP mode, the high-speed system clock oscillator and high-speed on-chip oscillator stop, stopping the whole system, thereby considerably reducing the CPU operating current. Because this mode can be cleared by an interrupt request, it enables intermittent operations to be carried out. However, because a wait time is required to secure the oscillation stabilization time after the STOP mode is released when the X1 clock is selected, select the HALT mode if it is necessary to start processing immediately upon interrupt request generation.
SNOOZE mode	In the case of CSIp or UARTq data reception, an A/D conversion request by the timer trigger signal (the interrupt request signal (INTRTC/INTIT) or ELC event input), and DTC start source, the STOP mode is exited, the CSIp or UARTq data is received without operating the CPU, A/D conversion is performed, and DTC start source. This can only be specified when the high-speed on-chip oscillator is selected for the CPU/peripheral hardware clock (f_{CLK}).

Note1. The RL78/G14 products with 40 or more pins are provided with a subsystem clock.

Note2. The XT1 oscillator oscillates with a crystal resonator (32.768 kHz (TYP.)) connected to the XT1 and XT2 pins.

Remark1. For RL78/G14,
30 to 64-pin products: p = 00; q = 0
80 to 100-pin products: p = 00, 20; q = 0, 2

Remark2. The functions incorporated and port functions to use are different depending on the product. For details, refer to the appropriate user's manuals (hardware).

H8/36109 has 4 Power-Down Modes: subactive mode, sleep mode, subsleep mode, and standby mode.

Figure 1.1 shows the transition of Power-Down Modes of H8/36109.

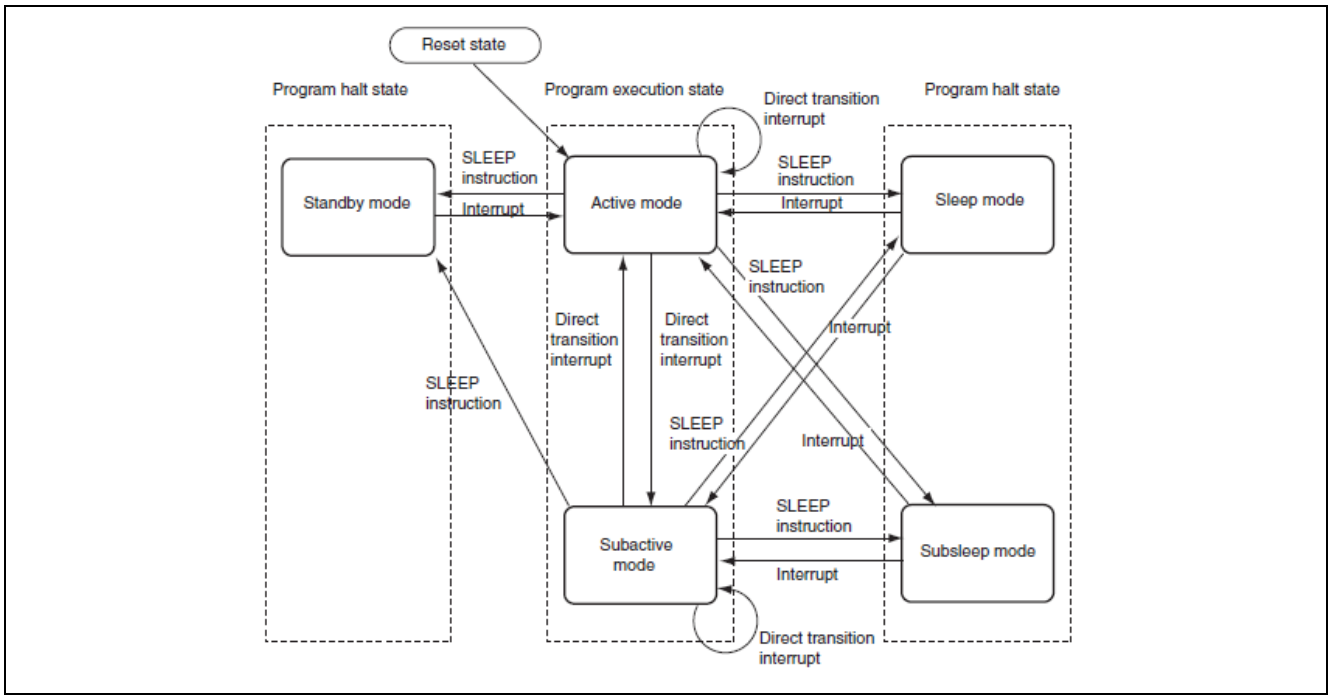

Figure 1.1 Transition of Power-Down Modes of the H8/36109

RL78/G14 standby function provides HALT mode, STOP mode, and SNOOZE mode.

Figure 1.2 shows the state transitions of RL78/G14 standby function.

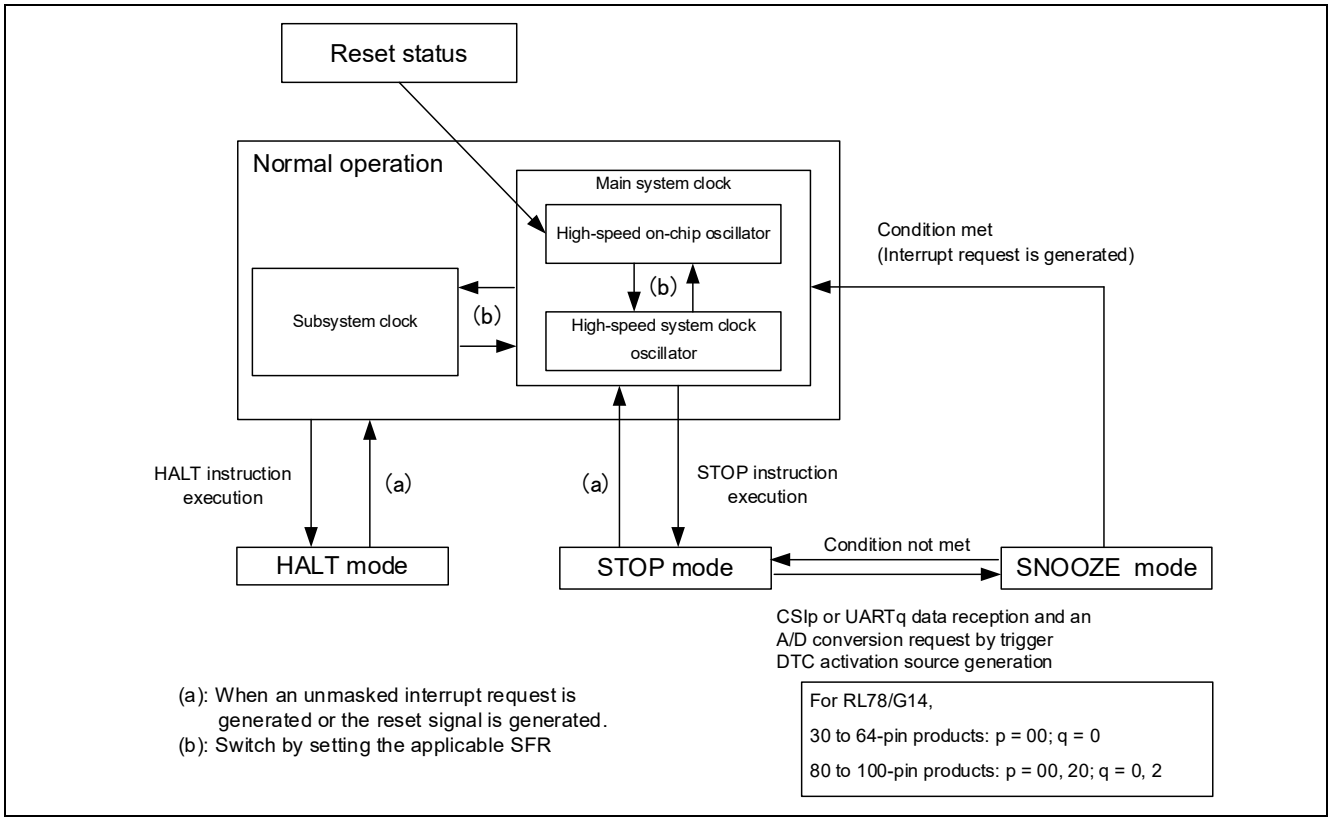

Figure 1.2 The state transitions of the RL78/G14 standby function

Table 1.3 shows the correspondence between the operating modes of H8/36109 and RL78/G14.

Table 1.3 Correspondence between the Operating Modes of H8/36109 and RL78/G14

H8/36109 Operating mode	RL78/G14 Operating mode
Active mode	Normal operation mode (Main system clock)
Subactive mode	Normal operation mode (Subsystem clock) (Note1)
Sleep mode	HALT mode (Main system clock)
Subsleep mode	HALT mode (Subsystem clock)
Standby mode	STOP mode
None	SNOOZE mode (Note2)

Note1. The RL78/G14 products with 40 or more pins are provided with a subsystem clock.

Note2. The SNOOZE mode can only be specified for CSIp, the A/D converter, or DTC. The UARTq can be specified only when FRQSEL4 in the option byte 000C2H is 0. Note that this mode can only be specified if the CPU clock is the high-speed on-chip oscillator clock.

Remark1. For RL78/G14,
30 to 64-pin products: p = 00; q = 0
80 to 100-pin products: p = 00, 20; q = 0, 2

Remark2. The functions incorporated and port functions to use are different depending on the product. For details, refer to the appropriate user's manuals (hardware).

2. Differences between Operating mode

2.1 Differences between Subactive mode

Table 2.1 lists the differences between the subactive mode of H8/36109 and the normal operation mode (subsystem clock) of RL78/G14.

H8/36109 enters the subactive mode when a SLEEP instruction is executed (direct transition) or when an interrupt occurs while in active mode, sleep mode, or subsleep mode.

RL78/G14 enters the normal operation mode (subsystem clock) when CSS bit of CKC register is set to 1.

Table 2.1 Differences between H8/36109 Subactive Mode and RL78/G14 Normal Operation Mode

Item	H8/36109 Subactive mode	RL78/G14 Normal operation mode (Subsystem clock)
System clock oscillator	Halted	Can choose to operate or stop.
Subclock oscillator	Functioning	Operable (Note1)
CPU	Functioning	Operable
RAM	Functioning	Operable
I/O ports	Functioning	Operable
External interrupts	Functioning	Operable
Peripheral functions	Functioning, Reset, Retained (Note2)	Operable (Note3)
Transition method	- SLEEP instruction execution (Direct transition) - Interrupt	Set the CSS bit in the CKC register to 1.

Note1. The RL78/G14 products with 40 or more pins are provided with a subsystem clock.

Note2. For H8/36109,

Functioning: RTC (The timekeeping time-base function is selected)
Reset: Timer V, SCI3, SCI3_2, SCI3_3, A/D converter
Retained: Peripheral modules other than above

Note3. For RL78/G14,

Operable: Peripheral functions other than below (which are disabled)
Operation disabled: A/D converter, Serial interface (IICA), High-speed CRC

2.2 Differences between Sleep Mode

Table 2.2 lists the differences between the sleep mode of H8/36109 and the HALT mode (main system clock) of RL78/G14.

H8/36109 enters the sleep mode when a SLEEP instruction is executed.

RL78/G14 enters the HALT mode when a HALT instruction is executed.

Table 2.2 Differences between H8/36109 sleep mode and RL78/G14 HALT mode

Item	H8/36109 Sleep Mode	RL78/G14 HALT Mode (Main system clock)
System clock oscillator	Functioning	Status before HALT mode was set is retained
Subclock oscillator	Functioning	Status before HALT mode was set is retained (Note)
CPU	Instructions: Halted, Registers: Retained	Instructions: Operation stopped, Registers: Retained
RAM	Retained	Retained (Operable while in the DTC is executed)
I/O ports	Retained	Status before HALT mode was set is retained
External interrupts	Functioning	Operable
Peripheral functions	Functioning	Operable
Transition method	SLEEP instruction execution	HALT Instruction is Executed

Note. The RL78/G14 products with 40 or more pins are provided with a subsystem clock.

2.3 Differences between Subsleep Mode

Table 2.3 lists the differences between subsleep mode of H8/36109 and HALT mode (subsystem clock) of RL78/G14.

H8/36109 enters the subsleep mode when a SLEEP instruction is executed.

RL78/G14 enters the HALT mode when a HALT instruction is executed.

Table 2.3 Differences between H8/36109 Subsleep Mode and RL78/G14 HALT Mode

Item	H8/36109 Subsleep Mode	RL78/G14 HALT Mode (Subsystem clock)
System clock oscillator	Halted	Operation disabled
Subclock oscillator	Functioning	Operable (Note1)
CPU	Instructions: Halted, Registers: Retained	Instructions: Operation stopped, Registers: Retained
RAM	Retained	Retained (Operable while in the DTC is executed)
I/O ports	Retained	Status before HALT mode was set is retained
External interrupts	Functioning	Operable
Peripheral functions	Retained or Reset (Note2)	Operable (Note3)
Transition method	SLEEP instruction execution	HALT Instruction is Executed

(Notes are listed on the next page.)

Note1. The RL78/G14 products with 40 or more pins are provided with a subsystem clock.

Note2. For H8/36109,

Functioning: RTC (The timekeeping time-base function is selected)
Reset: Timer V, SCI3, SCI3_2, SCI3_3, A/D converter
Retained: Peripheral modules other than above

Note3. For RL78/G14,

Operable: Peripheral functions other than below (which are disabled)
Operation disabled: A/D converter, Serial interface (IICA), High-speed CRC

2.4 Differences between Standby mode

Table 2.4 lists the differences between the standby mode of H8/36109 and the STOP mode of RL78/G14.

H8/36109 enters Standby mode when a SLEEP instruction is executed.

RL78/G14 enters STOP mode when a STOP instruction is executed.

Table 2.4 Differences between H8/36109 Standby Mode and RL78/G14 STOP Mode

Item	H8/36109 Standby mode	RL78/G14 STOP Mode
System clock oscillator	Halted	Operation disabled
Subclock oscillator	Functioning	Status before STOP mode was set is retained (Note1)
CPU	Instructions: Halted, Registers: Retained	Operation stopped
RAM	Retained	Retained
I/O ports	Registers: Retained Output: High-impedance state	Status before STOP mode was set is retained
External interrupts	Functioning	Operable
Peripheral functions	Retained or Reset (Note2)	Note3
Transition method	SLEEP instruction execution	STOP Instruction is Executed

Note1. The RL78/G14 products with 40 or more pins are provided with a subsystem clock.

Note2. For H8/36109,

Functioning: RTC (The timekeeping time-base function is selected)
Reset: Timer V, SCI3, SCI3_2, SCI3_3, A/D converter
Retained: Peripheral modules other than above

Note3. For RL78/G14,

Operable:
Real-time clock (RTC), 12-bit Interval timer, Watchdog timer (Can choose to operate or stop.), Timer RJ, Clock output/buzzer output, D/A converter, ELC, Power-on-reset function, Voltage detection function, Key interrupt function

Partially operable:
A/D converter (operable in SNOOZE mode), Comparator (only when the digital filter is not used and the external input is selected as the reference voltage of the comparator), Serial array unit (operable in SNOOZE mode), Serial interface IICA (Wakeup by address match operable), DTC (DTC activation source receiving operation enabled)

Operation disabled: Timer array unit, Timer RD, Timer RG

Operation stopped: CRC operation function, Illegal-memory access detection function, RAM guard function, SFR guard function

3. Comparison between Registers

Table 7.1 and Table 7.2 compares the registers for the Power-Down Modes of the H8/36109 and the RL78/G14.

Table 7.1 Comparison between Registers (1/2)

Item	H8/36109	RL78/G14
System control register	SYSCR1 register SYSCR2 register SYSCR3 register	None
Software Standby	SYSCR1 register SSBY bit	None
Standby Timer Select	SYSCR1 register STS2 - STS0 bit	OSTS register OSTS2 - OSTS0 bit
Noise Elimination Sampling Frequency Select	SYSCR1 register NESEL bit	None
Sleep Mode Select	SYSCR2 register SMSEL bit	None
Low Speed on Flag	SYSCR2 register LSON bit	None
Direct Transfer on Flag	SYSCR2 register DTON bit	None
Active Mode Clock Select	SYSCR2 register MA2 - MA0 bit	None
Subactive Mode Clock Select	SYSCR2 register SA1 bit, SA0 bit	None
Standby Timer Select	SYSCR3 register STS3 bit	OSTS register OSTS2 - OSTS0 bit
Module Standby Control Register	MSTCR1 register MSTCR2 register MSTCR4 register	PER0 register PER1 register
IIC2 Module Standby	MSTCR1 register MSTIIC bit	PER0 register IICA1EN bit IICA0EN bit
SCI3 Module Standby	MSTCR1 register MSTS3 bit	PER0 register SAU1EN bit SAU0EN bit
Watchdog Timer Module Standby	MSTCR1 register MSTWD bit	None
Timer V Module Standby	MSTCR1 register MSTTV bit	PER0 register TAU1EN bit TAU0EN bit
RTC Module Standby	MSTCR1 register MSTTA bit	PER0 register RTCEN bit

Table 7.2 Comparison between Registers (2/2)

Item	H8/36109	RL78/G14
SCI3_2 Module Standby	MSTCR2 register MSTS3_2 bit	PER0 register SAU1EN bit SAU0EN bit
Timer B1 Module Standby	MSTCR2 register MSTTB1 bit	PER0 register TAU1EN bit TAU0EN bit
PWM Module Standby	MSTCR2 register MSTPWM bit	PER0 register TAU1EN bit TAU0EN bit
Timer RC Module Standby	MSTCR4 register MSTTRC bit	PER0 register TAU1EN bit TAU0EN bit
A/D Converter Module Standby	MSTCR4 register MSTAD bit	PER0 register ADCEN bit
Timer RD_0 Module Standby	MSTCR4 register MSTTRD0 bit	PER1 register TRD0EN bit
Timer RD_1 Module Standby	MSTCR4 register MSTTRD1 bit	None
Control of D/A converter input clock supply	None	PER1 register DACEN bit
Control of timer RG input clock supply	None	PER1 register TRGEN bit
Control of comparator input clock supply	None	PER1 register CMPEN bit
Control of DTC input clock supply	None	PER1 register DTCEN bit
Control of timer RJ0 input clock supply	None	PER1 register TRJ0EN bit
Subsystem clock supply mode control register	None	OSMC register
Setting in STOP mode or HALT mode while subsystem clock is selected as CPU clock	None	OSMC register RTCLPC bit
Selection of operation clock for real-time clock, 12-bit interval timer, and timer RJ	None	OSMC register WUTMMCK0 bit

4. Sample Code for Standby function

The sample code for Standby function is explained in the following application notes.

- RL78/G13 CPU Clock Changing and Standby Settings (C Language) CC-RL (R01AN3128)
- RL78/G13 CPU Clock Changing and Standby Settings (Assembly) CC-RL (R01AN2912)

5. Documents for Reference

User's Manual:

- RL78/G14 User's Manual: Hardware (R01UH0186)
- H8/36109 Group User's Manual: Hardware (R01UH0294)

The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News:

The latest information can be downloaded from the Renesas Electronics website.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Sep.04, 2020	-	First edition issued

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1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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(Rev.5.0-1 October 2020)

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