RL78/G10

Interval Timer Using Interrupt Function of Watchdog Timer (With Clock Correction)

Introduction

This application note explains realizing method of the interval timer which uses interval interruption of a watchdog timer (WDT), without using a timer array unit (TAU). In this application note, frequency calibration is performed by software and interval timer accuracy is raised to less than ±3%. (Less than or equal to ±3% of accuracy is actual measurement in ambient temperature 25ºC.)

Target Device

RL78/G10

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Specifications

In this application note, the interval timer which can be set up from 100 ms to 500 ms (every 100 ms) using WDT is realized. The interval timer counts and generates the interval time for 100 ms.
The main program stands by interruption (INTWDTI) of a watchdog timer in the STOP mode after initial setting of an interval timer. The interval time for 100 ms measures the number of times of generating of INTWDTI at counting by software. The interval time for 100 ms is calibrated by adjusting this number of times of counting.

The LED drive will be reversed if the setup interval time (100 ms to 500 ms) lapses. Interval time is set up by the number of times of keypress of SW1 (INTP0). When SW1 is pressed, INTP0 occurs and it counts up the number of times of having been pressed.
Interval time is set as 100 ms after reset, and whenever SW1 is pressed, 100 ms is added. When SW1 is pressed in the state of 500 ms interval time, an interval returns to 100 ms.

Table 1.1 shows the peripheral function to be used and its use.
Figure 1.1 shows the overview of operations.
Figure 1.2 shows the interval timer operation using WDT.

Specific method to calibrate the interval time is described in “1.1 Accuracy Calibration of Interval Time” and “1.2 Accuracy Calibration of Interval Time during Operation”.

Table 1.1 Peripheral Function to be Used and its Use

Peripheral Function	Use
Watchdog timer	The base time of the interval timer is made by interval interruption of WDT.
INTP0 (External interrupt)	Changes the interval time of interval timer.

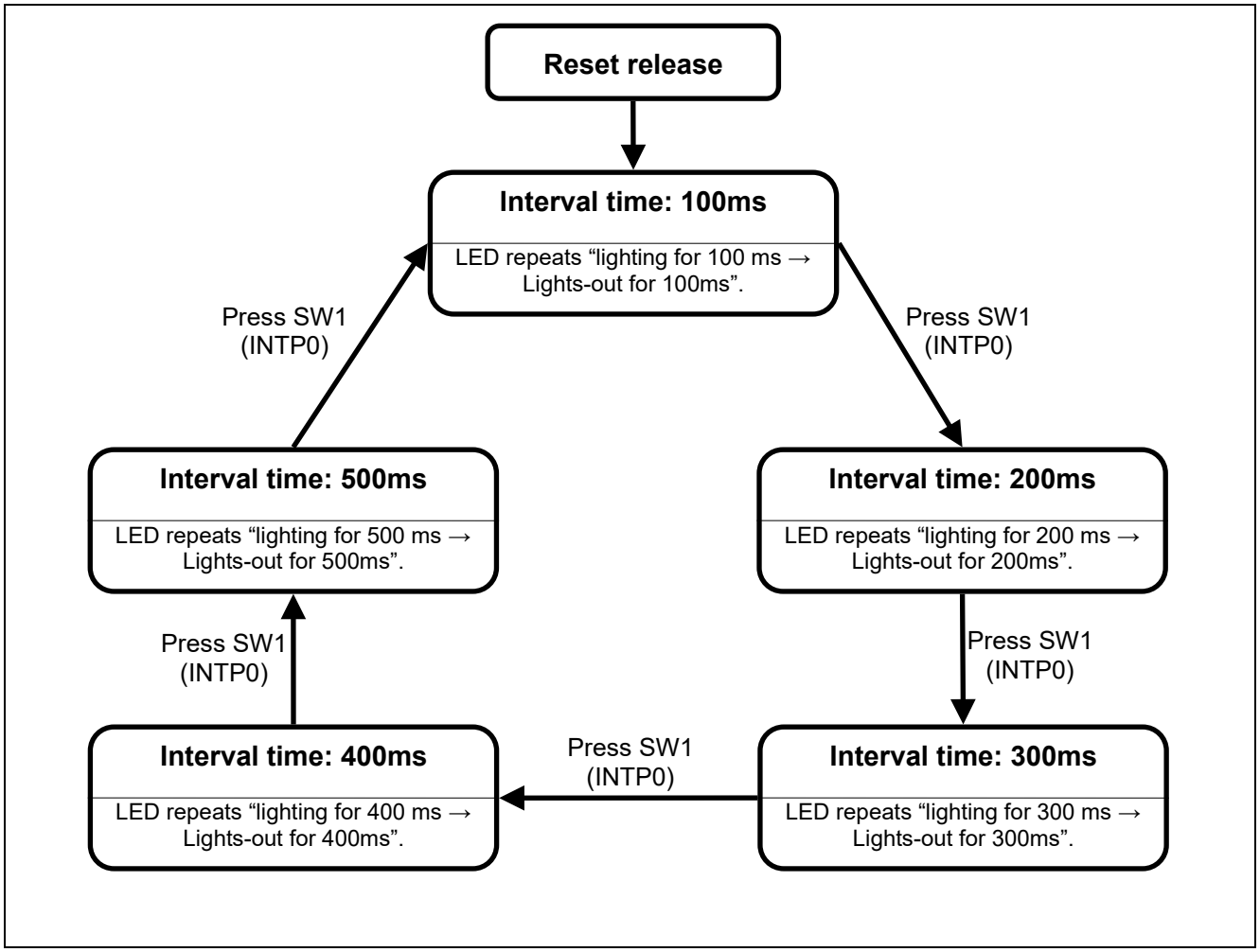

Figure 1.1 Overview of Operations

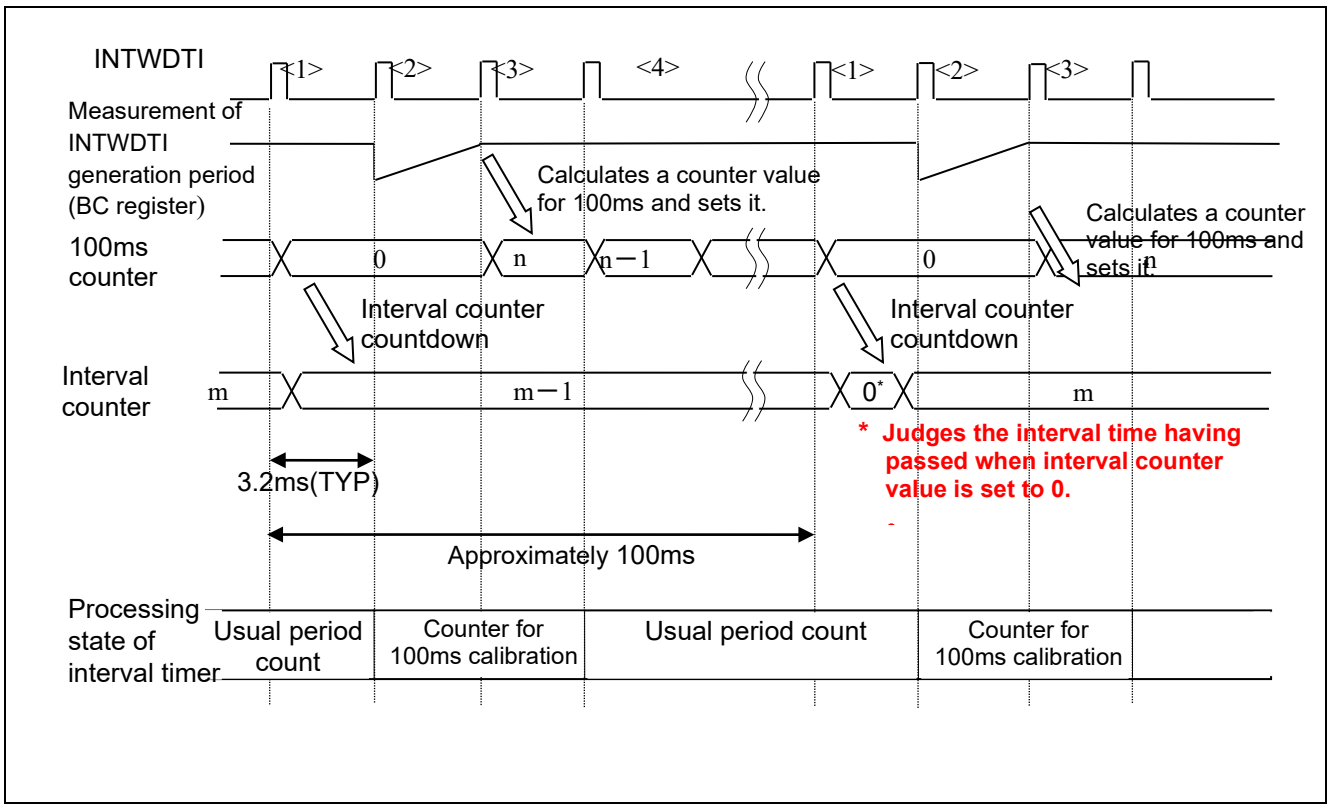

Figure 1.2 Interval Timer Operation using WDT

<1>. An interval counter will be counted down, if the usual period count is performed and a counter is set to 0 for 100 ms.

<2>. Performs 100ms counter calibration processing when INTEDTI is generated in the state of 100ms counter is set to 0. Generation period of INTWDTI is measured by the software. Waits for generating of INTWDTI, counting up BC register used for the generating period measurement of INTWDTI.

<3>. Using the generation period (BC register value) of INTWDTI measured in the procedure<2>, the number of times of generating INTWDTI for approximately 100 ms is calculated, and it is set to the 100 ms counter.

<4>. The usual period count is performed. Whenever INTWDTI occurs, counts down 100ms counter.

1.1 Accuracy Calibration of Interval Time

(1) Period measurement of INTWDTI

Measures the generation period of INTWDTI by software. Figure 1.3 shows a period measurement program. This program clears WDT, and then counts BC register until INTWDTI is generated. Since the number of instruction execution clocks of CLOOP in this program is 7, if CPU clock is operated by 10MHz, execution of a CLOOP takes 0.7us. Since the count value of BC register is 5378 when INTWDTI's cycle is the longest (3.76 ms ($=2^6/(15kHz-15\%) \times 0.75$)), realization is fully possible by 16-bit BC register.

```
      MOV    WDTE,  #0ACH       ; clear watch dog timer
CLOOP:
      INCW   BC                 ; Count up (2 clocks)
      BF     WDTIIF, $CLOOP     ; Wait for WDTI interrupt (5 clocks)
```

Figure 1.3 INTWDTI Period Measurement by Software

(2) The calculation method of a 100ms counter.

Based on the result of measuring period of INTWDTI, calculates the number of times of INTWDTI generation which uses the closest time to 100 ms.

Generation period of INTWDTI is calculated by the following formula.

Generation period of INTWDTI = $2^6 / f_{IL} \times 0.75$

f_{IL}: Low-speed on-chip oscillator (LOCO) frequency

Since the accuracy of f_{IL} is 15kHz±15%, generation period of INTWDTI is from 2.783ms to 3.765ms. Therefore, the number of times of INTWDTI generation to use the time which is the closest to 100 ms will be 27 to 36 times.

Next, judgment conditions are calculated in order to calculate the number of times of INTWDTI generation from the count value of BC register which uses for 100 ms. In order to judge which shall become the number of times of INTWDTI generation between 27 and 28, BC counted value when the number of times of INTWDTI generating which is an intermediate value is 27.5 is calculated. Similarly, calculates BC count value (C) at the time that the number of times of INTWDTI generation is from 28.5 to 35.5 (on 1 to 1 basis). (Refer to Table 2.1.)

Table 1.2 The Number of Times of INTWDTI Generation to Use the Closest to 100 ms

(A) The number of times of count	(B) Note Period (ms) = (100ms / (A))	(C) BC count value =((B) / 0.7us)	(D) =((C) / 128)	(E) 66－(D)	The number of times that INTWDTI generation occurs for 100 ms.
27.5	3.64	5194	40	26*	27
28.5	3.51	5012	39	27*	28
29.5	3.39	4842	37	29	29
30.5	3.28	4683	36	30	30
31.5	3.17	4535	35	31	31
32.5	3.08	4395	34	32	32
33.5	2.99	4264	33	33	33
34.5	2.90	4140	32	34	34
35.5	2.82	4024	31	35	35
-	-	-	-	-	36*1

Note In this table, the value rounded off with the third place of the decimal is indicated.

* Target of calibration.

In order to compute simply this number of times of INTWDTI generation takes about 100 ms, asks for the approximate expression using the counted value (C) of BC register. If the counted value (C) of BC register is divided by 128 (A 1-bit shift to the left is carried out in fact, and the value of B register is taken), the result of an integer will be obtained mostly. In order to adjust this value of (D) to 27 to 36 which is the number of times of INTWDTI generation, the value of (D) is subtracted from 66. (E) If 1 is added to the discontinuous calibration of (E) (*), the continuous integral values from 27 to 36 will be acquired.

The program which performs this processing is Figure 1.4, and it is a program takes 7clocks.

```
SHLW   BC,    1          ; 1bit shift left
MOV    A,     #66
SUB    A,                ; get loop count data
CMP    A,     #28        ; check less than 28
SKNC
INC    A,                ; adjust +1 if 27 or 26
```

Figure 1.4 The Program which Calculates the Number of Times of INTWDTI Generating for 100 ms

The 100 ms counter is realized by above-mentioned processing.

1.2 Accuracy Calibration of Interval Time during Operation

In order to maintain the accuracy of the interval time of the interval timer which uses the interruption function of a watchdog timer, it is necessary to perform measurement and calibration of interval time periodically. In this application note, when starting the count for 100 ms, measurement and calibration of INTWDTI generation period are performed.

1.3 Actual Measured Value of Interval Timer (Reference)

Table 1.3 Actual Measured Value of Interval Timer (TA = 25ºC) realized in this application note. Actual measured values in Table 1.3 are results in ambient temperature (TA) = 25ºC.
Since the relative error of 100ms which is the standard of each interval time is 2.3%, the relative error for 200ms to 500ms is 2.3% similarly.

Table 1.3 Actual Measured Value of Interval Timer (T_A = 25ºC)

Target value (ms)	Actual measured value (ms)	Relative error (%)
100	97.7	2.3
200	195.4	2.3
300	293.1	2.3
400	390.7	2.3
500	488.4	2.3

2. Operation Check Conditions

The sample code contained in this application note has been checked under the conditions listed in the table below.

Table 2.1 Operation Check Conditions

Item	Description
Microcontroller used	RL78/G10 (R5F10Y16)
Operating frequency	• High-speed on-chip oscillator (HOCO) clock: 10 MHz • CPU/peripheral hardware clock: 10 MHz
Operating voltage	5.0 V (Operation is possible over a voltage range of 2.9 to 5.5 V.) SPOR Operating Voltage: Rising voltage: 2.90V Falling voltage: 2.84V
Integrated development environment (CubeSuite+)	CubeSuite+ V2.02.00 from Renesas Electronics Corp.
Assembler (CubeSuite+)	RA78K0R V1.90 from Renesas Electronics Corp.
Integrated development environment (e2studio)	e2studio V2.2.0.13 from Renesas Electronics Corp.
Assembler (e2studio)	KPIT GNURL78-ELF Toolchain V14.0.1 from Renesas Electronics Corp.
Board to be used	RL78/G10 target board (QB-R5F10Y16A-TB)

3. Related Application Note

The application note that is related to this application note is listed below for reference.

RL78/G10 Initialization (R01AN1454E) Application Note

4. Description of the Hardware

4.1 Hardware Configuration Example

Figure 4.1 shows an example of hardware configuration that is used for this application note.

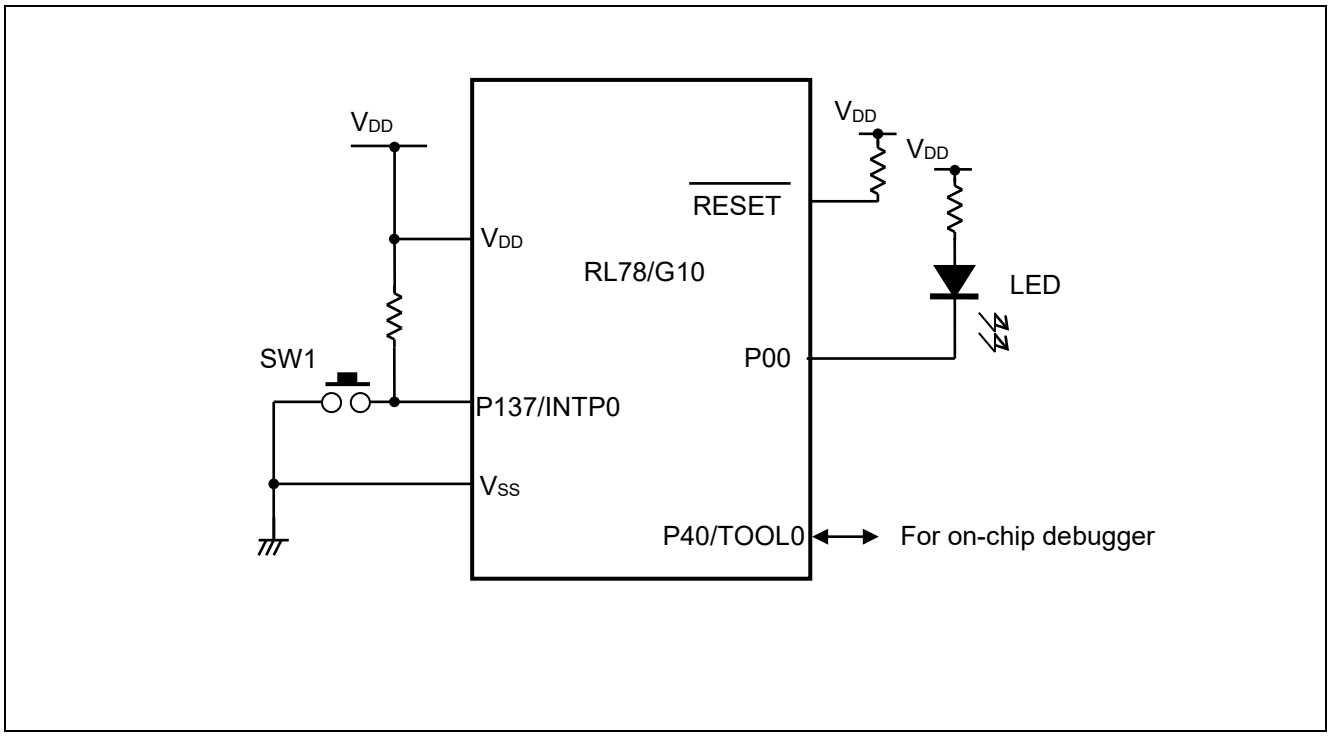

Figure 4.1 Hardware Configuration

Caution: 1. The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical specifications are met (connect the input-only ports separately to V_{DD} or V_{SS} via a resistor).

2. V_{DD} must be held at not lower than the reset release voltage (V_{SPOR}) that is specified by SPOR.

4.2 List of Pins to be Used

Table 4.1 lists the pins to be used and their function.

Table 4.1 Pins to be Used and their Functions

Pin Name	I/O	Description
P00	**Output**	Port for LED drive
P137/INTP0	**Input**	Switch input for interval time setup (SW1)

5. Description of the Software

5.1 Operation Outline

In this application note, waits for INTWDTI generating in the STOP mode after initial setting of an interval timer at a main program.

At the time of the count start for 100 ms, accuracy calibration of the interval time is performed. The generation period of INTWDTI is counted by software and a 100ms counter (variable TIMEBASE) is set up from the result. After that, 100ms counter (variable TIMEBASE) is counted down to the every INTWDTI generating.

The switch (SW1) input for interval time setting is always received. If SW1 is pressed, a processing for countermeasure against chattering is performed. If INTP0 interrupt occurs by keypress of SW1, INTP0 interruption is disabled, the counter for a chattering measure (variable CHATCOUNT) will be set up, and INTP0 interruption will be disabled. Whenever INTWDTI occurs, the counter for a chattering measure (variable CHATCOUNT) is counted down, and if chattering removal time passes (variable CHATCOUNT = 0), the input level of P137-/INTP0 pin will be checked. If P137-/INTP0 pin is a low level, it will judge with SW1 having been pushed, and INTP0 interruption is permitted again, and the counter for the number of times of keypress of SW1 (variable KEYCOUNT) is counted up. The data corresponding to the counter for the number of times of keypress of SW1 (variable KEYCOUNT) is set as an interval counter (variable PERIOD) as next interval time.

100ms counter (variable TIMEBASE) counts down whenever INTWDTI occurs, and when it becomes the timing for 100 ms (variable TIMEBASE = 0), it will count down an interval counter (variable PERIOD). If the set-up interval time passes (variable PERIOD = 0), the drive of LED will be reversed and the data corresponding to the counter for the number of times of keypress of SW1 (variable KEYCOUNT) will be set as an interval counter (variable PERIOD) as next interval time.

(1) Initializes peripheral functions to be used.

<Setting conditions>

a) Carries out the mask of the INTWDTI interruption and sets an interrupt-priorities level to a high priority.

b) Sets the valid edge of INTP0 as the falling edge detection, and release the interrupt mask of INTP0.

(2) Initializes variables to be used.

a) Sets the address of the processing for countermeasure against chattering (label: IINTWDTISUB) to the branch destination address in an INTWDTI interrupt handler (variable: PROCEDURE).

b) Clears the counter (variable KEYCOUNT) for the number of times of keypress of SW1.

c) Clears the counter (variable CHATCOUNT) for countermeasure against chattering.

(3) Starts count of 100ms counter and measures the time to INTWDTI generating.

a) Clears BC register which is used for measuring generation period of INTWDTI.

b) Clears the counter of WDT.

c) Waits for generating of INTWDTI, counting up BC register.

d) If INTWDTI occurs, the number of times of INTWDTI generation which uses the closest time to 100 ms will be calculated based on the generation period (BC register value) of INTWDTI, and it will set to a 100ms counter (variable TIMEBASE).

(4) Sets the interval time.

Sets the value of interval storing table “TINTVL[KEYCOUNT]” to Interval setting variable “PERIOD”. After reset, KEYCOUNT is cleared before this processing, and TINTVL [KEYCOUNT] is set to 1. Therefore, the interval time after reset is set as 100ms (PERIOD=1).

(5) Switches off LED, releases interrupt mask of INTWDTI, and enables vector interrupt.

(6) Shifts to STOP mode and stands by interruption. The main program executes a STOP command by an infinite loop. All subsequent program processing is performed by the interrupt handler of INTP0, or the interrupt handler of INTWDTI.

(7) If INTP0 interrupt occurs, sets 9 to the counter for countermeasure against chattering (variable CHATCOUNT), disables INTP0 interruption, and escapes from processing.

(8) Generating of INTWDTI will perform chattering measure processing and 100ms count processing.

Generating of INTWDTI will run the program in the interrupt handler which is accepted by release of STOP mode. (From STOP mode release to start interruption processing, it will take tens us of the STOP release time. This is about 1 to 2% of INTWDTI generation period of 3.2ms. At the time of accuracy calibration of a 100ms counter, this STOP release time is rectified by the initial value of BC register.) The flow of concrete processing is shown below.

a) Clears WDT counter.

b) During the count operation for 100ms, chattering measure processing and 100ms count processing are performed.

The flow of chattering measure processing is shown below.

- When counted value for countermeasure against chattering (variable CHATCOUNT) is 0, moves to 100ms count processing. When counted value for countermeasure against chattering (variable CHATCOUNT) is other than 0, counts down the variable of CHATCOUNT.
- When Variable CHATCOUNT is set to zero and chattering judging waiting time passes, INTP0 interruption is permitted and the input level of P137/INTP0 pin is checked.

  When the variable of CHATCOUNT is other than 0, moves to 100ms count processing.
- If the input logic of P137/INTP0 pin is low level, judges that SW1 is pushed, and counts up the counter (variable KEYCOUNT) for the number of times of SW1 keypress.

  If the input logic of P137/INTP0 pin is high level, judges that SW1 is not pushed, and moves to the 100ms count processing.
- When the number of times of SW1 keypress (variable KEYCOUNT) exceeds the range of the interval table TINTVL, clears the number of times of SW1 keypress, and shifts to 100ms count processing.

The flow of 100ms count processing is shown below.

- Counts down the 100ms counter (variable TIMEBASE).
- When the value of 100ms counter (variable TIMEBASE) is 0, counts down the interval counter (variable PERIOD).

  When the value of 100ms counter (variable TIMEBASE) is other than 0, executes following processes.
- When the value of interval counter (variable PERIOD) is 0 (specified interval is completed), sets he value (variable TINTVL [KEYCOUNT]) of an interval table to an interval counter (variable PERIOD), and reverses the drive of LED. Next, Sets the address of measurement processing (label: MEASURESUB) of the time to INTWDTI generating to the branch destination address in an INTWDTI interrupt handler (variable PROCEDURE).

  When the value of interval counter (variable PERIOD) is 0, executes following processes.

At the time of the count start for 100 ms, performs chattering measure processing and 100ms count processing after the generation period measurement of INTWDTI.

The flow of measuring generation period of INTWDTI is shown below.

- Sets the constant TMOFFSET + 1 to BC register as the initial value.

  In this application note, the constant TMOFFSET is set to 40. STOP mode release time takes 28.1us because it is 27us (TYP) + 11 clocks (if vector interrupt is performed) and RL78/G10 is operated by 10MHz in this application note. Since count-up of BC register takes 7 clocks (0.7us), the offset value is calculated as follows.

  $$TMOFFSET = (27us + 11 \times 0.1us) \div 0.7us = 40$$

  In order to reflect 6 clocks because of following 3 reasons, 1 is added to TMOFFSET. Before performing count-up processing of BC register, the contents of the BC register are evacuated to a stack (2 clocks). Sets the initial value to BC register (1 clock). And branches to BC register count-up processing (3 clocks).

  Refer to ‘RL78/G10 User's Manual: Hardware’ for more information about STOP mode release time.
- Waits for generating of INTWDTI, counting up BC register.
- If INTWDTI occurs, calculates the number of times of INTWDTI generating for about 100ms based on BC register value, and sets it to the 100ms counter (variable TIMEBASE).
- Counts down the 100ms counter (variable TIMEBASE).
- Sets the address of chattering measure processing (label: IINTWDTISUB)to the branch destination address in an INTWDTI interrupt handler (variable PROCEDURE), and performs chattering measure processing and 100-ms count processing.

5.2 List of Option Byte Settings

Table 5.1 summarizes the settings of the option bytes.

Table 5.1 Option Byte Settings

Address	Value	Description
000C0H/010C0H	11110001B	Enables watchdog timer operation. • Starts count after reset release. • Interval interrupt time: 2^6 / f_{IL} × 0.75 • Enables counter operation at the HALT/STOP mode.
000C1H/010C1H	11110111B	P125/RESET Pin: RESET input (On-chip pull-up resistance is always valid.) SPOR voltage Rising voltage: 2.90 V Falling voltage: 2.84 V
000C2H/010C2H	11111010B	HOCO : 10 MHz
000C3H/010C3H	10000101B	Enables the on-chip debugger.

5.3 List of Constants

Table 5.2 lists the constants that are used in this sample program.

Table 5.2 Constants for the Sample Program

Constant	Setting	Description
TMOFFSET	**40**	Offset value of BC register (BC register counted value for STOP mode release time)
CHATNo	**9**	INTWDTI counted value for countermeasure against chattering. In order to remove chattering, checks the input logic of a P137-/INTP pin after waiting for 9 times of INTWDTI occurrence following INTP0 generation.

5.4 List of Variables

Table 5.3 lists the variables that are used in this sample program.

Table 5.3 Variables for the Sample Program

Type	Variable Name	Contents	Function Used
8 bits arrays	TINTVL	Interval table	IINTWDTI、SETINTERVAL
1 bits	PROCEDURE	The branch destination address in an INTWDTI interrupt handler. It is set as (label: MEASURESUB) at the time of 100ms count starting, and as (label: IINTWDTISUB) under 100ms counting.	main、IINTWDTI、
8 bits	KEYCOUNT	Counter for the number of times of keypress of SW1	main、IINTWDTI、SETINTERVAL
8 bits	CHATCOUNT	Counter for countermeasure against chattering	main、IINTWDTI
8 bits	TIMEBASE	100ms counter	main、IINTWDTI
8 bits	PERIOD	Interval counter	IINTWDTI、SETINTERVAL

5.5 List of Functions (Subroutines)

Table 5.4 lists the functions (subroutines).

Table 5.4 Functions (Subroutines)

Function Name	Outline
RESET_START	**Initialization of CPU**
SINIPORT	**Setup of I/O port**
SINICLK	**Setup of the clock generator**
SINIINTP0	Initialization of INTP0
SINIWDT	Initialization of INTWDTI
SETINTERVAL	Setup of interval
GETINTERVAL	Measuring INTWDTI generation period (Clears the counter of BC register and WDT before measurement.)
CLOOP	Measuring INTWDTI generation period (Does not clears the counter of BC register and WDT before measurement.)
IINTP0	INTP0 Interrupt servicing
IINTWDTI	INTWDTI Interrupt servicing

5.6 Function Specifications

This section describes the specifications for the functions that are used in this sample program.

[Function Name] RESET_START

Synopsis	Initialization of CPU in the case of reset/start
Explanation	Calls main processing after setting up of the stack pointer and initialization of the hardware.
Arguments	• None
Return value	• None
Remarks	None

[Function Name] SINIPORT

Synopsis	Initialization of P0
Explanation	Sets P01/AN10 to P04/ANI3 pins as the digital output.
Arguments	• None
Return value	• None
Remarks	None

[Function Name] SINICLK

Synopsis	Initialization of HOCODIV
Explanation	Sets the frequency of high-speed on-chip oscillator clock to 10MHz.
Arguments	• None
Return value	• None
Remarks	None

[Function Name] SINIINTP0

Synopsis	Initialization of INTP0
Explanation	Sets INTP0 as falling edge detection.
Arguments	• None
Return value	• None
Remarks	None

[Function Name] SINIWDT

Synopsis	Initialization of INTWDTI
Explanation	Sets the 75% interval interrupt priorities of WDT to the level 0 (top priority).
Arguments	None
Return value	None
Remarks	None

[Function Name] SETINTERVAL

Synopsis	Setup of interval
Explanation	Reads the interval according to the number of times of SW1 keypress from a table, and sets to the variable (PERIOD) for a count.
Arguments	None
Return value	None
Remarks	Refers to variable KEYCOUNT.

[Function Name] GETINTERVAL

Synopsis	Measuring INTWDTI generation period (Clears counters of BC register and WDT)
Explanation	Calculates the number of times of INTWDTI generation which uses the closest time to 100 ms by measuring an INTWDTI generating cycle, after clearing BC register and clearing the counter of WDT, and sets a calculation result to 100ms counter (variable TIMEBASE).
Arguments	None
Return value	None
Remarks	None

[Function Name] CLOOP

Synopsis	Measuring INTWDTI generation period
Explanation	The number of times of INTWDTI generation which uses the closest time to 100 ms is calculated by measuring an INTWDTI generation period, and sets a calculation result to a counter (variable TIMEBASE) for 100ms.
Arguments	None
Return value	None
Remarks	None

[Function Name] IINTP0

Synopsis	INTP0 interruption
Explanation	Receives the INTP0 interruption and sets a chattering prevention counter. Disables INTP0 interruption (mask).
Arguments	None
Return value	None
Remarks	None

[Function Name] IINTWDTI

Synopsis	WDT75% interval interruption
Explanation	Receives INTWDTI interruption and performs chattering measure processing at the time of SW1 keypress. Moreover, performs 100ms counter processing, and reverses LED when the set-up interval time passes.
Arguments	None
Return value	None
Remarks	None

5.7 Flowcharts

Figure 5.1 shows the overall flow of the sample program described in this application note.

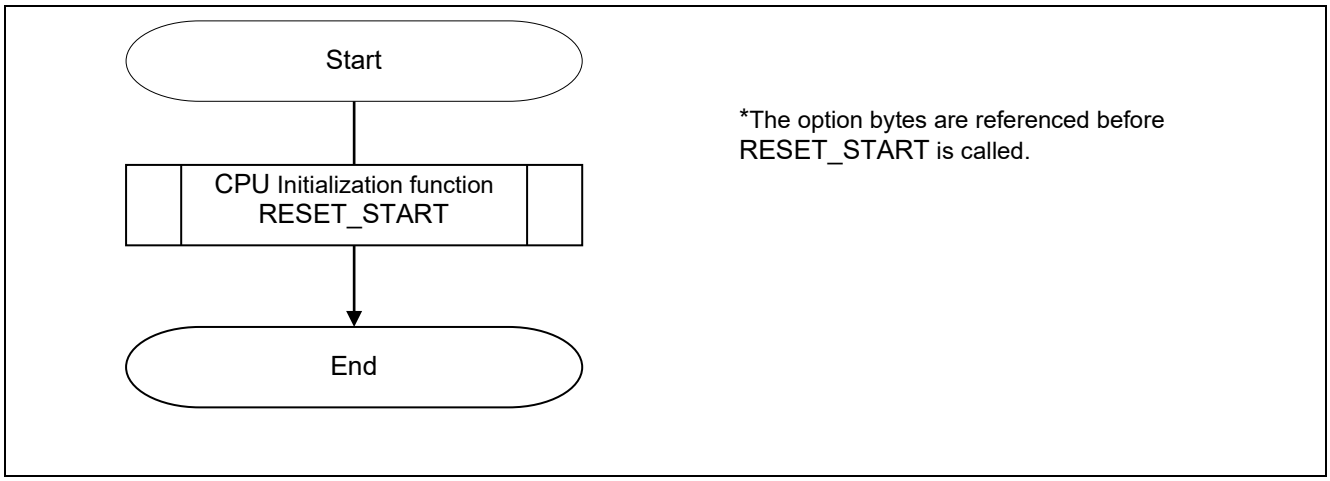

Figure 5.1 Flowchart of Overall

5.7.1 CPU Initialization Function

Figure 5.2 shows the flowchart for the CPU initialization function.

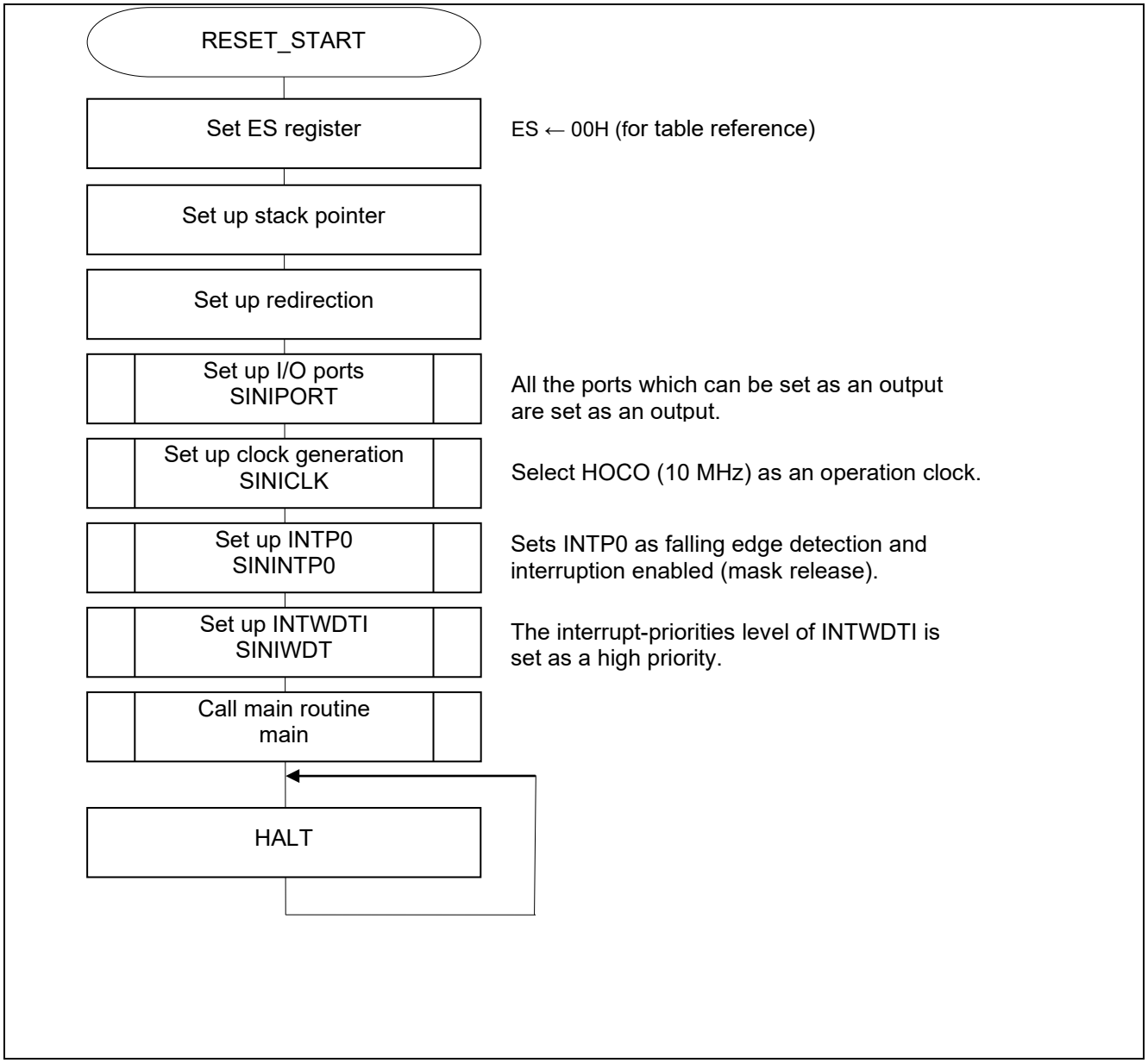

Figure 5.2 CPU Initialization Function

5.7.2 I/O Port Setup

Figure 5.3 shows the flowchart for I/O port setup.

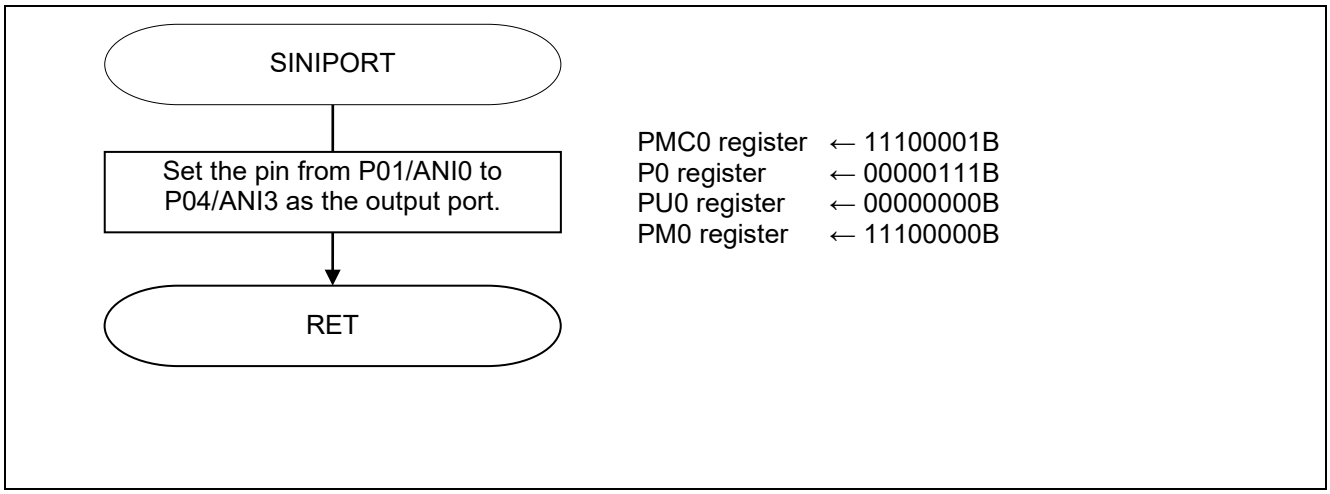

Figure 5.3 I/O Port Setup

Setup of the port mode.

- Port Mode Control Register 0 (PMC0)

  Switching between analog input and digital I/O.

- Port Register 0(P0)

  Setup of an output latch of each port

- Pull-up Resistor Option Register 0 (PU0)

  On-chip pull-up resistor selection.

- Port Mode Register 0 (PM0)

  Selection of the I/O mode of each port.

Symbol: PMC0

7	6	5	4	3	2	1	0
1	1	1	PMC04	PMC03	PMC02	PMC01	1
1	1	1	**0**	**0**	**0**	**0**	1

Bit 4 to 1

PMC0n	P0n pin digital I/O/analog input selection
0	**Digital I/O (alternate function other than analog input)**
1	Analog input

Note: Refer to ‘RL78/G10 User's Manual: Hardware’ for more information about the register setting method.

Symbol: P0

7	6	5	4	3	2	1	0
0	0	0	P04	P03	P02	P01	P00
0	0	0	x	x	x	x	**1**

Bit 0

P00	P00 pin output data control
0	Output 0
1	**Output 1**

Symbol: PM0

7	6	5	4	3	2	1	0
1	1	1	PM04	PM03	PM02	PM01	PM00
1	1	1	**0**	**0**	**0**	**0**	**0**

Bit 4 to 0

PM0n	P0n pin I/O mode selection
0	**Output mode (output buffer on)**
1	Input mode (output buffer off)

Symbol: PU0

7	6	5	4	3	2	1	0
0	0	0	PU04	PU03	PU02	PU01	PU00
0	0	0	**0**	**0**	**0**	**0**	**0**

Bit 4 to 0

PU0n	P0n pin on-chip pull-up resistor selection
0	On-chip pull-up resistor not connected
1	On-chip pull-up resistor connected

Note: Refer to ‘RL78/G10 User's Manual: Hardware’ for more information about the register setting method.

5.7.3 Clock Generation Circuit Setup

Figure 5.4 shows the flowchart for clock generation circuit setup.

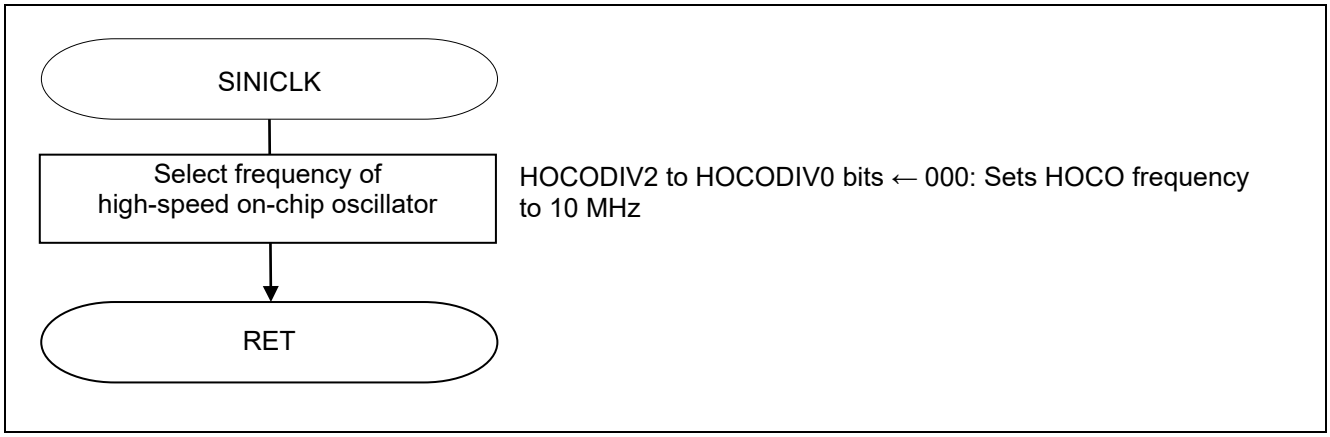

Figure 5.4 Clock Generation Circuit Setup

Selection of high-speed on-chip oscillator frequency.

- High-Speed On-Chip Oscillator Frequency Selection Register (HOCODIV)
  Selects the frequency of high-speed on-chip oscillator.

Symbol: HOCODIV

7	6	5	4	3	2	1	0
0	0	0	0	0	HOCODIV2	HOCODIV1	HOCODIV0
0	0	0	0	0	**0**	**1**	**0**

Bit 2 to 0

HOCODIV			High-speed on-chip oscillator clock frequency
2	1	0	
0	0	1	20MHz
0	**1**	**0**	**10MHz**
0	1	1	5MHz
1	0	0	2.5MHz
1	0	1	1.25MHz
Other than above			Setting prohibited

Note: Refer to ‘RL78/G10 User's Manual: Hardware’ for more information about the register setting method.

5.7.4 INTP0 Initialization

Figure 5.5 shows the flowchart for INTP0 Initialization.

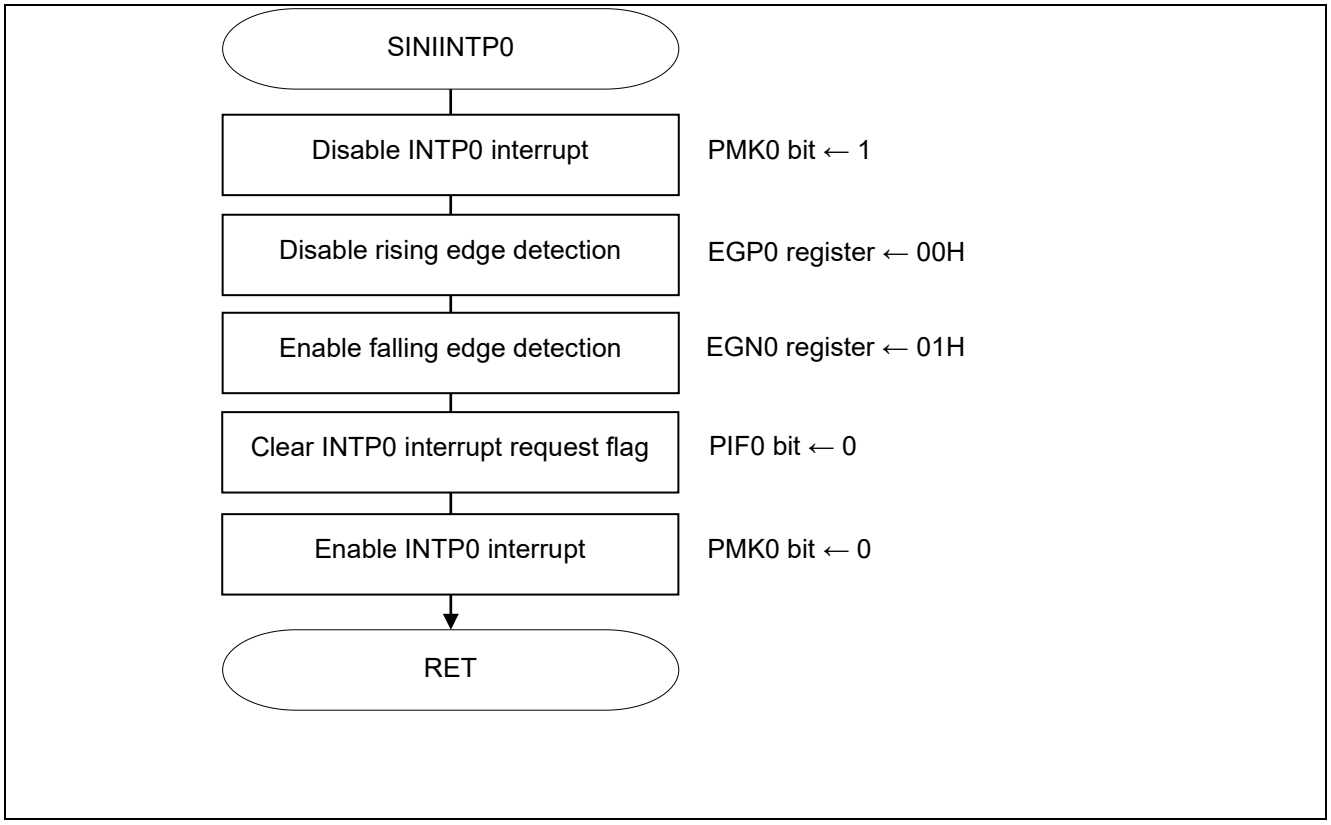

Figure 5.5 INTP0 Initialization

(1) Setup INTP0 pin edge detection.

・ External interrupt rising/falling edge enable register (EGP0、EGN0)

This register specifies the valid edge for INTP0.

Symbol: EGP0

7	6	5	4	3	2	1	0
0	0	0	0	EGP3[Note]	EGP2[Note]	EGP1	EGP0
0	0	0	0	x	x	x	**0**

Note 16-pin products only.

Symbol: EGN0

7	6	5	4	3	2	1	0
EGN7	EGN6	EGN5	EGN4	EGN3	EGN2	EGN1	EGN0
x	x	x	x	x	x	x	**1**

EGP0	EGN0	INTPn pin valid edge selection
0	0	Edge detection disabled
0	**1**	Falling edge
1	0	Rising edge
1	1	Both rising and falling edges

Note: Refer to ‘RL78/G10 User's Manual: Hardware’ for more information about the register setting

(2) Setup INTP0 edge detection interrupt.

- Interrupt request flag register (IF0L)

  Clears interrupt request flag.

- Interrupt mask flag register (MK0L)

  Sets up the interrupt mask flag.

Symbol: IF0L

7	6	5	4	3	2	1	0
TMIF00	TMIF01H	SREIF0	SRIF0	STIF0 CSIIF00 IICIF00	PIF1	PIF0	WDTIIF
x	x	X	x	x	x	**0**	x

Bit 1

PIF0	Interrupt request flag
0	No interrupt request signal is generated
1	Interrupt request is generated, interrupt request status

Symbol: MK0L

7	6	5	4	3	2	1	0
TMMK00	TMMK01H	SREMK0	SRMK0	STMK0 CSIMK00 IICMK00	PMK1	PMK0	WDTIMK
x	x	x	x	x	x	**0/1**	x

Bit 1

PMK0	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Note: Refer to ‘RL78/G10 User's Manual: Hardware’ for more information about the register setting method.

5.7.5 INTWDTI Initialization

Figure 5.6 shows the flowchart for INTWDTI Initialization.

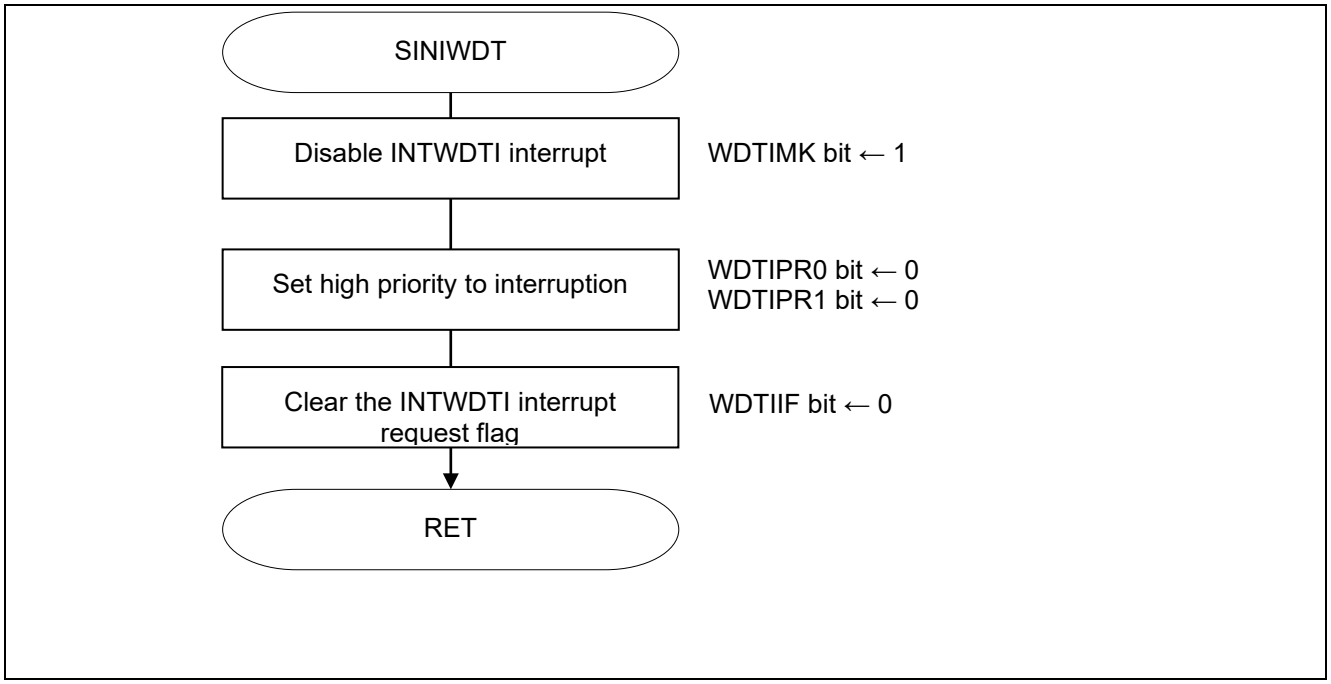

Figure 5.6 INTWDTI Initialization

(1) Setup of INTWDTI interrupt

- Interrupt request flag register (IF0L)

  Clears the interrupt request flag.

- Interrupt mask flag register (MK0L)

  Sets up the interrupt mask.

Symbol: IF0L

7	6	5	4	3	2	1	0
TMIF00	TMIF01H	SREIF0	SRIF0	STIF0 CSIIF00 IICIF00	PIF1	PIF0	WDTIIF
x	x	x	x	x	x	x	**1**

Bit 0

WDTIIF	Interrupt request flag
0	No interrupt request signal is generated
1	Interrupt request is generated, interrupt request status

Symbol: MK0L

7	6	5	4	3	2	1	0
TMMK00	TMMK01H	SREMK0	SRMK0	STMK0 CSIMK00 IICMK00	PMK1	PMK0	WDTIMK
x	x	x	x	x	x	x	**0/1**

Bit 0

WDTIMK	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Note: Refer to ‘RL78/G10 User's Manual: Hardware’ for more information about the register setting method.

(2) Setup of an interruption priority

・ Priority specification flag register (PR00L、PR10L)

Clears the interrupt request flag.

Symbol: PR00L

7	6	5	4	3	2	1	0
TMPR000	TMPR001H	SREPR00	SRPR00	STPR00 CSIPR000 IICPR000	PPR01	PPR00	WDTIPR0
x	x	x	x	x	x	x	**0**

Symbol: PR10L

7	6	5	4	3	2	1	0
TMPR100	TMPR101H	SREPR10	SRPR10	STPR10 CSIPR100 IICPR100	PPR11	PPR10	WDTIPR1
x	x	x	x	x	x	x	**0**

xxPR1x	xxPR0x	Priority Level Selection
0	**0**	Specifying level 0 (high priority)
0	1	Specifying level 1
1	0	Specifying level 2
1	1	Specifying level 3 (low priority)

Note: Refer to ‘RL78/G10 User's Manual: Hardware’ for more information about the register setting method.

5.7.6 Main Processing

Figure 5.7 shows the flow chart for main processing.

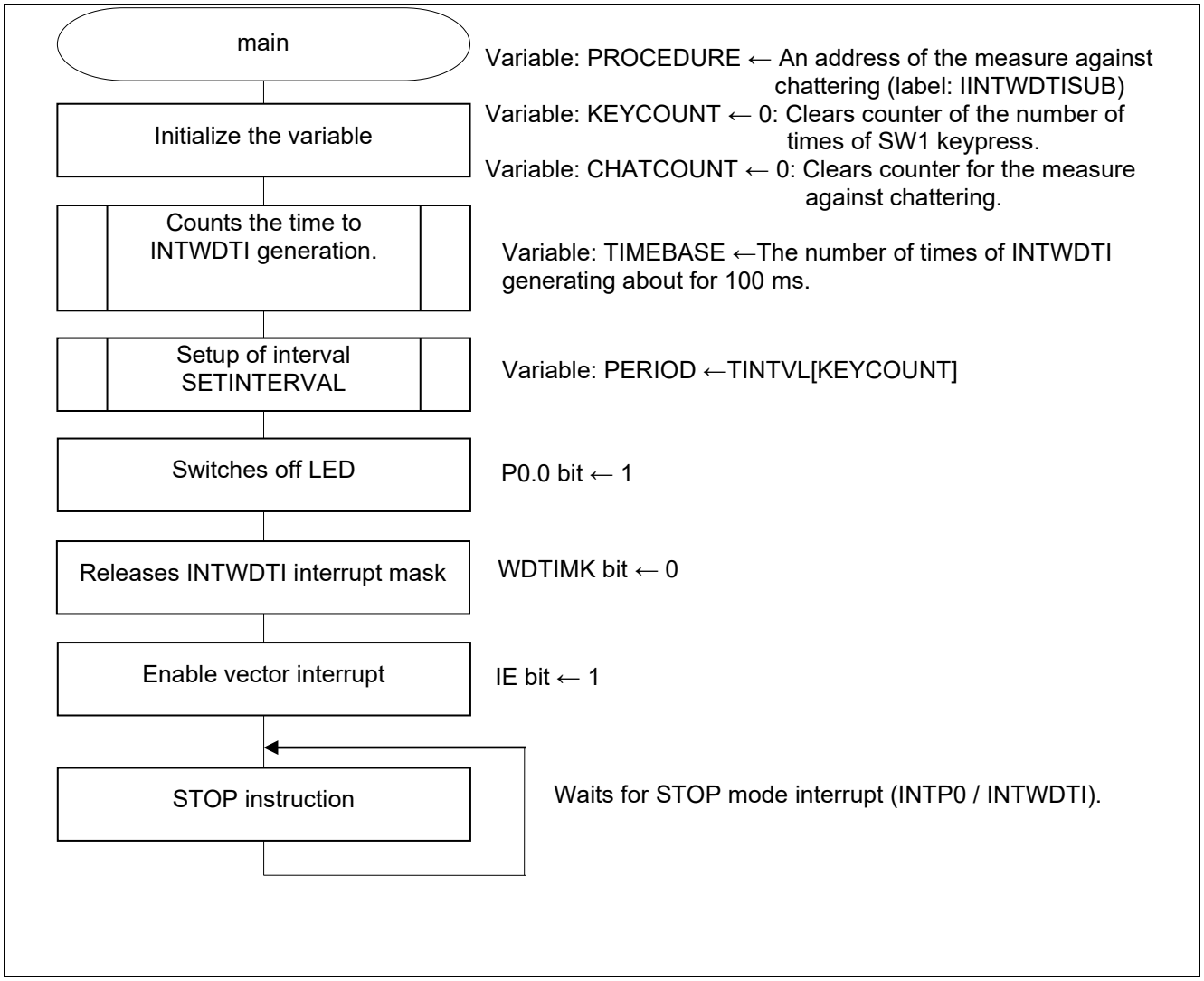

Figure 5.7 Main Processing

5.7.7 Interval Setup

Figure 5.8 shows the flow chart for the interval setup.

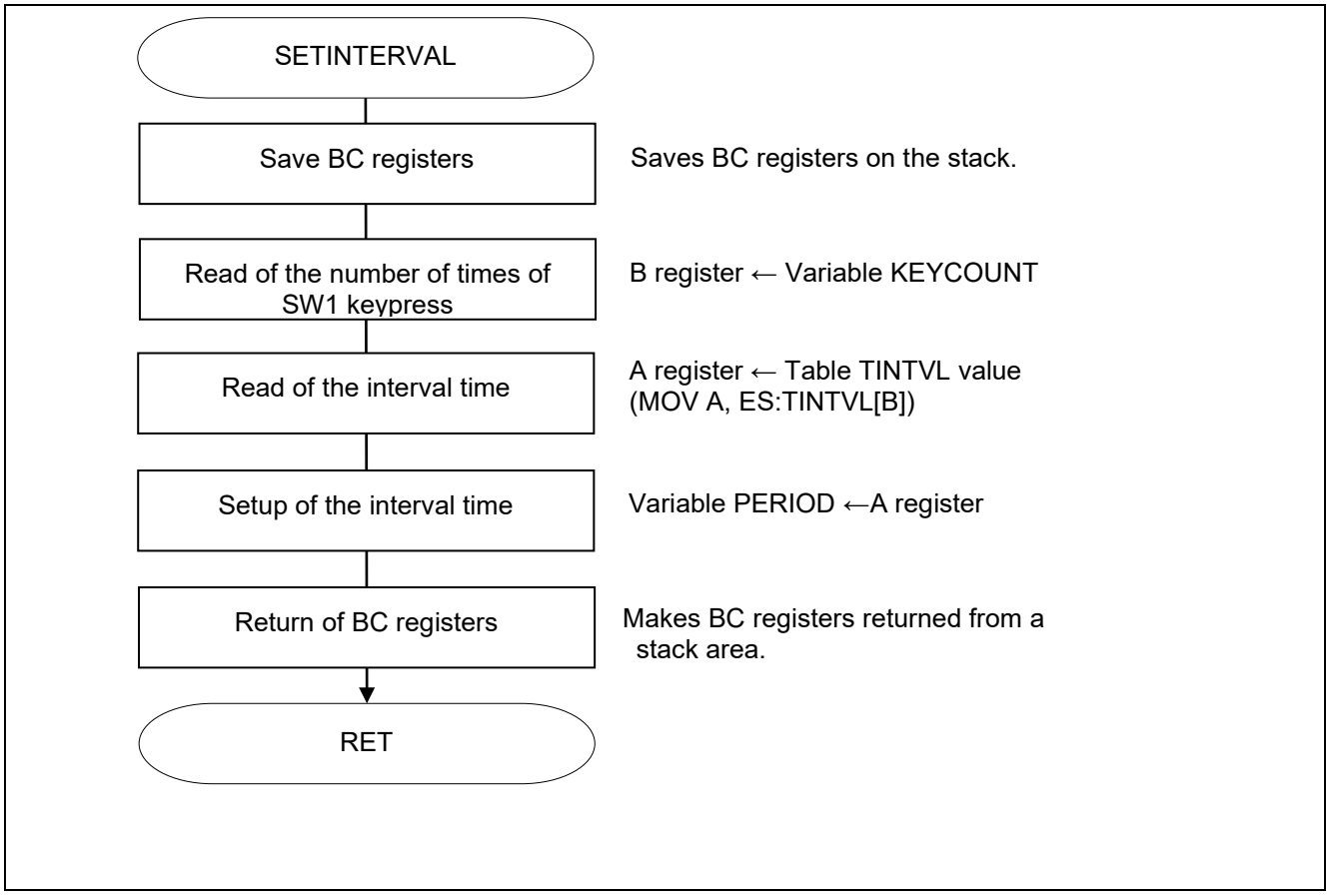

Figure 5.8 Interval Setup

5.7.8 INTWDTI Generation Period Measurement (BC register, WDT counter clear)

Figure 5.9 shows the flow chart for the INTWDTI generation period measurement (BC register, WDT counter clear).

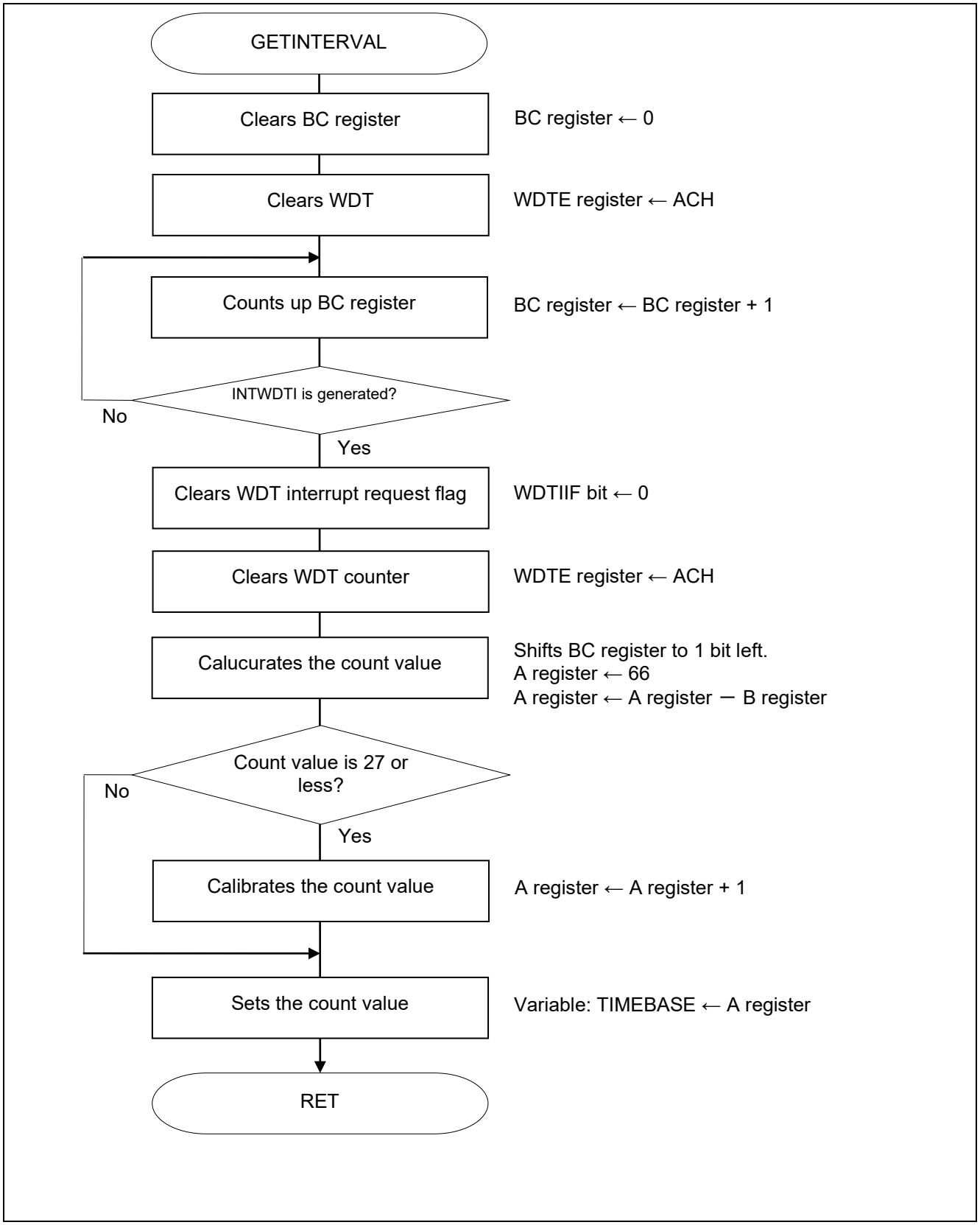

Figure 5.9 Time Measurement to INTWDTI Generating (BC register, WDT clear)

5.7.9 INTWDTI Generation Period Measurement

Figure 5.10 shows the flow chart for the INTWDTI generation period measurement.

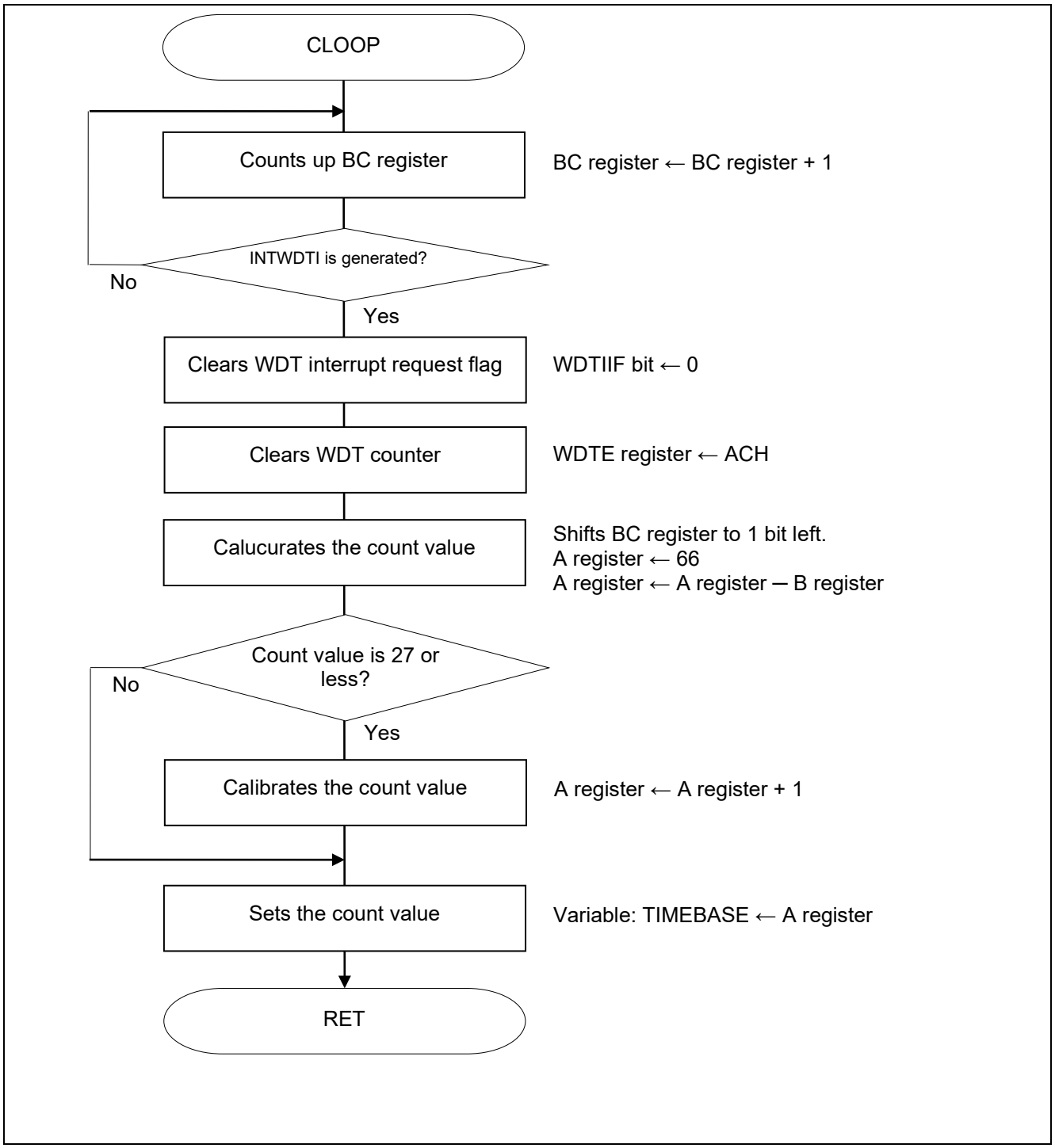

Figure 5.10 Time Measurement to INTWDTI Generating

5.7.10 INTP0 Interrupt Processing

Figure 5.11 shows the flowchart for the INTP0 interrupt processing.

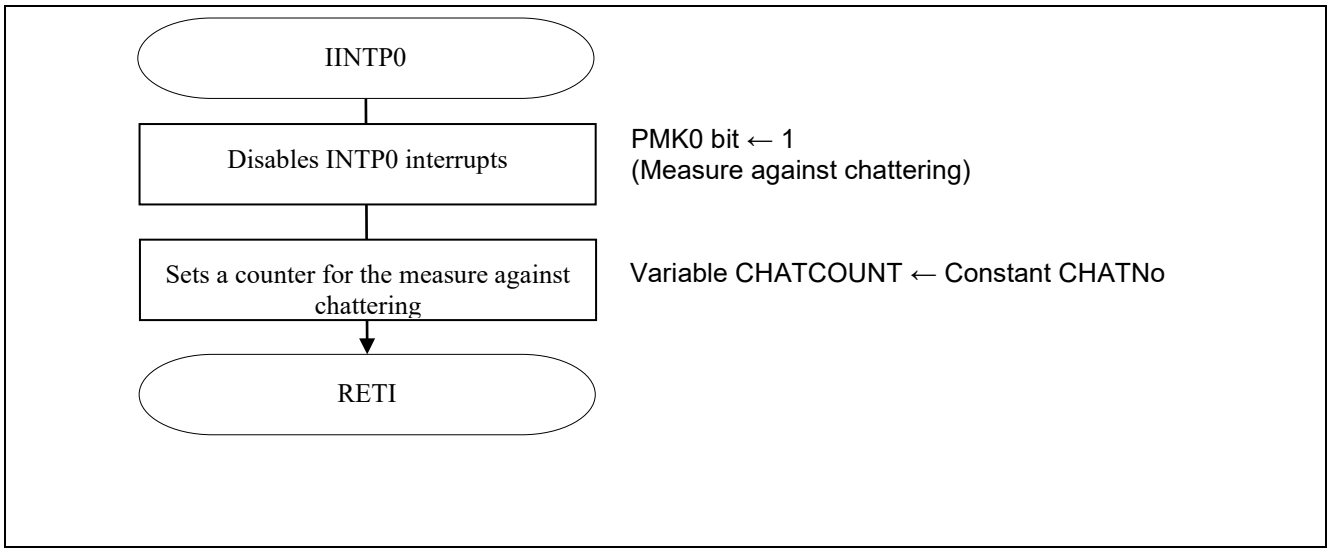

Figure 5.11 INTP0 Interrupt Processing

5.7.11 INTWDTI Interrupt Processing

Figure 5.12 shows the INTWDTI interrupt processing (1/3), Figure 5.13 shows the INTWDTI interrupt processing (2/3), and Figure 5.14 show the INTWDTI interrupt processing (3/3).

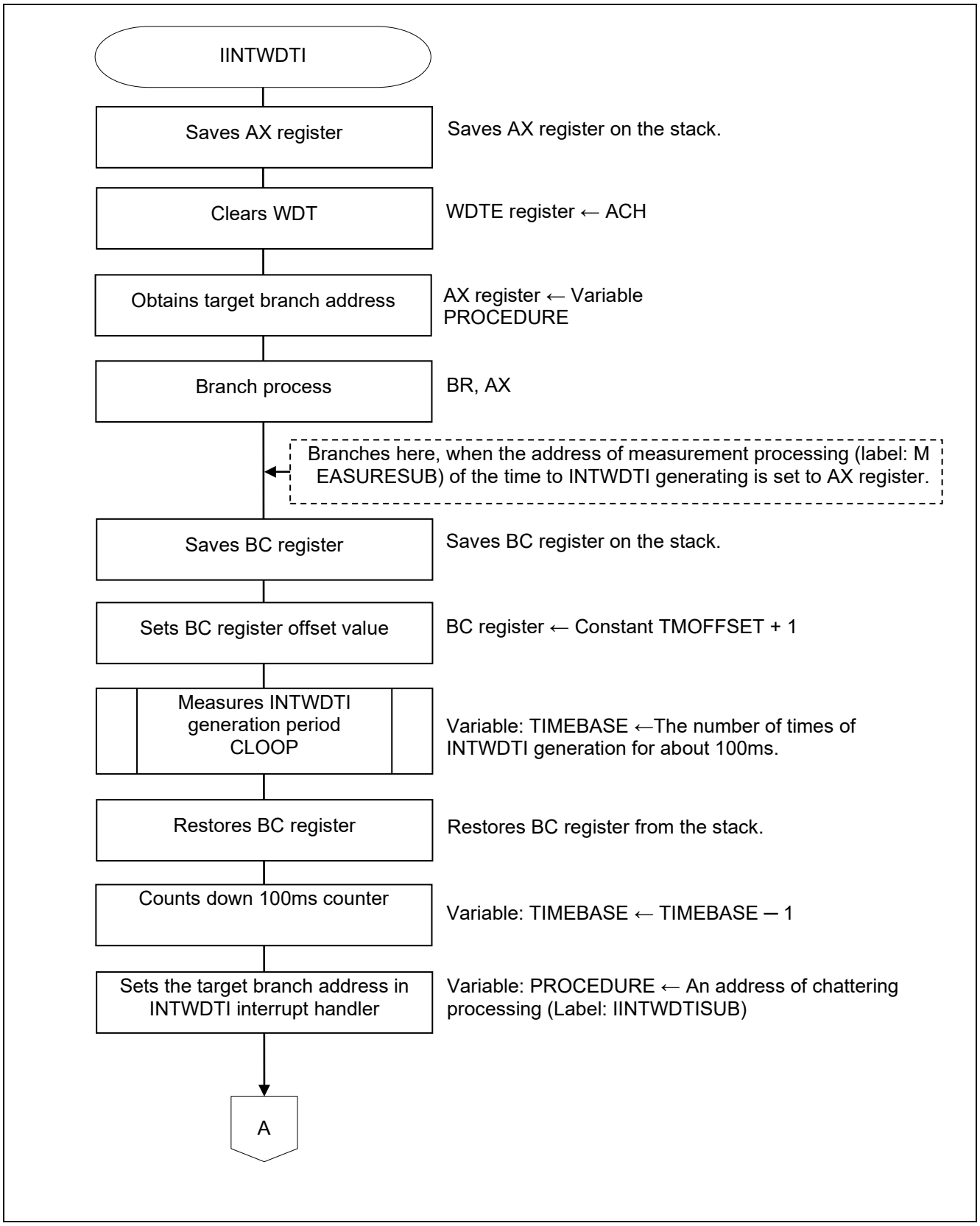

Figure 5.12 INTWDTI Interrupt Processing (1/3)

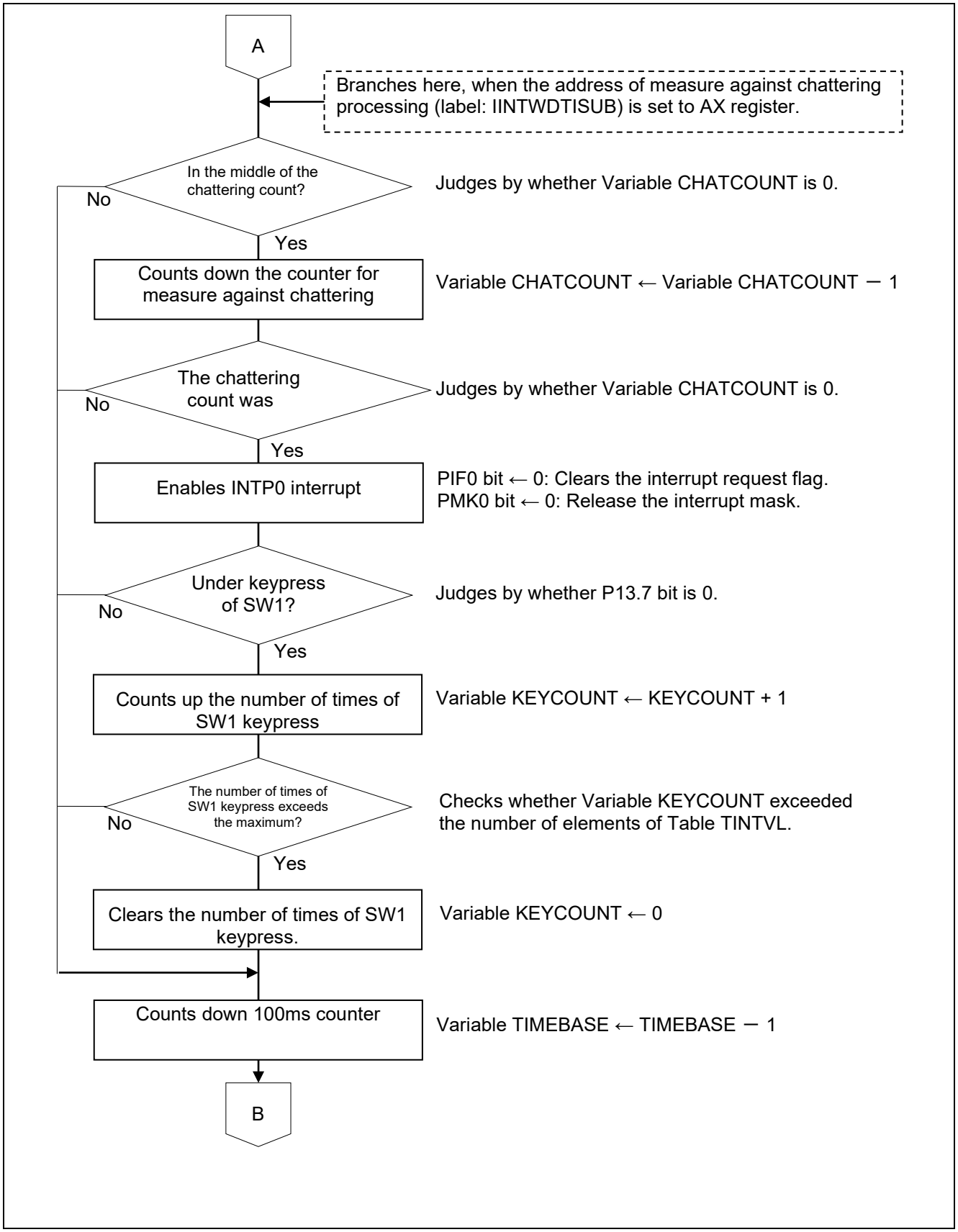

Figure 5.13 INTWDTI Interrupt Processing (2/3)

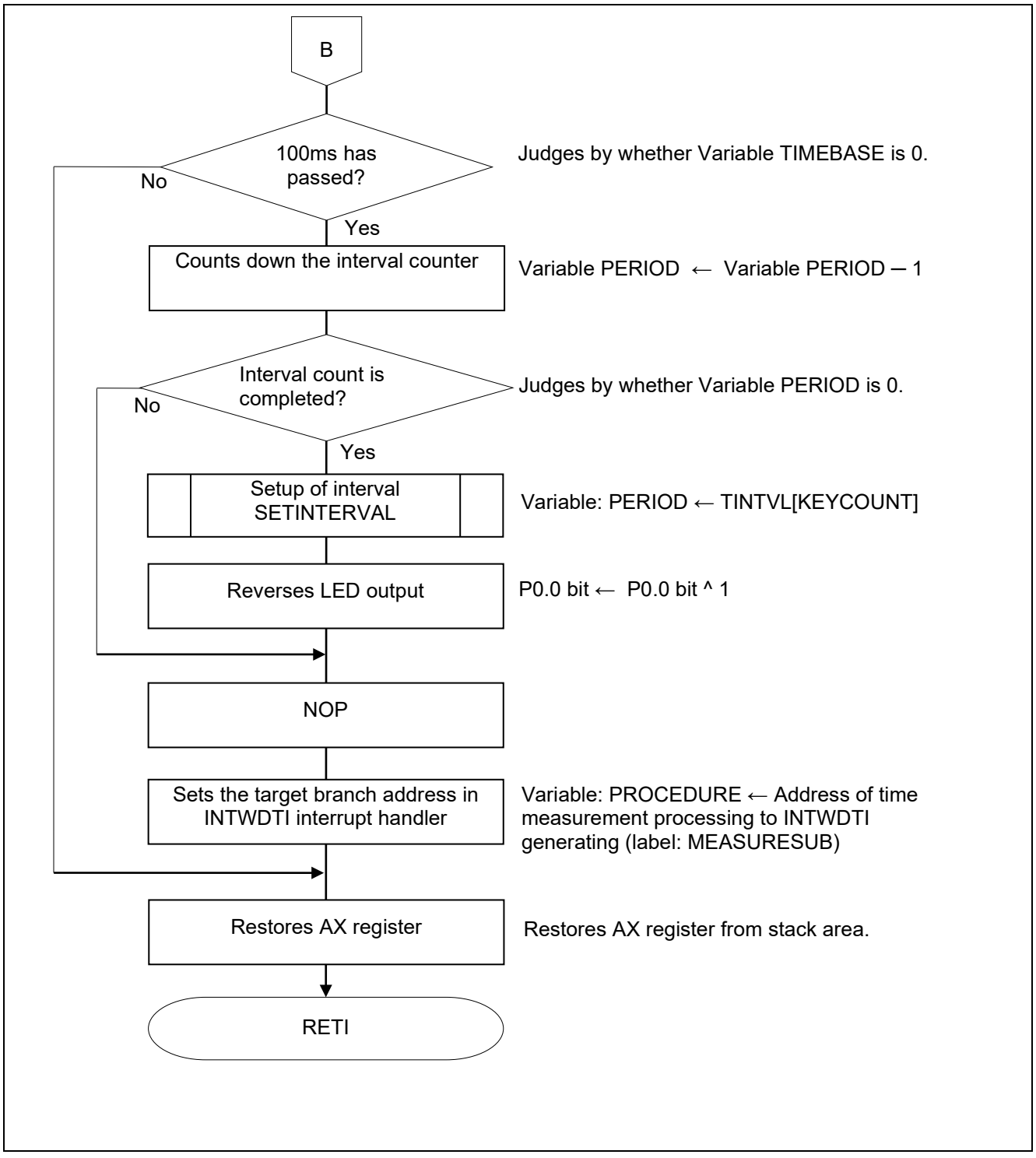

Figure 5.14 INTWDTI Interrupt Processing (3/3)

6. Sample Code

The sample code is available on the Renesas Electronics Website.

7. Documents for Reference

RL78/G10 User's Manual: Hardware (R01UH0384E)
RL78 Family User's Manual: Software (R01US0015E)
(The latest versions of the documents are available on the Renesas Electronics Website.)

Technical Updates/Technical Brochures

(The latest versions of the documents are available on the Renesas Electronics Website.)

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	2014.09.10	-	First Edition
1.10	2022.09.30	8	Delete IAR information from Table 2.1

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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