

RH850/U2C Group

GTM Current feedback for Solenoid Application Note

Summary

This application note summarizes operation examples of current feedback control using the Generic Timer Module (GTM). The current feedback control program is assumed to be located in the user area.

This document and program are intended to help users understand the functions implemented in the RH850/U2C and are not intended for use in mass production design.

In addition, it does not reflect the latest manuals, errata, technical updates, or updates to the development environment. When using the relevant functions, treat this program as a reference only and use the latest documentation and development environment at your own risk.

Applicable device

This document applies to RH850/U2Cx.

【Note】 When downloading to the Configuration Setting Area, set the desired option bytes in "set_csa.c", enable downloading, and then rewrite the option bytes.

For details, refer to the RH850/U2C Series Startup Application Note.

- (1) Select "***** (Debug Tool)" from the project tree.
- (2) Select the "Download file settings" tab.
- (3) "Allow downloads to the Configuration Setting Area" = set to "Yes"

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1. Introduction

This application note provides information on how to use the current feedback control using Generic Timer Module (GTM) on the RH850/U2Cx and examples of software development.

1.1 Functions Used

The hardware functions of RH850/U2Cx used in this application note are shown below.

- Generic Timer Module (GTM)
- ADCK

2. Current Feedback Control Overview

2.1 Operation Overview

In this operation example, current feedback control of a solenoid is performed using the Generic Timer Module (GTM). The solenoid current is converted into a digital value by the AD converter (ADCK), and upper/lower limit judgments are made.

The GTM determines the current value based on the AD conversion result and outputs a pulse from the GTMT000 pin through ATOM.

Figure 2-1 shows an example of current feedback control in this operation example.

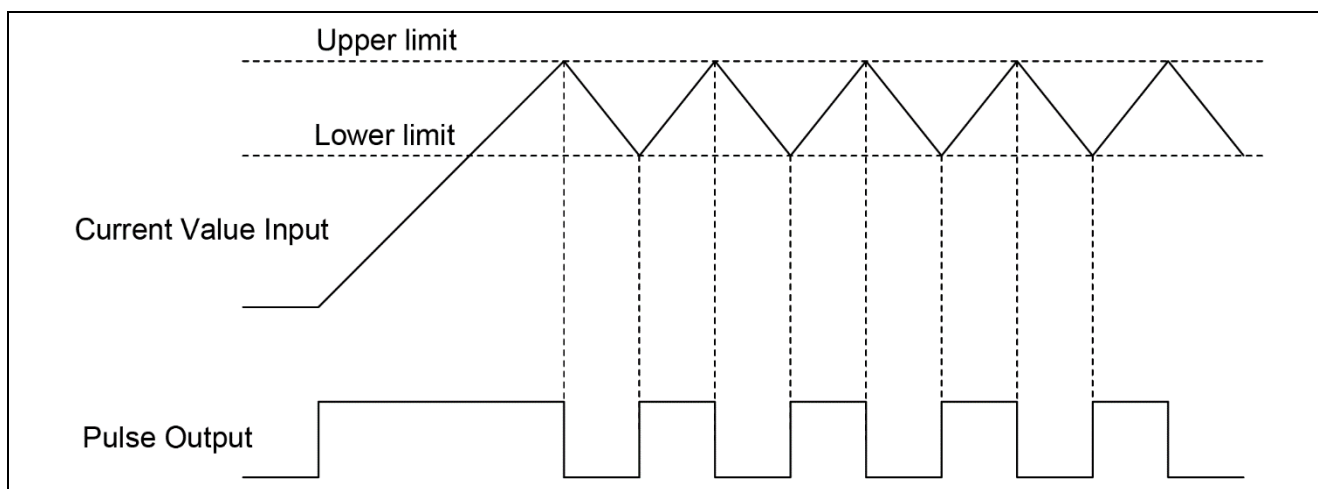


Figure 2-1 Example of Current Feedback Control

2.2 System Configuration Diagram

Figure 2-2 shows the system configuration for this operation example.

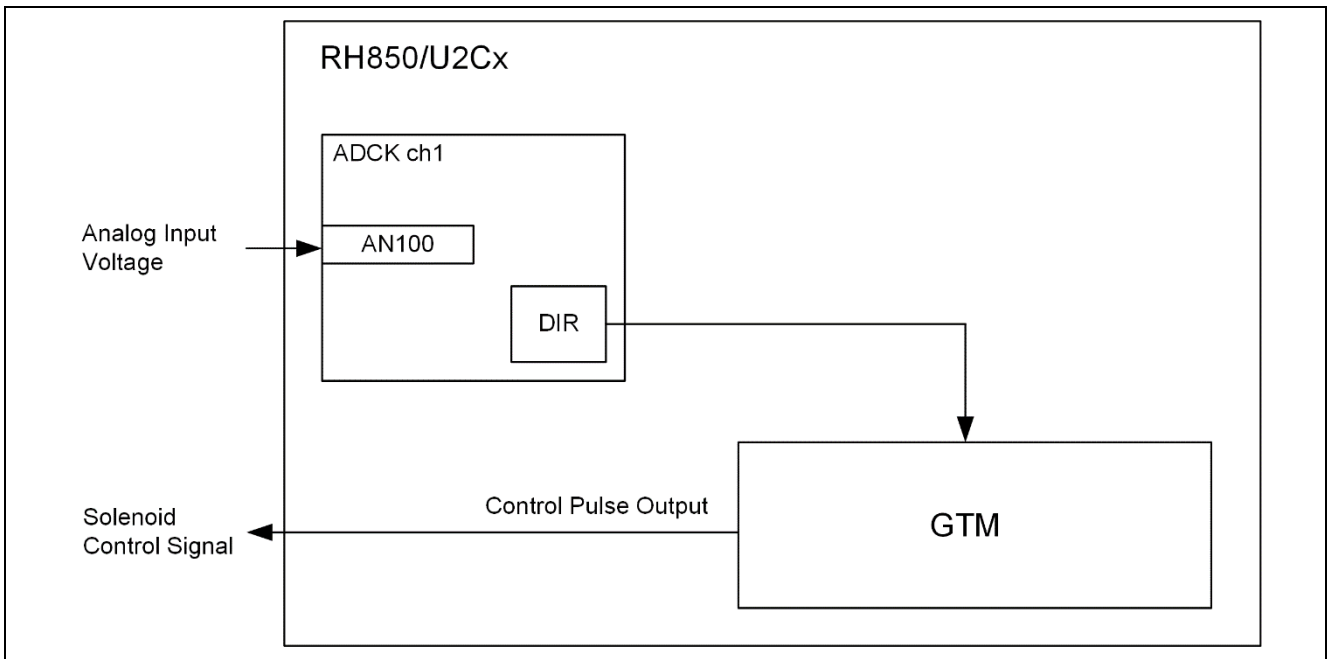


Figure 2-2 System Configuration

2.3 Pin Functions

Table 2-1 shows the pin functions used in this operation example.

Table 2-1 Pin Function List

Pin	Function
AP2_0 (AN100)	Analog Input Pin
ATOM0_0 (P10_1)	Pulse Output

2.4 Peripheral Functions

Table 2-2 shows the list of peripheral functions used in this operation example.

Table 2-2 Peripheral Functions List

Peripheral Functions	Usage
GTM Multi Channel Sequencer (MCS)	<ul style="list-style-type: none"> Upper/lower limits determination of current value, pulse output
GTM ARU-connected Timer Output Module (ATOM)	<ul style="list-style-type: none"> Pulse output
A/D converter (ADCK)	<ul style="list-style-type: none"> Digital conversion of current value

2.4.1 GTM Multi Channel Sequencer (MCS)

Retrieves the level of boundary flags detected by TIM using the ARU and AEI buses, and determines the upper and lower limits of the current value. Based on the upper/lower limit judgment, the output pulse from ATOM is controlled according to the level.

2.4.2 GTM ARU-connected Timer output Module (ATOM)

Outputs pulses.

- Configured in SOMI mode with High/Low level output.

2.4.3 A/D Converter (ADCK)

Converts the current value into a digital value.

- ADCK (AN100) performs A/D conversion of the analog input voltage using reference voltage A1VREFH.
- AD timer period: 5 μ s (200 ksps)
- Input voltage range: 0 to A1VCC (A1VCC: analog power supply voltage 0 to +5 V)
- Input voltage range: set as follows in this operation example.

- AnVCC = A1VCC = 5V

- A1VREFH = 5V

- A1VSS = 0V

- Analog input (AN100): 0 to 5 V

For details of each pin, refer to “RH850/U2C User’s Manual Section 57 Electrical Characteristics”.

3. Operation Example

The MCS accesses the AD conversion data register to obtain data. In addition, the MCS sets the output level to ATOM via the ARU in order to output control pulses from ATOM. Details of this operation example are described below.

3.1 AD Data Register Access

3.1.1 Overview

Figure 3-1 shows a schematic diagram of this operation example. The MCS reads the data register of ADCK via the AEI bus. By comparing the read data with the threshold value, the MCS sets the High/Low output to ATOM via the ARU, and a pulse is output.

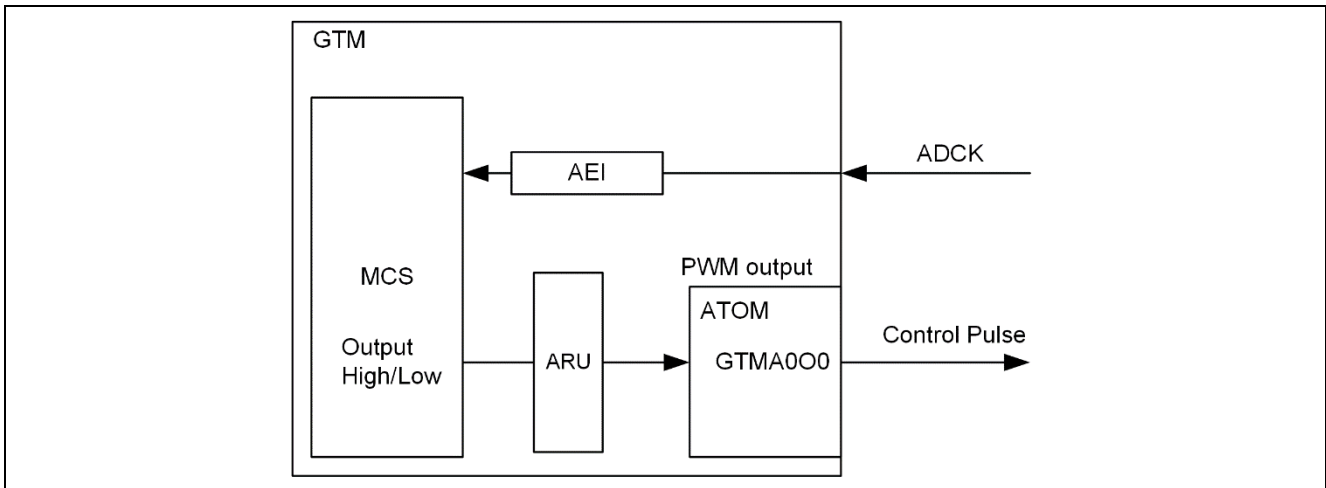


Figure 3-1 Schematic Diagram

3.1.2 Acquisition of Edge Detection Result with MCS

An overview of AEI access is shown below. (For details of each instruction, refer to the GTM specification.)

Note: The AEI access requires the MCS version to be set to V3 or later.

(1) Read of external GTM register (ADCK)

The data register value of ADCK can be read using the Bus Read (BRD) instruction.

3.1.3 Pulse Output with MCS

Figure 3-2 shows a schematic diagram of this operation example. ATOM is used in SOMI mode (Signal Output Mode Immediate). The MCS controls the High/Low output using the ACB (ARU Control Bit Register).

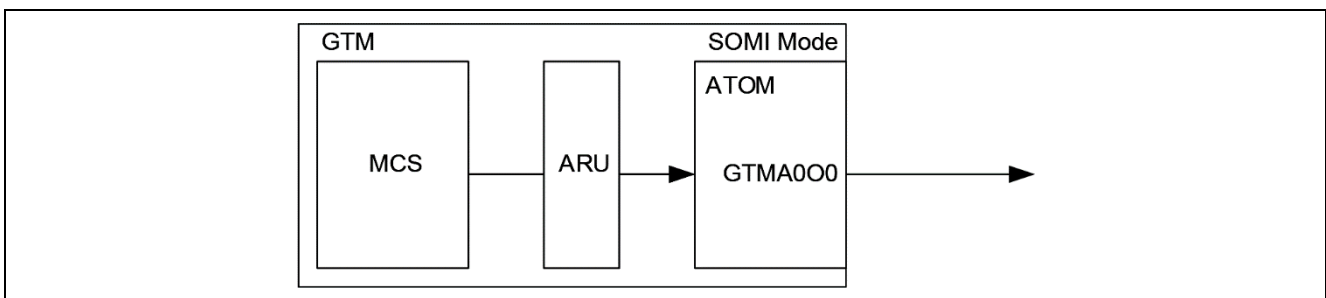


Figure 3-2 Schematic Diagram

Figure 3-3 shows an overview of ACB (ARU Control Bit Register).

When ATOM is used in SOMI mode (Signal Output Mode Immediate), the setting value of ACB (ARU Control Bit Register) is transferred to the ACB bit in the ATOM control register when the ARU write instruction is executed.

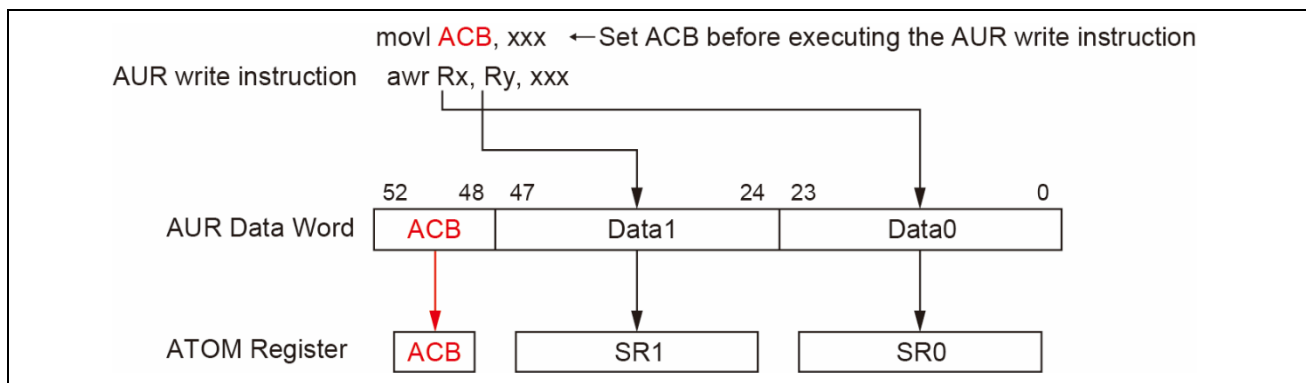


Figure 3-3 ACB (ARU Control Bit Register)

3.1.4 Operating Conditions of Used Functions

The operating conditions for the functions used in this operation example are shown below.

Table 3-1 Port Setting

Item	Description
Used Pin (Output)	P10_1 : GTMAT000

Table 3-2 ATOM0 Configuration

Item	Description
ATOM0 operating clock	100MHz
Channel used	ATOM0 ch0
Operating mode	Signal Output Mode Immediate (SOMI)
Signal level	High/Low level output
ARU Input stream	Enabled
ARU read address	ATOM0 ch0 : 0x04F (MCS0_WRADDR0)

Table 3-3 MCS0 Configuration

Item	Description
MCS0 operating clock	100MHz
Channel used	MCS0 ch0
Scheduling mode	Accelerated Scheduling

Table 3-4 ADCK1 Configuration

Item	Description
ADCK1 operating clock	40MHz
Channel used	ADCK ch1
Operating mode	Multi-Cycle Scan
Used Pin	AP2_0 : AN100
Format	Signed 12-bit fixed-point

3.1.5 Software Description

Setting examples for each register used in this operation example are shown below.

Table 3-5 GTM Configuration Example

Register	Setting Value	Function
GTM-IP Global control register (GTM_CTRL)	0x0000 0000	RF_PROT 1: SW RST function enabled (GTM_RST register protection released)
GTM-IP Global reset register (GTM_RST)	0x00000001	GTM IP reset : Enabled Bridge Mode : Enabled
GTM-ADCI register (GTM_ADCI_CHSEL0)	0x0000	Select ADDATA0

Table 3-6 MCS Register Configuration Example

Register	Setting Value	Function
MCS Control and Status register (MCS0_CTRL_STAT)	0x0000 0000	SCD_MODE 0x0 : Accelerated Scheduling
MCS Channel control register (MCS0_CH0_CTRL)	0x0000 0001	EN 1 : MCS0_ch0 enabled

Table 3-7 ATOM Register Configuration Example

Register	Setting Value	Function
ATOM Channel 0 control register (ATOM0_CH0_CTRL)	0x0000 0808	CH0 operation settings MODE[1:0] 0x0 : Signal output mode Immediate (SOMI) ARU_EN 1 : ARU input stream enabled SL 1 : High level output
ATOM Channel 0 ARU read address register (ATOM0_CH0_RDADDR)	0x01FE 004F	ARU read address setting RDADDR0 0x04F : MCS0_WRADDR0
AGC Output enable status register (ATOM0_AGC_OUTEN_STAT)	0x0000 0002	ATOM0 output control OUTEN_STAT0 0x02 : CH0 output enabled
AGC Enable/disable status register (ATOM0_AGC_ENDIS_STAT)	0x0000 0002	ATOM0 operation setting ENDIS_STAT0 0x02 : CH0 enabled

Table 3-8 CMU Register Setting Example

Register	Setting Value	Function
Clock Enable (CMU_CLK_EN)	0x0000 0002	Clock Setting EN_CLK0 0x2 : CMU_CLK0 enabled

Table 3-9 ADCK Register Configurations

Register	Setting Value	Function
ADCK1VCR00	0x00100000	Conversion type: normal A/D conversion
		Wait time table: not selected
		Entry to GTM: enabled
		Virtual channel end interrupt: disabled
		Physical Ch1/Sub Ch0 (AN100)
ADCK1ADCR2	0x00	Signed 12-bit fixed-point format
ADCK1SGCR3	0x42	ADTSTART: enabled
		Multi-cycle scan mode
		AD timer trigger 3 selected for SG3 trigger
ADCK1SGVCPR3	0x0000	Start virtual channel 0, end virtual channel 0
ADCK1SGMCRYCR3	0x00	Number of scans in multi-cycle scan mode: 1
ADCK1ADTIPR3	1	AD timer initial phase: 25 ns
ADCK1ADTPRR3	200	AD timer cycle phase: 5 μ s
ADCK1GTMENSGER	0x0800	Entry scan group: SG0 enabled

Table 3-10 Port Register Setting Example

Register	Setting Value	Function
Port Control Register (PCR10_1)	0x0000 004A	Port Setting P10_1 Multiplexed Mode 11 : GTMAT000

Table 3-10 lists the functions used in this operation example.

Table 3-11 List of Functions

Function Name	Description
main_pm0	Calls each function.
cmu_init	Initializes the clock.
gtm_init	Resets the GTM.
mcs0_init	Initializes MCS0.
atom0_init	Initializes ATOM0.
port_init	Initializes the ports.
adck1_init	Initializes ADCK1.

3.1.6 Operation Flow

Figure 3-4 shows the operation flow for this operation example.

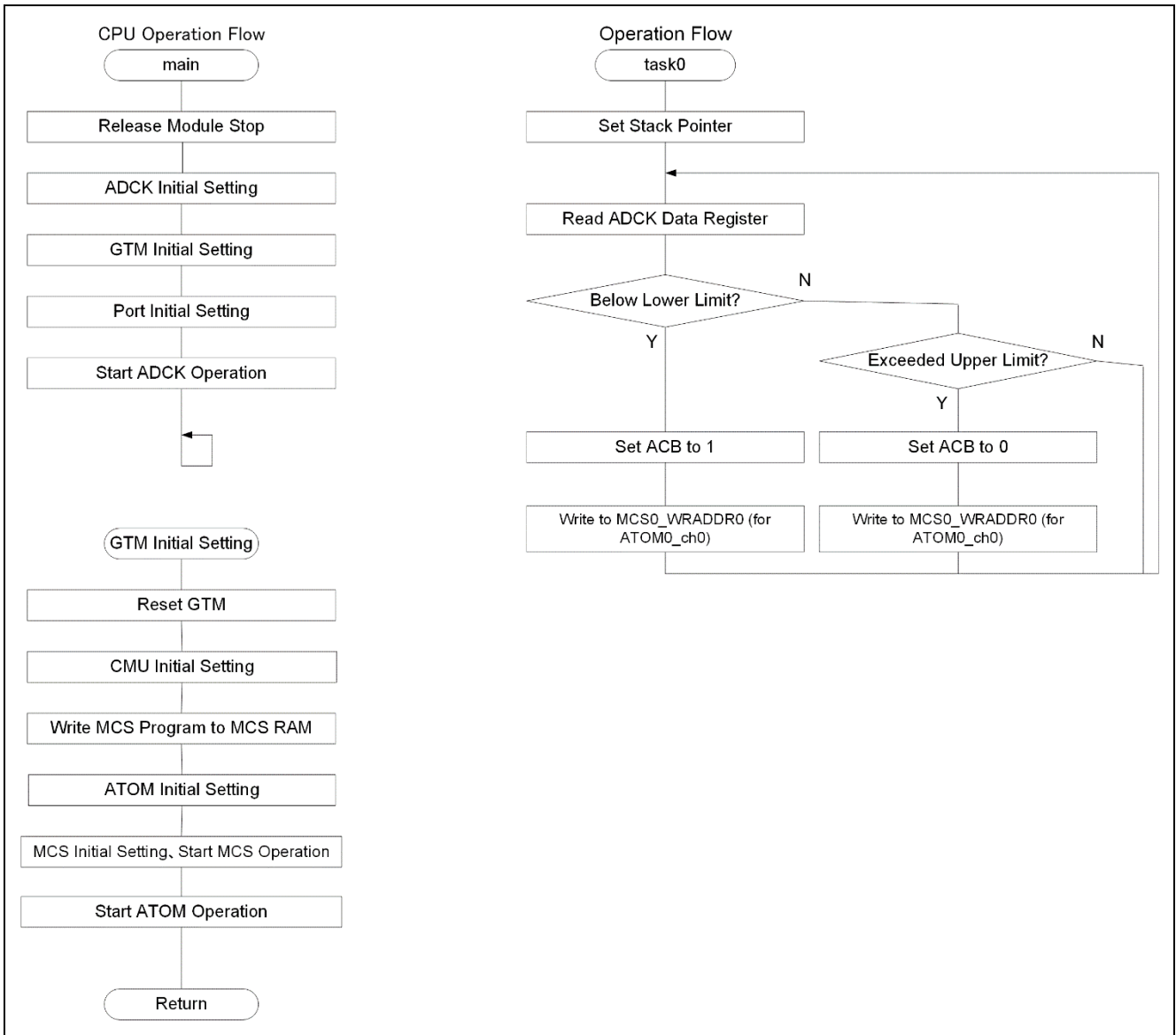


Figure 3-4 Operation Flow

4. Revision Record

Rev.	Issue date	Revised contents	
		Page	Points
1.00	Dec. 24, 2025	-	First edition

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

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