RH850/U2Bx-E Group, U2C Group

Ethernet TSN(RSWITCH) GigaBit Ethernet Application Note

Summary

This application note summarizes the operation examples of GigaBit Ethernet using Ethernet TSN (RSWITCH) of RH850/U2Bx-E. Ethernet TSN(RSWITCH) program is assumed to be in the user area. For an example of the operation of GigaBit Ethernet on the RH850/U2C, please refer to the SGMII section.

This document and program are intended to facilitate understanding of the functions equipped in the RH850/U2Bx-E and are not intended for mass production design.

In addition, it does not reflect the latest manuals, errata, technical updates, or updates to the development environment. When using the relevant functions, please treat this program as a reference and ensure that you proceed at the user's own responsibility with the latest documentation and development environment.

Apply

This document applies to RH850/U2Bx-E, U2C.

When downloading to the Configuration Setting Area, set arbitrary option byte in "set_csa.c", allow downloading and rewrite the option byte. For details, refer to the RH850/U2C Series Startup Application Note.

(1) Select "***** (Debugging Tool)" from the project tree.

(2) Select the “Download File Settings” tab.

(3) Set “Allow downloads to Configuration Setting Area” = “Yes”

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1. Introduction

This application note describes how to use the Ethernet TSN (RSWITCH) of the RH850/U2Bx-E and includes software creation examples.

1.1 Functions to use

The following shows the hardware functions of RH850/U2Cx used in this application note.

- TSNSWA
- Port（P21/P33）

1.2 System configuration

Figure 1-1 shows the connection diagram with PHY.

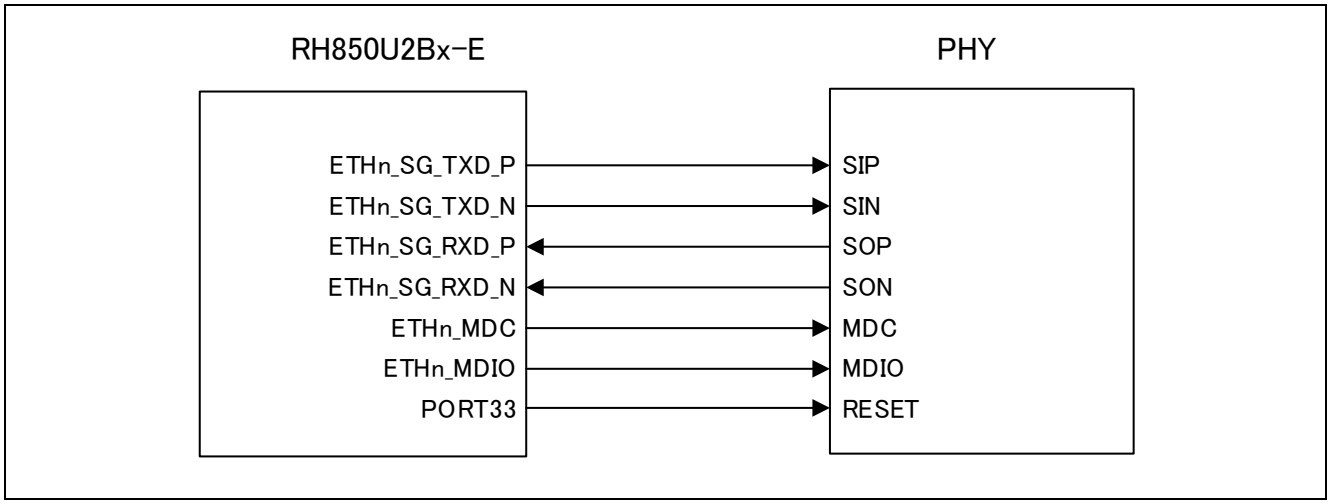

Figure 1-1 Connection diagram of RH850/U2Bx-E and PHY

1.3 Overview of TSNSWA

1.3.1 GigaBit Ethernet Communication

Figure 1-2 shows the block diagram of the TSNSWA module. GigaBit Ethernet communication uses TSNSWA's MFAB, MFWD, ETHA0,1 (TSNA), GWCA, COMA, and GMII2SGMII converters.

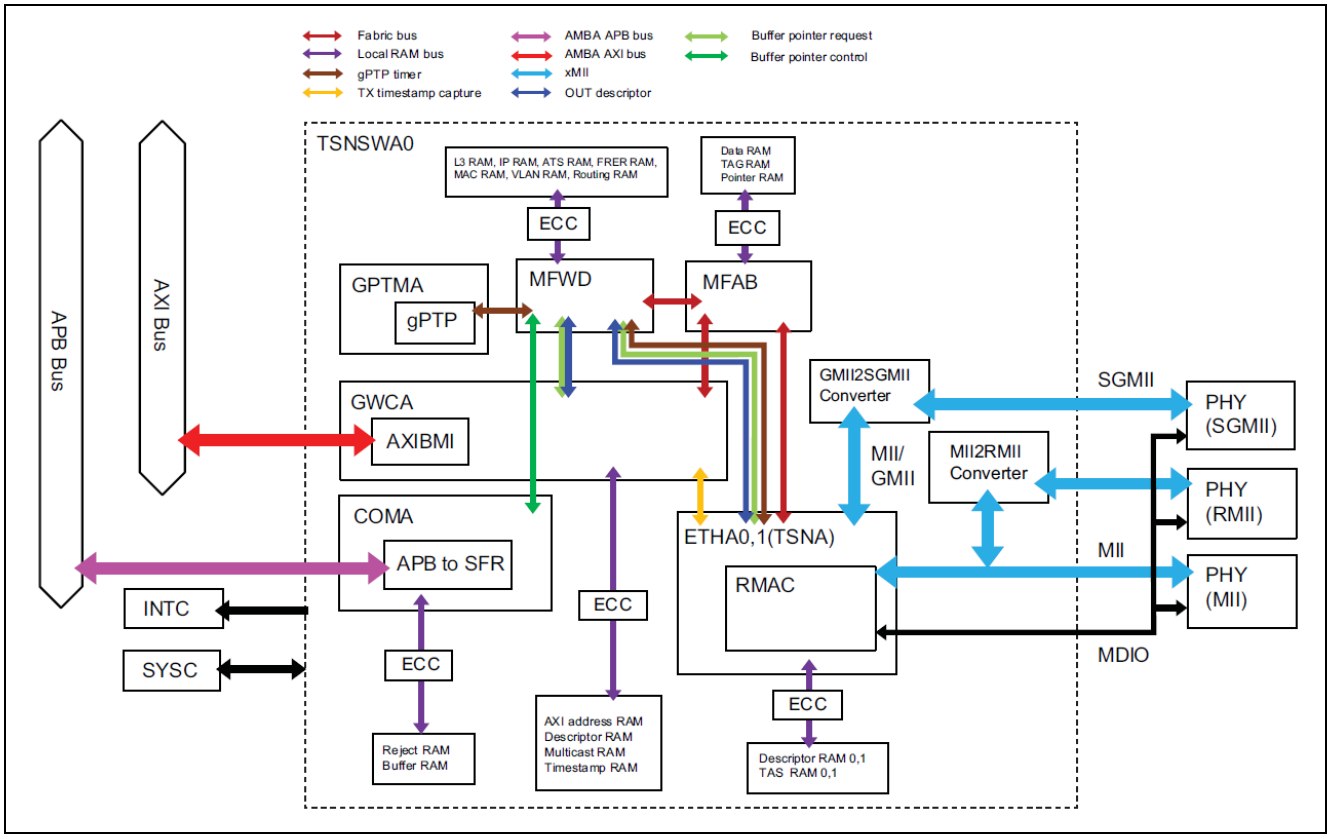

Figure 1-2 Block diagram of the TSNSWA module

1.3.2 Ethernet Frame Format

Supports Ethernet II and IEEE 802.3 frame formats.

1.3.3 Frame Formats for Data Transmission and Reception

figure 1-3 shows the Ethernet II/IEEE802.3 frame format.

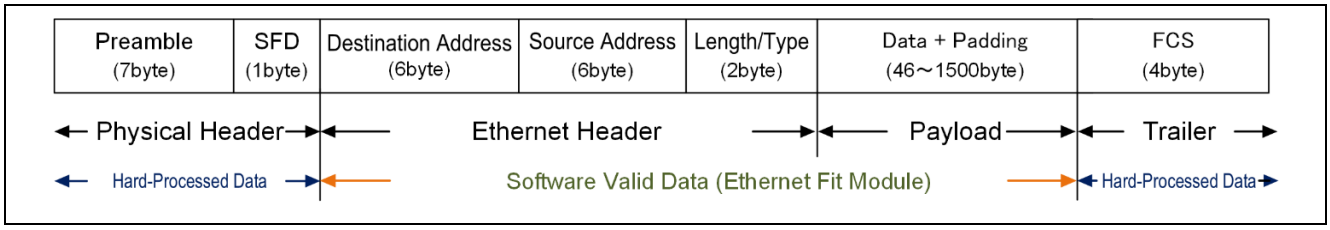

Figure 1-3 Ethernet II/IEEE802.3 frame format.

- The preamble and SFD are signals to indicate the beginning of the Ethernet frame. Additionally, the FCS stores the CRC value of the Ethernet frame calculated on the transmitting side, and the hardware calculates the CRC value in the same way when receiving data, and if the CRC value does not match, the Ethernet frame is discarded.
- If the hardware determines that the data is normal, the valid range of the received data will be as follows: (destination address) + (source address) + (length/type) + (data).

1.3.4 Frame Format of PAUSE Frame

Figure 1-4 shows the frame format of the PAUSE frame.

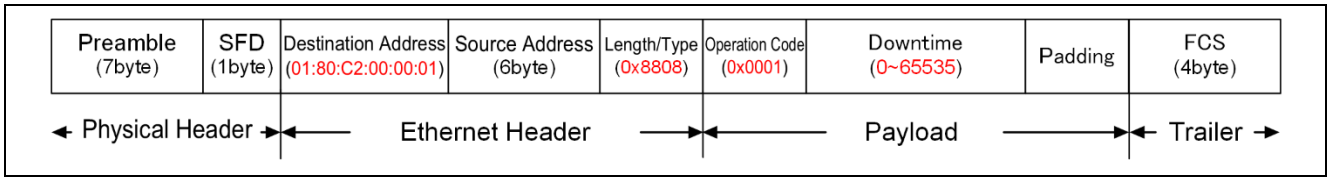

Figure 1-4 Frame format of the PAUSE frame.

- The destination address is specified as "01:80:C2:00:00:01", which is a multicast address reserved for PAUSE frames. Additionally, "0x8808" is specified for the length/type, and "0x0001" is specified as the operation code at the beginning of the payload.
-

1.3.5 Frame Format of Magic Packet

Figure 1-5 shows the frame format of the Magic Packet.

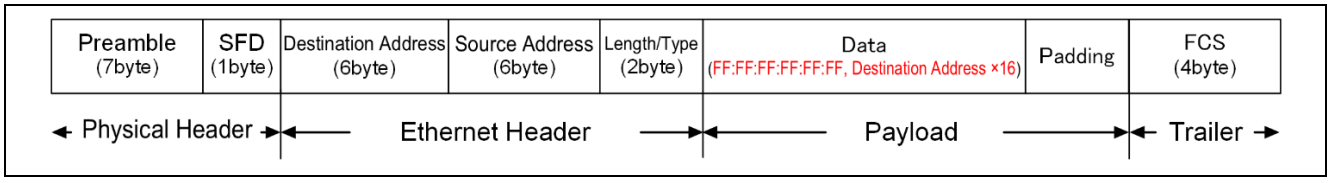

Figure 1-5 Frame format of a Magic Packet.

The magic packet inserts "FF:FF:FF:FF:FF:FF" followed by "the destination address repeated 16 times" somewhere in the Ethernet frame data.

1.3.6 Overview of TSNSWA0

In data transmission, the GWCA and MFAB fetch and write the frame data placed in the user RAM, and output it to the PHY via ETHA0,1. Additionally, when receiving data, the frame data input from the PHY is received by SGMII and transferred to the user RAM via ETH0,1. Figure 1-6 shows the transmit and receive data processing.

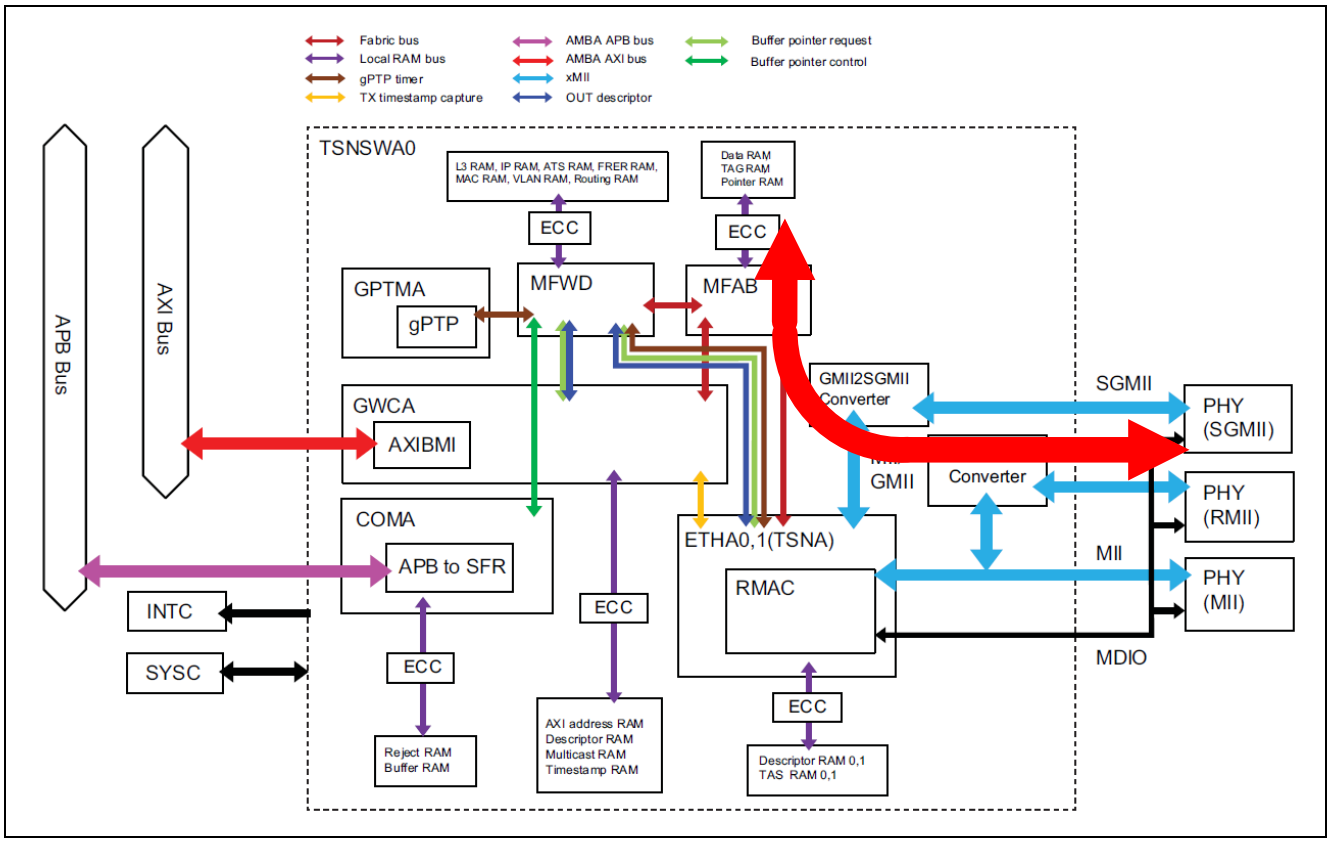

Figure 1-6 Transmit and receive data processing

1.3.7 Overview of RMAC

Figure 1-7 shows a block diagram of the RMAC module. The RMAC's PHY MDIO interface function is used to perform PHY management (reset, write/read on-chip registers) and link-up confirmation.

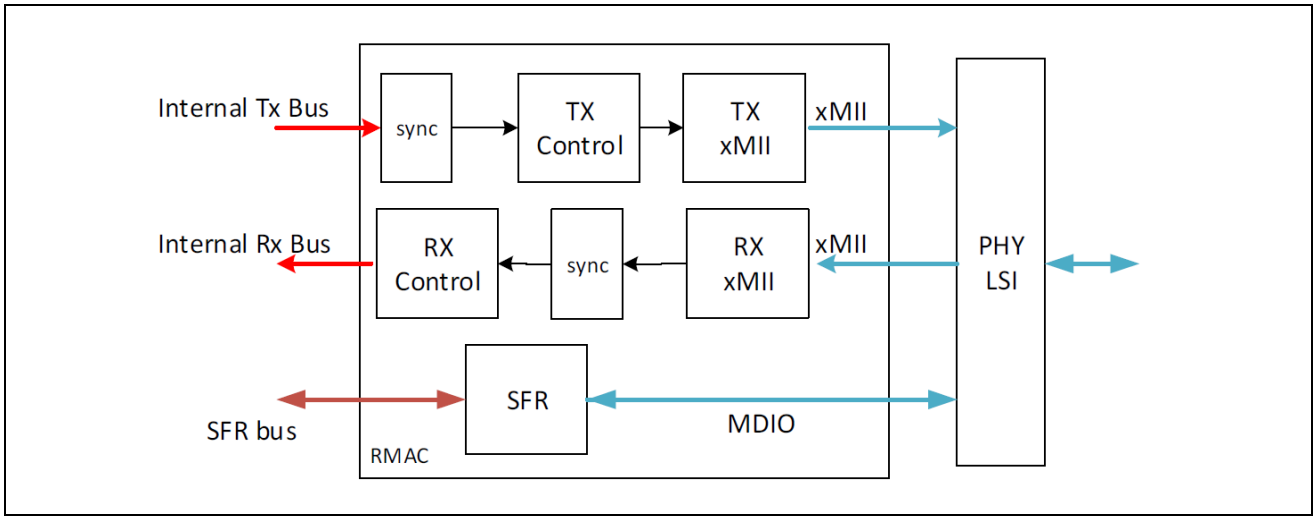

Figure 1-7 Block diagram of the RMAC

1.3.8 PHY Management and Link up

This section explains PHY configuration using the PHY MDIO interface function.

The PHY specifications for this operation example are as follows.

The setting values of the PHY registers are shown in Table 1-1.

- PHY interface：SGMII
- Communication format：Full duplex
- Transmission speed：1000Mbase
- Management Data Clock：clk/54(2.46MHz)
- Management Frame Format：IEEE802.3 の Clause 45
- PHY address：00000b

Table 1-1 PHY register

Device Address	Register Address	Setting Values	Function
0x0004	0x8000	0x8000（At reset）	PHY reset
		0x1340 (During communication）	Enabled Auto negotiation, 1000Mbps, Full duplex, Restart Auto negotiation.
0x0007	0x0200	0x1200	Auto negotiation, Restart Auto negotiation.

1.4 Example of a 64byte Transmit and Receive Operation (Loopback mode)

This operation example describes the method of transmitting and receiving a 64-byte standard frame four times consecutively in loopback mode.

1.4.1 Communication Specifications

Channel to be used：TSNSWA0

Frame：Normal Frame

Number of data: 64byte

Transmit and Receive FIFO: 64byte

Number of descriptors: 4

1.4.2 System Configuration

Figure 1-8 shows the system configuration.

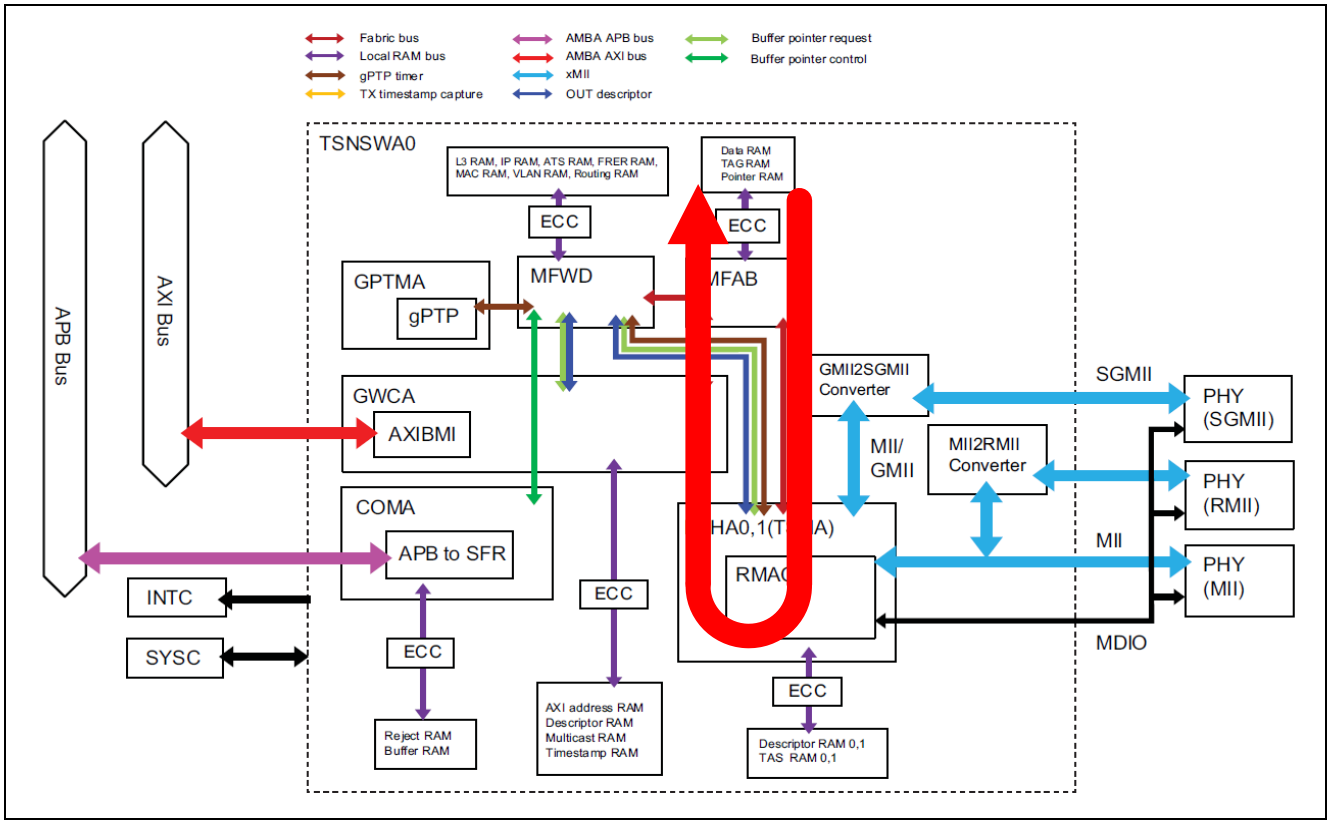

Figure 1-8 System configuration.

1.4.3 Descriptor Description

Transfer information set in the descriptor is used to transfer data between the storage destination for transmitted and received data (built-in RAM) and the FIFO in TSNES. In this operation example, the descriptor format is an extended descriptor (16 bytes) without a timestamp. Table 1-2 shows the descriptor settings.

Table 1-2 Descriptor Settings

Classification	Number	Type	Descriptor Address	Data Storage Destination Address	Size
Receive	1	FEMPTY	0xFDC01000	0xFE001000	64byte
	2	FEMPTY	0xFDC01010	0xFE001040	64byte
	3	FEMPTY	0xFDC01020	0xFE001080	64byte
	4	FEMPTY	0xFDC01030	0xFE0010C0	64byte
	5	EEMPTY	0xFDC01040	-	64byte
Transmission	1	FSINGLE	0xFDC01060	0xFE001200	64byte
	2	FSINGLE	0xFDC01070	0xFE001240	64byte
	3	FSINGLE	0xFDC01080	0xFE001280	64byte
	4	FSINGLE	0xFDC01090	0xFE0012C0	64byte
	5	EEMPTY	0xFDC01100	-	-

1.4.4 MAC Address Filter

In data reception, MAC address filtering is performed. In this operational example, unicast reception is enabled.

1.4.5 Software Description

- Module Description

The module list for this operation example is shown below.

Table 1-3 Module list

Module Name	Label Name	Function
Main routine	main_pm0	Configure various settings and start applications.
Port initialization Routines	port_init	Configure the initial settings for the port.
Start Ethernet Communication	eth_open	Performs processing to start Ether communication.
End Ethernet Communication	eth_close	Performs processing to end Ether communication.
COMA initial settings	coma	Perform COMA initial settings.
MFWD initial settings	mFwd	Perform MFWD initial settings.
GWCA initial settings	gwca	Perform GWCA initial settings.
RMAC initial settings	rmac	Perform RMAC initial settings.
SGMII initial settings	sgmii	SGMII、PWRCTL initial settings.
Descriptor initialization	init_ethram	Initializes Descriptor.
Data Transmission	eth_write	Set the transmission data and perform the processing to start transmission.
Receiving data	eth_read	Read the received data and perform the storage process.
Transmission Data Settings	write_ethram	Set transmission data in local RAM.
Reception Data Settings	read_ethram	Set received data in local RAM.
PHY initialization	phy_init	Reset the PHY.
Auto Negotiation	phy_start_autonegotiate	Set the communication format, transfer speed, enable auto negotiation, and execute the process.
PHY register read.	phy_read	Specify the PHY register address and read the internal register.
PHY register write	phy_write	Specify the PHY register address and write to the internal register.

- Register Setting

The register settings for each function in this operation example are shown below.

Table 1-4 TSNA Register setting

Register Name	Setting Values	Function
TARO0EAMC	0x00000001	Operation Mode Control: Disable Mode
	0x00000002	Operation Mode Control: Configuration Mode
	0x00000003	Operation Mode Control: Operation Mode
TARO0EAIRC	0x00000000	IPV Remapping: 0
TARO0EATDQDC0	0x00000040	Number of Descriptor Queues: 64
TARO0EAVCC	0x00000000	VLAN Mode: No VLAN.

Table 1-5 COMA Register setting

Register Name	Setting Values	Function
CARORRC	0x00000001	Reset Software
CARORCEC	0x0001000F	Clock Permission: Enabled
CAROCABPIRM	0x00000001	Initialization: Common Agent Pool Buffer Initialization

Table 1-6 MFWD Register setting

Register Name	Setting Values	Function
FWROFWGC	0x00000000	VLAN Mode: No VLAN.
FWROFWPBFC0	0x00000004	Port Based Forwarding: Port 0
FWROFWPBFC2	0x00000001	Port Based Forwarding: Port 2

Table 1-7 GWCA Register setting

Register Name	Setting Values	Function
GWROGWMC	0x00000001	Operation Mode Control: Disable Mode
	0x00000002	Operation Mode Control: Configuration Mode
	0x00000003	Operation Mode Control: Operation Mode
GWROGWARIRM	0x00000001	AXI RAM Initialization：Enabled
GWROGWIRC	0x00000000	IPV Remapping: 0
GWROGWRDQC	0x00000000	Receive Descriptor Queue Pause: Disabled
		Receive Descriptor Queue Prohibited: Enabled
GWROGWRDQDC0	0x00000040	Number of Descriptor Queues: 64
GWROGWRGC	0x00000001	Received CRC Passed: FCS Passed
GWROGWDCBAC0	0x00000000	AXI Descriptor Address High: 0x00000000
GWROGWDCBAC1	axidpkt	AXI Descriptor Address Low: Address of axidpkt Header
GWROGWMDNC	0x00000404	Timestamp Descriptor Maximum Value: 0
		Transmit Descriptor Maximum Value: 4
		Receive Descriptor Maximum Value: 4
GWROGWDCC0	0x01000100	Base Address Request: Enabled
		Descriptor Type: Receive
		Extended Descriptor: Extended
GWROGWDCC2	0x01000900	Base Address Request: Extended
		Descriptor Type: Transmit
		Extended Descriptor: Extended

Table 1-8 RMAC Register setting

Register Name	Setting Values	Function
RMRO0MRMAC1	MAC_ADDR [1] MAC_ADDR [2]	MAC Address Low: MAC_ADDR [1], MAC_ADDR [2]
RMRO0MRMAC0	MAC_ADDR [0]	MAC Address High: MAC_ADDR [0]
RMRO0MRAFC	0x00010001	p-Frame Unicast: Enabled
		e-Frame Unicast: Enabled
RMRO0MRGC	0x0000000F	Magic Packet Detection: Enabled
		Pause Frame Reception Time: Enabled
		Pause Frame Reception Control: Enabled
		Received CRC Check: Enabled
RMRO0MPIC	0x121A0408	Capture Time Adjustment: 1
		Hold Time Adjustment: 2
		Preamble Suppression: Disabled
		Clock Selection: 0x1A(clk/54=2.46MHz)
		Link Speed: 1000Mbps
		PHY I/F：GMII
RMRO0MLBC	0x00000001	Loopback Mode: Enabled

RMRO00MPSM （During Read）	0xXXXXYY04	PHY Register Data: XXXX (regad)
		Operation Code: YY Bit 6-5 (Address Frame = 0)
		PHY Register Address: YY bit 4-0 (devad)
		PHY Device Address: 0
		Management Frame Format: Clause 45
		Management: Enable
	↓	↓
	0xXXXXYY04	PHY Register Data: XXXX (data)
		Operation Code: YY Bit 6-5 (Read Frames = 3)
		PHY Register Address: YY bit 4-0 (devad)
		PHY Device Address: 0
		Management Frame Format: Clause 45
		Management: Enable
RMRO0MPSM （During Write）	0xXXXXYY04	PHY Register Data: XXXX (regad)
		Operation Code: YY Bit 6-5 (Address Frame = 0)
		PHY Register Address: YY bit 4-0 (devad)
		PHY Device Address: 0
		Management Frame Format: Clause 45
		Management: Enable
	↓	↓
	0xXXXXYY04	PHY Register Data: XXXX (data)
		Operation Code: YY Bit 6-5 (Read Frames = 2) PHY Register Address: YY bit 4-0 (devad)
		PHY Device Address: 0
		Management Frame Format: Clause 45
		Management: Enable

Table 1-9 SGMII Register setting

Register Name	Setting Values	Function
SGMII0ETN0SGSRST	0x00000001	Reset Software: Reset
	0x00000000	Reset Software: Release
SGMII0ETN0SGOPMC	0x0000000B	Transfer Rate: 1000Mbps
		Transfer Mode: Full Duplex
		Mode of operation: PHY-LSI Bypass
PWRCTL0SGCLKSEL	0x01	RevMII Output Clock: 25MHz
		Clock: Internal MOSC 20MHz
PWRCTL0ETN0SGRCIE	0x01	Reference Clock: Enabled

Table 1-10 Port Register Setting

Register Name	Setting Values	Function
PCR21_0	0x01000041	P21_0 : ETH0_MDC
PCR21_1	0x01000070	P21_1 : ETH0_MDIO
PCR33_1	0x00000001	P33_1 : ETH0_RESET

1.4.6 Flowchart

The following is a flowchart of this operation example.

1.4.7 Main

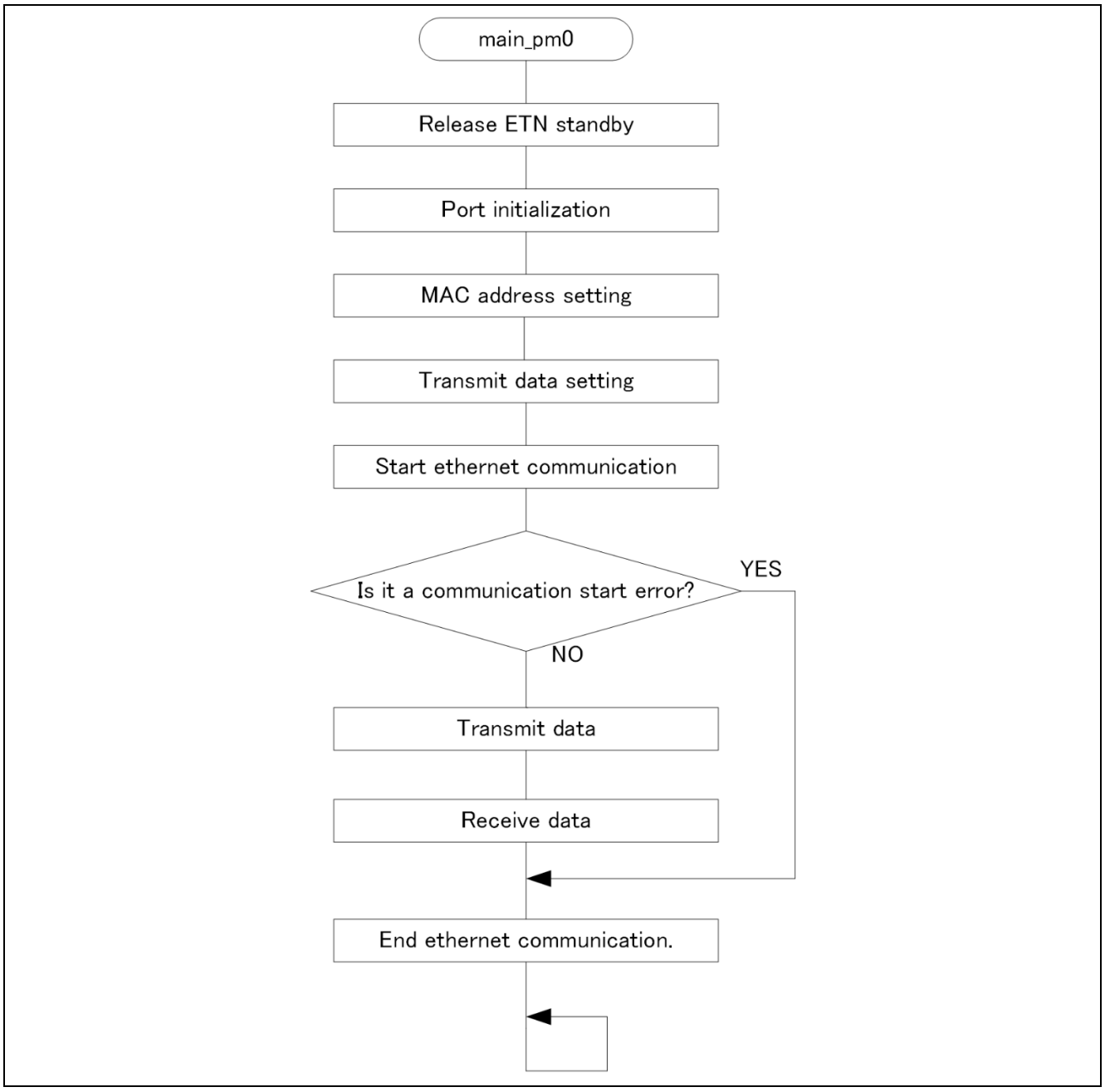

Figure 1-9 Main module flowchart

1.4.8 Start Ethernet Communication

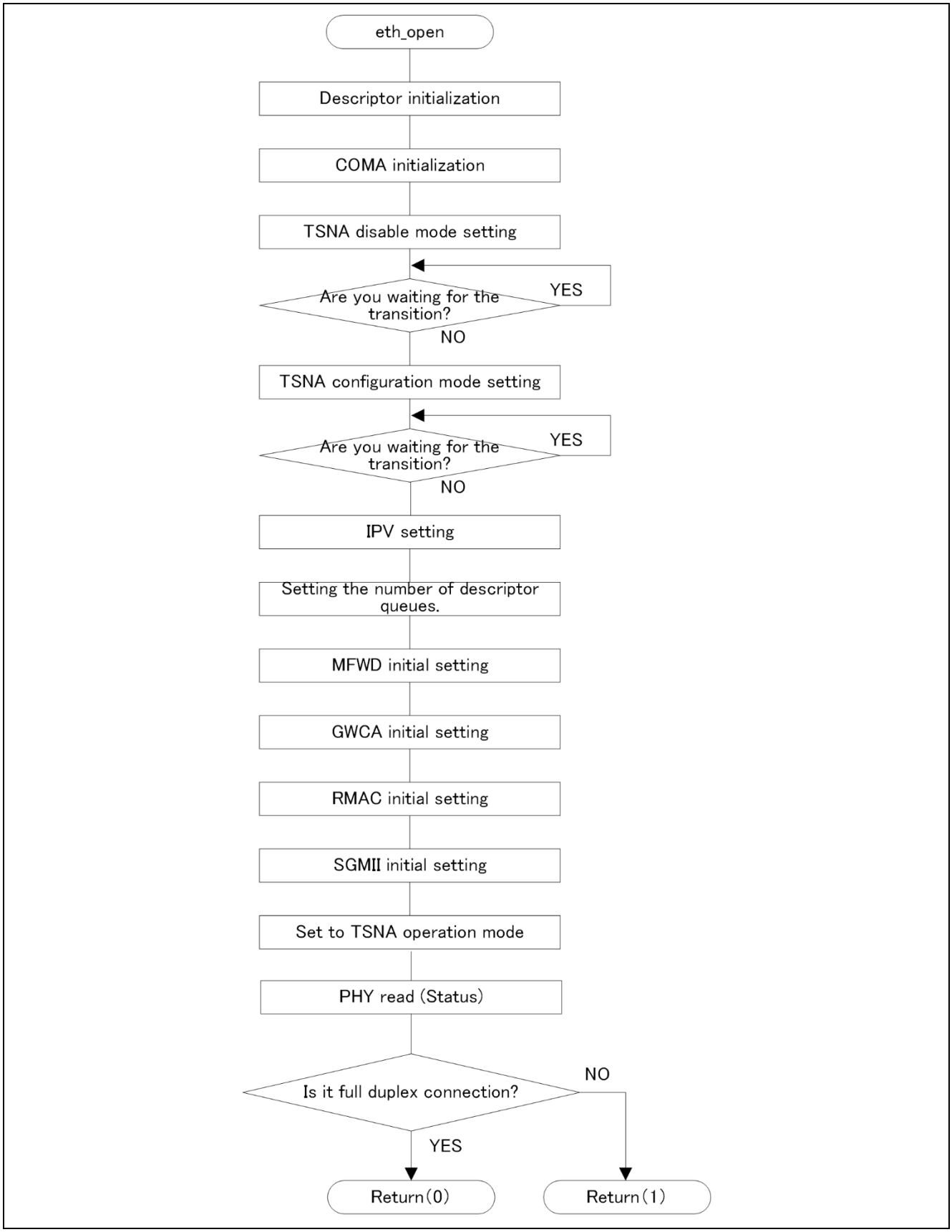

Figure 1-10 Ethernet Communication start module flowchart

1.4.9 End Ethernet Communication

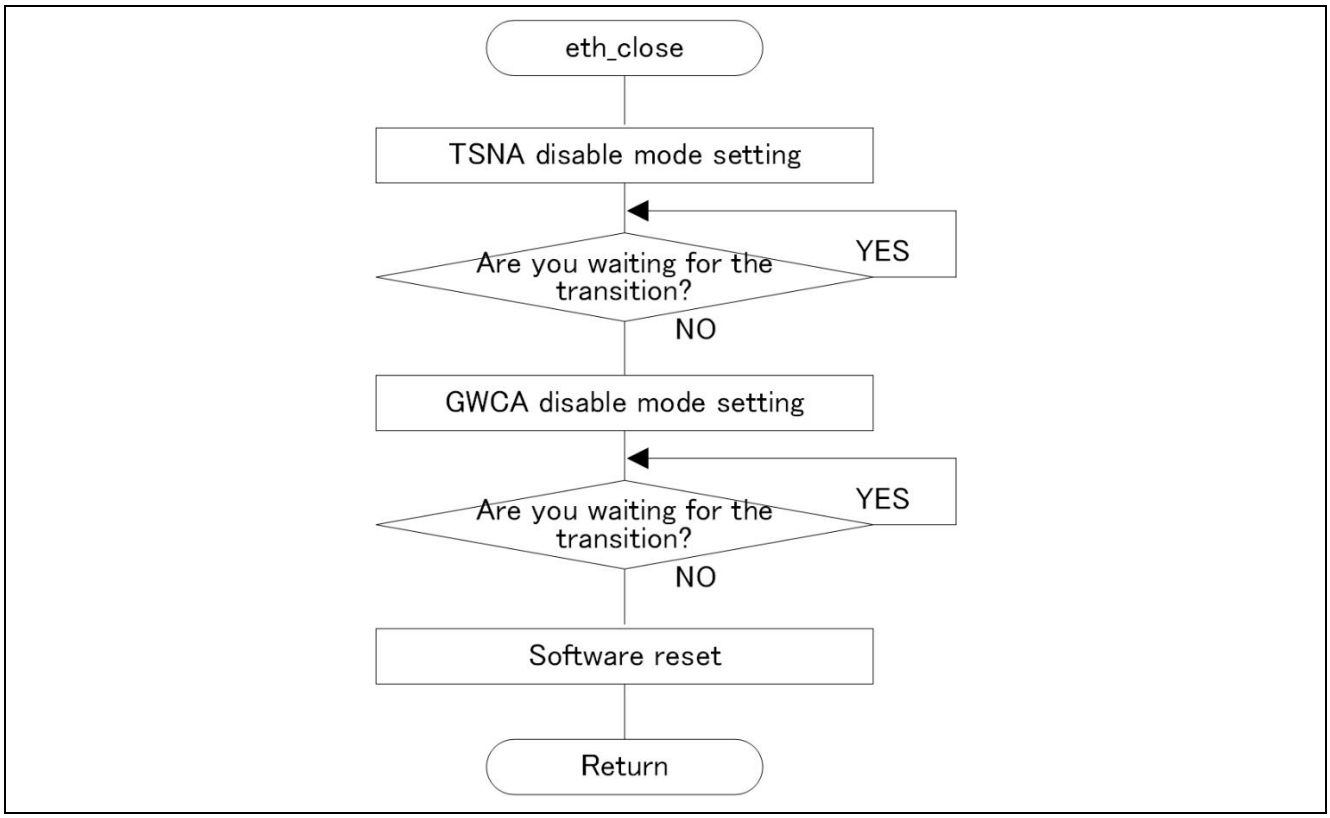

Figure 1-11 Ethernet Communication end module flowchart

1.4.10 COMA Initial Setup

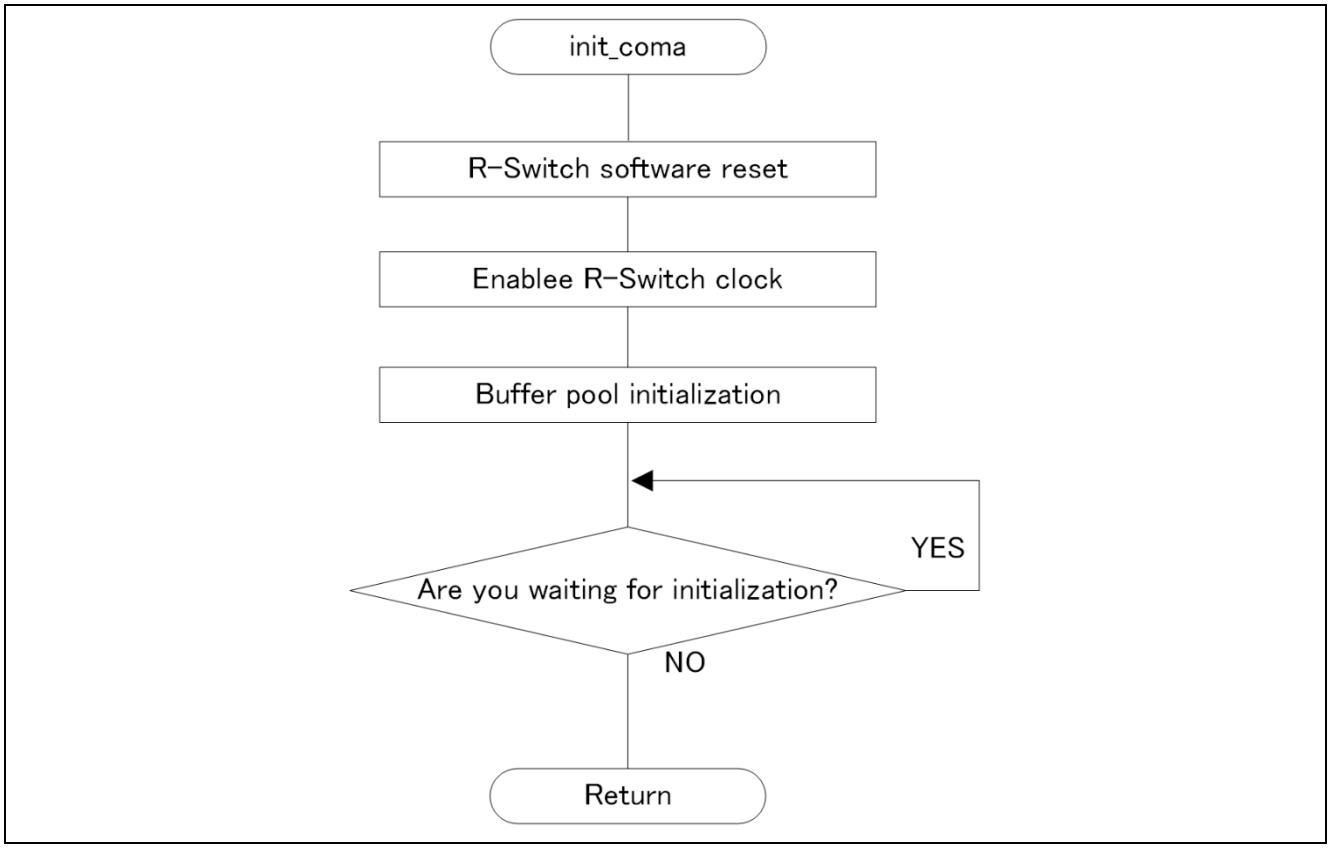

Figure 1-12 COMA initial set up module flowchart

1.4.11 GWCA Initial Setup

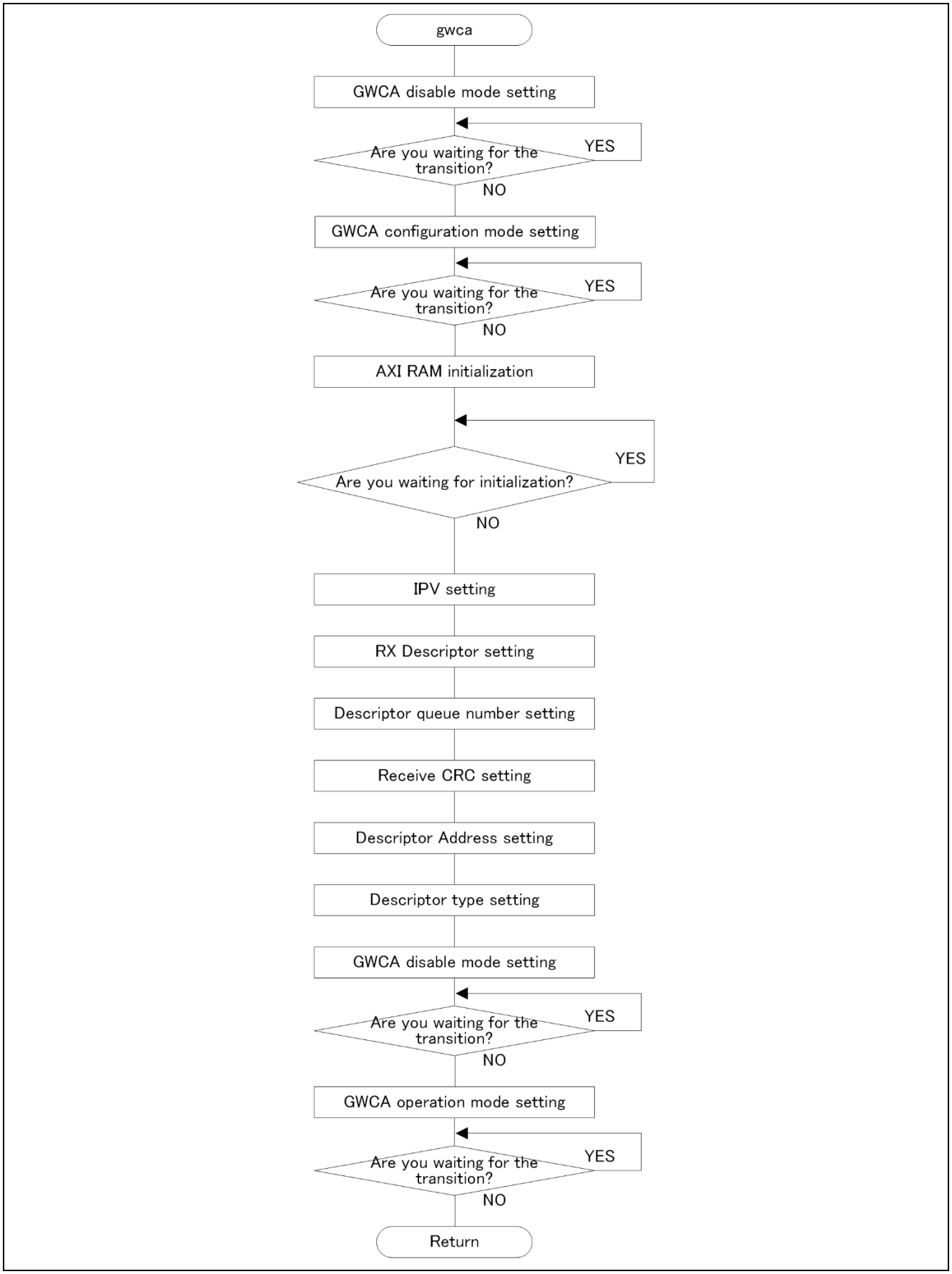

Figure 1-13 GWCA initial set up module flowchart

1.4.12 MFWD Initial Setup

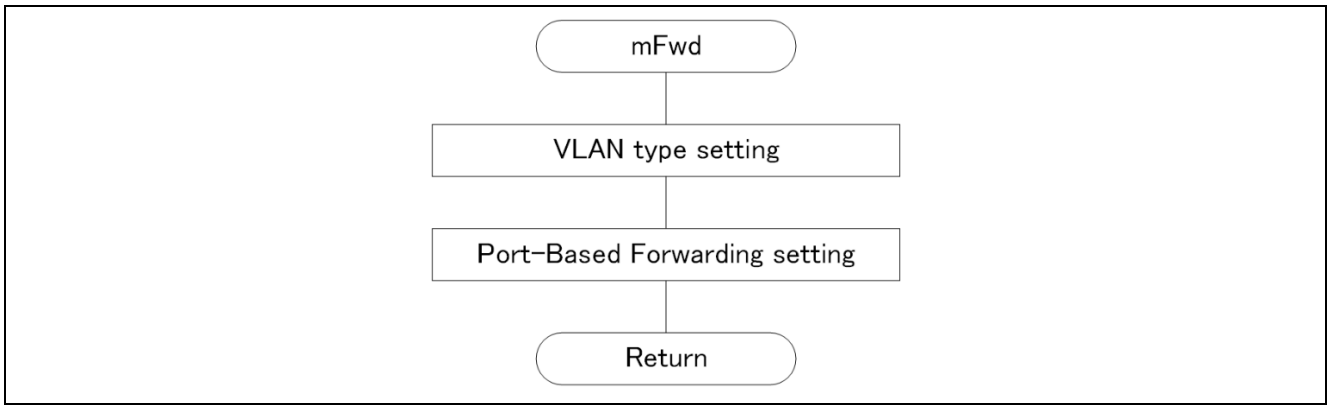

Figure 1-14 MFWD initial set up module flowchart

1.4.13 RMAC Initial Setup

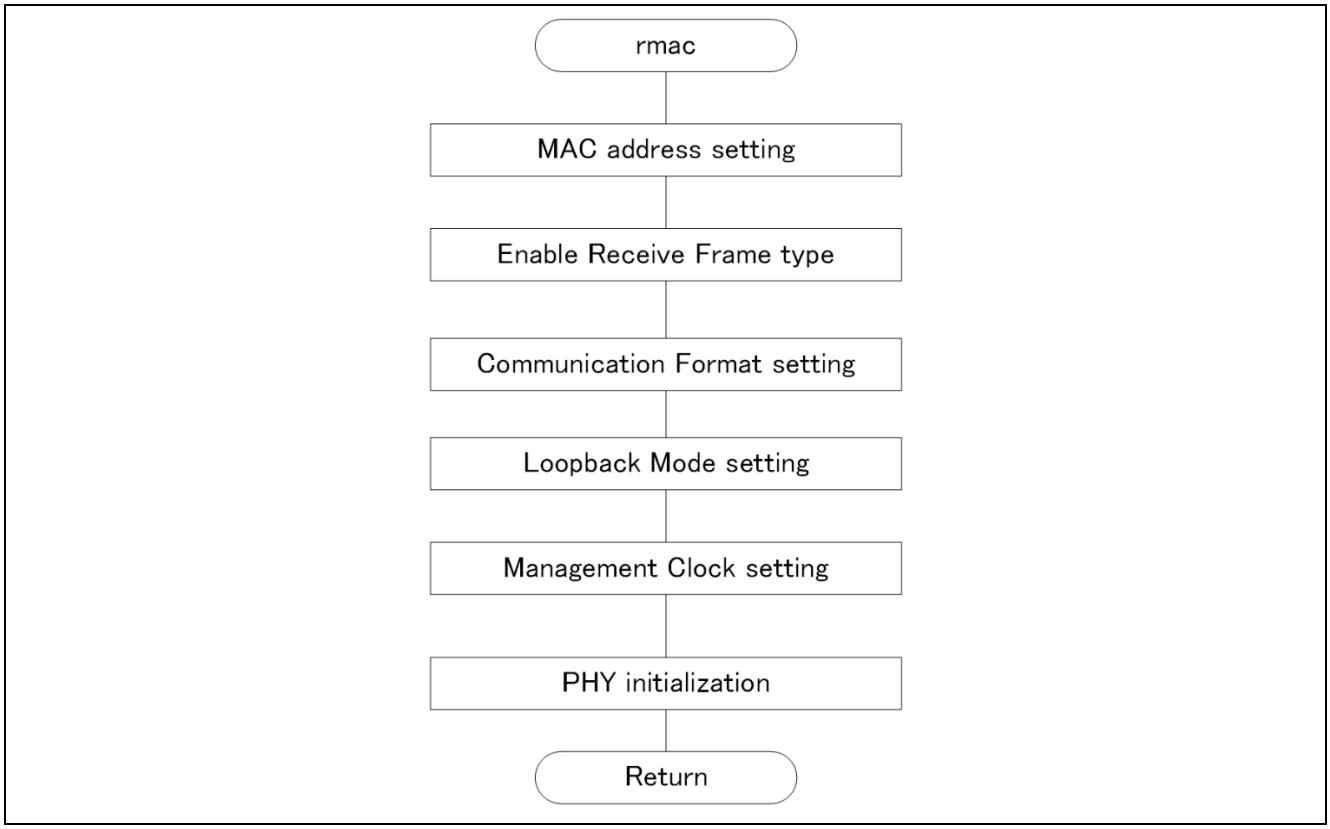

Figure 1-15 RMAC initial set up module flowchart

1.4.14 SGMII Initial Setup

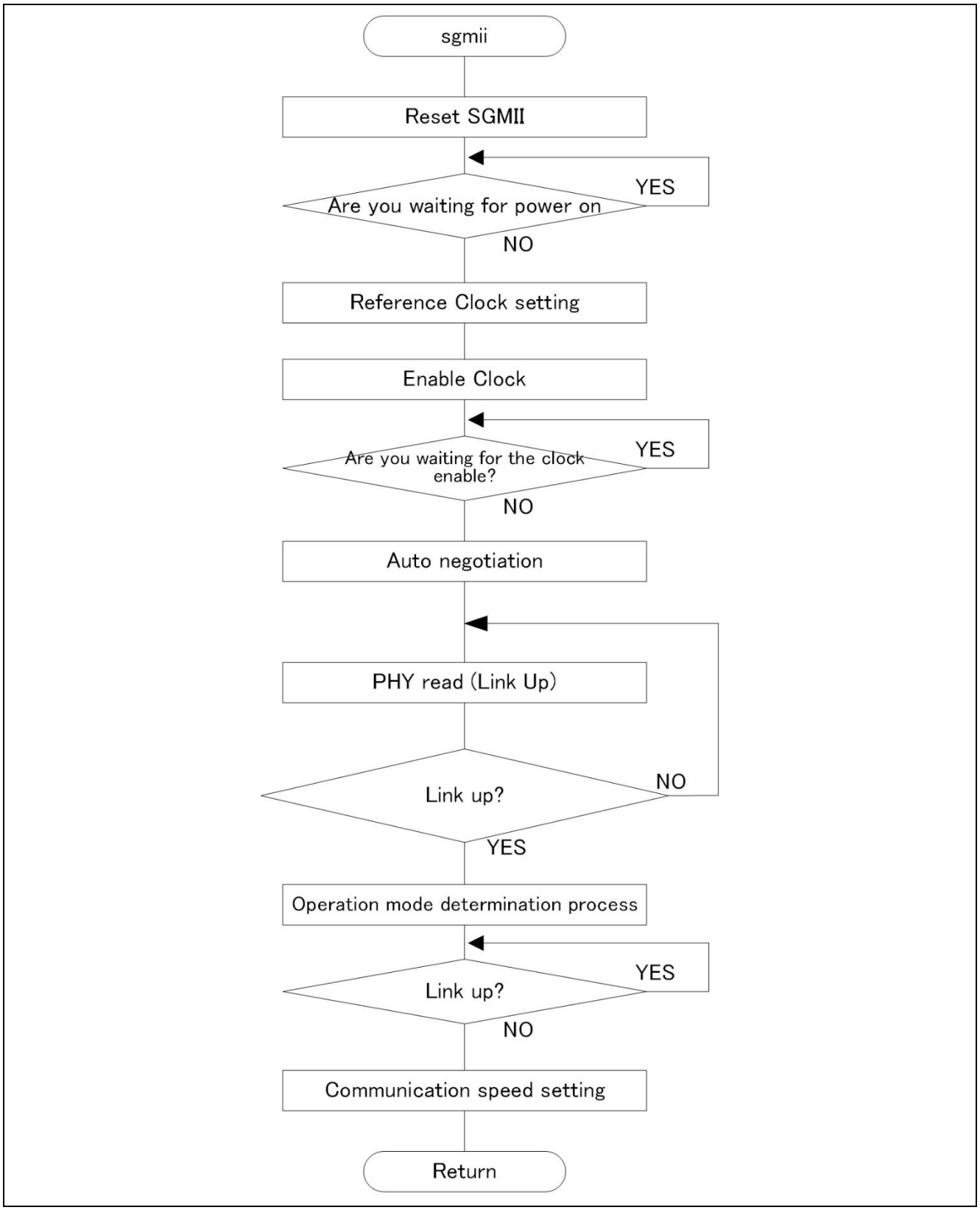

Figure 1-16 SGMII initial set up module flowchart

1.4.15 Descriptor Initialization

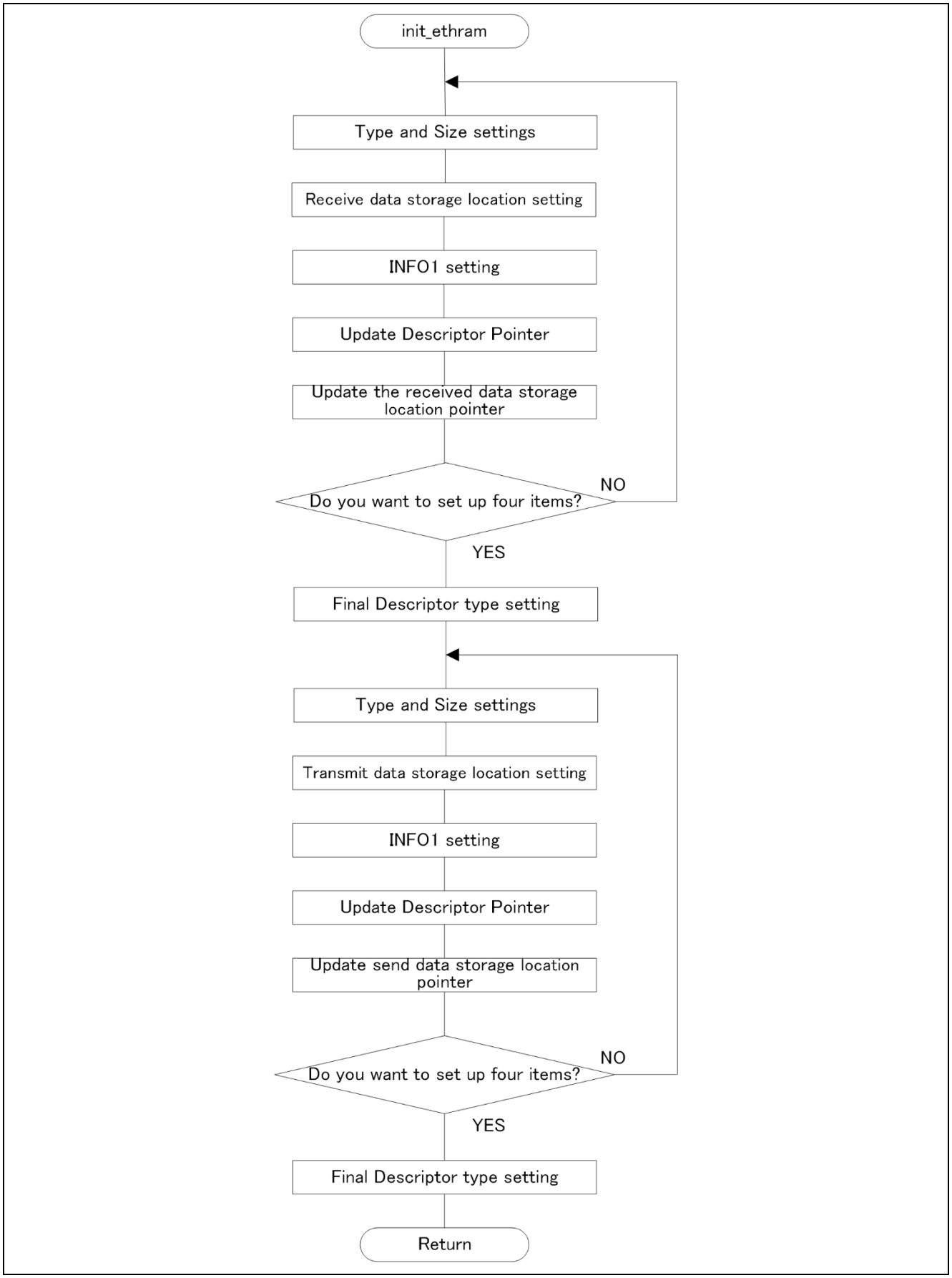

Figure 1-17 Descriptor initialization module flowchart

1.4.16 Data Transmission

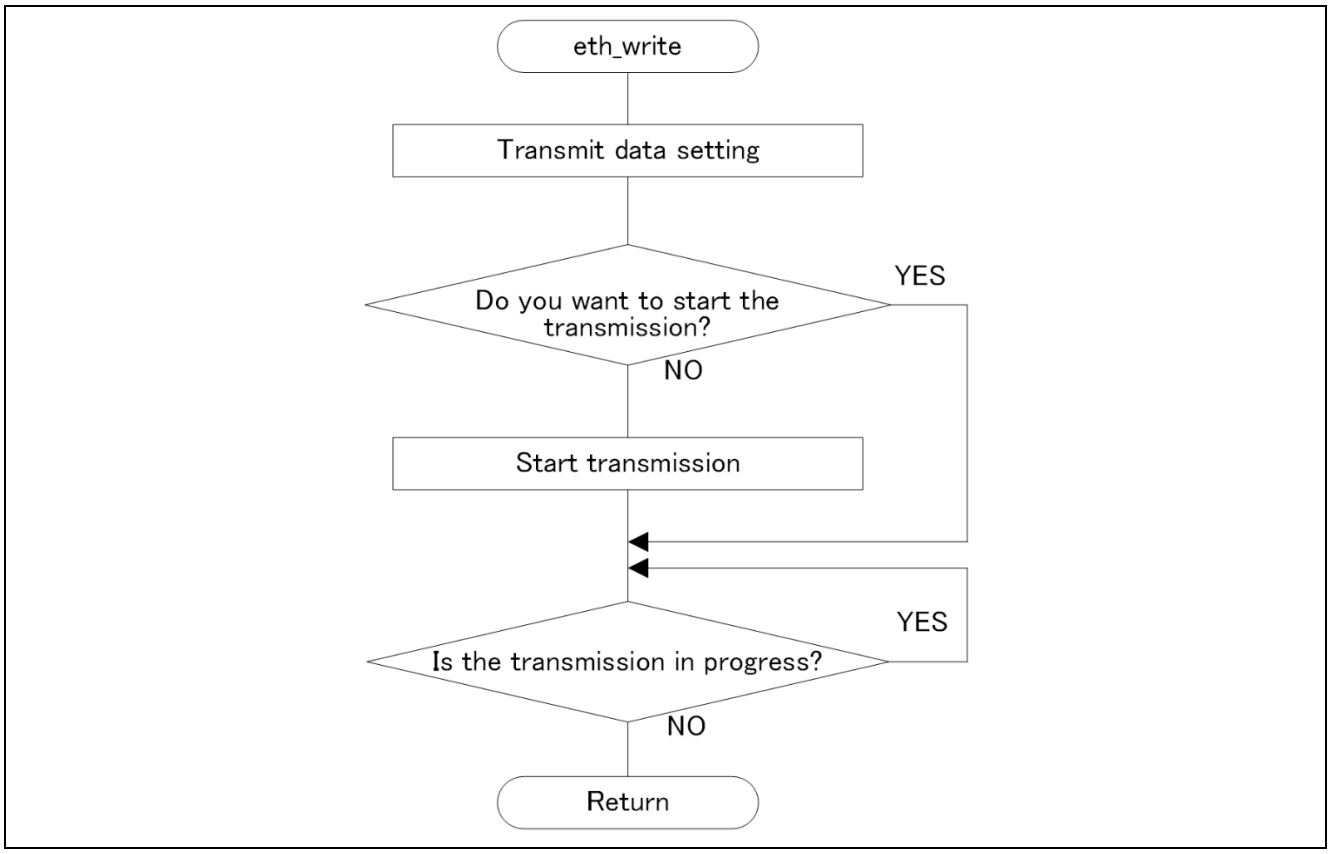

Figure 1-18 Data Transmission module flowchart

1.4.17 Data Receiving

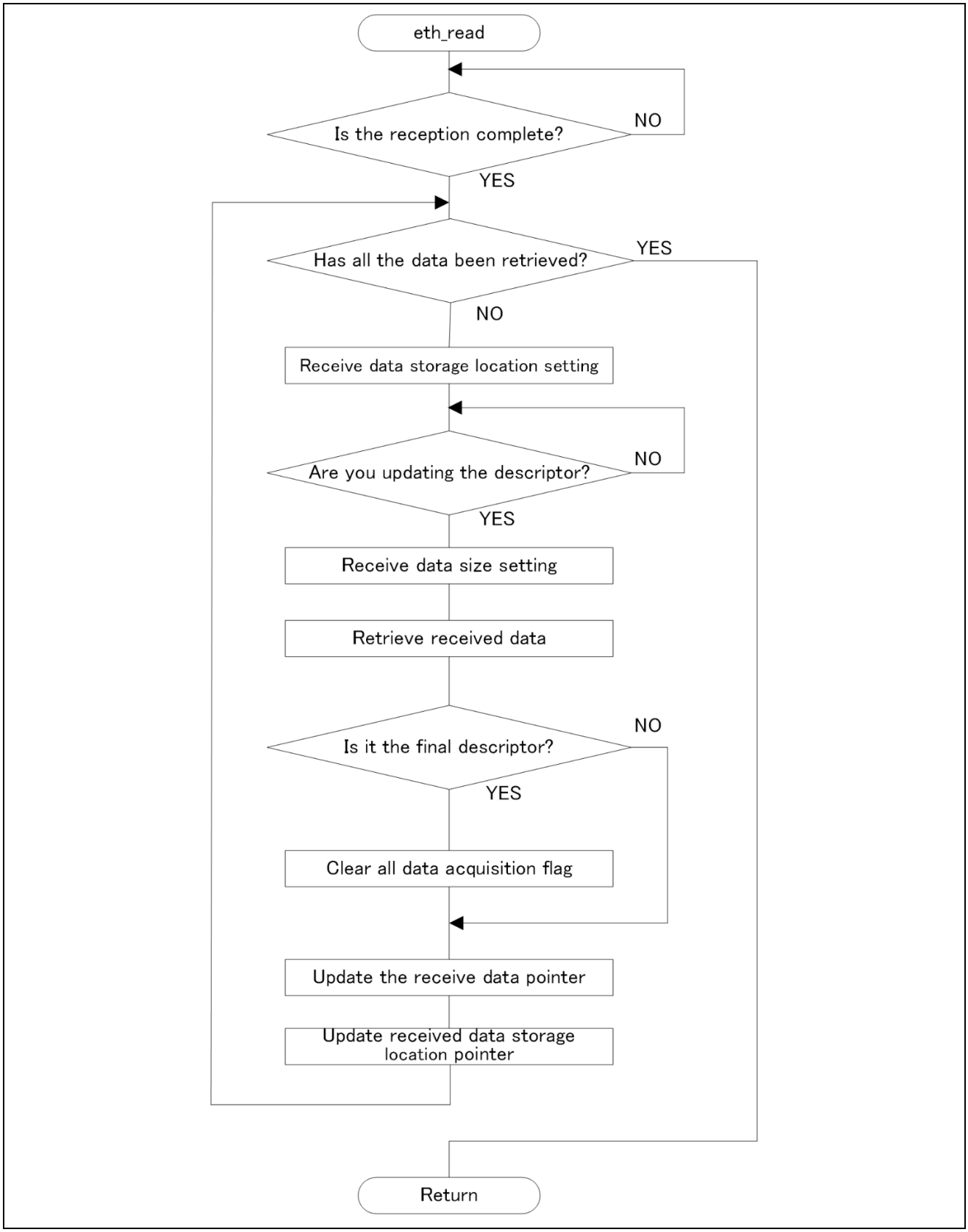

Figure 1-19 Data receiving module flowchart

1.4.18 Transmission Data Setting

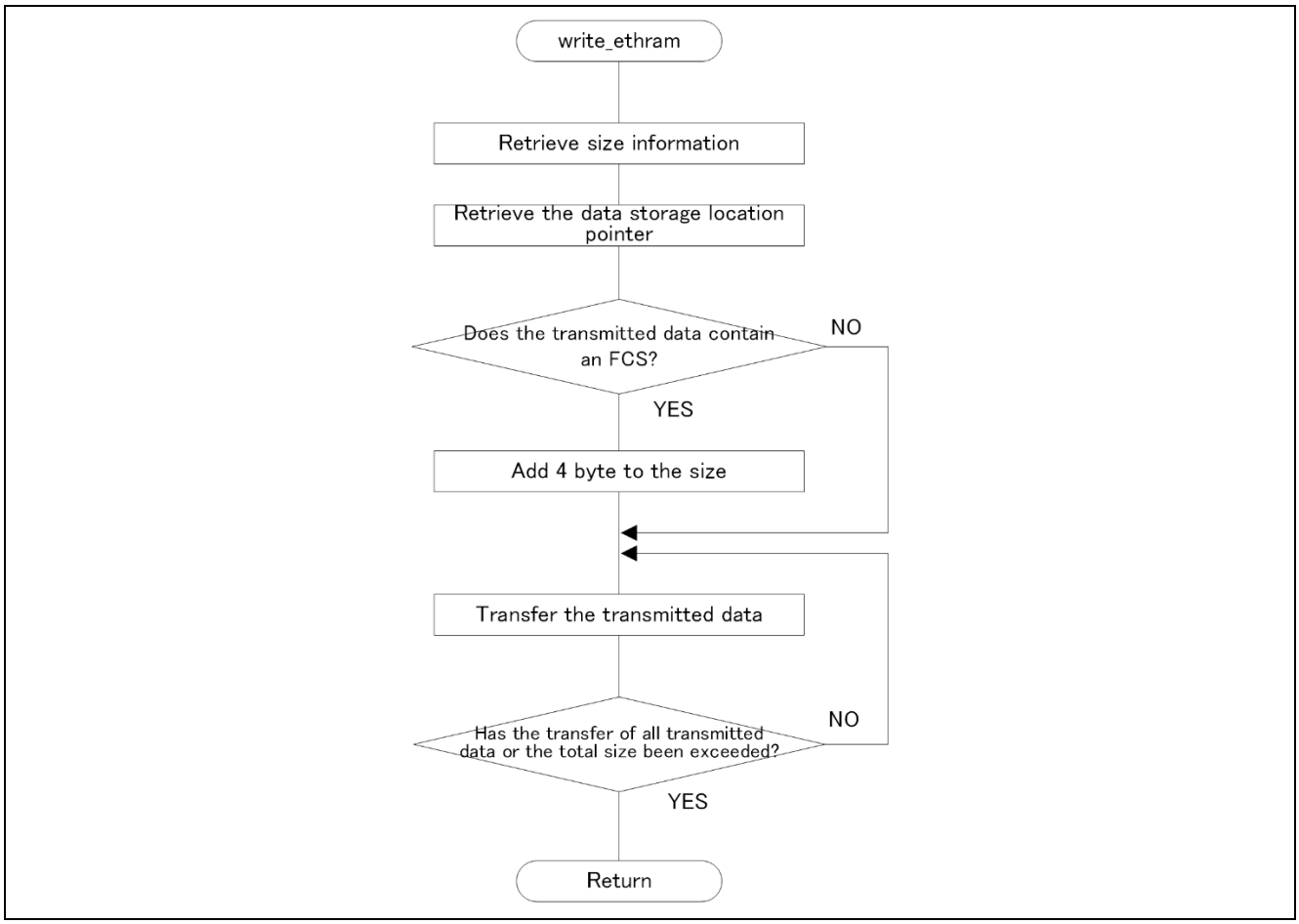

Figure 1-20 Transmission data setting module flowchart

1.4.19 Retrieving Received Data

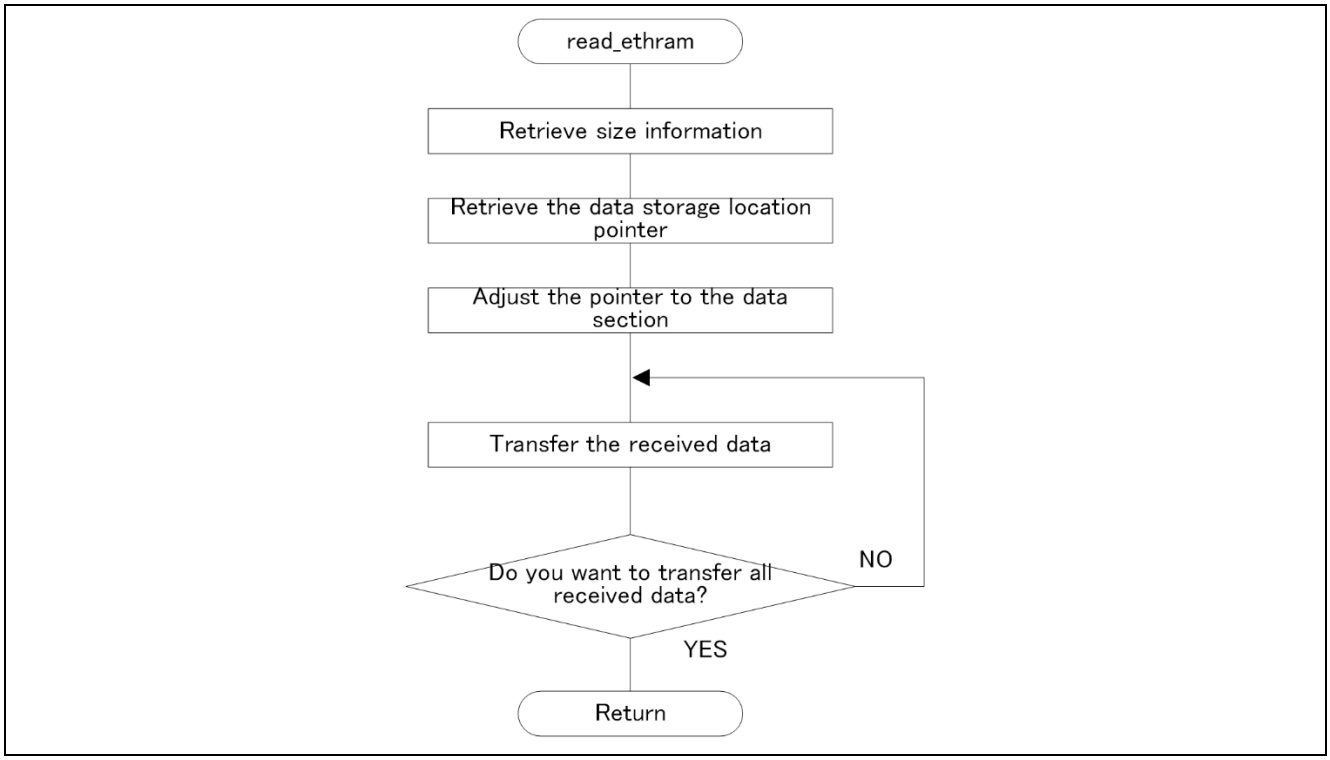

Figure 1-21 Flowchart of the Received Data Retrieval module

1.4.20 PHY Initialization

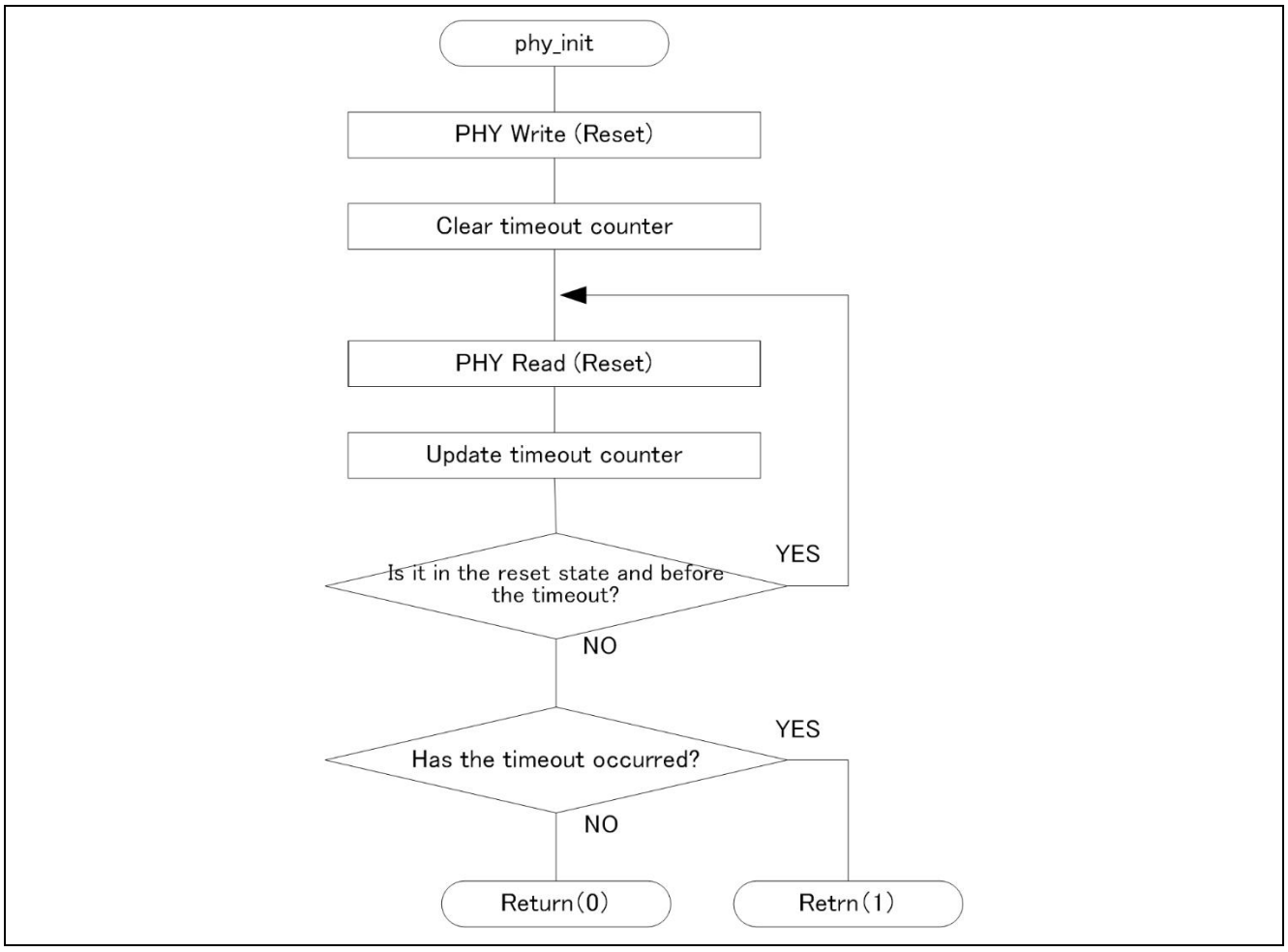

Figure 1-22 PHY initialization module flowchart

1.4.21 Auto Negotiation

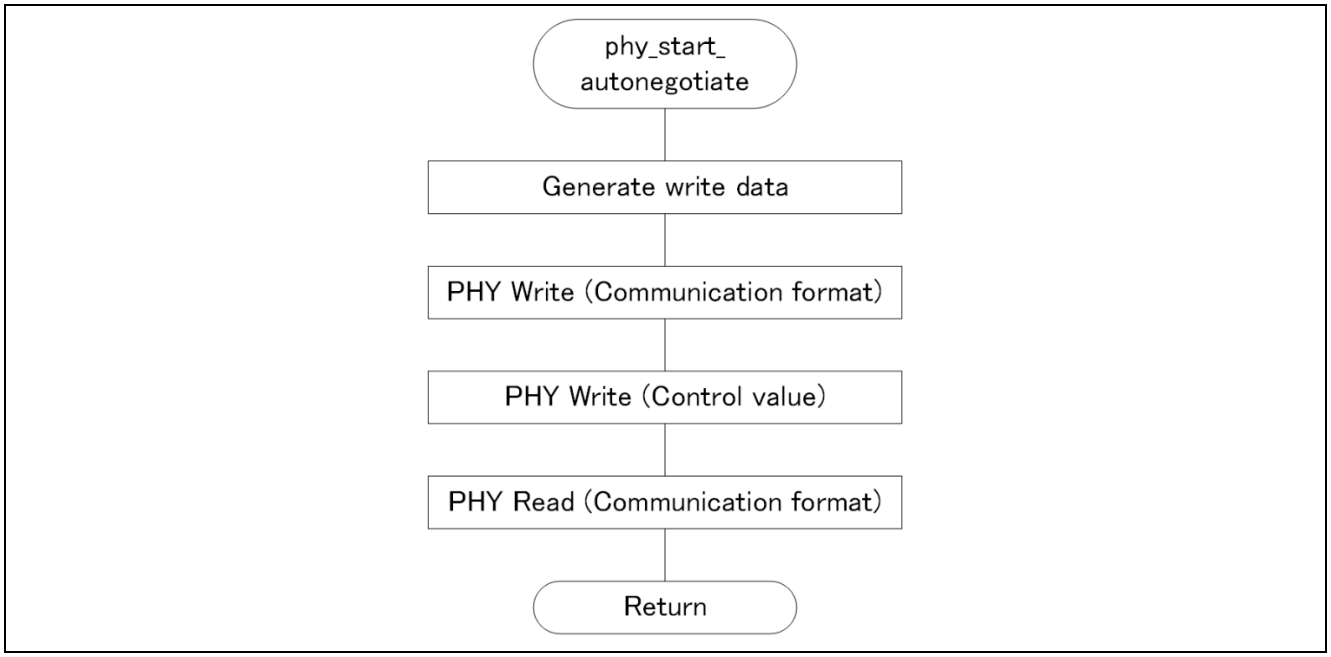

Figure 1-23 Auto Negotiation module flowchart

1.4.22 PHY Write

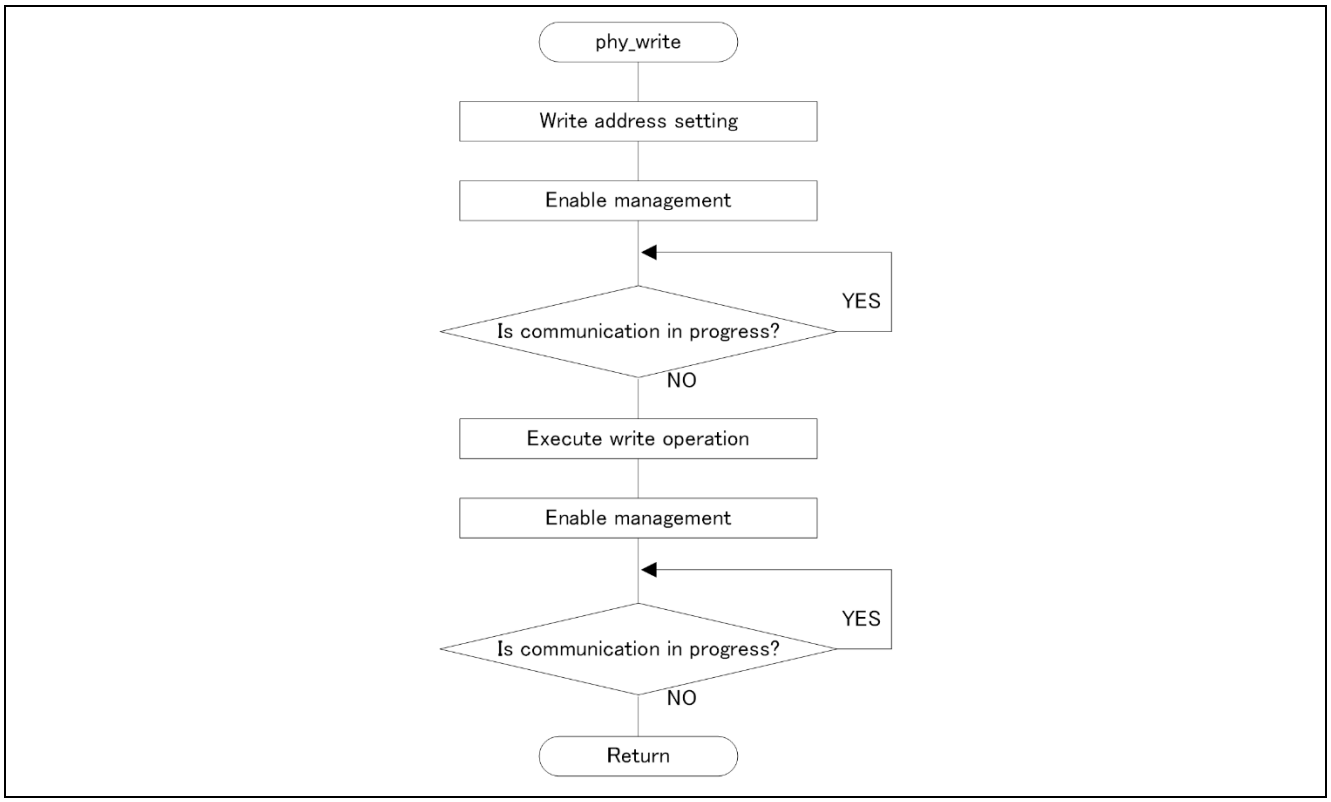

Figure 1-24 PHY Write module flowchart

1.4.23 PHY Read

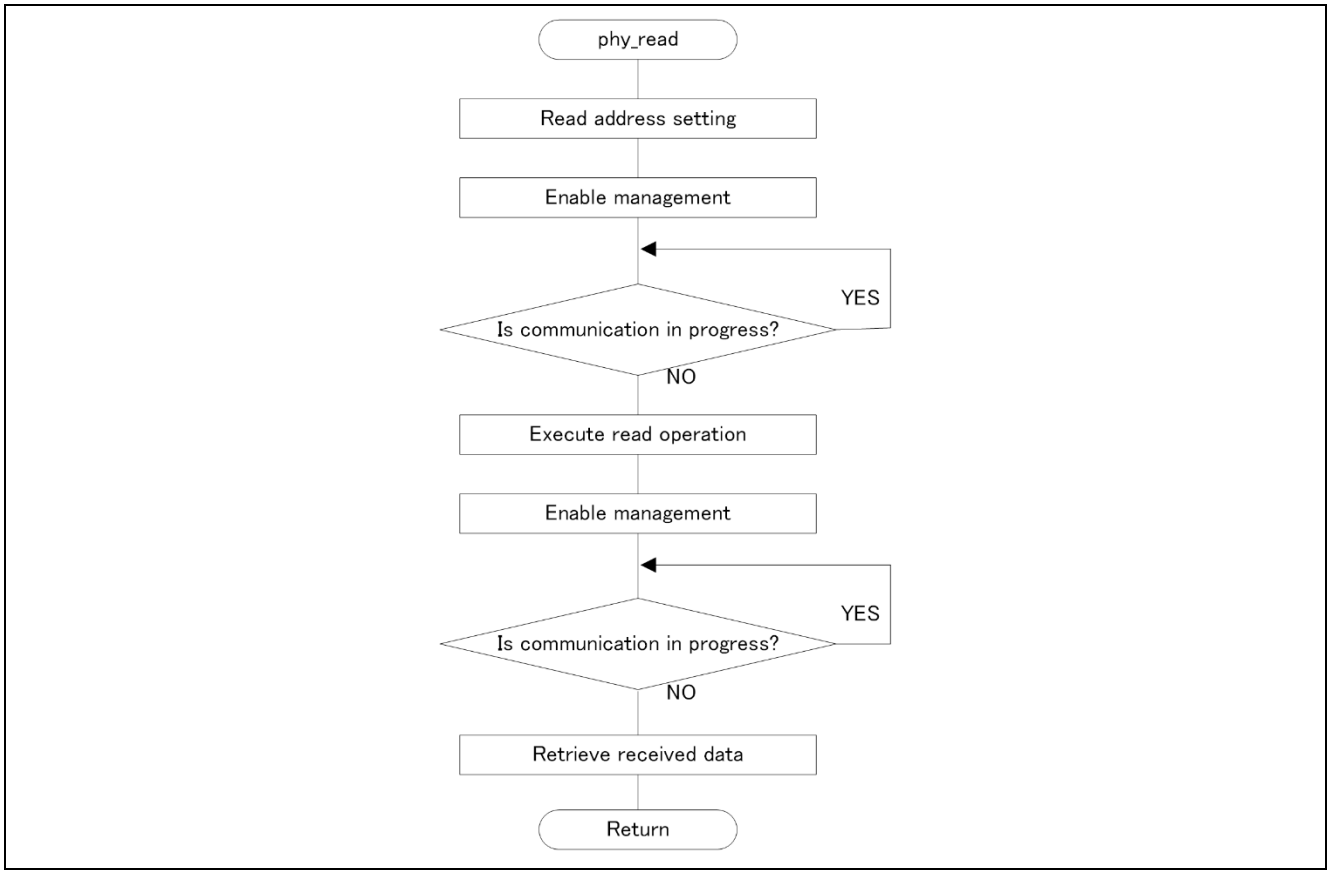

Figure 1-25 PHY Read module flowchart

1.5 256byte Transmit and Receive Operation

This operation example describes the transmission and reception of a 256byte normal frame and the reception of a magic packet.

1.5.1 Communication Specifications

Channel to be used: TSNSWA0

Frame：Normal Frame

Number of data: 256byte

Transmit and Receive FIFO: 256byte

Number of descriptors: 4

1.5.2 System Configuration

Figure 1-26 shows the system configuration.

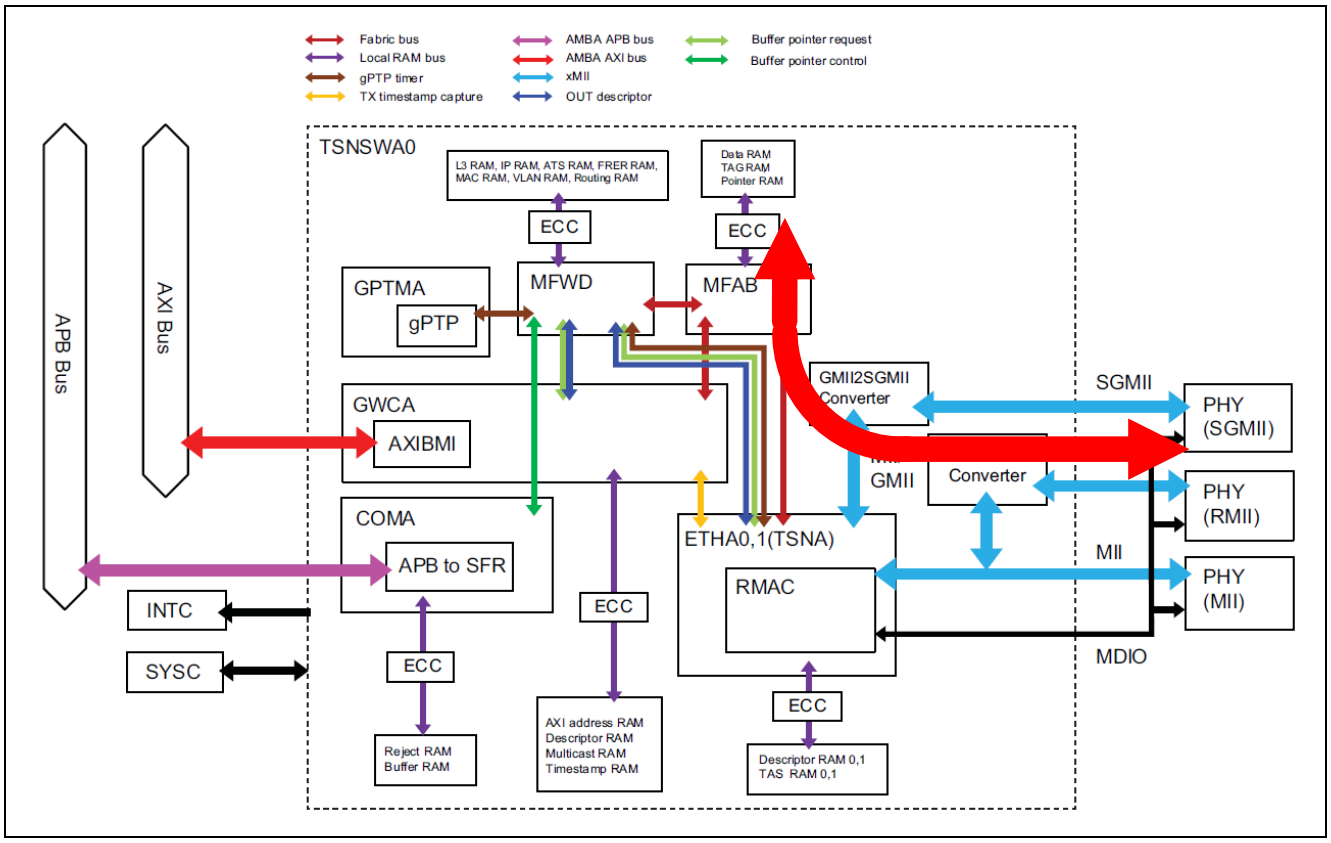

Figure 1-26 System Configuration

1.5.3 Descriptor Description

The data transfer between the storage destination of transmitted and received data (internal RAM) and the FIFO within TSNES is performed using transfer information specified in the descriptor.

In this operation example, the descriptor format is an extended descriptor without a timestamp (16 bytes). The 256byte data is divided into 64-byte segments for transmission and reception.

Table 1-11 shows the descriptor setting values.

Table 1-11 Descriptor Setting Values

Classification	Number	Type	Descriptor Address	Data Storage Destination Address	Size
Receive	1	FEMPTY	0xFDC01000	0xFDC01000	64byte
	2	FEMPTY	0xFDC01010	0xFDC01040	64byte
	3	FEMPTY	0xFDC01020	0xFDC01080	64byte
	4	FEMPTY	0xFDC01030	0xFDC010C0	64byte
	5	EEMPTY	0xFDC01040	-	-
Transmission	1	FSTART	0xFDC01060	0xFDC01500	64byte
	2	FMID	0xFDC01070	0xFDC01540	64byte
	3	FMID	0xFDC01080	0xFDC01580	64byte
	4	FEND	0xFDC01090	0xFDC015C0	64byte
	5	EEMPTY	0xFDC01100	-	-

1.5.4 Receiving a Magic Packet.

This operation example describes receiving a magic packet. The following is the data of the received magic packet.

「0xFF,0xFF,0xFF,0xFF,0xFF,0xFF」、「0x74,0x90,0x50,0x00,0x79,0x03」×16

1.5.5 Software Description

- Module Description

The module list for this operation example is shown below.

Table 1-12 Module list

Module Name	Label Name	Function
Main Routine	main_pm0	Configure various settings and start applications.
Port Initialization Routines	port_init	Configure the initial settings for the port.
Start Ethernet Communication	eth_open	Performs processing to start Ether communication.
End Ethernet Communication	eth_close	Performs processing to end Ether communication.
COMA initial settings	coma	Perform COMA initial settings.
MFWD initial settings	mFwd	Perform MFWD initial settings.
GWCA initial settings	gwca	Perform GWCA initial settings.
RMAC initial settings	rmac	Perform RMAC initial settings.
SGMII initial settings	sgmii	SGMII、PWRCTL initial settings.
Descriptor initialization	init_ethram	Initializes Descriptor.
Data Transmission	eth_write	Set the transmission data and perform the processing to start transmission.
Receiving data	eth_read	Read the received data and perform the storage process.
Transmission Data Settings	write_ethram	Set transmission data in local RAM.
Reception Data Settings	read_ethram	Set received data in local RAM.
PHY initialization	phy_init	Reset the PHY.
Auto Negotiation	phy_start_autonegotiate	Set the communication format, transfer speed, enable auto negotiation, and execute the process.
PHY register read.	phy_read	Specify the PHY register address and read the internal register.
PHY register write	phy_write	Specify the PHY register address and write to the internal register.

- Register Setting

The register settings for each function in this operation example are shown below.

Table 1-13 TSNA Register setting

Register Name	Setting Values	Function
TARO0EAMC	0x00000001	Operation Mode Control: Disable Mode
	0x00000002	Operation Mode Control: Configuration Mode
	0x00000003	Operation Mode Control: Operation Mode
TARO0EAIRC	0x00000000	IPV Remapping: 0
TARO0EATDQDC0	0x00000040	Number of Descriptor Queues: 64
TARO0EAVCC	0x00000000	VLAN Mode: No VLAN.

Table 1-14 COMA Register setting

Register Name	Setting Values	Function
CARORRC	0x00000001	Reset Software
CARORCEC	0x0001000F	Clock Permission: Enabled
CAROCABPIRM	0x00000001	Initialization: Common Agent Pool Buffer Initialization

Table 1-15 MFWD Register setting

Register Name	Setting Values	Function
FWROFWGC	0x00000000	VLAN Mode: No VLAN.
FWROFWPBFC0	0x00000004	Port Based Forwarding: Port 0
FWROFWPBFC2	0x00000001	Port Based Forwarding: Port 2

Table 1-16 GWCA Register Setting

Register Name	Label Name	Function
GWROGWMC	0x00000001	Operation Mode Control: Disable Mode
	0x00000002	Operation Mode Control: Configuration Mode
	0x00000003	Operation Mode Control: Operation Mode
GWROGWARIRM	0x00000001	AXI RAM Initialization：Enabled
GWROGWIRC	0x00000000	IPV Remapping: 0
GWROGWRDQC	0x00000000	Receive Descriptor Queue Pause: Disabled
		Receive Descriptor Queue Prohibited: Enabled
GWROGWRDQDC0	0x00000040	Number of Descriptor Queues: 64
GWROGWRGC	0x00000001	Received CRC Passed: FCS Passed
GWROGWDCBAC0	0x00000000	AXI Descriptor Address High: 0x00000000
GWROGWDCBAC1	axidpkt	AXI Descriptor Address Low: Address of axidpkt Header
GWROGWMDNC	0x00000404	Timestamp Descriptor Maximum Value: 0
		Transmit Descriptor Maximum Value: 4
		Receive Descriptor Maximum Value: 4
GWROGWDCC0	0x01000100	Base Address Request: Enabled
		Descriptor Type: Receive
		Extended Descriptor: Extended
GWROGWDCC2	0x01000900	Base Address Request: Extended
		Descriptor Type: Transmit
		Extended Descriptor: Extended

Table 1-17 RMAC Register Setting

Register Name	Label Name	Function
RMACA0MRMAC1	MAC_ADDR [1] MAC_ADDR [2]	MAC Address Low: MAC_ADDR [1], MAC_ADDR [2]
RMACA0MRMAC0	MAC_ADDR [0]	MAC Address High: MAC_ADDR [0]
RMACA0MPIC	0x121A0408	Capture Time Adjustment: 1
		Hold Time Adjustment: 2
		Preamble Suppression: Disabled
		Clock Selection: 0x1A(clk/54=2.46MHz)
		Link Speed: 1000Mbps
		PHY I/F：GMII
RMRO0MRGC	0x0000000F	Magic Packet Detection: Enabled
		Pause Frame Reception Time: Enabled
		Pause Frame Reception Control: Enabled
		Received CRC Check: Enabled

RMRO00MPSM （During Read）	0xXXXXYY04	PHY Register Data: XXXX (regad)
		Operation Code: YY Bit 6-5 (Address Frame = 0)
		PHY Register Address: YY bit 4-0 (devad)
		PHY Device Address: 0
		Management Frame Format: Clause 45
		Management: Enable
	↓	↓
	0xXXXXYY04	PHY Register Data: XXXX (data)
		Operation Code: YY Bit 6-5 (Read Frames = 3)
		PHY Register Address: YY bit 4-0 (devad)
		PHY Device Address: 0
		Management Frame Format: Clause 45
		Management: Enable
RMRO0MPSM （During Write）	0xXXXXYY04	PHY Register Data: XXXX (regad)
		Operation Code: YY Bit 6-5 (Address Frame = 0)
		PHY Register Address: YY bit 4-0 (devad)
		PHY Device Address: 0
		Management Frame Format: Clause 45
		Management: Enable
	↓	↓
	0xXXXXYY04	PHY Register Data: XXXX (data)
		Operation Code: YY Bit 6-5 (Read Frames = 2)
		PHY Register Address: YY bit 4-0 (devad)
		PHY Device Address: 0
		Management Frame Format: Clause 45
		Management: Enable

Table 1-18 SGMII Register Setting

Register Name	Setting Values	Function
SGMII0ETN0SGSRST	0x00000001	Reset Software: Reset
	0x00000000	Reset Software: Release
SGMII0ETN0SGOPMC	0x0000000B	Transfer Rate: 1000Mbps
		Transfer Mode: Full Duplex
		Mode of operation: PHY-LSI Bypass
PWRCTL0SGCLKSEL	0x01	RevMII Output Clock: 25MHz
		Clock: Internal MOSC 20MHz
PWRCTL0ETN0SGRCIE	0x01	Reference Clock: Enabled

Table 1-19 Port Register Setting

Register Name	Setting Values	Function
PCR21_0	0x01000041	P21_0 : ETH0_MDC
PCR21_1	0x01000070	P21_1 : ETH0_MDIO
PCR33_1	0x00000001	P33_1 : ETH0_RESET

1.5.6 Flowchart

The following is a flowchart of this operation example.

1.5.7 Main

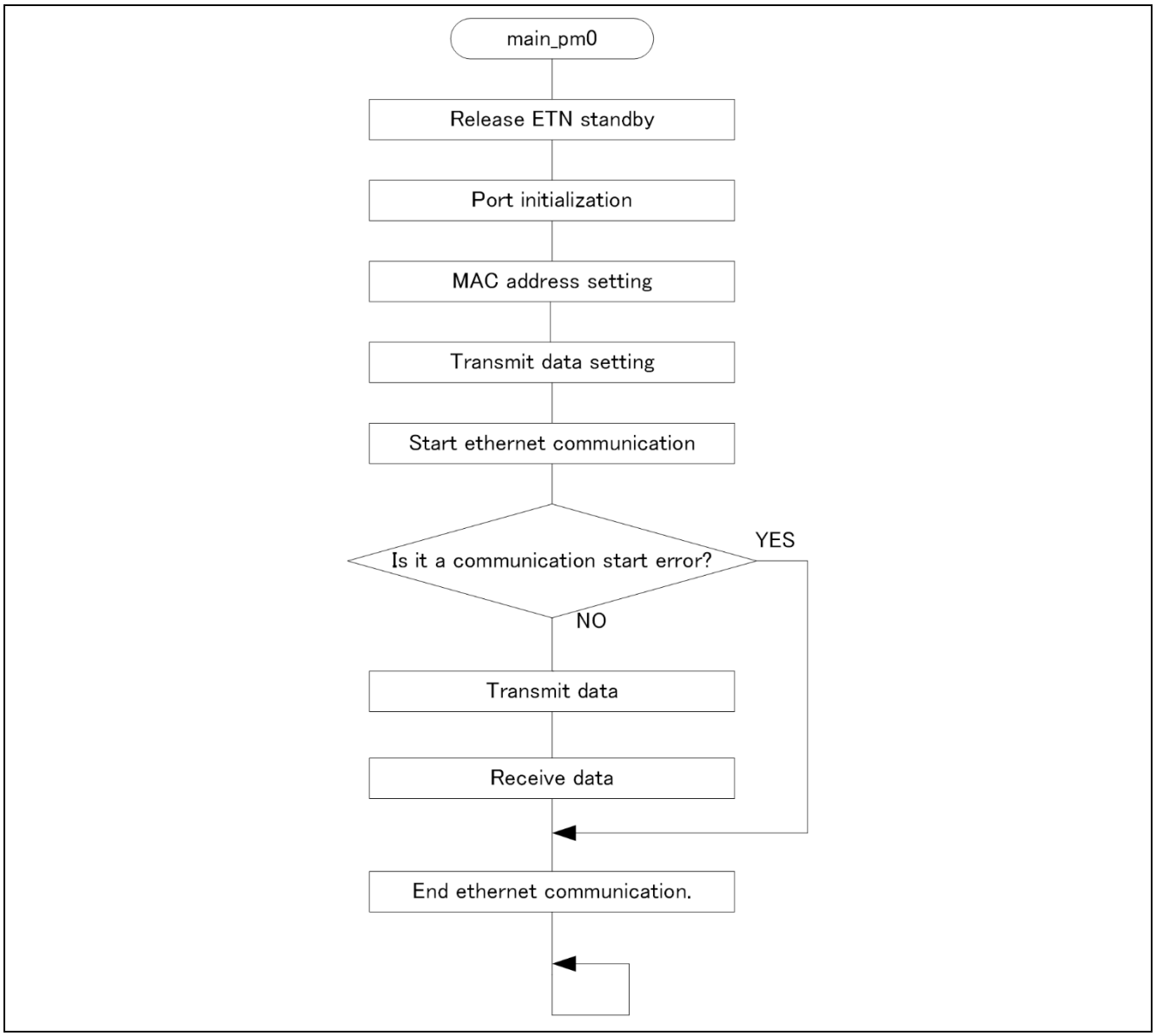

Figure 1-27 Main module flowchart

1.5.8 Start Ethernet Communication

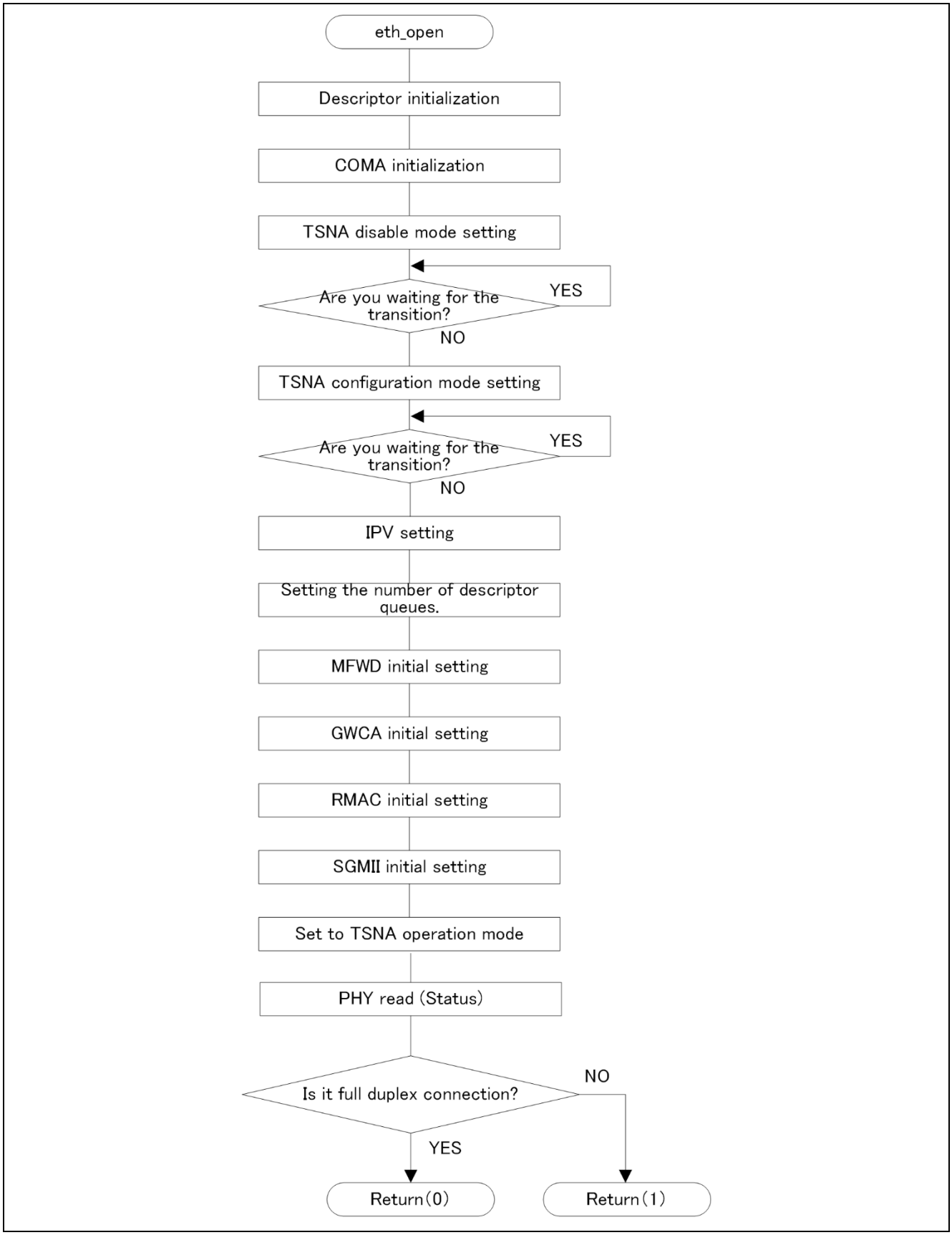

Figure 1-28 Ethernet Communication start module flowchart

1.5.9 End Ethernet Communication

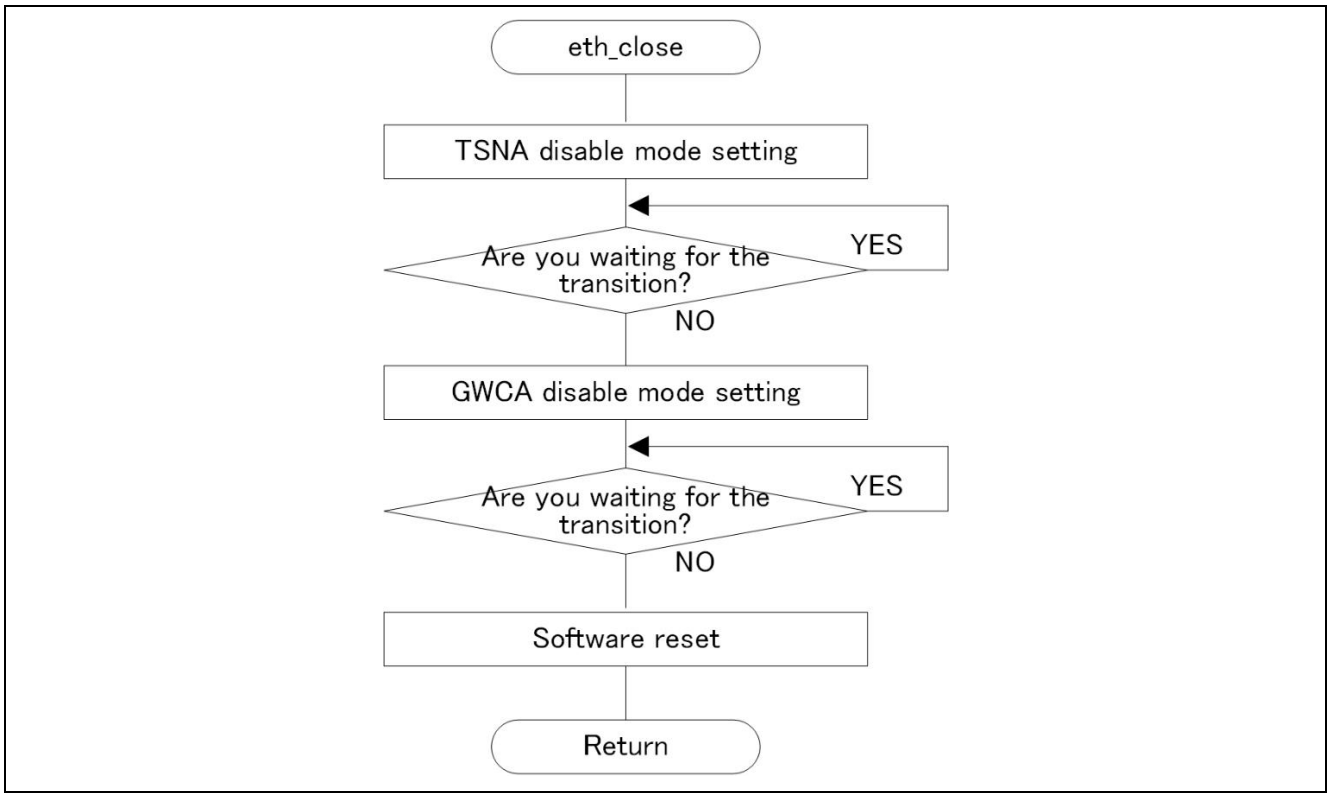

Figure 1-29 Ethernet communication end module flowchart

1.5.10 COMA Initial Setup

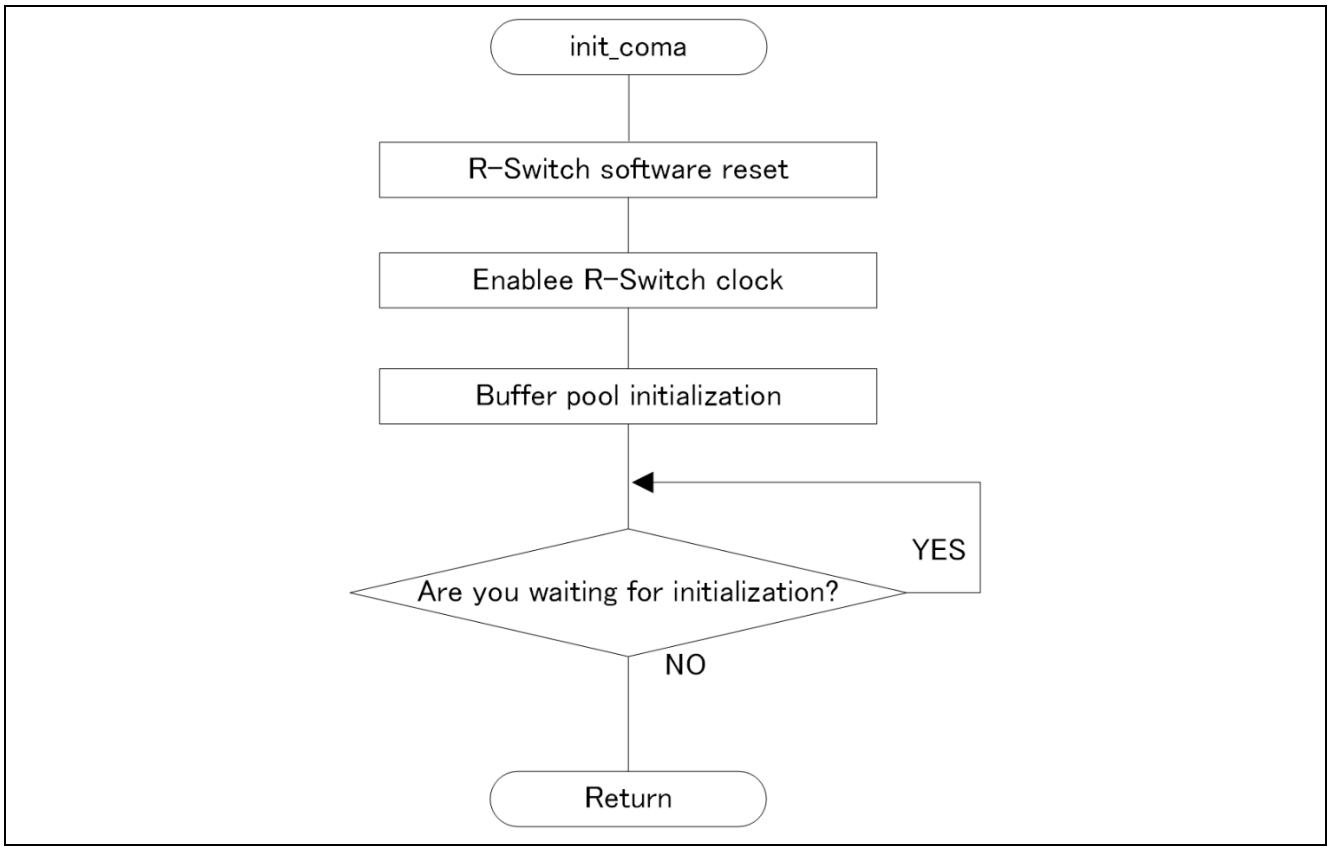

Figure 1-30 COMA initial set up module flowchart

1.5.11 GWCA Initial Setup

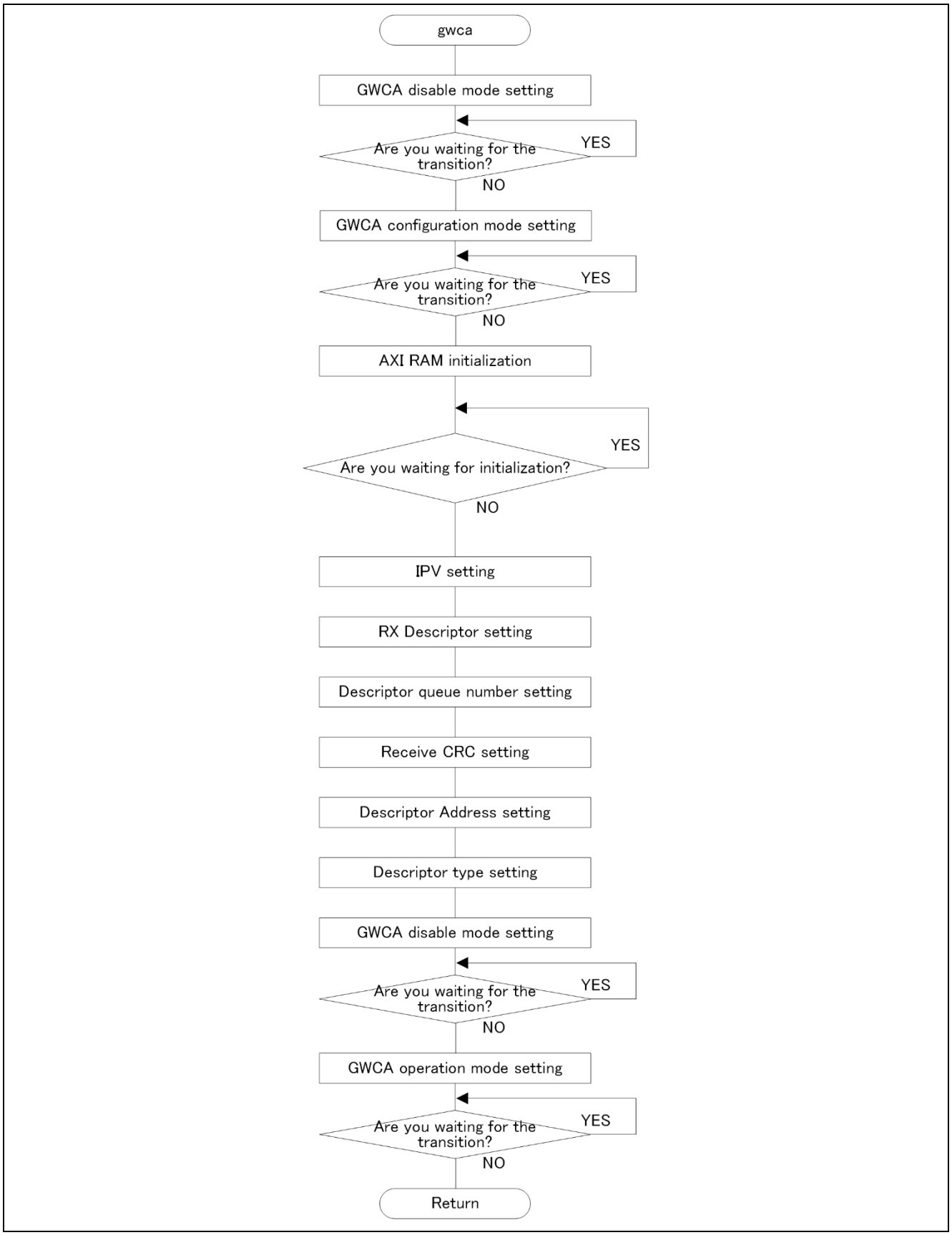

Figure 1-31 GWCA initial set up module flowchart

1.5.12 MFWD Initial Setup

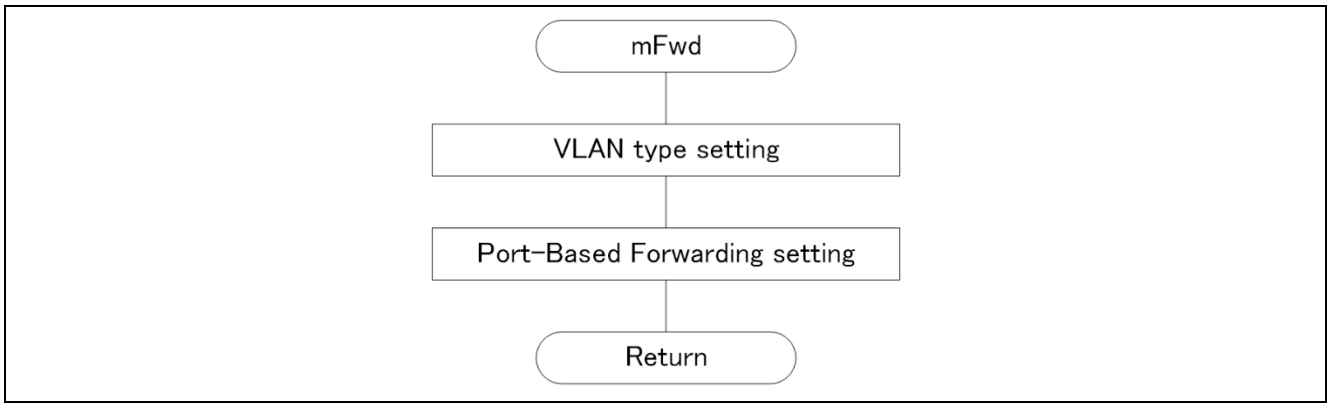

Figure 1-32 MFWD initial set up module flowchart

1.5.13 RMAC Initial Setup

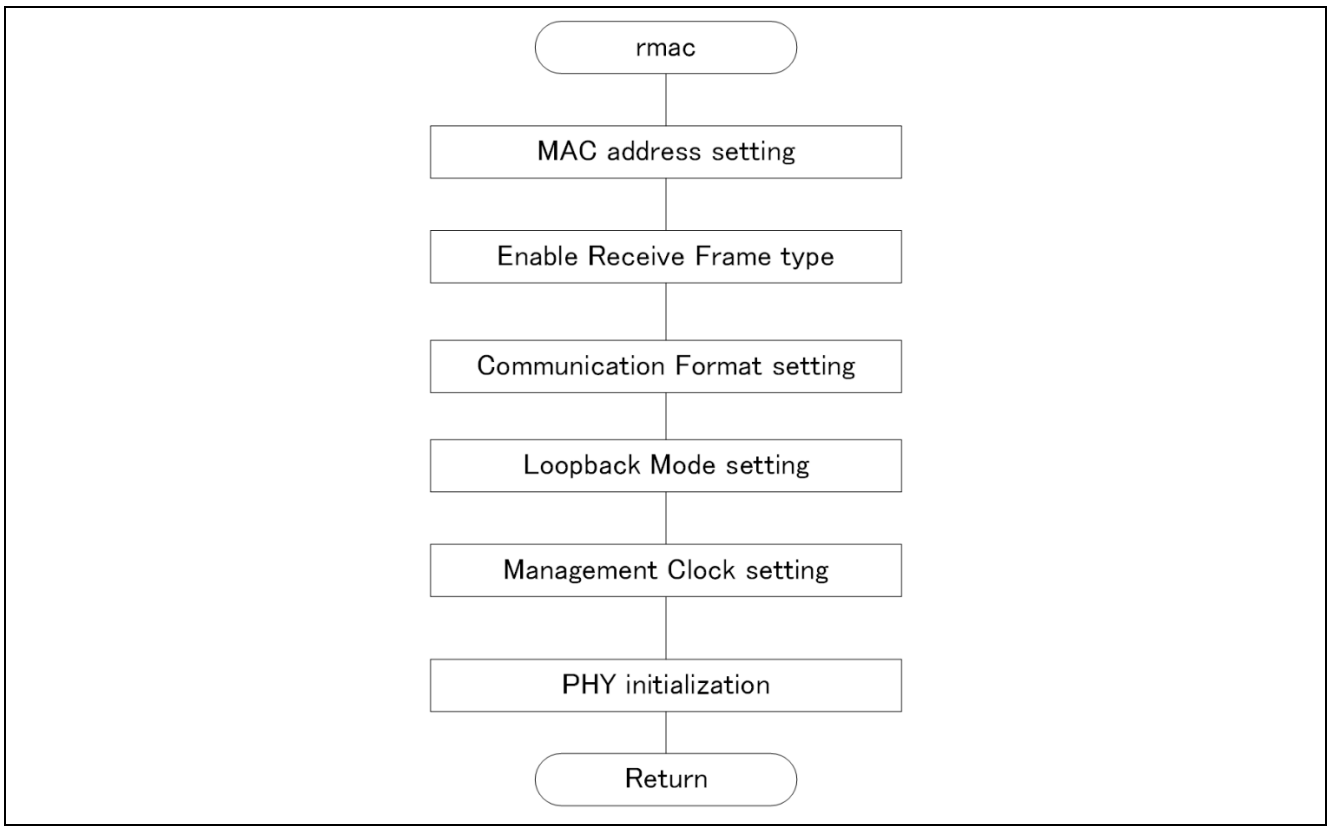

Figure 1-33 RMAC initial set up module flowchart

1.5.14 SGMII Initial Setup

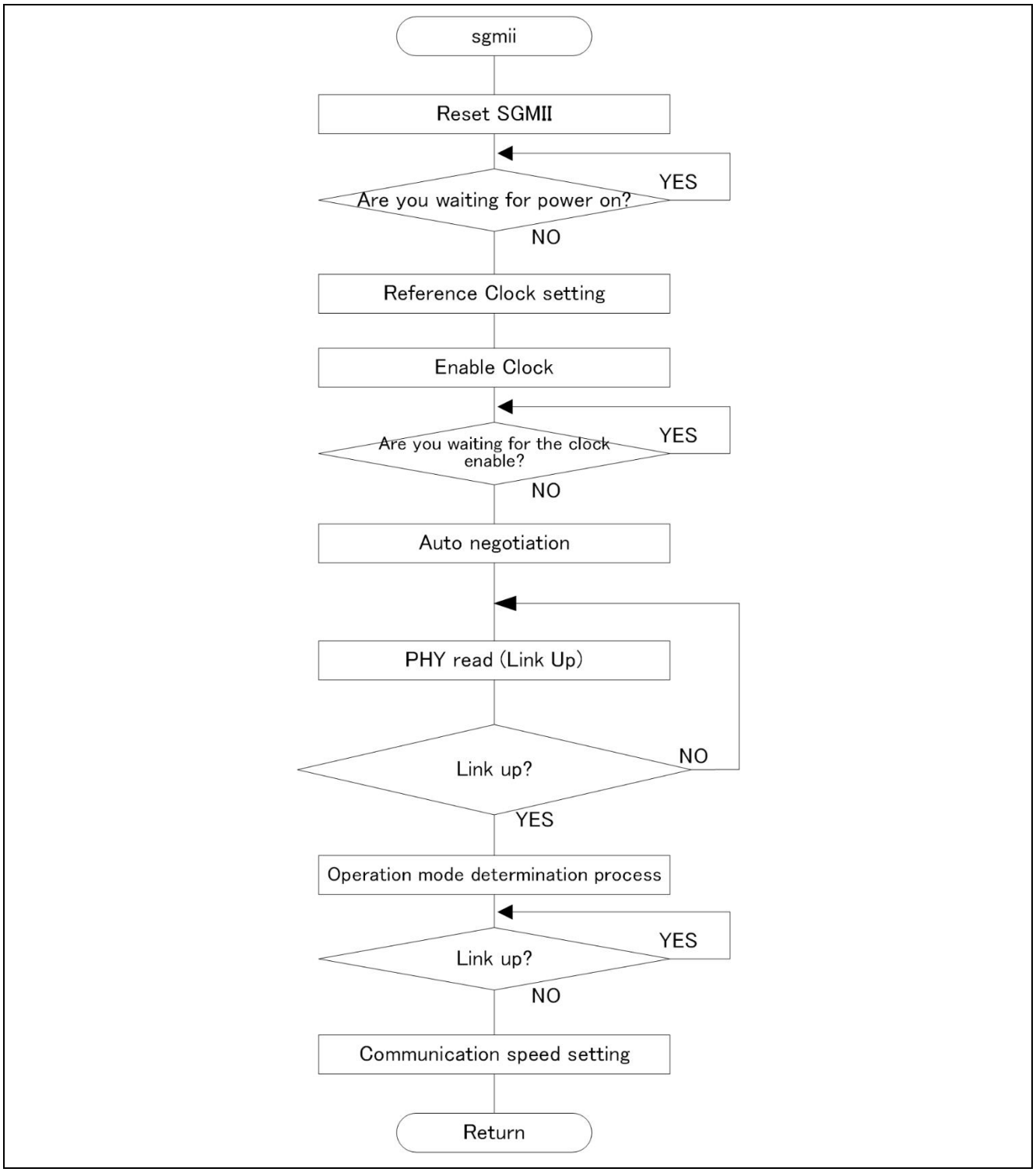

Figure 1-34 SGMII initial set up module flowchart

1.5.15 Descriptor initialization

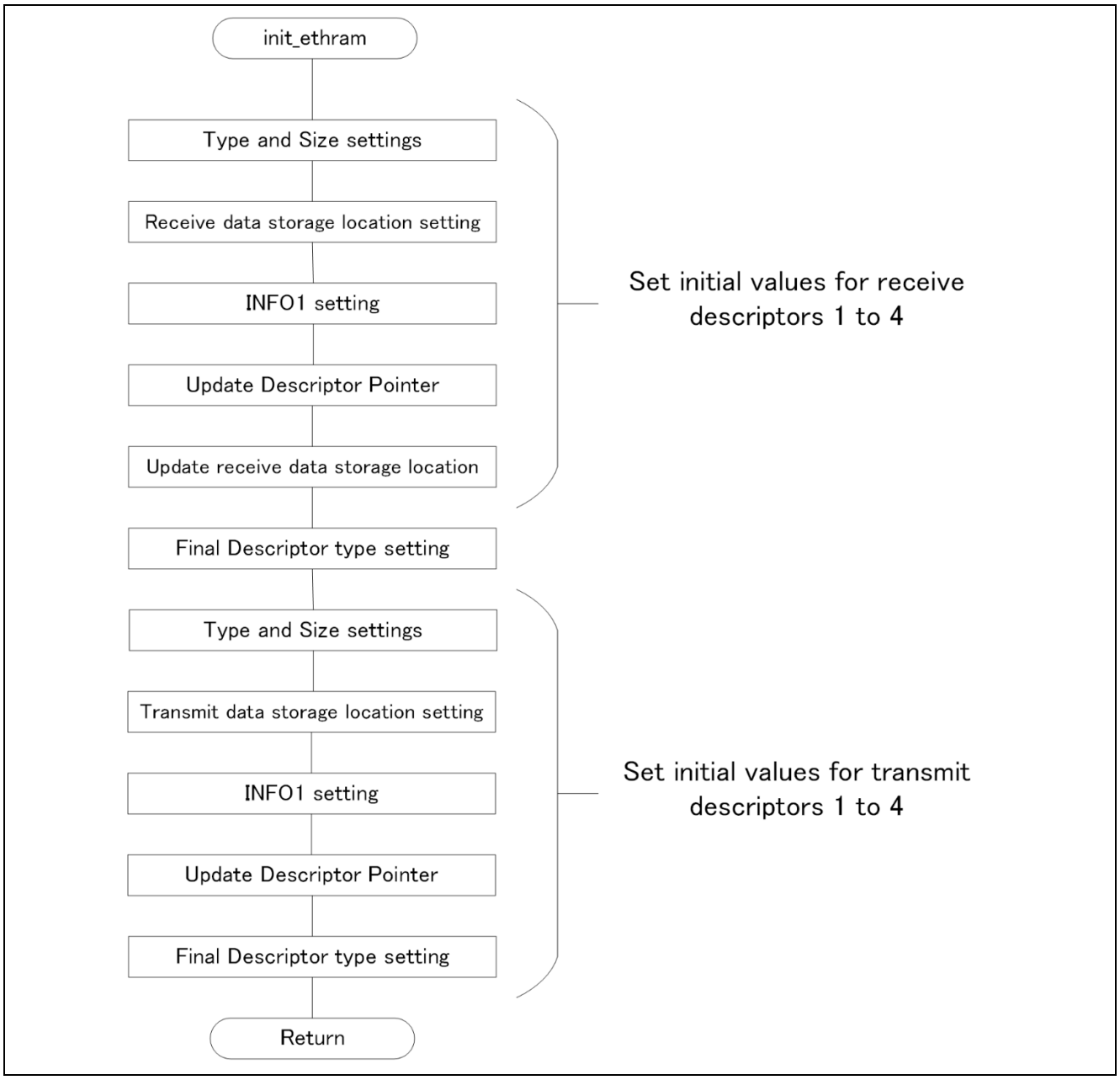

Figure 1-35 Descriptor initialization module flowchart

1.5.16 Data Transmission

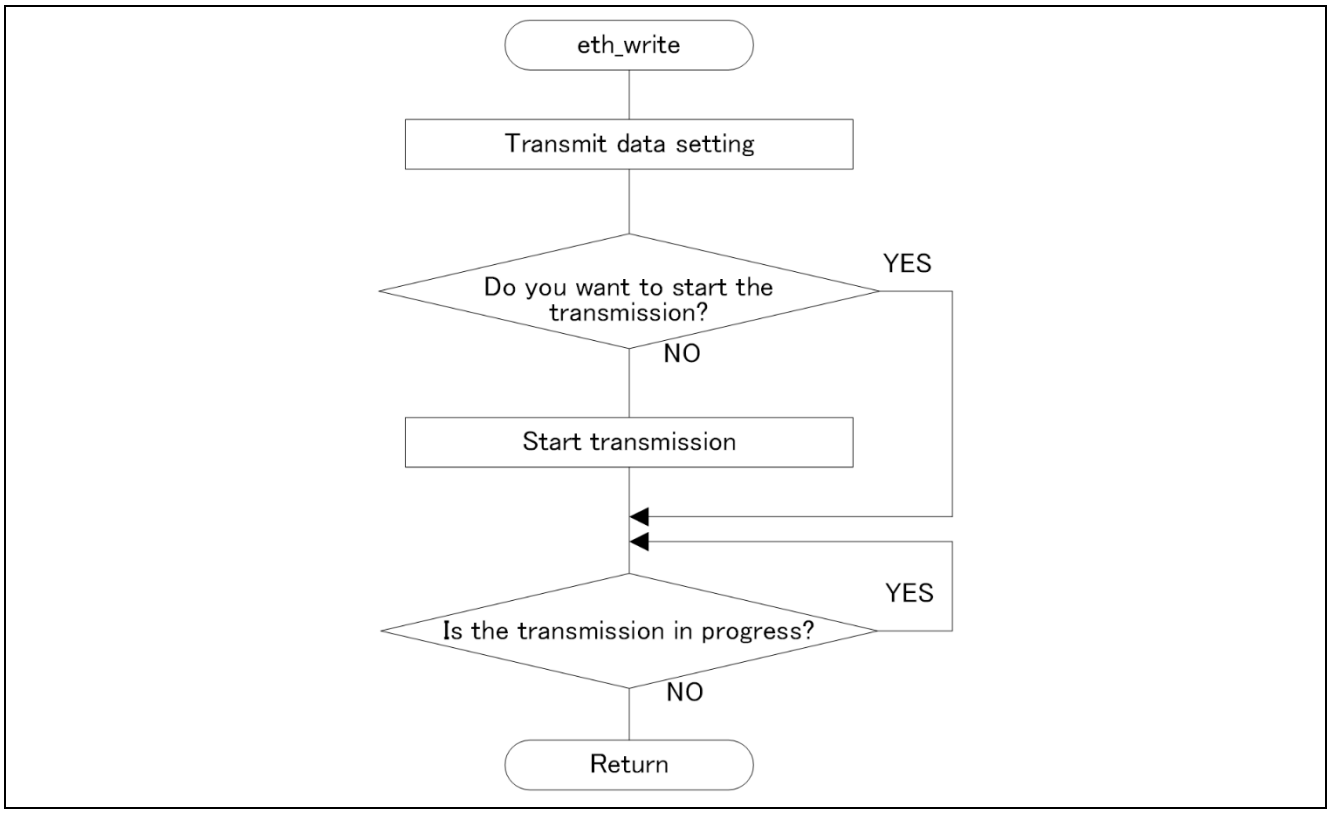

Figure 1-36 Data Transmission module flowchart

1.5.17 Receiving Data

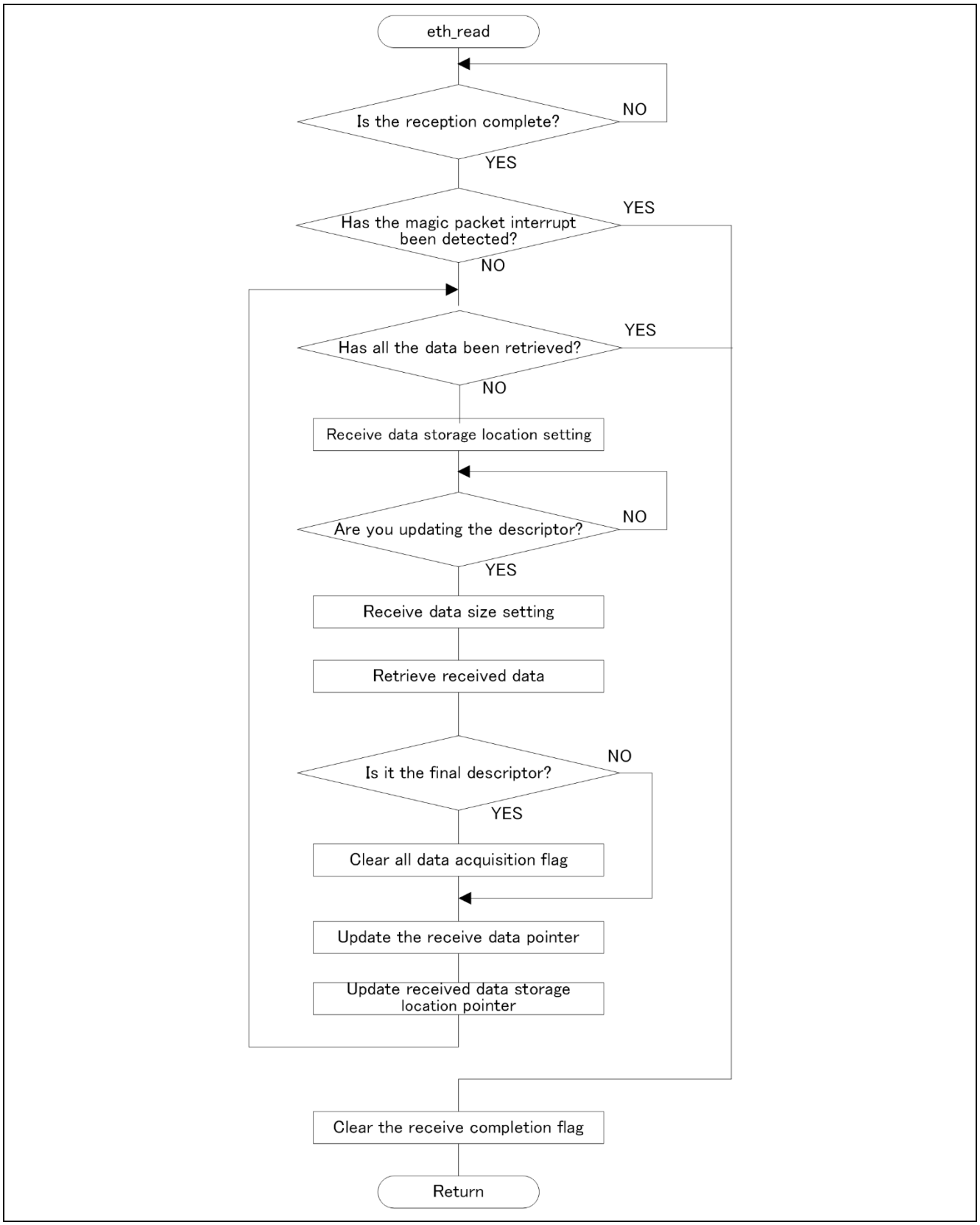

Figure 1-37 Data receiving module flowchart

1.5.18 Transmission Data Setting

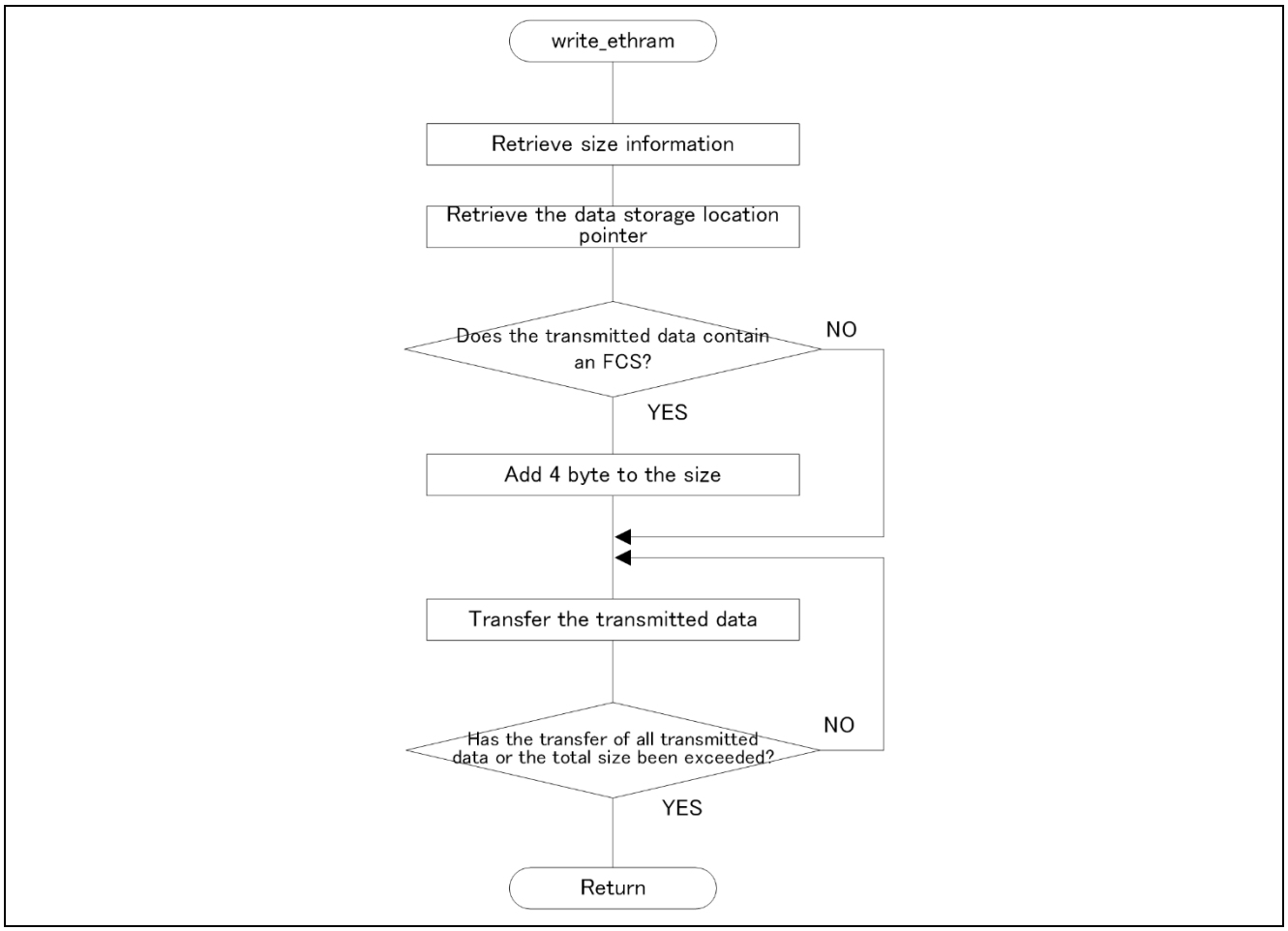

Figure 1-38 Transmission Data setting module flowchart

1.5.19 Retrieving Received Data

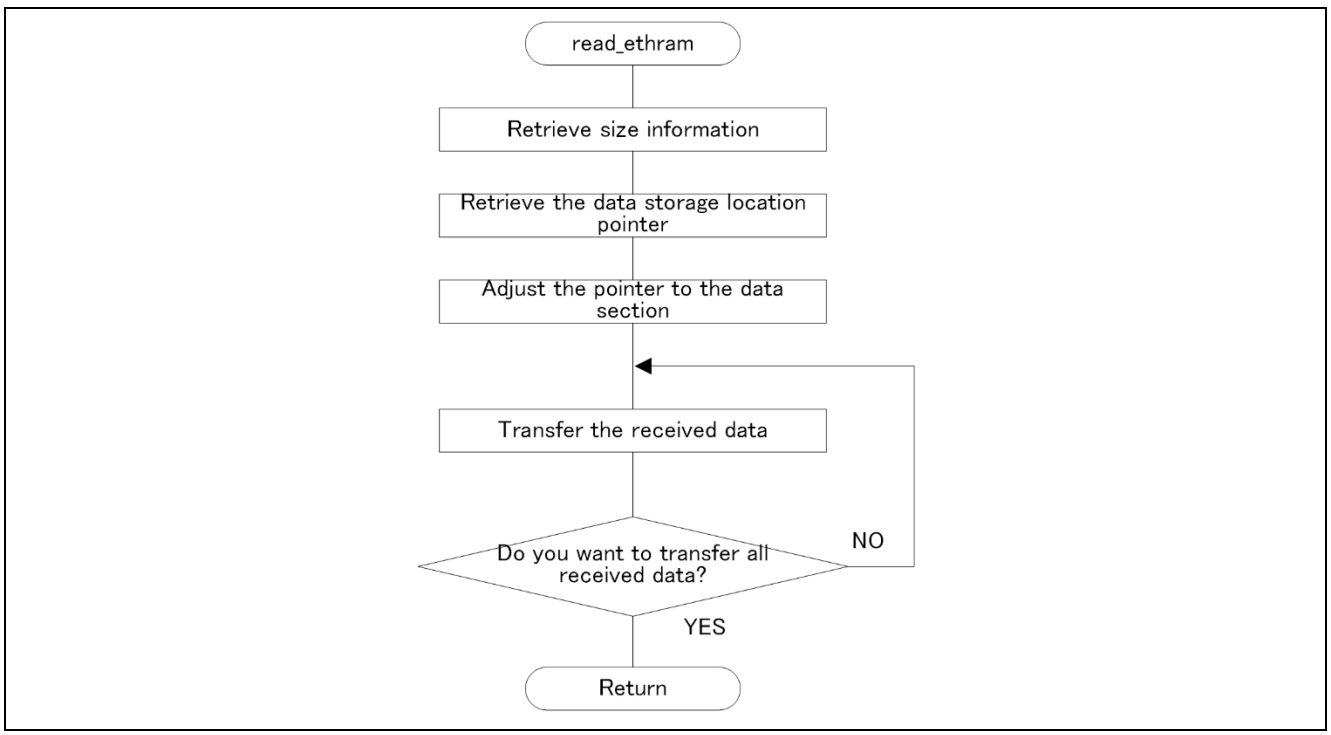

Figure 1-39 Flowchart of the Received Data Retrieval module

1.5.20 PHY Initialization

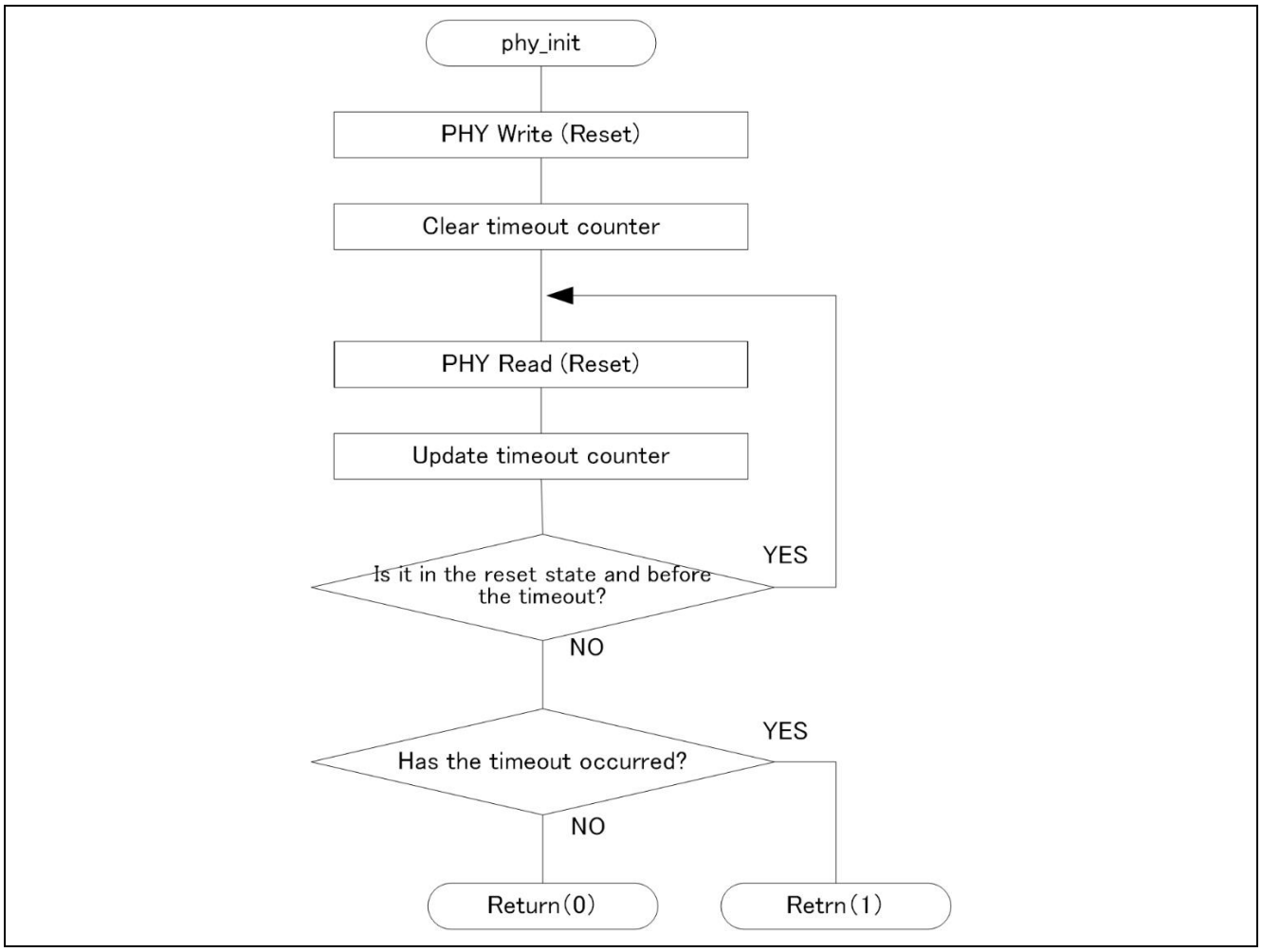

Figure 1-40 PHY Initialization module flowchart

1.5.21 Auto Negotiation

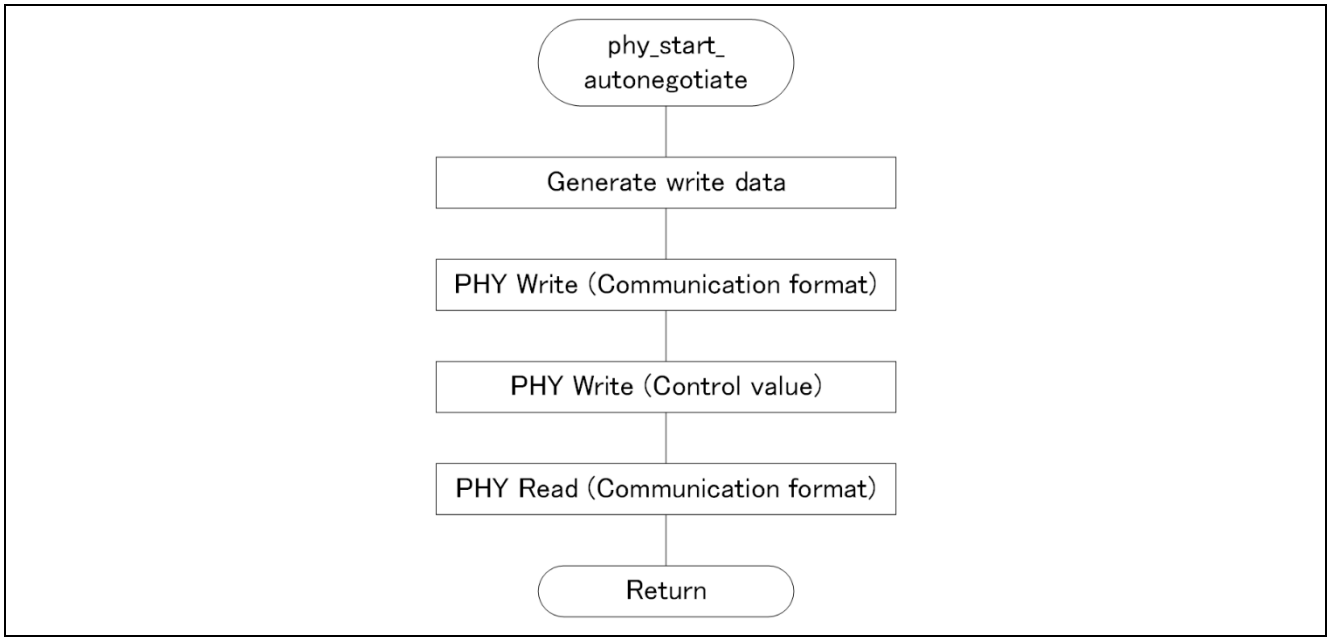

Figure 1-41 Auto Negotiation module flowchart

1.5.22 PHY Write

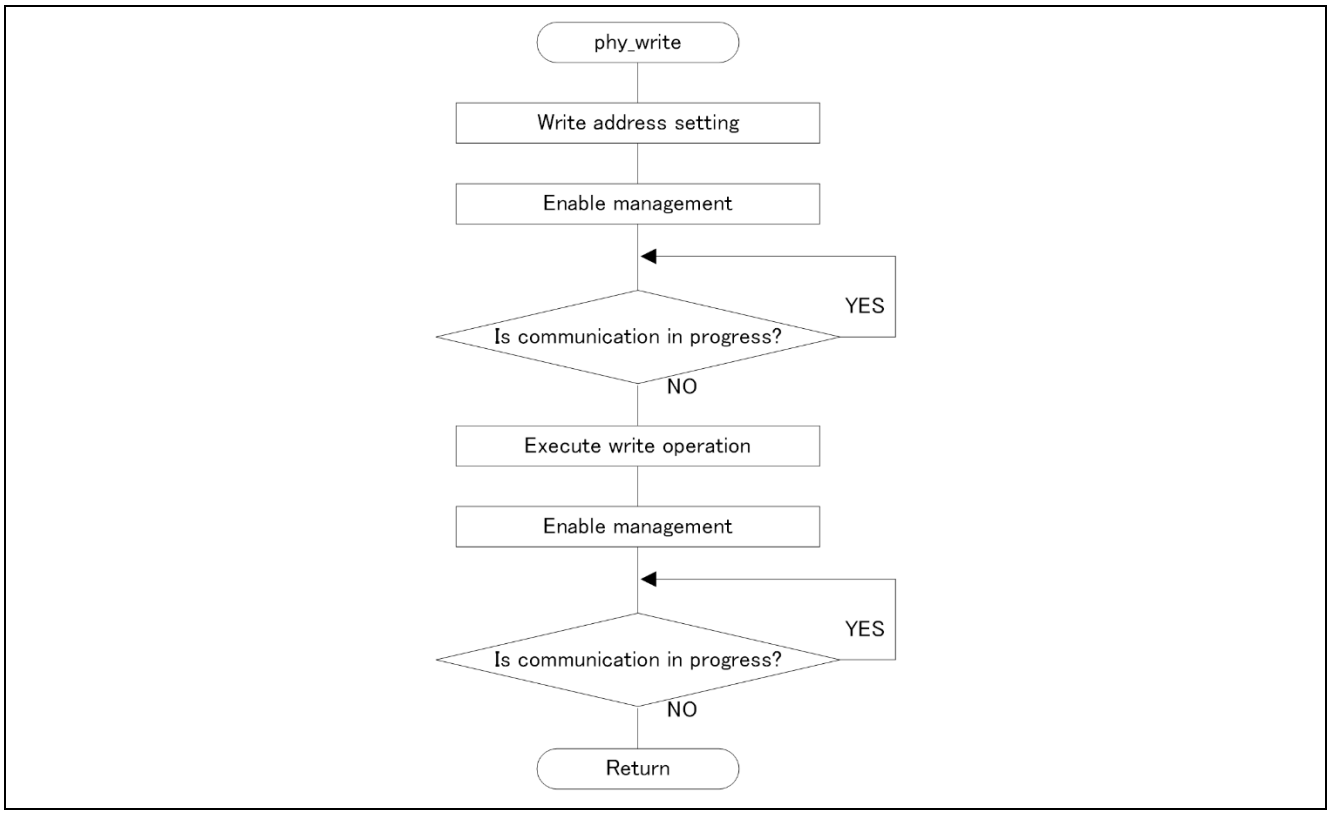

Figure 1-42 PHY Write module flowchart

1.5.23 PHY Read

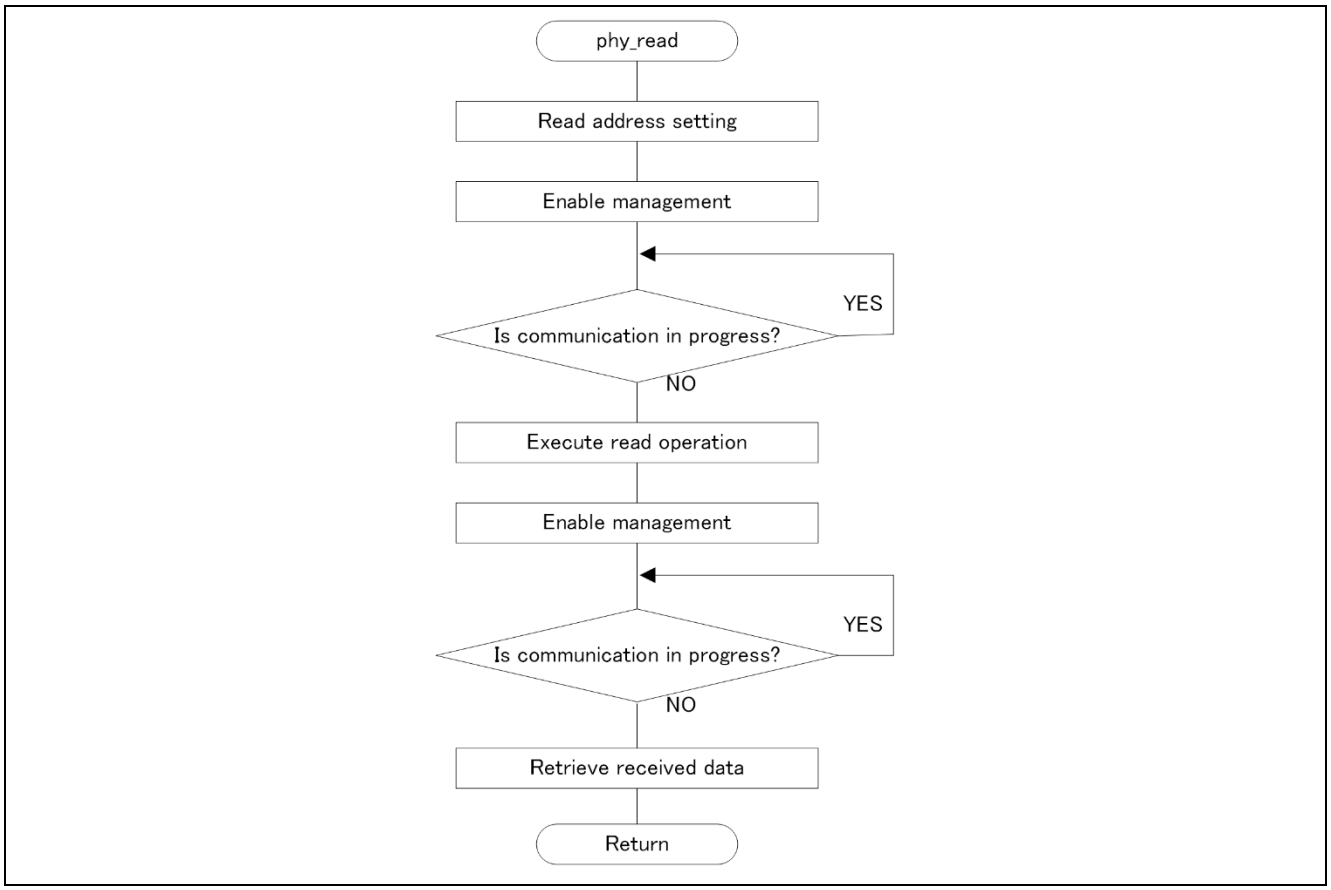

Figure 1-43 PHY Read module flowchart

2. Revision Record

Rev.	Issue date	Revised contents	
		Page	Points
1.00	March 16, 2025	Full page	First edition
1.10	January 28, 2026	1	Added RH850/U2C to target products

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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(Rev.5.0-1 October 2020)

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