RH850/U2B Group

Low-Power Operations Application Note

Introduction

To reduce the average current consumption and conserve energy, the RH850/U2B series provides a variety of different low-power options.

This document describes the hardware features implemented in the RH850/U2B devices as well as their usage in typical application scenario:

- Cyclic digital and analog signal polling (with port expansion)

The information in this document should be used in conjunction with the corresponding User's Manuals of the RH850/U2B series.

Target Device

This application note is intended to describe the Low-Power Operations on RH850/U2B series.

The RH850/U2B series has following variants:

RH850/U2B24-FCC	BGA468	R7F702Z23EDBG
		R7F702Z28EDBG
RH850/U2B10-FCC	BGA468	R7F702Z21EDBG
		R7F702Z26EDBG
	BGA373	R7F702Z21EDBA
		R7F702Z26EDBA
	BGA292	R7F702Z21EDBB
		R7F702Z26EDBB
RH850/U2B6-FCC	BGA292	R7F702Z22EDBB
RH850/U2B10	BGA468	R7F70254EFABG-C
		R7F70254FFABG-C
	BGA373	R7F70254AFABA-C
		R7F70254BFABA-C
	BGA292	R7F70254AFABB-C
		R7F70254BFABB-C
RH850/U2B6	BGA292	R7F702552FABB-C
		R7F702556FABB-C

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1. Background

The target of low-power operations is to reduce the (average) current consumption of the device in the related application scenarios.

Typical low-power application is

- Digital and analog port polling (with optional port expansion)

For this use case, the following functionalities are available:

- Support to stop or power-off certain peripherals when no active operation is required.
- CPU operation without Code Flash (Cyclic RUN mode and Cyclic STOP mode), including operation of all peripherals of the AWO area, as well as RLIN3 and MSPI located on the ISO area.
- Support the HW polling of digital and analog input signals and the comparison of the inputs with pre-configured thresholds.

This document introduces the related functions:

- Power supply, described in *Section 3*.
- Operation and chip standby modes, described in *Section 4*.
- Module standby mode, described in *Section 5*.
- Low-power sampler, described in *Section 6*.
- Typical use case of low-power application is presented in *Section 7*.

2. Reference Documents

This chapter contains information about the device reference documentation.

2.1 User's Manual

The Hardware User's Manual provides information about the functional and electrical behavior of the device.

At the release time of this document the following manual versions are available:

RH850/U2B Group User's Manual (Rev.1.00): R01UH0923EJ0100

3. Overview of power domains and power supply

The internal circuits of RH850/U2B series products are separated into two independent power domains:

- Always-On Area (AWO)
- Isolated Area (ISO)

These power domains are controlled by the power control located on the AWO Area. The AWO area itself remains powered in all operating modes.

The power supply of the Isolated area can be turned off to reduce the overall power consumption depending on the type of stand-by mode.

Dedicated on-chip voltage regulators generate the internal supply voltage for each power domain. The device RH850/U2B series includes the following voltage supplies:

- Power supply voltage SYSVCC for system logic and on-chip voltage regulators. The output voltage of the voltage regulators is supplied to the digital circuits in Always-On area power domain.
- Power supply voltage SVRDRVCC and SVRAVCC and SYSVCC for Switching Voltage Regulator (SVR).
- Power supply voltage ISOVDD for the digital circuits in Isolated area power domain. The ISO area power domain is supplied by an external power supply or SVR.
- Power supply voltage EnVCC for the I/O ports.
- Power supply voltage AnVCC and ADSVCC for the A/D converters and the separated I/O ports.
- Power supply voltage AFCVCC for the FCMP, RDC3AL and the separated I/O ports.
- Power supply voltage LVDVCC for the LVDS ports.
- Power supply voltages EMUVCC and EMUVDD for the Aurora ports.
- Power supply voltage GETH0PVCC, GETH0BVCC for the Ethernet.

3.1 Power Supply Pins

Table 3-1 lists all power supply pins and the related peripherals:

Table 3-1 Power Supply Pins

Power supply	Power Supply Pins	Power Supply for	Voltage Range
Power supply for internal circuits	SYSVCC	• Power supply for System Logic and Internal voltage regulator power and SVR power • Power supply terminal for PORTS	3.0 – 3.6 V 4.5 – 5.5 V
	VCC	Power supply for FLASH JP0x	
	J0VCC	RHSIF debug interface (RHSIFD)	3.0 – 3.6 V 4.5 – 5.5 V
	J1VCC	Reference clock for RHSIFD (HSIFD_REFCLK pin)	3.0 – 3.6 V 4.5 – 5.5 V
	OSCVCC	Power supply for OSC	3.0 – 3.6 V 4.5 – 5.5 V
	RAMSVCL	Stabilizing capacitance for Retention RAM	1.025 – 1.155 V
	SVRDRVCC (DRV_VCC)	Power supply for SVR	3.0 – 3.6 V
	SVRAVCC (AD_VCC)		4.5 – 5.5 V
	VDD	Power supply terminal for ISOVDD	1.025 – 1.155 V
	VSS	Common ground	–

	SVRAVSS (AD_VSS) SVRDRVSS (DRV_VSS)	Ground for SVR	–
	AWOVCL	External buffer capacitance of regulator Power supply terminal for ISOVDD	1.025 – 1.155 V
Power supply for I/O port	E0VCC	RESETOUT Port group Pxx_xx	3.0 – 3.6 V 4.5 – 5.5 V
	E1VCC	Port group Pxx_xx	
	E2VCC	Port groups Pxx_xx	
	VSS	Common ground	–
Power supply for A/D converters	A0VCC	Analog circuits of ADCK, Port group AN0xx	3.0 – 3.6 V 4.5 – 5.5 V
	A0VREFH		
	A0VSS		–
	A1VCC	Analog circuits of ADCK, Port group AN1xx	3.0 – 3.6 V 4.5 – 5.5 V
	A1VREFH		
	A1VSS		–
	A2VCC	Analog circuits of ADCK, Port group AN2xx	3.0 – 3.6 V 4.5 – 5.5 V
	A2VREFH		
	A2VSS		–
	A3VCC	Analog circuits of ADCK, Port group AN3xx	3.0 – 3.6 V 4.5 – 5.5 V
	A3VREFH		
	A3VSS		–
Power supply for Delta-Sigma and cyclic A/D converters	ADSVCC	Analog circuits of DSADC and CADC, Port group ADSVSS ANxx	3.0 – 3.6 V 4.5 – 5.5 V
	ADSVSS		–
Power supply for LVDS	LVDVCC	LVDS port	3.0 – 5.5 V
	VSS	Common ground	–
Power Supply for Fast comparator and RDC3AL	AFCVCC	FCMP RDC3AL	3.0 – 3.6 V 4.5 – 5.5 V
	AFCVSS		–
Power supply for Ethernet	GETH0PVCC	Power supply for Ethernet domain	• 3.14 – 3.46 V (w/ SGMII) • 3.0 – 3.6 V (w/o SGMII) • 4.5 – 5.5 V (w/o SGMII)
	GETH0BVCC		• 3.14 – 3.46 V (w/ SGMII) • – [*1] (w/o SGMII)
	GETH0VCL (SGVCL)		1.025 – 1.155 V
	GETH1VCL		1.025 – 1.155 V
	VSS	Common ground	–
Power supply for EMU	EMUVCC	Debug circuits	3.0 – 3.6 V
	EMUVDD	Debug circuits of EMU(Aurora)	• 1.04 – 1.14 V (Aurora ON)

		ERAM circuits of FLASH	• 1.025 – 1.155 V (Aurora OFF)
	VSS		–

Notes: 1. Typically input 3.0 – 3.6 V voltage or connect to VSS with ≥1kΩ pull-down resistance.

3.2 Power Domains Arrangement

Table 3-2 shows the functional distribution of the Power Domains:

Table 3-2 Functional Modules and Power Domain

Power Domain	Functions
AWO Area	• STBC, Reset controller • Retention RAM • CLMA0, CLMA1, CLMA2 • Main OSC, LS IntOSC, HS IntOSC • WDTBA, RTCA, TAUJ2, TAUJ3, ADCKA • LPS • AWO Port groups
ISO Area	• CPU subsystem, DFP • Code flash, Data flash, Local RAM, Cluster RAM • PLL, SGMII_PLL, HSIFPLL, SSCG, SSCG1 • CLMA3, CLMA4, CLMA5, CLMA6, CLMA7, CLMA8, CLMA9, CLMA10, CLMA12, CLMA13, CLMA14, CLMA15 • WDTB0, WDTB1, WDTB2, WDTB3, WDTB4, WDTB5 • RHSIF, TPBA, GTM • TAUD, OSTM, RS-CANFD, RLIN3, RIIC, LTSC • ADCK0, ADCK1, ADCK2, ADCK3, TAPA, TSG3, ATU6, ENCA, SFMA, FLXA, ETN, RSENT, MMCA • DSADC, CADC, DSMIF • RHSB, DFE, HRPWM, EMU3S • FCMP, RDC3AL/AS • SWDT, ICUM, ACEU • PSI5, PSI5-S • MSPI, PIC, KCRC, OTS, ECM • ISO Port groups • DMON

4. Operation and Chip Standby Modes

The standby controller of RH850/U2B series products support 2 standby modes:

- Chip Standby mode
- Module Standby mode

In this section, a general description about the chip-level low power operations is provided. For module standby modes, please refer to *Section 5 'Module Standby Mode'* in this document.

The RH850/U2B series support the following operation modes:

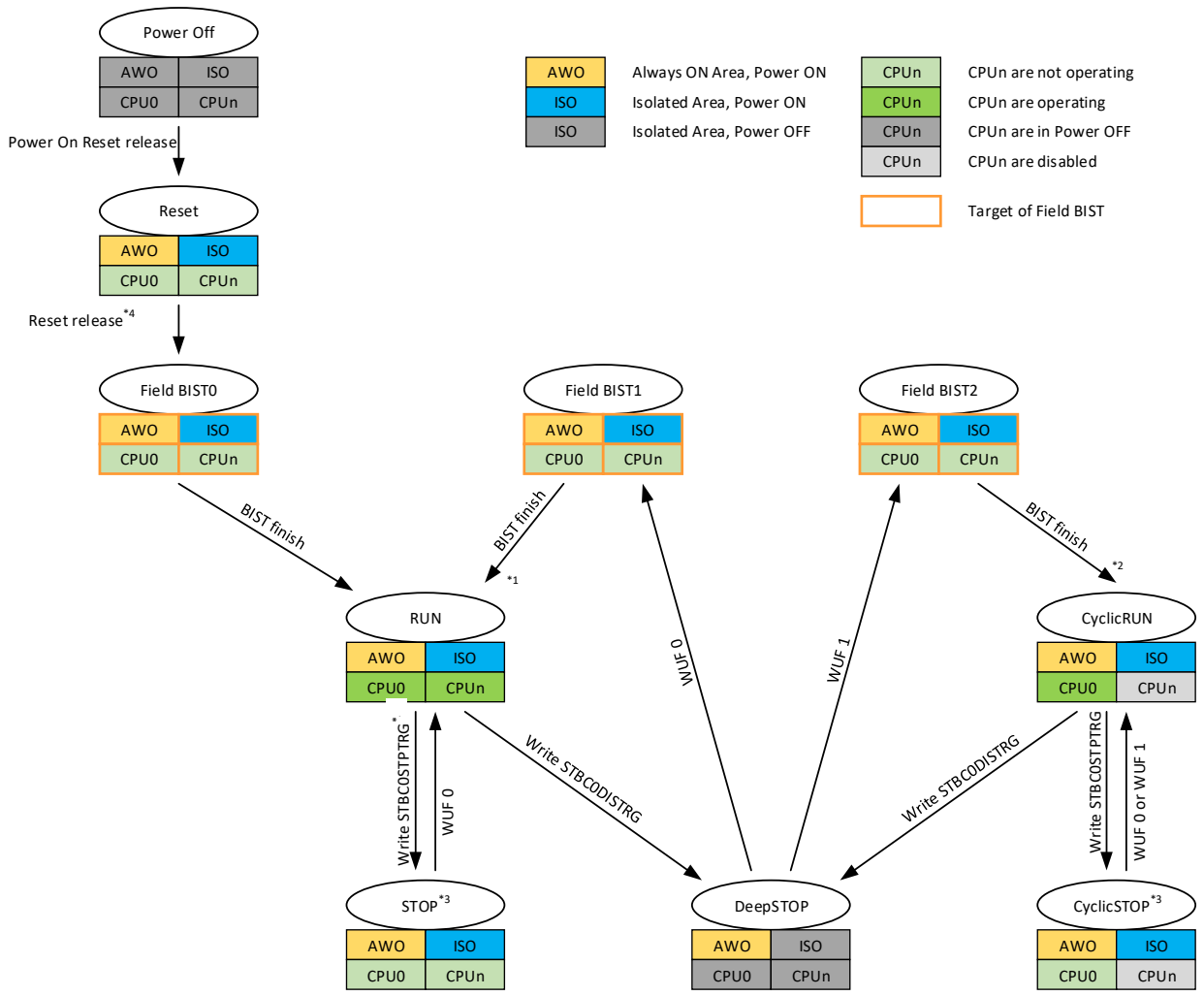
- RUN mode
- STOP mode
- DeepSTOP mode
- Cyclic RUN mode
- Cyclic STOP mode
- Power Off Standby mode

4.1 Overview

The chip-level low-power modes includes STOP mode, DeepSTOP mode and Cyclic operation (Cyclic RUN mode and Cyclic STOP mode).

Transition to chip standby mode should be performed by CPU0(PE0), when CPU0(PE0) shifts to chip standby mode, CPUn(PEn) will also shift to chip standby mode.

Figure 4-1 shows the state transition of operation modes.



Notes: 1. To return from DeepSTOP to RUN, ISO peripheral function registers must be set again. CPU0(PE0)/CPUn(PEn) start the operation from the reset address on the code flash.
2. The CPU0 starts the operation from the reset address on the retention RAM.
3. CPU and bus clocks are stopped at STOP mode/Cyclic STOP mode.
4. The Field BIST0 is executed before transition to RUN mode after Power On Reset and System Reset 1/2.

Figure 4-1 Transition to Chip Standby Modes

Table 4-1 lists the definition and mode transition trigger of the operation modes:

Table 4-1 List of Operation Modes

Operation Mode	Definition	Mode Transition Trigger
RUN[*1]	Normal operation mode, all functions are operational	-
STOP	Chip-level standby mode, the clock supplies to certain clock domain can be stopped	STBC0STPT.STBC0STPTRG
DeepSTOP	Chip-level standby mode to reduce power consumption further than STOP mode, clock supplies are stopped and the power supply to ISO area is switched off	STBC0PSC.STBC0DISTRG
Cyclic RUN	Low-power operation mode, limited peripherals can operate at low speed. The CPUn(PEn)[*2] is not available.CPU0 executes the instructions from the retention RAM.	• Wake-up factor 1 (from DeepSTOP mode) • Wake-up factor 0/1 (from Cyclic STOP mode)
Cyclic STOP	STOP mode in cyclic operation, CPU0 halts its operation	STBC0STPT.STBC0STPTRG
Power Off Standby	Only RAM retention is possible in this mode. Low leakage is realized by turning off the power outside of the MCU and by stopping oscillators.	Asserting the external reset pin and turning off the power except SYSVCC

Notes: 1. RUN mode is not discussed in this application note.
2. n!=0

In transition of operation modes, the Build-In-Self-Test (BIST) can be executed during DeepSTOP Reset. For detailed information please refer to *Section 4.6 BIST Execution*.

4.2 Clock Supply in Chip Standby Mode

4.2.1 Clock Oscillators

In chip standby mode (STOP mode, DeepSTOP mode, and Cyclic STOP mode), the LS IntOSC continues operation. Main OSC, HS IntOSC and PLL can be set to stop or continue via <name>STPM registers.

HV IntOSC continues in STOP and Cyclic modes and can be set stopped or continue via the VMONDSCR register in DeepSTOP mode.

Table 4-2 lists the operation of clock oscillators in standby modes.

Table 4-2 Operation of Clock Oscillators in Standby Modes

Oscillators	STOP mode	DeepSTOP mode	Cyclic STOP	Cyclic RUN
Main OSC	• For bit MOSCSTPM.MOSCSTPMSK = 0, oscillation is stopped • For bit MOSCSTPM.MOSCSTPMSK = 1, oscillation continues			Oscillation continues
LS IntOSC	Oscillation continues*1			
HS IntOSC	• For bit HSOSCSTPM.HSOSCSTPMSK = 0, oscillation is stopped • For bit HSOSCSTPM.HSOSCSTPMSK = 1, oscillation continues			Oscillation continues
PLL	Oscillation continues when bit MOSCSTPM.MOSCSTPMSK = 1 and PLLSTPM.PLLSTPMSK = 1*2	Disabled*3	Not available in cyclic operation	
HV IntOSC*4	Oscillation continues	• For bit VMONDSCR.DSDETEN = 0, oscillation is stopped • For bit VMONDSCR.DSDETEN = 1, oscillation continues	Oscillation continues	

Notes: 1. After power supply the LS IntOSC starts operation. It cannot be stopped.

2. For detailed information, please refer to the device User's Manual R01UH0923EJ0100 *Section 15.4.5 'Phase Locked Loop (PLL)'*.

3. PLL is disabled in DeepSTOP mode, a software restart is necessary to start the PLL after transition from DeepSTOP mode to RUN mode.

4. Only used for VMON, the general operation of this oscillator in chip standby mode is described in *Section 4.3.2 'DeepSTOP Mode'*. Further information is not provided in this application note.

4.2.2 System and Peripheral Clock

The following CPU subsystem clocks are stopped in chip standby modes (STOP mode, DeepSTOP mode and Cyclic STOP mode):

- CPU clock CLK_CPU
- SBUS clock CLK_SBUS
- HBUS clock CLK_HBUS

Regarding to peripherals, the clock stop mask bits MSR_<name>.STPMSK_<name> are used to determine the operation status of the clock in chip standby mode:

- If the stop mask bit is set to 0, the stop request is not masked, the related peripheral clock stops during chip standby mode.
  If the clock is in operation before entering standby mode, the clock restarts automatically after wake-up of chip standby mode.
- If the stop mask bit is set to 1, the stop request is masked, the corresponding peripheral clock continues operate during chip standby mode.
  The clock supply of ISO area is stopped in DeepSTOP mode.

Table 5-1 in *Section 5.2 'Module Standby Registers'* includes the information about the peripheral clock supplies which can be set continue using MSR_<name> registers in standby modes.

Section 5.3 provides the information of the clock supply to peripherals in each operation mode and chip standby mode.

4.3 Chip Standby Modes

4.3.1 STOP Mode

In STOP mode, the clock supply to the CPU core and the CPU subsystem is stopped.

The low speed internal oscillator CLK_LSIOSC and high voltage internal oscillator CLK_HSIOSC can operate.

Main oscillator CLK_MOSC, high speed internal oscillator CLK_HSIOSC and PLL are stopped in default settings, these clock sources can be configured to continue operating by masking stop request.

In addition, basically all peripheral functions are stopped before the transition to STOP mode is made. Only a limited number of peripherals may remain operable on the available clock sources.

The contents of Local RAM and Retention RAM before the transition to STOP mode are remained.

The I/O buffers remain their state before entering STOP mode.

(1) Preparation for STOP Mode

Before starting STOP mode, the following setup is needed as the preparation for standby:

- Stop Delay Monitor (DMON).
- Stop Clock Monitor (CLMA). (if the monitor clock would be stopped.)
- Stop all the peripheral functions whose clock supply will be stopped.
- Disable the interrupt handling by the CPU instruction “DI”.
- Set the interrupt control registers.
  - Clear the interrupt flag (EICn.EIRFn = 0).
  - Mask the interrupts for non-wake-up factors (EICn.EIMKn= 1).
  - Release the masks of the interrupts for wake-up factors (EICn.EIMKn = 0).
- Set the wake-up related registers.
  - Clear the wake-up factor flags (the WUFC0_Ax / WUFC0_Iy registers, x = 0 to 2, y = 0 to 3).
  - Mask the non-wake-up factor (the WUFMSK0_Ax / WUFMSK0_Iy registers, x = 0 to 2, y = 0 to 3).
  - Release the masks of the wake-up factors (the WUFMSK0_Ax / WUFMSK0_Iy registers, x = 0 to 2, y = 0 to 3).
- Set the clock stop mask register to select the clock domains to be stopped and the ones to continue operating (using the MSR__<name>.STPMSK_<name> bit).
- Specify whether to oscillate or stop each clock source. In addition, set the clock stop mask register to select the clock sources to be stopped and the ones to continue operating (using the MOSCSTPMSK bit in the MOSCSTPM register and the HSOSCSTPMSK bit in the HSOSCSTPM register and the PLLSTPMSK bit in the PLLSTPM register).

(2) Start of STOP Mode

According to Figure 4-1 and Table 4-1, setting the STBC0STPTRG bit of register STBC0STPT to 1, the device is shifted into STOP mode.

For the detailed information for the operation status of different modules in STOP mode, please refer to Table 4-3.

(3) End of STOP Mode

The device can return to RUN mode from STOP mode when a wake-up event is generated as configured in the corresponding WUF0_Ax or WUF0_Iy (x = 0 to 2, y = 0 to 3) registers.

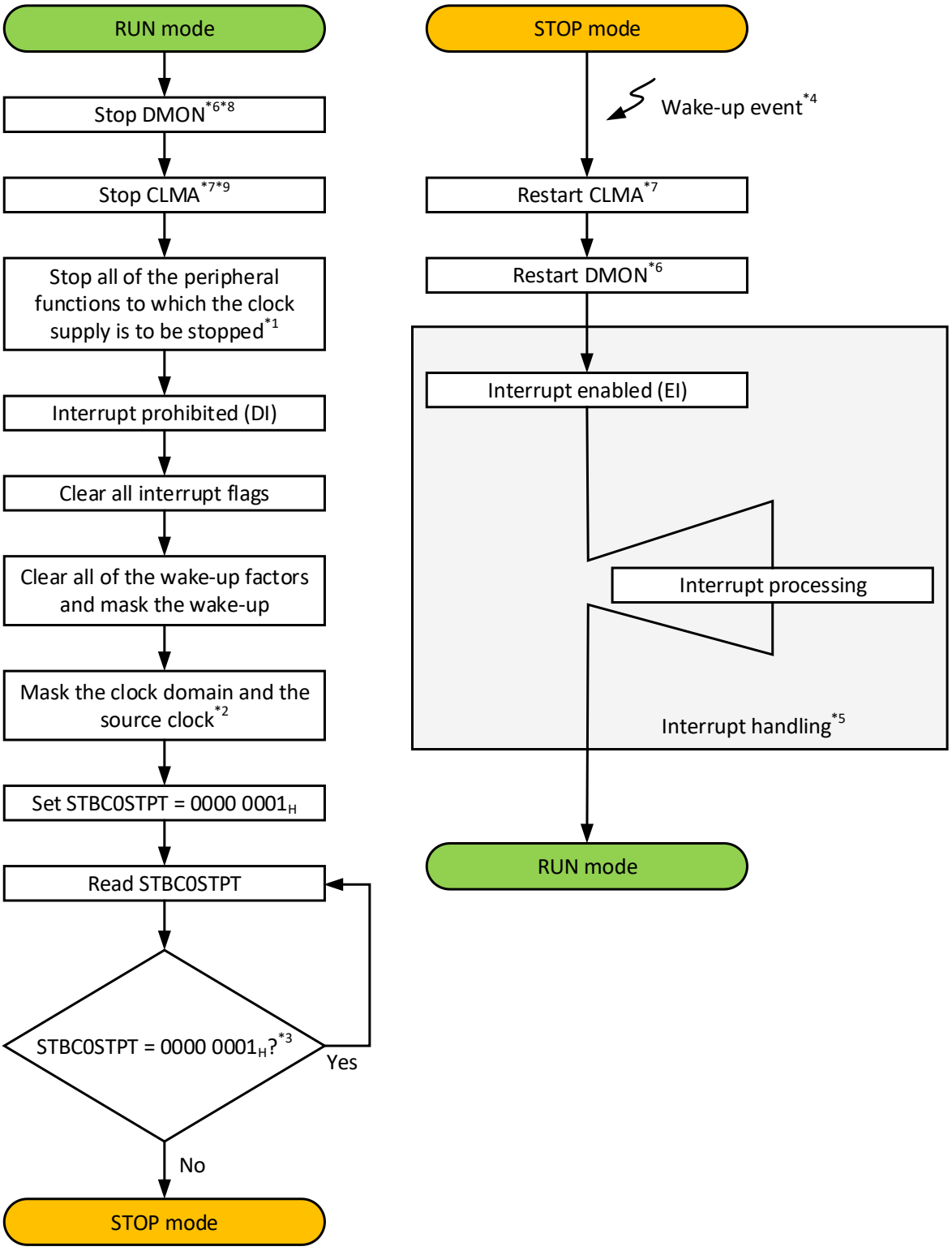
(4) Wake-up Handling

The generation of wake-up events can be determined by the wake-up factor flags WUF0_Ax or WUF0_Iy (x = 0 to 2, y = 0 to 3).

When an interrupt is enabled by the CPU instruction “EI”, the corresponding wake-up interrupt will be executed.

(5) Transition Procedure to STOP Mode

The transition procedure (example) to STOP mode is shown below in Figure 4-2.



Notes: 1. Before the transition to STOP mode, all the peripheral functions whose clock supply will be stopped, must be turned off. Otherwise the operation of the peripheral function may be incorrect.
2. The clock mask must be set before 0000 0001H is written to STBC0STPT.
3. STBC0STPT.STBC0STPTRG bit is cleared automaticlly after transition to STOP mode.
The clock supply to the CPU is stopped and the operation shifts to the STOP mode while checking that STBC0STPT = 0000 0001H.

4. STBC0STPT is set to 0000 0000_H at the generation of a wake-up event. The generated wake-up factor can be checked by the WUF0_Ax and WUF0_Iy (x = 0 to 2, y = 0 to 3) registers.
5. This processing is optional. It is required to execute the interrupt handling after the wake-up.
6. For details please refer to HW user's Manual R01UH0923EJ0100 *Section 13.4.7.4 'Procedures to Reset DMON*.
7. For details please refer to HW user's Manual R01UH0923EJ0100 *Section 16.6.2 'Procedures to Reset by CLMATEST.RESCLM*.
8. Stop DMON when Main OSC stops at chip standby mode.

Figure 4-2 Example of STOP mode transition

(6) Operation Status of STOP Mode

For the detailed information for the operation status of CPUs and peripherals during STOP mode, please refer to *Section 4.3.2* Table 4-3.

4.3.2 DeepSTOP Mode

In DEEPSTOP mode, the power supply to the Isolated Area is turned off.

The low speed internal oscillator LS IntOSC continues.

PLL is automatically disabled during transition to DeepSTOP mode.

Main oscillator Main OSC and high speed internal oscillator HS IntOSC are stopped in default settings, these clock sources can be configured to continue operating by masking stop request.

The high voltage internal oscillator HV IntOSC can be automatically disabled, depends on the configuration in the VMON DeepSTOP control register VMONDSCR.

For peripherals in Always-On Area that continue operation in DeepSTOP, the clock supply can be continued by setting the clock stop mask register.

The I/O buffers in DeepSTOP mode are changing into I/O buffer hold state by default, meaning the state of the buffers is frozen. The input or output remains in the state before entering DeepSTOP mode, no external or internal signal can change its state until the I/O buffer hold state is terminated after wake-up from DeepSTOP.

(1) Preparation for DeepSTOP Mode

Before starting DeepSTOP mode, the following setup is needed as the preparation for standby:

- Stop DMON.
- Stop CLMA (if the monitor clock would be stopped).
- Stop all the peripheral functions to which the clock supply is to be stopped.
- Disable the interrupt handling by the CPU instruction “DI”.
- Set the interrupt control registers.
  - Clear the interrupt flag (EIC.EIRFn = 0).
  - Mask the interrupts for non-wake-up factors (EIC.EIMKn = 1).
  - Release the masks of the interrupts for wake-up factors (EIC.EIMKn = 0).
- Set the wake-up related registers.
  - Clear the wake-up factor flags (the WUFCn_Ax / WUFCn_Iy registers, n = 0 or 1, x = 0 to 2, y = 0 to 3).
  - Mask the non-wake-up factor (the WUFMSKn_Ax / WUFMSKn_Iy registers, n = 0 or 1, x = 0 to 2, y = 0 to 3).
  - Release the masks of the wake-up factors (the WUFMSKn_Ax / WUFMSKn_Iy registers, n = 0 or 1, x = 0 to 2, y = 0 to 3).
- Set the clock stop mask register to select the clock domains to be stopped and the ones to continue operating (using the MSR__<name>.STPMSK_<name> bit).
- Specify whether to oscillate or stop each clock source. In addition, set the clock stop mask register to select the clock sources to be stopped and the ones to continue operating (using the MOSCSTPMSK bit in the MOSCSTPM register and the HSOSCSTPMSK bit in the HSOSCSTPM register).

(2) Start of DeepSTOP Mode

According to Figure 4-1, if the STBC0PSC.STBC0DISTRG bit is set to 1, the device starts DeepSTOP mode.

(3) End of DeepSTOP Mode

When a wake-up factor is generated, the microcontroller returns from DeepSTOP mode.

By releasing DeepSTOP mode, the Build-In-Self-Test (BIST) might be executed, for detailed BIST execution condition, please refer to *Section 4.5 BIST Execution*.

(4) Wake-up Handling

- If the device returns from DeepSTOP mode due to wake-up factor 0:
  - The device switches to RUN mode, the operation starts from the reset vector address.

    If one of the FENMI or FEINT interrupts has been generated before recovery from DeepSTOP mode to RUN mode, the microcontroller restarts operation from operation from exception handler address:

  - FENMI: FENMI handler address ($E0_H$)
  - FEINT: FEINT handler address ($F0_H$)

  The general-purpose registers and local RAM are undefined after return from DeepSTOP mode.

- If the device returns from DeepSTOP mode due to wake-up factor 1:

  — The device switches to Cyclic RUN mode, the CPU0 starts the operation from the reset address on the retention RAM.
  If one of the FENMI or FEINT interrupts has been generated before recovery from DeepSTOP mode to Cyclic RUN mode, the microcontroller restart operation from the exception handler address:
  - FENMI: FENMI handler address ($FE80\ 0000_H + E0_H$)
  - FEINT: FEINT handler address ($FE80\ 0000_H + F0_H$)

- The generation of the wake-up factors can be determined by the wake-up factor flags WUFn_Ax (n = 0 or 1, x = 0 to 2).

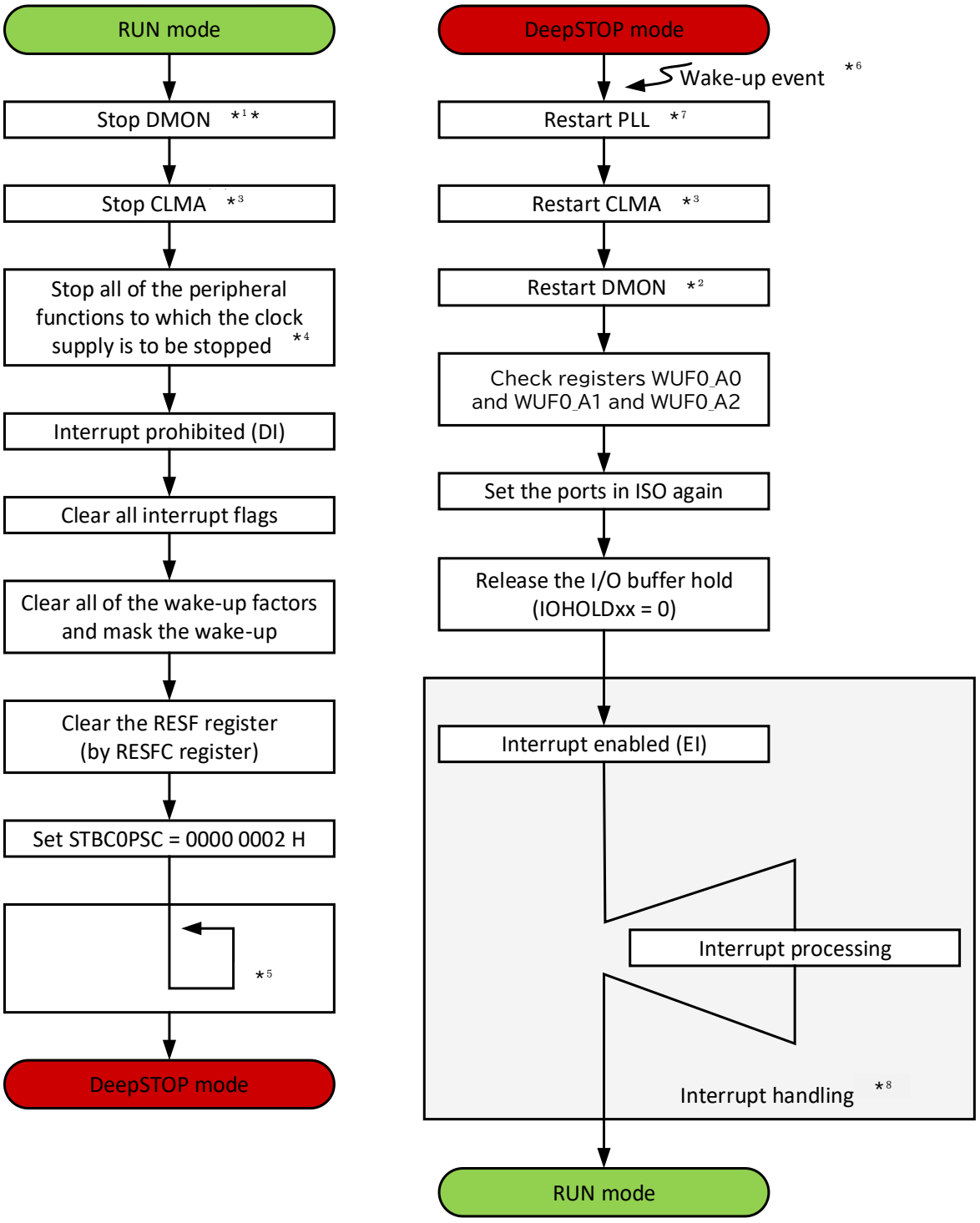
- The ports in the Isolated area maintain the I/O buffer hold state.

  Release the I/O buffer hold state by executing the following steps:
  1. Re-configure the peripheral functions and port functions.
  2. Set IOHOLDn.IOHOLD_xxx = 0. (n=0, 1)

- To execute an interrupt of the wake-up factor after the wake-up, evaluate the information of wakeup factor flag by software and set the interrupt request flag in the interrupt control register. Then, when an interrupt is enabled by the CPU instruction “EI”, the generated wake-up interrupt will be executed.

(5) Transition Procedure to DeepSTOP Mode

Figure 4-3 shows a general example of the transition procedure to enter and leave the DeepSTOP mode.



Notes: 1. Stop DMON when Main OSC stops at chip standby mode.
2. For details please refer to HW user's Manual R01UH0923EJ0100 *Section 13.4.7.4 'Procedures to Reset DMON*.
3. For details please refer to HW user's Manual R01UH0923EJ0100 *Section 16.6.2 'Procedures to Reset by CLMATEST.RESCLM'*.
4. When the operation of the peripheral function is stopped during operating due to the transition to the DeepSTOP mode, the operation of the peripheral function may be incorrect. Therefore, before the transition to the DeepSTOP mode, stop all of the peripheral functions whose clock supply is to be cut off.

5. After setting STBC0PSC = 0000 0002$_H$, wait for the transition to the DeepSTOP mode by the unconditional loop.
6. The CPU starts the program from the reset vector after the generation of a wake-up event. The return from the DeepSTOP mode by a reset can be checked by the RESF register. In addition, the generated wake-up event can be checked by the WUF0_A0, WUF0_A1 and WUF_A2 registers.
7. A software PLL restart is necessary, if PLL is requied after transition to RUN mode.
8. This processing is optional. It is required to execute the interrupt handling after the wake-up.

Figure 4-3 Example of DeepSTOP mode transition

(6) Operation Status of DeepSTOP Mode

For the detailed information for the operation status of CPUs and peripherals during DeepSTOP mode, please refer to Table 4-3.

Table 4-3 Operation statuses of STOP and DeepSTOP modes

Function			STOP Mode	DeepSTOP Mode
Port	AWO		Stop	Operable
	ISO		Stop	Stop
CPU			Stop	Stop
LPS			Operable	Operable
EXTCLK			Operable	Operable
Peripheral Interconnect (PIC)			Stop	Stop
DFP			Stop	Stop
Mortor Control IP	EMU		Stop	Stop
	RDC		Stop	Stop
DSMIF			Stop	Stop
Flash	Code Flash		Stop	Stop
	Data Flash		Stop	Stop
RAM	Local RAM		Stop	Stop
	Cluster RAM		Stop	Stop
	Retention RAM		Stop	Operable
Timer	Operating System Timer (OSTM)		Stop	Stop
	Window Watchdog Timer	WDTBA	Operable	Operable
		WDTB0 to 5, SWDTA	Stop	Stop
	Timer Array Unit D (TAUD)		Stop	Stop
	Timer Array Unit J	TAUJ2, TAUJ3	Operable	Operable
	Long-Term System Counter (LTSC)		Stop	Stop
	Generic Timer Module (GTM)		Stop	Stop
	ATU		Stop	Stop
	Real-time Counter (RTCA)		Operable	Operable
	Motor Control Timer (TSG3)		Stop	Stop
	Timer Option (TAPA)		Stop	Stop
	Timer Pattern Buffer (TABA)		Stop	Stop

	Encoder Timer (ENCA)		Stop	Stop
	High-Resolution PWM (HRPWM)		Stop	Stop
Communication	RLIN3		Operable	Stop
	Multichannel Serial Peripheral Interface (MSPI)		Stop	Stop
	Renesas High-Speed Serial I/F (RHSIF)		Stop	Stop
	I2C Interface (RIIC)		Stop	Stop
	CAN Interface (RS-CANFD)		Operable	Stop
	FlexRay (FLXA)		Stop	Stop
	Renesas High Speed Bus (RHSB)		Stop	Stop
	Ethernet (ETN)		Stop	Stop
	Single Edge Nibble Transmission (RSENT)		Stop	Stop
	PSI5		Stop	Stop
	PSI5S		Stop	Stop
	Multimedia Card Interface (MMCA)		Stop	Stop
	Serial Flash Memory Interface A (SFMA)		Stop	Stop
Safety	Clock Monitor	CLMA0 to 2	Stop	Operable
		CLMA3 to 15	Stop	Stop
	Voltage Monitor (VMON)		Stop	Stop
	OTS		Stop	Stop
	Data CRC Function K (KCRC)		Stop	Stop
	Error Control Module (ECM)		Operable*	Stop
A/D Converter	SAR-ADCA		Operable	Operable
	SAR-ADC0~3		Stop	Stop
	DS-ADC/CADC		Stop	Stop
	FCOMP		Stop	Stop
Digital Filter	DFE		Stop	Stop
Security	ICUMHA		Stop	Stop

Note: ECM delay timer clock (CLK_ECMCNT) stops.

4.3.3 Cyclic RUN Mode

Cyclic RUN mode is very similar to the ‘normal’ RUN mode, except the fact that:

- PLL and Flash memory are not available.
- The CPU0 fetches the instruction from the Retention RAM (Standby RAM), the CPUn (n!=0) are not available.
- Only a limited number of peripherals (RLIN3, MSPI and AWO peripherals) can be active.

(1) Preparation for Cyclic RUN Mode

Before the transition to Cyclic RUN mode, the following preparation is necessary:

- Stop DMON and CLMA if Main OSC is stopped in STOP mode.
- Arrange the program for Cyclic RUN in the Retention RAM.
- Set the wake-up related registers:
  - Clear the wake-up factor flags (the WUFC1_Ax/WUFC1_Iy register, x = 0 to 2, y = 0 to 3).
  - Mask the non-wake-up factor (the WUFMSK1_Ax/WUFMSK1_Iy register, x = 0 to 2, y = 0 to 3).
  - Release the masks of the wake-up factor (the WUFMSK1_Ax/WUFMSK1_Iy register, x = 0 to 2, y = 0 to 3).
- Make the transition to DeepSTOP mode. For details on how to transit to DeepSTOP mode, please refer to Section 4.3.2 DeepSTOP mode.

(2) Start of Cyclic RUN Mode

The operation transitions to Cyclic RUN mode from DeepSTOP mode at the generation of wake-up factor 1.

The operation transitions to Cyclic RUN mode from Cyclic STOP mode at the generation of wake-up factors 0 or 1.

The operation starts from the reset vector address of Cyclic RUN mode (the first address of the Standby RAM).

If one of the FENMI or FEINT interrupts has been generated before recovery from DeepSTOP mode to Cyclic RUN mode, the microcontroller restart operation from the exception handler address:

- FENMI: FENMI handler address (beginning address + $E0_H$)
- FEINT: FEINT handler address (beginning address + $F0_H$)

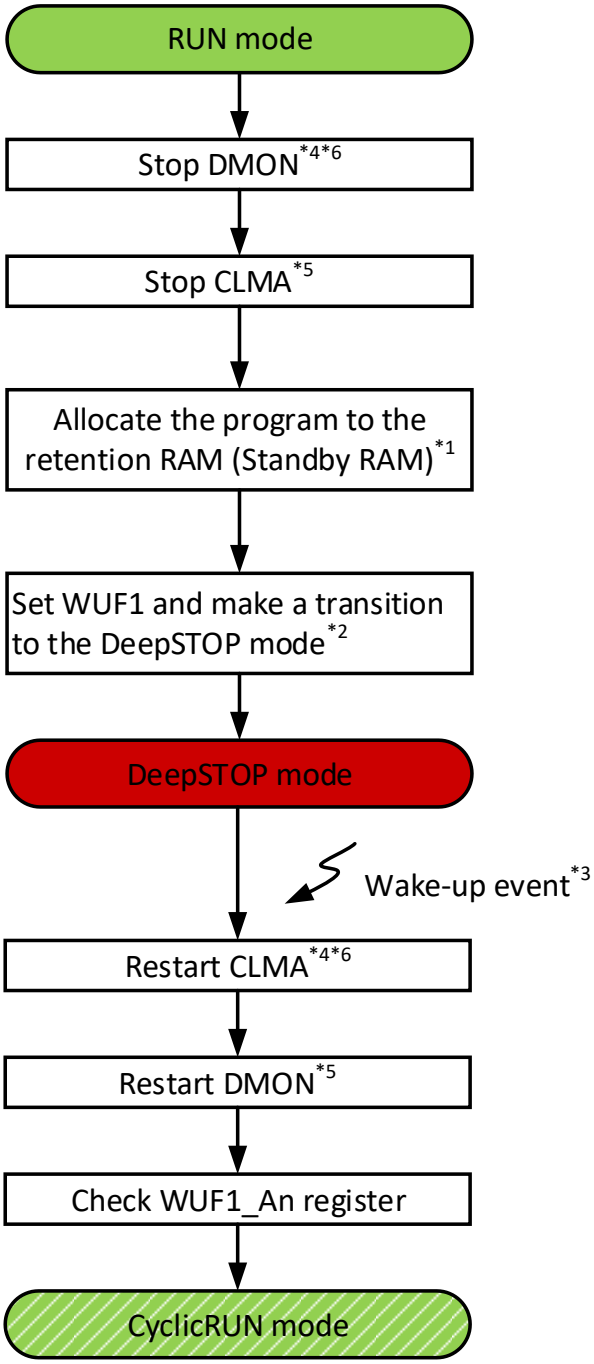
(3) End of Cyclic RUN Mode

The Cyclic RUN mode ends:

- at the transition to the Cyclic STOP mode by setting the STBC0STPT.STBC0STPTRG bit to 1
- at the transition to the DeepSTOP mode by setting the STBC0PSC.STBC0DISTRG bit to 1.

(4) Transition Procedure to Cyclic RUN Mode

The transition procedure (example) to Cyclic RUN mode is shown below in Figure 4-4.



Notes: 1. When the mode shifts from the Cyclic RUN mode to the RUN mode by a wake-up event, it is via DeepSTOP mode. The transition to the DeepSTOP mode should be made in the processing of the interrupt vector for the wake-up event. In that case, the interrupt processing program on the Retention RAM must be allocated.

2. Before the transition to the DeepSTOP mode, clear the flag for wake-up factor 1 in the WUFC1_An register and set wake-up factor 1 that is to be used by the WUFMSK1_A0/WUFMSK1_A1/WUFMSK1_A2 register. Other processing for the transition to the DeepSTOP mode is as usual, please refer to *Section 4.2.2 (5) Transition Procedure to DeepSTOP Mode*.
3. The CPU starts the program from the top address on the Retention RAM after the generation of a wake-up event. The generated wake-up event can be checked by the WUF1_Ax (x = 0 to 2) register.
4. For details please refer to HW user's Manual R01UH0923EJ0100 *Section 13.4.7.4 'Procedures to Reset DMON'* and *Section 13.4.6.4 'DMONDIAGME – DMON DIAG Monitor Enable Register'*.

5. For details please refer to HW user's Manual R01UH0923EJ0100 *Section 16.6.2 'Procedures to Reset by CLMATEST.RESCLM'* and *Section 16.5.7 'CLMAnCTL – CLMAn Control Register'*.
6. Stop DMON when Main OSC stops at chip standby mode.

Figure 4-4 Example of Cyclic RUN mode transition

(5) Operation Status of Cyclic RUN Mode

Table 4-4 lists the detailed operation status of Cyclic RUN mode.

Table 4-4 Operation Statuses of Cyclic RUN and Cyclic STOP modes

Function			Cyclic RUN Mode	Cyclic STOP Mode
Port	AWO		Operable	Operable
	ISO		Stop	Stop
CPU	CPU0		Operable	Stop
	CPUn (n ≠ 0)		Stop	Stop
LPS			Operable	Operable
EXTCLK			Operable	Operable
Peripheral Interconnect (PIC)			Stop	Stop
DFP			Stop	Stop
Motor Control IP	EMU		Stop	Stop
	RDC		Stop	Stop
DSMIF			Stop	Stop
Flash	Code Flash		Stop	Stop
	Data Flash		Stop	Stop
RAM	Local RAM		Stop	Stop
	Cluster RAM		Stop	Stop
	Retention RAM		Operable	Operable
Timer	Operating System Timer (OSTM)		Stop	Stop
	Window Watchdog Timer	WDTBA	Operable	Operable
		WDTB0	Operable	Stop
		WDTB1 to 5	Stop	Stop
		SWDTA	Operable	Stop
	Timer Array Unit D (TAUD)		Stop	Stop
	Timer Array Unit J	TAUJ2, TAUJ3	Operable	Operable
	Long-Term System Counter (LTSC)		Stop	Stop
	Generic Timer Module (GTM)		Stop	Stop
	ATU		Stop	Stop
	Real-time Counter (RTCA)		Operable	Operable
	Motor Control Timer (TSG3)		Stop	Stop
	Timer Option (TAPA)		Stop	Stop
	Timer Pattern Buffer (TABA)		Stop	Stop
	Encoder Timer (ENCA)		Stop	Stop
	High-Resolution PWM (HRPWM)		Stop	Stop
	RLIN3		Operable	Operable

Communication	Multichannel Serial Peripheral Interface (MSPI)		Operable	Stop
	Renesas High-Speed Serial I/F (RHSIF)		Stop	Stop
	I2C Interface (RIIC)		Stop	Stop
	CAN Interface (RS-CANFD)		Stop	Stop
	FlexRay (FLXA)		Stop	Stop
	Renesas High Speed Bus (RHSB)		Stop	Stop
	Ethernet (ETN)		Stop	Stop
	Single Edge Nibble Transmission (RSENT)		Stop	Stop
	PSI5		Stop	Stop
	PSI5S		Stop	Stop
	Multimedia Card Interface (MMCA)		Stop	Stop
	Serial Flash Memory Interface A (SFMA)		Stop	Stop
Safety	Clock Monitor	CLMA0 to 2	Operable	Operable
		CLMA3 to 15	Stop	Stop
	Voltage Monitor (VMON)		Stop	Stop
	OTS		Stop	Stop
	Data CRC Function K (KCRC)		Stop	Stop
	Error Control Module (ECM)		Operable*	Operable*
A/D Converter	SAR-ADCA		Operable	Operable
	SAR-ADC0~3		Stop	Stop
	DS-ADC/CADC		Stop	Stop
	FCOMP		Stop	Stop
Digital Filter	DFE		Stop	Stop
Security	ICUMHA		Stop	Stop

Note: ECM delay timer clock (CLK_ECMCNT) stops.

4.3.4 Cyclic STOP Mode

In Cyclic STOP mode, the functions except RLIN3 and the AWO area peripheral function are stopped.

(1) Preparation for Cyclic STOP Mode

For Cyclic STOP mode, the following setups must be done before the transition:

- Stop DMON.
- Stop CLMA (if the monitor clock would be stopped).
- Ensure the transition to Cyclic RUN mode is finished.
- Set the wake-up related registers.
  - Clear the wake-up factor flags (the WUFCn_Ax/WUFCn_Iy register, n = 0 or 1, x = 0 to 2, y = 0 to 3).
  - Mask the non-wake-up factor (the WUFMSKn_Ax/WUFMSKn_Iy register, n = 0 or 1, x = 0 to 2, y = 0 to 3).
  - Release the masks of the wake-up factor (the WUFMSKn_Ax/WUFMSKn_Iy register, n = 0 or 1, x = 0 to 2, y = 0 to 3).

(2) Start of Cyclic STOP Mode

According to Figure 4-1, the operation switches from Cyclic RUN to Cyclic STOP mode when the STBC0STPTRG bit in register STBC0STPT is set to 1.

(3) End of Cyclic STOP Mode

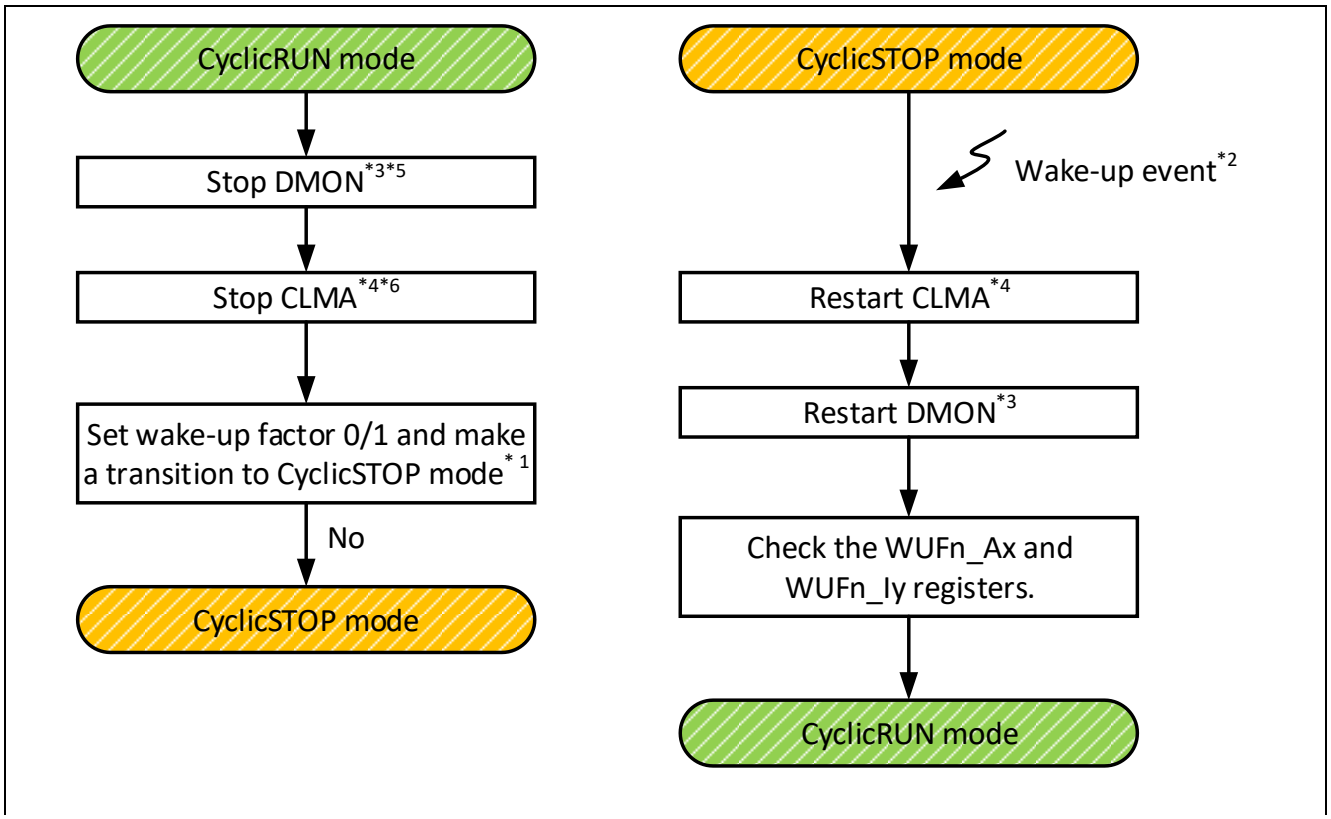
The operation transitions to Cyclic RUN mode at the generation of wake-up factor 0 or 1.

(4) Wake-up Handling

The generation of the wake-up factors can be determined by the wake-up factor flags (WUFn_Ax/ WUFn_Iy, n = 0 or 1, x = 0 to 2, y = 0 to 3).

(5) Transition Procedure to Cyclic STOP Mode

The transition procedure (example) to Cyclic STOP mode is shown below in Figure 4-5.



Notes: 1. The wake-up factors 0 and 1 are normally set to make a transition respectively to RUN mode and Cyclic RUN mode. In the case of Cyclic STOP mode, the operation can only directly switch to Cyclic RUN mode by either wake-up factor 0 or 1.
2. When a wake-up factor is generated in Cyclic STOP mode, the mode shifts to Cyclic RUN mode and the operation starts immediately after the processing shifted to Cyclic RUN mode. The generated wake-up factors can be checked by the WUFn_Ax, WUFn_Iy (n = 0 or 1, x = 0 to 2, y = 1) registers.
3. For details please refer to HW user's Manual R01UH0923EJ0100 *Section 13.4.7.4 'Procedures to Reset DMON'* and *Section 13.4.6.4 'DMONDIAGME – DMON DIAG Monitor Enable Register'*.
4. For details please refer to HW user's Manual R01UH0923EJ0100 *Section 16.6.2 'Procedures to Reset by CLMATEST.RESCLM'* and *Section 16.5.7 'CLMAnCTL – CLMAn Control Register'*.
5. Stop DMON when Main OSC stops at chip standby mode.

Figure 4-5 Example of Cyclic STOP mode transition

(6) Operation Status of Cyclic STOP Mode

For detailed operation status of Cyclic STOP mode, please refer to Table 4-4 in *Section 4.2.3*.

4.4 Wake-Up Control

The chip operation returns from standby modes when a wake-up event occurs.

For different mode transition, the RH850/U2B group provide different category of wake-up events. Table 4-5 shows an overview of these wake-up factors and the operation after wake-up events.

Table 4-5 Overview of Wake-Up Factors

Category	Mode Transition	Wake-Up Factor	Operation after Wake-Up	
			System Clock	Fetch Address
Wake-Up Factor 0	STOP → RUN	WUF0_Ax, x = 0 to 2 WUF0_Iy, y = 0 to 3	Clock setting before STOP mode	Next address before STOP mode was entered or interrupt vector
	DeepSTOP → RUN	WUF0_Ax, x = 0 to 2	Internal OSC Clock (200 MHz or 240 kHz)	RESET vector of code flash
	Cyclic STOP → Cyclic RUN	WUF0_Ax, x = 0 to 2 WUF0_Iy, y = 1	Internal OSC Clock (200 MHz or 240 kHz)	RESET vector of code flash
Wake-Up Factor 1	DeepSTOP → Cyclic RUN	WUF1_Ax, x = 0 to 2	Internal OSC Clock (200 MHz or 240 kHz)	RESET vector of retention RAM
	Cyclic STOP → Cyclic RUN	WUF1_Ax, x = 0 to 2 WUF1_Iy, y = 1	Internal OSC Clock (200 MHz or 240 kHz)	Next address before Cyclic STOP mode was entered or interrupt vector

The wake-up events are controlled by the following standby controller registers:

- Wake-up factor registers: WUF0_A0, WUF0_A1, WUF0_A2, WUF0_I0, WUF0_I1, WUF0_I2, WUF0_I3 WUF1_A0, WUF1_A1, WUF1_A2, WUF1_I0, WUF1_I1, WUF1_I2, WUF1_I3

  Upon occurrence of an effective wake-up factor, the associated wake-up factor flag is set to 1. By checking these registers and their flags, it is possible to identify the wake-up factor.

- Wake-up factor mask registers: WUFMSK0_A0, WUFMSK0_A1, WUFMSK0_A2, WUFMSK0_I0, WUFMSK0_I1, WUFMSK0_I2, WUFMSK0_I3, WUFMSK1_A0, WUFMSK1_A1, WUFMSK1_A2, WUFMSK1_I0, WUFMSK1_I1, WUFMSK1_I2, WUFMSK1_I3

  Each bit of these registers is assigned to a certain wake-up factor. Wake-up by this factor is enabled if its mask bit is set to 0. Wake-up factors assigned to both wake-up factor 0 and 1 should not be enabled at the same time.

- Wake-up factor clear registers: WUFC0_A0, WUFC0_A1, WUFC0_A2, WUFC0_I0, WUFC0_I1, WUFC0_I2, WUFC0_I3, WUFC1_A0, WUFC1_A1, WUFC1_A2, WUFC1_I0, WUFC1_I1, WUFC1_I2, WUFC1_I3

  By setting the applicable bits in these registers to 1, the wake-up factor bit (WUFny) in the wake-up factor registers (WUF0_A0, WUF0_A1, WUF0_A2, WUF0_I0, WUF0_I1, WUF0_I2, WUF0_I3, WUF1_A0, WUF1_A1, WUF1_A2, WUF1_I0, WUF1_I1, WUF1_I2, WUF0_I3) can be cleared.

Note: The wake-up factor flag in the wake-up factor registers only indicate the occurrence of wake-up factor. These flags do not indicate a transition from chip standby mode to normal operation mode.

Table 4-6 lists the assignment of the wake-up factors to the control register bits and status register bits.

Table 4-6 Wake-Up Factors

Wake-Up Factor	Module	Bit Assignment of Wake-Up Factor Registers[*1]	STOP → RUN	DeepSTOP → RUN	Cyclic STOP → Cyclic RUN[*2]	DeepSTOP → Cyclic RUN

TNMI	Port	WUF0_A0	[0]	√	√	√	√
INTCLMATI0	CLMA0	WUFMSK0_A0	[1]	√	√	√	√
INTCLMATI1	CLMA1	WUFC0_A0	[2]	√	√	√	√
INTCLMATI2	CLMA3 CLMA15	or WUF1_A0	[3]	√	–	–	–
INTWDTBA	WDTBA	WUFMSK1_A0	[5]	√	√	√	√
IRQ0	Port	WUFC1_A0	[6]	√	√	√	√
IRQ1	Port		[7]	√	√	√	√
IRQ2	Port		[8]	√	√	√	√
IRQ3	Port		[9]	√	√	√	√
IRQ4	Port		[10]	√	√	√	√
IRQ5	Port		[11]	√	√	√	√
IRQ6	Port		[12]	√	√	√	√
IRQ7	Port		[13]	√	√	√	√
IRQ8	Port		[14]	√	√	√	√
IRQ9	Port		[15]	√	√	√	√
IRQ10	Port		[16]	√	√	√	√
IRQ11	Port		[17]	√	√	√	√
IRQ12	Port		[18]	√	√	√	√
IRQ13	Port		[19]	√	√	√	√
IRQ14	Port		[20]	√	√	√	√
IRQ15	Port		[21]	√	√	√	√
IRQ16	Port	WUF0_A1	[0]	√	√	√	√
IRQ17	Port	WUFMSK0_A1	[1]	√	√	√	√
IRQ18	Port	WUFC0_A1	[2]	√	√	√	√
IRQ19	Port	or	[3]	√	√	√	√
IRQ20	Port	WUF1_A1	[4]	√	√	√	√
IRQ21	Port	WUFMSK1_A1	[5]	√	√	√	√
IRQ22	Port	WUFC1_A1	[6]	√	√	√	√
IRQ23	Port		[7]	√	√	√	√
IRQ24	Port		[8]	√	√	√	√
IRQ25	Port		[9]	√	√	√	√
IRQ26	Port		[10]	√	√	√	√
IRQ27	Port		[11]	√	√	√	√
IRQ28	Port		[12]	√	√	√	√
IRQ29	Port		[13]	√	√	√	√
IRQ30	Port		[14]	√	√	√	√
IRQ31	Port		[15]	√	√	√	√
IRQ32	Port		[16]	√	√	√	√
IRQ33	Port		[17]	√	√	√	√
IRQ34	Port		[18]	√	√	√	√
IRQ35	Port		[19]	√	√	√	√
IRQ36	Port		[20]	√	√	√	√
IRQ37	Port		[21]	√	√	√	√
IRQ38	Port		[22]	√	√	√	√
IRQ39	Port		[23]	√	√	√	√
IRQ40	Port		[24]	√	√	√	√
IRQ41	Port		[25]	√	√	√	√
IRQ42	Port		[26]	√	√	√	√
IRQ43	Port		[27]	√	√	√	√
WUTRG0	LPS	WUF0_A2	[0]	√	√	√	√

WUTRG1	LPS	WUFMSK0_A2 WUFC0_A2 or WUF1_A2 WUFMSK1_A2 WUFC1_A2	[1]	√	√	√	√
INTDCUTDI	JTAG		[2]	√	√	√	√
INTTAUJ2I0	TAUJ2		[3]	√	√	√	√
INTTAUJ2I1	TAUJ2		[4]	√	√	√	√
INTTAUJ2I2	TAUJ2		[5]	√	√	√	√
INTTAUJ2I3	TAUJ2		[6]	√	√	√	√
INTTAUJ3I0	TAUJ3		[7]	√	√	√	√
INTTAUJ3I1	TAUJ3		[8]	√	√	√	√
INTTAUJ3I2	TAUJ3		[9]	√	√	√	√
INTTAUJ3I3	TAUJ3		[10]	√	√	√	√
INTRTCA01S	RTCA		[11]	√	√	√	√
INTRTCA0AL	RTCA		[12]	√	√	√	√
INTRTCA0R	RTCA		[13]	√	√	√	√
INTADCKAI0	ADCKA		[14]	√ *3	√ *3	√ *3	√ *3
INTADCKAI1	ADCKA		[15]	√ *3	√ *3	√ *3	√ *3
INTADCKAI2	ADCKA		[16]	√ *3	√ *3	√ *3	√ *3
INTADCKAI3	ADCKA		[17]	√ *3	√ *3	√ *3	√ *3
INTADCKAI4	ADCKA		[18]	√ *3	√ *3	√ *3	√ *3
INTRCANGRECC0	RSCFD0	WUF0_I0 WUFMSK0_I0 WUFC0_I0	[0]	√	–	–	–
INTRCAN0REC	RSCFD0		[1]	√	–	–	–
INTRCAN1REC	RSCFD0		[2]	√	–	–	–
INTRCAN2REC	RSCFD0		[3]	√	–	–	–
INTRCAN3REC	RSCFD0		[4]	√	–	–	–
INTRCAN4REC	RSCFD0		[5]	√	–	–	–
INTRCAN5REC	RSCFD0		[6]	√	–	–	–
INTRCAN6REC	RSCFD0		[7]	√	–	–	–
INTRCAN7REC	RSCFD0		[8]	√	–	–	–
INTRCANGRECC1	RSCFD1		[9]	√	–	–	–
INTRCAN8REC	RSCFD1		[10]	√	–	–	–
INTRCAN9REC	RSCFD1		[11]	√	–	–	–
INTRLIN30	RLIN30	WUF0_I1 WUFMSK0_I1 WUFC0_I1 or WUF1_I1 WUFMSK1_I1 WUFC1_I1	[0]	√	–	√	–
INTRLIN31	RLIN31		[1]	√	–	√	–
INTRLIN32	RLIN32		[2]	√	–	√	–
INTRLIN33	RLIN33		[3]	√	–	√	–
INTRLIN34	RLIN34		[4]	√	–	√	–
INTRLIN35	RLIN35		[5]	√	–	√	–
INTRLIN36	RLIN36		[6]	√	–	√	–
INTRLIN37	RLIN37		[7]	√	–	√	–
INTRLIN38	RLIN38		[8]	√	–	√	–
INTRLIN39	RLIN39		[9]	√	–	√	–
INTRLIN310	RLIN310		[10]	√	–	√	–
INTRLIN311	RLIN311		[11]	√	–	√	–
INTRLIN312	RLIN312		[12]	√	–	√	–
INTRLIN313	RLIN313		[13]	√	–	√	–
INTRLIN314	RLIN314		[14]	√	–	√	–
INTRLIN315	RLIN315		[15]	√	–	√	–
INTRLIN316	RLIN316		[16]	√	–	√	–
INTRLIN317	RLIN317		[17]	√	–	√	–
INTRLIN318	RLIN318		[18]	√	–	√	–

INTRLIN319	RLIN319		[19]	√	–	√	–
INTRLIN320	RLIN320		[20]	√	–	√	–
INTRLIN321	RLIN321		[21]	√	–	√	–
INTRLIN322	RLIN322		[22]	√	–	√	–
INTRLIN323	RLIN323		[23]	√	–	√	–
INTRCAN0VMRX	RSCFD0	WUF0_I2 WUFMSK0_I2	[1]	√	–	–	–
INTRCAN1VMRX	RSCFD0	WUFC0_I2 or	[2]	√	–	–	–
INTRCAN2VMRX	RSCFD0	WUF1_I2 WUFMSK1_I2	[3]	√	–	–	–
INTRCAN3VMRX	RSCFD0	WUFC1_I2	[4]	√	–	–	–
INTRCAN4VMRX	RSCFD0		[5]	√	–	–	–
INTRCAN5VMRX	RSCFD0		[6]	√	–	–	–
INTRCAN6VMRX	RSCFD0		[7]	√	–	–	–
INTRCAN7VMRX	RSCFD0		[8]	√	–	–	–
INTRCAN8VMRX	RSCFD1		[10]	√	–	–	–
INTRCAN9VMRX	RSCFD1		[11]	√	–	–	–
INTETND05	ETND0	WUF0_I3 WUFMSK0_I3 WUFC0_I3 or WUF1_I3 WUFMSK1_I3 WUFC1_I3	[0]	√	–	–	–
INTETND06	ETND1		[1]	√	–	–	–
INTETNE06	ETND0		[2]	√	–	–	–

Notes: 1. To find the exact wake-up factor category and related registers for the corresponding mode transition, please refer to *Table 4-5 Overview of Wake-Up Factors*.

2. When the transition from Cyclic STOP to Cyclic RUN is made by wake-up factor 0, and the transition to DeepSTOP by STBC0PSC.STBC0DISTRG is made without clearing wake-up factor 0, the transition to RUN mode is made.

3. These wake-up factors are only available in LPS input mode.

4.5 I/O Buffer Control

In chip standby modes, the port groups in AWO area remain their state before entering standby mode. The port groups in ISO area supports the I/O buffer hold state.

In RH850/U2B group devices, the following port groups are individually arranged to AWO and ISO area:

- AWO area: JP0, JP1, P31, P33.
- ISO area: P0, P1, P2, P10, P11, P12, P13, P14, P15, P20, P21, P22, P23, P24, P25, P30, P32, P34.

During the I/O buffer hold state, the I/O buffer maintains the state before it enters this state. Therefore, no external or internal signal can change the state of the I/O buffer until the I/O buffer hold state is terminated.

Table 4-7 provides the information of buffer operation during chip standby mode and after wake-up.

Table 4-7 Buffer Operation before, during and after Chip Standby Modes

Chip Standby Modes	Power Domain	Before Standby	During Standby	After Standby
STOP	AWO	Normal Operation, the I/O buffer remains their state before entering STOP mode		
	ISO			
DeepSTOP	AWO	Normal Operation, the I/O buffer remains their state before entering DeepSTOP mode*2		
	ISO	Normal Operation	I/O buffer hold state	I/O buffer hold state*1

Notes: 1. To release the I/O buffer hold state, bit IOHOLDn.IOHOLD_xxx (n = 0, 1) must be set to 0 after reconfiguration of the peripheral or port function.

2. In the case an alternative function of peripherals in ISO area is assigned to the pin in AWO area, due to the initialization of the peripherals in ISO area by DeeSTOP reset, the state of the I/O buffer may change in the transition of DeepSTOP mode.
To avoid this behavior, it is recommended to change to function of peripherals in AWO area before entering DeepSTOP mode.

4.6 BIST Execution

Referring to Figure 4-1, the RH850/U2B group incorporates Built-In-Self-Test (BIST) function to detect failures of the safety mechanism itself:

- Power-On BIST, executed in both of ISO and AWO power domains before the CPU starts operation (Field BIST0), during the reset sequence of Power On reset, System Reset 1 and System Reset 2.
- Standby-Resume BIST, executed in ISO power domain only during the reset sequence of DeepSTOP reset before the CPU starts operation.

  In accordance with the setting of the BSEQ1CTL and BSEQ2CTL registers, After DeepSTOP reset is generated,
  - Field BIST1 (FBIST1) is executed on the transition from DeepSTOP mode to RUN mode,
  - Field BIST2 (FBIST2) is executed on the transition from DeepSTOP mode to Cyclic RUN mode.

This section describes the details of Standby-Resume BIST.

The BIST consists of Logic BIST (LBIST) and Memory BIST (MBIST). LBIST is considered as the effective hardware safety mechanism to measure latent faults which can reduce software load for error injection tests.

Any of MBIST, LBIST and both can be selected for Standby-Resume BIST by setting either flash option byte 3 or BSEQ0SEL register.

BIST execution results can be identified by the BIST result register (BSEQ0ST).

Table 4-8 Explains the conditions of FBIST1 and FBIST2 execution.

Table 4-8 Execution Conditions of Standby-Resume BIST

Reset Category	BIST	$\overline{\text{TRST}}$ pin	BSEQnCTL. HWBISTEXE		Execution
DeepSTOP Reset (DeepSTOP → RUN)	FBIST1	High	n = 1	0	BIST is skipped. *1 Reset is released without waiting the range of time.
				1	BIST is not executed. *2 Reset is released after waiting the range of time.
		Low		0	BIST is skipped. Reset is released without waiting the range of time.
				1	BIST is executed. Reset is released after BIST is finished.
DeepSTOP Reset (DeepSTOP → Cyclic RUN)	FBIST2	High	n = 2	0	BIST is skipped. Reset is released without waiting the range of time.
				1	BIST is not executed. *1 Reset is released after waiting the range of time.
		Low		0	BIST is skipped. Reset is released without waiting the range of time.
				1	BIST is executed. Reset is released after BIST is finished.

Notes: 1. In this case, BIST is completely not executed.
2. In this case, BIST timer still operates, it will affect to start-up time.

5. Module Standby Mode

This module standby mode stops the clock supply to the peripheral macros to reduce the power consumption in accordance with register settings.

The behavior of the peripheral clocks in both chip standby and module standby modes can be defined in MSR registers.

The peripheral which is in the Module standby mode is not reset and the register access is prohibited.

5.1 Procedure of Module Standby Mode

Example of the procedure of module standby mode is shown below.

5.1.1 Transition to Module Standby Mode

- Check the modules that participate in the module standby mode have completed the operation and are in idle state and no other module or external pin may activate the module. For the details of the way to confirm the idle state of the modules, see the section related to each module.
- Check the Software Module Reset Status Register of modules that participate in the module standby mode is 0. (SWMRESS_<name>. SWMRESS_<name>_n = 0)
- Enable writing to protected registers (MSRKCPROT = A5A5A501H).
- Stop all target clock domains that participate in the module standby mode. (MSR_<name>.MS_<name>_n = 1)
- Disable writing to protected registers (MSRKCPROT = A5A5A500H).

5.1.2 Cancelling Module Standby Mode

- Check the Software Module Reset Status Register of modules that participate in the module standby mode is 0. (SWMRESS_<name>. SWMRESS_<name>_n = 0)
- Enable writing to protected registers (MSRKCPROT = A5A5A501H).
- Start all target clock domains that cancels Module standby mode. (MSR_<name>.MS_<name>_n = 0)
- Read the value of MSR_<name>.MS_<name>_n bit and check the value is 0. In case of cancellation it is necessary to wait until clock is supplied to module.
- Disable writing to protected registers (MSRKCPROT =A5A5A500H).
- Read the value of MSRKCPROT and check the value is 00000000H.

5.2 Module Standby Registers

Table 5-1 shows the peripherals and their clock operation propriety in each operation mode.

Table 5-1 MSR Registers*2

Module	Power Domain	MSR Register		
		Register Name	Bit MS_<name>	Bit STPMSK_<name>
WDTBA	AWO	MSR_WDTB_AWO	MS_WDTBA_0	STPMSK_WDTB_AWO
TAUJ2 TAUJ3		MSR_TAUJ_AWO	MS_TAUJ_AWO_0 to 1	STPMSK_TAUJ_AWO
RTCA		MSR_RTCA	MS_RTCA_0	STPMSK _RTCA
SAR-ADCA		MSR_ADCK_AWO	MS_ADCK_AWO_0	STPMSK_ADCK_AWO
SFMA	ISO	MSR_SFMA	MS_SFMA_0	–*1
MMCA		MSR_MMCA	MS_MMCA_0	–*1
MSPI		MSR_MSPI	MS_MSPI_0 to 9	–*1
RLIN3		MSR_RLIN3	MS_RLIN3_0 to 23	STPMSK_RLIN3
RIIC		MSR_RIIC	MS_RIIC_0 to 1	–*1
RS-CANFD		MSR_RSCFD	MS_RSCFD_0 to 1	STPMSK_RSCFD
Flex Ray		MSR_FLXA	MS_FLXA_0	–*1
RHSB		MSR_RHSB	MS_RHSB_0 to 3	–*1
RSENT		MSR_RSENT	MS_RSENT_0 to 29	–*1
RHSIF		MSR_RHSIF	MS_RHSIF_0 to 1	–*1
Ethernet		MSR_ETH	MS_ETN_0 to 2	–*1
PSI5		MSR_PSI5	MS_PSI5_0 to 3 & 5	–*1
PSI5-S		MSR_PSI5S	MS_PSI5S_0 to 1	–*1
OSTM		MSR_OSTM	MS_OSTM_0 to 5	–*1
TAUD		MSR_TAUD	MS_TAUD_0 to 3	–*1
TSG3		MSR_TSG3	MS_TSG3_0 to 2	–*1
GTM		MSR_GTM	MS_GTM_0	–*1
ATU		MSR_ATU	MS_ATU_0	–*1
ENCA		MSR_ENCA	MS_ENCA_0 to 1	–*1
TAPA		MSR_TAPA	MS_TAPA_0 to 5	–*1
HRPWM		MSR_HRPWM	MS_HRPWM_0	–*1
SAR-ADC 0~3		MSR_ADCK_ISO	MS_ADCK_ISO_0 to 7	–*1
DS-ADC/CADC		MSR_DSADC_CADC	MS_DSADC_CADC_0 to 6	–*1
DFE		MSR_DFE	MS_DFE_0	–*1
DFP		MSR_DFP	MS_DFP_0	–*1
EMU		MSR_EMU	MS_EMU_0 to 1	–*1
RDC		MSR_RDC	MS_RDC_0 to 3	–*1
TPBA		MSR_TPBA	MS_TPBA_0 to 1	–*1
FCOMP		MSR_FCOMP	MS_FCOMP_0 to 10	–*1
DSMIF		MSR_ DSMIF	MS_ DSMIF_0 to 1	–*1

Notes: 1. There is no STPMSK_<name> bit in MSR registers for these peripherals, the clock is automatically stopped in chip standby modes.

2. Before configuring the MSR_<name> registers, the key code protection register MSRKCPROT must be set to A5A5A501H.

5.3 Behavior of Module Standby Mode during Chip Standby Mode

Depending on the state of module standby register MSR_<name>, the clock supply state in each operation mode and chip standby mode is shown in Table 5-2.

Table 5-2 Module Standby Settings and Clock Supply of Peripherals in Chip Standby Mode

Register MSR_<name>		Operation Mode		Chip Standby Mode		
Bit MS_XXX	Bit STPMSK_XXX	RUN	Cyclic RUN	STOP	DeepSTOP	Cyclic STOP
0	0	Operable	Operable	Stop	Stop	Stop
	1	Operable	Operable	Operable	Operable	Operable
1	0	Stop	Stop	Stop	Stop	Stop
	1	Stop	Stop	Stop	Stop	Stop

6. Low-Power Sampler (LPS)

This section provides information about low power sampler and some typical use cases, in that the LPS is used to cyclically poll either digital inputs, analog inputs or both.

6.1 Overview

The Low-Power Sampler (LPS) provides the possibility to periodically poll digital and/or analog inputs without the need for any interactions of the CPU. Applying only peripherals that reside on the AWO are, the LPS can operate in any standby mode, especially the DeepSTOP mode.

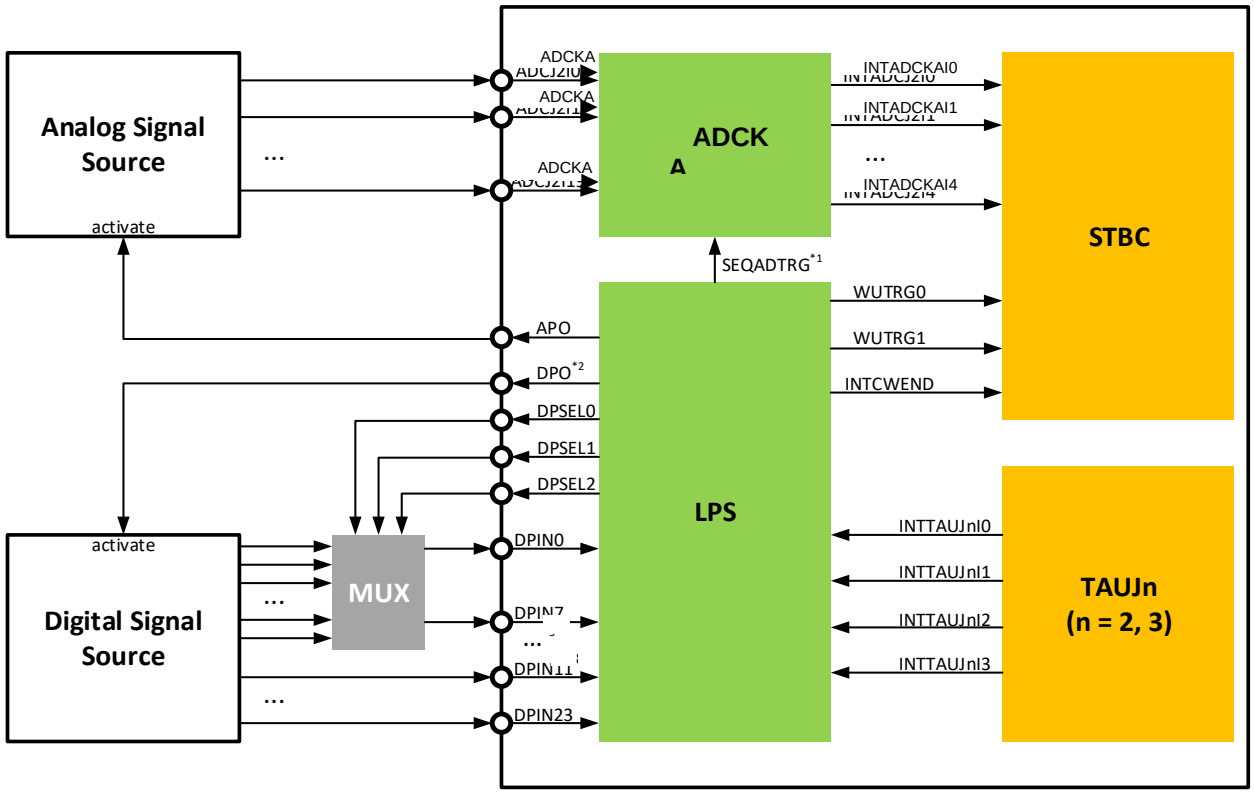
Wake-up of the device from the standby mode is only required, if the input values sampled by the LPS are not within programmable limits.

As the complete flow of input signal polling and evaluation is performed by a dedicated HW, the average power consumption addition to any standby mode is very small.

A complete LPS application is related to the following peripherals:

- LPS
- Clock Controller
- ADCKA
- TAUJ2, TAUJ3
- STBC

Figure 6-1 shows a connection example between the main components of the LPS and the external circuit.



Notes: 1. SEQADTRG is one of the Hardware triggers for A/D conversion. The APO is set to 1, after the stabilization time that is configured by register CNTVAL, the LPS outputs a trigger to A/D converter.
2. When the port input is acquired for the first time in a operation cycle, the DPO is set to 1.

Figure 6-1 Block Diagram of the LPS

This section contains a description of the generic functions and configuration for the Low-Power Sampler (LPS).

In this section, the individual LPS units are identified by the index “n”.

The number of digital port input channels for LPS port polling, as well as the number of analog input channels for A/D converter, is indicated by the index “m”.

The external multiplexer select output signal for digital port is indicated by the index “k”.

LPS sequence start trigger input signal is indicated by the index “x”.

For RH850/U2B group devices, n = 0, k = 0 to 2, x = 0 to 3. The index “m” is device-dependent.

LPS operation is started by interval timer TAUJ2/TAUJ3 on AWO area and ended by the wake-up factors or sequencer end. During the operation, the external events are checked periodically.

The following sections provides the detailed information of 3 input modes:

- Digital input mode
- Analog input mode
- Mixed input mode

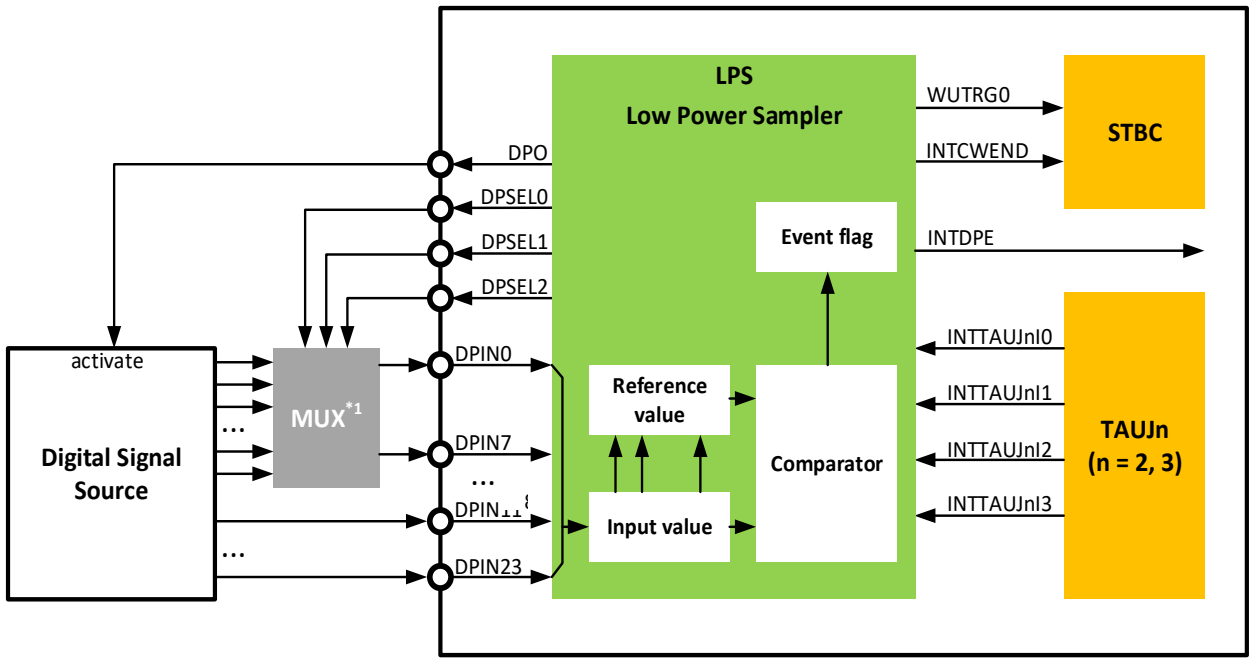
6.2 Digital Input Mode

6.2.1 General Feature of Digital Input Mode

According to Figure 6-2, the digital input ports DPINm are connected to the digital signal source.

Up to 64 input ports can be monitored if multiplexer is connected externally. Port DPSELk is used to switch the external multiplexer. The DPSELk output is switched for the number of times specified in the SCTLR register.

TAUJ2/TAUJ3 is used to set the timing to check the value input to the port.



Notes: 1. If multiplexer is connected to the digital input, the sequencer can be used to implement port expention in digital input mode.

Figure 6-2 Block Diagram for the Digital Input Mode of LPS

Upon a trigger by the interval set by a TAUJ2 or TAUJ3 channel the input polling sequence is started.

When the HS IntOSC is stopped in a standby mode, the operation of the HS IntOSC will be resumed while the sequencer is running.

In case an external multiplexer is used (to increase the number of digital inputs), the multiplexer is set to the desired address by the DPSELk outputs. After setting a new address, the operation waits a stabilization time, this is set in the register CNTVAL.

The port check is then executed.

The digital input values are captured and stored in the DPIN data input monitor registers DPDIMR0 to 7. The reference value is set by the DPIN data set registers DPDSR0, DPDSRM and DPDSRH.

The comparator compares the input value and the reference value. If both values don't match, the event flag of the register EVFR is set to 1 and the low-power sampler outputs a wake-up factor WUTRG0 to the standby controller.

The interrupt INTDPE is triggered in case of a comparison mismatch in any operation modes.

At the completion of checking all ports that have been set, an INTCWEND interrupt occurs.

For details, referring to the related description in the chapter ‘Low-Power Sampler (LPS)’, sub-chapter ‘Digital Input Mode’ in the User’s Manual, on the:

- *Figure 18.5 Operation of Digital Input Mode (8 Ports × 8) when the Input Value is not Changed (RUN Mode)* and
- *Figure 18.6 Operation of Digital Input Mode (24 Ports × 1) when the Input Value is Changed (DeepSTOP Mode)*.

6.2.2 Configuration of Digital Input Mode

In digital input mode, the digital source signals and the digital sensor control signal DPO is used by the low-power sampler. If the input is extended using multiplexer, the multiplexer selection signals are output from LPS to choose the corresponding input.

(1) TAUJ2 or TAUJ3 configuration for digital input mode:

The low-power sampler can be started by the TAUJn (n = 2 or 3) trigger. To configure a TAUJn channel, the following TAUJn registers listed in Table 6-1 must be specified.

Table 6-1 TAUJ Configuration for LPS Application

Operation		Rgister	Bit Name	Bit Position
Select the clock source of CLKA_TAUJ[*1].		CKS_ATAUJC	ATAUJSCSID[2:0]	2 to 0
Specify the TAUJn Clock for	CK0	TAUJnTPS	TAUJnPRS0[3:0]	3 to 0
	CK1		TAUJnPRS1[3:0]	7 to 4
	CK2		TAUJnPRS2[3:0]	11 to 8
	CK3_PRE		TAUJnPRS3[3:0]	15 to 12
Specify CK3_PRE clock division factor for CK3.		TAUJnBRS	TAUJnBRS[7:0]	7 to 0
Specify the operation mode. In this application, the interval timer mode is selected.		TAUJnCMORm	TAUJnMD[4:0]	4 to 0
Determine the timing to update the data register TAUJnCDRm and status register TAUJnCSRm.			TAUJnCOS[1:0]	7 to 6
Select the external start trigger. In this application, the software trigger is selected by setting these bit to 0_H.			TAUJnSTS[2:0]	10 to 8
Set master or slave channel if synchronous channel operation is required.			TAUJnMAS	11
Select a count clock for TAUJnCNTm counter.			TAUJnCCS[1:0]	13 to 12
Select an operation clock, which is used with the TAUJnTTINm input edge detection circuit.			TAUJnCKS[1:0]	15 to 14
Configure of a valid edge of input signal TAUJTTINm.		TAUJnCMURm	TAUJnTIS[1:0]	1 to 0
Enable/disable simultaneous rewrite of the data register of channel 3 to 0.		TAUJnRDE	TAUJnRDE03 to 00	3 to 0
Specify when the signal that triggers simultaneous rewrite is generate		TAUJnRDM	TAUJnRDM03 to 00	3 to 0
Trigger the simultaneous rewrite enabling state.		TAUJnRDT	TAUJnRDT03 to 00	3 to 0
Enable/disable Independent Channel Output Function.		TAUJnTOE	TAUJnTOE03 to 00	3 to 0
Specify the channel output mode to independent or synchronous output mode		TAUJnTOM	TAUJnTOM03 to 00	3 to 0
Specify the output mode.		TAUJnTOC	TAUJnTOC03 to 00	3 to 0
Determine the output logic of the channel.		TAUJnTOL	TAUJnTOL03 to 00	3 to 0

Specify and reads the level of TAUJnTTOUTm.	TAUJnTO	TAUJnTO03 to 00	3 to 0
Enable the counter operation for channel m.	TAUJnTS	TAUJnTS03 to 00	3 to 0

Notes: 1. This register is write-protected register.

In a LPS application, the TAUJn is configured as an interval timer.

For further information of TAUJ functions and configuration please refer to the HW User's Manual R01UH0923EJ0100 *Section 15.5.5 'Clock Selector/Divider Control Register'* and *Section 36 'Timer Array Unit J'*.

(2) Pin Functions configuration for digital input mode:

In digital input mode, the sequencer has following external input/output signals:

- DPO
- DPSELk
- DPINm

To enable these LPS input and output, the related pins must operate in software I/O control alternative function mode, please refer to the HW User's Manual R01UH0923EJ0100 *Section 2 'Pin Functions' Table 2.7 Alternative mode selection table.*

For the arrangement of port alternative functions, please refer to the HW User's Manual R01UH0923EJ0100 *Section 2 'Pin Functions'*.

(3) LPS configuration for digital input mode:

To switch the LPS into digital mode, the registers listed in Table 6-2 must be specified, and the LPS status of digital input mode can be checked in the registers in Table 6-3.

Table 6-2 Configuration of LPS for Digital Input Mode

Operation		Register[*2]	Bit Name	Bit Position
Enable comparison, specify the corresponding compare target bit in	DPDSR0, DPDIMR0	DPSELR0	D0EN_23 to 0	23 to 0
	DPDSRM, DPDIMRM	DPSELRM	D1EN_7 to 0	7 to 0
			D2EN_7 to 0	15 to 8
			D3EN_7 to 0	23 to 16
			D4EN_7 to 0	31 to 24
	DPDSRH, DPDIMRH	DPSELRH	D5EN_7 to 0	7 to 0
			D6EN_7 to 0	15 to 8
			D7EN_7 to 0	23 to 16
specifies the data to be compared with the data captured at a digital input pin and stored in	DPDIMR0	DPDSR0	D0_23 to 0	23 to 0
	DPDIMR4 to DPDIMR1	DPDSRM	D1_7 to 0	7 to 0
			D2_7 to 0	15 to 8
			D3_7 to 0	23 to 16
			D4_7 to 0	31 to 24
	DPDIMR7 to DPDIMR5	DPDSRH	D5_7 to 0	7 to 0
			D6_7 to 0	15 to 8
			D7_7 to 0	23 to 16
Specify the stabilization time[*1] of the external circuits. Stabilization time = (1 / ($f_{HS\ IntOSC}$/20)) · 16 · CNT0n		CNTVAL	CNT0[7:0]	7 to 0
Specify the number of times the port is read in digital input mode.		SCTLR	NUMDP[2:0]	6 to 4
Select the TAUJ2/TAUJ3 channel			TJIS[2:0]	7, 3 to 2
Enable digital input mode.			DPEN[*3]	0

Notes: 1. When the DPO output is set to 1, the port input is acquired for the first time after the setting time.
2. These bits above must be set before the sequence operation is started, i.e. when SCTLR.DPEN = 0, SCTLR.ADEN = 0 and SOSTR.SOF = 0.
3. After all the LPS configuration is finished, the bit DPEN can be set to 1 to enable the digital input mode.

Table 6-3 Status and Result Registers of LPS

Rgister	Bit Name	Bit Value	Contents
SOSTR	SOF	0	Operation of the LPS is not started
		1	Operation of the LPS is in progress
EVFR	DINEVF	0	The result of comparison is match
		1	The result of comparison is mismatch

For further information, please refer to HW User's Manual *Section 18.3 'Registers (LPS)'*.

(4) STBC configuration for digital input mode:

The LPS can run in any operation/standby mode of the device. Still, the typical use case is its operation while the device remains in DeepSTOP mode. Therefore, this use case will further be described here.

To wake-up the device from DeepSTOP mode to RUN mode in case the polled valued does not match the expected value, the STBC peripheral must be configured as is described below:

- Set the Wake-Up Factor Mask registers WUFMSK0_A2.
  The wake-up factor WUTRG0 can be enabled by setting the bit WUFMSK0_A2 [0] of this register to 0.
- Start DeepSTOP mode using the Power Save Control register STBC0PSC.
- After the operation mode of the MCU is switched into RUN mode:
  - Clear the wake-up factor by writing 1 to the corresponding bit of the Wake-Up Factor Clear register WUFC0_A2.
  - Release the I/O hold state by writing 0 to the IOHOLD0 and IOHOLD1 registers.

6.3 Analog Input Mode

6.3.1 General Feature of Analog Input Mode

In analog input mode, the analog input ports that are connected to the analog signal sources can be supervised. Please refer to Figure 6-3 for an overview.

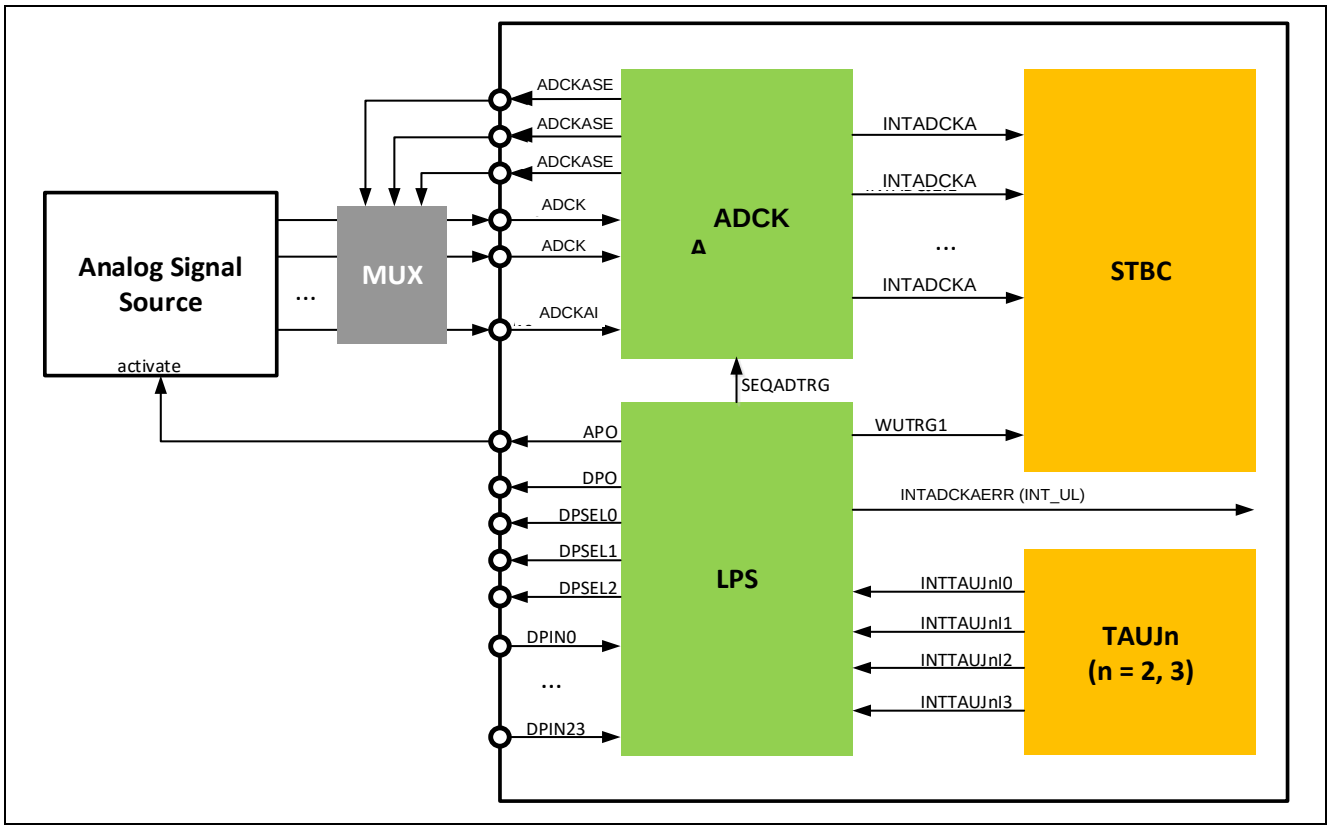


Figure 6-3 Block Diagram for the Analog Input Mode of LPS

Upon a trigger by the interval set by a TAUJ2 or TAUJ3 channel the input polling sequence is started.

When the HS IntOSC is stopped in a standby mode, the operation of the HS IntOSC will be resumed while the sequencer is running.

The APO signal is set to 1 to activate the analog signal sources (e.g. sensors). After the APO wait time is passed, an A/D conversion trigger is sent to the ADCKA.

The A/D conversion trigger of the LPS starts the conversion of the related Scan Group (the Scan Group that has selected this trigger).
In case a multiplexer is used to increase the number of analog signals, it is controlled by the logic of the ADCK.

The analog inputs are converted by the ADCKA and the conversion result is evaluated/compared using the ADCK upper/lower limit function. If the input signal is not in the expected voltage range, an LPS0 analog port error interrupt INTADCKAERR (INT_UL) is generated, what results in the occurrence of a wake-up factor WUTRG1.

For details, referring to the related description in the *Section 18.5 'Analog Input Mode'* in the HW User's Manual, to the following figures:

- *Figure 18.9 Operation of Analog Input Mode when the Conversion Result is within the Expected Range (RUN Mode)* and
- *Figure 18.10 Operation of Analog Input Mode when the Conversion Result is not within the Expected Range (DeepSTOP Mode)*.

6.3.2 Configuration of Analog Input Mode

In analog input mode, the input signals are connected to the A/D converter, the low-power sampler outputs the APO signal and triggers the ADCKA, and the standby controller receives the wake-up factor WUTRG1 and INTADCKAERR if the input is out of the expected voltage range.

(1) TAUJ2 or TAUJ3 configuration for analog input mode:

To configure TAUJ2/TAUJ3 for analog input mode, please refer to *Section 6.2.2 (1) TAUJ2 or TAUJ3 configuration for digital input mode*.

(2) Pin functions configuration for analog input mode:

In analog input mode, the sequencer has following external input/output signals:

- APO
- ADCKAIm

To configure the LPS output signal APO, the related pins must operate in software I/O control alternative function mode, for details please refer to *Section 6.2.2 (2) Pin functions configuration for digital input mode*.

The ADCKA inputs are special alternative pins that are permanently connected to the A/D module.

To configure the ADCK I/O channels please refer to the HW User's Manual R01UH0923EJ0100 *Section 2 'Pin Functions'*.

(3) ADCKA configuration:

The following setup in Table 6-4 is required for using the ADCKA:

Table 6-4 ADCJ2 Configuration*2

Function	Register	Bit Name	Bit Position
Select the clock for ADCKA.	CKS_AADCC	AADCSCSID[1:0]	1, 0
Set the suspending method between scan groups.	ADCKAADCR1	SUSMTD[1:0]	1, 0
Specify the data format of conversion result in ADCKADRj.	ADCKAADCR2	DFMT[2:0]	6 to 4
Select the addition count of addition mode A/D conversion.		ADDNT	0
Enable/disable trigger overlap check error interrupts.	ADCKASFTCR	TOCEIE	6
Set read and clear enable operation.		RDCLRE	4
Enable/disable overwrite error interrupts.		OWEIE	2
Enable/disable parity error interrupts.		PEIE	1
Enable/disable ID error interrupts.		IDEIE	0
Specify the upper-limit threshold value of A/D conversion values.	ADCKAVCULLMTBR0 to 7	VCULMTB[15:0]	31 to 16
Specify the lower-limit threshold value of A/D conversion values.		VCLLMTB[15:0]	15 to 0
Enable/disable output of upper/lower limit check interrupt.	ADCKAVCLMINTER1	ADUL31IE to ADUL00IE	31 to 0
	ADCKAVCLMINTER2	ADUL63IE to ADUL32IE	31 to 0
Specify if upper/lower limit check status is reported.	ADCKAVCLMSR1	VC31LMS to VC00LMS	31 to 0
	ADCKAVCLMSR2	VC63LMS to VC32LMS	31 to 0
Specify extended sampling period if extended sampling A/D conversion mode is selected in CNVCLS[3:0].	ADCKASMPCR	EXSMPT[7:0]	23 to 16
Enable/disable buffer amplifier.		BUFAMPD	15
Enable/disable the selection of sampling period.		SMPTS	12

Specify the sampling period.		SMPT[7:0]	7 to 0
Specify the normal/addition mode in which the wiring-break detection is performed.	ADCKAODCR	WADDE	8
Select the pulse width of wiring-break detection.		ODPW[4:0]	4 to 0
Enable/disable the overlap check function.	ADCKATOCCR	TOCE	0
Set a virtual channel to monitor the A/D conversion timing signal.	ADCKAADENDP0 to 4	ENDP[5:0]	5 to 0
Set the initial phase of A/D timer x.	ADCKAADTIPR3 to 4	ADTIP[20:0]	20 to 0
Set the cycle of A/D timer x.	ADCKAADTPRR3 to 4	ADTPR[20:0]	20 to 0
Set voltage dividing resistor.	ADCKAVMONVDCR1	VDE1	0
	ADCKAVMONVDCR2	VDE2	0
Specify the end virtual channel.	ADCKASGVCPR0 to 4	VCEP[5:0]	13 to 8
Specify the starting virtual channel.		VCSP[5:0]	5 to 0
Specify the scan count in multicycle scan mode.	ADCKASGMCYCR0 to 4*1	MCYC[7:0]	7 to 0
Setup arbitrary wait time before executing a virtual channel.	ADCKAWAITTR 0 to 7	WAITTIME[13:0]	13 to 0
Select an upper/lower limit check table register to be compared.	ADCKAVCRn	VCULLMTBS[3:0]	31 to 28
Select the wait time to be inserted before executing a virtual channel.		WTTS[3:0]	27 to 24
Select whether to perform entry to the DFE.		DFENT	20
Set the channel of DFE if entry is requested.		DFETAG[3:0]	19 to 16
Select conversion type.		CNVCLS[3:0]	14 to 11
Set the channel of external MPX to be transferred to the external analog multiplexer.		MPXV[2:0]	10 to 8
Enable/disable virtual channel interrupt.		ADIE	7
Set A/D conversion for each conversion mode*2.		GCTRL[5:0]	5 to 0
Enable/disable A/D conversion simultaneous start.	ADCKASGCR0 to 4	ADSTARTE	6
Set scan mode of scan group x.		SCANMD	5
Enable/disable scan end interrupt.		ADIE	4
Enable/disable hardware triggers of scan group x.		TRGMD	0
Select hardware trigger*3 for A/D conversion.	ADCKASGTSELx	TxSEL[5:0]	5 to 0

Notes: 1. Setup of this register is only required if the multicycle scan mode is selected in register ADCKASGCRx.

2. The setup details for RH850/U2B group devices are described in HW User's Manual *Section 50.3.2.1 'ADCKnVCRj — Virtual Channel Register j'*.

3. The hardware triggers for A/D conversion are described in HW User's Manual *Section 50.3.4.1 'ADCKnSGTSELx — Scan Group x Start Trigger Control Register.*

(4) LPS configuration for analog input mode:

To switch the LPS into analog input mode, the registers listed in Table 6-5 below must be specified:

Table 6-5 Configuration of LPS for Analog Input Mode

Operation	Register[*2]	Bit Name	Bit Position
Specify the stabilization time[*1] of the external circuits. Stabilization time = (1 / ($f_{HS\ IntOSC}$/20)) ・16・ CNT1n	CNTVAL	CNT1[7:0]	15 to 8
Select the TAUJ2/TAUJ3 channel.	SCTLR	TJIS2	7
		TJIS[1:0]	3 to 2
Enable analog input mode.		ADEN[*3]	1

Notes: 1. When the APO output is set to 1, the port input is acquired after the LPS outputs the A/D conversion trigger to ADCKA within the setting time.
2. These bits above must be set before the sequence operation is started, i.e. when SCTLR.DPEN = 0, SCTLR.ADEN = 0 and SOSTR.SOF = 0.
3. After all the LPS configuration is finished, the bit ADEN can be set to 1 to enable the digital input mode.

The LPS status of analog mode can be checked in the LPS Operation State register SOSTR. For detailed information, please refer to *Section 6.2.2 (3) LPS Configuration for digital input mode*.

(5) STBC Configuration for analog input mode:

For analog input mode, the STBC peripheral configuration is described below:

- Set the Wake-Up Factor Mask registers WUFMSK0_A2.
  - The wake-up factor WUTRG1 can be enabled by setting bit WUFMSK0_A2 [1] in this register to 0.
  - If a cyclic operation is required after the A/D conversion, the wake-up factor INTADCKAIx of the scan group x, that is employed for the application, can be enabled by setting 0 to the bit WUFMSK1_A2[x] of register WUFMSK1_A2, where x = 14 to 18.
- Start the DeepSTOP mode using the Power Save Control register STBC0PSC.
- After the operation mode of the MCU is switched into RUN mode:
  - Clear the wake-up factor by writing 1 to the corresponding bit of the Wake-Up Factor Clear register WUFC0_A2.
  - Release the I/O hold state by setting 0 to the IOHOLD0 and IOHOLD1 register.

6.4 Mixed Mode

If digital input mode and analog input mode are both required in an application use case, the low-power sampler operates in the mixed mode.

Figure 6-4 illustrates the basic flow chart of the LPS mixed mode.

The mixed mode is an operation mode includes both digital and analog input mode. Therefore, the configuration of mixed mode is a combination of digital and analog input mode. For details, please refer to *Section 6.3.2 and 6.3.3*.

6.5 Pin Assignment

For the external input/output and pin assignment of LPS, please refer to HW user's manual R01UH0923EJ0100 attachment "E02_01_List_of_Pin_Assignment.xlsx".

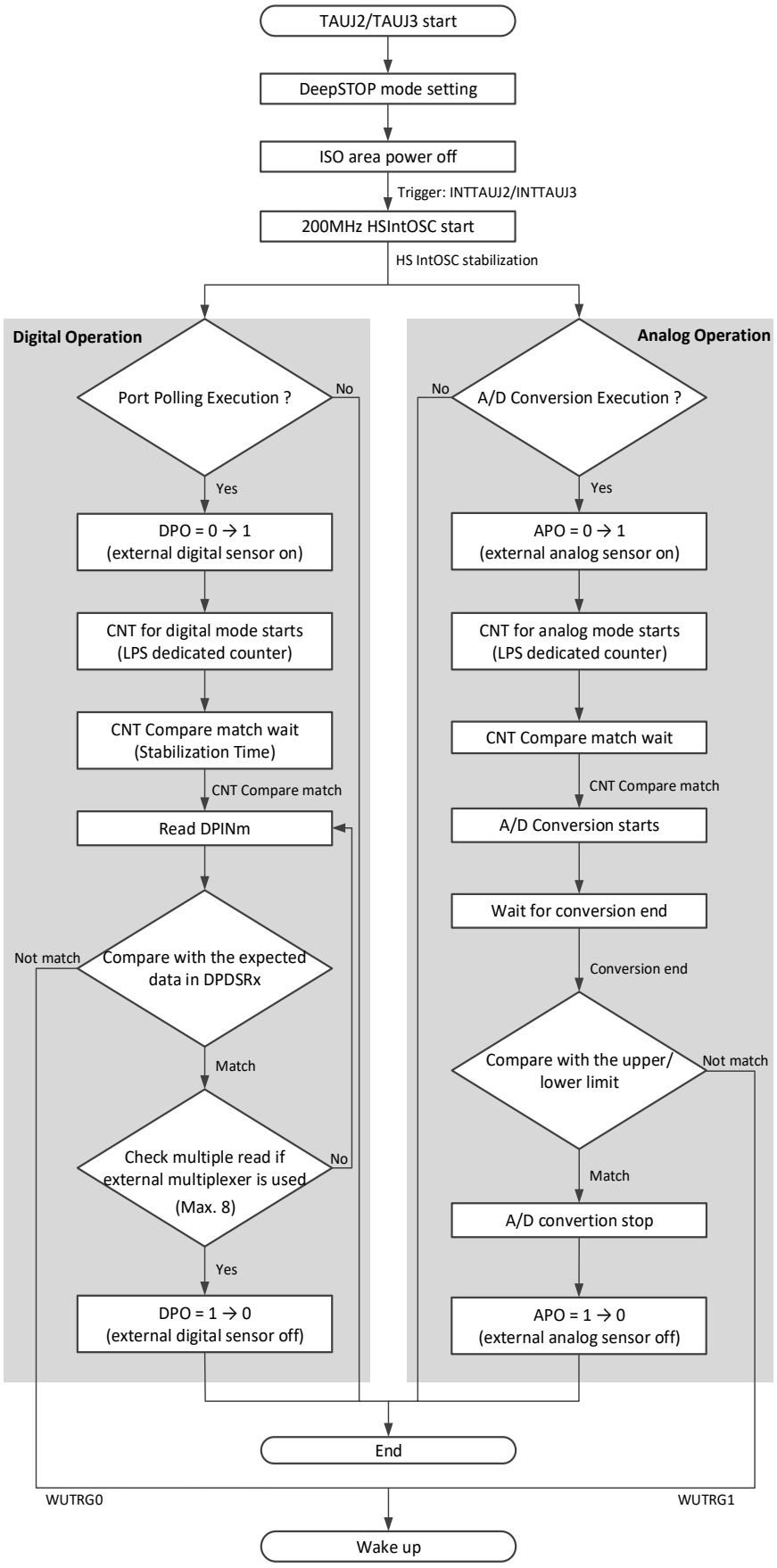


Figure 6-4 Basic flow chart of the mixed mode

7. Use Cases

This section shows several examples of the low-power operation as typical use cases.

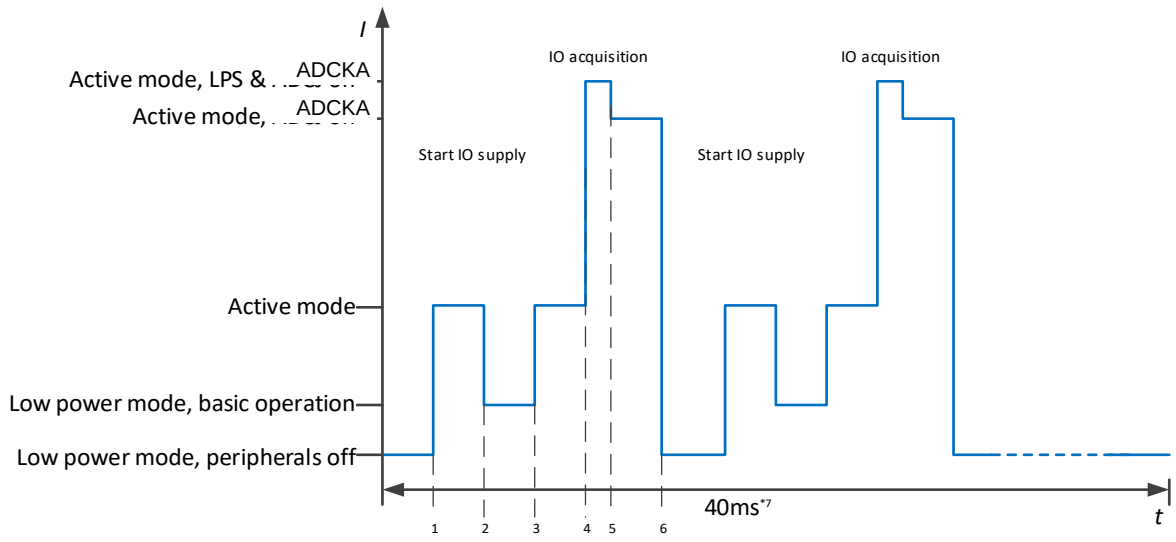
7.1 Digital and analog port polling

To show a cyclic wake-up example application, using both digital and analog input mode of LPS, the following conditions are used for the setups:

- Cyclic Period: 40ms;
- Peripherals used: LPS, TAUJ2 and ADCKA;
- Operating modes: DeepSTOP;
- Channels: 24 digital inputs and 8 analog inputs.

The flow chart of the application is illustrated in Figure 6-4.

Figure 7-1 shows the cyclic wake-up current calculation of digital and analog inputs.



Notes: 1. Referring to Figure 6-7, the I/O supply is started when the DPO or APO is set to 1.
2. The SEQ dedicated counter starts the count for a stabilisation time of about 50 µs for digital mode and 100 µs for analog mode.
3. After the 50 µs stabilization time, the LPS starts the I/O acquisition and data comparetion.
4. The SEQ dedicated counter reaches the stabilisation time of about 100 µs for analog mode, the ADCKA starts the I/O acquisition and conversion.
5. If there is no mismatch of the input signal, the digital compare process is ended and the MCU continues the A/D conversion if the analog process is not completed.
6. If there is no mismatch or unexpected voltage during the digital and analoge process, the microcontroller returns to low-power mode before the next operation cycle starts.
7. In the 40 ms cyclic period, the microcontroller works first in DeepSTOP mode before the I/O supply is started. Then stays in DeepSTOP mode with LPS operation and A/D conversion as it is described in Note 1 to 6. After the operation is finished, the MCU ends the period with a TAUJ2/TAUJ3 trigger, and remains in DeepSTOP mode until the start of the next period.

Figure 7-1 Cyclic Wake-up Calculation of Digital and Analog Inputs

The configuration of the following peripherals is required for this example, the setup details are described in *Section 6.2.2* and *Section 6.3.2*.

8. Summary

The standby modes of the RH850/U2B group devices provide a variety of possibility to reduce the average current consumption.

The peripherals Power Supply, STBC, Clock Controller and LPS are related to low-power operations.

The RH850/U2B series supports the following power-save modes:

- STOP mode
- DeepSTOP mode
- Cyclic RUN mode
- Cyclic STOP mode
- Power Off Standby mode

To implement the low-power operations, the corresponding peripherals must be configured according to the required application.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	2024.06.14	-	Initial edition

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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