RH850/U2A-EVA Group

Usage notes of LDVS PCB design

Introduction

This application note explains notes on LVDS board design for RH850/U2A-EVA Group.

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Target Device

- RH850/U2A-EVA Group
  - RH850/U2A-EVA
  - RH850/U2A16
  - RH850/U2A8
  - RH850/U2A6

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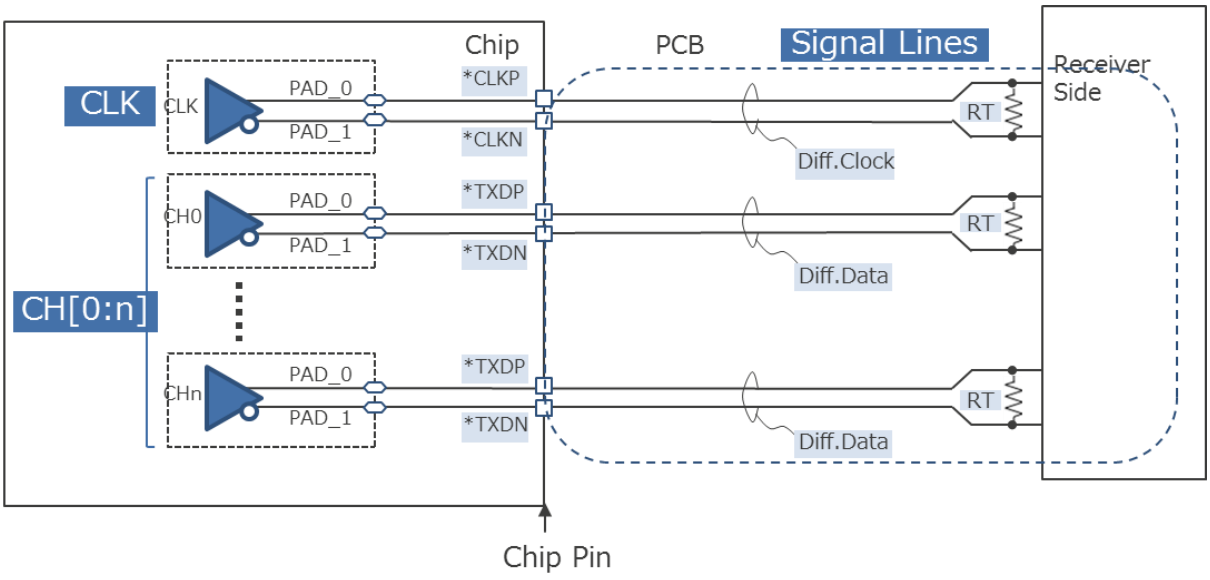
1. Guideline of LVDS signal line

1.1 Topology (LVDS-TX, RX)

[Signal line symbol]

- *CLKP、*TXDP : Positive Single-ended signal(pos.)
- *CLKN、*RXDN : Negative single-ended signal(neg.)
- Diff. Clock、Data : Differential Signal
- RT（100Ω±1%） : Termination Resistor(If external Resistor is required)
  Please place RT nearer the receiver pins.

[TX]



[RX]

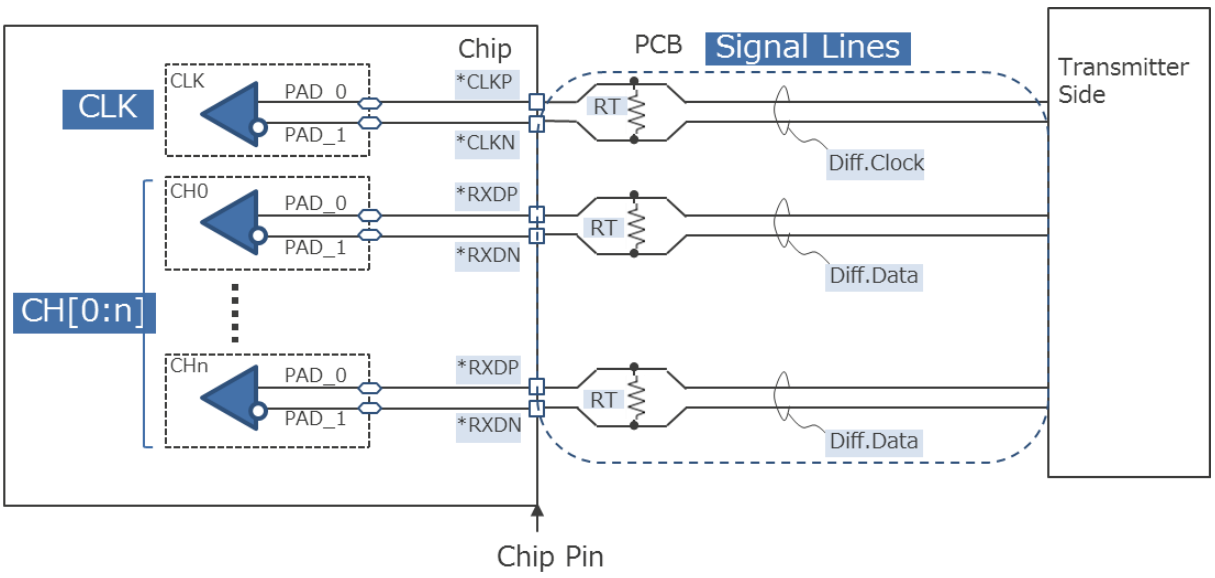


Figure 1.1 Connection Example of LVDS

1.2 PCB guideline

Items		Guidelines	Fig.	Notes
Line impedance		★: Differential 100Ω±20%	―	1
Line length difference	b/w Diff. Clock and Diff. Data	★ : As same length as possible	―	2
	b/w each pos. and neg.	★ : Line length is as short as possible		
Line bending		Recommended :external angle 45° （Prohibition:>45° ）	―	3
Line layer Numbers of via	b/w Diff. Clock and Diff. Data	Same layer ※Recommended :top layer without any vias	―	―
	b/w each pos. and neg.	Same via number（number is as few as possible）		
Line spacing	b/w each pos. and neg.	S（min. of PCB design criterion）	1.2.①	4
	b/w Diff. and next Diff.	≧3S ※when there is no GND shield	1.3.⑥	
	b/w Diff. and GND shields	≧S ※placed GND shields in both sides of Diff.	1.2.②	
	b/w Diff. and other high speed / low speed signal	≧3S ※it is unnecessary when there are GND shields	―	
	b/w Diff. and Continuous Ground Plane	≧S	1.2.③	
Line width		≧S	1.2.④	
Return path		★ : Placed Continuous Ground Plane under Diff.	1.2.⑤	5
		Placed gnd through-hole next to signal through-hole Placed gnd vias symmetrically next to Diff.	―	

★Please be designed with the highest priority.
Note1: Time domain reflectometry (TDR) measurement condition:
Example: Transition time of rise and fall(TRF)=0.5ns@350mV
Note2: This is guideline to reduce the line skew.
Note3: Do not bend at an acute angle. Bend as arc.
Note4: These sizes are reference. These can be changed to the designer side actual value.
Note5: Ensure a sufficient Ground Plane width for signal lines width.

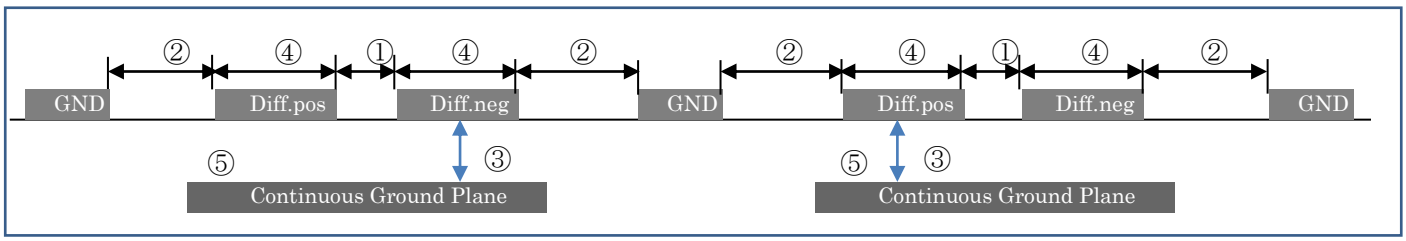


Figure 1.2 Example of Signal Line 1

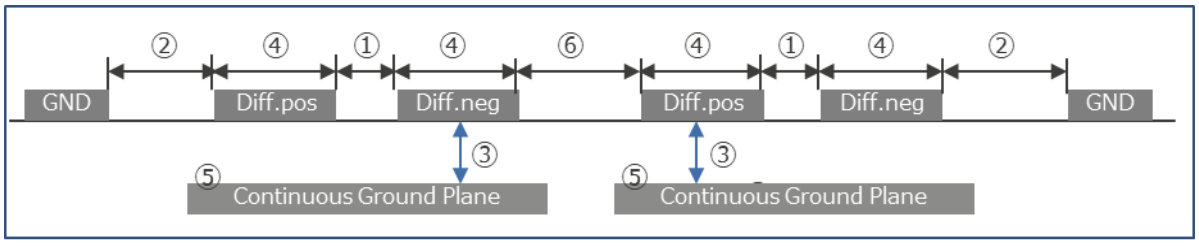


Figure 1.3 Example of Signal Line 2

2. Guideline of LVDS power line

2.1 Topology

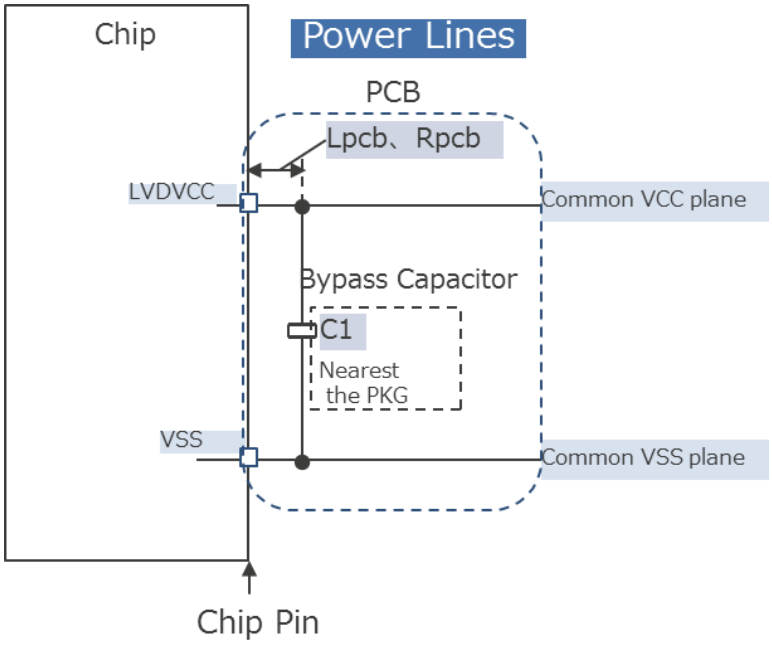


Figure 2.1 Connection Example of Power Wiring

2.2 PCB guideline

Supply the power from LVDVCC with the ground as the common VSS plane of the PCB.

Items	Power line	Notes
Rpcb	≦30mΩ	—
Lpcb	≦2.8nH/5ch	1, 2
C1 (Nearest the chip)	0.1uF	3, 4

Note1 Please calculate the value depending on the number of channels (N).

Example：N = 4（CLK、CH0、CH1、CH2）→ Lpcb＝2.8nH×5/N＝3.5nH

Note2 Be as small as possible the power line inductance to C1 from the CHIP pins. refer to Section 2.3 “Concept of Loop inductance”.

Note3 Place C1 nearer the CHIP pins to prevent the ripple noise by transient current. Place bypass capacitor between the respective power supply planes and solder balls for VSS pin.

Note4 0.1uF is a reference value. Please determine the optimum capacitance value by evaluation.

Note5 Please reduce the potential difference of GND between transceiver and receiver as small as possible. Because the potential difference of GND causes the potential difference of common-mode voltage (VCM) of transceiver and VCM of receiver. Please make a sufficient margin against the specification of the interface to use.

Note6 If the product doesn’t have LVDS dedicated power supply pin, please refer to User Manual and Application Note of the product.

2.3 Concept of loop inductance

The target inductance can be obtained by calculating loop inductance from the *VCC ball of the package to the VSS balls of the package taken as an ideal GND in the way shown in the figure below. In this case, include the equivalent series inductance (ESL) component of the bypass capacitor placed close to the LSI chip.

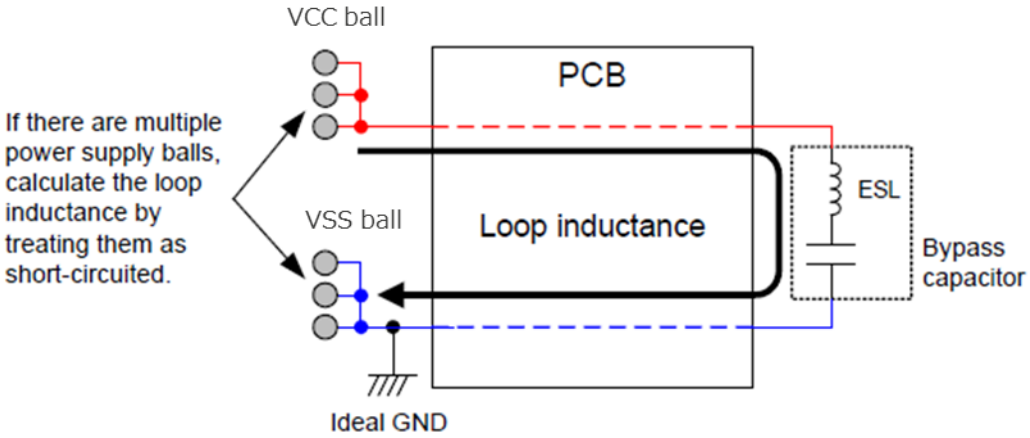


Figure 2.2 Loop Inductance

3. Serial Gigabit Media Independent Interface (SGMII)

The differential pair signals (Data, Clock) of SGMII are DC balanced signals. Thus, DC coupling and AC coupling can be used as a coupling method between MCU and PHY. The following section explains regarding each coupling method.

3.1 Connection Example of SGMII

3.1.1 Connection Example with DC Coupling

Figure 3.1 shows a connection example with DC coupling. The termination resistor (Rin) is implemented in the Rx pin of MCU, therefore external resistor is unnecessary when DC coupling. The following figure is an example in case the termination resistor is implemented in PHY.

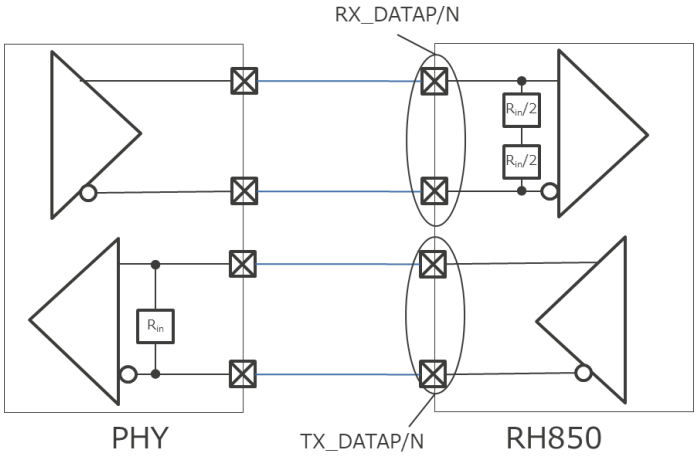


Figure 3.1 Connection Example with DC Coupling

3.1.2 Connection Example with AC Coupling

Figure 3.2 shows a connection example with AC coupling. The termination resistor (Rin) and the circuit for AC coupling are implemented in the Rx pin of MCU, therefore it has to put only capacitor when AC coupling. The following figure is an example in case the termination resistor and the circuit for AC coupling are implemented in PHY.

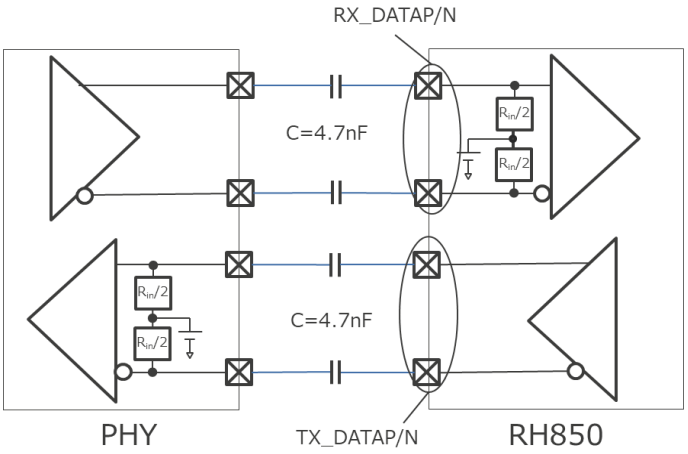


Figure 3.2 Connection Example with AC Coupling

3.1.3 Connection Example with DC Coupling（U2A-EVA）

Figure 3.3 shows a connection example with DC coupling. U2A-EVA does not have a Clock Data Recovery (CDR) circuit. Therefore, the clock input of 625MHz from PHY to RX_CLKP/N pins is required. The termination resistor (Rin) is implemented in the Rx pin of MCU, therefore the external resistor is unnecessary when DC coupling. The following figure is an example in case the termination resistor is implemented in PHY.

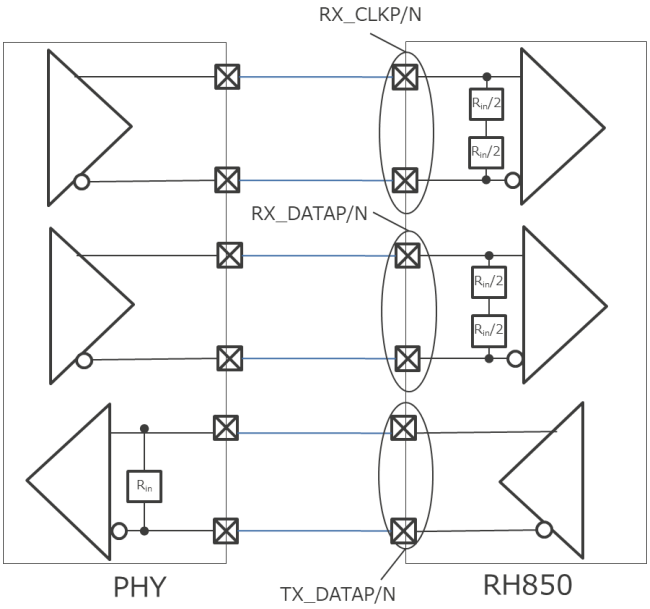


Figure 3.3 Connection Example with DC Coupling (U2A-EVA)

3.1.4 Connection Example with AC Coupling（U2A-EVA）

Figure 3.4 shows a connection example with AC coupling. U2A-EVA does not have a Clock Data Recovery (CDR) circuit. Therefore, the clock input of 625MHz from PHY to RX_CLKP/N pins is required. The termination resistor (Rin) and the circuit for AC coupling are implemented in the Rx pin of MCU, therefore it has to put only capacitor when AC coupling. The following figure is an example in case the termination resistor and the circuit for AC coupling are implemented in PHY.

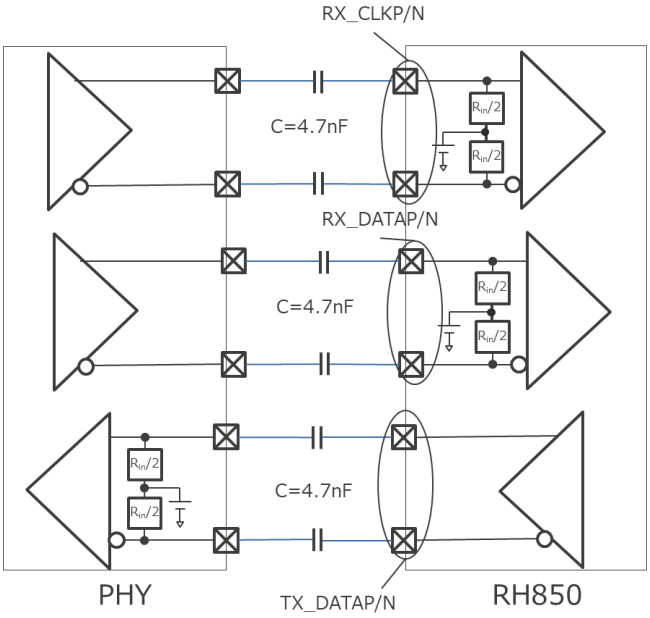
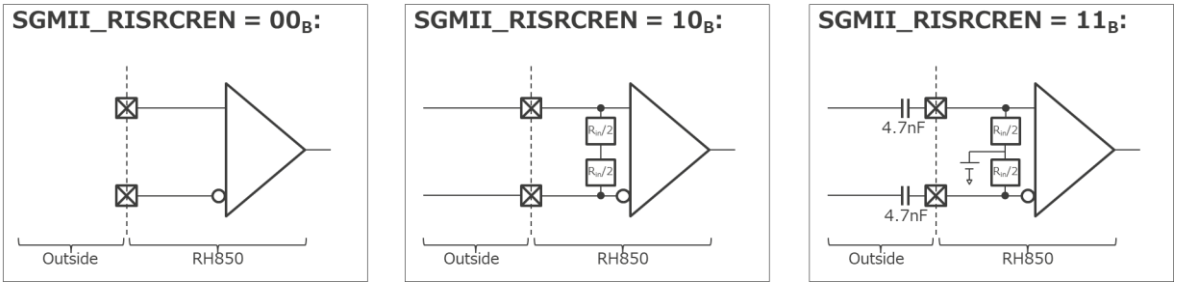


Figure 3.4 Connection Example with AC Coupling (U2A-EVA)

3.2 Usage notes for SGMII

3.2.1 Connection

- It is recommended to confirm the characteristics by using IBIS model including the MCU, the PHY and transmission line.
- It is recommended to place the MCU and the PHY adjacently (less than 15cm).
- The guideline of PCB is same as LVDS. Please refer to the guideline on Chapter 1 and Chapter 2.
- It is recommended to locate external capacitors for AC coupling adjacent to the receiver.
- SGMII on RH850 communicates with LVDS. Therefore, please confirm that the specification of the PHY fulfills the characteristics such as the Output Differential Voltage (VOD) described in the datasheet for RH850.
- Although the recommended value of external capacitors for AC coupling is 4.7nF, please confirm that the input voltage range (Vi), the input differential threshold (Vidth) and Jitter are fulfilled by the simulation using IBIS model in case the other value is specified for the PHY.
- The signal speed deviation of the PHY should be less than ±100ppm.
- SGMII on RH850 (excluding U2A-EVA) has the function to invert the polarity of Pos/Neg pins. Please use according to the usage conditions.
- Please set the coupling method for Rx pin to the option byte SGMII_RISRCREN according to the usage conditions.



SGMII Unused (Hi-Z) DC Coupling AC Coupling

Figure 3.5 Setting Example of Rx pin state

3.2.2 Reference clock input (REFCLK)

- It is possible to select the external clock input from REFCLK or the internal clock from Main OSC (using crystal resonator).
- Please confirm that the clock fulfills the deviation (less than ±100ppm) taking into consideration the temperature deviation.
- In case of using the internal clock, please consult with the crystal resonator manufacturer regarding the evaluation of frequency deviation in addition to the general oscillation characteristics (negative resistance, drive level, etc) on the actual product board.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Apr.15.21	-	Initial version
1.10	Apr.01.22	1	Add U2A6 in target device

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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