RH850/U2A-EVA Group

Test Mode Procedure (CAN FD Mode)

Summary

This application note explains the procedure example when performing RS-CANFD module test in the RH850/U2A series of automotive single-chip microcontrollers from Renesas Electronics (hereafter referred to as U2A).

These documents and programs are intended to understand the RH850/U2A built-in function, and are not intended for mass production design

Aim of this document and software is to provide supplemental information for the function on RH850/U2A. It is not intended to implement in the design for mass production.

There is no guarantee to update in this document and software to reflect the latest manual, errata, technical update, and development environment. You are fully responsible for the incorporation or any other use of the information of this document in the design of your product or system, and please refer to latest manual, errata, technical update, and development environment.

Target Device

- RH850/U2A-EVA Group

Target Integrated Development Environment

CS+(from Renesas Electronics)

Version :V8.07.00

Device file :DR7F702300.DVF

:DR7F702301.DVF

:DR7F702302.DVF

Reference Document

RH850/U2A-EVA User's Manual: Hardware

For function details and electrical characteristics, please refer to "User's Manual: Hardware".

This application note is based on the following manual.

- RH850/U2A-EVA User's Manual (Rev.1.20): R01UH0864EJ01200

The register name in this text omits "RSCFDnCFD".

Contents

1. Test Functions

RH850/U2A-EVA Group have the following test functions. These functions can be used to perform self-tests of the CAN communication by CAN transceiver and MCU, and self-tests of RAM. Refer to the next chapters for each processing details.

- 2. Communication Test Functions
  - ・2.1 Standard Test Mode (CRC Test)
  - ・2.2 Listen-only Mode
  - ・2.3 Self-Test Mode (Loopback Mode)
  - ・2.4 Restricted Operation Mode (Only in CAN FD Mode)
  - ・2.5 Inter-channel Communication Test
- 3. RAM Test Function
- 4. Bus Traffic Measurement Function

2. Communication Test Functions

2.1 Standard Test Mode (CRC Test)

When enabling the communication test mode (the CTME bit in CmCTR register is ”1”), the CRC value calculated based on sent or received message can be read from the register storing the CRC calculation data. Also, when disabling the communication test mode (the CTME bit in CmCTR register is ”0”), the CRC calculation data is always read as “0”.

The registers to read the CRC calculation data are shown below.

・Classical CAN frame: CRCREG[14:0] bits in CmERFL register

・CAN FD frame: CRCREG[20:0] bits in CmFDCRC register

The inter-channel communication test mode allows communication between channels inside the MCU. Therefore, the CRC calculation circuit can be tested on the MCU alone by comparing the CRC calculation data of the transmit channel with the CRC calculation data of the receive channel. Refer to “2.3.3 Self-Test Mode Setting Procedure” for the inter-channel communication test.

Figure 2-1 shows the CRC test image diagram.

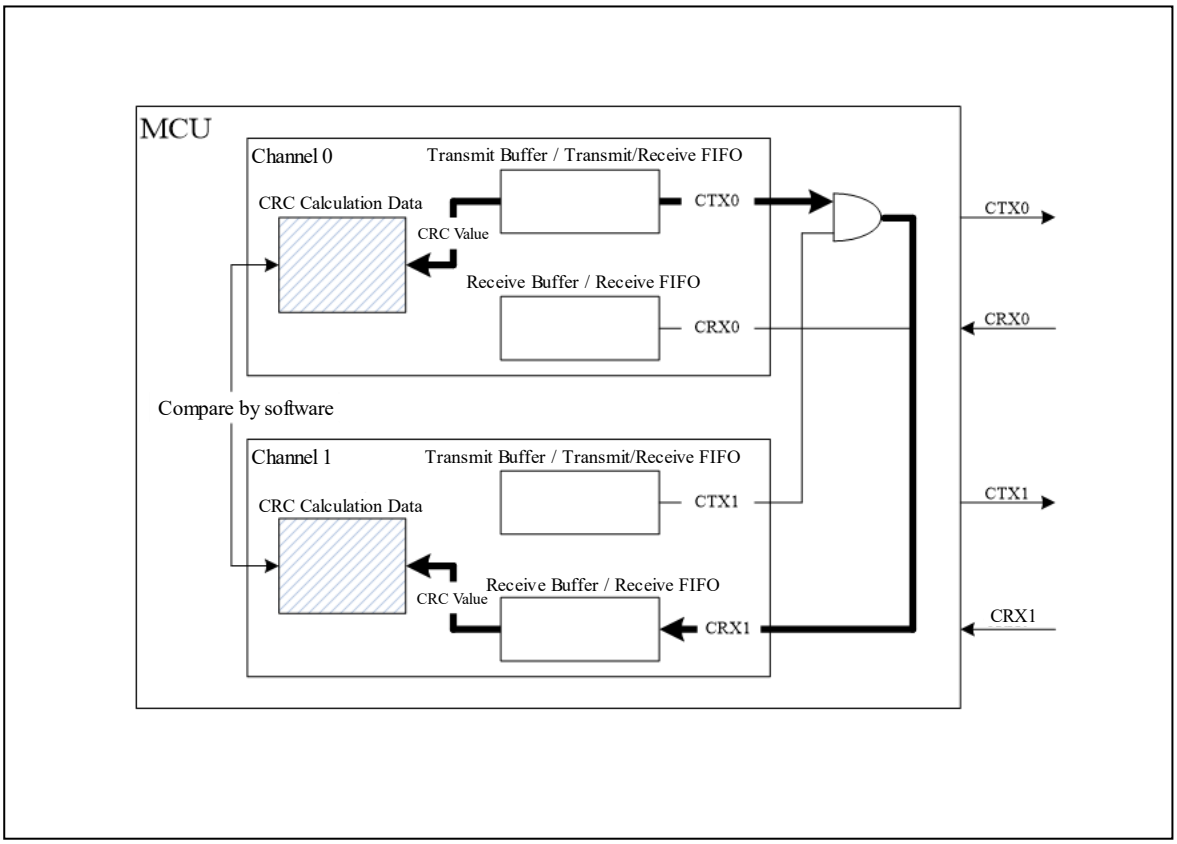
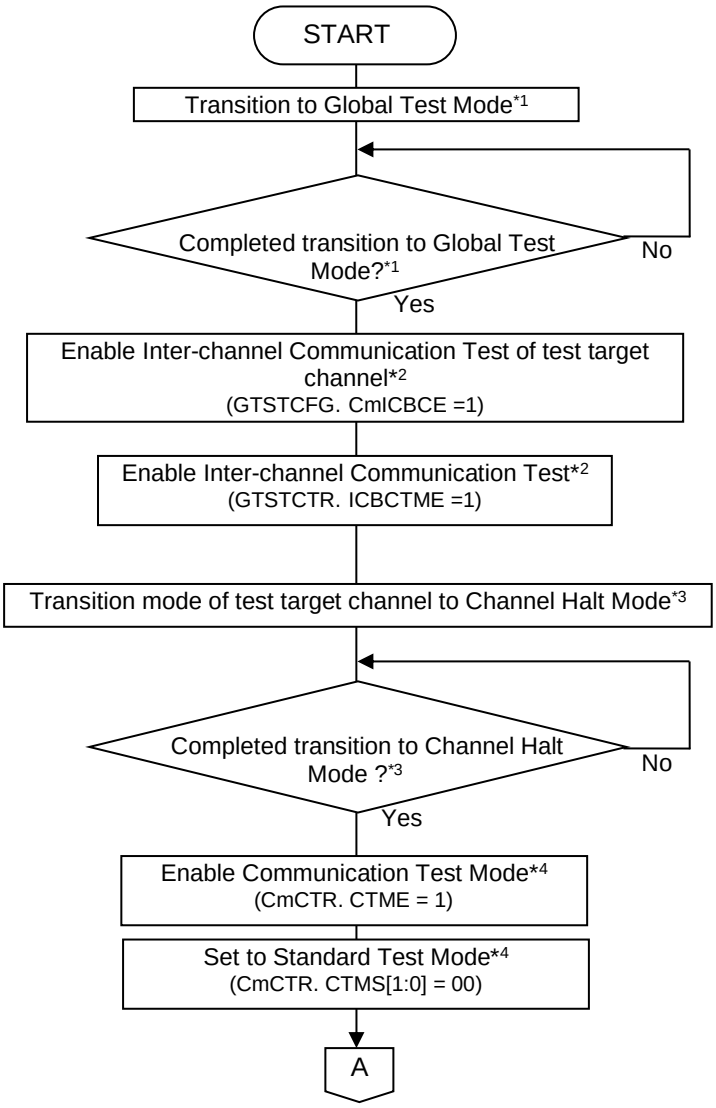


Figure **2-1** CRC Test Image(When between Channel 0 and 1)

2.1.1 Standard Test Mode Setting Procedure

Figure 2-2 to Figure 2-4 show the setting procedure of the standard test mode



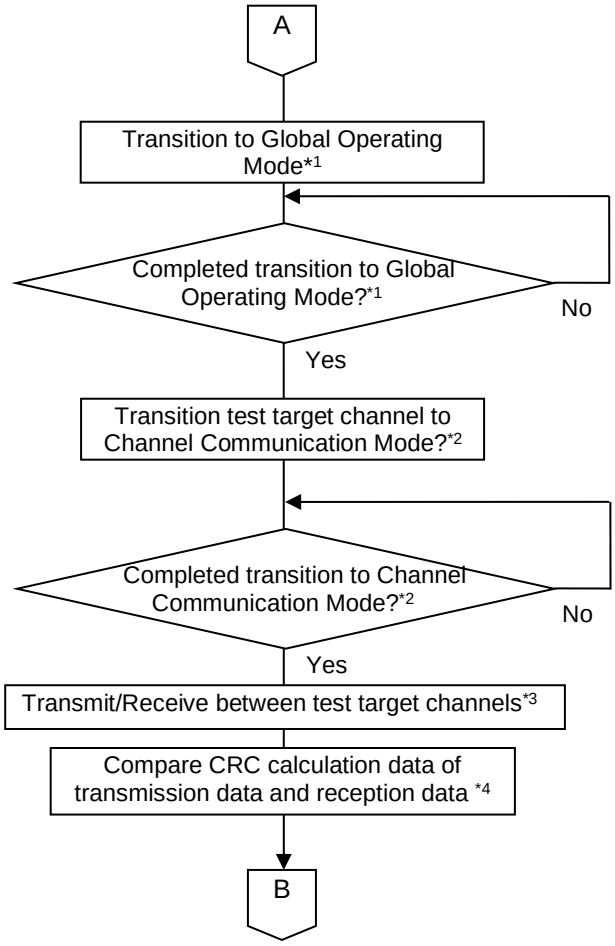
Note 1. When changing the global mode (the GSLPR bit and GMDC[1:0] bits in the GCTR register), confirm with the GSTS register that the mode has been switched. Do not change the mode selection bit until the mode is switched.

Note 2. Rewrite the CmICBCE bit and ICBCTME bit in the Global Test Mode.

Note 3. When changing the channel mode (the CSLPR bit and CHMDC[1:0] bits in the CmCTR register), confirm with the CmSTS register that the mode has been switched. Do not change the mode selection bit until the mode is switched.

Note 4. Rewrite the CTMS [1:0] bits and CTME bit in the CmCTR register in Channel Halt Mode.

Figure 2-2 Standard Test Mode Setting Procedure 1



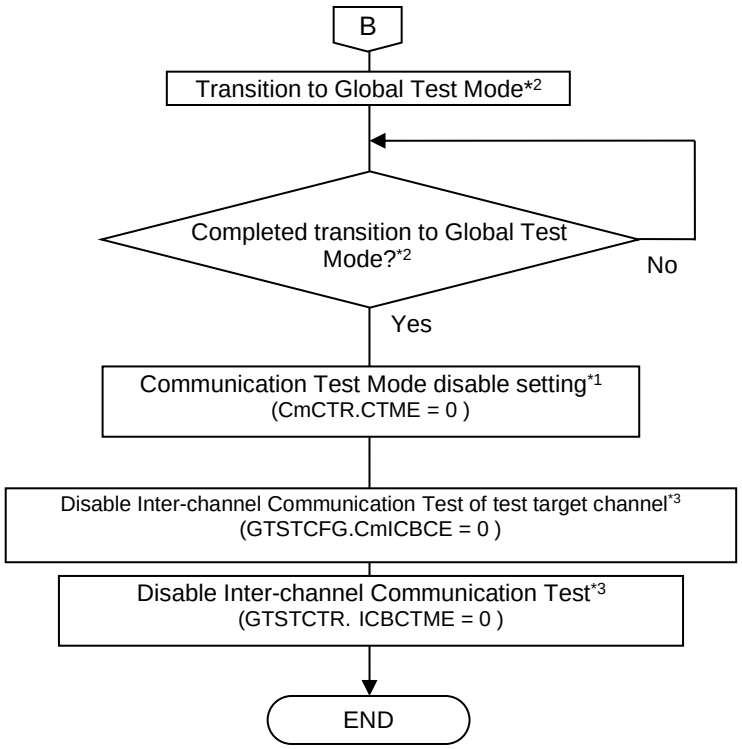
Note 1. When changing the global mode (the GSLPR bit and GMDC[1:0] bits in the GCTR register), confirm with the GSTS register that the mode has been switched. Do not change the mode selection bit until the mode is switched.

Note 2. When changing the channel mode (the CSLPR bit and CHMDC[1:0] bits in the CmCTR register), confirm with the CmSTS register that the mode has been switched. Do not change the mode selection bit until the mode is switched.

Note 3. Configure the transmit/receive settings for the channels to be tested.

Note 4. When the Communication Test Mode is enabled (CmCTR.CTME = 1), the CRC calculation data can be checked by the CRCREG [14:0] bits in the CmERFL register in Classical CAN Frame and the CRCREG [20:0] bits in the CmFDCRC register in CANFD frame. When the transmission test mode is disabled (CmCTR.CTME = 0), the CRCREG [14:0] bits in the CmERFL register and CRCREG[20:0] bits in the CmFDCRC register always become “0”.

Figure 2-3 Standard Test Mode Setting Procedure 2



Note 1. Rewrite the CTME bit in the CmCTR register in the Channel Halt Mode.
Note 2. When changing the global mode (the GSLPR bit and GMDC[1:0] bits in the GCTR register), confirm with the GSTS register that the mode has been switched. Do not change the mode selection bit until the mode is switched.
Note 3. Rewrite the CmICBCE bit and ICBCTME bit in Global Test Mode.

Figure 2-4 Standard Test Mode Setting Procedure 3

2.2 Listen-only Mode

In Listen-only Mode, only recessive bits are transmitted on the CAN bus. The ACK bit, overload flag, and active error flag are not transmitted. Both data frame and remote frame can be received. Therefore, Listen-only Mode can be used for bus monitoring, communication speed detection, etc.

Do not transmit in Listen-only mode (do not make transmit request to the transmit/receive FIFO buffer, transmit buffer, and transmit queue).

Figure 2-5 shows the connection when selecting Listen-only Mode.

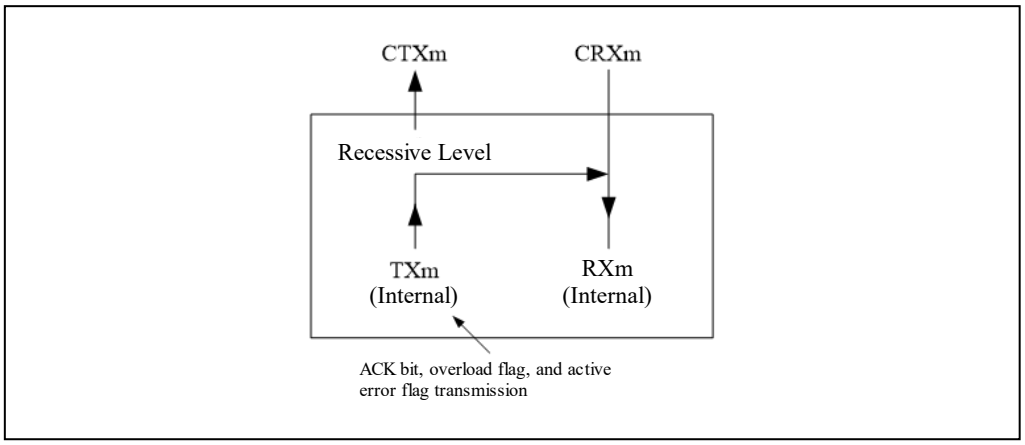
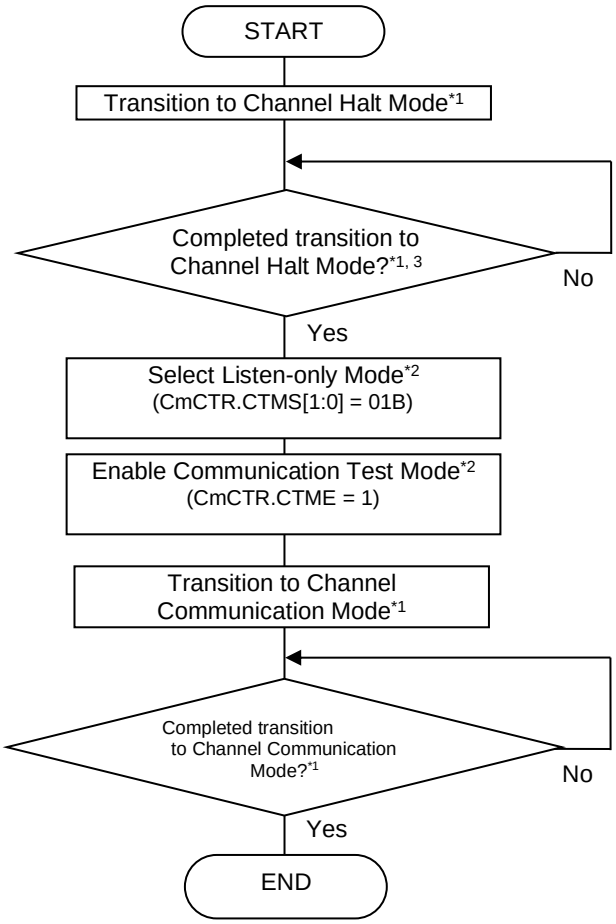


Figure 2-5 Connection when Selecting Listen-only Mode

2.2.1 Listen-only Mode Setting Procedure

Figure 2-6 shows the setting procedure of Listen-only Mode.



Note 1. When changing the channel mode (the CSLPR bit and CHMDC[1:0] bits in the CmCTR register), confirm with the CmSTS register that the mode has been switched. Do not change the mode selection bit until the mode is switched.

Note 2. Rewrite the CTMS [1:0] bits and CTME bit in the CmCTR register in Channel Halt Mode.

Note 3. Configure the reception settings for the channel to be used in Listen-only Mode, as necessary.

Figure 2-6 Listen-only Mode Setting Procedure

2.3 Self-Test Mode (Loopback Mode)

In Self-Test Mode, the messages transmitted from own node are compared with the receive rules, and messages that have passed the filtering processes are stored in the buffer.

Messages transmitted from other CAN nodes are compared only with the reception rules for messages transmitted from other CAN nodes (GAFLIDj.GAFLLB=0).

If the mirror function and self-test mode are enabled at the same time, the self-test mode setting takes precedence.

Table 2-1 Reception Rule Comparison in Self-test Mode

Reception Rule Target Message	Message Transmit Node	Comparison with Reception Rule
GAFLIDj.GAFLLB = 0	Other node	Compare
	Own node	Compare
GAFLIDj.GAFLLB = 1	Other node	No compare
	Own node	Compare

2.3.1 Self-test Mode 0 (External Loopback Mode)

In Self-Test Mode 0, the loopback test of the channel including the CAN transceiver is performed.

In this mode, the messages transmitted from own node are received via the CAN transceiver and are stored according to the reception rule. Also, an ACK bit is generated to receive the messages transmitted form own node.

Figure 2-7 shows the connection when selecting Self-Test Mode 0.

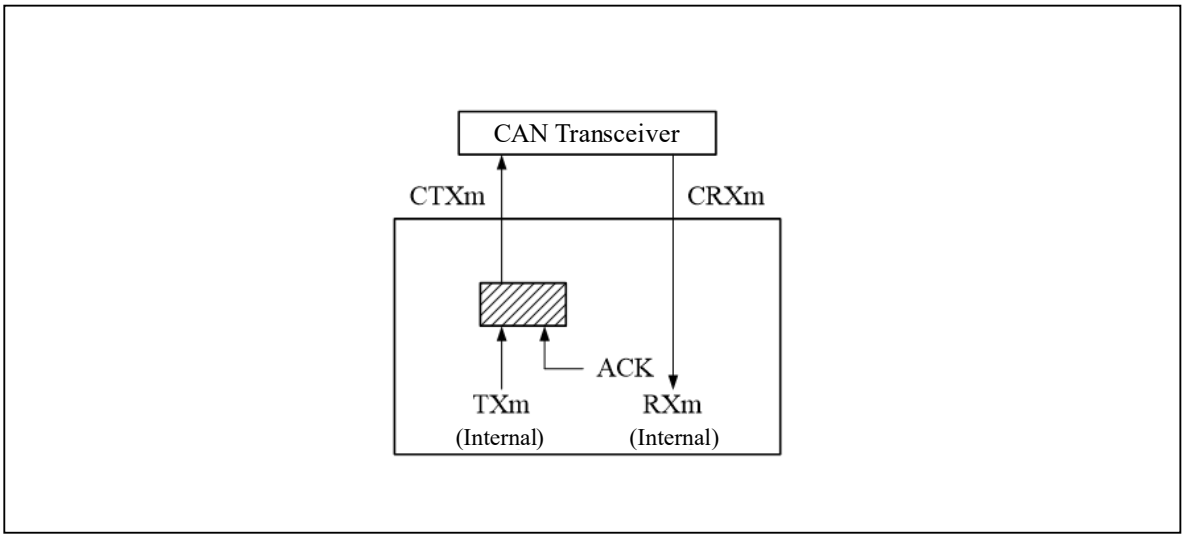


Figure 2-7 Connection when Selecting Self-Test Mode 0

2.3.2 Self-Test Mode 1 (Internal Loopback Mode)

In Self-Test Mode 1, the loopback test of the channel is performed inside MCU.

In this mode, the messages transmitted from own node are received via MCU internal port. The receive messages are stored according to the reception rule. Also, an ACK bit is generated to receive the message transmitted form own node.

In this test, only the internal feedback from the internal TX to the internal RX of the channel is performed. The external CTX pin and external CRX pin are disconnected from the internal pins, and the external CTX pin outputs a recessive bit (CAN transceiver is not used.)

Figure 2-8 shows the connection when selecting the Self-Test Mode 1.

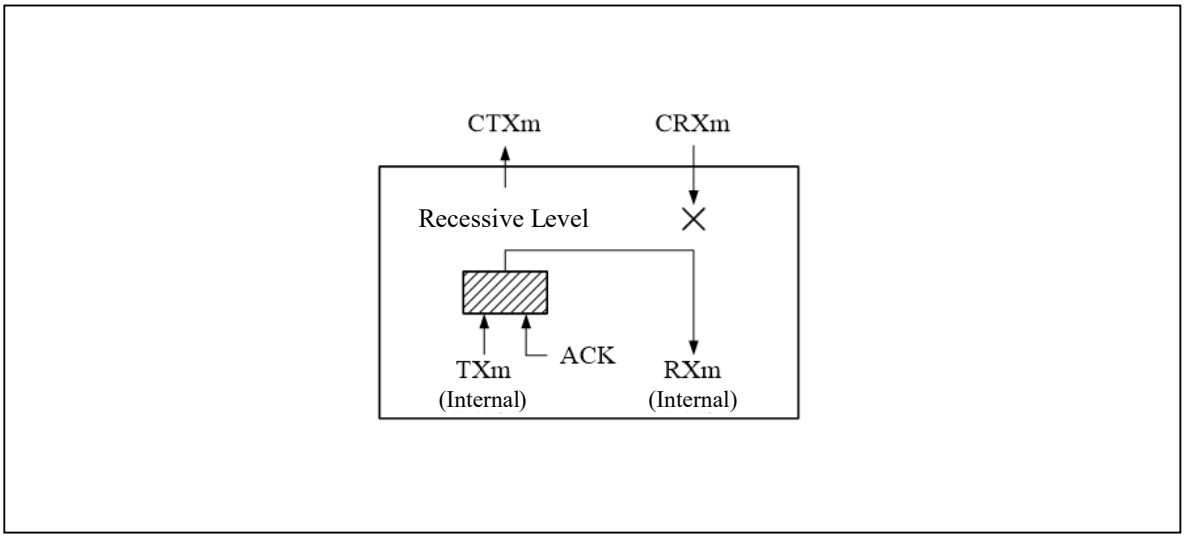
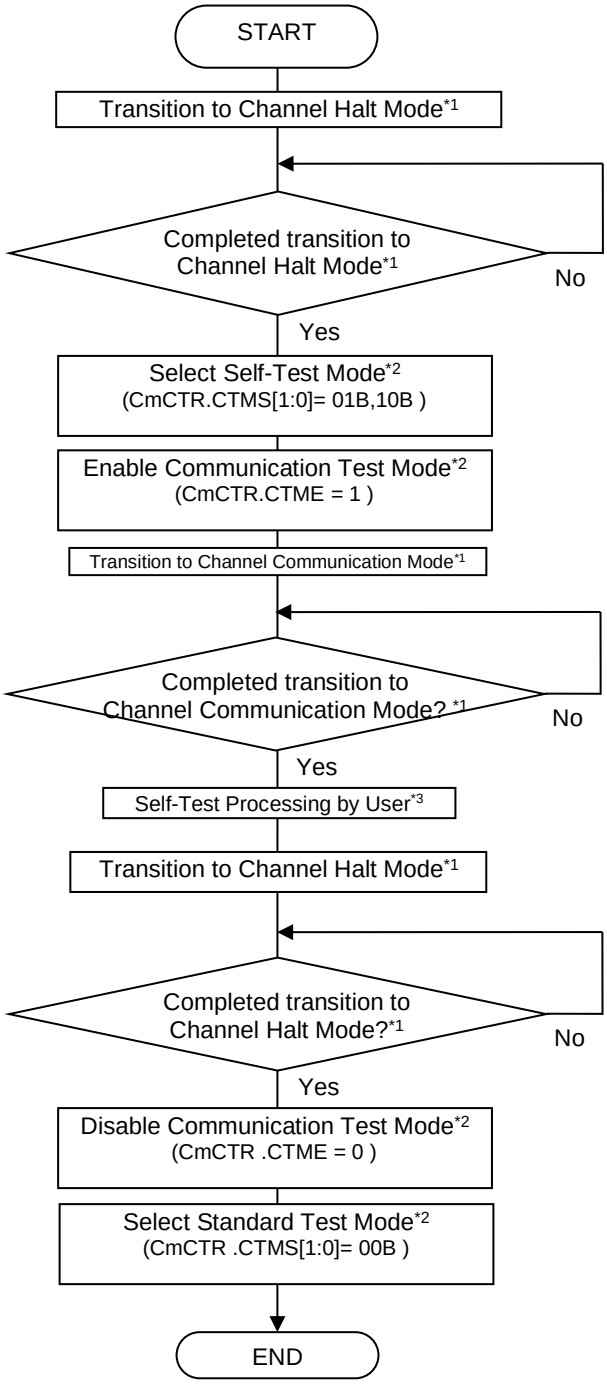


Figure 2-8 Connection when selecting Self-Test Mode 1

2.3.3 Self-Test Mode Setting Procedure

Figure 2-9 shows the setting procedure of Self-Test Mode.



Note 1. When changing the channel mode (the CSLPR bit and CHMDC[1:0] bits in the CmCTR register), confirm with the CmSTS register that the mode has been switched. Do not change the mode selection bit until the mode is switched.

Note 2. Rewrite the CTMS [1:0] bits and CTME bit in the CmCTR register in Channel Halt Mode.

Note 3. Configure the transmit/receive settings for the channels to be tested.

Figure 2-9 Self-Test Mode Setting Procedure

2.4 Restricted Operation Mode (Only in CAN FD Mode)

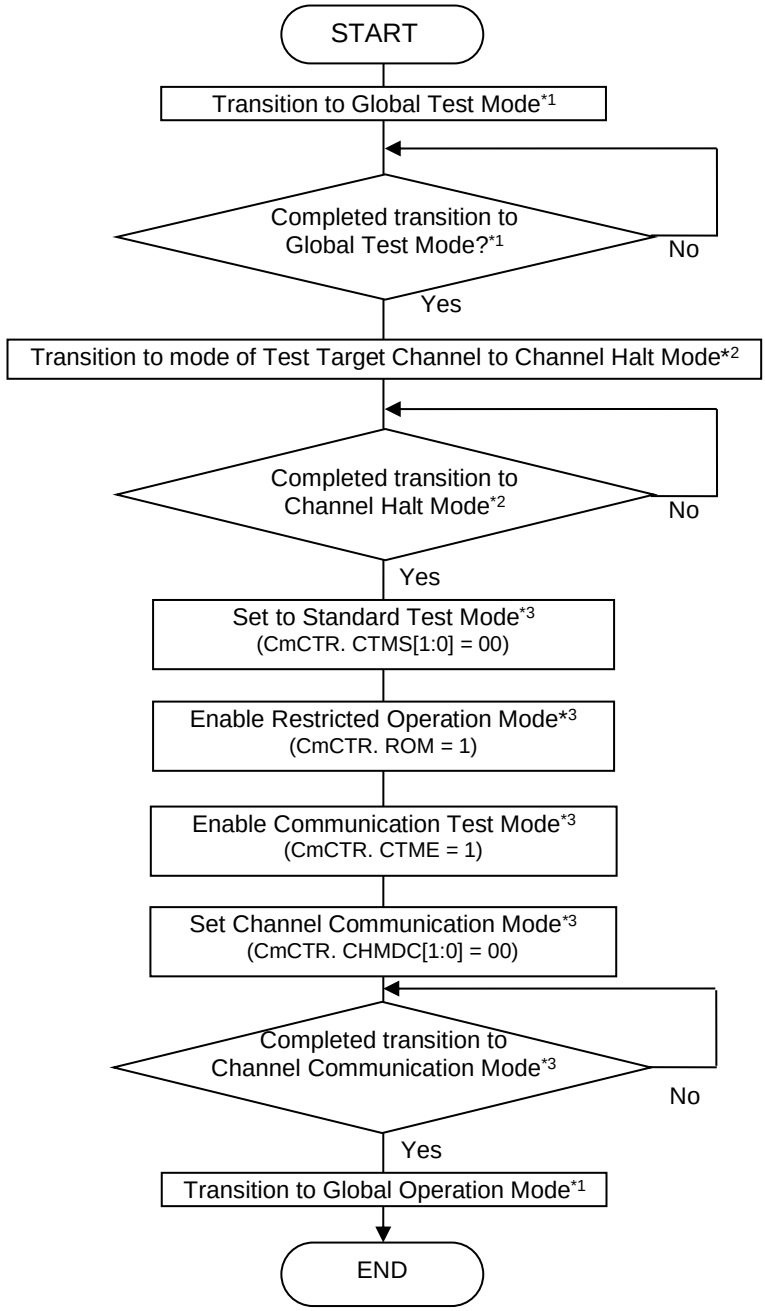
In Restricted Operation Mode, the ACK bit is generated when a valid data frame or remote frame is received, but even if an error frame or overload frame transmission condition is detected, these frames are not transmitted. When the conditions are detected, operation is suspended until the bus idle state comes for resynchronization with the CAN communication. The receive error counter (REC) and the transmit error counter (TEC) do not change with the occurrence of errors.

Use the restricted operation mode only in the standard test mode (the CTMS [1:0] bits in the CmCTR register are “00B”).

For transmission, any transmission request can be made without restrictions.

2.4.1 Restricted Operation Mode Setting Procedure

Figure 2-10 shows the setting procedure of the restricted operation mode



Note 1. When changing the global mode (the GSLPR bit and GMDC[1:0] bits in the GCTR register), confirm with the GSTS register that the mode has been switched. Do not change the mode selection bit until the mode is switched.

Note 2. When changing the channel mode (the CSLPR bit and CHMDC[1:0] bits in the CmCTR register), confirm with the CmSTS register that the mode has been switched.

Note 3. Rewrite the CTMS [1:0] bits, ROM bit and CTME bit in the CmCTR register in Channel Halt Mode.

Figure 2-10 Restricted Operation Mode Setting Procedure

2.5 Inter-channel Communication Test

The inter-channel communication test function allows communication test by internally connecting CAN channels to each other.

In this test, only internal feedback is performed from the channel's internal CTXm pin to the CRXm pin. The external CRXm and external CTXm pins are disconnected from the internal pins, and the external CTXm pin outputs the recessive bit (CAN transceiver is not used.)

Perform the transmission/reception setting for each channel, and then start transmission/reception in the channel communication mode. Refer to “2.1.1 Standard Test Mode Setting Procedure” for the setting procedure.
Using the inter-channel communication function and standard test mode, the CRC calculation circuit can be tested. Refer to “2.1 Standard Test Mode (CRC Test)” for the CRC test details. Figure 2-11 shows the inter-channel communication test connection diagram.

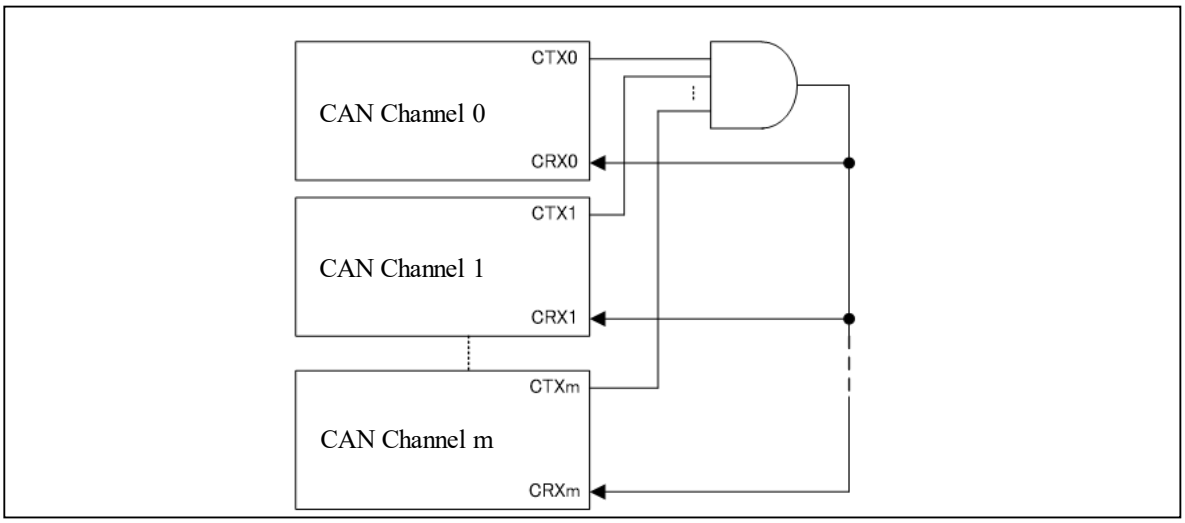


Figure 2-11 Inter-channel Communication Test Connection Diagram

3. RAM Test Function

3.1 RAM Read/Write Test

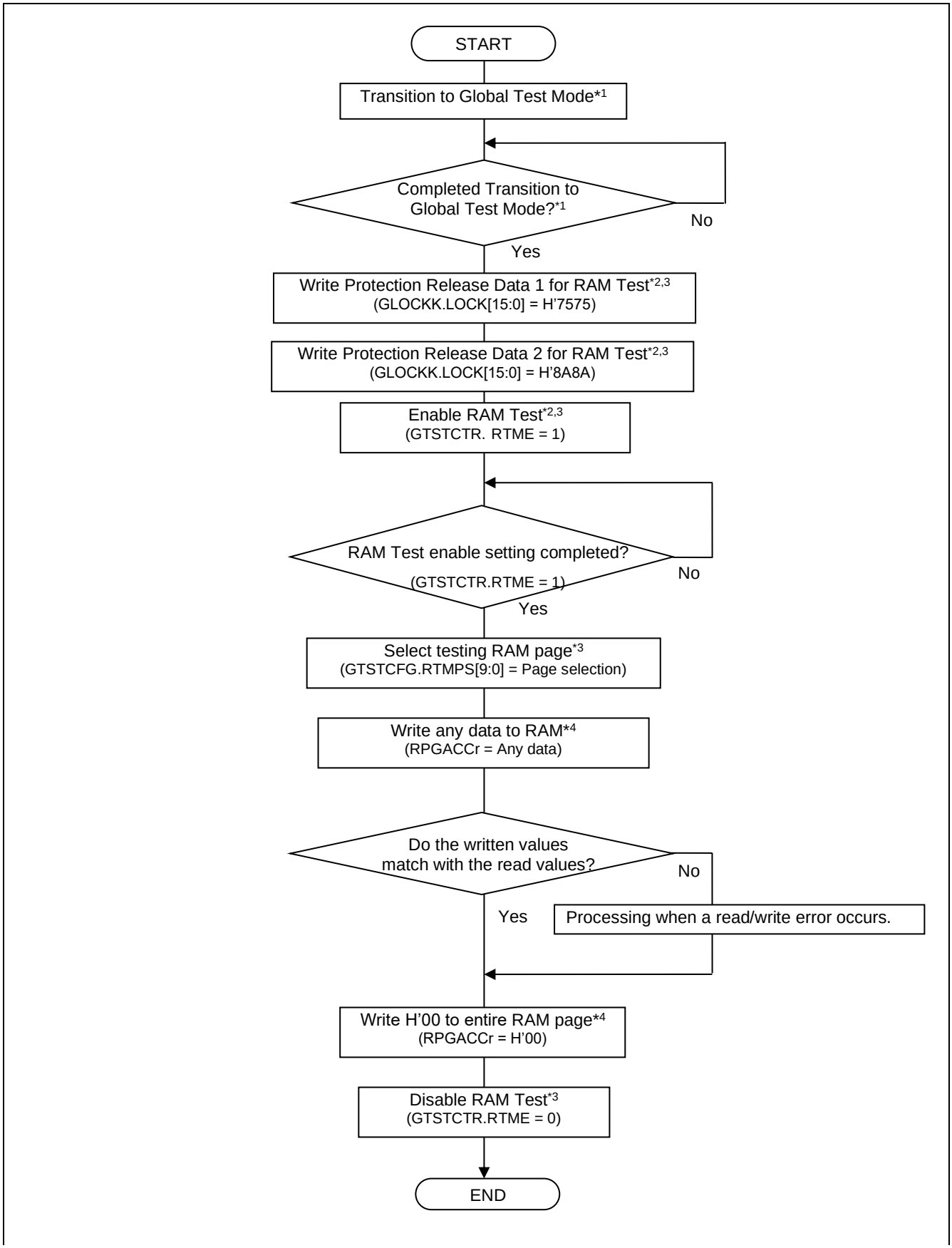
When the RAM test is enabled (GTSTCTR.RTME = 1), the RAM Read/Write Test can be performed on the entire RAM for CAN.

When using the RAM test function, the RAM is divided into pages of 256 bytes each, and set the page selection by the RTMPS [9:0] bits in the GTSTCFG register. RAM in pages can be read/written by the RPGACCr register.

By comparing the value written to the entire RAM for CAN with the value read back, it can be confirmed that the RAM is normal. Also, write “H’00” to the RAM for CAN after performing the RAM Read/Write Test.

3.2 RAM Test Setting Procedure

Figure 3-1 shows the setting procedure of RAM Test (RAM Read/Write Test).



Note 1. When changing the global mode (the GSLPR bit and GMDC[1:0] bits in the GCTR register), confirm with the GSTS register that the mode has been switched. Do not change the mode selection bit until the mode is switched.

Note 2. Be sure to execute the instructions to write protection release data 1 and 2 for the test function to GLOCKK.LOCK[15:0] bits and the instruction to enable the RAM test in succession.

Note 3. Rewrite the LOCK[15:0] bits in the GLOCKK register, the RTME bit in the GTSTCTR register, and the RTMPS bit in the GTSTCFG register in Global Test Mode.

Note 4. Rewrite the RPGACCr register in Global Test Mode and with RAM Test enabled.

Figure 3-1 RAM Test Setting Procedure

4. Bus Traffic Measurement Function

The bus load counter can measure the idle time of the CAN bus using the clkc clock or the clk_xincan clock. Thereby, the CAN bus traffic can be measured from the idle time.

Figure 4-1 shows the bus traffic measurement function overview.

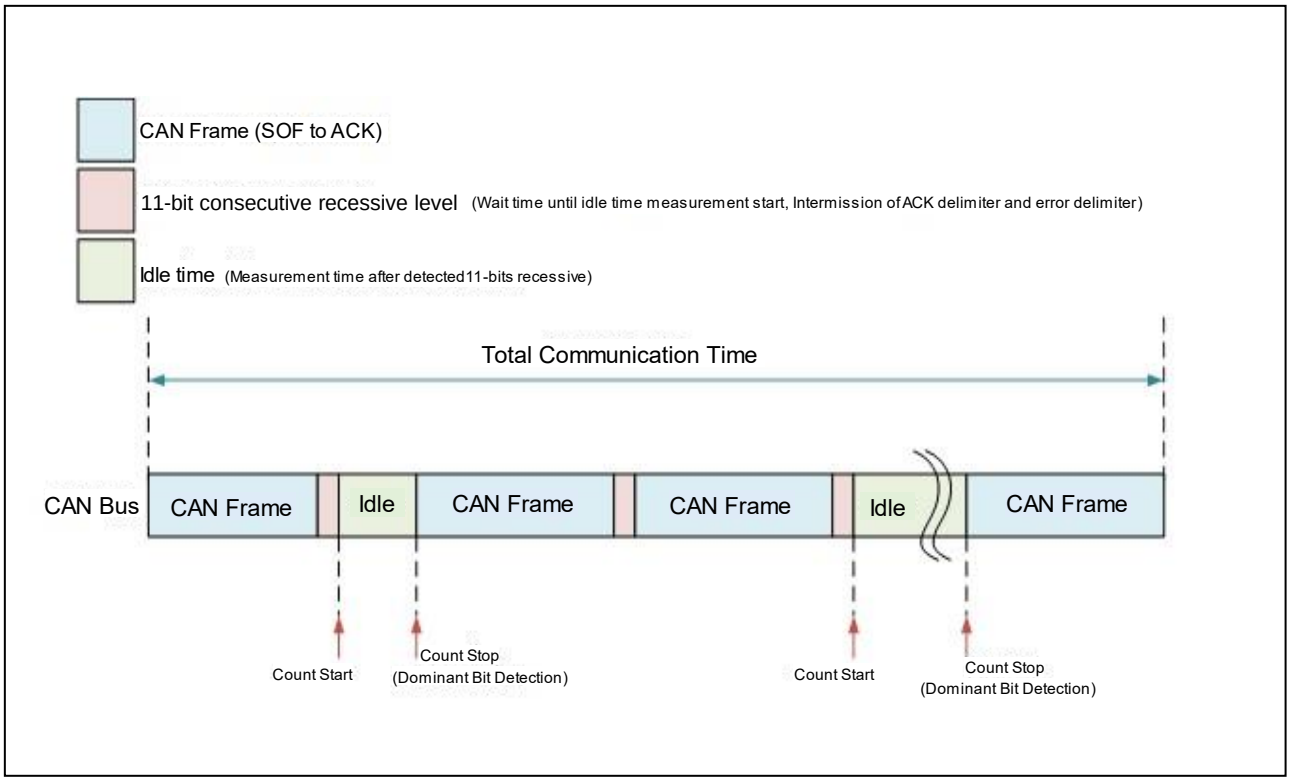


Figure 4-1 Bus Traffic Measurement Function Overview

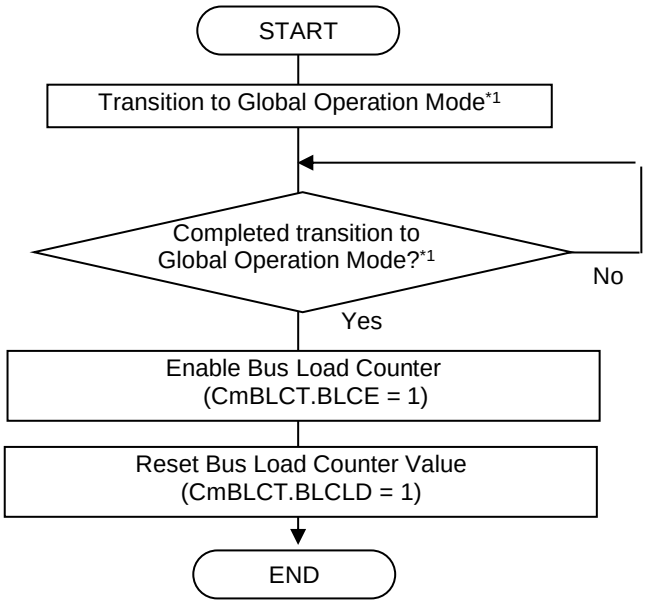
The bus load counter starts counting when the nominal bit in the recessive level is calculated 11 bits consecutively on the CAN bus.

The bus load counter continues counting until it measures a dominant bit on the CAN bus.

The count is stopped when the dominant bit is detected on the CAN bus, and the count is restarted when the nominal bit in the recessive level is measured the 11bits consecutively.

4.1 Bus Traffic Measurement Function Procedure

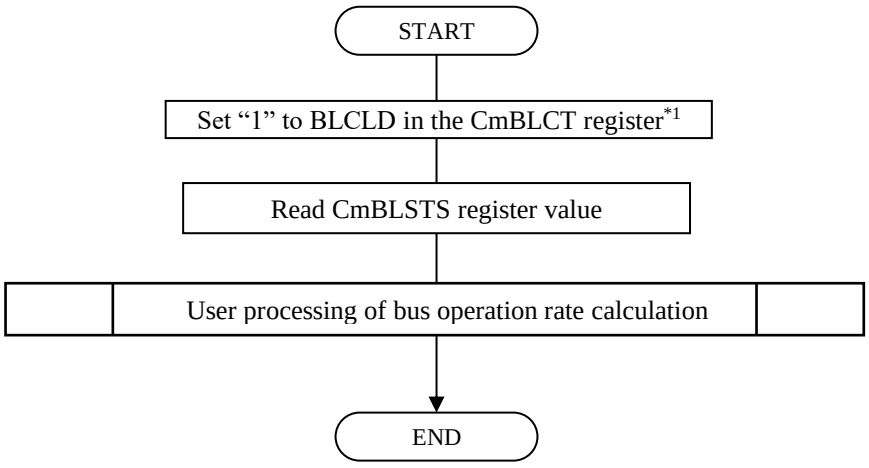
Figure 4-2 shows the setting procedure of the bus traffic measurement function.



Note 1. When changing the global mode (the GSLPR bit and GMDC[1:0] bits in the GCTR register), confirm with the GSTS register that the mode has been switched. Do not change the mode selection bit until the mode is switched.

Figure 4-2 Bus Load Counter Setting Procedure

Figure 4-3 shows the read procedure of the bus load counter.



Note 1. When CmBLCT.BLCLD is set to 1, the counter value is loaded into the CmBLSTS register and the counter is cleared at the same time.

Figure 4-3 Read Procedure of Bus Load Counter

4.2 Bus Operation Rate Calculation Method

The CAN bus operation rate can be calculated by the following formula.

$$\frac{\text{Total Communication Time} - \text{Total Idle Time}}{\text{Total Communication Time}} = \frac{\text{Total Bus Operation Time}}{\text{Total Communication Time}} = \text{Bus Operation Rate}$$

Total idle time: BLC value of BLSTS register × A clock cycle of clkc

Total communication time: Interval time to set BLCLD bit in CmBLCT register.

Calculation Example)

Bit rate: 1Mbps

clkc Clock: 40MHz(25ns)

CmBLCT.BLCLD setting: 1ms cycle

CmBLSTS register value: 4E20H (20000)

$$\frac{\text{Total Communication Time} - \text{Total Idle Time:}}{\text{Total Communication Time}} = \frac{(1000000\text{ns} - 20000 \times 25\text{ns})}{1000000\text{ns}} = 50\%$$

5. Notes on Processing Flow

Refer to “CAN Configuration Application Note” for notes on processing flow.

6. Appendix

6.1 Software Explanations

Module Explanation

The following shows the module list of the sample program for the RAM test.

Table 6-1 Module List

Module Name	Label Name	Function
Main routine	main_pm0	Perform each setting and application start.
PORT setting procedure	PORT_Init	Perform PORT initial setting.
CAN initial setting procedure	R_CAN_Init	Perform CAN initial setting.
Global test start function	R_CAN_Global _TestStart	Perform Global Test (RAM Test).

Register Setting

The following shows the register setting of each function in the sample program of the RAM test.

Table 6-2 CANFD register setting (1/2)

Register Name	Setting Value	Function
CFDGCFG	0x00001006	・Unused interval timer presccaler ・Select the bit time clock for channel 0 in the time stamp clock source selection. ・Select the bit time clock in the time stamp source selection. ・No time stamp source division. ・Reject the message in message payload overflow. ・Set internal clock (clkc [80MHz]) to CAN clock source selection. ・Mirror mode disables ・DLC exchanges enables ・DLC check enables ・Set ID priority to transmit priority selection
CFDCmNCFG (m=0)	0x061C0C03	Set communication speed to 1 Mbps ・NBRP :3(4BRP) ・NTSEG1:14(15TQ) ・NTSEG2:3(4TQ) ・NSJW :3(4TQ)
CFDCmNCFG (m=1~7)	0x00000000	Not set
CFDCmDCFG (m=0)	0x03030E00	Set communication speed to 4 Mbps ・DBRP :0(1BRP) ・DTSEG1:14(15TQ) ・DTSEG2:3(4TQ) ・DSJW :3(4TQ)
CFDCmDCFG (m=1~7)	0x00000000	Not set
CFDCmFDCFG (m=0~7)	0x00000000	Not set
CFDGAFLCFGv (v=0~3)	0x00000000	Not set
CFDGAFLECTR	0x00000000	Not set
CFDGAFLIDj (j=1~16)	0x00000000	Not set
CFDGAFLMj (j=1~16)	0x00000000	Not set
CFDGAFLP0j (j=1~16)	0x00000000	Not set
CFDGAFLP1j (j=1~16)	0x00000000	Not set
CFDRMNB	0x00000000	Not set

Table 6-3 CANFD Register Setting (2/2)

Register Name	Setting Value	Function
CFDRFCCx (x=0~7)	0x00000000	Not set
CFDCFCCk (k=0~23)	0x00000000	Not set
CFDTMIECy (y=0~15)	0x00000000	Not set
CFDTXQCm (m=0~3)	0x00000000	Not set
CFDGCTR	0x00000002	・No time stamp prescaler counter reset ・Disable GW FIFO message overwrite interrupt ・Disable TXQ message lost interrupt ・Disable TXQ message overwrite interrupt ・Disable payload overflow interrupt ・Disable transmit history buffer overflow interrupt ・Disable FIFO message lost interrupt ・Disable DLC error interrupt ・Disable Global sleep request ・Global mode control keeps current value
CFDGTSTCTR	0x00000004	・Enable RAM Test Mode ・Disable Inter-channel Communication Test
CFDGTSTCFG	0x0XXX0000	・RAM Test Page (For U2A-EVA, U2A16, U2A8: Specify 0_H~364_H) (For U2A6 ch0: Specify 0_H~130_H) ・Disable Inter-channel Communication Test for CAN0 to 7

Revision History

Rev.	Date	Description	
		Page	Summary
1.11	2023.01.23	-	Released English version of R01AN4894JJ0111.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Notice

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